VLA Technical Report No. 49

MODULE T5C BASEBAND DRIVER

W. E. Dumke

December 1980

CONTENTS

1.0 GENERAL DESCRIPTION

The T5C Baseband Driver performs a number of functions. Refer to Block Diagram C13820B3D. First, it amplifies the output of the T4C Baseband Filter module to a level required by the D1 Sampler module input including the cable loss from "D" rack to Screen Room.

Second, the output level is stabilized by a Sample and Hold ALC loop during the time the IF signals are being received at the Central Electronics Room "D" rack at the "Cal Off" period (the time the Front End calibration noise source is turned off). The detector for this level can either be the D1 Sampler Input Level detector (normal operation) or the internal T5C Precision Square Law Detector (used for ALC bench testing). By using the D1 Sampler Detector the level can be more precisely set at the input to the sampler, because the coax cable/filter loss (which varies from "D" rack to "D" rack) is within the loop.

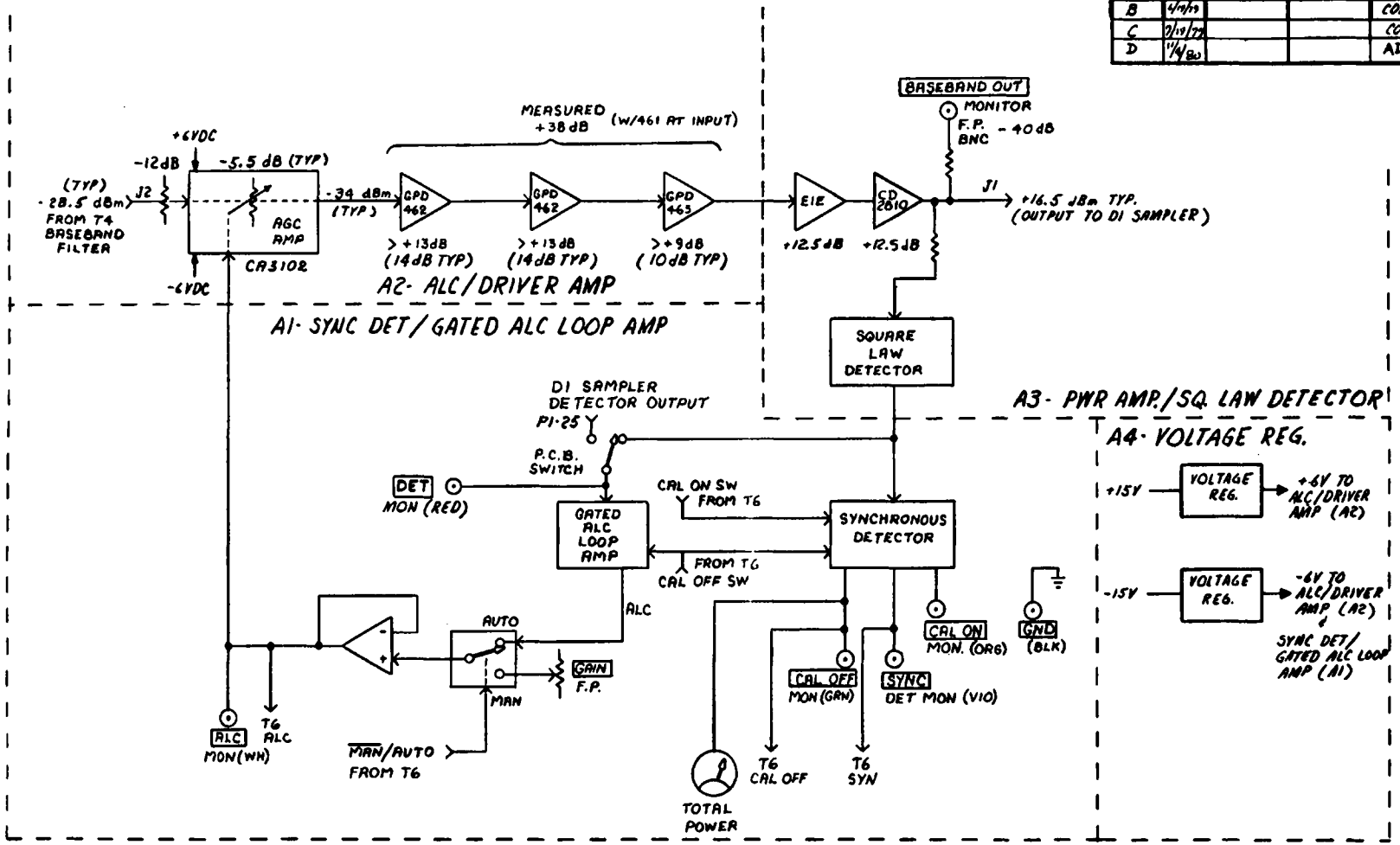
Third, a precision synchronous Square Law Detector in the T5C Baseband Driver is used to derive the "SYN" and "Cal Off" voltages from which the T_{SYS}/T_{CAL} ratio can be calculated after the final analog filtering in the T4C Baseband Filter, for use in the spectral line observing mode. This can be used to calibrate out Front End noise temperature variations and signal/noise ratio variations from the IF transmission system versus frequency. However, IF transmission compression effects must be compensated to assure accuracy.

2.0 CIRCUIT DETAILS

2.1 Module Shielding and Filtering

Refer to module Schematic D13820S1E. Because of the operating frequency range of 200 KHz to 50 MHz in the T4C and T5C baseband system, special precautions had to be taken to insure adequate shielding and filtering to prevent interference from LO and digital signals. Special modules were designed with shielding as the prime concern. To prevent interference from LO signals (5 MHz and above) the module was designed with tight fitting lids (with eleven fastening screws rather than the usual six), and all inputs and outputs filtered,

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	7/1/77			CHG: PWR AMP. GAIN
B	4/11/79			CORRECTED DWG ERROR
C	9/19/79			CORRECTED DWG ERROR
D	11/4/80			ADDED STAGE



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

PROJECT: T5C

TITLE: BASEBAND DRIVER (BLOCK DIAGRAM)

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY — DATE 30/12/78
DESIGNED BY — DATE 26/12/78
APPROVED BY — DATE 30/12/78

[redacted] 3820[redacted] REV. [redacted]

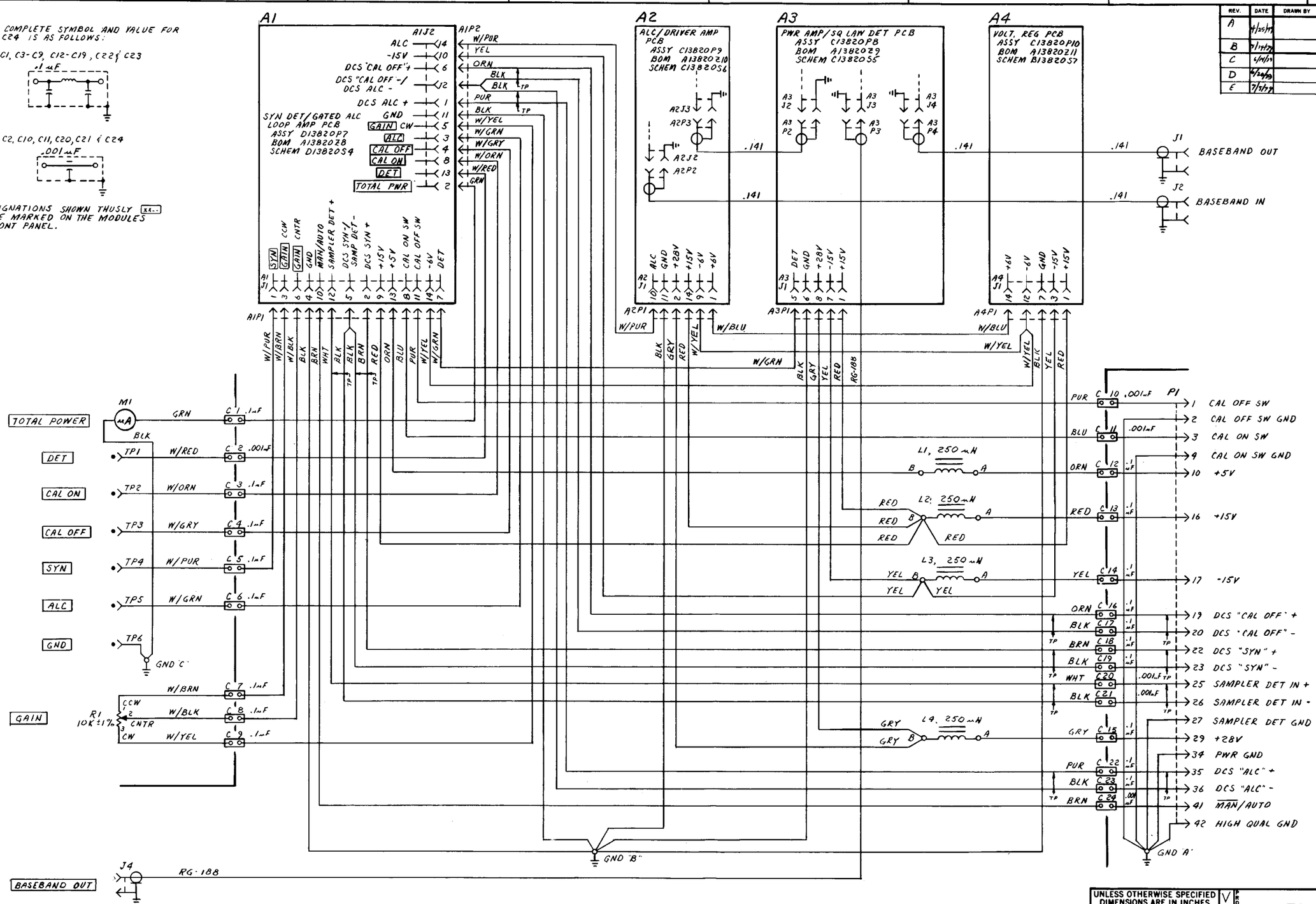
NOTES:

1. THE COMPLETE SYMBOL AND VALUE FOR C1-C24 IS AS FOLLOWS:

C1, C3-C9, C12-C19, C22 & C23 — .1 µF

C2, C10, C11, C20, C21 & C24 — .001 µF

2. DESIGNATIONS SHOWN THUSLY [XX..] ARE MARKED ON THE MODULES FRONT PANEL.



REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	4/25/79			ADDED: L1-L4. REVERSED A1J1 PINS
B	7/19/79			CHG A1J1-B WAS A1J1-4
C	4/4/79			ADD: CAP VALUES
D	6/26/79			CHG. WIRE COLORS ON A2
E	7/5/79			ADD. R1 TERM NOS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY	USED ON

VLA PROJECT: T5-C

TITLE: BASEBAND DRIVER SCHEMATIC

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

		DATE
DRAWN BY		1/29/79
DESIGNED BY		1/29/79
APPROVED BY		1/29/79

SHEET NUMBER | DRAWING NUMBER D1382OS1 | REV. E | SCALE

through shielded compartments. All power supply lines are filtered with π section low pass feedthrough filters. All digital signals are fed through 0.01 μF feedthrough capacitors to not degrade rise and fall times excessively. No wires or cables enter or leave the chassis without feedthrough filtering or proper grounding. This prevents signals entering the module flowing on the outsides of coax, for example.

However, even these steps proved inadequate for lower frequency interference from the fundamental and harmonics of various digital communications system clock signals. The worst culprit, in this case, was a 10 KHz LED driver clock signal from the M2 Data Tap module. It and its harmonics could enter the module on any of the power supply buss lines common to the entire "D" rack. Since the specified bandwidth of operation in the entire baseband system is 200 KHz to 50 MHz with less than 1.5 dB peak to peak variation, and since signal levels are low in several locations, serious interference could occur in the spectral line mode which uses the narrower and consequently lower frequency filters.

A filter for general use on the T3, T4, T5 module power supply lines consists of a 250 μH low resistance choke with a 33 μFd low series resistance tantalum capacitor. This provides -30 dB attenuation at 10 KHz under worst case conditions. The capacitors are mounted on the printed circuit boards in the T4C and T5C modules. The chokes are mounted inside the rear module shielded compartment near the Amp connector.

The T4C and T5C module housing are unique designs that provide shielding, optimum air flow, and excellent grounding for the microstrip and analog printed circuit boards. Maximum air flow is achieved by using the largest diameter holes consistent with the mechanical constraints of the top and bottom rail design. The holes are small enough to also provide adequate shielding in the operating frequency range.

The modules are designed such that the PC boards are accessible from both sides by removing each side plate for

ease in servicing. By using adjustable divider rails, PC boards can be moved to different positions within the module. Also PC boards of different sizes can be accommodated for versatility with possible future changes.

Microwave power transistors or hybrid amplifiers (such as those used in the T5C modules) can be readily heatsunk to the top or bottom rails using special heatsink brackets that allow for short RF connections to the PC board microstrip lines as well as low thermal resistance. These heatsink brackets can be moved to any rail location again for versatility with possible future changes.

2.2 ALC Driver Amplifier Assembly A2

Refer to Schematic C13820S6F. To obatin excellent phase stability versus temperature, along with non-variation of amplitude and phase non-linearity of the 200 KHz to 50 MHz passband over the typical ALC range of the T5 module, a differential amplifier ALC system is used.

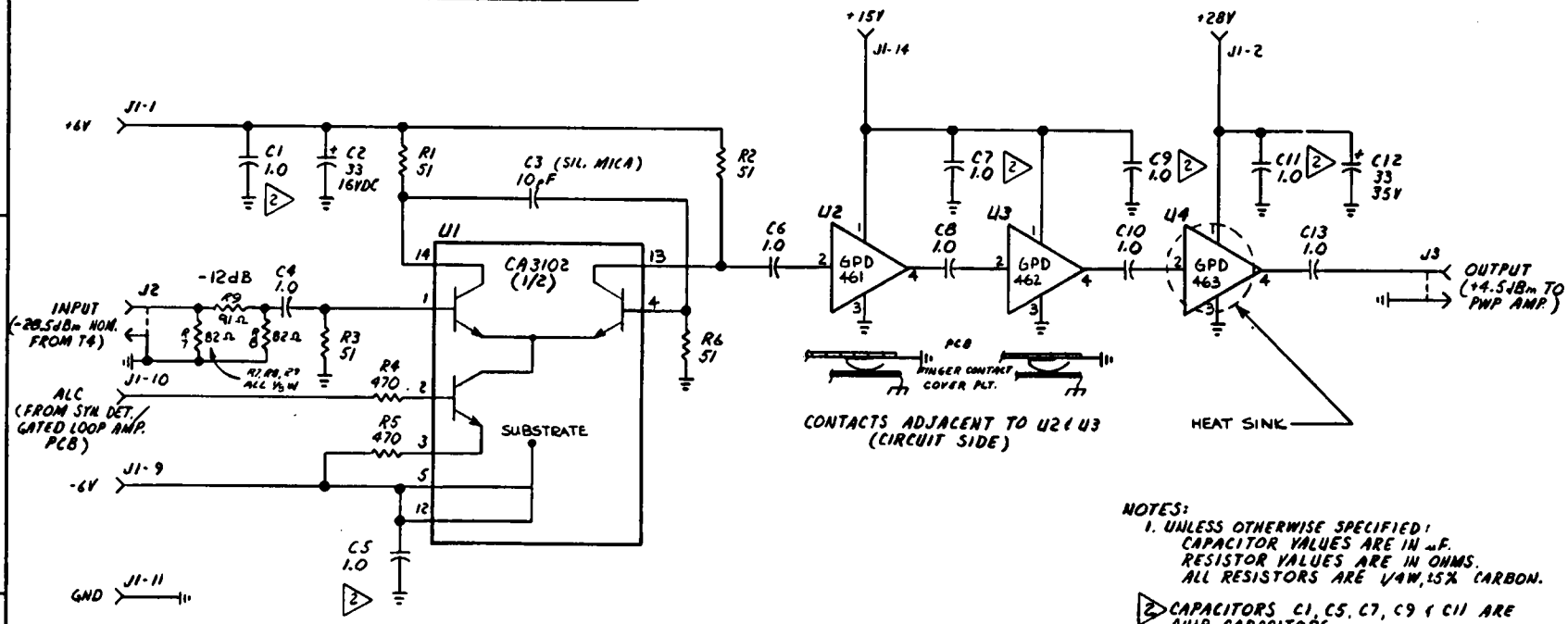
A pin diode or "mixer" type variable attenuator constitutes a variable resistance to vary attenuation. If a single device is driving any substantial reactance at the load, the phase linearity versus passband response will vary with varying attenuation. Another requirement of operation of such a device, is low level RF drive to minimize intermodulation distortion.

A differential amplifier ALC with a 51Ω input and output load resistance resolves these problems while providing excellent phase stability versus temperature.

The CA3102E transistor array forms the differential amplifier in the T5C ALC system. Because the amplifier gain is based on the difference in RF voltage across the two transistor base to emitter junctions, and because these transistors are closely matched, the phase stability versus temperature is excellent. Since the input and output are terminated immediately in 51Ω, and only the voltage gain and not input and output impedances change with ALC voltage, the phase

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	12/1/78			ADDED C13, C14, C15
B	3/12/79			REDESIGN
C	5/11/79			REV DUE TO CKT. CHGS
D	4/7/80			ADDED PIN NOS TO CA3102
E	5/20/80			CORR TO TABLE, NOTES
F	8/29/80			ADDED R7, R8, R9

CONN.	PIN	FUNCTION	SOURCE	WIRE COLOR
A2-J1	1	+6V	A4-P1-14	WHT/BLU
	2	+28V	L4B	GRY
	3			
	4			
	5			
	6			
	7			
	8			
	9	-6V	A4-P1-12	WHT/YEL
	10	ALC	A1-P2-14	WHT/PUR
	11	GND	CHASSIS GND "B"	BLK
	12			
	13			
	14	+15V	L2B	RED
A2-J2	—	RF INPUT	J2	.141 COAX.
A2-J3	—	RF OUTPUT	A3-J2	.141 COAX.



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   CAPACITOR VALUES ARE IN µF.
   RESISTOR VALUES ARE IN OHMS.
   ALL RESISTORS ARE 1/4W, ±5% CARBON.

2. CAPACITORS C1, C5, C7, C9 & C11 ARE CHIP CAPACITORS.

3. LAST CAP. = C13, LAST RESISTOR = R9

NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

VLA

T5-C BASEBAND DRIVER

TITLE: ALC/DRIVER AMP. P.C. CARD "A2" SCHEMATIC

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY		DATE	10-30-78
DESIGNED BY		DATE	10-30-78
APPROVED BY		DATE	10-30-79
SHEET NUMBER	1 of 1	DRAWING NUMBER	C1382056
REV	F	SCALE	—

non-linearity versus passband response versus ALC voltage remains constant.

Phase change versus ALC has been measured at less than 0.6°/dB at 50 MHz at the typical operating point over a ±10 dB range, for this particular amplifier after frequency compensation. Phase non-linearity versus passband response was measured at less than 2° from 10 MHz to 50 MHz. This varied less than 2° per ±10 dB ALC variation about the typical operating point from 10 MHz to 50 MHz.

Frequency compensation is required because of the uncompensated amplifier. This is accomplished through the use of a 10 pF capacitor in a positive feedback configuration. Passband amplitude variation will only occur as a result of component tolerances, and otherwise was shown to be negligible over a 10 MHz to 50 MHz range.

Maximum gain of the amplifier was measured at +3.1 dB at -0.7 VDC. Minimum gain (or isolation) was measured at -62 dB at -6.0 VDC at 50 MHz.

Hybrid amplifiers GPD 461, GPD 462 and GPD 463 (with heatsink) comprise most of the gain in the Driver Amplifier. Because all 3 stages along with the ALC amplifier were contributing significantly to module compression, -12.5 dB of attenuation was added to the ALC amplifier input to compensate for the +12.5 dB of extra power amplifier gain while keeping the ALC amplifier operating near it's most stable (versus temperature) range.

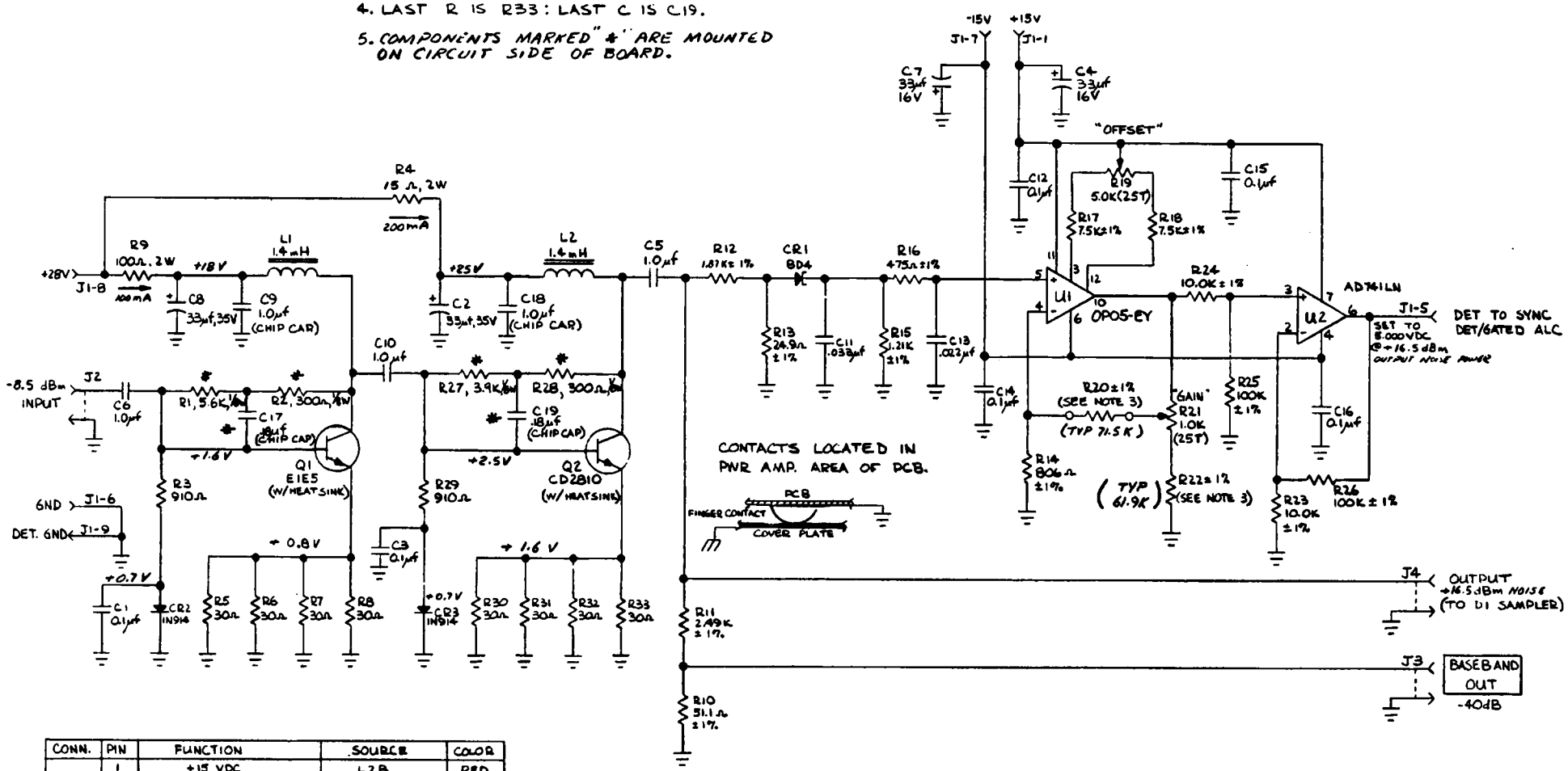
2.3 Power Amplifier/Square Law Detector Assembly A3B

To minimize compression in the T5C output stage a two stage discrete transistor power amplifier is utilized. This was required as the result of the inability of any available hybrid driver amplifier to operate at a required power level of +16.5 dBm - 12.5 dBm = +4 dBm with less than 1% compression. The E1E5 stage Q1 is identical to the power amplifier of the obsolete A3A board. A Schematic of the obosolete version is given in Appendix 8.2, Drawing No. C13820S5H, for reference only.

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
J	1/19/80			REDRAWN FOR 2ND P.AMP
K	2/15/80			CHG. R1, R2, R27, R28 TO ¼W CHG C17, C19 TO .18μf CHIP
L	7/11/81			CHG R12, R20, R22, ADD NOTE 5

NOTES:

1. ALL RESISTORS ARE ¼W, 5% UNLESS OTHERWISE SPECIFIED.
2. FUNCTIONS SHOWN THUSLY [XX---] ARE MARKED ON MODULE FRONT PANEL.
3. THE VALUE OF R20 & R22 IS DETERMINED AT ASSY. SHOULD R20 BE LESS THAN 50KΩ, R22 WILL NOT BE REQD.
4. LAST R IS R33: LAST C IS C19.
5. COMPONENTS MARKED "*" ARE MOUNTED ON CIRCUIT SIDE OF BOARD.



CONN.	PIN	FUNCTION	SOURCE	COLOR
A3J1	1	+15 VDC	L2B	RED
	2			
	3			
	4			
	5	DETECTOR	A1P1-7	WHT/BRN
	6	GROUND	CHASSIS GND "B"	BLK
	7	-15VDC	L3B	YEL
	8	+28VDC	L4B	GRY
	9	DET. GND.	~	~
	10			
	11			
	12			
	13			
	14			
A3J2		INPUT	A2J3	.141 COAX.
A3J3		BASEBAND OUT	J4	RG 188
A3J4		OUTPUT	MODULE J1	.141 COAX.

NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

VLA PROJECT: T5C BASEBAND DRIVER

TITLE: POWER AMP/SQ LAW DET. PCB SCHEMATIC A3-B

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY		DATE	1-18-80
DESIGNED BY		DATE	1-18-80
APPROVED BY		DATE	1-24-80

SHEET NUMBER 1 of 1 | DRAWING NUMBER C1382055 | REV. L | SCALE ~

The new version two stage amplifier is shown in Schematic C13820S5L.

Both stages operate on the resistor negative feedback Class A mode for low distortion and 50Ω input/output matching. Resistor values have been chosen to obtain this matching, and thereby result in a gain of +12.5 dB per stage independent of transistor h_{FE}. Passband flatness in both stages is limited by three major effects. First the passband performance of the collector choke limits flatness, especially at high DC currents which tend to saturate the core. A special choke was wound on stacked iron cores, for high inductance at 200 KHz with DC current and simultaneous low interwinding capacitance. At zero DC current the shunt effect of the inductor in a 50Ω system was measured at -0.00 dB at 200 KHz and -0.07 dB at 50 MHz. Because of the minimal effect on passband response the temperature variation of the inductor core material should have negligible effect on system phase stability.

The second passband rolloff effect is due to the series inductance of the emitter resistor. Inductance will cause a gain decrease IF comparable to the collector impedance. Therefore 4 resistors with short leads and wide PC board pads are used in parallel to minimize this effect.

The third major contribution to passband rolloff is due to positive feedback through the power supply lines with cascaded amplifiers. This will occur usually at low frequencies (due to the ineffectiveness of power supply bypass capacitors) and will result in a peaking of the total gain response toward the 200 KHz end. Because the coupling capacitor reactances limit low end frequency response total gain will peak at some frequency below 200 KHz. Since this peaking is the opposite effect as passband rolloff at the high frequency end, it, in effect, contributes to total passband rolloff.

This effect has been minimized through the use of large value, low series resistance and low series inductance tantalum bypass capacitors. If frequency compensation is

desired later, this effect will have to be corrected independently of the high frequency rolloff to minimize passband phase non-linearity.

No frequency compensation has been added to any of the baseband amplifier stages with the exception of the ALC amplifier in the T3, T4 and T5 modules since it appeared that the passband response design goals could be met without it.

Passband response profiles of the two stage amplifier have not been made at this time. However, earlier measurements of the single stage A3A amplifier (somewhat in compression) indicated -0.55 dB total amplitude rolloff with a total phase non-linearity of 3.7° peak to peak from 200 KHz to 50 MHz.

Total amplifier compression in the T5C module was measured at -1.3% or -1.5% at actual system noise power output levels for two modules.

The precision Square Law Detector is a BD-4 back diode. A back diode is used for combined linearity and temperature stability. A hot-carrier diode is totally unsuitable for a temperature stable detector. Because of the low DC level out of the diode, a very low input offset voltage bipolar OP Amp (OP-05-EY) was required as a preamplifier.

"CERMET" trimpots for the OP Amp gain and offset adjustments were found to be unsuitable because of wiper contact problems resulting in 10 times worse temperature stability than the "CERMET" material specification along with significant low frequency noise.

Thus wirewould trimpots were chosen instead. These trimpots have a disadvantage in that they have limited resolution. Thus a fixed gain control resistor R20 has to be chosen during module checkout to provide a coarse adjustment.

Precision measurement of diode non-linearity on noise power at the system operating point resulted in -0.7% or -2.7% absolute compression for two different modules. Temperature stability at the normal operating point for the complete T5C breadboard detector and amplifier resulted in 0.1%/°C error.

2.4 Synchronous Detector/Gated ALC Loop Amp Assembly A1

Refer to Schematic D13820S4F.

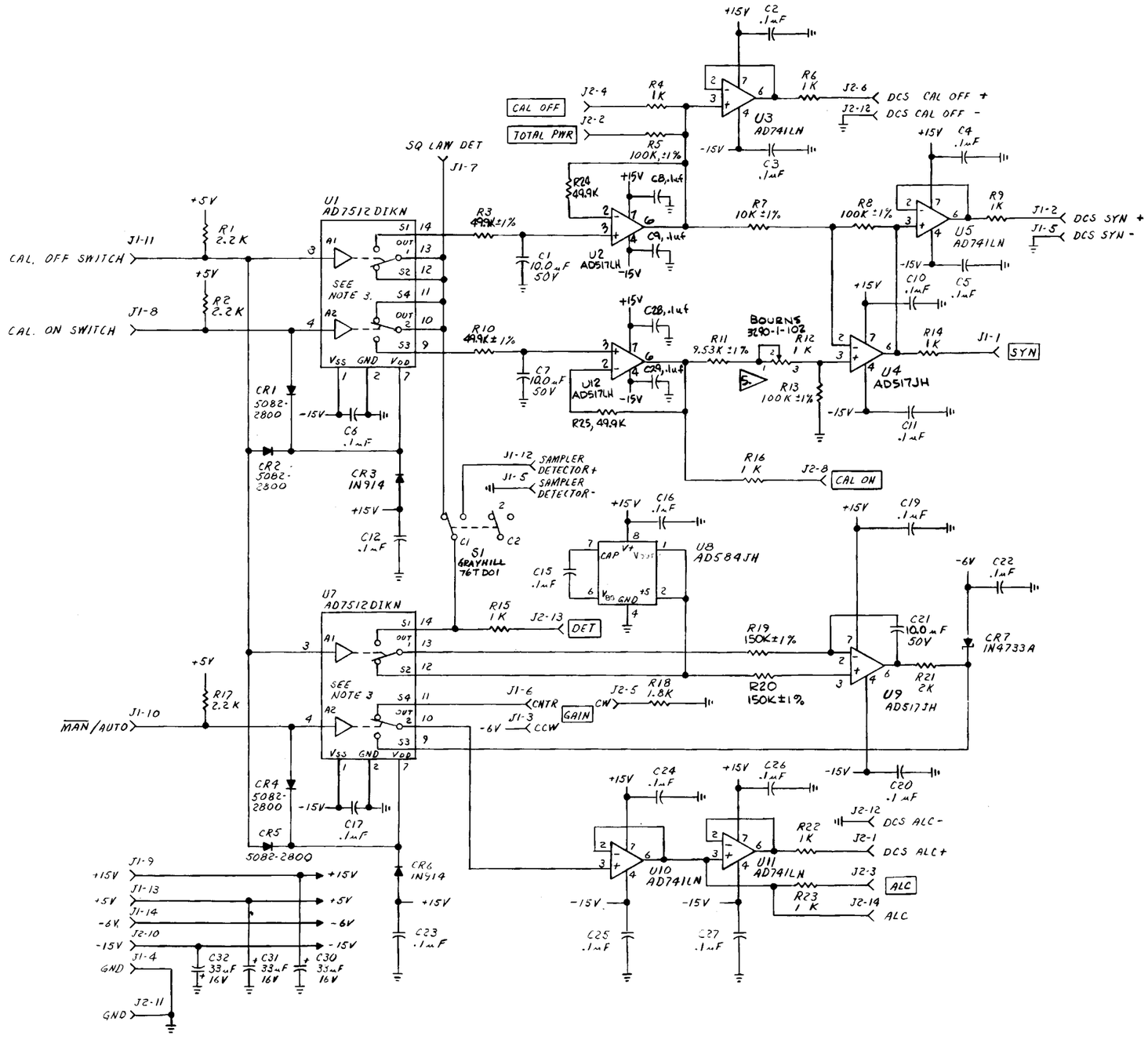
The synchronous detector in the T5C Baseband Driver had some stringent requirements on stability and accuracy. For this reason ultra-low offset voltage bipolar Op Amps are used in the detector circuit. Offset trimpots were unnecessary with these amplifiers resulting in simpler module set-up and less possibility of operator error. Bipolar Op Amps also have a major advantage over JFET Op Amps (commonly used in synchronous detectors) in that input offset voltages will remain stable with time. However, higher input bias and offset currents require smaller sample and hold timing resistances, to minimize total input offset voltage. Thus large value low leakage polycarbonate capacitors (10 μF) are required.

Detailed analysis of synchronous detector and ALC loop amplifier worst case errors is given in Figure 2.4.2. Note that a "Gain Match" potentiometer (again wirewound) was utilized to match the input gains of the difference amplifier U4, determined by 1% resistance values.

AD 741 LN Op Amps are used as output buffers to isolate the system from DCS noise feeding back from the T6C module. "SYN", "CAL OFF", and "ALC" monitor voltages are isolated in this manner.

Figure 2.4.3 shows the relationship of $V_{CAL\ OFF}$ and V_{SYN} to the calculation of the system T_{SYS}/T_{CAL} ratio.

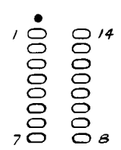
REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	29/9/78			REMOVED U6, C13, 14, R15
B	3/15/79			REV DUE TO EXTENSIVE CHANGES
C	5/14/79			REV. PER CKT CHANGES
D	5/17/79			CORRECTED VALUE OF C16 C7
E	9/20/79			CORR TO TABLE
F	10/31/79			CORRECTED WIRING ERROR



NOTES:

1. DESIGNATIONS SHOWN THUSLY [XX...] ARE MARKED ON MODULE FRONT PANEL.
2. UNLESS OTHERWISE INDICATED, ALL RESISTORS ARE 1/4 W ± 5%
3. I.C. CIRCUITS U1 & U7: ADDRESS HIGH MAKES "S1" TO "OUT 1" AND "S3" TO "OUT 2". ADDRESS INPUTS ARE SHOWN LOW.
4. J1 & J2 ARE 14 PIN DIP SOCKETS. FUNCTIONS ARE ASSIGNED AS SHOWN BELOW.

PIN LAYOUT (COMPONENT SIDE)



CONN.	PIN	FUNCTION	SOURCE	COLOR
A1J1	1	[SYN]	C5	W/PUR
	2	DCS "SYN +"	C18	BRN
	3	[GAIN] CCW	C7	W/BRN
	4	GND	CH GND "B"	BLK
	5	DCS SYN -/SAMP DET-	C19/C21	BLK
	6	[GAIN] CNTR	C6	W/BLK
	7	DET	A3P1-5	W/GRN
	8	CAL ON SWITCH	C11	BLU
	9	+15V	L2B	RED
	10	[MAN/AUTO]	C24	BRN
	11	CAL OFF SWITCH	C10	PUR
	12	SAMPLER DET +	C20	WHT
	13	+5V	L1B	ORN
	14	-6V	A4P1-12	W/YEL
A1J2	1	DCS "ALC" +	C22	PUR
	2	[TOTAL PWR]	C1	GRN
	3	[ALC]	C6	W/GRN
	4	[CAL OFF]	C4	W/GRY
	5	[GAIN] CW	C9	W/YEL
	6	DCS "CAL OFF" +	C16	ORN
	7			
	8	[CAL ON]	C3	W/ORN
	9			
	10	-15V	L3B	YEL
	11	GND	CH. GND "B"	BLK
	12	DCS CAL OFF-/DCS ALC -	C17/C23	BLK
	13	[DET]	C2	W/RED
	14	ALC	A2-P1-10	W/PUR

5 ADJUST R12 FOR 0.000 VDC ± 0.0005 VDC AT [SYN] FOR CAL ON = CAL OFF = 5.000 VDC.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY	USED ON
D1382P7	D1382015

PROJECT: VLA — T5-C

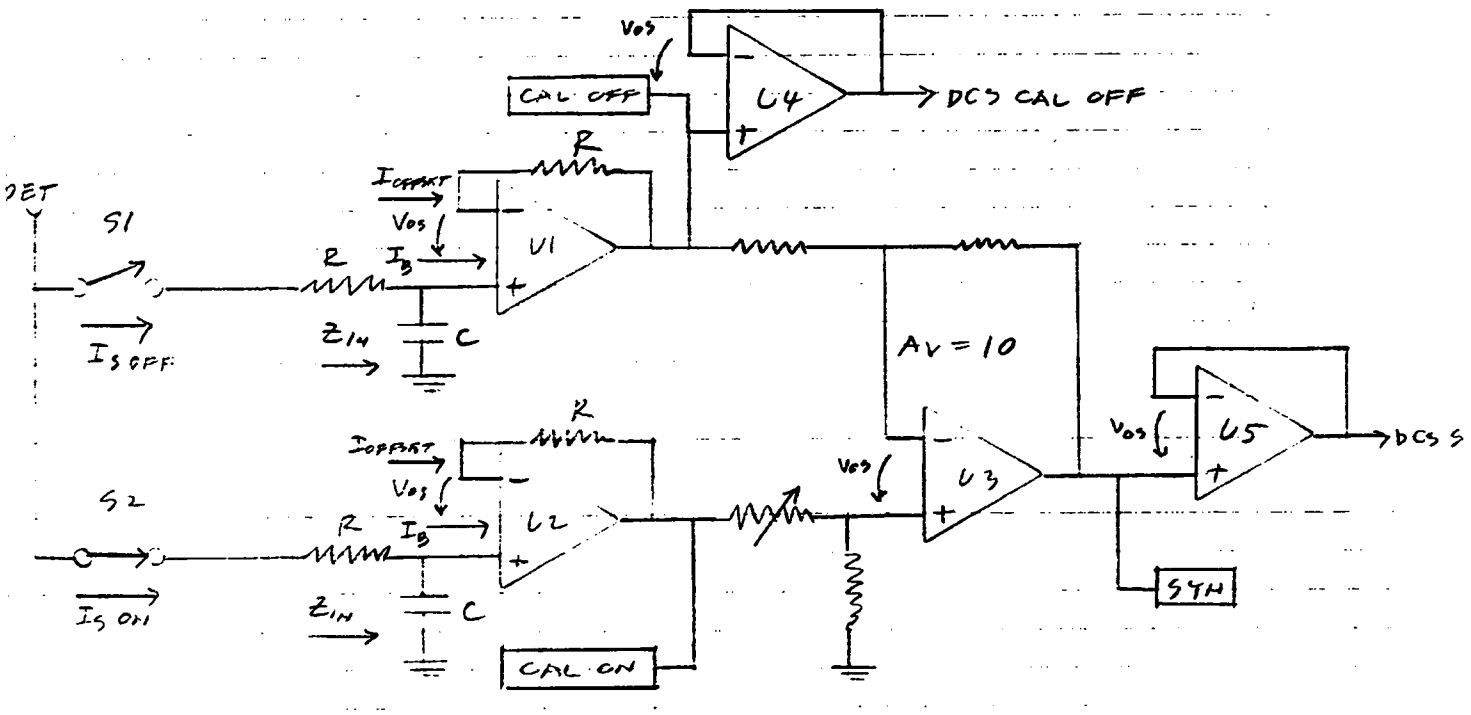
TITLE: SYNCHRONOUS DETECTOR/ GATED ALC LOOP AMP. SCHEMATIC "A1"

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

		DATE
DRAWN BY		12/1/78
DESIGNED BY		12/1/78
APPROVED BY		12/1/78

SHEET NUMBER | DRAWING NUMBER D1382034 | REV. F | SCALE

SYNCHRONOUS DETECTOR ERROR CALCULATIONS



Simplified Circuit

Figure 2.4.2

LET S1 = S2 = AD 7512DI

$I_{SON} \leq 10nA$ @ 25°C OVER FULL INPUT VOLTAGE RANGE

I_{SOFF} CURVE (SHOULD BE SIMILAR TO I_{SON} CURVE) SHOWS

$I_{SOFF} = 430\,pA$ @ −12 VDC TYPICAL

$I_{SOFF} = 60\,pA$ @ +5 VDC TYPICAL

$\therefore I_{SON} \leq (10nA)\left(\frac{60pA}{430pA}\right)$ @ 25°C @ 5 VDC

$\therefore$ $\boxed{I_{SON} \leq 1.3\,nA \text{ @ } 25°C \text{ @ } 5\,VDC}$

$I_{SOFF} = 5nA$ MAX @ 25°C OVER FULL INPUT VOLTAGE RANGE

I_{SOFF} CURVE SHOWS

$I_{SOFF} = 430\,pA$ @ −12 VDC TYPICAL

$I_{SOFF} = 60\,pA$ @ +5 VDC TYPICAL

$\therefore I_{SOFF} \leq (5nA)\left(\frac{60pA}{430pA}\right)$ @ 25°C @ 5 VDC

$\boxed{I_{SOFF} \leq 0.7\,nA \text{ @ } 25°C \text{ @ } 5\,VDC}$

LET U1 = U2 = AD 517LH

$V_{OS} \leq 25 \times 10^{-6}\,V$

$Z_{IN} = 2 \times 10^{11}\,\Omega$ COMMON MODE

$I_B \leq 1 \times 10^{-9}$ AMPS

$I_{OFFSET} \leq 0.25 \times 10^{-9}$ AMPS

LET U3 = AD 517 JH

$$\boxed{V_{os} \leq 150 \times 10^{-6}\ V}$$

LET U4 = U5 = AD741LN

$$\boxed{V_{os} \leq 0.5 \times 10^{-3}\ V}$$

LET RC = 0.5 SEC (MINIMUM ALLOWED)

LET $\boxed{C = 10\ \mu Fd}$ POLYCARBONATE (MAXIMUM STANDARD VALUE)

$$\therefore \boxed{R = 49.9\ K\Omega}$$

DROOP ERROR CALCULATIONS

TOTAL DROOP @ SYN $= \frac{(I_b + I_{SOFF}) \cdot t}{C} \cdot A_V \cdot 2 + 5\left[1 - e^{\frac{-t}{Z_{IN} C}}\right] \cdot A_V \cdot 1$

(DROOP DUE TO Z_{IN} ASSUMES $Z_{IN1} >> Z_{IN2}$)

$$= \frac{(1 \times 10^{-9} + 0.7 \times 10^{-9}) \cdot 50 \times 10^{-3}}{10 \times 10^{-6}} \cdot 10 \cdot 2$$

$$+ 5\left[1 - e^{\frac{-50 \times 10^{-3}}{(2 \times 10^{11})(10 \times 10^{-6})}}\right] \cdot 10 \cdot 1$$

$$= 1.7 \times 10^{-4} + 2.5 \times 10^{-7}$$

$$\boxed{\text{TOTAL DROOP @ SYN} = 1.7 \times 10^{-4}\ V}$$

$$\boxed{\text{TOTAL \% DROOP @ SYN} = \frac{1.7 \times 10^{-4}}{5} \times 100\% = 3.4 \times 10^{-3}\ \%}$$

SPEC. $\leq 0.1\%$ IN 50 mSEC

$3.4 \times 10^{-3} \leq 0.1\%$ ∴ OK

TOTAL DROOP @ CAL OFF OR CAL ON $= \frac{(I_b + I_{SOFF}) \cdot t}{C} \cdot A_V \cdot 1 + 5\left[1 - e^{\frac{-t}{Z_{IN} C}}\right] \cdot A_V \cdot 1$

$$= \frac{(1 \times 10^{-9} + 0.7 \times 10^{-9}) \cdot 50 \times 10^{-3}}{10 \times 10^{-6}} \cdot 1 \cdot 1 + 5\left[1 - e^{\frac{-50 \times 10^{-3}}{(2 \times 10^{11})(10 \times 10^{-6})}}\right] 1.$$

$$= 8.5 \times 10^{-6} + 2.5 \times 10^{-8}$$

$$\boxed{\text{TOTAL DROOP @ CAL OFF OR CAL ON} = 8.5 \times 10^{-6}\ V}$$

$$\boxed{\text{TOTAL \% DROOP @ CAL OFF OR CAL ON} = \frac{8.5 \times 10^{-6}}{5} \times 100\% = 1.7 \times 10^{-4}\ \%}$$

SPEC $\leq 0.1\%$ IN 50 mSEC

$1.7 \times 10^{-4} \leq 0.1\%$ ∴ OK

OFFSET ERROR CALCULATIONS

TOTAL OFFSET @ DCS SYN $= \left(I_{517L\,OFFSET} + I_{SON}\right) \cdot R \cdot A_{V(10)} \cdot 2 + V_{517L\,OFFSET} \cdot A_{V(10)} \cdot 2$

$+ V_{517J\,OFFSET} \cdot A_{V(10)} \cdot 1 + V_{741L\,OFFSET} \cdot A_{V(1)} \cdot 1$

(ASSUMES I_{BIAS} CANCELLED BY BALANCED RESISTORS IN "ON" STATE)

$= (0.25 \times 10^{-9} + 1.3 \times 10^{-9})(49.9 \times 10^{3})(10)(2)$

$+ (25 \times 10^{-6})(10)(2) + (150 \times 10^{-6})(10)(1)$

$+ (0.5 \times 10^{-3})(1)(1)$

$= 1.5 \times 10^{-3} + 0.5 \times 10^{-3} + 1.5 \times 10^{-3} + 0.5 \times 10^{-3}$

$\boxed{\text{TOTAL OFFSET @ DCS SYN} = 4.0 \times 10^{-3}\ \text{V}}$

$\boxed{\text{TOTAL OFFSET \% ERROR @ DCS SYN} = \frac{4 \times 10^{-3}}{5} \times 100\% = 0.08\%}$

SPEC $\leq 0.1\%$

$0.08\% \leq 0.1\%$ $\therefore$ OK

TOTAL OFFSET @ DCS CAL OFF $= \left(I_{5172L\,OFFSET} + I_{SON}\right) \cdot R \cdot A_{V(1)} \cdot 1 + V_{5172L\,OFFSET} \cdot A_{V(1)} \cdot 1$

$+ V_{741L\,OFFSET} \cdot A_V \cdot 1$

$= \left(0.25 \times 10^{-9} + 1.5 \times 10^{-9}\right)\left(49.9 \times 10^{3}\right)(1)(1)$

$+ \left(25 \times 10^{-6}\right)(1)(1) + \left(0.5 \times 10^{-3}\right)(1)(1)$

$= 7.7 \times 10^{-5} + 25 \times 10^{-6} + 0.5 \times 10^{-3}$

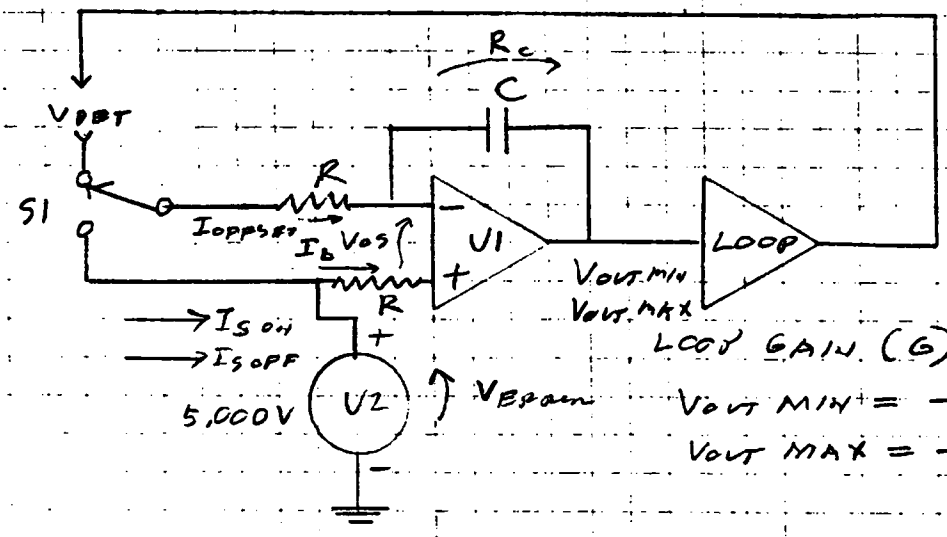
$\boxed{\text{TOTAL OFFSET @ DCS CAL OFF} = 6.0 \times 10^{-4}\ V}$

$\boxed{\text{TOTAL OFFSET FROM COL @ DCS CAL OFF } \% = \frac{6 \times 10^{-4}}{5} \times 100\% = 0.012\%}$

SPEC $\leq 0.1\%$

$0.012\% \leq 0.1\%$ ∴ OK

ALC AMPLIFIER ERROR CALCULATIONS



LOOP GAIN (G) = 1.5 TO 100

$V_{OUT\,MIN}$ = −6.0 VDC

$V_{OUT\,MAX}$ = −1.0 VDC

SIMPLIFIED CIRCUIT

LET S1 = AD7512DI

$I_{SON} \leq 1.3\,nA$ @ 25°C @ 5 VDC	FROM P. 2
$I_{SOFF} \leq 0.7\,nA$ @ 25°C @ 5 VDC	FROM P. 2

LET U1 = AD517JH

$V_{OS} \leq 150 \times 10^{-6}$ V

$Z_{IN} = 2 \times 10^{11}\,\Omega$ COMMON MODE

$I_B \leq 5 \times 10^{-9}$ AMPS

$I_{OFFSET} \leq 1 \times 10^{-9}$ AMPS

LET U2 = AD584JH

$V_{OUT} = 5.000\,V \pm 15 \times 10^{-3}\,V$

$1\,SEC \geq \tau = \frac{RC}{G} \geq 5 \times 10^{-6}$ SEC AT ALL LOOP GAIN

$G_{MIN} = 1.5$, LET $C = 10\,\mu Fd$ POLYCARBONATE (MAXIMUM STANDARD VALUE)

$$\tau_{MAX} = \frac{RC}{G_{MIN}}$$

$$1\,SEC = \frac{R(10 \times 10^{-6})}{1.5}$$

$$\therefore R = 150 \times 10^{3}\,\Omega \quad 19.$$

$$\tau_{MIN} = \frac{RC}{G_{MAX}} = \frac{(150 \times 10^{3})(10 \times 10^{-6})}{100}$$

$\tau_{MIN} = 0.015$ SEC $\geq 5 \times 10^{-6}$ SEC $\therefore$ OK

CAPACITOR INSULATION RESISTANCE $= 3 \times 10^{5}(10^{6}\,\Omega \cdot 10^{-6}\,F)$ @ 25°C

$$\therefore 3 \times 10^{5} = R_C(10^{6}\,\Omega)\,C(10^{-6}\,F)$$

$$\therefore R_C = 3 \times 10^{4} \times 10^{6}\,\Omega = 3 \times 10^{10}\,\Omega = R_C$$

ALC

DROOP ERROR CALCULATIONS

TOTAL DROOP @ DET $= (V_{IN} - V_{OUT\,MIN.})\left(1 - e^{-\frac{t}{R_C C}}\right)(G_{MAX}) +$

$$\left[\frac{(I_{SOH} + I_{OFFSET}) \cdot t}{C}\right] \cdot (G_{MAX}) +$$

$$\left[\frac{(I_{OFFSET} \cdot 2R + V_{OS}) \cdot t}{RC}\right] \cdot (G_{MAX})$$

$\Rightarrow$ SHUNT RESISTANCE DROOP +
LEAKAGE CURRENT DROOP +
OFFSET VOLTAGE DROOP

(ASSUMES I_b CANCELLED BY BALANCED RESISTORS)

$$= [5 - (-6)]\left[1 - e^{-\frac{50 \times 10^{-3}}{(3 \times 10^{10})(10 \times 10^{-6})}}\right][100] +$$

$$\left[\frac{(1.3 \times 10^{-9} + 1 \times 10^{-9})\, 50 \times 10^{-3}}{10 \times 10^{-6}}\right][100] +$$

$$\left[\frac{[(1 \times 10^{-9})(2)(150 \times 10^{3}) + 150 \times 10^{-6}] \cdot 50 \times 10^{-3}}{(150 \times 10^{3})(10 \times 10^{-6})}\right][10$$

$$= 1.8 \times 10^{-4} + 1.15 \times 10^{-3} + 1.5 \times 10^{-3}$$

$$\boxed{\text{TOTAL DROOP @ DET} = 2.8 \times 10^{-3}\ V}$$

$$\boxed{\text{TOTAL \% DROOP @ DET} = \frac{2.8 \times 10^{-3}}{5} \times 100\% = 0.06\ \%}$$

SPEC $\leq 0.1\%$

0.06 $\leq$ 0.1% $\therefore$ OK

M.S.D. 2/28/79-10

ALC
OFFSET ERROR CALCULATIONS

TOTAL ALC OFFSET ERROR $= V_{ERROR} + (I_{OFFSET} + I_{SOFF})\,2R$

(ASSUMES I_b CANCELLED BY BALANCED RESISTORS)

$= 15 \times 10^{-3} + (1 \times 10^{-9} + 0.7 \times 10^{-9})(2)(150 \times 10^{-}$

$= 15 \times 10^{-3} + 5.1 \times 10^{-4}$

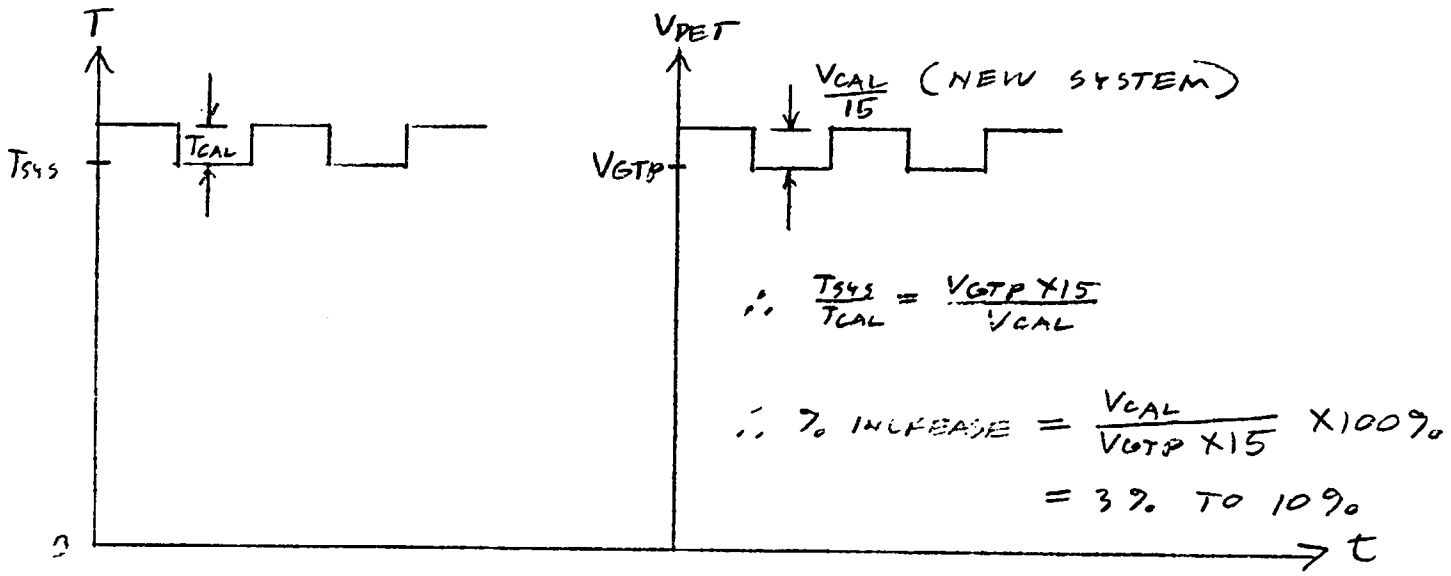
$$\boxed{\text{TOTAL ALC OFFSET ERROR} = 16. \times 10^{-3}\ V}$$

$$\boxed{\text{TOTAL \% ALC OFFSET ERROR} = \frac{16 \times 10^{-3}}{5} \times 100\% = 0.32\%}$$

SPEC $\leq 1.0\%$

$0.32\% \leq 1.0\%$ $\therefore$ OK

F4 (FRONT END)



T5 (AFTER FINAL ANALOG FILTERING)

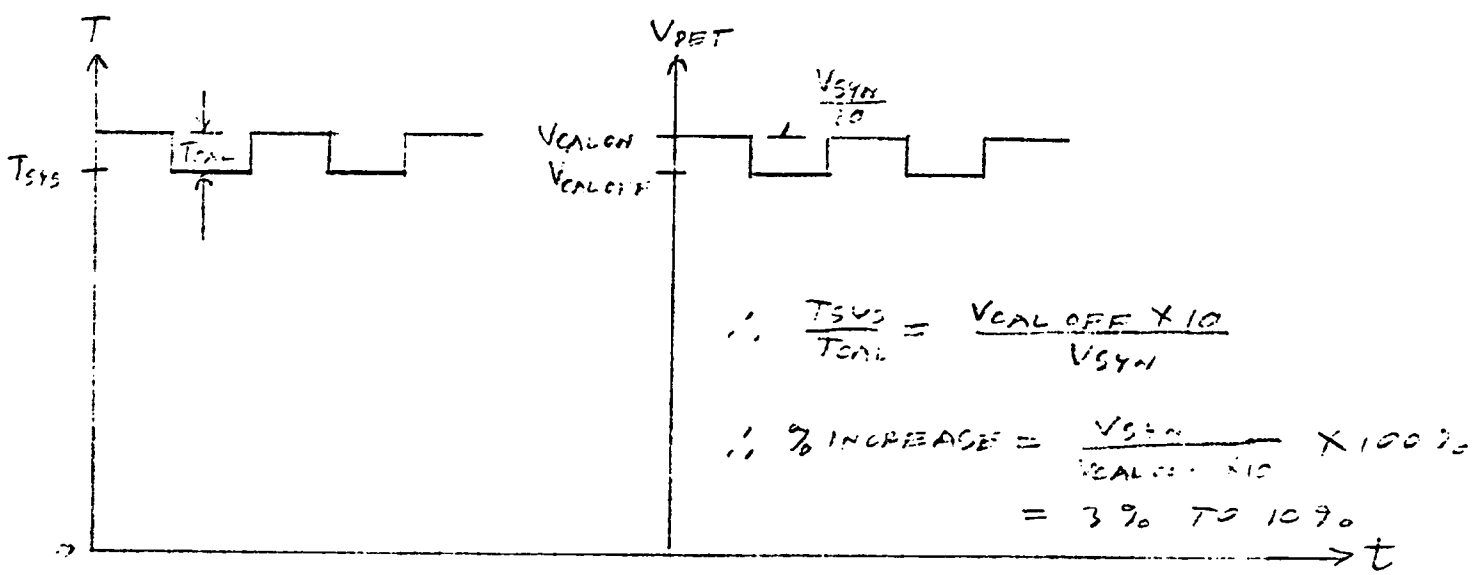


Figure 2.4.3

2.5 Voltage Regulator Assembly A4

The ALC amplifier on the ALC/Driver amplifier requires ±6 VDC for proper operation. Three terminal IC regulators of the 7805 family were found to be inherently unstable. Because of the broad frequency range of the T5C module, these were abandoned in favor of a simpler stable Zener diode system. The Schematic is given by B13820S7D.

3.0 FRONT PANEL INDICATORS AND CONTROLS

3.1 Total Power Meter

This meter is connected to the "CAL OFF" output of the synchronous detector. Thus it is always connected to the T5C internal square law detector. It is calibrated to 50 μA (+5 VDC @ $V_{CAL\ OFF}$) for +16.5 dBm output. Note that in the system it will read higher than 50 μA because of cable losses to the sampler module, which is normally used to set the T5C output level.

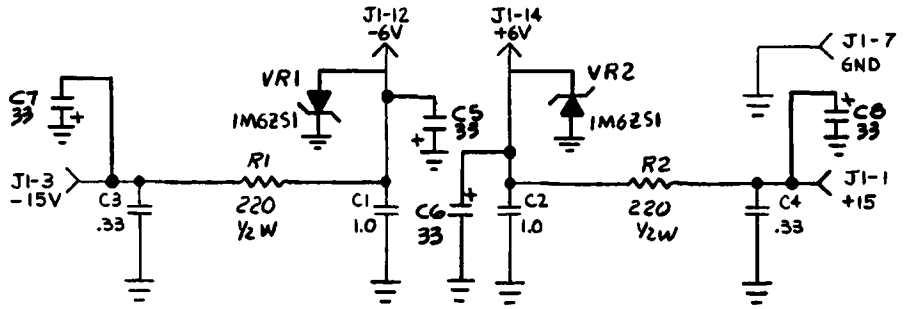
3.2 Monitor Jacks

"DET" is connected to the detector line that feeds the ALC loop filter. In normal operation the detector switch on the A1 card is in the "D1 Sampler" detector position, and this monitor jack will read the sampler detector output at +5.00 VDC gated with the modem T/R pulse. In the test position (switch in the "T5" detector position) this monitor jack will read the internal T5C detector output. If the internal switch is accidently left in the test position when placed in the system, both the total power meter and the detector monitor jack will read +5.00 VDC.

"CAL ON" is connected to the A1 card "CAL ON" synchronous detector output. This voltage is sampled when the front end calibration noise source is turned on. Therefore in normal operation it would be 3 to 10% higher than the "CAL OFF" monitor jack.

"CAL OFF" is connected to the A1 card "CAL OFF" synchronous detector output. This voltage is sampled when the front end

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION



CONN.	PIN	FUNCTION	SOURCE	COLOR
A4-J1	1	+15V	L2B	RED
	2			
	3	-15V	L3B	YEL
	4			
	5			
	6			
	7	GND	CHASSIS GND "B"	BLK
	8			
	9			
	10			
	11			
	12	-6V	A1-P1-14, A2-P1-9	W/YEL
	13			
	14	+6V	A2-P1-1	W/BLU

NOTES:

1) ALL CAPACITORS IN μf UNLESS NOTED OTHERWISE

NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

VLA PROJECT: T5-C BASEBAND DRIVER

TITLE: VOLTAGE REGULATOR P.C. CARD SCHEMATIC "A4"

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY | DATE
DESIGNED BY | DATE
APPROVED BY | DATE

SHEET NUMBER 1 of 1 | DRAWING NUMBER B138205 7 | REV. D | SCALE —

calibration noise source is turned off. It should normally read somewhat higher than +5 VDC in the system.

"SYN" is connected to the difference amplifier output of the T5C synchronous detector output. The difference amplifier has a gain of 10 so that

$$\frac{T_{SYS}}{T_{CAL}} = \frac{V_{CALOFF} \times 10}{V_{SYN}}$$

The percentage increase is normally 3 to 10% of 5 VDC. Therefore V_{SYN} should be positive and between 0.15 and 0.5 VDC. If it is negative, check the gating system.

"ALC" is connected to the ALC voltage feeding the A2 card ALC amplifier. This voltage is clamped to -6.7 volts at minimum gain and about -0.7 volts at maximum gain by Zener diode CR7 on the A1 card. At normal system operation it should read about -4 VDC. When the T5C module is first plugged into the rack this voltage will be at maximum gain -0.7 volts until the integrator capacitor charges to its normal state. Also the total power meter will peg high as a result.

3.3 "Gain" Control

This pot is connected to the ALC amplifier input when the T6C Baseband Control module is switched to the manual position for that channel. Clockwise is increasing gain.

3.4 "Baseband Out" BNC Jack

This jack is connected to the output of the T5C power amplifier through a -40 dB resistor voltage divider network when both the T5 output and the BNC jack are terminated in 50Ω.

Note that this is connected to a resistive voltage divider and not a directional coupler. Therefore the total voltage across the T5C output is being measured and not forward power. Total voltage is the sum of the forward voltage and the return voltage from the Screen Room filters and sampler input return losses.

Calculation of maximum in-band (200 KHz - 50 MHz) amplitude ripple and frequency due to D1 sampler and Screen Room filter VSWR as measured at T5C "Baseband Out" BNC monitor jack is given below:

Assume cable loss negligible

D1 Sampler $\rho s = .056$ for $s = 1.12$ max

70 MHz LPF $\rho f = .20$ for $s = 1.5$ max

Total coax to LPF 100 ft $\geq \ell \geq$ 50 ft.

$$\therefore \text{"Baseband Out" ripple}_{pp} \leq 20 \text{ dB LOG}_{10} \left(\frac{1+(\rho s+\rho f)}{1-(\rho s+\rho f)} \right)$$

$$\leq 4.5 \text{ dB}_{pp} \text{ WORST CASE}$$

$$f_{ripple} \geq \frac{Vp\ C}{2\ l_{max}} \text{ (Hz)}$$

$$\geq \frac{(.66)(3x10^8 \text{ m/s})}{2\ (30.48\text{m})_{max}} = 3.25 \text{ MHz for 100 ft.}$$

$$f_{ripple} \leq \frac{Vp\ C}{2\ l_{min}} \text{ (Hz)}$$

$$\geq \frac{(66)(3x10^8\text{m/s})}{2\ (15.24)} = 7.5 \text{ MHz for 50 ft.}$$

Calculation of maximum in-band (200 KHz - 50 MHz) amplitude ripple due to D1 sampler, Screen Room filter and T5C VSWR as measured at D1 sampler input is given below:

Assume cable loss negligible

D1 Sampler $\rho s = .056$ for $s = 1.12$ max

70 MHz LPF $\rho f = .20$ for $s = 1.5$ max

T5C output $\rho t = .060$ for $s = 1.13$ max

$$\text{D1 input ripple}_{pp} \leq 20 \text{ dB LOG}_{10} \left(\frac{1+\rho t(\rho s+\rho f)}{1-\rho t(\rho s+\rho f)} \right)$$

$$\leq 0.27 \text{ dB}_{pp} \text{ worst case}$$

4.0 TEST PROCEDURE

Check wiring harness with ohmmeter against module Schematic D13820S1.

Check that all IC's are oriented properly in their sockets. (Dot on component side marks Pin 1. Tab on TO-99 packages marks Pin 8.) DO NOT confuse these markings.

Check that GPD amplifiers are correctly mounted against board. (⊓ marks tab of GPD amplifier.)

Set power supply voltages at filter inductors for ±10 mV.

Place T5B in Manual mode and turn Front Panel Gain Control clockwise. Check for increasing power output past +20 dBm. If this cannot be obtained, check to be sure the E1E and CD2810 are soldered in correctly. Removing A3-P1 should lower +28 VDC power supply current by 200 mA if power amplifiers are functioning properly.

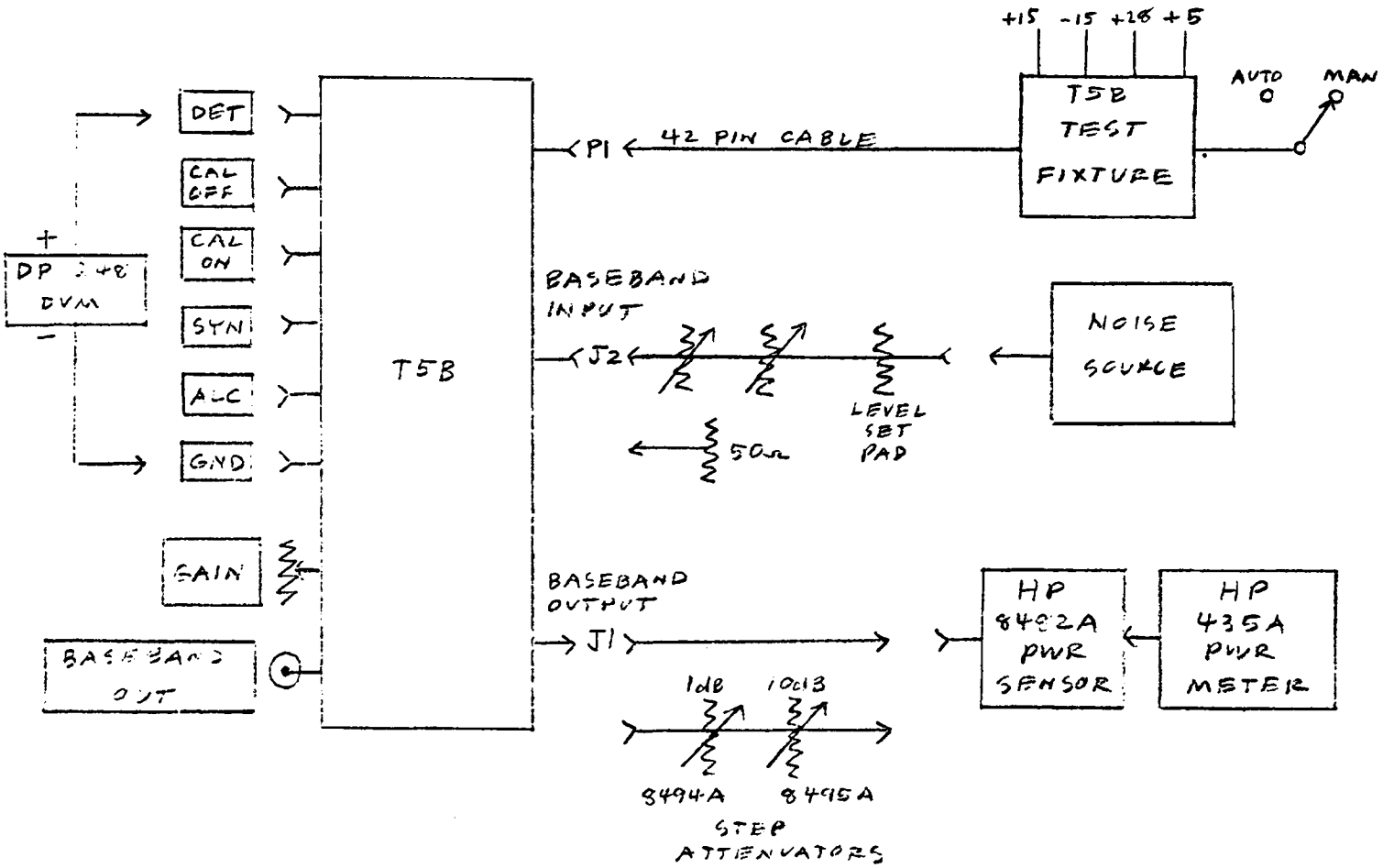
If the ALC Driver Board lacks output check for -1 to -6 volts on V_{ALC} line as gain is adjusted. Use a high speed scope (such as a 475) to trace through the various stages for signal if V_{ALC} is satisfactory.

Place spectrum analyzer on output jack. If oscillation appears (usually near 900 MHz) at any given setting of the Front Panel Gain Control, check all component values, plated-through holes, and chip capacitors for leaching. (Sudden changes in meter reading versus gain control setting is also a symptom of this problem.)

BASEBAND ALIGNMENT PROCEDURES

T5B Alignment - as follows

4.1 Test Set-up



4.2 Detector "OFFSET" Adjustment

Terminate J2 (baseband input) and connect J1 (baseband output) to HP8482A power sensor. Turn T5B front panel gain to minimum in manual mode. With left side panel secured to module let module stabilize to room temperature. (Approximately ½ hour.)

Install 71.5 KΩ 1% resistor at R20 on A3 board.

Connect DVM to DET and GND and adjust "Offset" pot on A3 board for 0.0000 ± .0005 VDC output.

4.3 Detector "GAIN" Resistor Selection (R_{20}) and Gain Adjustment

Connect J2 (Baseband Input) to noise source through fixed attenuator pad selected to give approximately -28.5 dBm noise power as measured with HP8482A and HP435A. Record level.

Connect DVM to "DET" and "GND".

Connect J1 (Baseband Output) to HP8482A power sensor.

With T5B in manual mode, adjust front panel manual gain control for +16.5 dBm output power.

Set power meter cal factor for 30 MHz.

Measure detector voltage with A3 Board "Gain" adjust trimpot at minimum and maximum settings. Calculate R_{20} value using following formula:

$$R_{20} = R_{20(Initial)} \frac{10}{V_{DET(Max)} + V_{DET(Min)}}$$

Insert R_{20} on A3 board and set "Gain" adjust trimpot for +5.000 ± .001 VDC output at "DET". Check front panel meter for midscale. Change R_{20} if necessary.

Recheck offset.

4.4 Synchronous Detector "Gain Match" Adjustment

Set S1 on A1 Board to T5 detector position.

With "DET" at 5 VDC as in 4.3, move DVM to "SYN" and "GND".

Adjust "Gain Match" trimpot on A1 Board to 0.000 VDC ± .001 VDC averaged over many DVM samples.

4.5 (A) Check Front Panel Voltages

(Use set up of 4.4.)

DET = 5.000 ± .001 VDC

CAL OFF = 5.000 ± .005

CAL ON = 5.000 ± .005

SYN = 0.000 ± .001 VDC

ALC ≈ -4.0 VDC

(B) Check DCS Voltages at Test Fixture Outputs

DCS CAL OFF = 5.000 ± .005 VDC

DCS SYN = 0.000 ± .001 VDC

DCS ALC ≈ -4.0 VDC

4.6 Check ALC Operation

(Use set up of 4.4.)

Set S1 on A1 Board to T5 Detector position.

Set T5B in automatic mode and remeasure front panel voltages after stabilization.

DET = 5.00 ± .15 VDC

CAL OFF = 5.00 ± .020 VDC

CAL ON = 5.00 ± .020 VDC

SYN = 0.000 ± .001 VDC

ALC ≈ -4.0 VDC

4.7 Return S1 on A1 Board to D1 Sampler Detector Position

T5B ALIGNMENT RESULTS

Module Serial No. _____

Date _____

By _____

R_{20} = _____ Ω (From 3.)

DET = _____ V (From 5.)

CAL OFF = _____ V

CAL ON = _____ V

SYN = _____ V

ALC = _____ V

DCS CAL OFF = _____ V

DCS SYN = _____ V

DCS ALC = _____ V

DET (AUTO) = _____ V (From 6.)

CAL OFF (AUTO) = _____ V

CAL ON (AUTO) = _____ V

SYN (AUTO) = _____ V

ALC (AUTO) = _____ V

5.0 LIST OF DRAWINGS

REVISIONS				
REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

DRAWN BY	DATE			
DESIGNED BY	DATE			
APPROVED BY	DATE			
			NEXT ASSY	USED ON

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLA

PROJECT (T5C)

TITLE BASEBAND DRIVER

DWG NO. A13820C2 SHEET 1 OF 4

ASSEMBLY NAME (T5B) BASEBAND DRIVER | SERIES/MODEL | USED ON

DRAWING NO.	REV.	TITLE	NOTES
A13820Z05	J	BASEBAND DRIVER MODULE -- BOM	
D13820F05	E	-- ASSY	
C13820F03	D	- BLOCK DIAGRAM	
D13820S01	E	- SCHEMATIC	
A13820W13	—	- WIRE LIST	
A13820Z11	E	VOLTAGE REGULATOR PCB - BOM	
C13820F10	C	- ASSY	
B13820S07	D	- SCHEMATIC	
C13820AB16	C	- DRILL DWG.	
C13820AB15	C	- ARTWORK	
A13820Z10	G	ALC/DRIVER AMP PCB - BOM	
C13820P09	F	- ASSY	
C13820S06	F	- SCHEMATIC	
E13820M32	C	- HEAT SINK	
C13820AB14	D	- DRILL DWG	
C13820AB12	D	- ARTWORK	
A13820Z09	K	PWR AMP/SQ LAW DET. PCB - BOM	
C13820P08	G	- ASSY	
C13820S05	L	- SCHEMATIC	
B13820M25	—	- HEAT SINK	
C13820AB17	D	- DRILL DWG	
C13820AB11	D	- ARTWORK	
C13820S05	H	(SINGLE STAGE)	FOR REF ONLY

NOTES:

1. GENERAL USE ITEM

DWG. NO. A13820C2

SHEET 2 of 4

REV.

ASSEMBLY NAME (T5B) BASEBAND DRIVER | SERIES/MODEL | USED ON

DRAWING NO.	REV.	TITLE	NOTES
A13920Ø2Ø8	D	SYNC. DET/GATED ALC LOOP AMP PCB - BOM	
D13820PØ7	B	- ASSY	
D13820SØ4	F	- SCHEMATIC	
D13920AB18	B	- DRILL DWG	
D13920AB1Ø	B	- ARTWORK	
A13820Z27	—	ALC/DRIVER AMP TEST FIXTURE - BOM	
C13820F26	—	- ASSY	
C13820S1Ø	—	- SCHEMATIC	
B13820S11	A	PWR AMP/SQ LAW DET TEST FIXTURE - SCHEMATIC	
C13820S12	B	BASEBAND DRIVER MOD. TEST FIXTURE - SCHEMATIC	
A13920Z26	—	ALC/DRIVER AMP TEST FIXTURE CABLE - BOM	
B13920P25		- ASSY	
A13920Z28	—	PWR AMP/SQ LAW DET. CABLE - BOM	
C13820P27	—	- ASSY	
A13920Z3Ø		CHOKE, 1.4 mH R.F - BOM	
B13920P3Ø		- ASSY	
B13050MØ4	D	GUIDE	1
C13820MØ2	E	PANEL, FRONT	
C13920MØ5	—	PANEL, REAR	

NOTES:

1. GENERAL USE ITEM

DWG. NO. A13920C2

SHEET 3 of 4

ASSEMBLY NAME (T5B) BASEBAND DRIVER

SERIES/MODEL

USED ON

DRAWING NO. (1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18)	REV.	TITLE	NOTES
D138206Ø6	B	SIDE PLATE	
D138206Ø7	C	BAR SUPPORT, TOP & BOTTOM	
D138206Ø8	C	DIVIDER RAILS & PLATES	

NOTES:

1. GENERAL USE ITEM

DWG. NO. A138206C2

SHEET 4 of 4

REV.

6.0 DATA SHEETS

CA3049T, CA3102E

DUAL HIGH-FREQUENCY DIFFERENTIAL AMPLIFIERS

For Low-Power Applications at Frequencies up to 500 MHz

Features:

- Power Gain 23 dB (typ.) at 200 MHz
- Noise Figure 4.6 dB (typ.) at 200 MHz
- Two differential amplifiers on a common substrate
- Independently accessible inputs and outputs
- Full military-temperature-range capability- (−55°C to + 125°C) for the CA3102E and for the CA3049T

- **The CA3049 is available in a sealed-junction Beam-Lead version (CA3049L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".**

RCA-CA3049T and CA3102E consist of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six transistors which comprise the amplifiers are general-purpose devices which exhibit low 1/f noise and a value of f_T in excess of 1 GHz. These features make the CA3049T and CA3102E useful from dc to 500 MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

The monolithic construction of the CA3049T and CA3102E provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual-channel applications where matched performance of the two channels is required.

The CA3102E is like the CA3049T except that it has a separate substrate connection for greater design flexibility. The CA3049T is supplied in the 12-lead TO-5 package; the CA3102E, in the 14-lead plastic dual-in-line package.

Applications

- VHF amplifiers
- VHF mixers
- Multifunction combinations – RF/Mixer/Oscillator; Converter/IF
- IF amplifiers (differential and/or cascode)
- Product detectors
- Doubly balanced modulators and demodulators
- Balanced quadrature detectors
- Cascade limiters
- Synchronous detectors
- Balanced mixers
- Synthesizers
- Balanced (push-pull) cascode amplifiers
- Sense amplifiers

MAXIMUM RATINGS, ***ABSOLUTE-MAXIMUM VALUES, AT T_A = 25°C***

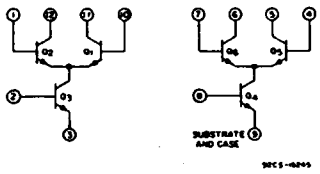
Power Dissipation, P:	CA3049T	CA3102E	
Any one transistor	300	300	mW
Total package	600	750	mW
For T_A > 55°C Derate at:	5	6.67	mW/°C
Temperature Range:			
Operating	−55 to + 125	−55 to + 125	°C
Storage	−65 to + 150	−65 to + 150	°C

Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. ..... +265°C

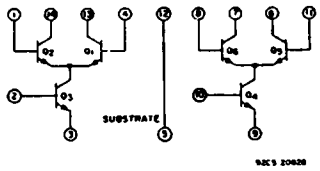
The following ratings apply for each transistor in the device

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

*The collector of each transistor of the CA3049T and CA3102E is isolated from the substrate by an integral diode. The substrate (terminal 9) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.



Schematic Diagram for CA3049T



Schematic Diagram for CA3102E

Typical Characteristics for CA3049T and CA3102E

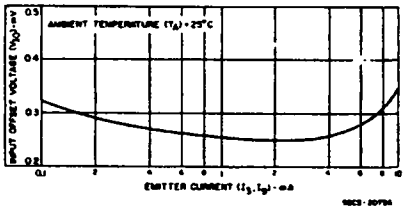


Fig. 4—Input offset voltage vs. emitter current.

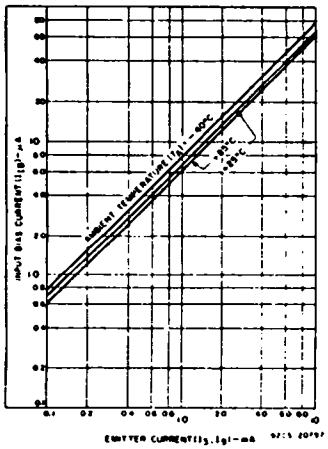


Fig. 5—Input bias current vs. emitter current.

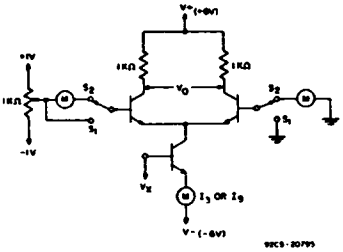


Fig. 1—Static characteristics test circuit for CA3102E.

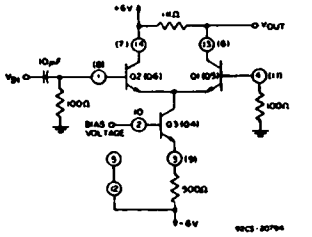
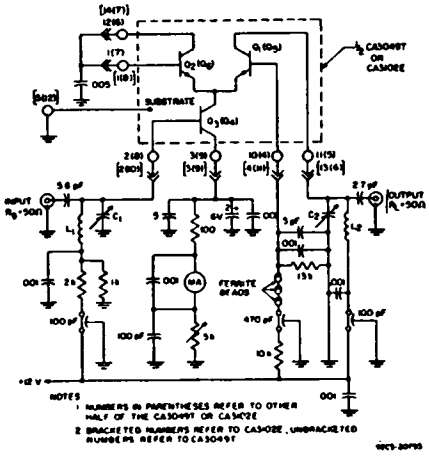


Fig. 2—AGC range and voltage gain test circuit for CA3102E.



L_1, L_2 – Approx. 1/2 Turn #18 Tinned Copper Wire, 5/8" Dia.
C_1, C_2 – 15 pF Variable Capacitors (Hammarlund, MAC 15, or Equivalent)
All Capacitors in μF Unless Otherwise Indicated
All Resistors in Ohms Unless Otherwise Indicated

Fig. 3—200 MHz cascode power gain and noise figure test circuit.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		TEST CIRCUIT FIG.	CA3049T LIMITS MIN.	TYP.	MAX.	UNITS	TYPICAL CHARACTERISTICS CURVES FIG.
STATIC CHARACTERISTICS									
For Each Differential Amplifier									
Input Offset Voltage	V_{IO}			1	—	0.28	—	mV	4
Input Offset Current	I_{IO}	$I_3 = I_9 = 2$ mA		1	—	0.3	—	μA	—
Input Bias Current	I_{IB}			1		13.6	35	μA	5
Temperature Coefficient Magnitude of Input Offset Voltage	$\lvert\Delta V_{IO}/\Delta T\rvert$			1	—	1.1	—	μV/°C	6
For Each Transistor									
DC Forward Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 6$ V, $I_C = 1$ mA		—	—	774	—	mV	6
Temperature Coefficient of Base-to-Emitter Voltage	$\Delta V_{BE}/\Delta T$	$V_{CE} = 6$ V, $I_C = 1$ mA		—	—	-0.9	—	mV/°C	6
Collector Cutoff Current	I_{CBO}	$V_{CB} = 10$ V, $I_E = 0$		—	—	0.0013	100	nA	7
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1$ mA, $I_B = 0$		—	15	24	—	V	—
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10$ μA, $I_E = 0$		—	20	60	—	V	—
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10$ μA, $I_B = 0$, $I_E = 0$		—	20	60	—	V	—
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10$ μA, $I_C = 0$		—	5	7	—	V	—
DYNAMIC CHARACTERISTICS									
1/f Noise Figure (For Single Transistor)	NF	f = 100 KHz, $R_S = 500\ \Omega$, $I_C = 1$ mA		—	—	1.5	—	dB	12
Gain Bandwidth Product (For Single Transistor)	f_T	$V_{CE} = 6$ V, $I_C = 5$ mA		—	—	1.35	—	GHz	11
Collector Base Capacitance	C_{CB}	$I_C = 0$, $V_{CB} = 5$V	* / **	—	—	0.28 / 0.26	—	pF / pF	8
Collector Substrate Capacitance	C_{CI}	$I_C = 0$, $V_{CI} = 5$V		—	—	1.65	—	pF	8
For Each Differential Amplifier									
Common Mode Rejection Ratio	CMR	$I_3 = I_9 = 2$ mA		—	—	100	—	dB	—
AGC Range, One Stage	AGC	Bias Voltage = 5V		2	—	75	—	dB	—
Voltage Gain, Single Ended Output	A	Bias Voltage = -4.2V, f = 10 MHz		2	—	22	—	dB	9, 10
Insertion Power Gain	G_p	f = 200 MHz, $V_{CC} = 12$V	Cascode	3	—	23	—	dB	—
Noise Figure	NF		Cascode	3	—	4.8	—	dB	—
Input Admittance	Y_{11}	For Cascode Configuration $I_3 = I_9 = 2$ mA	Cascode	—	—	1.9 + j 2.46	—	mmho	14, 16, 18
			Diff Amp	—	—	0.878 + j 1.3	—		15, 17, 19
Reverse Transfer Admittance	Y_{12}	For Diff Amplifier Configuration $I_3 = I_9 = 4$mA (each collector $I_C \simeq 2$mA)	Cascode	—	—	0 - - 0.009	—	mmho	—
			Diff Amp	—	—	0 - j 0.013	—		—
Forward Transfer Admittance	Y_{21}		Cascode	—	—	17.9 - j 30.7	—	mmho	26, 28, 30
			Diff Amp	—	—	- 10.5 + j 13	—		27, 29, 31
Output Admittance	Y_{22}		Cascode	—	—	- 0.503 - j 15	—	μmho	20, 22, 24
			Diff Amp	—	—	0.071 + j 0.62	—		21, 23, 25

*Terminals 1 & 14, or 7 & 8. (CA3102E) 1 & 12 or 6 & 7 (CA3049T)
**Terminals 13 & 4, or 6 & 11. (CA3102E) 10 & 11 or 4 & 5 (CA3049T)

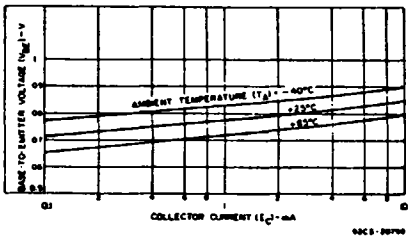


Fig. 6—Base-to-emitter voltage vs. collector current.

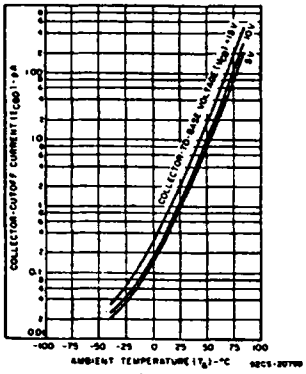


Fig. 7—Collector-cutoff current vs. temperature.

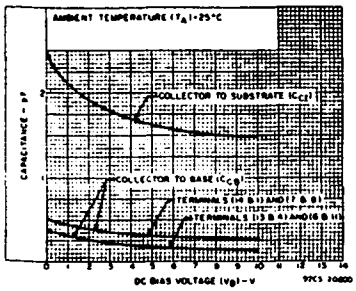


Fig. 8—Capacitance vs. dc bias voltage.

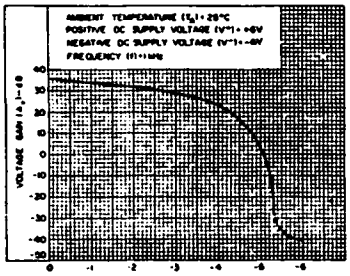


Fig. 9—Voltage gain vs. dc bias voltage.

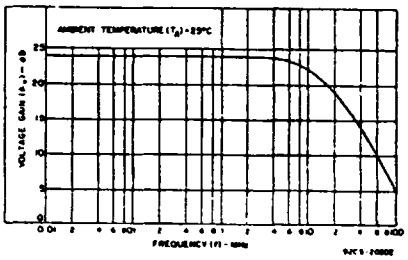


Fig. 10—Voltage gain vs. frequency.

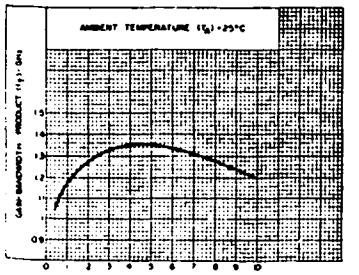


Fig. 11—Gain bandwidth product vs. collector current.

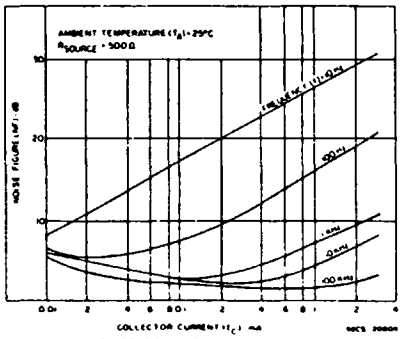


Fig. 12—1/f noise figure vs. collector current.

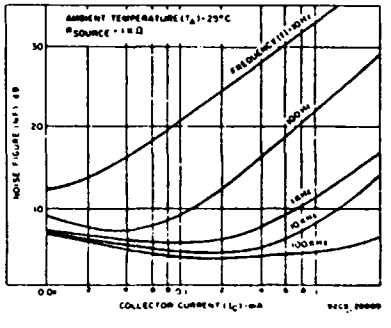


Fig. 13—1/f noise figure vs. collector current.

CA3049T, CA3102E

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		TEST CIRCUIT FIG.	CA3102E LIMITS MIN.	TYP.	MAX.	UNITS	TYPICAL CHARACTERISTICS CURVES FIG.
STATIC CHARACTERISTICS									
For Each Differential Amplifier									
Input Offset Voltage	V_{IO}			1	...	0.75	5	mV	4
Input Offset Current	I_{IO}	$I_3 = I_9 = 2$ mA		1	...	0.3	3	μA	...
Input Bias Current	I_{IB}			1		13.5	33	μA	5
Temperature Coefficient Magnitude of Input Offset Voltage	$\lvert\Delta V_{IO}/\Delta T\rvert$			1	...	1.1	...	μV/°C	6
For Each Transistor									
DC Forward Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 6$ V, $I_C = 1$ mA		...	674	774	874	mV	8
Temperature Coefficient of Base-to-Emitter Voltage	$\Delta V_{BE}/\Delta T$	$V_{CE} = 6$ V, $I_C = 1$ mA		...	...	-0.9	...	mV/°C	6
Collector Cutoff Current	I_{CBO}	$V_{CB} = 10$ V, $I_E = 0$				0.0013	100	nA	7
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1$ mA, $I_B = 0$		...	15	24	...	V	...
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10$ μA, $I_E = 0$		...	20	60	...	V	...
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10$ μA, $I_B = 0$, $I_E = 0$			20	60	...	V	...
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10$ μA, $I_C = 0$			5	7	...	V	...
DYNAMIC CHARACTERISTICS									
1/f Noise Figure (For Single Transistor)	NF	f = 100 kHz, $R_S = 500\ \Omega$, $I_C = 1$ mA				1.5		dB	12
Gain-Bandwidth Product (For Single Transistor)	f_T	$V_{CE} = 6$ V, $I_C = 5$ mA		...		1.25	...	GHz	11
Collector-Base Capacitance	C_{CB}	$I_C = 0$, $V_{CB} = 5$ V	*	...		0.28		pF	8
			**	...		0.15		pF	
Collector-Substrate Capacitance	$C_{C'}$	$I_C = 0$, $V_{CI} = 5$ V				1.65		pF	8
For Each Differential Amplifier									
Common Mode Rejection Ratio	CMR	$I_3 = I_9 = 2$ mA				100		dB	...
AGC Range, One Stage	AGC	Bias Voltage = -6V		2		75		dB	
Voltage Gain, Single Ended Output	A	Bias Voltage = -4.2V, f = 10 MHz		2	18	22		dB	9, 10
Insertion Power Gain	G_p	f = 200 MHz, V_{CC} = 12V, For Cascode Configuration, $I_3 = I_9 = 2$ mA, For Diff Amplifier Configuration, $I_3 = I_9 = 4$ mA (each collector $I_C = 2$ mA)	Cascode	3		23		dB	
Noise Figure	NF		Cascode	3		4.6		dB	...
Input Admittance	Y_{11}		Cascode	...		1.5 + j2.45		mmho	14, 16, 18
			Diff Amp			0.878 + j1.3			15, 17, 19
Reverse Transfer Admittance	Y_{12}		Cascode			0 - j0.008	...	mmho	...
			Diff Amp			0 - j0.013			
Forward Transfer Admittance	Y_{21}		Cascode			13.9 - j30.7		mmho	26, 28, 30
			Diff Amp			1.05 + j1.3			27, 29, 31
Output Admittance	Y_{22}		Cascode			0.503 - j15		mmho	20, 22, 24
			Diff Amp			0.071 + j0.62			21, 23, 25

*Terminals 1 & 14, or 7 & 8 (CA3102E) 1 & 12 or 6 & 7 (CA3049T)
**Terminals 13 & 4, or 6 & 11 (CA3102E) 10 & 11 or 4 & 5 (CA3049T)

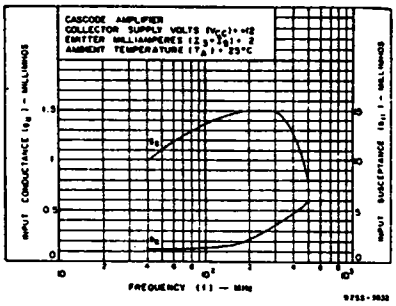


Fig. 14—Input admittance (Y_{11}) vs. frequency.

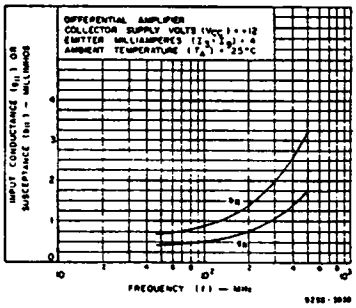


Fig. 15—Input admittance (Y_{11}) vs. frequency.

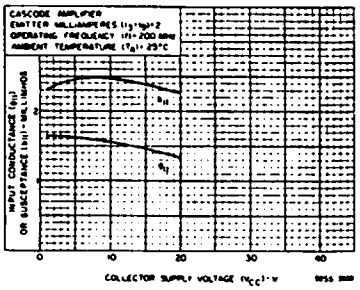


Fig. 16—Input admittance (Y_{11}) vs. collector supply voltage.

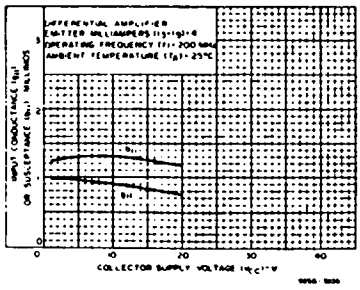


Fig. 17—Input admittance (Y_{11}) vs. collector supply voltage.

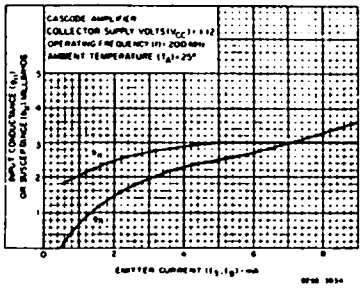


Fig. 18—Input admittance (Y_{11}) vs. emitter current.

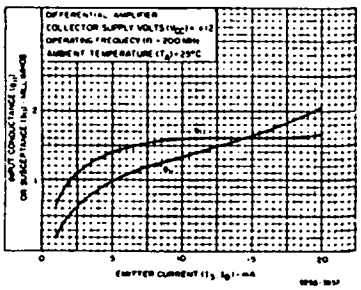


Fig. 19—Input admittance (Y_{11}) vs. emitter current.

Typical Output Admittance Characteristics for CA3049T and CA3102E

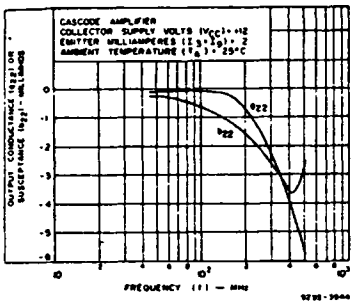


Fig. 20—Output admittance (Y_{22}) vs. frequency.

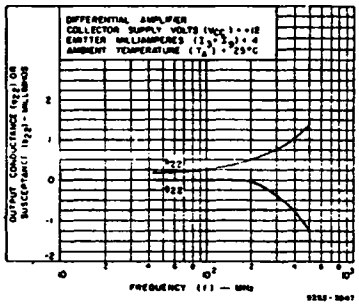


Fig. 21—Output admittance (Y_{22}) vs. frequency.

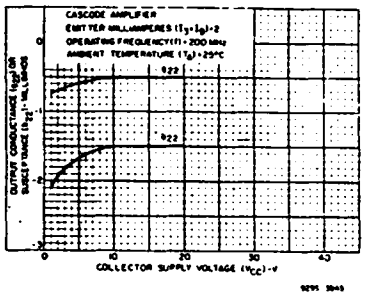


Fig. 22—Output admittance (Y_{22}) vs. collector supply voltage.

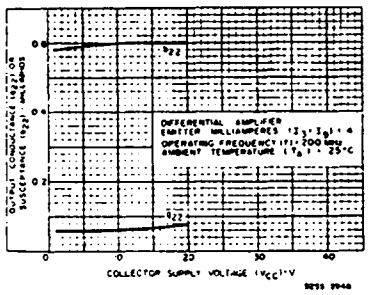


Fig. 23—Output admittance (Y_{22}) vs. collector supply voltage.

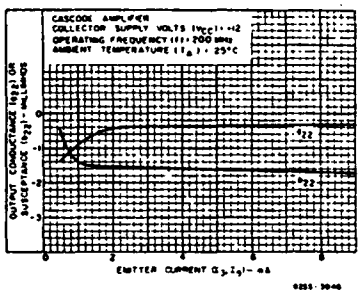


Fig. 24—Output admittance (Y_{22}) vs. emitter current.

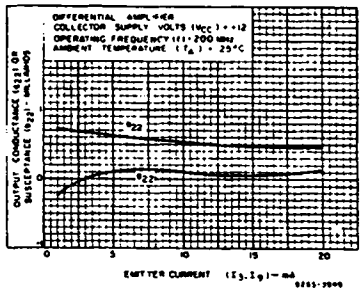


Fig. 25—Output admittance (Y_{22}) vs. emitter current.

Typical Forward Transfer Characteristics for CA3049T and CA3102E

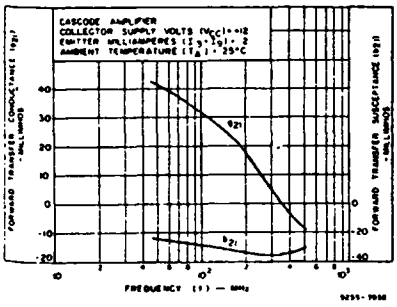


Fig. 26—Forward transfer admittance (Y_{21}) vs. frequency.

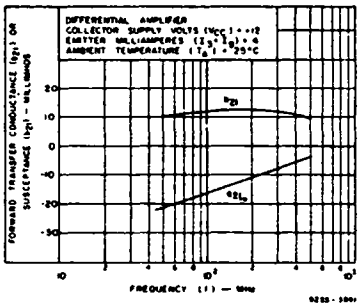


Fig. 27—Forward transfer admittance (Y_{21}) vs. frequency.

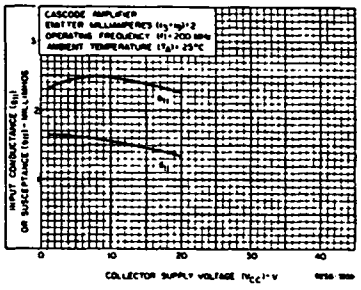


Fig. 28—Forward transfer admittance (Y_{21}) vs. collector supply voltage.

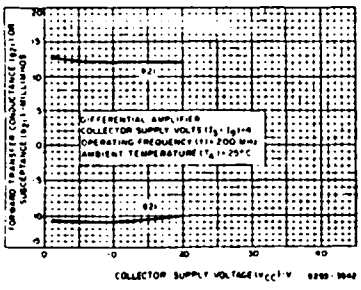


Fig. 29—Forward transfer admittance (Y_{21}) vs. collector supply voltage.

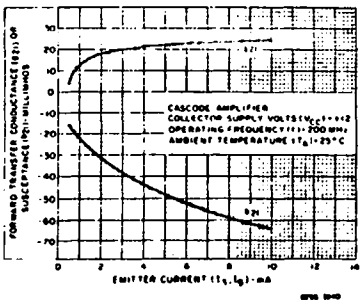


Fig. 30—Forward transfer admittance (Y_{21}) vs. emitter current.

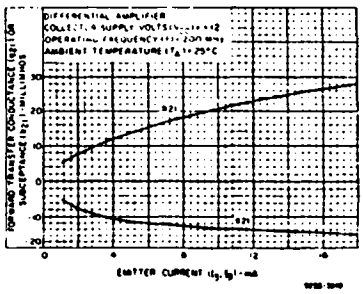


Fig. 31—Forward transfer admittance (Y_{21}) vs. emitter current.

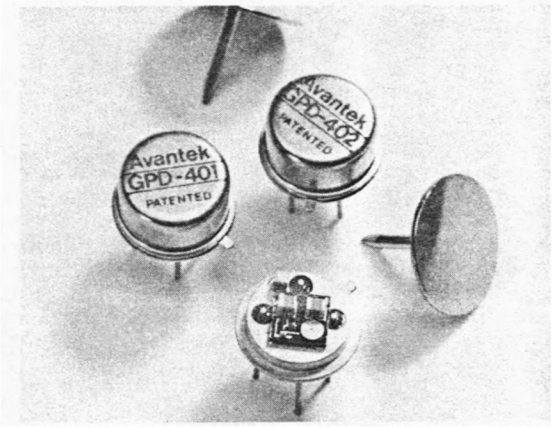
Avantek

DATA SHEET

GPD-400 Series
Patented*

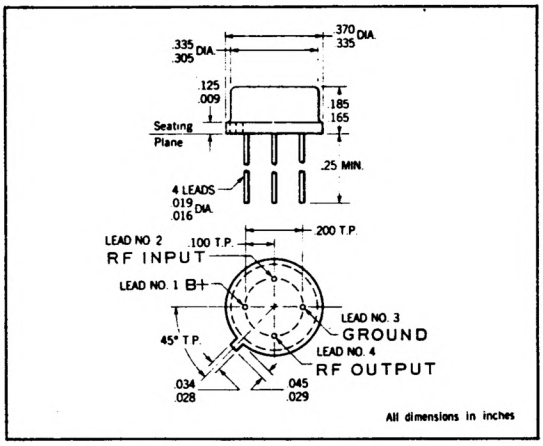
Thin Film Amplifier
5 to 400 MHz

Miniature Transistor Amplifier



FEATURES

- Low Cost
- Cascadable
- Low Profile TO-12 (4-leaded TO-5) Package
- Thin Film Sapphire Construction
- Over 6 Octaves of Amplifier Bandwidth
- Avantek® Silicon Transistor Chips



DESCRIPTION

The GPD is a complete transistor amplifier, ready to operate in a microstrip circuit upon application of DC voltage. Packaged in a miniature TO-12 transistor package, the Avantek® GPD serves as a completely cascadable amplifier, without bandwidth shrinkage, from 5 to 400 MHz. The low frequency response of the GPD-460 series may be set arbitrarily low by selection of external series input and output capacitors, and the DC bypass capacitor.

The Avantek GPD is an entirely new kind of basic device, designed to provide the circuit engineer major savings in both time and money. Various gain and power output choices are available to permit the user to cascade modules to meet the performance characteristics required in his equipment design. Small size, excellent performance, ready availability and substantial cost savings in equipment manufacture and parts handling are significant advantages that can be gained over standard discrete component methods of manufacture by the use of GPD amplifiers. The costly and time-consuming problems accompanying in-house amplifier design, construction and testing can be totally avoided by inserting GPD's, either singly or cascaded, into a system circuit.

The Avantek GPD is a wideband, single-stage unit of gain, featuring flat response across its greater-than-six-octave bandwidth. The tiny GPD modular amplifier is made with highly reliable ceramic substrates, Avantek microwave transistor chips, thin film circuits, thin film resistors and chip capacitors. All the complex circuitry is encapsulated inside the tiny TO-12 package. The using engineer is spared the normal frustrating RF design problems — impedance matching networks, feedback loops, biasing and stabilization elements.

APPLICATIONS:

The GPD-400 Series amplifier is designed for applications requiring very broadband amplifiers, preamplifiers, isolation amplifiers, and IF amplifiers. The patented circuit design of the GPD permits cascading of units to achieve gain up to any desired level without interstage matching when cascaded in 50-ohm systems. The specified band edges (5 to 400 MHz) are not 3 dB points, but are the points between which the specified gain performance is guaranteed. The low frequency response of the GPD-460 units may be set as close to DC as required.

* U.S. Patent 3493882

Avantek, Inc., Advanced solid-state products • 3175 Bowers Avenue, Santa Clara, California 95051 • Phone (408) 249-0700 • TWX 910-339-9274 • Telex 34-6337

INSTALLATION AND OPERATING INSTRUCTIONS:

Installation of the GPD amplifier is similar to the installation of any standard semi-conductor product in a TO-8 or TO-5 package. A clamp is provided to secure the GPD firmly to the ground plane. This step insures positive contact between the GPD package and the ground plane so that no problems with VSWR or oscillation in a multi-stage system will be encountered.

The GPD amplifier is designed for use in a 50-ohm microstrip system. It can be used in other impedance systems, but performance may be degraded.

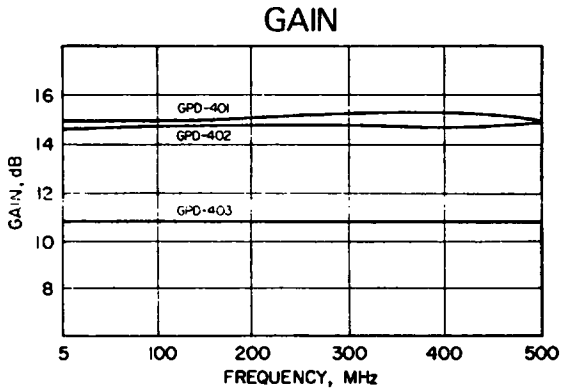
The microwave transistor used in the GPD must be protected from current surges which may be generated by energy storage in system capacitances. Always remove bias voltages from the GPD before inserting or removing the unit under test.

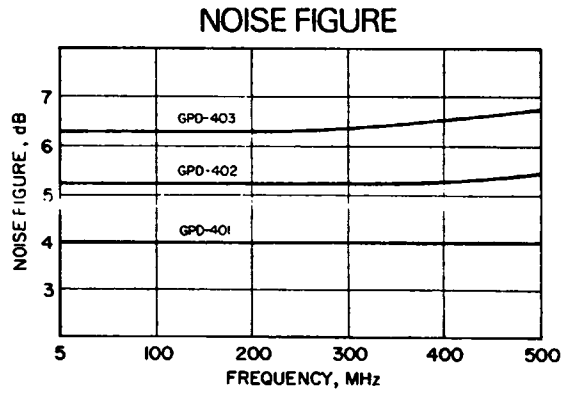
The use of a high-pass filter and/or pad is recommended at the output of gas-discharge-tube noise sources. This protects the transistor in the amplifier from possible high-level ignition-pulse transients which may appear at the RF output ports of these generators (see appropriate manufacturer's literature for further details).

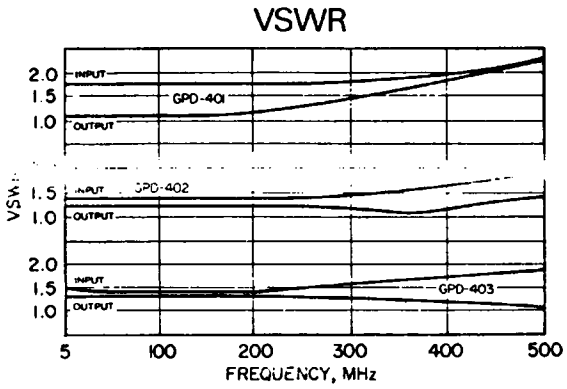
The amplifiers may be stored at temperatures from -65°C to +200°C. The transistors are silicon and all metallization is gold. The operating case temperature is specified at +71°C (+160°F). The amplifiers will operate reliably at temperatures through +125°C (+257°F) although an external heat sink should be used, particularly on the GPD-403.

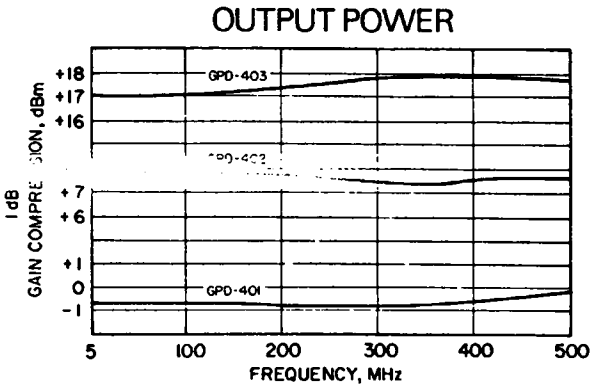
More information concerning applications and use of the GPD amplifier is available from Avantek. Write for the Applications Bulletin *Designing With GPD Amplifiers.*

TYPICAL PERFORMANCE









GUARANTEED SPECIFICATIONS

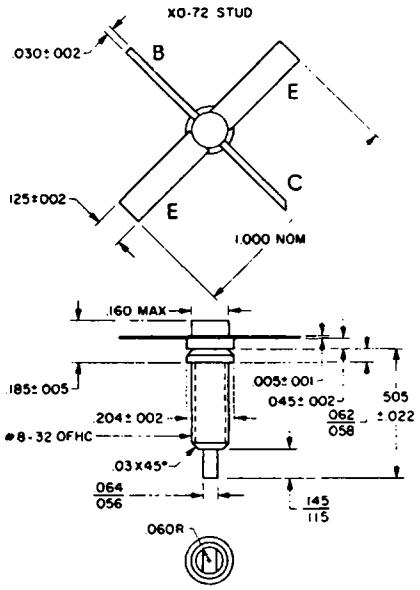
Model	Frequency Response (MHz) Minimum	Gain (dB) Minimum	Flatness (dB) Typical	Noise Figure (dB) Typical	Reverse Isolation (dB) Typical	Power Output for 1 dB Gain Compression (dBm) Typical	Avantek Intercept Point for IM Products (dBm) Typical	VSWR (50 ohms) Typical In	VSWR (50 ohms) Typical Out	Input Power Volts DC	Input Power Current (mA) Typical	Storage Temperature (°C)	Weight (grams)
GPD 401	5-400	13	1.0	4.5	20	2	+8	2.0	2.0	15	10	-65 to +200	1.0
GPD 461	Same as GPD 401, except three external capacitors are required to establish low frequency roll-off												
GPD-402	5-400	13	1.0	6.0	20	+6	+18	2.0	2.0	15	24	-65 to +200	1.0
GPD 462	Same as GPD 402, except three external capacitors are required to establish low frequency roll-off.												
GPD-403	5-400	9	1.0	7.5	20	+15	+26	2.0	2.0	24	65	-65 to +200	1.0
GPD 463	Same as GPD 403, except three external capacitors are required to establish low frequency roll-off												

COMMUNICATIONS TRANSISTOR CORPORATION

E1E
F1E

MICROWAVE ● CLASS A LINEAR RF POWER TRANSISTORS

GENERAL DESCRIPTION - The E1E & F1E are specifically designed for operation in Class A broadband or narrow-band applications covering the frequency range of 200-3000 MHz.

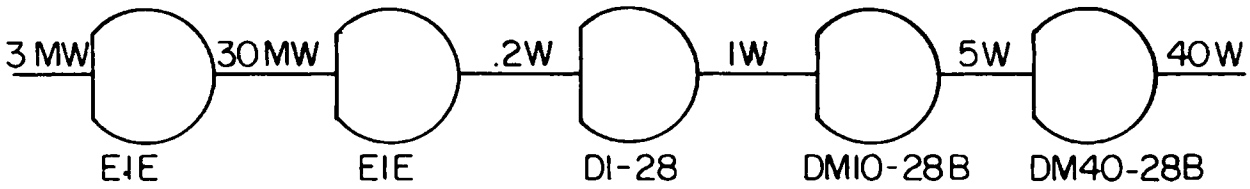


Note: Studless package also available

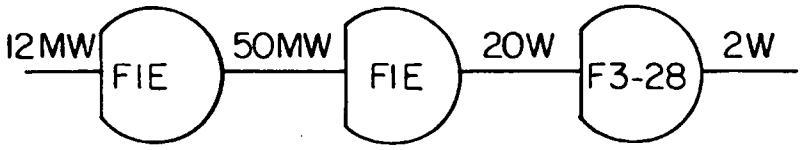
FEATURES

- SUPERIOR LINEARITY DUE TO HIGHER f_T.
- MAXIMUM RELIABILITY DUE TO SINGLE CHIP CONSTRUCTION.
- GREATER HIGH FREQUENCY PERFORMANCE IN LOW INDUCTANCE CERAMIC STRIPLINE PACKAGES.
- IDEAL FOR USE IN LINEAR APPLICATIONS REQUIRING OPERATION IN CLASS A DUE TO IMPROVED FORWARD BIASED SAFE AREA.

750-1000 MHz



2100-2300 MHz

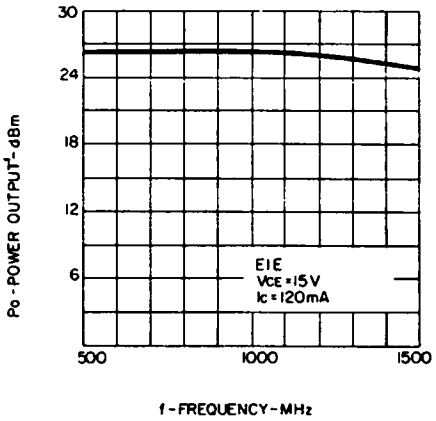


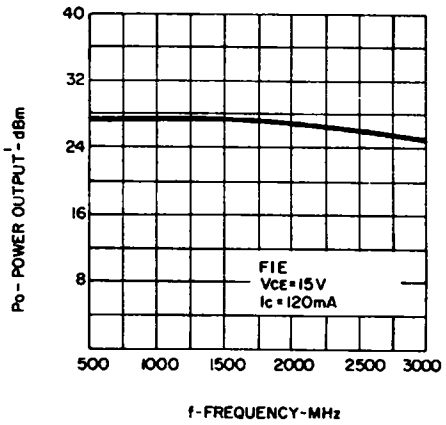
COMMUNICATIONS TRANSISTOR CORPORATION
301 Industrial Way, San Carlos, California 94070

An Affiliate of Eimac/Varian
(415) 591-8921 TWX 910-376-4893

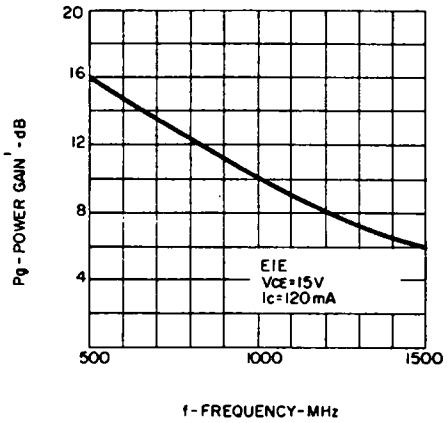
COMMUNICATIONS TRANSISTOR E1E ● F1E

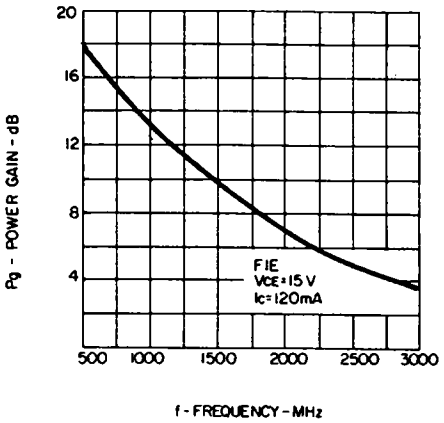
POWER OUTPUT VERSUS FREQUENCY



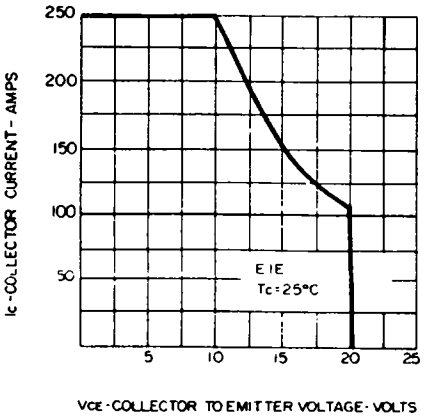


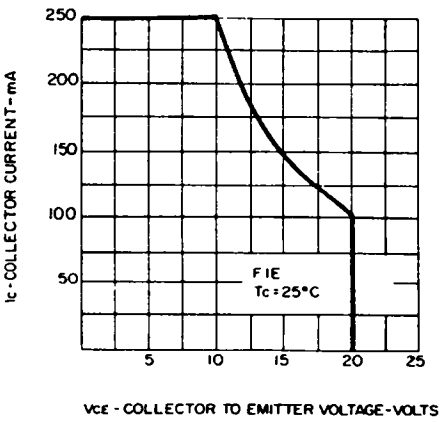
POWER GAIN VERSUS FREQUENCY





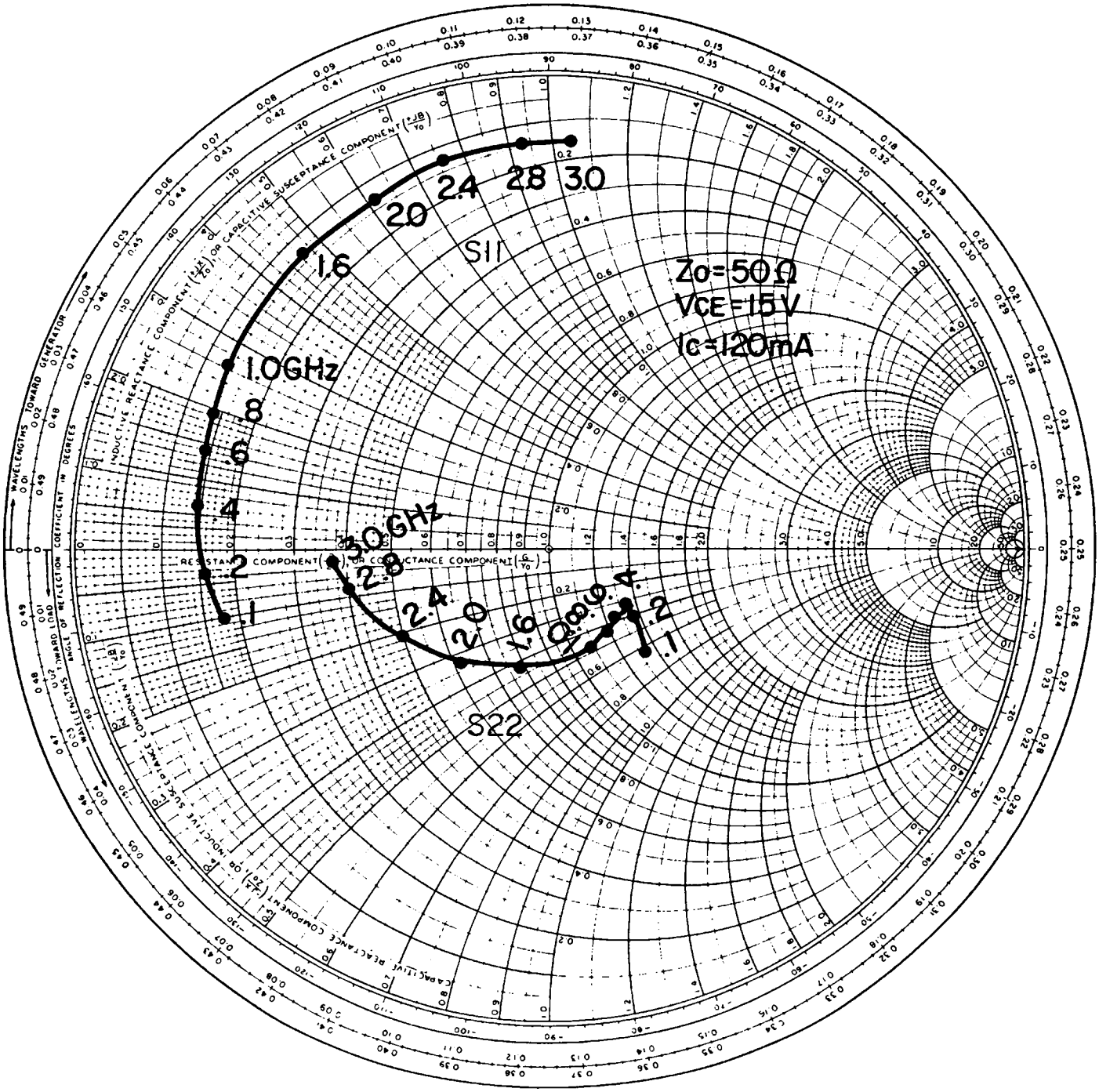
DC SAFE OPERATING AREA





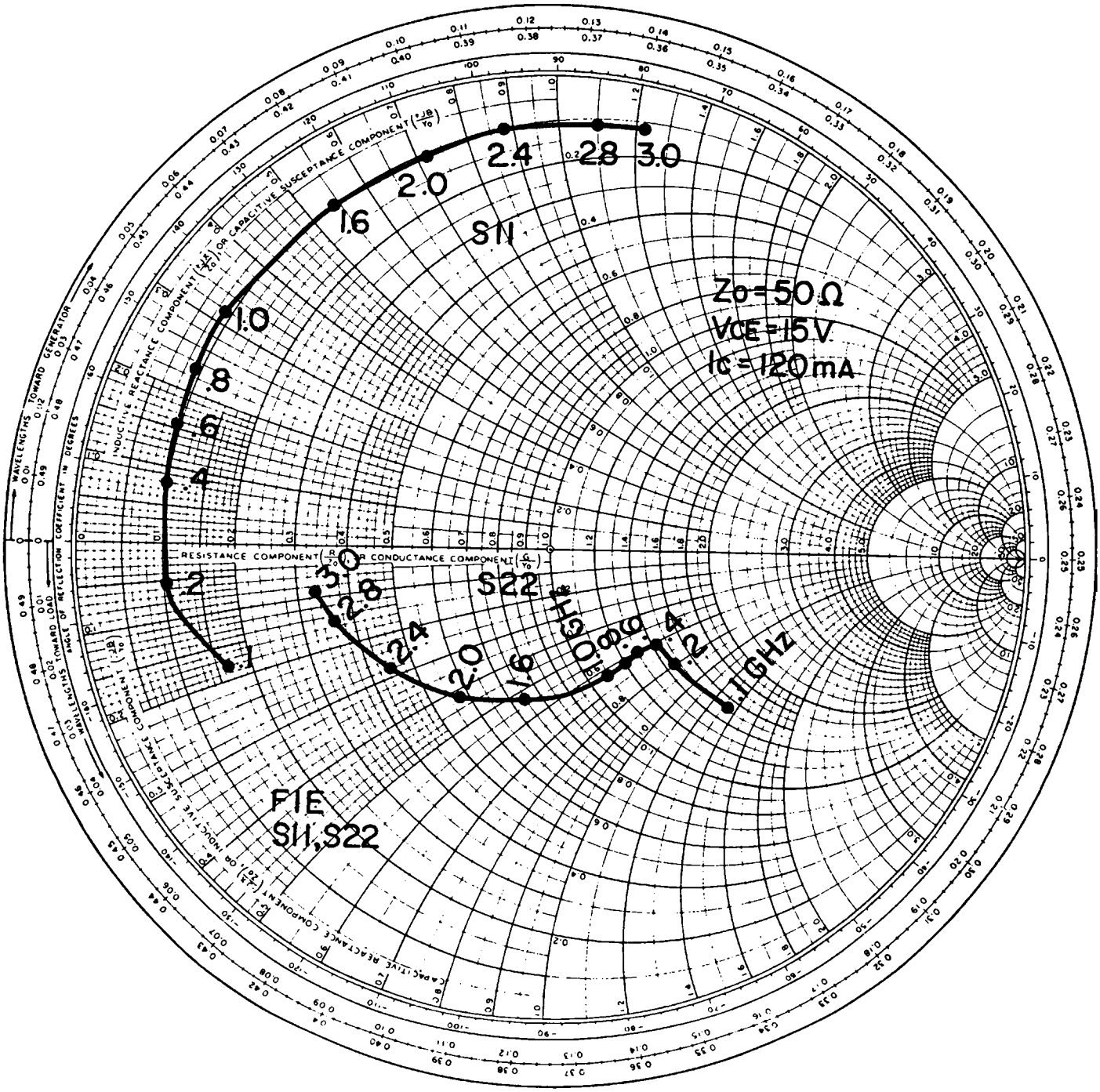
COMMUNICATIONS TRANSISTOR E1E ● F1E

E1E S11, S22



COMMUNICATIONS TRANSISTOR E1E ● F1E

F1E S11, S22



COMMUNICATIONS TRANSISTOR E1E ● F1E

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

MAXIMUM TEMPERATURES	E1E	F1E
Storage Temperatures	-65° C to + 200° C	-65° C to + 200° C
Operating Junction Temperatures	200° C	200° C
Lead Temperature (Soldering 8 seconds time limit) ≤ 1/32" from Ceramic	260° C	260° C
MAXIMUM POWER DISSIPATION (Note 2)		
Total Power Dissipation at 25° C Case Temperature	5.3 W	5.3 W
MAXIMUM VOLTAGES AND CURRENT		
BV_{CBO} Collector to Base Voltage	50 V	50 V
BV_{EBO} Emitter to Base Voltage	4 V	4 V
LV_{CEO} Collector to Emitter Voltage	20 V	20 V
I_C Collector Current	.25 A	.25 A

ELECTRICAL CHARACTERISTICS (25° C unless otherwise specified)

SYMBOL	CHARACTERISTIC	E1E	F1E	UNIT	LIMIT	TEST CONDITIONS
	100% TESTED AND GUARANTEED					
P_g	Power Gain (Note 3)	9.0		dB	MIN.	f = 1 GHz
			7.0	dB	MIN.	f = 2 GHz
LV_{CEO}	Collector to Emitter Voltage	20	20	VOLTS	MIN.	Ic = 10 mA
BV_{EBO}	Emitter to Base Voltage	4.0	4.0	VOLTS	MIN.	Ic = 5 mA
BV_{CBO}	Collector to Base Breakdown Voltage	50	50	VOLTS	MIN.	Ic = 10 mA
H_{fe}	Current Gain	20	20	---	MIN.	V_{CE} = 5V, Ic = 50 mA

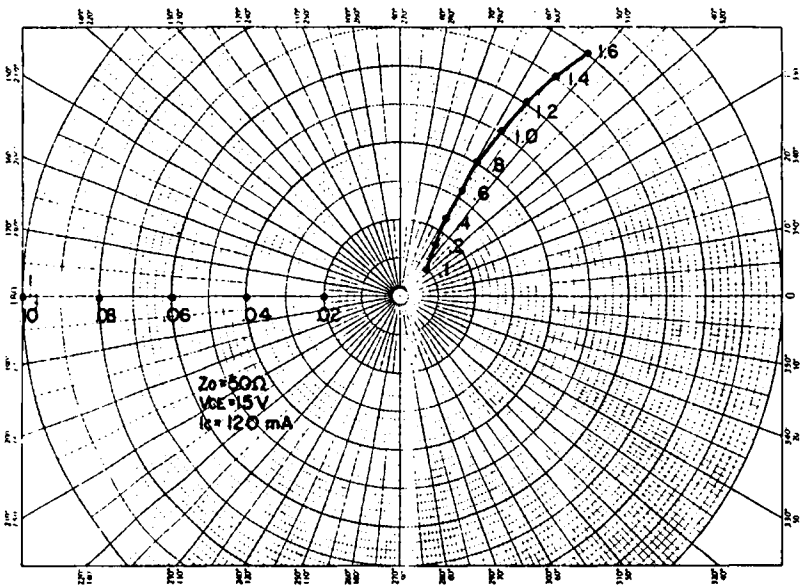
NOTES:

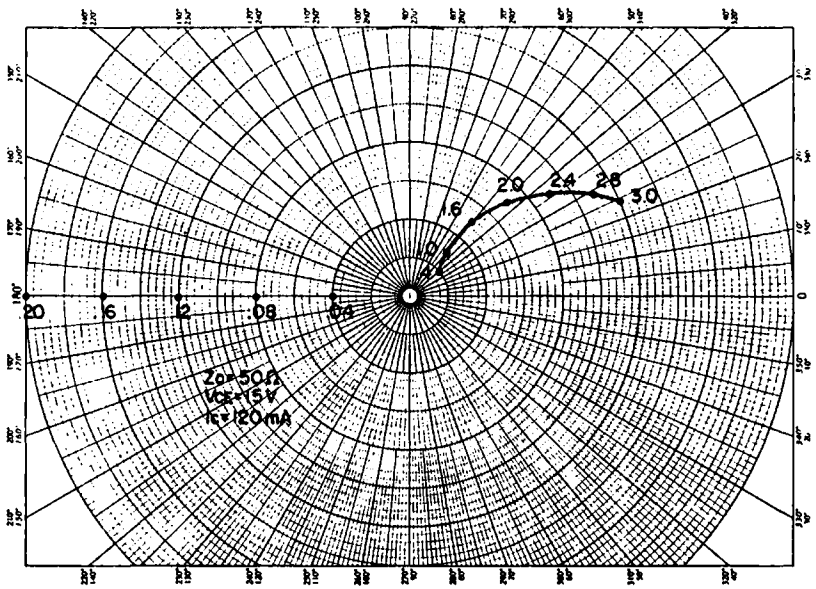
1. At 1 dB compression point.
2. These ratings give a maximum junction temperature of 200° C with junction to case thermal resistance of 33° C/watt.
3. Values measured at bias point: V_{CE} = 15 Volts, Ic = 120 mA.

COMMUNICATIONS TRANSISTOR E1E ● F1E

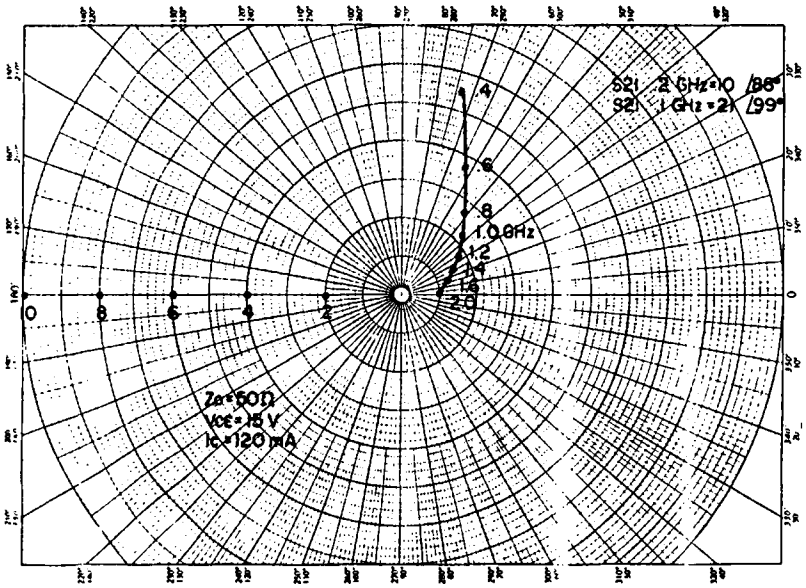
E1E F1E

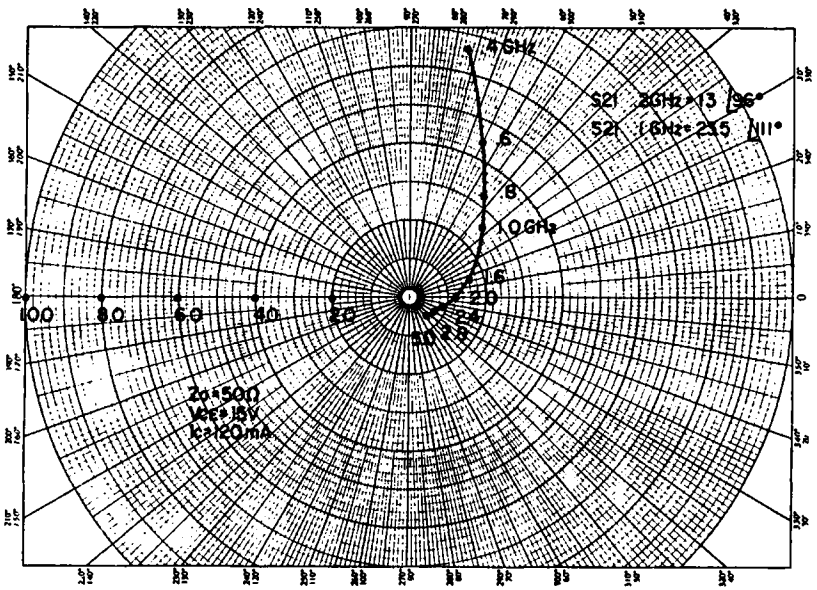
S12





S21





COMMUNICATIONS TRANSISTOR CORPORATION

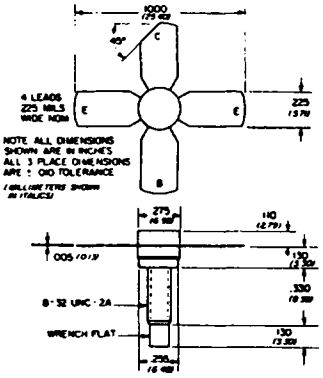
CD2810

CT 2.5.8.0E Feb. 1978

HIGH EFFICIENCY ULTRA-LINEAR TRANSISTOR

GENERAL DESCRIPTION - This device is a silicon NPN transistor designed for high efficiency high linearity class A operation in UHF (bands IV and V) television transmitters and transposers.

PACKAGE



Maximum Voltages and Currents

BV_{CES}	Collector to Emitter Voltage	50 V
BV_{EBO}	Emitter to Base Voltage	4.0 V
I_C	Collector Current	0.5 A

ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
$P_{O\ sync}$[1]	Power Output	.75	0.9		WATTS	f_{vision} = 800 MHz Vcc = +25V I_C = 200 mA dim = -60 dBc
G_P	Power Gain	8.0	9.2		dB	f_{vision} = 800 MHz Vcc = +25V I_C = 200 mA dim = -60 dBc
η_C	Collector Efficiency		18		%	f_{vision} = 800 MHz Vcc = +25V I_C = 200 mA dim = -60 dBc
Θ_{jc}[2]	Thermal Resistance Junction to Case		11.0	13.0	°C/W	IR Scan Vcc = +25V I_C = 200 mA
h_{FE}	DC Current Gain		50			I_C = 100 mA V_{CE} = +5V
C_{OB}	Collector to Base Capacitance		4		pF	V_{CB} = +25V I_E = 0 f = 1.0 MHz
BV_{EBO}	Emitter to Base Voltage	4			VOLTS	I_E = 5 mA
BV_{CES}	Collector to Emitter Voltage	50			VOLTS	I_C = 20 mA

NOTES:

1. European three tone test method: vision carrier -8 dB, sound carrier -7 dB, sideband signal -16 dB, O dB corresponds to peak sync level.
2. This rating gives a maximum power dissipation rating of 15 watts at a maximum junction temperature of 200° C.

COMMUNICATIONS TRANSISTOR CORPORATION
301 Industrial Way, San Carlos, California 94070

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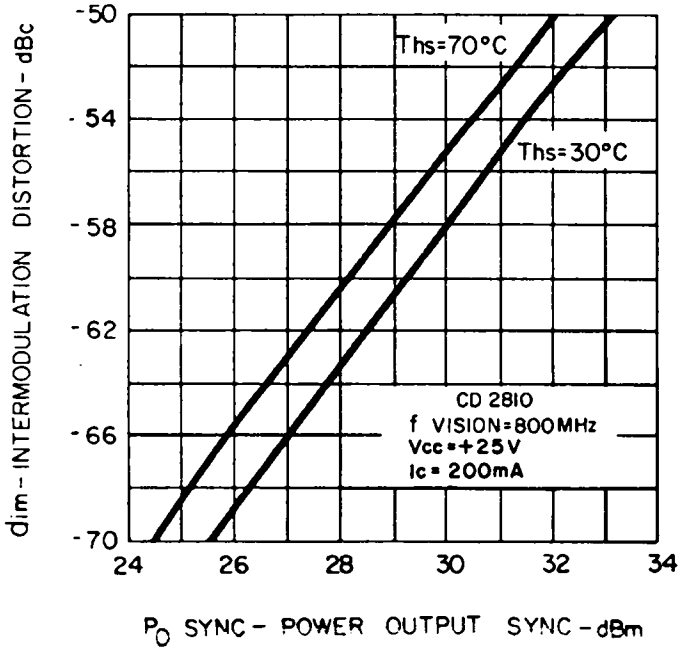
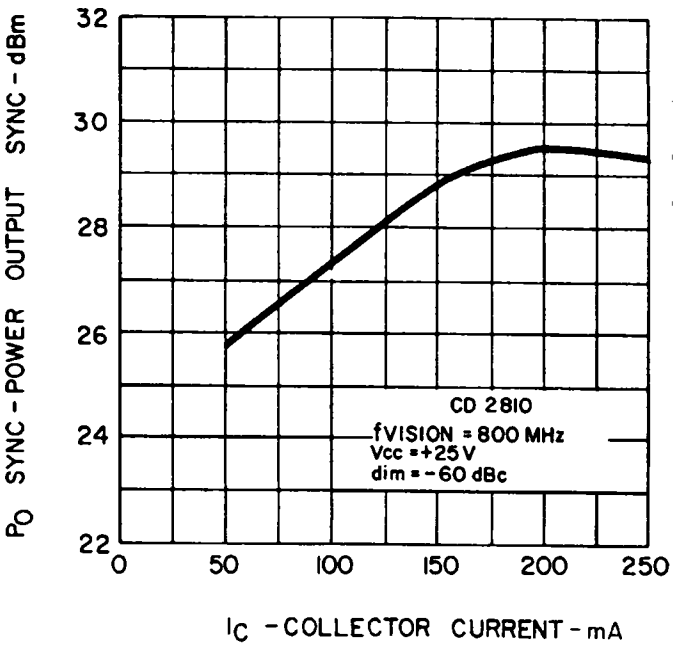
COMMUNICATIONS TRANSISTOR CD 2810

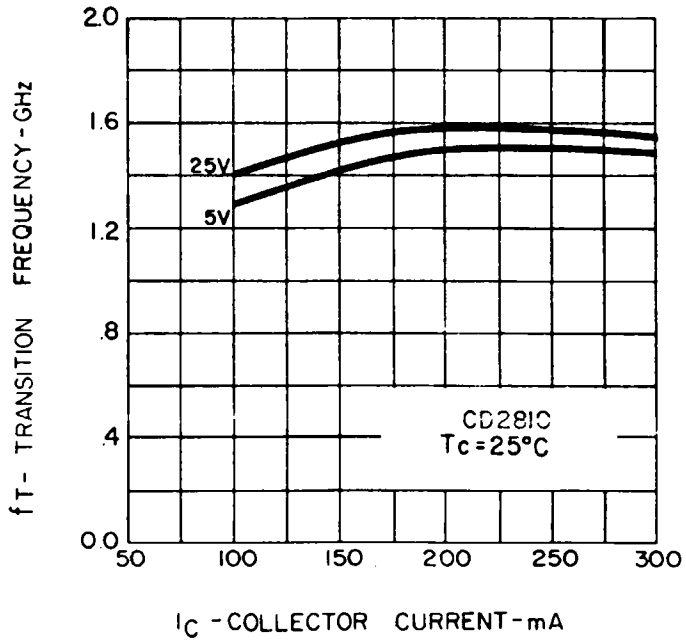
INTERMODULATION DISTORTION vs Po SYNC



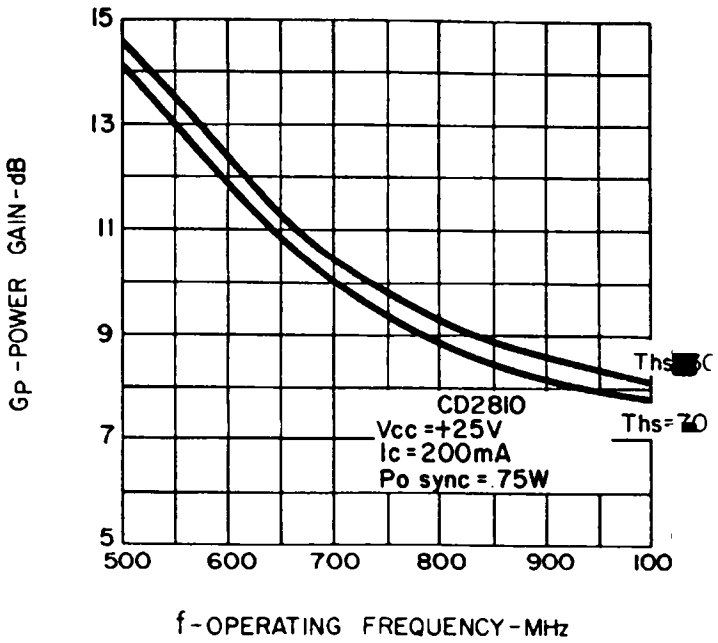
POWER OUTPUT SYNC vs COLLECTOR CURRENT



TRANSITION FREQUENCY vs COLLECTOR CURRENT

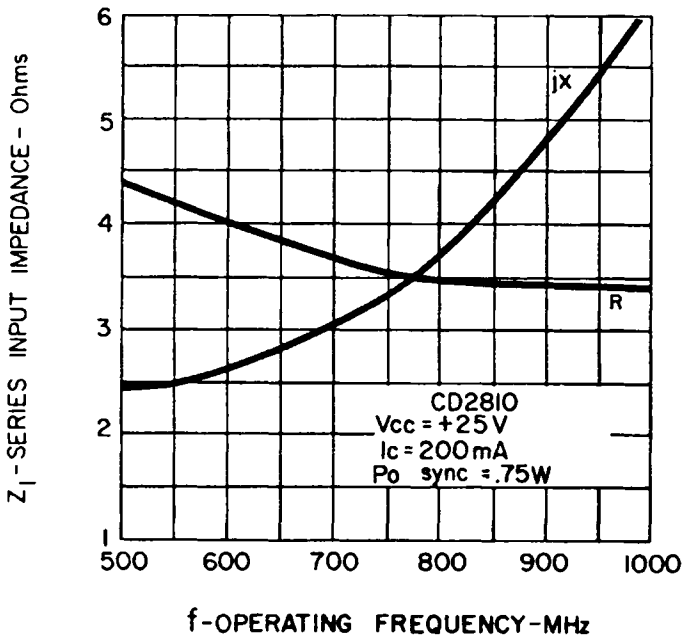


POWER GAIN vs OPERATING FREQUENCY

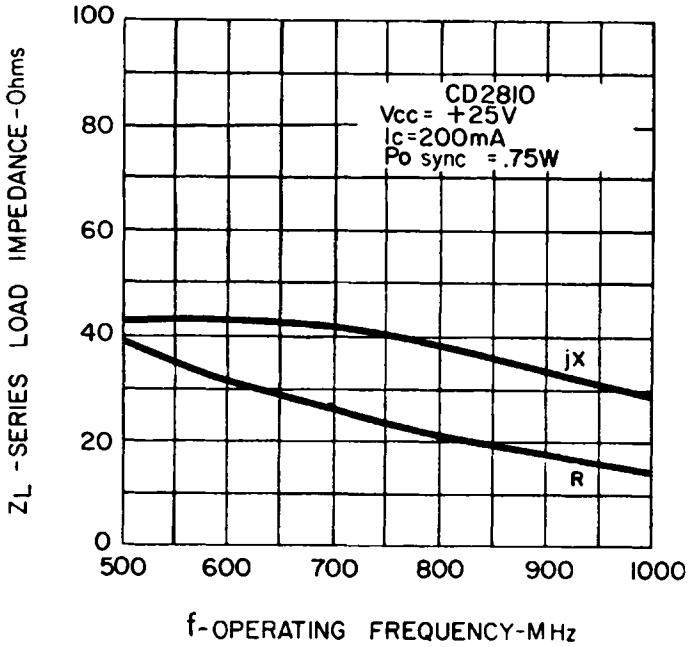


COMMUNICATIONS TRANSISTOR CD 2810

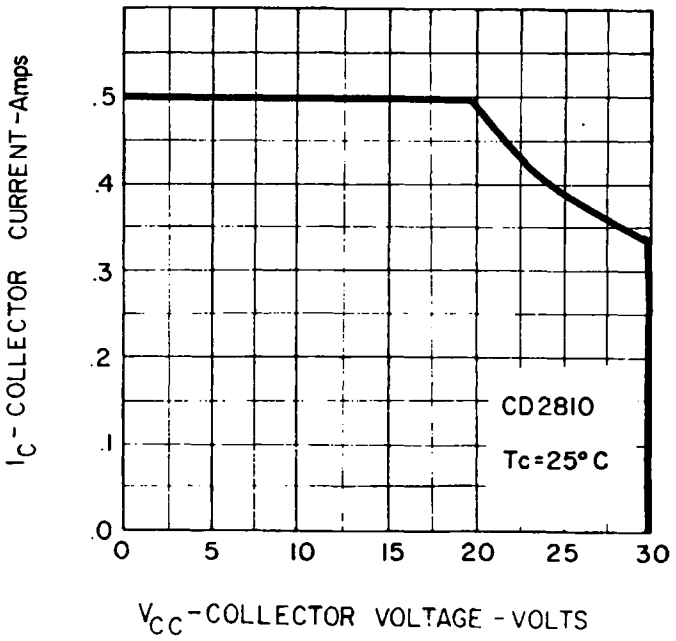
INPUT IMPEDANCE vs OPERATING FREQUENCY

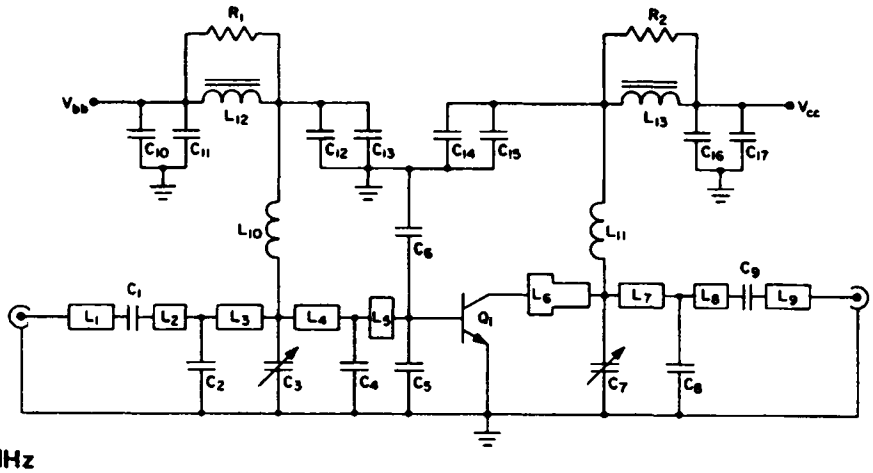


LOAD IMPEDANCE vs OPERATING FREQUENCY



DC SAFE OPERATING AREA





470-860 MHz
Broadband Linear Power Amplifier
UHF TV Bands IV and V

(Bias not shown)

Q1 CD2810

C_1	8.2 pf	ceramic chip	ATC pkg B
C_2	1.0 pf	ceramic chip	ATC pkg B
C_3, C_7	.8 - 10 pf	Air tuned	Johannson
C_4	4.7 pf	ceramic chip	ATC pkg B
C_5	10 pf	ceramic chip	ATC pkg A
C_8	3.0 pf	ceramic chip	ATC pkg B
C_9	22 pf	ceramic chip	ATC pkg B
C_6	12 pf	ceramic chip	ATC pkg A
C_{10}, C_{17}	1 μf	electrolytic	Sprague
C_{11}, C_{16}	10 μf	electrolytic	Sprague
C_{12}, C_{15}	220 pf	ceramic chip	ATC pkg B
C_{13}, C_{14}	390 pf	ceramic chip	ATC pkg B
L_1, L_9	.154" wide line		any length
L_2	.154" wide line		.115" long
L_3	.154" wide line		.785" long
L_4	.154" wide line		.650" long
L_5	.275" wide line		.300" long
L_6	.275" wide line		.300" long followed by .154" wide line, .345" long
L_7	.154" wide line		1.050" long
L_8	.154" wide line		.135" long
L_{10}	4.7 μh deciductor		
L_{11}	½ turn #22 wire, I. D. = .150"		
L_{12}, L_{13}	6 turns #20 wire on F 627-8Q toroid		
R_1, R_2	15 Ω 10% ½ Watt carbon		

BOARD MATERIAL = 1/16" teflon fiberglass

7.0 APPENDICES

7.1 Baseband System Specifications (L. R. D'Addario 7/19/78)

Goals:

1. In the complete signal processing, loss of sensitivity due to non-ideal bypass should be <5%.
2. Closure errors (which result from mismatch between antennas) should be <1° phase, <1% amplitude.

To achieve this, gain flatness must be better than 4 dB (pp). I believe we can afford to allocate 1.5 dB of this to the IF receiver subsystem (including IF Converter), neglecting any contribution from the filters. In addition, to meet Goal 2 above, matching between units must be better than 5° in phase (peak difference) and 0.3 dB in amplitude. Most of this is already allowed in the filters, but I think we can allow 2.5° and 0.2 dB in the rest of the subsystem.

Thus we have the following specification for T3, T4, T5 combined, excluding the filters:

For frequencies 0.19 to 50.0 MHz -

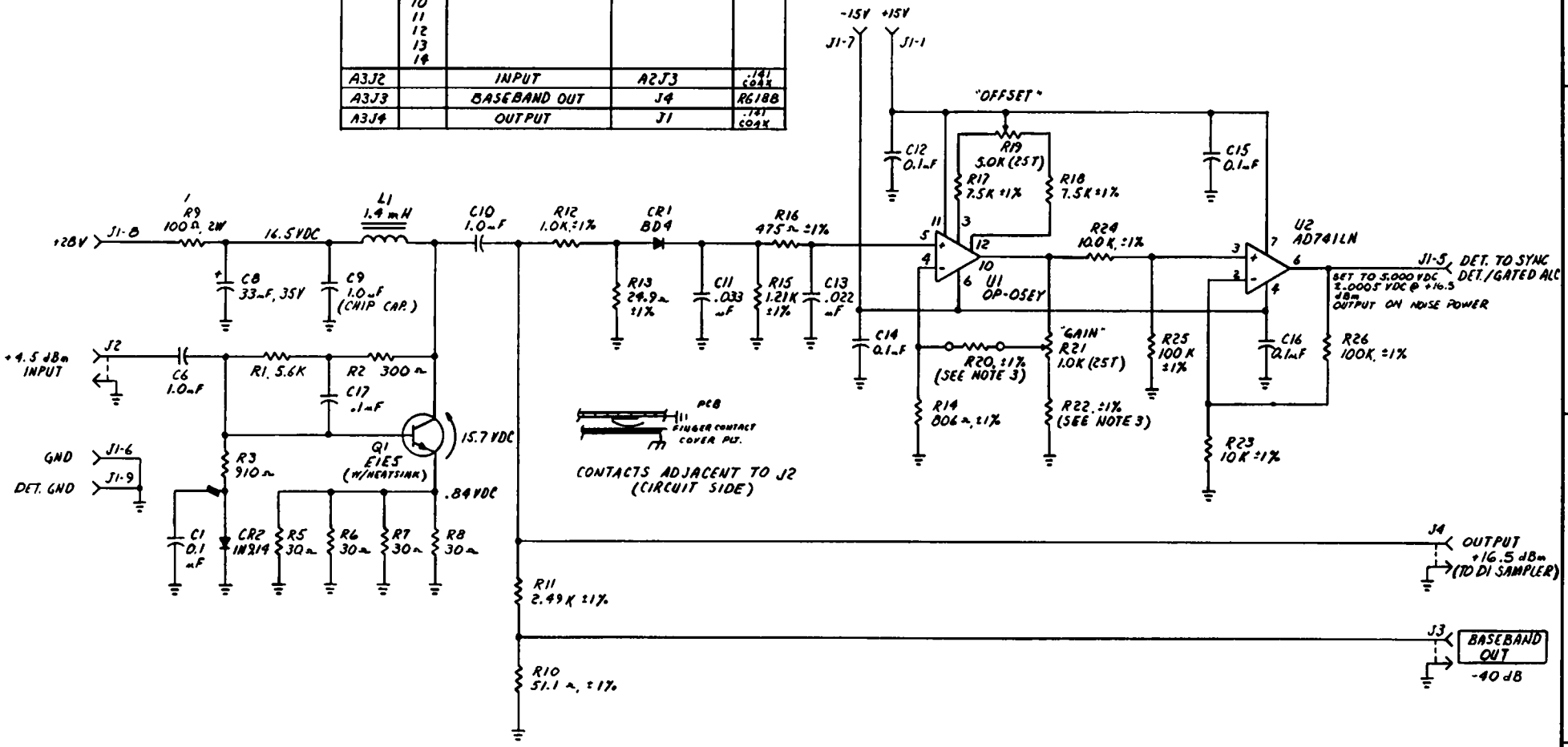
1. Gain flatness shall be $\leq$1.5 dB peak to peak.
2. Ratio of gains of any two units shall be constant with frequency to ±0.1 dB (0.2 dB pp).
3. Difference between two units of departures from linear phase shall not exceed ±2.5°.

7.2 Power Amp/Square Law Detector Assembly A3A (FOR REFERENCE ONLY)

NOTES:
1. ALL RESISTORS ARE 1/4 W ±5% UNLESS OTHERWISE SPECIFIED.
2. FUNCTIONS SHOWN THUSLY [A2...] ARE MARKED ON MODULE FRONT PANEL.
3. THE VALUE OF R20 & R22 IS DETERMINED AT ASS'Y. SHOULD R20 BE 50K Ω OR LESS, R22 WILL NOT BE REQD.

CONN.	PIN	FUNCTION	SOURCE	COLOR
A3J1	1	+15V	L2B	RED
	2			
	3			
	4			
	5	DET	A1P1-7	WHT/GRN
	6	GND	CHASSIS GND "B"	BLK
	7	-15V	L3B	YEL
	8	+28V	L4B	GRY
	9	DET. GND	~	~
	10			
	11			
	12			
	13			
	14			
A3J2		INPUT	A2J3	.141 COAX
A3J3		BASEBAND OUT	J4	RG188
A3J4		OUTPUT	J1	.141 COAX

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
D	7/11/77			REDRAWN DUE TO CKT CHG ASSOC WITH Q1
E	6/6/79			REV PER "AS BUILT" COND
F	6/8/79			REV - DWG ERROR
G	4/20/83			CHGS. IN TABLE
H	9/2/79			C17 WAS .01 uF/CHG LVL



FOR REF. ONLY

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:

NEXT ASSY	USED ON

PROJECT: T5-B

TITLE: POWER AMP. / SQ. LAW DET. PCB SCHEMATIC "A3"

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY | DATE
DESIGNED BY | DATE
APPROVED BY | DATE

SHEET NUMBER | DRAWING NUMBER C13B2055 | REV H | SCALE