VLA Technical Report No. 52

DCS SYSTEM TEST BENCH THEORY AND OPERATIONS USER'S GUIDE

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April, 1982

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I. INTRODUCTION

The purpose of this report is to provide the reader with a working reference for the DCS System Test Bench and its use in the checkout procedure for both the DCS system modules and for laboratory checkout of complete racks prior to installation in antennas. It is assumed that the reader is moderately familiar with the workings of both small scale computers and the Monitor and Control system modules.

Suggested reading for those not familiar with these systems include the DCS System Manual and the Data Set, Data Tap, Central and Antenna Buffer Manuals as well as Technical Report #29, for an overview of the complete VLA electronics systems.

Additional materials for those interested in the computer hardware and software interfaces include: Intel MDS-800 Hardware and Software Manuals, Intel 8080/85 User's Reference Manual and the CP/M 2.2 Operating System User's Manual set, as well as the appropriate programming language manuals.

II. DCS SYSTEM GENERAL THEORY OF OPERATION

The DCS system can be thought of as a bi-directional link between the various VLA electronics subsystems and the MODCOMP computers which are the system controllers and data processors. The subsystems include such items as the front end receivers, the LO/IF systems, the antenna control units, and the focus feedmount subreflector systems.

Figure 1 is a generalized block diagram of the monitor and control system. The serial line controller, the heart of the DCS system, is responsible for 1) polling each central buffer in turn and effecting transfers of this data to the MODCOMPS, 2) rebroadcasting the data received from each central buffer to all other buffers in the system, and 3) extracting commands from the MODCOMPS, reformatting them into a standard 45 bit word and broadcasting them to all central buffers. All data transfers between the SLC and the MODCOMPS are via 16 bit parallel words, while elsewhere in the system, a standard 45 bit serial word is used for commands and monitor data. The 45 bit word format is shown in Figure 2.

The central buffers, contained in the D racks located in the Control Electronics Room (CER), receive all commands issued by the computers and do a comparison between the DCS command address and the DCS address for which each central buffer is hard-wired. If the DCS addresses match, the buffer then does a quick check to determine whether it is a command destined for the local data set (#5) or a command for one of the antenna data sets (DS#0-3). The commands are loaded into one of the command buffer memories in the central buffer and output to either the local data set or the antenna buffer (via the LO/IF XMTR RCVRS) at the proper unload times.

The antenna buffer sends 10 monitor words to the central buffer during each Waveguide Communications Cycle (WCC) for storage and unloading to the SLC. In addition to handling commands to the local data set, the central buffer outputs 2 'Q' characters to query data set #5 (i.e. precipitate transmission of a monitor word from the DS to the central buffer). These monitor words are placed in the monitor word buffer memory within the C.B. for later transmission to the SLC.

The antenna buffer (located in the B rack) receives commands from the central buffer and stores them in a buffer memory for unloading later to all antenna data sets simultaneously. The A.B. also generates 2 Q's per data set and saves the resulting monitor words in another buffer memory for unloading to the central buffer. The A.B. contains a simple circuit which counts the number of commands received during one waveguide cycle and responds as data set #4 with a data multiplex address (or MUX) of '205. The data readback is six identical nybbles (4 bits) whose value is the number of commands received in a given WCC cycle. Data set #4 is treated as a real data set, however, it can't be commanded.

Data set #4 is also used to fill the monitor word buffer in the antenna buffer in the event that a data set does not respond to the buffer. The forced data set data shows up with a mux address of '205 in place of the missing data set. The data portion of the forced message is a valid command count for this waveguide cycle.

Another specialized circuit within the antenna buffer reads the antenna serial number hardwired in the B rack and transmits this data through data set #2 to the MODCOMPS. This data is formatted as three

redundant bytes (8 bits) and is used by the computer to determine the antenna origin of the data.

All data sets throughout the system are identical with one minor exception to be discussed later. The data set is the interface unit for the various electronics subsystems to the computers. The data set is capable of monitoring up to 128 discrete analog voltage points and 64 digital data points as well as relaying 48 external commands and executing 16 internal commands, of which only 3 are used.

Upon receipt of a command, the data set does a parity check and address comparison to verify that no transmission errors have occured. All extraneous bits (parity, start and addressing) are stripped from the command. The remaining data and associated mux address are unloaded to the intended module.

This handshaking relationship is used in a similar fashion for the gathering of digital data by the data set. The digital data is clocked out of a serial source register into the data set when the proper MUX state of the data set is attained, i.e. when the data set is ready for digital data from a given monitor point.

Analog sampling is more simplistic in that the other modules track the data set's SMA states and present the desired analog voltages on one of eight differential analog inputs to the data set, until the D.S. goes to its next state, at which time the next input is presented. Analog data is multiplexed into a single channel of information and is applied to a 12 bit A/D converter whose outputs are temporarily stored in a set of latches. The D.S. always does analog conversions in pairs and the 2 resulting 12 bit conversions are packed into a 45 bit word along with addressing and parity information, allowing for maximum thru-put.

Digital data consists of 24 bits/monitor point and consumes one entire 45 bit word, when the addressing and parity data is added. The contents of any DCS word within the system is determined by the multiplex address associated with it as shown in Table 1.

Table 1

MPX vs. CONTENTS

MPX (OCTAL)	Contents	Format
000-177	Analog data	2-12 bit samples
200-277	Digital data	1-24 bit word
300-377	Digital command	1-24 bit command

The data set has two time sequential modes of operation which each produce one monitor word (MW) per WCC cycle. The first MW scans selected data points according to the contents of a 1702A EPROM, allowing selective scanning of data points and scanning rates. The second MW has two modes of scanning: 1) it can be selected to continuously monitor a single monitor point every cycle, or 2) it can be set to sequentially scan all of the 192 possible points, even though many of these points have no valid inputs. In mode 2, the data set requires about 10 seconds to complete a full scan. The array data processing is based on information obtained from monitor word #1 due to the point selection and the higher sampling rate.

The data taps (located in the B, C and D racks) are the human interface element in the DCS system. The antenna data taps are tied to the nearest data set's inputs and receive all antenna commands and echoed (gossip) monitor data, allowing the user to obtain a real time display of any data or parity errors incurred at the antenna. The CER data tap is tied to the central buffer's input and can receive any monitor data, command or parity error generated in the system.

III. DCS SYSTEM TEST BENCH (STB) THEORY AND USAGE

A. System Test Bench Construction

The DCS System Test Bench (STB) is physically constructed as shown in Figure 3 with the corresponding block diagram of Figure 4. It can be seen from these diagrams that the modular configuration of the STB is roughly identical to the layout of the DCS system for one working antenna: the central buffer, antenna buffer, data sets and data taps are interconnected in the same manner.

The Intel MDS-800 microprocessor is the STB controller and is capable of a real time display of monitor data as well as formatting

and outputting commands to the STB system. The Intel contains a special interface card for this purpose. From initial power-up, the MDS-800 contains only the standard Intel monitor, which allows machine language programming (refer to the Intel manual). The STB operation program is stored on a flexible magnetic disk (floppy disk) and is loaded into the Intel's RAM under the CP/M disk operating system.

1702A EPROMS, which are used in the data set (as well as many home projects), can be programmed using the Intel universal PROM programmer and the programming routines which are primitive functions contained in the Intel monitor. Additionally, 2704, 2708, 2716, 2758, 2732 and 8755 EPROMS may be programmed using the More Universal PROM Programmer (see Programming Errors chapter).

The CRT is used for a real time display of monitor data, and in conjunction with the keyboard, user entry of program parameters.

The MDS-800 computer is used as a single antenna simulation of the MODCOMP computer and its interfaces to the serial line controller simulator (SLCS) via a special interface card. Data transfers to the SLCS are accomplished by means of 8 bit parallel words. As stated earlier, the MDS-800 is 'stupid' on power-up and must have the test program loaded from the floppy disk.

The Intel contains 62K bytes of RAM, and 2K bytes of EPROM containing the Intel monitor program. There is an additional 2K bytes of bootstrap EPROM, which is present only at initial load time. The STB test program is loaded into RAM and is self-executing. This program uses many of the subroutines in the Intel monitor. A block diagram of the STB monitor program is shown in Figure 5 and a memory utilization map of the MDS-800 is shown in Figure 6.

The interrupt vectors are used for both manual interrupts and for program hardware interrupts. The STB monitor is basically controlled by the directive input processor. All directive inputs cause program jumps to subroutines which may or may not be self-returning. Non-returning jumps produce some type of real time display and wait for the user to supply a keyboard ('X') interrupt.

The SLCS interface card transfers commands from the CPU to the SLCS in 8 bit parallel words and accepts monitor data from the SLCS in the same format. The SLCS contains circuitry to reformat the byte formatted data into standard 45 bit serial words for transmission to

the central buffer. The SLCS also generates the QQ, track and hold and 5 MHz timing signals for the control room end of the STB. Q's are generated for unloading of monitor data from the central buffer (CB) to the SLCS. Upon receiving a monitor word from the CB, the SLCS checks parity over the entire word and outputs the MW to the MDS-800 for analysis and display.

Bin B of the STB contains a central buffer, a data tap (when available) and data set #5 (hard wired DSA), which is similar to the D rack except: 1) the DCS address of the central buffer and the data set is programmable by the DCS (antenna) address switches, and 2) the analog and digital data inputs and the command outputs of the data set are connected to the Binary/Analog Data Source.

The data set analog inputs for channels 0-6 consist of fixed voltages from a string of non-precision resistors, yielding readbacks as shown in Table 2. Analog channel 7's input is a staircase function of -1.0 v/MUX address and an offset of +8.000 v, giving the voltages shown in Table 2, to allow a distinction between the different addresses, as well as a rough approximation of conversion values.

Table 2

MPX vs. VOLTAGE INPUT

MUX Group	Even Address	Odd Address
000-017	1.000	-1.000
020-037	2.000	-2.000
040-057	3.000	-3.000
060-077	4.000	-4.000
100-117	5.000	-5.000
120-137	6.000	-6.000
140-157	7.000	-7.000

160	8.000	7.000	6.000	5.000	4.000	3.000	2.000	1.000
170	0.000	-1.000	-2.000	-3.000	-4.000	-5.000	-6.000	-7.000

The Binary/Analog Data Source (BADS) provides a means of forcing binary data to the local data set (#5), as well as providing the analog voltage inputs. The data set tester is tied to DS 5's SMA, command, clock and strobe lines, as well as the binary input data, clock and strobe lines.

The seven segment LEDs combined with the thumbwheel switches allow the user to enter and view the digital information loaded via the toggle switches. The MUX LEDs display the last address entered ('00-'77 with an implied offset of '200), and the data LEDs show the last binary data entered ('00000000 - '77777777). Note that the clear switches clear the data or address to the all ones state (MUX = '77, data = '77777777). The SEL/ANY switch allows the user to select a specific MUX address for programming, or to program all digital addresses upon their update. The data and address portions of the BADS are independent to allow alteration of one parameter without affecting the other, providing an easy method of aligning the data tap D/A converters and verifying the operation of the data set's binary input logic.

On the opposite end of the test bench, the data set port selector interfaces the data set with the antenna buffer, providing the capability of changing the hardwired DS address and the antenna buffer ports to which it is connected. The port selector also contains a simple minded circuit to read the DSA switch and create (or simulate) monitor data for all other antenna data sets except the hardwired data set. This allows checkout of the antenna buffers with a full compliment of monitor data. The binary data value of these monitor words is shown in Table 3.

Table 3
SIMULATED DATA SET OUTPUT
(Port Selector Module)

D.S.#	000	001	Pattern (HEX)
0	0.000v	0.000v	000000
1	6.825v	6.825v	555555
2	4.095v	4.095v	333333
3	9.555v	9.555v	777777

The antenna buffer is connected to the antenna data set's SMA lines for the antenna serial number readback on MUX '202, so MUX '202 for the real data set will always show the antenna serial number, regardless of the data set's actual I.D. (0-3). In the real system,

the AB is tied only to data set 2's SMA lines. The antenna serial number readback information is provided by the 2 antenna ID thumbwheel switches on the thumbwheel switch panel.

B. Program Loading

1. Turn power strip, MDS-800 key, DISC power on.
2. On MDS-800 turn boot switch on and hit reset. Press space bar on keyboard. MDS-800 responds with :

```
MDS MONITOR, V1.1
```

3. Turn boot switch off. MDS responds with:

```
[LF].           ;.=PROMPT
```

3a. Turn the CP/M boot switch on (up).

4. Insert floppy disk titled 'STB PROGRAMS' in the left disk drive, and type:

```
.AL=C[CR]       ;ASSIGN LIST DEVICE TO CRT
.G8000[CR]           ;EXEC DOS BOOTSTRAP SYSTEM
```

If the system loads properly, it will respond with:

```
>>>ENGRAM CP/M BIOS VERSION 1.2<<<
*DENSITY:  A,B-DOUBLE C,D-SINGLE*

A>
```

5. Be sure to turn the CP/M boot switch off at this point.

Type 'STB[CR]' and the DOS will load and execute the test bench program. You may remove the disk and turn the drives off once the program has printed the list of directives.

C. Command Directives for DCS System Test Bench Monitor III.0, 12 Feb., 1982

Directives:

C = Command processor
D = List directives
E = Exit to MDS monitor
F = Free data set
G = List global buffer
I = List command buffer
K = Kill global buffer
L = Kill parity buffer
M = Monitor word processor
P = Parity buffer display
R = Reset commands
S = Select MW 2 MUX
Z = Zero error counters

1. General Information

Each of the operating systems available on the MDS-800 places a different prompt symbol at the beginning of the input line.

CP/M (Disk system) uses A> or B> (depends on current drive)

INTEL monitor uses

STB monitor uses %

PROM programmer uses ?

Each system also has it's own error message.

CP/M has an assortment

INTEL uses '*'

STB uses '?'

PROM programmer says WHAT?

Address information (DSA, ANT) to the STB monitor is always entered and displayed in octal format. Data entry for commands can be entered either as hexadecimal or octal, but is always displayed as hexadecimal.

2. C - Command Processor

The command processor allows keyboard entry of commands for any valid antenna and data set address in either a repetitive (continuous) mode or in a single shot mode where the command is output once per entry. Up to 12 commands may be entered and output every cycle to the central buffer, which will store only the last 4 valid antenna and the last 6 local (#5) data set commands per cycle.

The format for a single shot command is:

```
CS,#HHHHHH,MMM,D,AA[CR]        #H=HEX DATA ENTRY

CS,'OOOOOOOO,MMM,D,AA[CR]      'O= OCTAL DATA ENTRY
```

upon [CR] command is output and returns to STB monitor.

To enter repetitive commands:

```
CR,#HHHHHH,MMM,D,AA,III [CR]

1CR,'OOOOOOOO,MMM,D,AA,III[CR]
↑
```

on [CR], monitor places command number here.

The III shown here is the interval at which commands are output; command is output every III+1th system cycle. Note that commands are output only while in the MW mode. For continuous commands, use an interval of 000.

Use of the I directive (see I-List command buffer) allows the user to perodically review and edit the contents of the command buffer.

The command processor also has the capability of altering the parity bits of one command at a time, allowing checkout of the parity error detection logic in a data set. Before using this routine, the command buffer must have a command entered.

```
CG,#,BBBBB,III[CR]        # = COMMAND NUMBER
                          B = BINARY MASK
                          1 = CHANGE PARITY (induce an error)
                          0 = LEAVE INTACT (correct parity this byte)
                          III = ERROR INTERVAL (for an error every
                               cycle, use 000 for interval)
```

To clear the command garbage processor, enter:

```
CG,1,00000,000[CR]
```

3. D - Directives

While in the STB monitor mode, typing 'D' produces the STB command directory and returns control to the STB monitor.

```
S T B  T E S T  P R O G R A M
VER III.0 ***E.L.T.*** 08 MAR 1982
     Directives:
C = Command processor
D = List directives
E = Exit to CP/M operating system
F = Free MW 2
G = List global buffer
I = List command buffer
K = Kill global buffer
L = Clear parity buffer
M = Monitor word processor
P = Parity buffer display
R = Reset commands
S = Select MW 2 MUX
Z = Zero error counters
%  (This is a prompt for user input)
```

4. E - Exit to MDS Monitor

While in the STB monitor mode, typing E[CR] transfers control to the CP/M operating system, which does a 'warm boot'. This means that the system reloads itself from disk. To exit, the disk drives must be turned on and the "STB Test Programs" disk installed in the left drive (drive 'A'). The 'E' command does not always work properly, due to some as yet unlocated bug in the code. If this occurs, reboot the system from scratch (see Program Loading).

5. F - Free MW 2

The free command allows the user to 'free' monitor word 2 for any given data set. This processor formats a command with a MUX of 301 to the specified antenna and data set. This command is output three times per entry to insure freeing the data set. Control is returned to the STB monitor.

F,DSA,ANT[CR] A space may be used for ,

6. G - List Global Buffer

The global buffer keeps track of which antennas and data sets respond while in the monitor word processor since this buffer was last cleared (see k-Kill Global Buffer). This provides an indication of a module's response address if an unknown address is read back. Control returns to the STB monitor.

G[CR]

RESPONSE:

ANT	DS	MUX
XX	X	XXX
XX	X	XXX

X = LAST VALUES RECEIVED

NOTE: The global buffer is updated only while the program is in the 'mw' monitor word display mode.

7. I - List Command Buffer

This displays the contents of the command buffer. Up to 12 commands will be displayed, depending on the number previously entered. The digital data portion of the command will be displayed as 6 hexadecimal digits regardless of the method of entry. All other parameters are shown in octal format. This routine returns to the STB monitor.

I[CR]

```
1 CR,#XXXXXX,MMM,D,AA,III
2                              X = HEX DIGIT
3                              M = MUX ADDRESS (300-377)
4                              D = DATA SET # (1-5)
5                              A = ANTENNA # (00-37)
6                              I = CMD INTERVAL (000-377)
7
8
9
A
B
C
```

8. K - Kill (Clear) Global Buffer

Typing K[CR] invokes a routine which clears the global buffer and returns control to the STB monitor. Executing G[CR] immediately will verify this by displaying an empty global buffer.

9. L - Clear Parity Buffer

Similar to the K command, L[CR] fills the parity error buffer with zeros and returns to the STB monitor. P[CR] will verify this operation.

10. M - Monitor Word Processor

The monitor word processor interprets the binary data received from the SLCS and displays MW 1 or 2 for the selected antenna and data set. Additionally, the processor records and displays in octal format the number of monitor and command parity errors when they occur. The command parity count is determined from the MUX 200 readback of the selected data set.

```
MW,1,ANT,DS[CR]          1 SPACE CAN BE USED IN
MW,2,ANT,DS[CR]            PLACE OF COMMAS
MW[CR]                   DISPLAYS LAST MW CALLED UP

(A000)   V V V V V V V V        MW = (1 or 2)
(A010)   V V V V V V V V        ANT = AA
(A020)   V V V V V V V V        DS = D
(A030)   V V V V V V V V
(A040)   V V V V V V V V
(A050)   V V V V V V V V
(A060)   V V V V V V V V
(A070)   V V V V V V V V
(A100)   V V V V V V V V
(A110)   V V V V V V V V
(A120)   V V V V V V V V
(A130)   V V V V V V V V
(A140)   V V V V V V V V
(A150)   V V V V V V V V
(A160)   V V V V V V V V
(A170)   V V V V V V V V
(D200)   H H H H H H H H        M = ###
(D210)   H H H H H H H H        C = ###
(D220)   H H H H H H H H
(D230)   H H H H H H H H
(D240)   H H H H H H H H
(D250)   H H H H H H H H
(D260)   H H H H H H H H
(D270)   H H H H H H H H
```

Where: V = Analog voltages (-10.240 to +10.235V)

H = 6 Hexidecimal digits (binary data)

M = Monitor parity error count

C = Command error count

This is a real time display and is constantly updating if data from this antenna and data set is received. If no data is received, the last monitor parity error count is displayed to kill time. During the display, the command output of the SLCS is enabled and commands are output to the central buffer.

To return to the STB monitor:

X[NO CR!!!]

11. P - Parity Buffer Display

The parity buffer holds the last 16 monitor parity error messages received while in the monitor processor (display) mode, and reproduces them in both a hex and a binary format to allow the user to locate the byte(s) in error. The parity display is a single screen full of information, and after displaying, returns to the input processor, awaiting another command from the user.

P[CR]

```
ANT DSA MUX   DATA     BYTE 0       BYTE 1       BYTE 2       BYTE 3       BYTE 4
-------------------------------------------------------------------------------
 00  0  000   000000   00000000 0   00000000 0   00000000 0   00000000 0   00000000 0
 01  1  123   FFFFFF   00001001 0   01010011 0   11111111 0   11111111 0   11111111 0
                                 ↑            ↑            ↑            ↑            ↑
                                 |            |            |            |            |
PARITY BITS ---------------------|------------|------------|------------|------------|
```

The last 16 error messages are displayed in the above format. If no errors have occurred, 16 words of zeros are displayed.

12. R - Reset Command(s)

The R command is used to remove either a selected command from the command buffer or to remove all commands from the buffer. Use of the R and the I commands allow selective editing of the command buffer.

R,X[CR]	RESETS CMD #X
R,E[CR]	RESETS ALL CMDS
	SPACE MAY BE USED IN PLACE OF COMMA

13. S - Select MW 2 MUX

This directive formats a command to the specified DCS and data set address (MUX = 300) to select the desired MUX for continuous scanning by monitor word 2. This command is the complement of the Free (F) command, both of which return to the STB monitor.

S,MMM,D,AA[CR]

MMM = MUX DESIRED

D = DATA SET

AA = ANTENNA SPACE = COMMA

14. V - View DCS Array Data

The view command allows examination of real time VLA-DCS system data. To use this directive, the SLC interface data tap must be plugged into the Control Room D.T. slot on the STB. The SLC/STB switch on the antenna address panel goes to SLC, and the D.T. antenna and data set switches should be selected to the desired DCS and data set numbers. The MUX should be set to ANY and the Parity/Normal switch goes to NORM. The command Data/Monitor Data switch on the data tap should be set to MON. DATA.

The V command format:

```
V MW DCS DS          TO SPECIFY ALL PARAMETERS
V                    TO RESUME VIEWING OF PREVIOUSLY CALLED MW

                     WHERE:  MW = 1 OR 2
                             DCS IS OCTAL 1-37
                             DS = 0-5
```

Upon [CR], the program will display the data as shown under M - Monitor Word Processor. To exit the display, type 'X' (same as the monitor word display).

To recall the last MW displayed, enter V[CR].

15. Z - Zero Error Counters

Both Monitor and Command (M,C) error counters are zeroed by the same command which is Z[CR]. Control is passed to the STB monitor and the counters will not display (while in MW Word Processor mode) until errors have occured.

16. No-No's For Program Operation

Never start a line with a backspace (Control H) while in the STB program command mode as this causes the CPU to re-boot CP/M. Once this happens it is necessary to reload the program.

Never leave a floppy disk in the disk drive while the power is being turned on or turned off, as this is absolutely guaranteed to crash the disk (write garbage onto it), making recovery impossible!!!

D. Programming UV Errors

1. 1702A UV EPROM Programming

The Intel universal PROM programmer coupled with the UV eraser provide the capability of changing the contents of the 1702A EPROMS used in the data sets for the MW 1 data point selection. The PROM programmer routines are part of the Intel monitor, requiring operation in the Intel monitor.

To erase EPROMs:

Place EPROMS on the foam pad in the eraser with the quartz window facing the UV bulb. Set the timer to maximum and turn the bulb on (red button). When the timer is done (30 minutes) the PROMS should contain all 00's. It is seldom necessary to erase a 1702A more than once, this being the first indication of a PROM going sour.

PROM programming:

The programming routines use RAM for an image of the programming data. To copy a PROM, the contents are read into RAM from the PROM directly and then programmed into a blank PROM. Instead of using a PROM for an image, the operator can specify all data into RAM prior to programming.

Socket one (1) on the programmer is used for all operations on 1702A PROMS. Socket 2 is reserved for a second personality card for other PROM families.

The programmer directives are:

TTYAAAA,BBBB	Transfer contents of PROM to RAM
TFYAAAA,BBBB	Complement and transfer contents of PROM to RAM
PTYAAAA,BBBB,000	Program using image at AAAA-BBBB
PFYAAAA,BBBB,000	Complement and program using image at AAA-BBBB
CTXAAAA,BBBB	Compare PROM contents and AAAA-BBBB
CFXAAAA,BBBB	Complement and compare PROM contents and AAAA-BBBB

If an error is incurred during programmer command entry, type 'RUBOUT' and the monitor will ignore the command and give an error indication.

Building an image or altering one:

To alter an image, first place the image in memory using the T command. The image can be examined by using the Dump command.

DAAAA,BBBB[CR]

Now go into RAM and change the address(es) desired:

SXXXX DD-12 WHERE XXXX = ADDRESS, DD = PRESENT CONTENTS AND 12 IS THE USER ENTRY.

By doing one space after DD- the address is incremented and the original data is unaltered:

SXXXX DD- EE-12

In the same manner, an entire image can be built from scratch. The S command can be entered once and data continuously entered until the first [CR]. If erroneous data is entered and recognized before the space, key in the correct data since the INTEL takes only the last 2 characters entered per location.

A hard copy may be obtained by assigning the list device to the printer (be sure to set up printer first) and doing a dump of RAM:

AL=L[CR]
DAAAA,BBBB[CR]
and reassigning the list when printing is done:
AL=C[CR]

It is suggested that PROM images in RAM be placed no lower than address 0100H.

Typical sequence for copying a PROM with a few mods:

1. Turn programmer on and hit reset on PROM programmer.
2. Plug source PROM into socket 1.
3. TTY3000,30FF ; transfer from data to RAM
4. D3000 30FF ; dump RAM (PROM) data to CRT

The data looks like this:

```
3000 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
3010 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
3020 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
3030 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
3040 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
3050 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
3060 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
3070 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX   XX=DATA
3080 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
3090 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
30A0 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
30B0 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
30C0 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
30D0 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
30E0 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
30F0 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX

.S3011 XX-3D XX-3E XX-3F XX-40
.S30A0 XX-3C XX-3D XX-3E XX-3F     (MAKE A FEW CHANGES HERE)
```

The image is now correct and ready for programming.

5. Place a blank PROM in Socket 1.

6. .PTY30000 30FF 00 Program entire PROM with data found here.

Programming takes about 1 minute. The programming light is lit while the programmer is active.

[CRLF]	Indicates PROM is programmed right
0XX*	Shows an error was encountered at location XX. Erase this PROM and do another one.
.CTX3000 30FF	Compare PROM contents with RAM image
.AL=L	Assign list to printer
.D3000 30FF	With printer on, get a hard copy
.AL=C	when printer done

2. Other EPROM Types

In addition to the Intel universal prom programmer, there is a custom build prom programmer available (I won't say who built it!) for programming and verifying several of the more common types of proms: i2704, i2708, i2758, i2716 (5 volt version ONLY), i2732 and the i8755. This programmer is known as the More Universal Prom Programmer (MUPP for short), and can be connected to the MUPP I/O port of either the Intel MDS-800 or the North Star computer. Since both computers run under the CP/M operating system, a common set of program/read code has been developed.

To use MUPP, first power the programmer up, then load the programmer program from the CP/M. This is done by typing 'PROMPGMR<CR>' at the CP/M prompt of A>. The code will then load and start execution. Since the code is very friendly, the actual operation is left as an exercise for the reader.

The only things to be aware of are:

1. Be sure to plug the prom into the appropriately labeled socket on MUPP. Plugging a prom in upside down is a sure method of destroying it. Be very careful.....
2. Since the program is responsible for initializing the hardware, DO NOT insert the prom until the program has asked for and been told the type of prom it is to work with. This is to avoid possibly programming a byte or two accidentally during insertion.

IV. STB OPERATION FOR MODULE CHECKOUT

A. Local Buffers

The items to be checked on local buffers are:

1. Local monitor data (DS #5)
2. Antenna monitor data MW 1,2 for DS#0-4
3. Antenna command output (4/WCC cycle)
4. Local commands output to DS #5 (4/WCC cycle)
5. All DCS addresses programmable

Requires these working modules:

1-Antenna buffer

2-Data sets

3-Simulated data sets (provided by PSL logic)

1-Data tap

Procedure:

1. Local monitor data

Set DCS address switches to 00 and the CB front panel should show the same numbers. Call up MW 1 for ANT. 0, DS #5. When the CB is working, MW 1 and 2 data will be displayed with no missing data or parity errors.

2. Antenna monitor data

Call up MW 1 for DCS shown on antenna buffer, DS #0. After much agonizing over the integrator (SH. 3 of the prints), all 10 monitor words from the antenna will be available at the terminal for display. This can be verified by calling each monitor word in turn.

3. Antenna command output

Manually load 4 commands to DCS 00, DS 0-3 and check out the command path. The processor must be in the monitor word display mode for commands to be output to the central buffer. All commands received by the antenna buffer will be visible on the antenna data tap.

4. Local commands output

Manually load 2 commands to the local data set (#5) and trace the logical command path. This is best done starting at the output of the command register shown on Sheet 5 of the blueprints.

5. Antenna address programmable

Manually load a command for data set 1, DCS address 0,1,2,3,4,5,6,7,10,20,37 and kill the global buffer. Call up a monitor word to output the commands. Slowly change the antenna address switches through: 1,2,3,4,5,6,7,10,20,37 and verify that the antenna buffer follows these addresses. On completion of this step, examine the global buffer to insure that a response was obtained from each of these antennas for DS #0-5.

B. Antenna Buffers

Items to check:

1. Monitor data readback (DS #0-3)
2. Command acceptance and storage
3. Data set 4 command count readback
4. Antenna serial number information
5. Forced data for missing data sets

Required:

1-Central buffer

2-Data sets

3-Simulated data sets (provided by PSL logic)

1-Data tap

1. Monitor Data Readback

Call up MW 1 for ANT. # shown on buffer, DS #3, and check out Q'ing and monitor data circuitry. When working correctly, MW 1 and 2 for DS #0-3 should be present with no holes (missed addresses) or parity errors. Note DS #4 may or may not work at this point.

2. Command Acceptance

Manually enter an antenna command for each of: DCS 0,1,2,3,4,5,6,7,10,20,37 data set 1 and call up a monitor word display. Run the antenna address switches through 1,2,3,4,5,6,7,10,20 and 37. The A.B. should follow these addresses and these commands will be visible on the antenna data tap. If not, select one address and check out the command path. When working, by clearing the global buffer and repeating this step, a listing of all responses may be obtained.

3. Data Set 4 Readback

Manually load 4 commands to the antenna selected and call up MW 1 for DS #4. MUX '205 only should respond. By killing one command at a time, the values shown below should be readback.

#CMDS/WCC	VALUE
0	000000
1	111111
2	222222
3	333333
4	444444

DS #4, MUX '205 READBACK

4. Antenna Serial # Information

Select the real antenna data set to data set 2, MUX '202 and display MW 2 for it. The antenna serial # switches should program this point to indicate the switch values in 3 redundant hex bytes.

Some typical values:

SER # (OCTAL)	VALUE (HEX)
00	000000
01	010101
10	080808
20	101010
30	181818
37	1F1F1F

ANT SERIAL NUMBER DATA

5. Forced Data For Missing Data Sets

To check this item, the antenna data set must be removed from the antenna bin of the STB. By setting the DSA on the PSL, the operator is given control over which data set is physically missing. The PSL logic will formulate monitor data for all non-selected data sets. The D.S. 4 logic in the antenna buffer will respond with the missing DSA and the correct command count at MUX '205.

C. Data Set Checkout

Items to check

1. All MUX addresses scan properly
2. All analog voltages convert correctly
3. All binary monitor points are programmable
4. DS internal commands work
5. DS external commands clocks and strobes work
6. Parity detection circuit detects
7. DS antenna address programmable
8. DS address (0-5) is programmable
9. DS exercised using data set tester module

Required:

1-Central buffer

1-Antenna buffer

1-Data tap

1. MUX Address Scanning

With the DS as the local DS (#5) set the antenna address to 00 and call up MW 2 0 5 with no A/D board installed. DS should scan from address 000-277 sequentially. If the DS is selected to 1 MUX, either

load a continuous free command (MUX 301) or momentarily short pin D14-4 to ground.

2. Analog Voltages Convert

After checking the A/D power wiring, using a bare A/D board, install a calibrated A/D and a test prom and compare the MW 2 displayed conversion values with Table 2. Scrambled input lines result in scrambled voltages and reversed pairs result in the wrong polarity.

3. Binary Monitor Points Are Programmable

The Binary/Analog data source is used to check the inputs to the data set. A typical sequence is:

Put SEL/ANY switch to SEL

Dial all 7's and enter as data

Dial '01 as starting MUX address and enter as address

Display MW 2 for DS #5 and after 1 full scan, address 201 should read FFFFFFF

Increment MUX address entered by 1 and repeat for values 201-207. Scrambling here is due to SMA 0-2.

Increment MUX address by 10 (octal) and repeat for MUX 207-277. Scrambling here is due to SMA 3-5.

Now put the MUX SEL/ANY switch to ANY. Binary data points 201-277 should read FFFFFF.

Select a binary address (not MPX 200) by loading a select command and display the MW 2 for DS #5.

Load this address into the B.A.D.S. and toggle each bit via the data switch and the thumbwheel switches. This indicates that the right number (24) of shift clocks get to the binary source.

This completes the use of the DS tester.

4. DS Internal Commands

This command group is MUX 300-317 inclusive and only one command of this group is valid per WCC cycle. Manually load one command only and check the command decoder-D8,SH 2 of the prints. The selected command selects one MUX address for MW 2 readback. Free puts DS in sequential mode and reset will reset the prom counter upon each occurance of the command. To check reset, load a command with a fairly long interval and MW 2 should scan I+1 monitor word points and reset to address 002 to start again.

5. DS External Commands

Three groups of external commands are available, 320-337, 340-357, 360-377. Load a command for 1 group at a time and check the data, clock and strobe outputs on the BADS front panel.

6. Parity Detector

The parity error detector can be exercised by loading a command and then a command garbage with an interval of 000. The output of MUX 200 is the parity error readback and will not be displayed when not FFFFFF. The output of these registers should be checked with a scope or on a data tap.

7. DS Antenna Adress

The global buffer can be cleared and used to keep track of antenna responses. Remove the antenna buffer, call up a MW and dial the ANT. address switches slowly through all possibilities. DS should respond with each address. The 'G' command will display all addresses the data set has responded with.

8. DSA Programmable

Replace the A.B, select the antenna buffer to ANT 00 and put the data set under test in the antenna DS slot. Dial each data set address and display MW 1 and 2 for each one to verify proper operation.

9. Data Set Tester

The data set tester module checks many items not possible through manual testing. Refer to the data set tester manual for information about its care and feeding.

D. M10 CMD/MON Interface Checkout

Requires:

1-Central buffer

1-Antenna buffer

1-Data set (in ANT DS location, DS ID = 2)

The M10 module has the following capabilities:

24 analog channels

1-12 bit command channel with echo

1-12 bit binary monitor channel

The first section of logic to check consists of the analog multiplexers. There are 24 different analog voltages applied to the M10, as listed in the chart below. This information is also present on the logic diagrams for quick reference. Use MW 2 display (in 'free' mode) to examine readbacks.

MUX	0	1	2	3	4	5	6	7
000	7v	6v	5v	4v	3v	2v	1v	0v
010	-7v	-6v	-5v	-4v	-3v	-2v	-1v	0v
020	0v	1v	2v	3v	4v	5v	6v	7v

NOTE: Values approximate due to low precision divider chain.

The M10 will accept only the top 12 bits of a command and echo the 12 bit command left justified in a 24 bit monitor word. Refer to sheet 2 of the logic diagrams for programming jumper locations, and to sheet 4 for MUX addresses as applicable on the test bench.

Like the command/echo, the binary monitor word packs 12 bits of real data into a 24 bit monitor word. Here again refer to the logic diagrams for programming jumper locations and MUX addresses. NOTE: The command/echo and the binary monitor MUX addresses MUST be different. Checkout is accomplished via application of logic 1's and 0's to the binary monitor shift register inputs.

Prior to installation in the system, M10 must have its MUX addresses programmed to suit the environment in which it is installed. As this is usually a bone of contention between hardware and software types, be prepared to make changes.

E. L23 MLO Switch Monitor Interface Checkout

Requires:

1-Central buffer

1-Antenna buffer

1-Data set (Antenna DS slot, DS ID = 2)

The L23's capabilities consist of:

8 analog channels

1-6 bit command with echo

2-24 bit binary monitor channels

As the test bench is currently wired, the L23's analog readbacks are on MUX 000-007, with the following values:

MUX	000	001	002	003	004	005	006	007
VALUE	7v	6v	5v	4v	3v	2v	1v	0v

The L23s MUX addresses are hardwired, unlike the M10 which is programmable. The command address is '333 and the corresponding command echo MUX is '233. Only the 6 most significant bits of the command are accepted and echoed by L23. This can be cause for confusion during debugging. The readback has the 6 command bits packed into a byte left justified, and repeated 3 times to make up a standard 24 bit monitor message.

Example: Command sent = 0101 0101 0000 0000 0000 0000
readback = 0101 0100 0101 0100 0101 0100
↑↑ ↑↑ ↑↑
hardwired 0's

The L23 has 48 digital input lines, and these 48 bits are packed into two 24 bit digital monitor words with MUX addresses of '231 and '232 (on the test bench). With no inputs applied, these words are readback as 000000H. The only feasable method of checkout here is to apply logic 0 (ground) at the bit input pins on the back panel or at the 7404 inverter inputs within the module.

V. PROCEDURE FOR RACK CHECKOUT

A. 'A' Rack Checkout

Requies:

1-Central buffer
1-Antenna buffer
1-A rack cable
1-Data set with D.S.1 prom installed
1-Port selector set to D.S.1

The A rack cable should be installed from the antenna data set position in the STB. The buffers should be set to antenna 00 (via the switches and STB commands). Set the data set ID to 1 on the port selector module.

With these conditions met, it should be possible to display monitor data and command the F5 from the STB console, given that the rack is wired correctly. Faults which have been found in earlier racks include:

1. 5 MHz and 19.2 Hz reversed.
2. 5 MHz and return reversed on data set, or 100 OHM terminating resistor missing altogether.
3. Command, strobe and clock lines scrambled and/or grounded at either data set or F5.
4. Analog channels reversed.
5. F.E. personnel don't know everything about the analog or digital readbacks. A (hopefully current) list of this data can be found in the FE test file or consult Bob Schweigert.

Things to check:

The analog and digital readbacks are concerned mainly with the state of the F5. By putting the F5 to manual, the readbacks can be exercised manually.

The FE personnel will ask for various commands to be entered on both single shot and repetitive modes to check the F3 and the F5.

VI. A/D ALIGNMENT PROCEDURES

A. Burr Brown A/D (Rev D) Alignment
Analog Devices (Rev E) Alignment

1. Using the H.P. high precision DVM, adjust the balance resistor for 240.000 ohms. For the Rev D board, these points are TP 3 and pin 17 of the converter socket. Refer to the logic diagrams for the Rev E boards. This adjustment is critical and requires as much precision as is possible.

2. Install the A/D converter (and multiplexer module on Rev E) on the board and plug the board (with the power off!!!) into the A/D test unit. Set the tester switches as follows:

CMP/LC	LC
SCAN/SEL	SEL
MANUAL/OFF	OFF
BUS A +/-	+
BUS SOURCE	EXT
BUS 0-50	0
BUS DIFF/CM	DIFF
BUS B +/-	+
BUS SOURCE	GND
BUS 0-50	0
BUS DIFF/CM	DIFF

3. Apply a 0.0000v input from the fluke reference to the tester external 'A' input and set the zero adjust on the ADC for a panel reading of 0.000v.

4. Increase the input to 10.000v and adjust the gain pot on the ADC for a reading of 10.000v.

Repeat steps 3 and 4 until no further adjustment is needed.

5. Vary the input from -10.000v to +10.000v in 1v increments and record the converted values on the A/D calibration data sheet.

If the ADC is highly nonlinear, repeat steps 3 and 4 using +9, 0 and -9v for alignment.

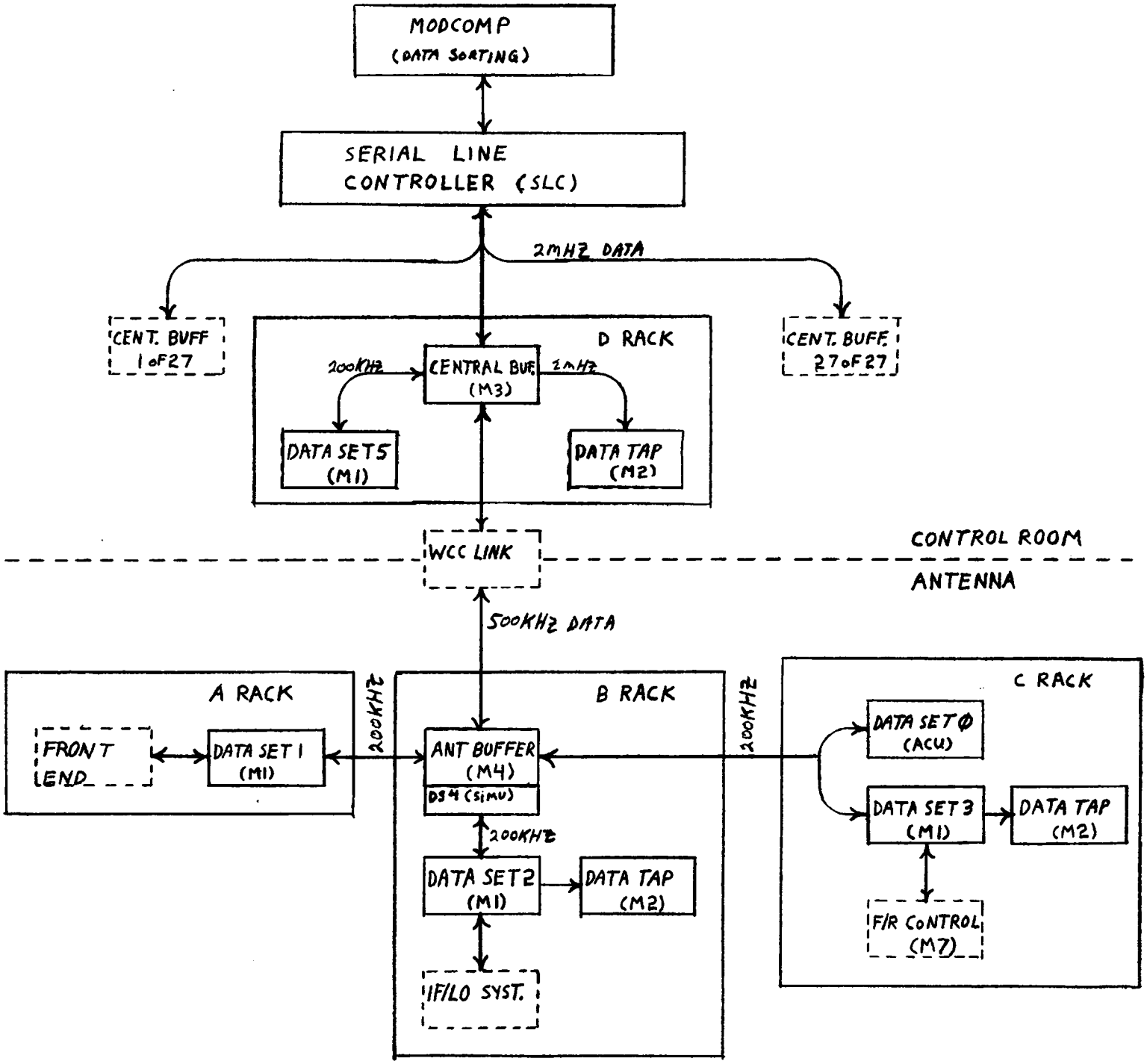

FIG. 1 DCS SYSTEM BLOCK DIAGRAM

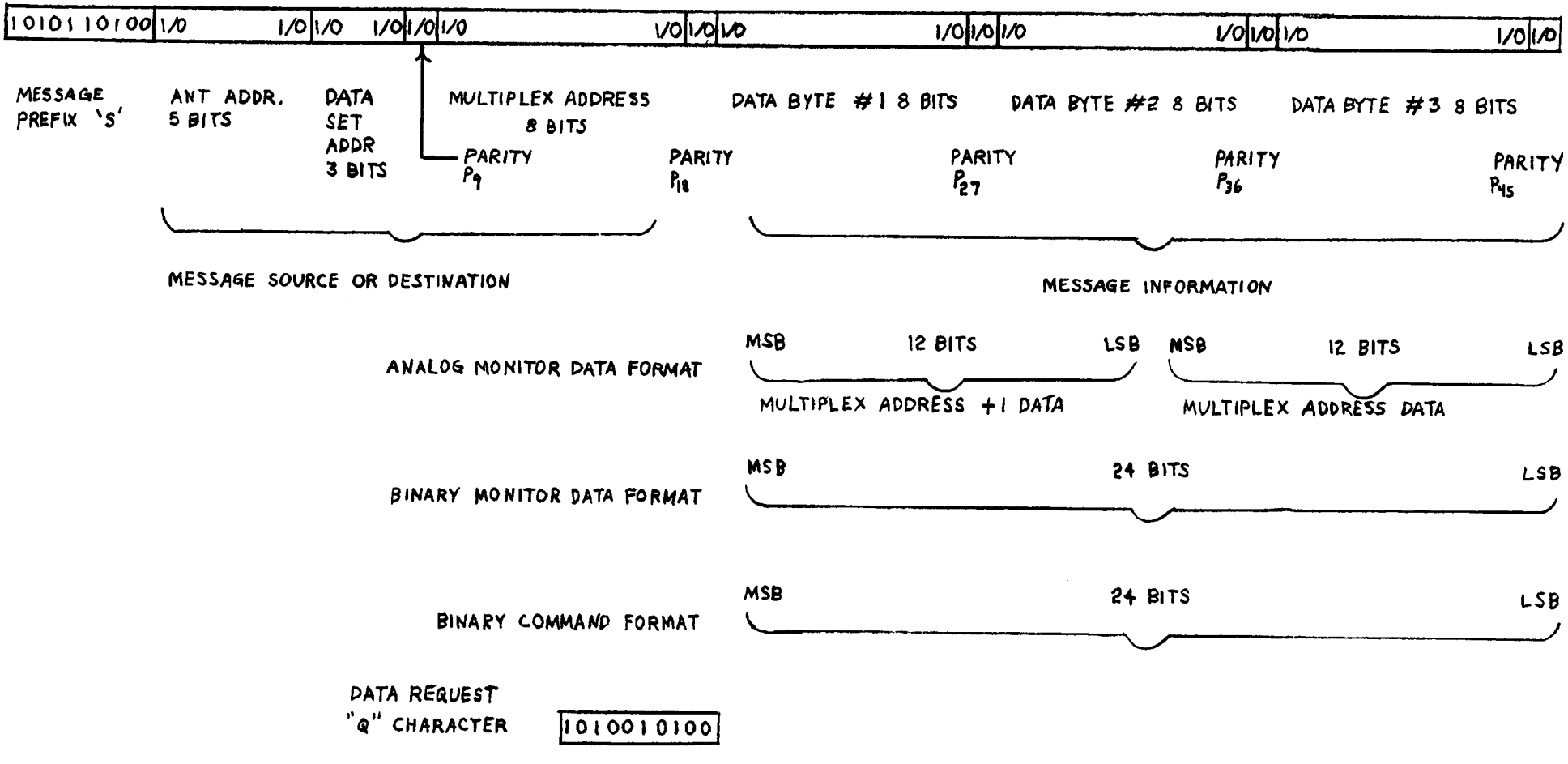

FIG 2* COMMAND AND DATA FORMAT

* this Fig. TAKEN FROM REPORT 30

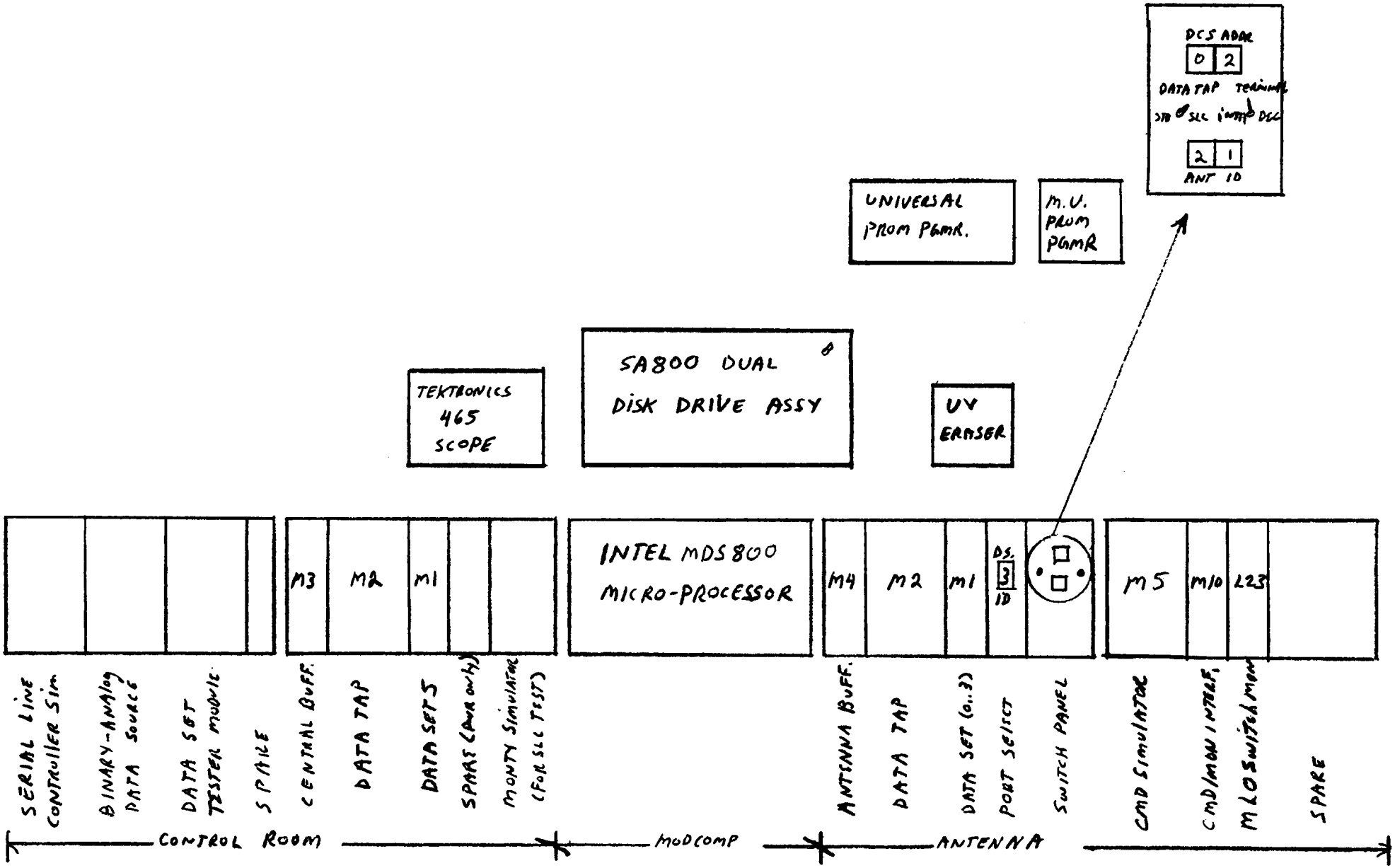

FIGURE 3 STB PHYSICAL LAYOUT

2/82 EJT

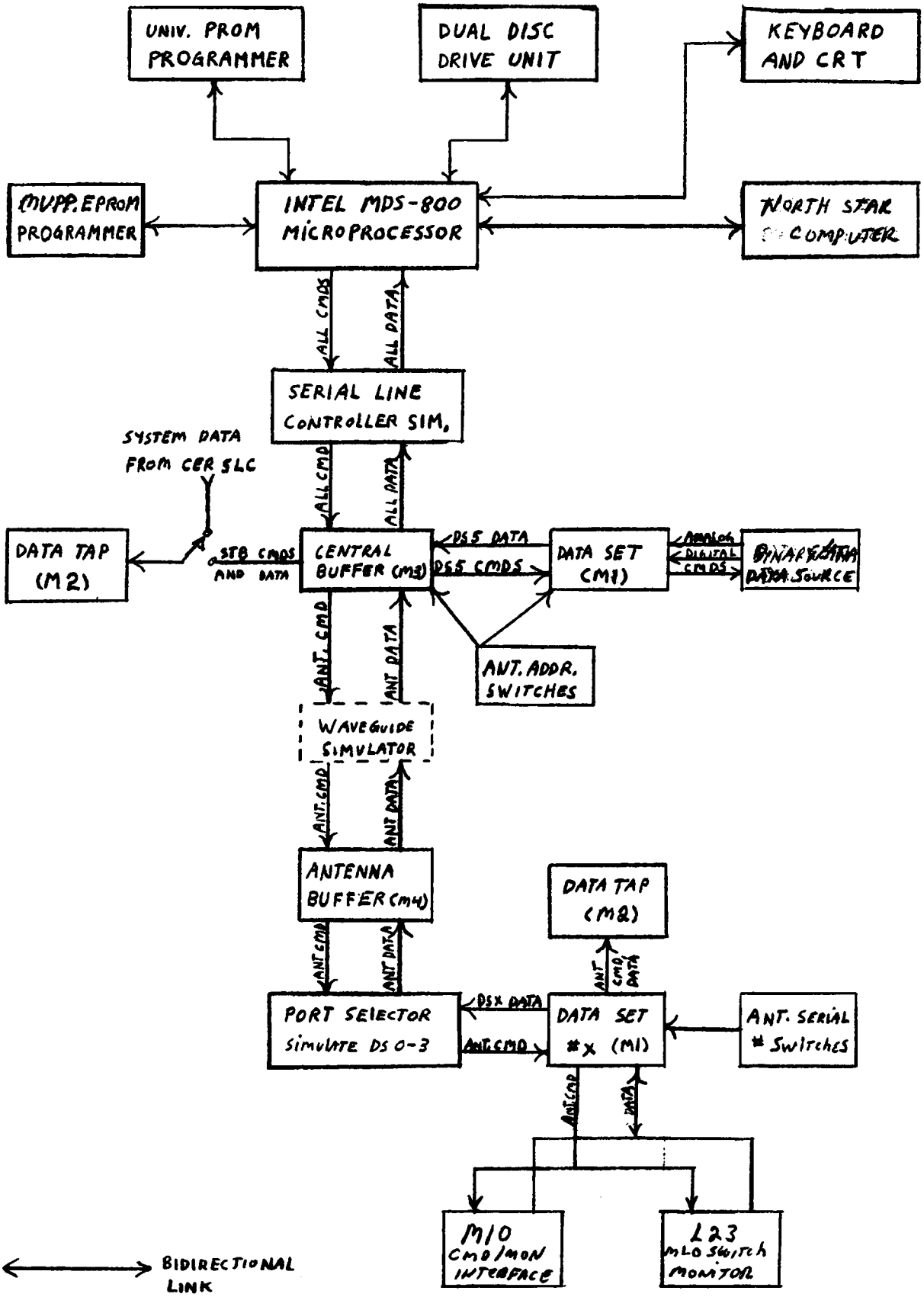

FIG. 4 STB BLOCK DIAGRAM

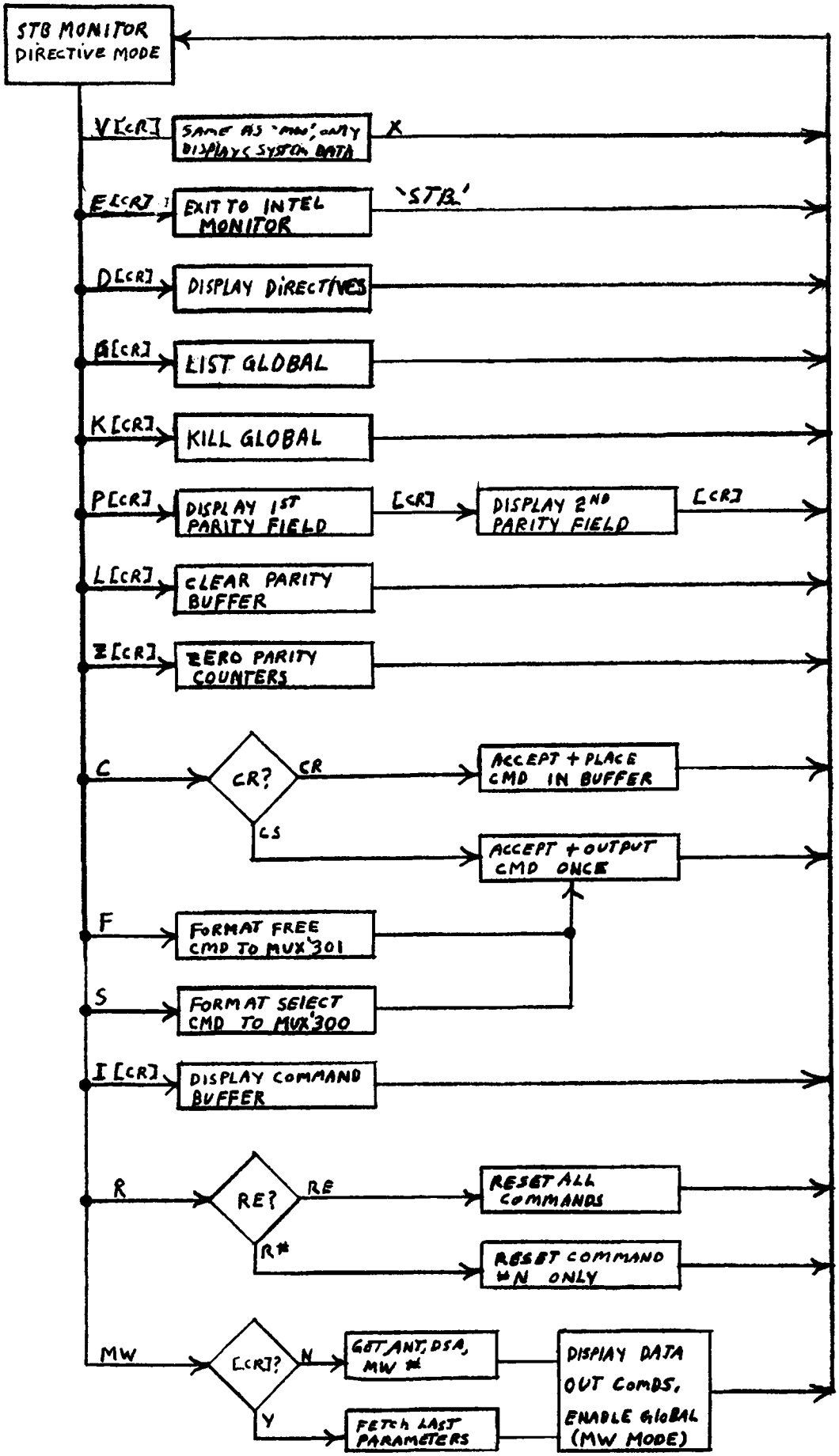

FIG 5 STB PROGRAM FLOWCHART

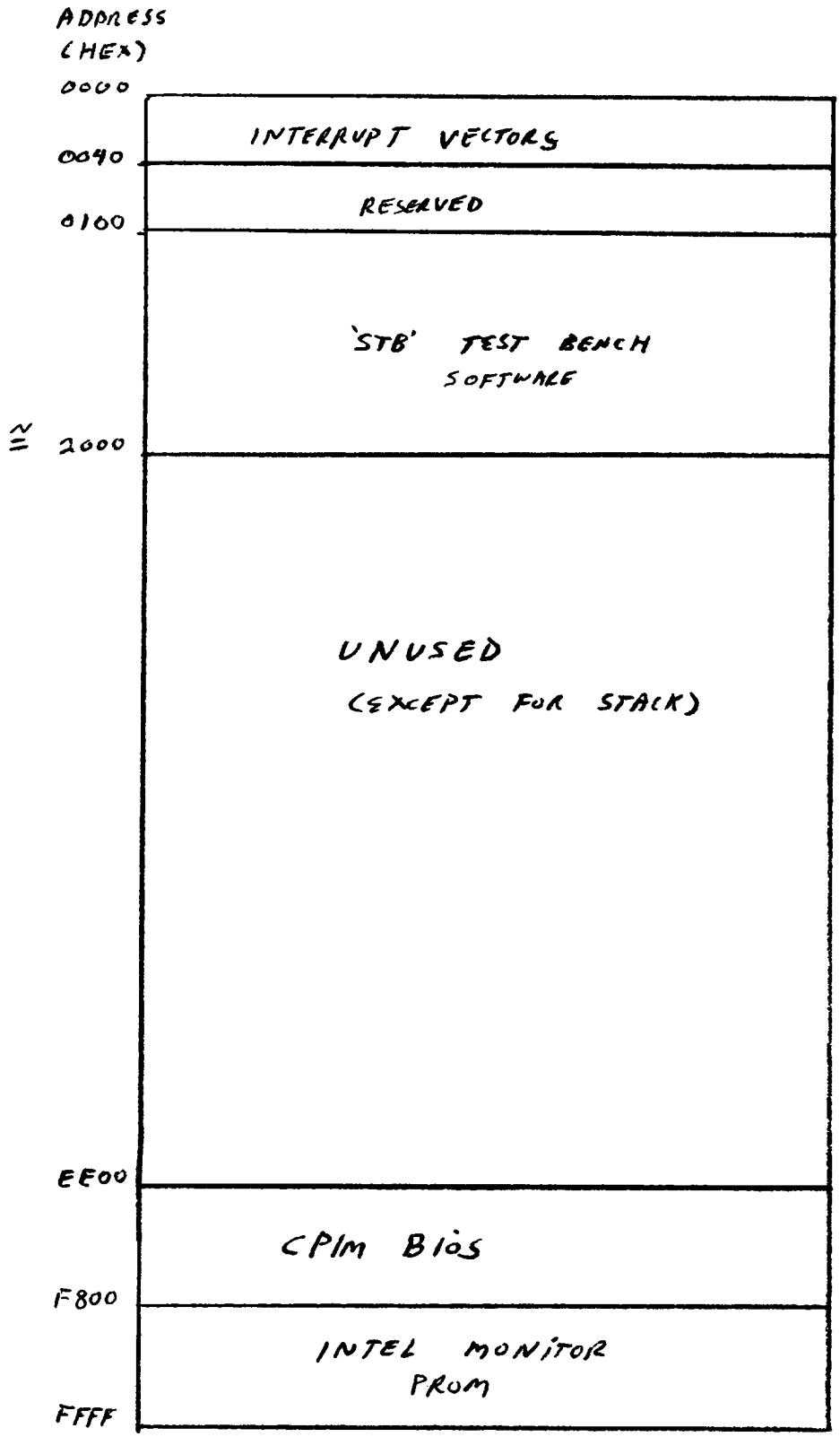

FIG. 6 MDS 800 STB TEST PROGRAM MEMORY MAP

AND REASSIGNING THE LIST WHEN PRINTING IS DONE:

AL=C[CR]

IT IS SUGGUESTED THAT PROM IMAGES IN RAM BE PLACED NO LOWER THAN ADDDRESS 0100H.

TYPICAL SEQUENCE FOR COPYING A PROM WITH A FEW MODS.

1. TURN PROGRAMMER ON AND HIT RESET ON PROM PROGRAMMER.
2. PLUG SOURCE PROM INTO SOCKET 1.
3. TTY3000,30FF ;TRANSFER PROM DATA TO RAM
4. D3000 30FF ;DUMP RAM (PROM) DATA TO CRT

THE DATA LOOKS LIKE THIS:

```
3000 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
3010 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
3020 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
3030 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
3040 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
3050 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
3060 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
3070 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX   XX=DATA
3080 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
3090 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
30A0 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
30B0 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
30C0 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
30D0 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
30E0 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX
30F0 XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX XX

.S3011 XX-3D XX-3E XX-3F XX-40
.S30A0 XX-3C XX-3D XX-3E XX-3F    (MAKE A FEW CHANGES HERE)
```

THE IMAGE IS NOW CORRECT AND READY FOR PROGRAMMING.

4. PLACE A BLANK PROM IN SOCKET 1
5. .PTY3000 30FF 00 PROGRAM ENTIRE PROM WITH DATA FOUND HERE

PROGRAMMING TAKES ABOUT 1 MINUTE. THE PROGRAMMING LIGHT IS LIT WHILE THE PROGRAMMER IS ACTIVE.

[CRLF].	INDICATES PROM IS PROGRAMMED RIGHT
0XX*	SHOWS AN ERROR WAS ENCOUNTERED. ERASE THIS PROM AND DO ANOTHER ONE.
.CTX3000 30FF	COMPARE PROM CONTENTS WITH RAM IMAGE
.AL=L	ASSIGN LIST TO PRINTER
.D3000 30FF	WITH PRINTER ON, GET A HARD COPY
.AL=C	WHEN PRINTER DONE

2. OTHER EPROM TYPES

In addition to the Intel universal prom programmer, there is a custom built prom programmer available (I won't say who built it!) for programming and verifying several of the more common types of proms: i2704, i2708, i2758, i2716 (5 volt version ONLY), i2732 and the i8755. This programmer is known as the More Universal Prom Programmer (MUPP for short), and can be connected to the MUPP I/O port of either the Intel MDS-800 or the North Star computer. Since both computers run under the CP/M operating system, a common set of program/read code has been developed.