VLA TECHNICAL REPORT NO. 54

VLA CORRELATOR SOFTWARE MANUAL EXCERPT

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1.0 INTRODUCTION

This manual will briefly describe the software written to support the system controller in performing continuum and spectral line observations with the VLA correlator system.

The system controller is a 16-bit microprogrammable microprocessor with an instruction set of about 75 computer like commands. The system controller is provided with observational parameters by the Modcomp computer, SPECTRE.

The system controller software can operate in three modes;

1) idle mode,
2) setup mode, and
3) observing mode.

In idle mode the system controller has only limited duties. It performs various front panel display functions such as providing drive to the 27 x 27 and 4 x 5 LED front panel arrays, supporting the front panel step and clear switch functions, and checks the various front panel error files for data to be flagged by red LED's in the 4 x 5 array. The system controller also responds to any commands from either SPECTRE or the local CRT during idle mode. Idle mode is entered via three conditions;

1) upon exit from an initial program load,
2) upon a station reset, and,
3) via an END observation command.

Setup mode is entered in response to a SETUP mode command and can be entered from either the idle or observing modes. Upon entering setup mode the system controller will clear out, from its memory, any trace of old observing parameters in expectation of receiving a complete set of new parameters. Once this clear-out is complete the software will revert to performing only those duties it normally performs in idle mode.

Observing mode is entered in response to a START mode command. This command tells the system controller that all pertinent modes have been received and that it may now configure the equipment so as to support the desired observation. Having configured the system properly, the system controller then starts performing all tasks necessary to support the observation.

The sequence of events to start an observation is thus to;

1) either load the system controller software initially and issue a SETUP command, or, if the system controller is already loaded, simply issue the SETUP command (whether the system is observing or in idle mode);
2) issue all required mode commands such as:
   a) antenna mode, i.e., continuum, single band spectral line, two-band spectral line, etc., on an antenna basis;
   b) integrator modes;
   c) recirculation parameters if any antennas are to observe in spectral line;
   d) a full set of delay line delays if the very first dump of correlation products is expected to be valid; and
3) issue START mode command.

At the end of the observation an END observation mode command will allow the system controller to put all delay lines in their low-power state to conserve about 5 kW of power. This END mode command is not necessary, its only function being in saving energy and in lowering the equipment operating temperature.

Note that the term "observation" as used above is not an observation in the astronomical sense, i.e., a single stay time on a single source, but the period the VLA does observing with a given set of correlator parameters.

The system controller observing program has been given the drawing number A13800F2. Software written for the Intel 8035 CRT processor has been given the drawing number A13800F3.

It is assumed that readers of this manual have some knowledge of the VLA correlator system hardware: this hardware is described in detail in VLA Technical Report No. 45.

The software described in this manual is Revision F of the delay/multiplier observing program. The software revision letter is stored in memory location 0007 which can be inspected by using the F3-R CRT function.

2.0 MACROFLOW DIAGRAM

Drawing C13800B9 (Figure 2-1) is a macroflow diagram of the VLA correlator observing program. As stated in the introduction, the system controller has few duties in idle mode and most of the duties illustrated in C13800B9 are performed only when observing. These duties may be divided into two categories, those duties performed during the approximately 50-msec data valid portion of the waveguide cycle and those performed during the approximately 1.5-msec data invalid period. In addition, the data valid tasks may be subdivided into tasks performed in the main routine and to tasks performed in response to interrupts. Below is a summary of the recurrent tasks performed by the system controller during observing mode;

1) Data valid, main routine
   a) enable interrupts;
   b) read error card data, if required;
   c) read error card self-test results, if required;
   d) check self-test results against predicted values, if c) above performed;
   e) clear error files, if front panel clear switch is depressed;
   f) step the 4 x 5 LED array pointer (green) LED, if front panel step switch is depressed;
   g) service the sampler monitor panel, if able;
   h) check the system power status;
   i) loop waiting for the start of a new waveguide cycle and then return to a) above.
2) Data valid interrupt subroutines
   a) blanking time interrupt;
      i) support interface software requirements (see Appendix III of the VLA Technical Report No. 45 for interface maintenance requirements);
      ii) support drive to both the 27 x 27 and 4 x 5 front panel LED arrays;
      iii) support integrator memory-to-storage memory dump;
      iv) support 19.2-Hz cycle counter;

v) support spectral line recirculator lag generation requirements;

vi) support storing of 92.16-μsec 12-bit results if required;

b) support Modcomp interrupts;

i) receive delay values;

ii) receive mark dump time commands;

iii) provide V_s values;

iv) provide information on detected errors;

v) respond to miscellaneous commands/requests;

c) support miscellaneous CRT commands/requests.

3) Data invalid tasks

a) disable interfaces;

b) do integrator self-test;

c) initialize software for next waveguide cycle;

d) get V_s and 50-msec sin x cos results from last waveguide cycle;

e) service exchange requirements;

i) service input MUX, if required;

ii) service output MUX and institute exchange, if required;

f) provide delay values to test delay lines;

g) support interchange delay routine, if necessary;

h) run self-test 92.16-μsec integration;

i) restore system to observing configuration;

j) load delays;

k) enable continuum interfaces.

In the pages that follow the descriptions of the major items of drawing C13800B9 will be presented. These descriptions will follow both the C13800B9 drawing and the program coding sheets and will be given only in gross detail.

2.1 Main Routine

Execution of the main routine begins upon either the initial program load, or a station reset, at memory location (LOC) 0000. The first task performed, between LOC 0010 and 001A, is to load interrupt vector locations into the interrupt registers.

LOC 001B branches to the routine that cleans out errors in the error files. This routine will be described in more detail later.

LOC 001E branches to the routine that ends an observation. The only reason to go to this routine is that it will shift-out delay words to all delay lines that result in their going to the low-power state. This routine will also be described later.

LOC 0020 is the start of the main routine waveguide cycle loop. This loop extends from LOC 0020 to LOC 006B and is run once per 19.2-Hz waveguide cycle. This loop is executed for the most part with interrupts enabled and consists entirely of nonessential, although useful, tasks. All essential software tasks, i.e., tasks absolutely necessary for supporting the observation, are performed in interrupt routines with interrupts disabled. The main routine tasks consist of self-test results analysis, self-heal considerations, supporting the front panel error display, servicing the sampler monitor panel, and other useful and desirable but still nonessential functions.

2.1.1 Reading 12-Bit Integration Results Stored on One of The Error Cards

The routine at LOC 17C8 will shift-in, via the serial I/O card, a 27 x 27 block of 12-bit 92.16-μsec integration results that were stored, in real time, in one of the four error cards (see logic diagram D13800L21 and Section 4.7.1.3 of Technical Report No. 45). The routine at LOC 17C8 can be entered from either LOC 002B or LOC 0032, since the storage of 12-bit results on the error card can result from either:

1) self-test; if self-test is enabled, a test 92.16-μsec integration is run during data invalid and a 27 x 27 block of the results of this integration is stored on an error card. Entry into the LOC 17C8 routine to read these results is made from LOC 0032.

2) observational storage; the 12-bit 92.16-μsec results may be stored for inspection if desired, in trouble-shooting for example, by i) disabling self-test, ii) storing the quadrant, array and blanking time to be inspected in LOC 1D01, 1D02 and 1D03 respective, and iii) reading the results via the local CRT F3-W, X, Y, or Z options (see Section 7.5.2 and Figure 29 of TR 45). Entry into the LOC 17C8 routine is made from LOC 002B.

Both of these potential tasks are bypassed in idle mode via the conditional branch at LOC 0021.

2.1.2 Check Self-Test Results

If the system is in observing mode and if self-test is enabled, the branch at LOC 003B will cause execution of the main self-test subroutine beginning at LOC 1500. This subroutine will test the 27 x 27 array of results, shifted in as described in Section 2.1.1, against predicted, will report discrepancies to SPECTRE and insert them into the front panel error files, and analyze the pattern of failures to see if a problem exists that can be healed by exchanging a test delay/recirculator path for a dedicated delay/recirculator path.

2.1.3 Service Front Panel Functions

Three front panel related subroutines may be executed following self-test.

1) LOC 003D, clear front panel error files if front panel clear switch is depressed. Execution of this subroutine begins at LOC 186A.

2) LOC 003F, error search. This subroutine, beginning at LOC 1886, will search the 20 error storage files for any error indications (any logic one bit in any of the 54 16-bit words that comprise each file). Any of the 20 files that contain errors are marked by illuminating corresponding red LED's in the 4 x 5 LED front panel array.

3) LOC 0045, step front panel pointer LED if front panel step switch is depressed (pointer LED is the single green LED in the 4 x 5 LED front panel array). This subroutine has a 5 waveguide cycle software delay so if the step switch is pressed and left pressed the pointer LED will shift right at about a 4 place per second rate (if the switch is pressed for longer than about 8 seconds, lamp test is entered and all LED's come on).

2.1.4 Service Sampler Monitor Panel

The sampler monitor panel is the rack panel located just above the channel A samplers. Sampler parameters, such as digital output duty cycle or sin x cos product, can be requested via front panel switches with the parameters displayed on an analog meter on the panel. The software that senses the switch positions and delivers the requested parameter starts at LOC 0A48 and is entered via the branch at LOC 004D. The branch is conditional and the 0A48 subroutine is performed in observing mode only.

2.1.5 Power Monitor Subroutine

Conditional branches at 0053 (for quadrants 1 and 2) and 0055 (for quadrants 3 and 4) test discrete signals that tell if power is up in the various portions of the system. The system can, via its self-monitoring, recognize a potentionally damaging condition, such as a power supply overvoltage or a high rack temperature, and power down threatened portions of the system. This software subroutine monitors the power status of the system and notifies SPECTRE, via branch at LOC 005E, and sounds an alarm, via branch at LOC 0062, which notifies the 8035 Intel CRT processor which rings the CRT bell. The software delay at LOC 0050 results in a distinctive once- per-second CRT bell sounding if a portion of the system powers itself down.

2.1.6 Loop Waiting for the Start of a New Waveguide Cycle

After all of the tasks above have been finished the software loop 0067 thru 006C allows the system controller to idle away the remaining portion of the current waveguide cycle awaiting the start of a new one.

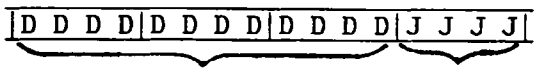
2.2 Blanking Time Interrupts

The main routine of Section 2.1 is run, except for minor exceptions such as when the serial I/O card must be used, with interrupts enabled. The most important interrupt, from a station maintenance standpoint, is generated by the 92.8-μsec blanking time divider. This divider controls the basic correlation cycle of the system, establishing the 92.16-μsec correlate data — 0.64 μsec put results into storage times.

The software BT interrupt subroutine begins at LOC 0600. The tasks performed in this subroutine can be divided into two categories; tasks that must be performed every BT, and tasks performed only in specific BT(s).

2.2.1 BT Job Assignment

The command at LOC 0602 reads the BT counter to see where in the waveguide cycle execution is currently progressing. The command at LOC 0603 uses the lookup table in the mapping ROM to find out what tasks must be performed in the current BT. This command uses the current BT number (in register R0) to address the mapping ROM, with the resulting lookup entry going into register R4. The job assignment word has the format;



Data related to specific job assignment.

Specifies one of 16 job assignments.

The four-bit JJJJ field is used as an index in LOC 0613 to the lookup table in LOC 0630 thru 063F (0640 thru 064F in idle mode). This table provides a single task to be performed during a current BT interrupt. Below is a summary of job assignments.

1) LOC 0630

   For BT's in which no specific job is assigned (most of them), LOC 0630 is the address of a NO-OP.

2) LOC 0631 thru 0635

These 5 job assignments direct the software to perform the various tasks associated with the interface between the multipliers and the integrator.

3) LOC 0636 thru 0638

Three job assignments are associated with the processor front panel. This front panel has a large 27 x 27 LED array which is time-multiplex driven. Approximately once each 5 BT's a 27-bit word to drive a single column of LED is provided via the serial I/O card. Thus to drive all 27 columns takes 27(5) or 135 BT's which is about $\frac{1}{4}$ of the data valid waveguide cycle. Hence in a single 19.2 Hz waveguide cycle the complete display can be driven 4 times for a 80-Hz flicker rate.

The small 4 x 5 LED array is time-multiplexed between the green and red LED functions. By time-multiplexing these diodes, a simultaneous red and green on condition can appear to exist on an LED if appropriate.

4) LOC 0639

The integrator memory-to-storage memory dump is accomplished with specific BT timing by the software via this job assignment.

5) LOC 063A

See Section 2.3.

6) LOC 063B

A software waveguide cycle counter is maintained via this BT job assignment. This counter gives the number of waveguide cycles counted since the start observation command.

2.2.2 Lag Maintenance

One BT task must be performed every BT and hence is not done on a job assignment basis. The routine between LOC 0607 and 0611 will shift-out a new lag program word to the recirculator control cards. As described in the hardware manual, the lag to each recirculator quadrant must change by the respective lag step

(four changes necessary) each BT (until the lag returns to zero after going to the max lag). The actual lag program words sent were composed the previous BT in the subroutine at LOC 0700 (entered from command at LOC 0626).

2.2.3 Record Array

As mentioned in Section 2.1.1, item 2, the 92.16-μsec 12-bit results from the multipliers can be stored in RAM's on the error card for display and inspection via the CRT. This function is accomplished by first stopping self-test, and then storing the BT number of the results to be stored in LOC 1D03. The BT interrupt routine at LOC 0616 will check to see if the BT to be stored is the same as the one currently being serviced and if so will go to the subroutine at 1D0C to effect storage. If no such action is desired, LOC 1D03 will have a number larger than any possible BT (like 7000 hex)stored in it so comparison will not take place.

2.2.4 BT Error Check

Two checks of valid operation is performed in the BT interrupt routine;

1) BT skipped

   The software checks, in LOC 0623, to see if the BT currently being serviced is exactly one more than that serviced on the last BT interrupt. If, say, BT 013B had been last serviced and BT 013D is presently being serviced, BT 013C must have been skipped, i.e., the interrupt generated when the BT counter incremented to 013C was not answered (due to a malfunction or to a long task being performed in response, say, to a Modcomp interrupt) and the lags and BT task assigned to that BT were not supported. This error, if detected, is reported to SPECTRE and the Intel CRT processor.

2) BT exceeded

   In response to a BT interrupt, the system controller begins serving that interrupt at LOC 0600. The system controller reads the BT counter and when the software supporting that specific BT has been completed the BT counter is again read, in LOC 0620, and the two BT

numbers compared to see if they are the same. If this comparison fails, it means that at least some of the tasks to have been performed in support of the interrupting BT 0135, say, may not have been completed until BT 0136 had started. Hence the 0135 BT was incorrectly serviced and correlator results may have been affected. An error of this type, if detected, is reported to SPECTRE and the CRT processor.

2.3 Data Invalid

One of the BT job assignments in Section 2.2 flagged BT number 544 as the last BT in the current data valid cycle. The job assigned to BT 544 begins execution at LOC 1000 and will result in execution of many small tasks. Below is a summary of these tasks.

2.3.1 Interface Disable

The command at LOC 1001 will result in execution of the subroutine at LOC 0663 which will disable all interface lines.

2.3.2 Memory Self-Test

The memory self-test subroutine at LOC 1060 is entered via the command at LOC 1003. This subroutine will support the memory self-test as described in VLA Electronics Memorandum No. 182.

2.3.3 Delay/Multiplier Self-Test

Portions of the delay/multiplier self-test software are distributed throughout the data invalid subroutine. Below is a summary of the various tasks performed by, or called from, this software.

1) Load test N and test lag (located at LOC 1146, called from LOC 1028).

   This software loads a test value of the sample factor (N = 2 for self-test) and one of the four lags used in self-test.

2) Load test delays (located at LOC 1100, called from LOC 102C).

   This software loads all delay lines with one of the four delays used in self-test.

3) Load test BT delay (located at LOC 09B3, called from LOC 103A).

See hardware manual Section 4.7.1.2.

4) Run test (LOC 1670, called from LOC 1043).

This software causes the actual self-test integration to be performed and causes the results of the integration to be stored on the error card.

5) Restore station to observing configuration (LOC's 067A, 0978 and 09B0, called from LOC's 1047, 1049 and 104B).

These routines undo items 1 and 3 above.

2.3.4 Initialize Software for Next Waveguide Cycle

The software between 1008 and 1023 will initialize various portions of the software for the next waveguide cycle.

2.3.5 Get V_s and Sin x Cos Products From Last Waveguide Cycle

This software, located at LOC 1160 and called from LOC 102E, will shift-in the 50-msec V_s and sin x cos products from the ST-BT cards.

2.3.6 Service Exchange

The subroutine at LOC 1200, called from LOC 1030, will perform all of the tasks required to;

1) parallel a test delay/recirculator path across a dedicated hardware path.

2) cause exchange at a recirculator output of the test path for the dedicated path.

2.3.7 Service Test Delay Lines and Delay Interchange

The subroutine at LOC 05DD, called from LOC 1032, will perform two tasks;

1) Compute a set of delays to be used in programming the test delay lines. This test delay is computed by subtracting a constant (hex A, for continuum for example) from the delay assigned to a delay line across which a test delay line is paralleled.

2) There exists a troubleshooting option in the software whereby the delays assigned to two antennas may be interchanged. This subroutine accomplishes this interchange.

2.3.8 Remove Dump-to-Storage Flags

The subroutine at LOC 10F6, called from LOC 1045, will remove any dump-to-storage flags.

2.3.9 Load Delays

The software at LOC 067A, called from LOC 1047, will load the delays received from SPECTRE during the last data valid period into the delay lines so that they will be effective during the upcoming data valid period.

2.3.10 Enable Continuum Interfaces

When BT 561 is recognized, the subroutine at LOC 0660 is entered via the command at LOC 1054 and continuum interface commands are sent in anticipation of a new waveguide cycle start.

2.3.11 Service Error Lamp

The error lamp is pulsed each waveguide cycle at precisely the same time. Any timing error that causes a missed pulse, or a pulse too soon, will result in an error indication located at LOC 10BC, being called from LOC 1056.

2.3.12 Row 1 Front Panel Lamps

As discussed in Section 2.2.1, item 3, the 27 x 27 LED array is time-multiplexed. The first entry into the subroutine that accomplishes drive into this array is made from LOC 105A.

3.0 SOURCE OF ADDITONAL INFORMATION

The VLA CORRELATOR SOFTWARE MANUAL contains detailed descriptions of each subroutine mentioned in Chapter 2. Table 3-1 is a copy of the complete index for the manual.

Neither the software manual nor the source listing for the System Controller Software will be distributed, but a copy of each will be maintained in the Correlator Room for reference.

TABLE 3-1

CORRELATOR SOFTWARE MANUAL INDEX

Table 3-1 (Continued)

Table 3-1 (Continued)

Table 3-1 (Continued)

Table 3-1 (Continued)

TABLES

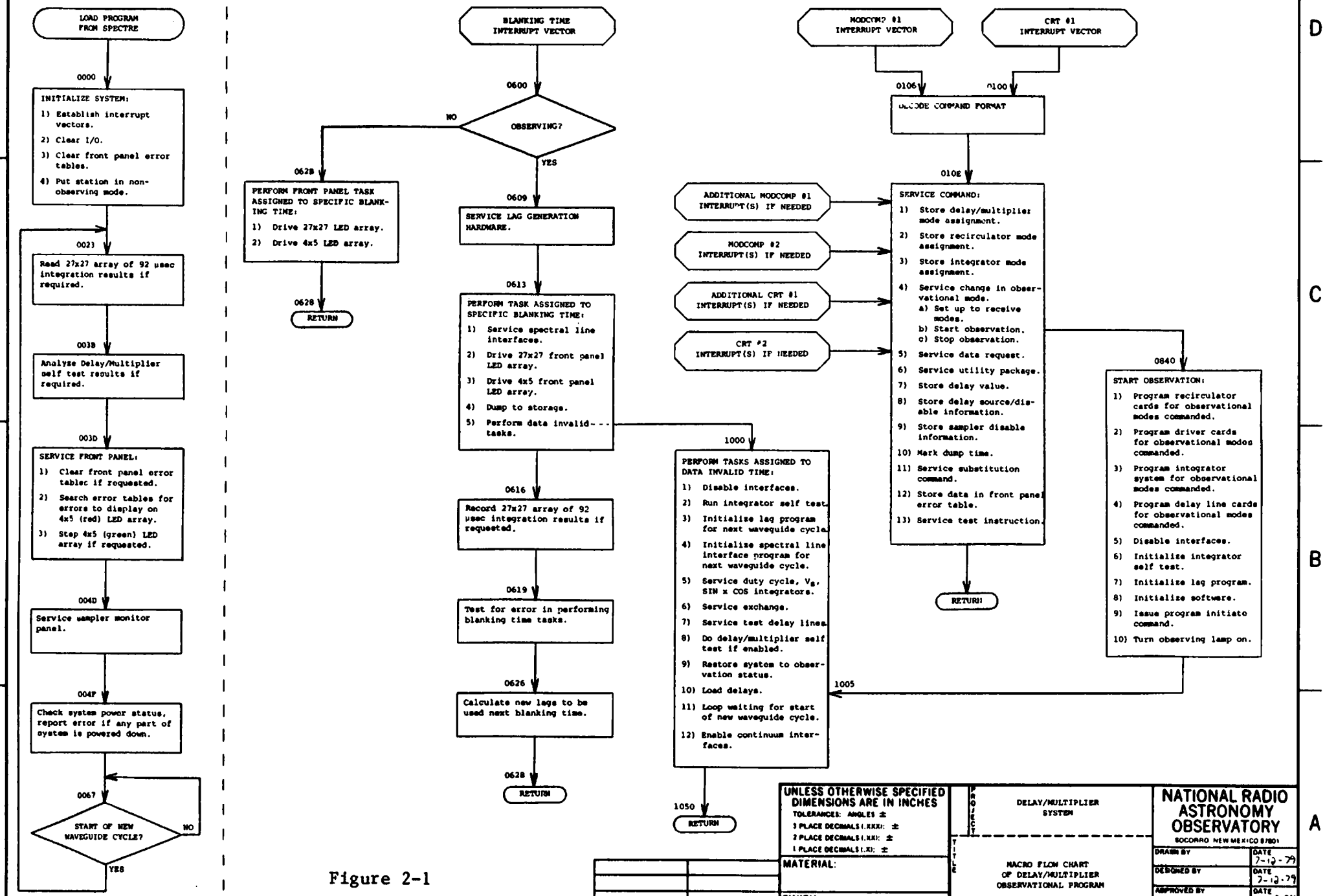


Figure 2-1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
NEXT ASSY | USED ON

PROJECT: DELAY/MULTIPLIER SYSTEM
TITLE: MACRO FLOW CHART OF DELAY/MULTIPLIER OBSERVATIONAL PROGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO NEW MEXICO 87801

DRAWN BY		DATE 7-12-79
DESIGNED BY		DATE 7-12-79
APPROVED BY		DATE 7-12-79

SHEET NUMBER 1 of 1 | DRAWING NUMBER C13800B9 | REV. | SCALE