VLA TECHNICAL REPORT NUMBER 55

ARCHIVE STORAGE UNIT

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1.0 INTRODUCTION

This report will describe the archive storage unit (ASU). This unit consists of a modified consumer-type, VHS video cassette recorder (VCR), plus a 3-1/2 inch rack mounted chassis of electronics for interfacing the VCR to a DEC unibus for the purpose of high volume digital data storage. The ASU interfaces to a DEC unibus via a user interface card supplied by DEC called a DR-11W interface.

The VCR has been modified for 4 Mbit/sec direct digital recording, has a new read amplifier and transverse equalizer installed, and one video read/write head has been adjusted to allow read-after-write capability.

The high error rates, to be expected from uncertified consumer tape casettes, required several strategies for circumvention. First, a powerful error correcting code was utilized. This code, a GOLAY (23,12) code, appends 11 bits of parity to each 12 bits of data, resulting in a three-error correction capability on playback data. Second, an interleaving technique is used which spreads the 23 bits of an ECC block across a large portion of tape to prevent burst errors, common in magnetic tape recording, from overwhelming the GOLAY code. Finally, the read-after-write capability is used to insure the least dependence on the ECC possibility.

In testing thus far no residual erorrs in playback have been observed. The ECC capability alone has proved sufficient to correct all readback errors with the exception of a single damaged cassette.

The ASU is a completely synchronous device with somewhat inefficient start/stop characteristics. For this reason, the ASU is intended for application, such as data archiving, where a steady rate of data flow is available.

All operation of the VCR with the exception of cassette insertion and ejection is under control of a microprocessor in the ASU electronics chassis.

2.0 SPECIFICATION

Unibus data rate: 124.92 Kbyte/sec.

Data storage capacity: 2.7 Gbyte (on a T-120 cassette in 6-hour mode).

Data format: 4096 bytes data plus 68 bytes in a supervisory field, each 1/30 sec.

Tape format: Data naturally blocks on tape in 1/60 second tracks of 4164 bytes, which corresponds to one pass of a rotating video head across the tape.

Tape required: 1/2 inch VHS cassette (any length).

ECC code: 3-error correcting GOLAY (23,12) block code.

Data interleaving: 2776 23-bit ECC blocks spread across 1/60 sec track.

Read-after-write: Reads each track just after write and allows for any track that does not playback perfectly to be re-written.

Residual bit error rate: Less than 1 in 10^{12} bits.

Interface: DEC unibus

Power required: 120 VAC, 60 Hz at 24W for VCR; 120 VAC, 60 Hz at 100W for electronics.

Linear bit density: 17.4 KB/in.

Maximum transition density: 34.8 KØT/in.

Track density: 658 tracks/in (one head).

Areal density: 8.4 Mbit/in^2.

Tape speed: 0.44 IPS.

Head-tape velocity: 230 in/sec.

3.0 BLOCK DIAGRAM

Figures 1 through 4 present the ASU in block diagram form. Figures 1 through 3 follow the three sheets of the logic diagram and Figure 4 is a further breakdown of the ECC circuit.

Page 1 of the ASU logic diagram D3290L02 and Figure 1 describe the I/O logic that interfaces the ASU to a unibus via a DR-11W user interface card. Data is double buffered using two RAM's. In general, one RAM is at the disposal of the unibus while the other services the VCR.

The I/O logic is bus oriented with an internal 16-bit bus. Devices that can be serviced by this bus include the two RAM buffers, a unibus port, an ECC circuit (VCR) port, a microprocessor port, and a read-only error buffer. In general, except for the read-only error buffer, data may be transferred from any device to any other. A ROM controller uses status logic levels from the various devices to sense which, if any, operation is requested and services the requirements by selecting the proper output to enable and the proper device write line to activate.

The ASU microprocessor has an 8-bit command register in this portion of the logic with which it can control operation.

Each of the data buffers is divided into a 2048 x 16 data portion and a 34 x 16 supervisory data portion.

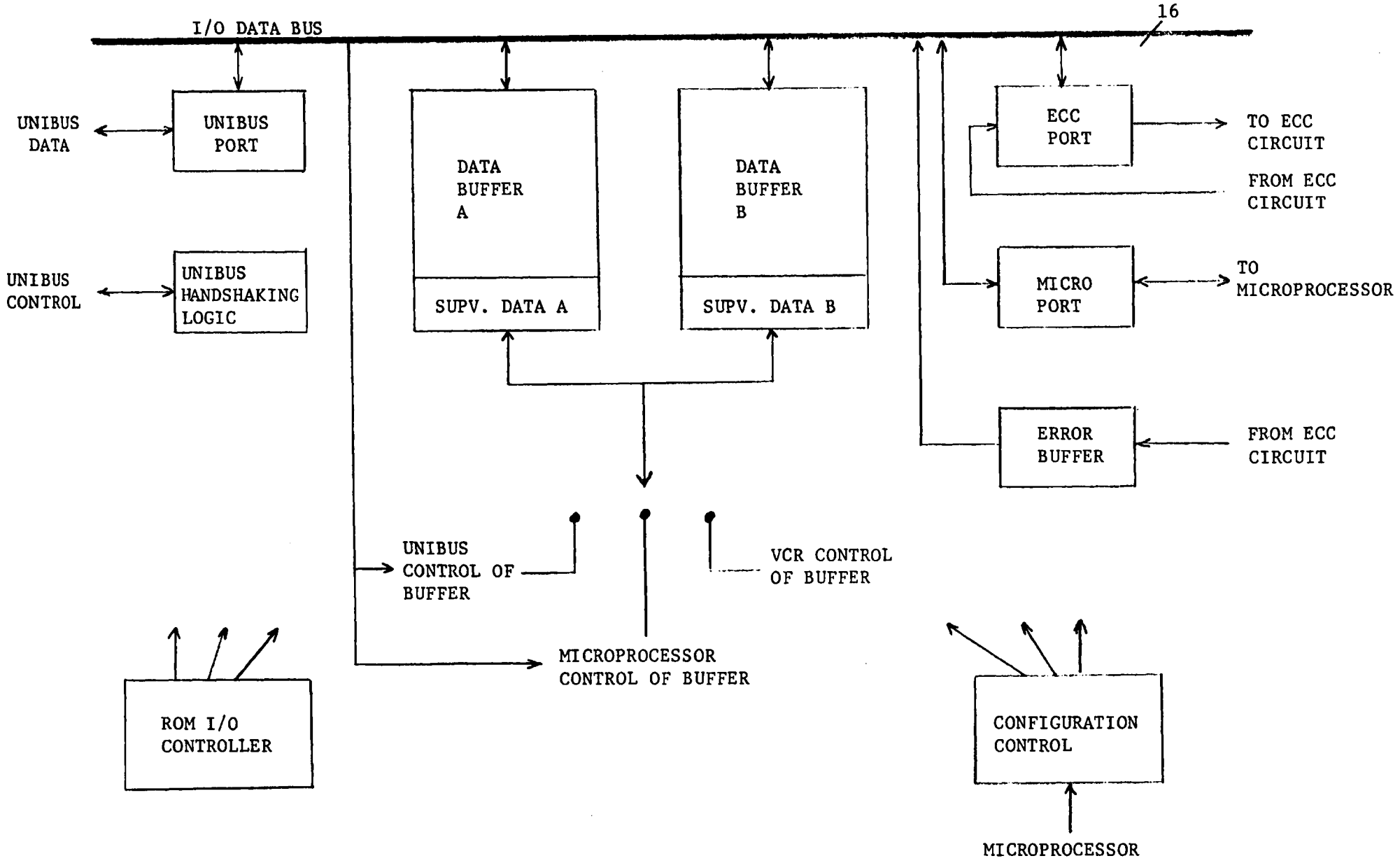


Fig. 1. I/O Block Diagram.

Page 2 of the ASU logic diagram and Figure 2 show the logic for ECC encoding/-correcting, dynamic RAM buffers needed for data interleaving, and two ROM controllers.

The ECC circuit both encodes and corrects data blocks for writing and reading tapes. This circuit is discussed in more detail in considering Figure 4.

The dynamic RAM's are each 65536 x 1 bit RAM's that double buffer data being transferred from the I/O RAM's to VCR or VCR to I/O RAM's. RAM's are needed here because data interleaving occurs at this stage. Data interleaving is accomplished by non-sequential data addressing of the RAM's when data is being transferred between the DRAM's and the VCR.

The two controllers seen on Figure 2 take the 4.0 MHz clock and divide it down to generate event timing signals. The macro controller generates the 60 Hz VCR reference and divides each 1/60 second interval into 512 increments. A ROM look-up table provides timing signals for macro events within the 1/60 second cycle. The micro controller provides micro control through the basic 2832 step data cycle that represents 1/23 of a 1/60 second track. Signals generated by this controller include ECC timing signals, sync times and DRAM counter control lines.

An 8-bit microprocessor port in this logic section allows the ASU microprocessor to configure this logic to accomplish the function desired.

Page 3 of the ASU logic diagram and Figure 3 describe logic in the ASU concerned with timing, reading and writing of the VCR and the microprocessor control of both the VCR and the ASU logic. Basic clock generation occurs in this logic. A 64-MHz crystal oscillator establishes the clock reference. Two dividers (sequence generators) divide this 64-MHz reference down to the basic 4-MHz clock, simultaneously generating timing signals needed by the DRAM's. One of these divides is fixed in radix while the other (the read sequencer) has an adjustable radix which serves as a phase lock loop during tape read operations.

During the read operation the equalized playback voltage from the VCR is clipped and zero crossings detected and processed in two ROM's to provide both radix control for the read sequencer (clock recovery) and data recovery.

The recovered data drives the sync detector which uses a 40-bit data template to look for sync patterns inserted into the data when written. These sync pattern detections control the operation of the DRAM address counters on page 2. To

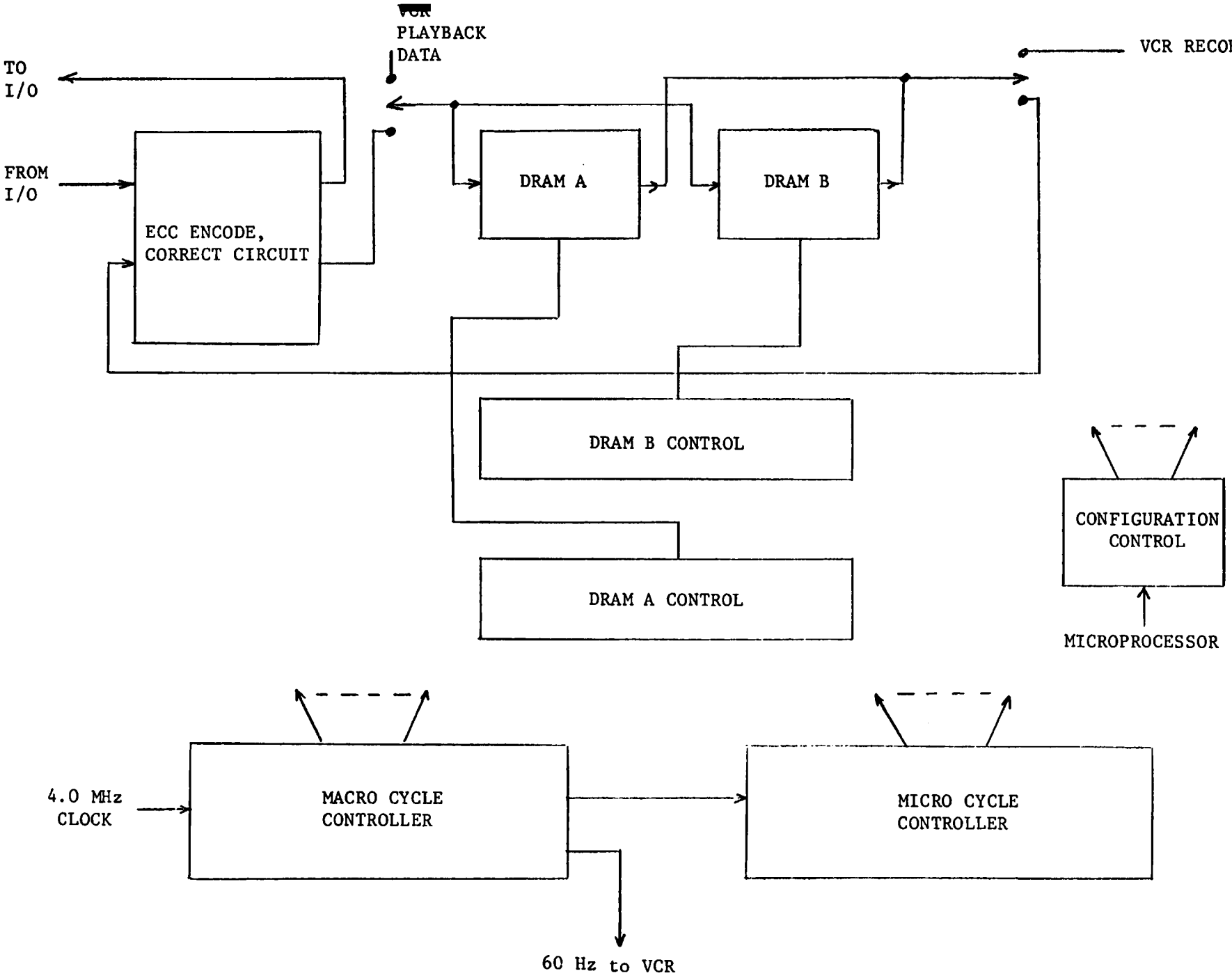


Fig. 2. ECC and DRAM Block Diagram.

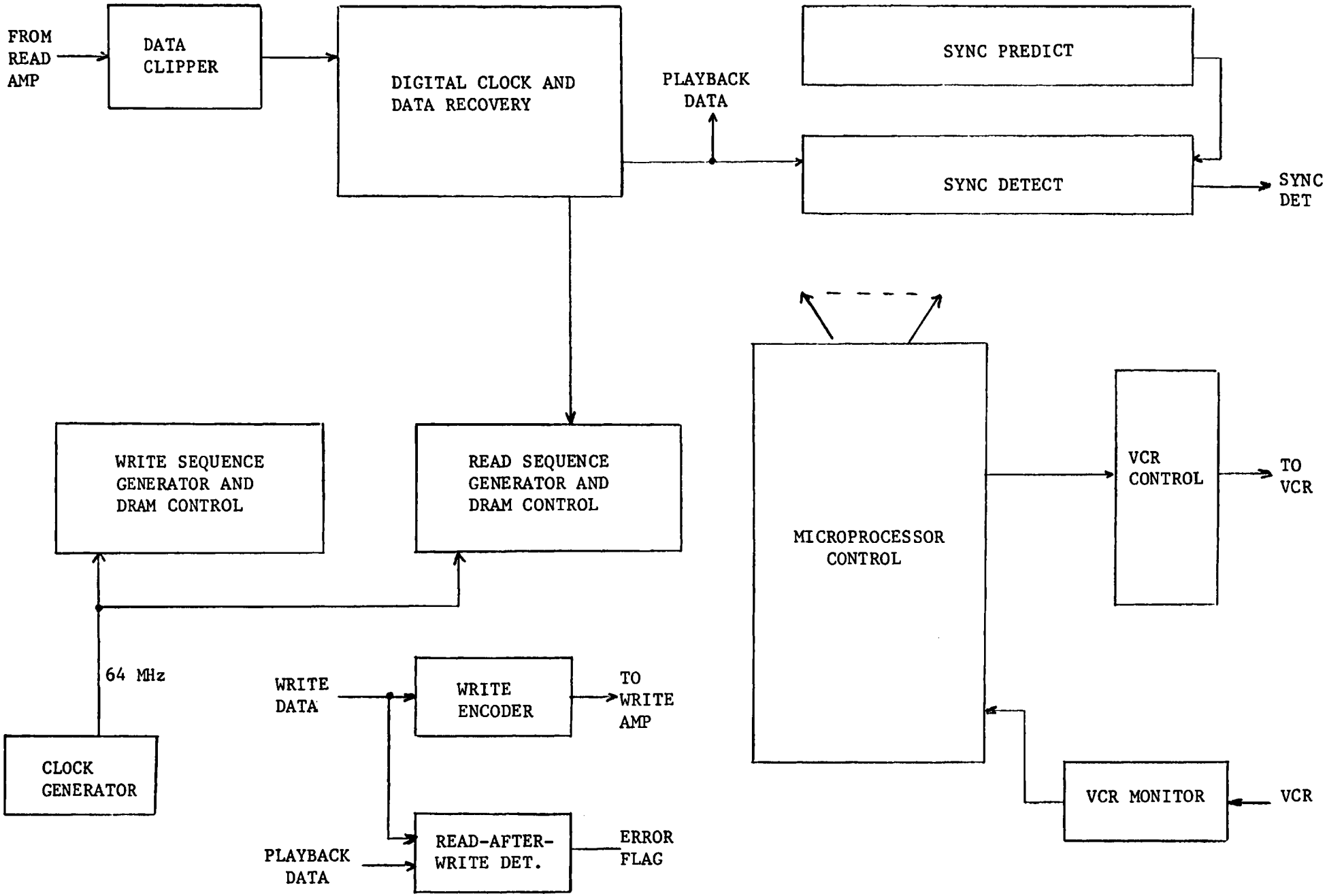


Fig. 3. Data Encoding, Recovery and Microprocessor Block Diagram

allow the logic to flywheel through missing sync pattern (sync patterns obliterated by readback errors) a sync predict counter is also provided.

Overall control of both the ASU logic and the VCR is via an Intel 8748 one-chip microprocessor.

4.0 CIRCUIT DESCRIPTION

4.1 Overview

Before attempting a detailed circuit description, an overview is desirable. The ASU consists of a modified VCR and an electronics chassis. The VCR has been modified in the following ways:

1) The VCR servo electronics has been modified so that it locks its head and capstan servo loops to an externally provided 60 Hz reference in both record and playback.. By locking the VCR head wheel phase to the ASU electronics, proper timing in the record and playback modes can be maintained.

2) A write data input to the VCR has been provided that bypasses the normal VCR FM modulator. This modification allows the ASU logic to write an appropriate magnetic recording code directly onto tape.

3) The playback signal has been provided with a transverse tapped delay line equalizer and this equalized output is taken directly from the VCR for demodulation by the ASU electronics.

4) The ASU microprocessor has been provided with hard wired access to the VCR front panel function switches. With this control, the ASU microprocessor can operate the VCR with minimum operator intervention.

5) Various monitor points within the VCR have been brought out so that the ASU microprocessor can tell the operational status of the VCR.

6) Means have been provided to the ASU microprocessor to keep a tape position counter to allow it and the master computer to know at all times where within a tape cassette the current position is.

7) One head of the two-head video head wheel has been adjusted slightly so that it can play back the other head's track. This adjusted head must be of the same polarity as the unadjusted head and is used for read-after-write.

The modified VCR thus provides a magnetic recorder channel, through which a signal such as a 4 Mbit/sec Manchester code may be recorded. Playback, with a properly adjusted equalizer, will provide a signalling channel with a native error rate of about 1 in 10^8 bits. Poor tape quality, however, can quickly

degrade the error rate down to the 1 in 10^4 range. In addition to a large increase in isolated bit errors, poor tape can also result in signal dropouts which occur at discrete locations on the tape where the oxide coating is damaged or missing. Large tape flaws may cause loss of signal for over 100 microseconds on each of several adjacent tracks. A longitudinal scratch on the tape, a not infrequent flaw in old tapes, can cause 100 microsecond losses of signal on consecutive tracks for many seconds. The term track is used here to denote the path one video head takes as it sweeps diagonally across the tape during a 1/60 second, one-half revolution of the head wheel.

Within each track, about 65536 bits may be recorded using a 4.0 Mbit/sec record rate. This recording rate results in a linear bit density of 17.4 Kbit/in. The rotating head lays down tracks with a 658 track/in. density (using one head). An areal bit density of about 8.4 Mbit/in^2 is thus obtained.

The main task of the ASU electronics is to utilize the very high areal bit density capability of a VCR in a computer peripheral application. The high error rate of a VCR must be dealt with if computer data storage is to be attempted.

4.2 Error Correction Strategy

Three levels of error correction is used in the ASU:

1) A read-after-write capability has been provided. Since the VCR has two video heads on its spinning head wheel assembly, one head could be dedicated to read-after-write. This dedication resulted in having the possible data rate of a VCR writing at 4.0 Mbit/sec by reducing the write duty cycle to 50%. In this mode, one head writes a 1/60 second track diagonally across the tape. As this head leaves the tape, the opposite head contacts the tape. This head has been slightly re-positioned to allow for the small amount of the tape movement resulting in its reading the track just written by the first head. A bit-by-bit comparison is made between this playback data and the data that was to have been written which is still in DRAM. If exact comparison does not occur, a rewrite is made.

2) A GOLAY (23,12) block error correcting code is used. This code records 23-bit blocks of information for each 12 bits of raw information to be stored. Upon playback, up to three errors within the 23-bit field may be corrected.

3) 2776 of the 23-bit blocks of encoded information are interleaved so that no bit of any of a given 23-bit block is physically within 2775 bits on tape of a second bit from the same 23-bit block.

Of the three levels of error protection above, items 2 and 3 are normally sufficient to allow all but physically damaged cassettes to play back error free. Read-after-write, however, allows the power of the ECC correction to be reserved for tape aging effects.

Page 2 of the ASU logic diagram has a diagram of the ASU track format located just below the center on the left side of the page. This diagram illustrates the makeup of data on a single 1/60 second track. As the video head assembly rotates, a read/write head starts across the tape, starting at the tape edge just at the left-hand edge of the track diagram. The first several hundred microseconds of a track is written with logic zero's so that on playback the phase lock loop has plenty of time to lock up after headswitch. Following these leading zero's are 23 groups of bits, each consisting of a 56-bit sync pattern followed by 2776 data bits. The first group contains the 2776 first bits of the 2776 23-bit blocks to be written in a track. The second group contains a sync pattern followed by all 2776 of the second bits in each 23-bit block. All the third bits are recorded next, etc. Thus, a dropout of, say, 200 bits in playback will lose 200 bits of data which consist of only one bit in each of 200 independent 23-bit ECC blocks, all of which are within the capacity of the ECC circuit to correct. An incidental trailing sync pattern and some trailing zero's complete a track makeup.

Loss of a sync pattern due to a tape defect does not affect the ASU performance since the ASU logic contains a counter that can predict sync time. If the very first sync pattern of a track on playback is lost, the entire first 2776-bit block of data is lost, but proper operation will start when the next sync pattern is detected.

Loss of bit sync and a subsequent bit slip in the phase lock loop during a long dropout can also be corrected by the next properly received sync pulse.

In general, no single tape flaw, short of a massive defect that disrupts playback for several milliseconds, will result in uncorrected errors propagating through the ECC circuit on playback. A sequence of four properly spaced flaws within a single track are normally required to cause uncorrected errors.

4.3 I/O Logic Description

As seen in Figure 1, the I/O logic consists of bus oriented ports controlled by a ROM controller. The ports that sit on the internal I/O bus are:

1) The Unibus - The unibus interface consists of two 16-bit buses, one for each data direction, and various handshaking, status, and interrupt lines. Diagrams of the handshake sequence are shown on page 1 of the ASU logic diagram. All I/O transactions are started by the unibus DR-11W via a pulse on its GO line with additional word transactions being initiated by the END signal. The controller is notified of a required action on its part by a logic high on the UNIBUS SERV REQ line. The three FNCT lines tell the controller what action is required. Table I defines the actions possible:

TABLE I

FNCT 1	FNCT 2	FNCT 3	ACTION
0	0	0	Unibus writes to address reg.
1	0	0	Unibus writes supv. data.
0	1	0	Unibus writes data.
1	1	0	Unibus writes to microprocessor.
0	0	1	Unibus reads supv. data.
1	0	1	Unibus reads data.
0	1	1	Unibus reads error counter.
1	1	1	Not used.

2) The ASU Microprocessor - The ASU microprocessor interface consists of two 16-bit registers, one for each direction of data flow. The ASU micro writes data to some unit on the I/O internal bus by writing 8 bits to IC F64, 8 bits to IC F62, 3 bits of direction code (S8, S9 and S10) to IC F44 and by pulsing signal EN5 setting the μPROC SERV REQ line. The controller senses action required via the SERV REQ line and routes data via the S8, S9 and S10 bits. Table II defines the actions possible:

TABLE II

S8	S9	S10	ACTION
0	0	0	μproc writes to address reg.
1	0	0	μproc writes supv. data.
0	1	0	μproc writes data.
1	1	0	μproc writes to unibus.

TABLE II (continued)

S8	S9	S10	ACTION
0	0	1	µproc reads supv. data.
1	0	1	µproc reads data.
0	1	1	µproc reads error counter.
1	1	1	Error written to unibus blindly

3) The VCR - The VCR may only read 16-bits from the data buffer or write to that buffer. The micro-controller lines C5 nd C6 control this action. These lines also control IC's E24 and E23 that serially interface with the ECC circuit. Table III illustrates:

TABLE III

C5	C6	ACTION
0	0	Hold.
1	0	Right shift register.
0	1	Write to buffer.
1	1	Read buffer.

4) The Error Register - This counter is controlled by the ECC circuit and is read-only on this page of the logic diagram.

5) Data Buffers - The data buffers consist of two 2082 x 16 RAM's. The two RAM's are used for double buffering. The microprocessor controlled signal S13 determines the assignment of RAM's to either the unibus I/O or the VCR output.

6) Data Buffer Address Register - The data buffers may be addressed by any of three address registers. The unibus address register (E45 and E42) is presettable by command from the unibus port and increments each time the unibus accesses data or supervisory data. The µproc address register is presettable by command from the microprocessor and also auto increments. The VCR port also has an independent address register used as a buffer and is accessed by the ECC logic.

Of the six devices on the ASU internal I/O bus, only the unibus, the microprocessor, or the VCR may initiate a transaction, the other devices being

sources or destinations. An internal bus transaction proceeds by the controller ROM IC F23 recognizing an action request from an initiating device and in one clock pulse selecting the proper output to enable (OE0 through OE6) via IC F53, selecting the proper write line to strobe (W0 through W6) in IC F43 and selecting which, if any, buffer address register to auto-increment via signals AS0 through AS2 in IC F33.

The controller ROM handles bus contention by assigning priority in the following way:

Highest Priority: VCR req (C5 and C6)
Next Priority: Unibus req (UNIBUS SERV REQ)
Lowest Priority: µproc req (µPROC SERV REQ)

IC E35, controlled by signal S13, sets the assignment of buffer A (IC E16 and E11) and Buffer B (IC E36 and E31) between unibus or microprocessor (W4 and OE4) and the VCR (W5 and OE5). The EX-OR gate E34-3, also controlled by S13, does the same for the supervisory buffer. IC's E46 and E41 are internally divided into supv. buffer A and B.

In a typical application, say writing a tape, the process goes as follows: Signal S13 is, say, high. At the beginning of a 1/30 second cycle, the unibus is notified, via an interrupt on its ATTN line and microprocessor set status bits DSTAT A, B and C, that it has a buffer available. Since S13 is high, it can then write data into data or supv. data buffer B. It will normally, through the next 1/30 second, fill first the data buffer (B) with 2048 words of data and then the supv. data buffer (B) with 34 words of data. It could, if desired, preset its buffer address counter to some location other than zero (which is set by the microprocessor before the ATTN interrupt) and write data starting anywhere in the buffer. While buffer B is being filled by the unibus computer, the VCR is reading all 2082 words of data/supv. data written into buffer A previously by the unibus computer. This read is via shift registers E24 and E23 which provide serial 4 Mbit/sec data into the ECC circuit. Since the ECC circuit is driven by a fully synchronous controller, it must have data on request and, hence, this port has the highest priority on the buffers.

At the end of this 1/30 second period, all of the data in buffer A has been ECC encoded and buffer B is full of new data. The microprocessor will

at the start of the next 1/30 second cycle switch the logic state of signal S13 and the cycle will repeat.

4.4 ECC Circuit

The upper left corner of sheet 2 of the ASU logic diagram gives the logic design of the (23,12) GOLAY ECC encoder/corrector circuit. Figure 4 gives a more basic block diagram. Operation is as follows:

1) Encoding - The three 74LS399 IC's (C46, C45 and C44) and the associated EX-OR gates form a division circuit. The intent is to take 12 bits of data and treat them as binary coefficients of a 12-term polynomial. The 74LS399 circuit will divide this polynomial by an ECC generator polynomial:

$$X^{11} + X^{10} + X^6 + X^5 + X^4 + X^2 + 1.$$

After a serial division of 12 clock cycles, an 11-bit division remainder is left in the 74LS399 registers. The original 12 bits were saved in IC's C34, C33 and C32. Now the original 12 bits and the 11-bit remainder are strobed into the 23-bit shift register C15, C14 and C13. The 74LS08 chips insure no action is taken by the C16 and C36 ROM's or the C24, C23 and C22 EX-OR gates. Thus, the 23 bits consisting of 12 bits of data plus 11 bits of division remainder are shifted out into the dynamic RAM's and eventually get recorded on tape.

2) Correcting - The 23 bits being played back from tape are divided in the 74LS399 divider circuit by the original generator polynomial. Since this 23-bit block contained 12 bits plus a division remainder, the full 23-bit division should result in a zero remainder. If any bit(s) of the 23-bit block are in error, however, a non zero remainder results. This remainder, called the 11-bit syndrome, has a precise mathematical relation to the error pattern. The (23,12) GOLAY code used happens to be a "perfect code." There exists exactly 2048 possible ways to make either 0 or 1 or 2 or 3 errors in 23 bits and the 11-bit syndrome can enumerate exactly 2048 patterns. The look-up table ROM's C16 and C36 convert the 11-bit syndrome into the error pattern concerning the original 12 data bits (that is, errors in the original 12 bits are corrected, errors that occur in the 11 parity bits are ignored by the C16 and C26 ROM's since these bits are discarded anyway). The C24, C23 and C22 EX-OR gates correct the erroneous bits and the corrected 12-bit data pattern is clocked into the C14, C13 register for serial shift out to the static RAM's. A running error

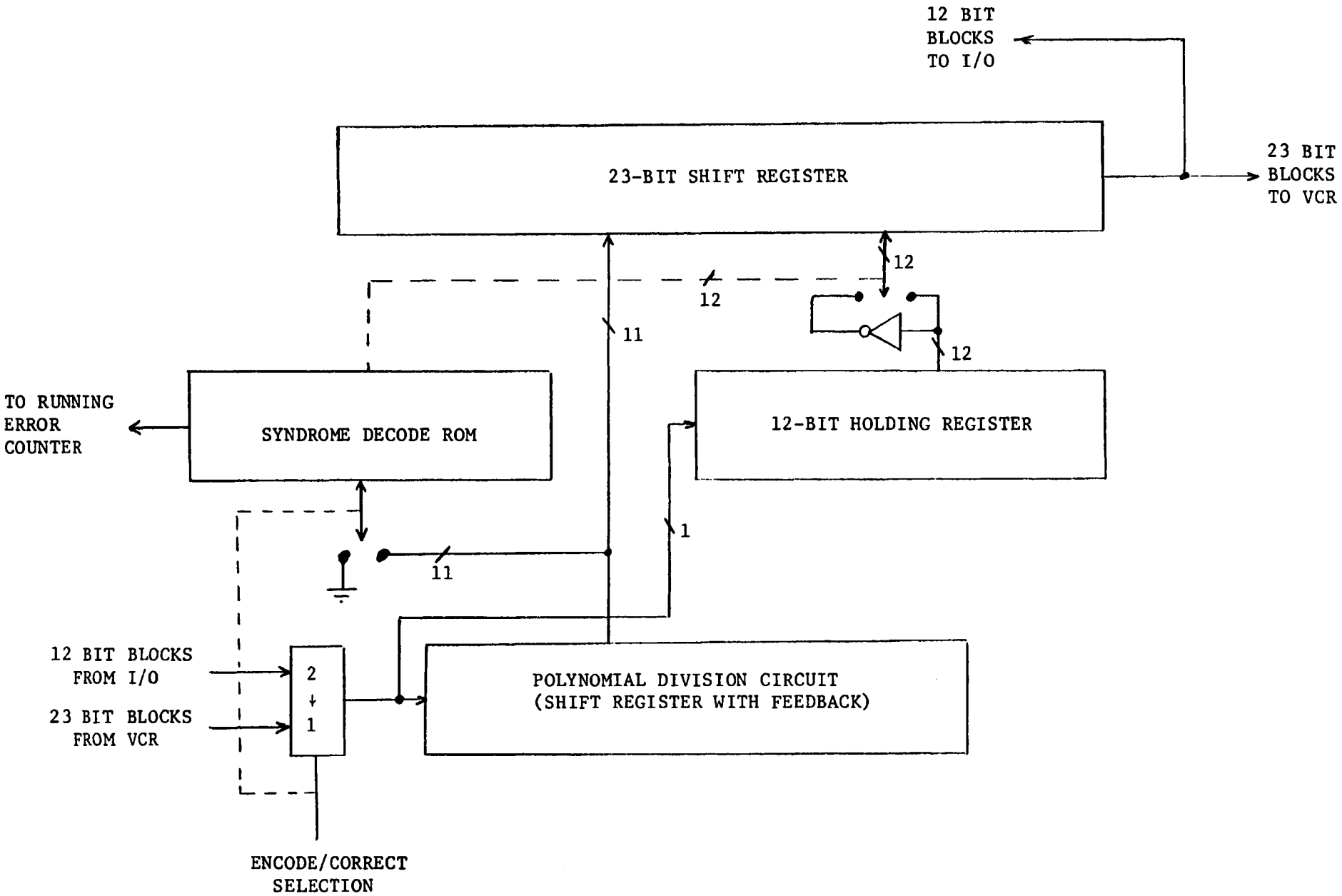


Fig. 4. ECC Circuit Block Diagram.

count is kept by the ERR0 through ERR3 bits adding the number of bit errors detected into the (ASU schematic, page 1) adder consisting of IC's F65, F55 and F46. This running error sum can be read at the end of a VCR track to give the unibus CPU an idea of tape quality. Good tape quality should result in zero track error counts over 95% of the time.

4.5 Dynamic RAM's

As mentioned earlier, data interleaving is necessary to prevent error bursts from overwhelming the ECC circuit. The dynamic RAM's are used in the interleaving process. On each track, these RAM's are loaded with 2776 23-bit error encoded blocks from the static RAM via the ECC circuit during record. This total of 63848 bits are stored into the DRAM's in memory location order. That is, the first bit of a track goes into memory location 0, the next into memory location 1, the next into 2, etc., through all 63848 locations used. This is accomplished by incrementing the 74S482 counters by one each time a bit is written into a DRAM.

Data is taken out of the DRAM's for recording on tape in a much different order. In stead of incrementing by one for each bit read, the full adders in the 74S482's are used to add 23. Thus, the bits come out in the order:

0, 23, 46, 69, 92, 115, 138, ---, 63779, 63802, 63825, 1, 24, 47

The overflow from 63825 to 1 is accomplished by parallel loading the 74S482's from the C66 ROM. In effect, the transfer sequence of bits from DRAM to tape will take all the 2776 bit 1's of the 2776 23-bit ECC blocks, followed by all 2776 bit 2's, followed by all 2776 bit 3's, etc.

On playback the same thing occurs unscrambling the bits. In going from VCR to DRAM's, the playback bits are written into every 23rd DRAM location. In going from DRAM to static RAM (via the error correction circuit), the DRAM locations are read in order.

4.6 Counters and Controllers

The counters in the lower left corner of sheet 2 of the logic diagram form a divide by 67072 circuit in three stages. C65 and C64 form a ÷ by 131, C63 and C62 a ÷ by 256, and D63-6 a ÷ by 2. The resulting output at D63-6 is a 60 Hz square wave. The combination of C63, C62 and D63-6 and ROM C66 form a 512 step macro sequencer. ROM C66 provides gross macro-timing signals, such

as the overflow locations to the DRAM address counters in their count by 23 mode. The resolution of this macro sequencer is 131 4-MHz cycles or 32.75 μsec.

The eight outputs of this controller include:

1) The five-bit, non-sequential DRAM address overflow locations.

2) WTRACK whose falling edge starts the recording of a track of data onto the VCR.

3) The VCR 60-Hz reference is generated in the ROM and allows for the time offset that exists between the VCR 60-Hz reference and the VCR headswitch signal.

4) Pin 17 of C66 provides timing for interrupting the μproc and for predicting the final sync pulse of a track.

The second controller on sheet 2 of the ASU logic diagram is the micro sequencer. IC's D45, D55 and D65 form a ÷ by 2832 circuit. The ROM controller D16, D36, D46 and D66 (which act as a single 8192 x 8 ROM) control the bit-by-bit operation of the data flow from static RAM to VCR or from VCR to static RAM. The 2832 bit loop consists of 1/23 of a VCR track which is a 56-bit sync pattern followed by 2776 bits of data (all bit N's of the 2776 23-bit ECC blocks).

In order to understand the requirements of the micro sequencer, it will be necessary to explain the four-cycle ASU process as shown in Figure 5.

The micro-sequencer is not used in cycle 1 or 3 in record or in cycle 0 or 2 in playback since these cycles depend on wowing and fluttering playback clock and the micro-sequencer runs in the fixed 4 MHz write clock.

During cycle 0 or 2 of record, the micro controller ROM provides the following signals:

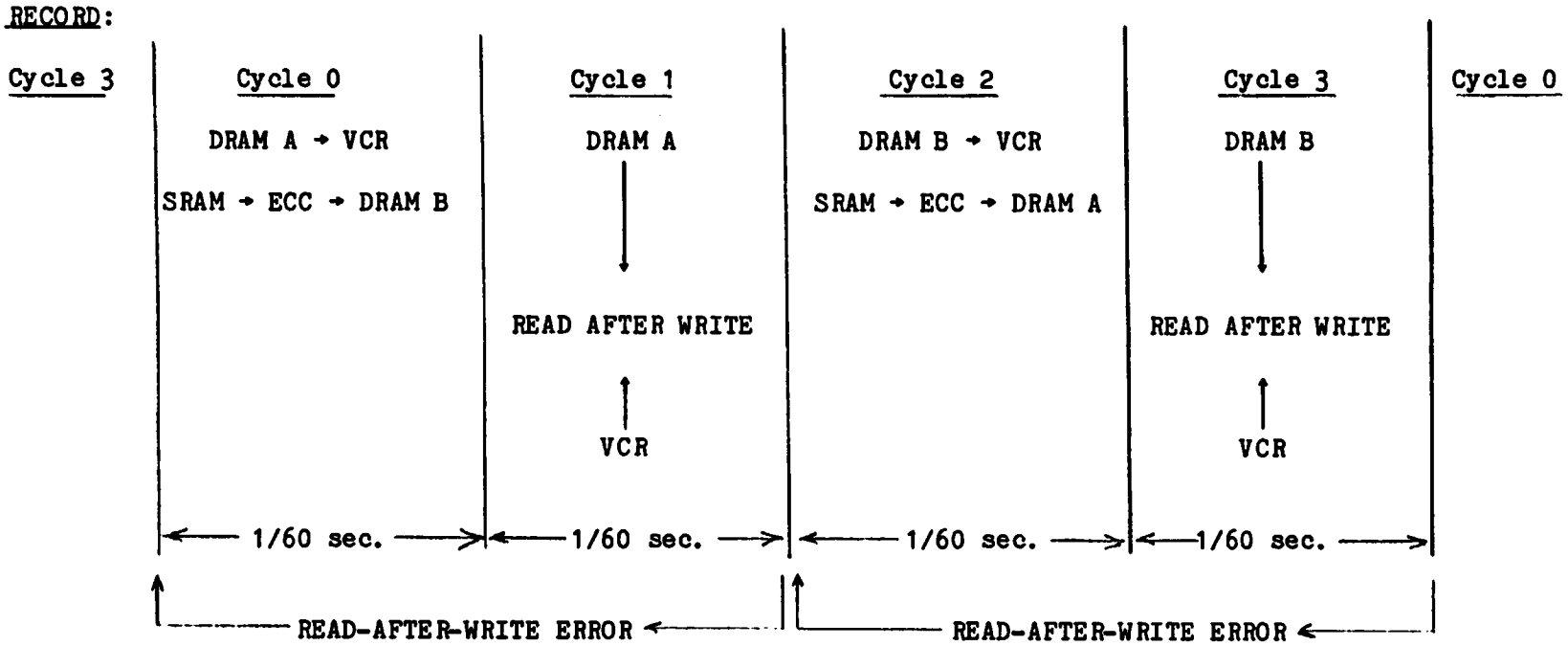
C0 - is a 56-bit up, 2776-bit down signal that signals sync record time. It switches MUX D11-7 from DRAM data to C1 sync pattern.

C1 - the actual 50-bit sync pattern (000089247B703B Hex).

C2 - this signal restarts the 12-bit ECC division each 23 bits.

C3 - is a gate for the 12 data bits shifted into C34, C33 and C32.

C4 - is the parallel load pulse for the 23 bit C15, C14, C13 register.



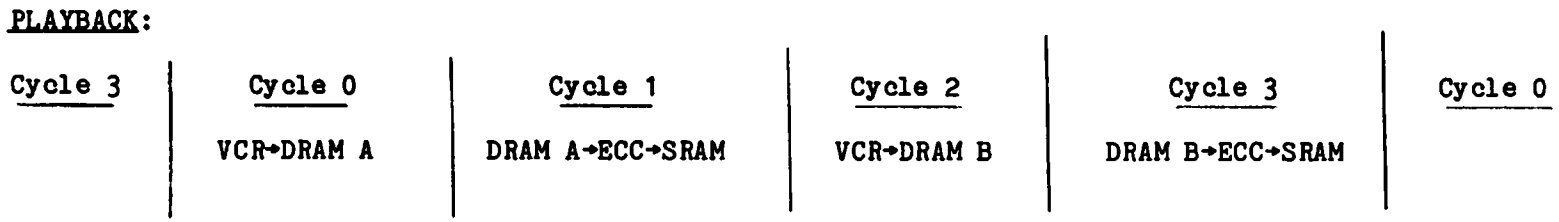


Fig. 5. ASU Data Flow Diagram.

C5 and C6 - control the static RAM and I/O controller and the E24, E23 serial shift register.

C7 - enables the count by one input into the DRAM address counters.

The action for cycle 0 in record is as follows:

1) If C0 is high, C1, the sync pattern, is written onto tape. When C0 is low, DRAM A, previously filled with 2776 23-bit ECC blocks, is read in non-sequential mode, (its address counter incrementing by 23 each clock). Signals C2 through C7 control data flow from static RAM's, through the serial I/O port, through the ECC circuit and sequentially into DRAM.

The action for cycle 1 in playback is as follows:

1) Again, C2 through C7 control data flow, properly blocking the 23 and 12 bit operations, sequentially out of the DRAM, through the ECC corrections, through the serial I/O port, into static RAM.

During playback the DRAM address counters run off of unstable playback clock. The non-sequential overflow restart address (location 63825 to location 1, etc.) is handled by the recovered sync pattern via IC's D25-7 and D25-9. The C66 macro controller provides the restart addresses on an approximate time scale and SYNC PATT does the exact strobe.

4.7 Modulator

IC A36-5 on sheet 3 of the ASU logic diagram is the Manchester code modulator. It puts out a 2 MHz square wave if WDATA is low and 4 MHz if WDATA is high.

4.8 Write Timing Generator

IC's A63, A65, A64, A62-9 and A66 form a divide by 16 Johnston counter. This counter divides the 64 MHz crystal oscillator down to the 4 MHz bit rate. The timing diagram in the lower left corner of sheet 3 illustrates the operation

of this counter and how it also generates the timing signals necessary for DRAM operation.

4.9 Read Circuit

The read amplifier output from the VCR drives the input of the LM360 at the top left of sheet 3 of the ASU schematic. This comparator and the two 74F74 flip/flops are the clipper and quantizer in the read circuit.

IC's B63, B62, B52, B61, B51 and B41 yield clock and data recovery from the clipper/quantizer output. The operation can be seen from the sketch just below the clipper. This sketch shows one playback bit. All playback bits have flux transitions at the bit boundaries and logic 1's have an additional flux transition in the center of a bit cell. The B63 shift register and B62 and B52 registers form samples across a bit cell as seen by the arrows. The B61 ROM compares the H and G samples for data recovery (H = G yields logic 0, H ≠ G yields logic 1). The position of a zero crossing across samples A through G shows the phase offset and allows compensating phase adjustments via the variable radix counter A55.

ROM B51 (and secondary storage B41) hold a count. A phase offset seen by ROM B61 will increment or decrement this counter depending on the error direction. Overflow or underflow of this counter will result in a phase correction via PBCC1 through PBCC3 signals changing the radix of A55. The counter within ROM B51 thus sets the loop constant.

4.10 Read Timing Generator

IC's A55, A52-5, A54 and A53 form a second Johnston counter. This counter runs just as does the write timing generator, except that since the radix of A55 is adjustable it can be made to follow the wow and flutter of the VCR playback.

4.11 Sync Detection/Prediction

The comparators and counters at the top of page 3 of the ASU schematic form a template for sync detection and a counter for filling sync pulses missed by playback errors. Only 40 of the 56 bits of sync are checked. The first 16 bits of a sync pattern are zero's to allow the phase lock loop to re-sync in case of loss of bit sync during a long dropout.

The signal SYNC DET indicates a detected sync pattern and signal $\overline{\text{SYNC DET}}$ indicates either a received or predicted sync pattern.

4.12 Microprocessor

IC A11/A21 is an Intel 8748 one-chip microprocessor used to control gross (in time) actions of the ASU. This microprocessor can receive instructions from the unibus CPU. The command format takes the form of one or two 16-bit words with the command format given in Table VI.

The 8748 monitors and controls the ASU via 8 write ports controlled by signals EN0 through EN7 decoded in IC A23, 8 read ports controlled by signals EN8 through EN15 decoded in IC A33, its parallel input/output ports P1 and P2, and the I, T0 and T1 interrupt and sense lines. Table IV gives the function of the EN0 through EN15 signals.

TABLE IV

Signal	Sheet	IC	Use	Function
EN0	3	A14	Write	Control VCR
EN1	2	D64	Write	Control DRAM/ECC
EN2	1	F44	Write	Control I/O logic
EN3	1	F64	Write	Write LSbyte to I/O logic
EN4	1	F62	Write	Write MSbyte to I/O logic
EN5	1	F35	Strobe	I/O logic service request
EN6	1	F16	Write	DR-11W interface lines

TABLE IV (continued)

Signal	Sheet	IC	Use	Function
EN7				Not used
EN8	1	F63	Read	Read LSbyte of I/O logic
EN9	1	F61	Read	Read MSbyte of I/O logic
EN10	1	F25	Strobe	Interrupt unibus CPU ATTN
EN11	2	D53	Strobe	Reset 60 Hz interrupt
EN12	1	F36	Strobe	Reset unibus RAM address counter
EN13	3	A51	Strobe	Reset error
EN14	3	B55	Strobe	Reset reel count interrupt
EN15				Not used

A bit-by-bit description of the 8748 ports is given below:

EN00

Command (PV1520)	Command (PV1370)	Function
01	01	Fast forward
02	02	Stop
04	04	Rewind
08	08	Pause
04 (in play)	10	9X speed reverse
01 (in play)	20	9X speed forward
40	40	Play
80 then C0	80 then C0	Record

EN01 - (See D64 on sheet 2.)

Signal S0 - controls, via IC's D11-7, D25 and D15, source and destination of data to/from DRAM's.

Signal S1 - selects, via IC's D51 and D12, if W clock or PB clock controls DRAM's.

Signal S2 - controls, via IC C53-7, if static RAM's or dynamic RAM's drive ECC circuit (encode or correct); also controls microcontroller ROM.

Signal S3 - controls random or sequential addressing mode for DRAM A address counter.

Signal S4 - same as S3, except for DRAM B.

Signal S5 - controls, via gates D54-3 and D54-6, data flow to/from static RAM's.

Signal S6 - enables DRAM A write signal.

Signal S7 - enables DRAM B write signal.

EN02:

Signals S8, S9, S10 - see Table II.

Signal S13 - switches via IC E35 and E34-3 between static RAM banks (double buffer banks).

EN06 - see Table VII.

The two input/output ports P1 and P2 on the 8748 serve for both input and output. A bit-by-bit description is given below:

Port 1:

Bit 0 - output, stops the read timing generator and, hence, DRAM RAS and CAS so that changeover between read and write clocks in the DRAM circuit can be made without glitching DRAM's and causing data loss.

Bit 1 - input, ERROR is result of read-after-write comparison.

Bit 2 - input, WTRACK gives the 8748 timing information.

Bit 3 - input, PBTRACK tells the 8748 if a read-after-write comparison saw even a single sync pulse. PBTRACK blanks error comparator A51-10 since comparison must wait for playback start of data. If no sync pulse is even seen, PBTRACK never goes high and ERROR is low. Thus, the criteria for good read-after-write comparison is PBTRACK = 1 and ERROR = 0.

Bit 4 - input, allows 8748 to sense if a reel position counter interrupt has been received.

Bit 5 - output, rewrite front panel lamp.

Port 2: (all inputs)

Bit 0 - headswitch (30 Hz) from VCR.

Bit 1 - load complete from VCR.

Bit 2 - play monitor point from VCR.

Bit 3 - record monitor point from VCR.

Bit 4 - FF/REW monitor point from VCR.

Bit 5 - SLP monitor point from VCR.

Bit 6 - cassette down monitor point from VCR.

Bit 7 - power on/off from VCR.

5.0 ASU INTERFACE SPECIFICATION

5.1 Introduction

The unibus computer controls the archive storage unit (ASU). Communications with this unit is via DMA transfers with only one exception as will be described below. The DR11-W unibus controller function lines will control the operation of a unibus to archive storage unit DMA transfer. The possible options for a DMA transfer are given and explained below in Table V:

TABLE V

FNCT. 1	FNCT. 2	FNCT. 3	FUNCTION
0	0	0	Unibus writes to address register
1	0	0	Unibus writes supervisory data
0	1	0	Unibus writes data
1	1	0	Unibus writes to ASU microprocessor
0	0	1	Unibus reads supervisory data
1	0	1	Unibus reads data
0	1	1	Unibus reads error counter
1	1	1	Not used

A) Unibus Writes to Address Register

This DMA transfer will write one word to an internal register in the ASU. The range of addresses is 0000 through 07FF for data or 0000 through 0021 for supervisory data. (See Section 5.3.C).

B. Unibus Writes Supervisory Data

This DMA transfer will write from 1 to 33 words to the ASU which will get subsequentially written onto tape as supervisory data. An N block transfer will get written into the ASU memory starting at the address specified by A, above, with the ASU address counter automatically incrementing through the N locations.

C. Unibus Writes Data

This DMA transfer will write from 1 to 2048 words to the ASU data buffer. The start address will be set as in A, above.

D. Unibus Writes to ASU Microprocessor

This DMA transfer will write one or two 16-bit words to the ASU microprocessor. This transfer will command the action of the ASU. Command protocol is given in the next section.

E. Unibus Reads Supervisory Data

This DMA transfer will transfer from 1 to 34 words of supervisory data from the ASU to the unibus computer. The start address of the block is specified as in A, above.

F. Unibus Reads Data

This DMA transfer will transfer from 1 to 2048 words of data from the ASU to the unibus controller. The start address of the block is specified as in A, above.

G. Unibus Reads Error Counter

This DMA transfer will transfer one word from the ASU to the unibus controller. This word will specify the number of errors corrected by the ASU ECC logic in the last VCR track.

5.2 Command Protocol

Any action of the ASU must be initiated by the unibus computer. The unibus computer has two types of control over the ASU. The first control is via the DR11-W initialize line which will reset the ASU to an inactive state.

The second type of control the unibus computer has over the ASU is via the DMA transfer defined in Section 5.1, above. The protocol for this control is given in Table VI.

TABLE VI

COMMAND WORD		DATA WORD	FUNCTION
0000		NONE	NO-OP
0001	(1)(2)	PPPP	SLEW TO POSITION PPPP
0002	(2)	NONE	REWIND CASSETTE (TO END)
0003	(2)	NONE	FF CASSETTE (TO END)
NN04	(2)	NONE	PAUSE RECORDER NN SEC.
0005	(2)	NONE	STOP RECORDER
NN06	(2)	NONE	SLEW FORWARD NN SECONDS
NN07	(2)	NONE	SLEW BACKWARD NN SECONDS
0008	(3)	NONE	RECORD
0009	(3)	NONE	RECORD (NO REWRITE)
000A	(3)	NONE	PLAYBACK
000B	(1)(2)	PPPP	INITIALIZE POSITION COUNT TO PPPP
00TC		NONE	TEST
XXPD	(2)	NONE	WRITE XX TO PORT P
000E		NONE	RESET
000F	(1)(2)	NONE	PUT PPPP IN SUPV. RAM

NOTES: 1) PPPP is a tape position indicator and is maintained by the ASU microprocessor via an interrupt from the VCR tape-up reel. It is never initialized by the ASU microprocessor but can be set to any 16-bit number by the unibus computer. If set to 0000 at the start of a six-hour cassette by the unibus computer, it will be at about position 7000 for the PV1370 VCR or 1500 for the PV1520 VCR by cassette end. Since the interrupt comes from the tape reel, it is not linear; at cassette start a delta of 1 in the PPPP position represents about 11 tracks and at cassette end about 36 tracks (for the PV1370 VCR). The unibus computer can read the PPPP code at any time via the 000F command word followed by a supervisory data RAM read.

2) ASU interrupts the unibus computer upon completion.

3) ASU interrupts the unibus computer when the VCR is up to speed and data transfer can proceed.

The ASU microprocessor can initiate communication between the ASU and the unibus computer via the DR11-W attention line. The microprocessor will pulse the attention line which results in a CPU interrupt if interrupts are

enabled. The ASU microprocessor will pass 3 bits of status to the DR11-W status register when it issues an ATTEN interrupt. Table VII gives the function of the status bits. The unibus computer can, upon interrupt, read the DR11-W status word to obtain these 3 bits. This 3-bit transfer is the only non-DMA transfer between the unibus computer and the ASU.

TABLE VII

DSTAT C	DSTAT B	DSTAT A	FUNCTION
0	0	0	NO-OP
0	0	1 (1)	COMMAND COMPLETE
0	1	0 (2) (4)	BUFFER READY
0	1	1 (3) (4)	DATA READY
1	0	0	END OF CASSETTE
1	0	1	REWRITE
1	1	0	ERROR
1	1	1	NOT IN SLP MODE

NOTES: 1) See note 2 on Table VI.

2) Occurs each 1/30 second while in record except when rewrite required.

3) Occurs each 1/30 second while in playback.

4) Address counter will have been set to zero just before interrupt issue.

5) Not in SLP mode function occurs in place of buffer ready or data ready in record or playback modes.

5.3 Hardware Structure

The ASU hardware to the unibus computer consists of 2 memory buffers and 3 registers as defined below:

A. Supervisory Data Buffer

This buffer is a 34-word read/write memory that gets recorded in all tracks of a tape cassette. The first 33 words are unibus computer defined and are intended for such uses as time, data, record numbers, names, record boundaries, track number, etc. The last word is a 16-bit tape position indicator (0000 for start of cassette and 7000/1500 for end of cassette) which in recording mode is written into LOC 0021 of the supervisory data buffer, and hence onto tape by the ASU microprocessor. In playback mode LOC 0021 of the supervisory

data buffer will be the playback position indicator as recorded on tape. In both record and playback modes, the ASU microprocessor will also write the position indicator into LOC 0022 of the supervisory data buffer. Thus in record, LOC's 0021 and 0022 contain the same 16-bit position indicator while in playback mode LOC 0021 is the position indicator read from tape while LOC 0022 is the ASU microprocessor position indicator. These two position numbers may and may not be the same.

B. Data Buffer

This buffer is a 2048 read/write memory which gets recorded on the VCR tape or contains playback data.

C. Address Register

This register will address either of the two memories above and is a write-only register. It is reset to zero just prior to issuance of a buffer ready or data ready interrupt by the ASU. Upon reception of one of these interrupts, the unibus computer can write (buffer ready) or read (data ready) the 2048 data buffer words starting at location zero without writing a start address to the ASU. Overflow from word 2047 of the data buffer to word Ø of the supervisory data buffer is automatic but the DR11-W FNCT. 1, 2 and 3 bits must be changed from data to supervisory data.

D. Error Counter

This register is a read-only register and will give the number of errors corrected by the ASU ECC logic in the current 2082 word playback track.

E. ASU Microprocessor

This register provides for a 16-bit command word transfer from the unibus computer to the ASU microprocessor (see Table VI).

5.4 Record Sequence

Below is a typical record sequence in which VLA archive tapes are transcribed onto a VCR cassette via the ASU:

A. Operator loads a cassette into the VCR.

B. The unibus computer issues a command to the ASU telling it to record.

C. The ASU microprocessor starts the VCR and when it is up to speed, it interrupts the unibus computer telling it that a data buffer is ready.

D. The unibus computer has 1/30 second to write 2048 words of data and 33 words of supervisory data. Each block transfer must be preceded by setting

the DR11-W FNCT. 1, 2 and 3 bits (to 010 for data, then to 100 for supervisory data).

E. The ASU interrupts the unibus computer when it again has buffer space available.

F. Repeat D and E until finished.

6.0 TESTER OPERATION

The ASU tester is a microprocessor based, unibus/DR-11W simulator that can run various diagnostic and operational tests on an ASU. This unit has a high-speed 6809 CPU and interfaces to the ASU via its DR-11W ports. The tester also interfaces with a CRT (1200 baud, 7-bit, no parity, echo from ASU tester).

On master reset the ASU tester puts a * prompt on the CRT. The utility program in the ASU tester allows an operator to display tester memory, modify tester memory, or execute tester memory as below:

DXXXX C/R will display 16 bytes starting at memory location XXXX. Additional C/R's get 16 more bytes each.

MXXXX YY ZZ C/R will modify memory location XXXX to YY and XXXX+1 to ZZ. The C/R ends modification.

GXXXX C/R will act as a jump to location XXXX. (Do an RTI to return.)

If the operator types "E" (no C/R required), the ASU tester will print its error buffer with the format described in Sections 6.5.11 and 6.5.12. In addition to these utility operations, the ASU tester firmware has various ASU specific tests it can run.

6.1 Command

The ASU tester can simulate the unibus CPU by sending 16-bit words as typed on the CRT to the ASU 8748. In this way, an operator can manually do anything with the ASU via the command format in Table VI that the unibus CPU can do. This function is like a utility operation as described below:

CXXXX C/R - will write XXXX to the ASU 8748.

Examples: (1) C000A C/R will put the ASU in playback.

(2) C000B C/R

C1234 C/R will initilize the position counter to 1234 (hex).

6.2 Switch

If the operator types "S" on the CRT, the ASU tester will command the 8748 to switch static memory banks. No carriage return is needed.

6.3 Loop

If the operator types "L" on the CRT (again no C/R), the ASU does the following:

1) Set a psuedo random data generator seed to 0000 (hex).

2) Download 2082 16-bit words from ASU tester into static RAM (whichever memory bank that is selected).

3) Switches memory banks (so the just downloaded data can be passed through the ECC circuit into a DRAM).

4) Takes data out of static RAM, through the ECC circuit, and into DRAM.

5) Takes just loaded DRAM and reads its data through the ECC correction circuit and static RAM.

6) Switches memory banks.

7) ASU tester reads 2082 16 bits of data that just circulated through the ASU (but was not put on tape) and compares to original data.

8) ASU tester reads running error count to see if ECC circuit had to correct any errors.

9) Add one to psuedo random data seed and loop to step 2.

This loop will continue forever. If any errors are detected, they are printed out. If no errors were corrected by the ECC circuit and if no errors propagated through the ECC circuit, the ASU tester will print out every 256th data seed. Thus, a bad loop test results in nothing being printed (I/O hung up) or errors being printed. A good test will result in a column of numbers on the CRT.

0000
0100
0200
0300
0400
----

with a new number being printed each 77 seconds.

6.4 Play

If the operator types "P" on the CRT (no C/R), the ASU will read two tracks of a tape (if the VCR is loaded and playing a valid ASU cassette). Comparison between data on tape and data in ASU tester memory starting at LOC D800 and extending for 2084 words is attempted and any errors printed on the CRT. The error counter is also printed out. If the cassette being played was recorded using test E (Section 6.5.E), a "P" command will result in printout of about four words in each track read:

1) The track number.
2) The position counter.
3-4) Two words just out of the legal ASU buffer.

plus the error count.

6.5 Tests

There are 15 tests that can be run with the ASU tester. A test is started by an operator typing TX C/R on the CRT to perform test X. An "R" (no C/R) typed on the CRT or a master ASU tester reset will stop some of the endless loop tests.

6.5.1 Test 1

Test 1 is an endless loop of writing a binary count to an ASU static RAM (whichever is selected).

6.5.2 Test 2

Same as test 1, except binary count written to supervisory RAM.

6.5.3 Test 3

Same as test 1, except binary count written to unibus address counter.

6.5.4 Test 4

Contents of ASU tester memory location F002-F003 (16 bits) is endlessly written to the ASU microprocessor.

6.5.5 Test 5

ASU tester will go into endless loop reading static RAM (data read thrown away).

6.5.6 Test 6

Same as test 5, except ASU tester reads supervisory RAM.

6.5.7 Test 7

ASU tester will read ASU error counter and print on CRT.

6.5.8 Test 8

Test 8 will take a psuedo random data generator seed word stored by the operator at ASU tester memory location F000-F001 (16 bits), fill a buffer from its location D800 to E7FF with a pseudo random data pattern and downloads this pattern into the ASU static data and supervisory RAM (whichever bank selected).

6.5.9 Test 9

Test 9 will read 2084 words out of whichever static data and supervisory RAM is selected and compare the contents against its buffer starting at LOC D800. Any deviation of ASU data from predicted is printed, expected and actual, on the CRT. The printout is limited to the first 16 errors to prevent scroll off the screen. If no printout results, comparison was perfect.

6.5.10 Test A, B, C, D

Test A, B, C, or D will cause a 1/60 second transfer (a complete dump) of data between various RAM's in the ASU as defined below:

Test	Transfer
A	Static RAM → ECC (encode) → DRAM A
B	DRAM A → ECC (correct) → Static RAM
C	Static RAM → ECC (encode) → DRAM B
D	DRAM B → ECC (correct) → Static RAM

After test B or D, the error buffer may be read (test 7).

6.5.11 Test E

Test E will write most of a 6-hour cassette with psuedo random data. The psuedo random pattern seed is operator enter at ASU tester location F000-F001 (16 bits). All VCR tracks written on tape during the 6-hour write are identical except for two 16-bit words. The ASU tester adds a unique 16-bit track number to each track and the ASU microprocessor writes the reel position counter into the buffer before it is put on tape.

ASU tester memory location F002 is an operator set test parameter. If LOC F002 = 08, the ASU will do read-after-write and rewrite tracks that play back with errors. If LOC F002 ≠ 8, no rewrites are performed.

At the end of about 5.65 hours (2.5 Gbytes of data recorded), the VCR will be commanded to rewind, a count of tracks written and a count of track rewrites (followed by several fields of zero) will be printed on the CRT. Upon completion of cassette rewind, test F will be automatically entered.

6.5.12 Test F

Test F can be entered either automatically from test E, as above, or in the normal way of the operator typing TF C/R. Test F will read and verify a cassette written by test E, above. The CRT printout obtained from test F is as follows:

1) In most cases the test F printout will be a single line of 15 four-character hex numbers. The first four-character entry in this line will be the position counter. The next 14 four-character entries are of one of the forms below:

0XXX	XXX errors corrected during track read by ECC circuit. Track was not rewritten.
FXXX	XXX as above, but F indicates this track was rewritten later because of read-after-write error during test E.
F000	The F indicates, as above, that this track did not play back perfect during test E read-after-write and was rewritten. However, the 000 indicates that it played back error free this time (during test F).

2) If an out of sequence track number is read, the CRT will line feed up, but print nothing otherwise.

If track was not rewritten (test F knows this because its track number was not repeated as in a rewrite by the following VCR track) and if the ECC circuit had to correct no errors, then nothing is printed on the CRT. Since over 90% of the VCR tracks should be error-free, both during test E and test F, the CRT cursor should move only slowly across the one line being printed.

3) If an error propagates through the ECC circuit, the ASU tester will carriage return, print the track number, print the number of errors corrected by the ECC in that track, print the number of uncorrected errors that propagated through the ECC circuit, and carriage return again.

At the end of 2.5 Gbytes of data tested by test F, an automatic error printout appears on the CRT. The printout format is:

AAAAAA BBBBBB CCCCCC DDDDDDDD EEEEEEEE FFFF

where

AAAAAA = total number of tracks tested (hex)

BBBBBB = total tracks rewritten or that required ECC corrections made

CCCCCC = total tracks in BBBBBB, above, that required ECC corrections made

DDDDDDDD = total number of bit errors corrected by ECC circuit

EEEEEEEE = total number of bit errors in DDDDDDDD, above, that were in rewritten tracks

FFFF = total number of word errors that propagated through the ECC circuit.

7.0 FIRMWARE DESCRIPTION

The Intel 8748 ASU microprocessor is a one-chip microcomputer with onboard UVROM and RAM. The 1K x 8 ROM contains all of the firmware to control and operate the ASU. The 8748 duties include:

1) Communication with the unibus CPU to support the command structure of Table VI.

2) Control and monitor the VCR.

3) Dynamic configuration of the ASU logic via its control ports to accomplish the four-cycle operation described in Section 4.6.

4) Monitor self test.

5) Support reel position counter.

6) Aid DRAM switch between read and write clock.

7) Perform various diagnostic tests.

7.1 Register and RAM Assignments

Register R0 and R1: These microprocessor registers are utility registers used for various applications throughout the ASU program.

Register R2: Register R2 contains an ASU mode word that allows the ASU microprocessor to support the operation desired. A bit-by-bit functional definition is given below:

BIT 4 AND 5 MODE

Bit 4	Bit 5	Function
0	0	Idle
1	0	Record
0	1	Playback
1	1	Record with read-after-write

BIT 0 + 1 MISC. STATUS

Bit 0	Bit 1	Function
0	0	No action pending
1	0	60 Hz interrupt
0	1	Attn flag
1	1	Attn flag with rewrite

BIT 2 ERROR FLAG

Bit 2	Function
0	Check for error
1	No action pending

BIT 3 HEAD SWITCH

Bit 3	Function
0	Headswitch = 0
1	Headswitch = 1

BIT 6 AND 7 CYCLE COUNTER

Bit 6	Bit 7	Function
0	0	Cycle 0
1	0	Cycle 1
0	1	Cycle 2
1	1	Cycle 3

Register R3: Register R3 has the byte to program μproc port EN01 with (see Table IV).

Register R4: Register R4 has the byte to program μproc port EN02 with.

Register R5: Register R5 has the byte to program μproc port EN06 with.

Registers R6 and R7: Registers R6 and R7 are used in the wait subroutine.

RAM LOCATION	FUNCTION
32	Port 2 Storage
33	Error Counter
34	Direction Flag (00, 01, or FF)
35	Position LS Byte
36	Position MS Byte
37	NN Constant
38	Drive to Position LS Byte
39	Drive to Position MS Byte

7.2 Non-Interrupt Routines

Most of the firmware from memory location 0000 to 00A5 is run in the "main loop." Most of the other firmware in the ASU microprocessor is run in interrupt routines. The non-interrupt firmware consists of the initialization (upon power-up or reset) between location 0009 and 0032.

The loop between 0032 and 0038 is where the microprocessor spends 95% of its time. The only two exits from this loop (other than hardware reset)

is an interrupt or via the jump to subroutine PRE-ASM.

The jump at location 0036 is a jump in response to a 60 Hz VCR interrupt. This interrupt will set bit 0 in register R2. The jump to PRE-ASM will allow the microprocessor to execute the firmware between LOC 0040 and 00A5. The action is that after return from a 60 Hz interrupt, the bit in R2 is recognized and the jump to PRE-ASM made. In PRE-ASM the mode and cycle number is sensed and pre-selected ASU program bytes for EN01 and EN02 are loaded in registers R3 and R4. These program bytes will be used to program the ASU logic during the next 60 Hz interrupt.

7.3 Interrupt Routines

An interrupt to the ASU μproc will cause a jump to LOC 0100. There are three possible sources of an interrupt.

1) 60 Hz VCR interrupt
2) Unibus command word interrupt
3) Position counter interrupt

7.3.1 60 Hz VCR Interrupt

A 60 Hz interrupt is recognized by the microprocessor testing the T0 input discrete. Firmware execution starts at location 0300.

In the I60 Hz subroutine, the following things are done:

1) Read ports 1 and 2 to get the results of a possible read-after-write test (port 1) and the headswitch and VCR status (port 2).

2) If in read-after-write, evaluate the read-after-write test. An error is indicated if a) PBTRACK never went high or, b) ERROR is high. If a read-after-write error is sensed, a rewrite is commanded by going back two cycles (in the cycle 0, 1, 2, 3 sequence in section 4.6).

3) If a read-after-write error is sensed, a radix 256 counter is maintained (LOC 0394) in RAM LOC 33. A read-after-write track will be rewritten only 255 times. The reason for limiting rewrites is the one chance in 2^{40} that a 40-bit sync pattern will occur in data. A sync pattern in data will cause the read logic to parallel load the DRAM address counters out of sequence forcing an error in the read-after-write logic even with perfect tape. If a read-after-write limit were not imposed, the accidental presence of a sync pattern in the data would hang the ASU up permanently rewriting this one un-playable track. On playback this same track will playback in error but the ECC circuit

will still correct the disruption caused by the spurious sync detection yielding error free reproduction.

4) Will write out the pre-assembled EN01 and EN02 bytes (starting at LOC 0340). The clocks to the DRAM's are stopped during this program change to prevent the DRAM's from being changed.

5) The error flag is reset.

6) Will put the position counter in the supervisory RAM if necessary (LOC 0370).

7) Will reset the unibus ADDR counter if necessary (LOC 037F).

8) Will check if VCR is in correct mode (LOC 0385).

9) Will set up unibus ATTN interrupt if necessary (LOC 0388).

10) Will reset 60 Hz interrupt.

7.3.2 Unibus Command Interrupt

A unibus command interrupt will cause a jump to subroutine unibus at LOC 106. Two look-up tables from LOC 01E0 to 01EF and from 01F0 and 01FF are used to decode the unibus command. The subroutines addressed from these tables support all of the commands given by the unibus. These commands include several tests that the ASU microprocessor can run. These tests are addressed via LOC 01EC in the first table and all of the second table.

7.3.3 Position Counter Interrupt

Subroutine POSCNT is called to update the microprocessor maintained tape cassette position counter. This subroutine (which calls subroutine UPDATE at LOC 00B0) uses the RAM location 34 direction flag to update the position counter. As position counter interrupts are received, the 8748 will increment (if the VCR is going in the forward direction) or decrement (if the VCR is going in the reverse direction) the position count. The direction flag at RAM LOC 34 indicates the VCR motion direction.