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FOCUS/ROTATION CONTROL SYSTEM, MODEL E

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1.0 INTRODUCTION

This manual describes the new VLA Focus/Rotation Control system and was written to serve as a maintainance guide for the system and modules. The primary purpose of this manual is to provide a detailed functional description of the operation of the system, the modules and control programs. The emphasis is on practical data: module schematic diagrams, control programs, cable drawings, and bin wire lists are included to make this a comprehensive reference manual with all the data that are handy for use on the lab bench or at an Antenna.

A secondary purpose is to describe the functional operation of the mechanical components and the inter-relationships between these components and the control system hardware/software. The manual also has sections which briefly describe the F/R Control System operation, the F/R Mount, the control and F/R Mount specifications and telescope operator CRT overlay & diagnostic information. These sections may be read for information on these topics without bothering to plow through the detailed descriptions of the modules and programs.

1.1 PERFORMANCE SUMMARY

The following table summarizes the performance of the new F/R System.

Parameter	Focus	Rotation
Command execution time	64 sec/12 inches	15 sec/180 deg
Max drive rate	0.197 in/sec	16.7 deg/sec
Readout resolution, (14 bit conversion)	0.000732 in/bit	1.318 arc-min/bit
Command repeatability	0.5 bit,RMS	2 arc-min, RMS
Physical stability	0.001 in	3.85 arc-min

1.2 BACKGROUND

A previous manual (VLA Technical Report No 42, F/R System Manual, Jan 1980), described the first version of the F/R Control System and the F/R Mount. This control equipment was designed in 1974 and is installed in most of the VLA antennas. Specifications for the new system resulted from the need for better performance and experience with the earlier mechanism and electronics. The new control system provides more powerful control, extensive local fault analysis, higher position resolution, more reliable position readout devices, faster mechanism response time and easier maintainance. It is also capable of relatively easy alteration of the control algorithms by changing the firmware. The F/R Mount has undergone extensive mechanical redesign and the Controller design has been made sufficiently general so as to be able to adapt to these changes.

Several experimental versions of F/R Control systems have been used in recent years. A microprocessor controller with synchro position readouts was used in Antenna 27 in 1980. Although the controller operated satisfactorily, it was decided not to retrofit other antennas with this controller until some mechanical design changes were made to improve the the stability of the F/R Mount.

The stability and repeatability of the Subreflector Rotation position is a very critical parameter in that small Subreflector angular position errors

cause large antenna pointing errors. Focus position instability impacts the visibility data phase. Section 10 describes the effects of Subreflector positional errors on pointing and phase. Much of the mechanical and electrical redesign effort has been directed at reducing the Rotation position uncertainty. The unreliability of the position readout potentiometers has also been a persistant problem which has cost many dollars for replacement parts and many man-hours for maintainance and repair time.

An approach to solving the Rotation position uncertainty is an index locking pin mechanism in which a tapered pin is inserted into sockets at angular positions associated with receiver feed horns. An F/R Mount incorporating this feature was installed in Antenna 12 with a new F/R Controller and operated on a trial basis for a year. The idea behind this scheme was that a snug-fit pin/socket combination would provide a tight lock and eliminate the typical 30 to 60 arc-minutes of Rotation ring gear-brake lost motion. The Antenna 12 F/R Control System operated satisfactorily but there were reliability problems with the pin actuation motor so this approach was abandoned and the Antenna 12 F/R Mount was redesigned.

The essence of the final mechanical re-design is to reduce the brake-ring gear lost motion by relocating the Rotation brake to the traveling platform and coupling the brake to the ring gear with only one gear pass. This reduces the Rotation gear slack to about four arc-minutes. The Rotation position readout sensor is relocated so as to be closely coupled (ie one gear pass) to the Subreflector mounting drum. This change eliminates about 1.5 degrees (out of 3200 degrees) lost motion in the existing Rotation ring gear-to-readout potentiometer gear train.

To improve reliability, the Rotation position readout sensor was changed from a potentiometer to a synchro and a high resolution (14 bits) Synchro to Digital Converter. Military reliability analysis has shown that in a given environment, synchros are an order of magnitude more reliable than multi-turn, precision potentiometers. The higher resolution readout has provided a great improvement in the capability of the controller to precisely set and monitor the Rotation position. The Focus position readout potentiometer was also replaced with a synchro and 14 bit S/D Converter. The use of synchros and an integrating S/D Converter has made the position readout circuitry virtually invulnerable to noise perturbations on the long cable runs from the Apex to the Pedestal Room.

After the Antenna 12 prototype system operated for a year without failure or noticeable performance degradation, it was decided to retrofit the new mechanical and electrical designs into all antennas as a part of the periodic antenna refurbishment schedule. The new F/R Controller and reworked F/R Mount have been installed in Antenna 20. Antenna 20 also has a 327 MHz dipole/ring feed system installed in front of the subreflector; this has added several mechanical components to the F/R Mount and Apex structure. When the 327 MHz receiver is in use, the feed ring is extended to enclose the 327 MHz dipoles. When the other receiving bands are used, the ring is retracted back toward a quadrapod spar. Although the ring is not part of the F/R System, the F/R System controls the ring motion because of the proximity of the ring actuator to the Apex junction box and the flexibility of the F/R control electronics.

The existing stepper motors and Translators have been retained but the Translators have been relocated to provide more room in Rack C.

The Apex to Pedestal Room cable structure has not been changed other than signal reassignment of some wires. A 3-wire 110 VAC cable has been added to power the 327 MHz Ring actuator.

Beside the changes described above, a number of mechanical improvements have been incorporated in the F/R mount mechanical design. Notable examples are:

Renovation of the aluminum Rotation ring gear bearing surfaces by steel inserts.

The use of better weather-proof flexible boots over the lead screws and spline shaft.

The use of heaters on the gear box and traveling platform to warm the gear train lubricant to about 40 deg F in cold weather. This prevents cold weather lubricant stiffening which can cause drive sticking problems due to the marginal drive motor torques.

1.3 F/R CONTROL SYSTEM DESCRIPTION

See Figure 1, F/R Control System Block Diagram and Figures 2 & 3 which show the location of the F/R Control System Components.

The F/R Controller closes the position loops and activates all driving elements of the F/R Mount, senses positions and discretes, analyzes conditions in the mount and Pedestal Room to detect faults and reports on these states to Central Control via Data Set 3.

In CMP (Central Computer control) mode, the F/R Controller receives a position command from the Data Set which activates an interrupt in either the Focus or Rotation portion of the controller. The controller tests the Multiplex address and command argument (some Focus arguments are not accepted because of mechanical constraints), and it calculates motor ramping parameters, steering direction and activates the associated brake and stepper motor translator. If brake voltage and current and translator power are above test thresholds and there are no system faults, the controller begins to emit drive pulses to the Stepper Motor Translators so as to null the error. The pulse rate is ramped from 100 Hz to 1000 Hz (500 Hz in Focus) in 50 Hz steps. Drive continues at 1000 Hz until a calculated ramp down position is reached at which time the stepping rate is ramped down to 100 Hz for convergence to the commanded set point. When the set point is reached the controller turns off the Stepper Translator AC and activates the brake.

During ramp-up, main drive, ramp down and convergence, position changes are compared with what they should be to test for drive sticking or dragging. If this happens, the stepping rate is reduced to 100 Hz and the drive is ramped back up to 250 Hz (the peak torque speed of these motors) and the controller attempts to complete the command. In the event that the drive sticks again, the controller aborts the command. When drive sticking occurs, a "Drive Fault" bit is set in the controller status data readout and this bit flags this message on the Operator's Data Checker program and the Operator's F/R Overlay.

In the LOCAL mode (selected by the F/R Controller front panel switch), the F/R system is controlled by actuation of the manual control switches on the F/R Power Supply. These switches are: Focus Drive Up/Down; Rotation Drive CW/CCW; and the Focus and Rotation Ramp/100 Hz switches. LED displays on the Power Supply panel indicate actuation of the brakes, translators etc. In the LOCAL mode the computer commands are ignored and command inputs come from the switches mentioned above. The portion of the control program which implements LOCAL control is similar to the portion which implements CMP (central computer) control and calls the same drivers to perform basic functions such as turning on the brakes, ramping up/down, providing monitor data to the Data Set, etc.

The controller is not directly connected to any circuitry in the Apex; all position and discrete readouts from the Apex are sensed by an Apex Interface unit which transfers this data to the controller via an optically isolated serial link. The Apex Interface front panel displays the Focus and Rotation position in 14 bit octal code and the state of various discretes and activity sensors on an LED annunciator. Logic in the Apex Interface tests for malfunctions; in the event that any of these occur an inhibit (YOWP!) is sent to the F/R Controller to disable all drive outputs. When limit conditions are sensed by the Apex Interface, drive inhibits are sent to the F/R Controller to inhibit further drive into the limit (but not out of the limit). The Apex Interface is isolated from the controller as a lightning protection measure;

it is the sacrificial element in the event of strikes on the Apex structure restricting damage to this unit which has a minimum of parts.

A Switching Module contains the brake controllers (DC power supplies) and solid state relays to switch the AC for the brake controllers, translators and 327 MHz feed ring actuator. A 400 Hz synchro exciter in the Switching Module provides the 400 Hz required by the synchros and the S/D Converters.

A NAP mode has been incorporated to enable the controller to ignore position commands until reset by a RESET command. This permits reduced performance operation in the event of a drive failure.

A ZOT BOX capability has been incorporated into the sysetm to permmit manual control of the Subreflector position by a ZOT BOX which may be plugged into either the F/R control bin or the Apex Junction Box. Discrete and position readouts on the ZOT BOX display the state of the F/R Mount position.

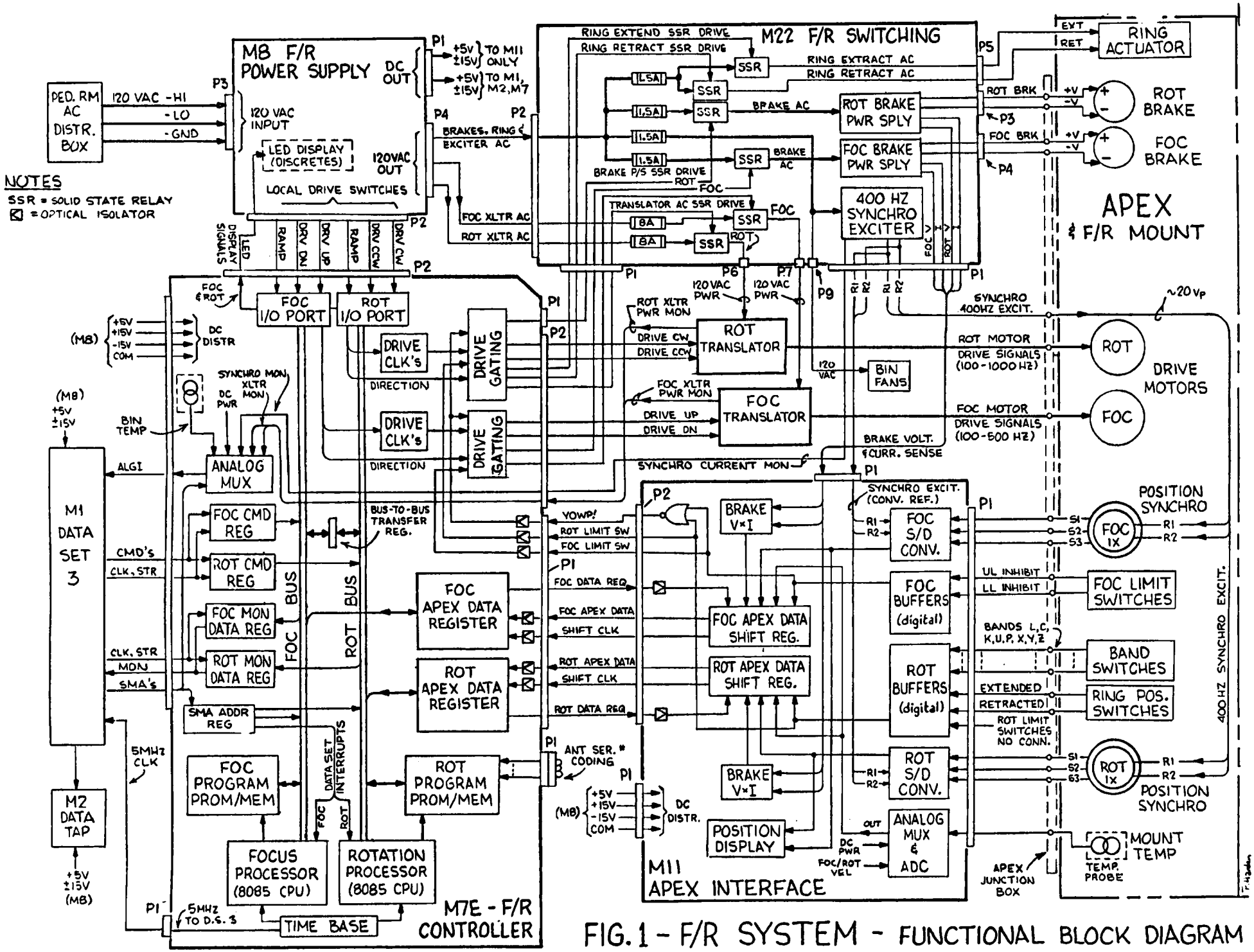
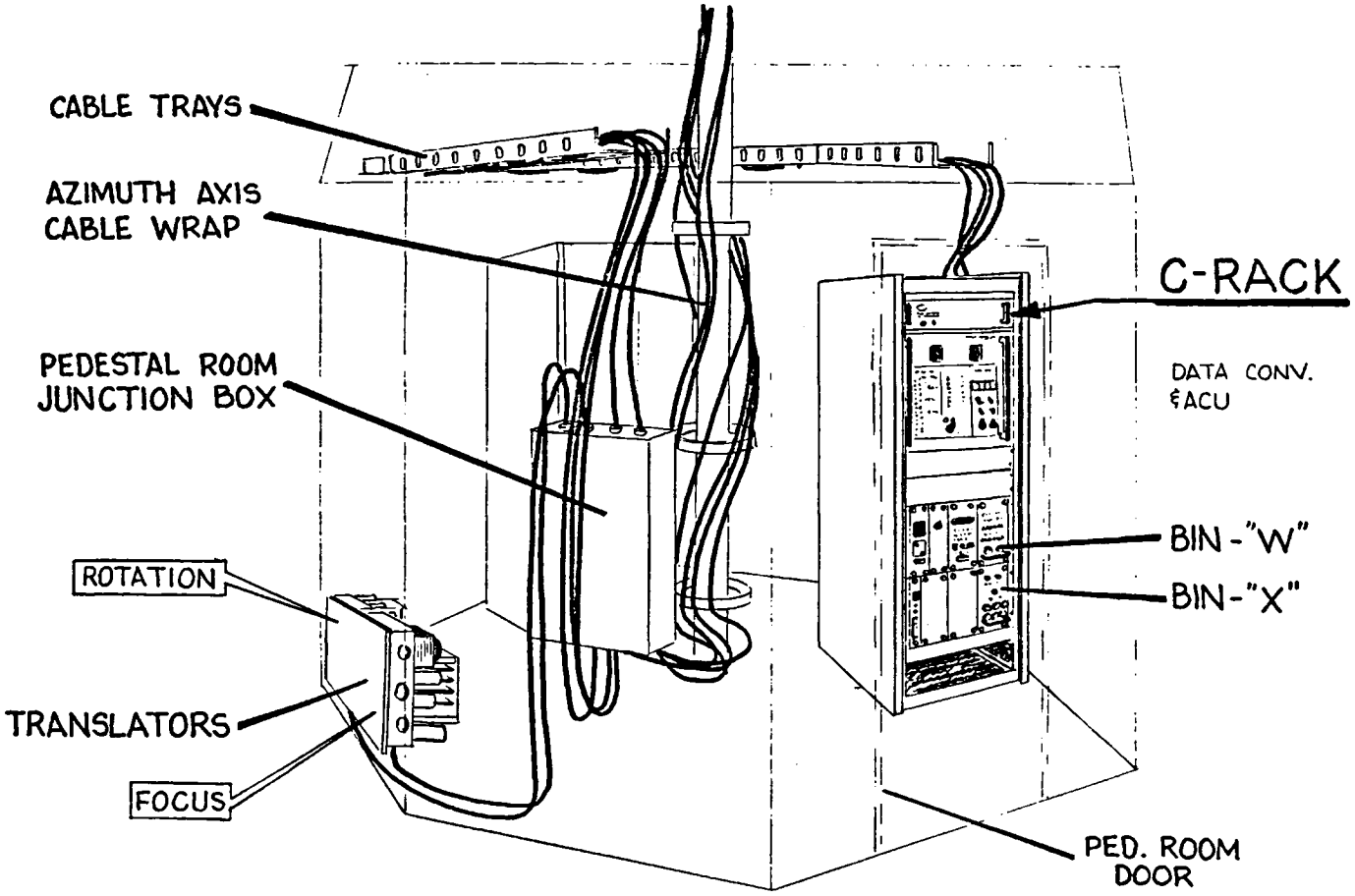
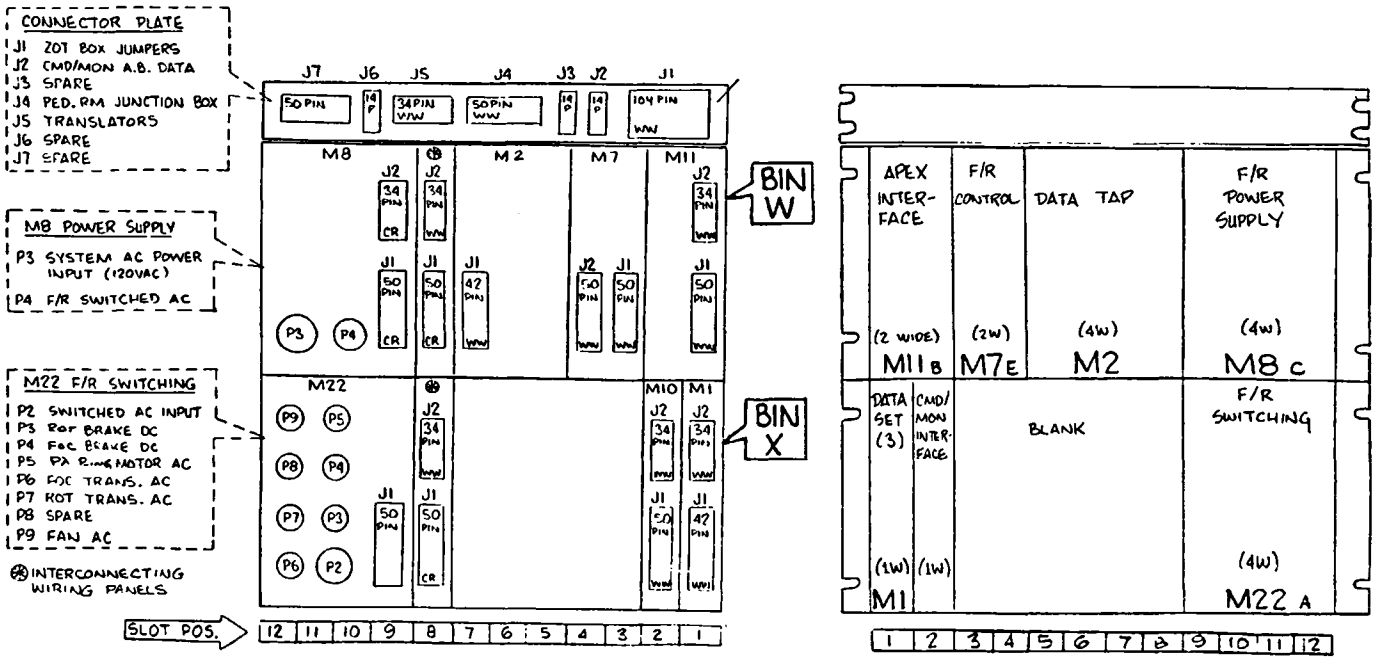


FIG. 1 - F/R SYSTEM - FUNCTIONAL BLOCK DIAGRAM

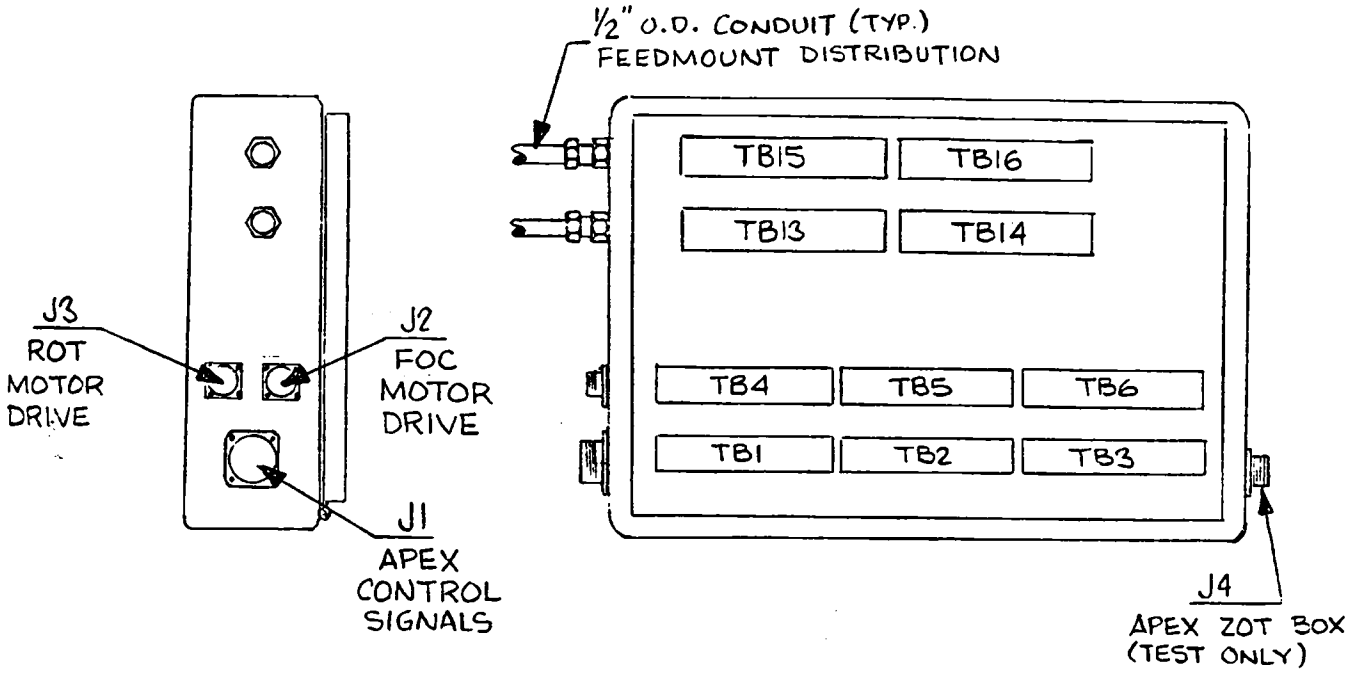


PEDESTAL ROOM F/R COMPONENTS

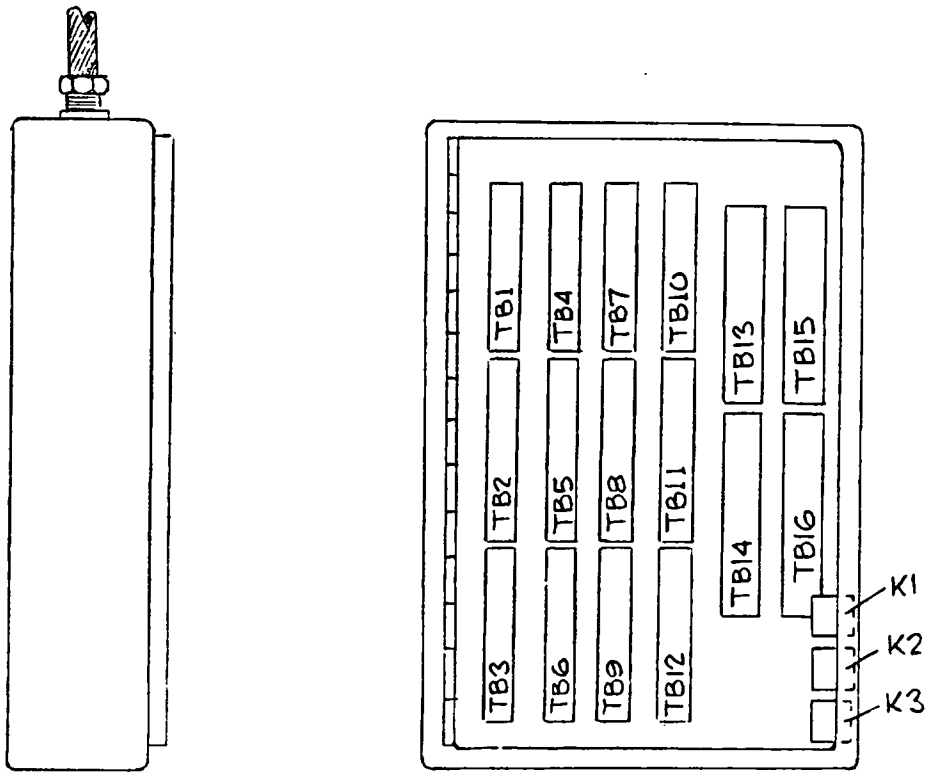


DETAIL - F/R ELECTRONICS BINS W & X

FIG. 2 - PEDESTAL ROOM F/R COMPONENTS



APEX JUNCTION BOX



PEDESTAL ROOM JUNCTION BOX

FIG. 3 APEX & PEDESTAL RM. JUNCTION BOX LAYOUTS

1.4 F/R MOUNT DESCRIPTION

The F/R Mount is almost inaccessible; most of the mechanism parts are enclosed by the gearbox or hidden by the barrel and support structure. This section was written to provide a brief description of the mechanism for electronics maintainance personnel who must understand how the mount operates in order to be able to maintain the electronics.

The F/R Mount is a two axis mechanism consisting of three rings, four guide shafts, four lead screws, two gear trains, two drive motors, two fail-safe brakes and two position readout synchros. Figure 4 depicts the F/R Mount and Subreflector as they appear from the inside of the dish. Figure 5 depicts an exploded isometric view of the F/R Mount and the associated components. Figure 6 depicts the locations of the motors, brakes and Focus position readout synchro.

The top ring is a gear box for the two drive trains; the motors are mounted on the top of the gear box. The Focus motor and gears rotate lead screws which move the Traveling (middle ring) platform up and down the Guide Shafts to produce the Focus motion. The Focus brake is mounted on the top of the gear box and is coupled to the Focus gear train inside the box.

The Rotation motor and gear train drives a sliding spline gear which rotates a large ring gear mounted on the Traveling platform to produce the Rotation motion. The Rotation brake is mounted on the traveling platform and is coupled to the Rotation ring gear through a single gear pass.

A flange on the center of the ~42" diameter barrel is bolted to the Rotation ring gear. The Subreflector is bolted to the bottom of the barrel and counter-weights are bolted to the top of the barrel. The bottom ring is a supporting member for the guide rods and lead screws.

Rubber spring couplings between the drive motors and gear trains buffer the motors so that they are not subjected to large instantaneous inertial loads such as at initial drive motion. The spring deflection is proportional to the torsional loads imposed upon the motor by the drive.

The brakes are fail-safe; that is they are always engaged until energized.

The Rotation gear train reduction ratio is 108:1, that is, each 1.8 degree motor step rotates the Subreflector by 1.8/108 or 0.01666 degrees so that 21,600 motor steps are required to rotate the Subreflector 360 degrees. The Focus gear train reduction ratio to the lead screws is 2.54:1. The lead screw pitch is .200 so that five rotations of the lead screws are required to move the traveling platform one inch. The total Focus travel is 12 inches (ignoring that lost by limit switch inhibit action) so that the total number of motor steps required to traverse this Focus range is: 1.8 * 200 * 5 * 2.54 * 12 = 30480 motor steps.

Focus and Rotation positions are read out as 14 bit values (16384 counts range). The motor-step/readout-resolution ratios are: 21600/16384 = 1.318 steps/bit (also 1.318 arc-min/bit) in Rotation motion and 30480/16384 = 1.860 steps/bit (also 0.0003937 in/step and 0.000732 in/bit) in Focus motion.

Rotation position is read out by a synchro mounted on a tripod above the

barrel. The synchro shaft is coupled to the center of the drum through a sliding "Trombone" which takes out the Focus motion of the barrel; see Figure 5 for details on this mechanism. A tubular shaft attached to the top of the Trombone drives the Rotation position synchro through a flexible coupling and pick-off gear (1:1 ratio) which drives an anti-backlash gear on the synchro shaft.

Focus position is read out by a 10:1 anti-backlash reduction gear box and synchro coupled to the Focus gear train. The gear box is used because the synchro and gear box mimic the 10-turn helipot used with the older system.

Focus upper/lower limit switches sense the extremes of Focus motion and cause the F/R Controller to inhibit further drive into the limit. There are no Rotation limit switches as the Rotation drive is capable of continuous rotation; in executing a Rotation command, the F/R Controller rotates the Subreflector through the smallest angle to move to a new position. This permits faster band changes.

The 327 MHz feed dipoles travel up and down with the Subreflector Focus motion but do not rotate with the Subreflector Rotation motion. This non-rotation is accomplished by mounting the dipoles on a square shaft which is prevented from rotating by a square-holed collar attached to the top of the Rotation synchro gear box. The dipoles are caused to move with the Subreflector in Focus motion by a thrust bearing in the Subreflector which is attached to the square shaft. The square shaft passes through the Trombone, the Rotation synchro drive shaft and slides through the square-holed collar in Focus motion. Coaxial cables carry the RF signals from the feed and are routed through the square shaft. Since this square shaft penetrates the Rotation readout box, a seal ring under the square-holed collar prevents water entry. Details of this mechanism are depicted in Figure 4.

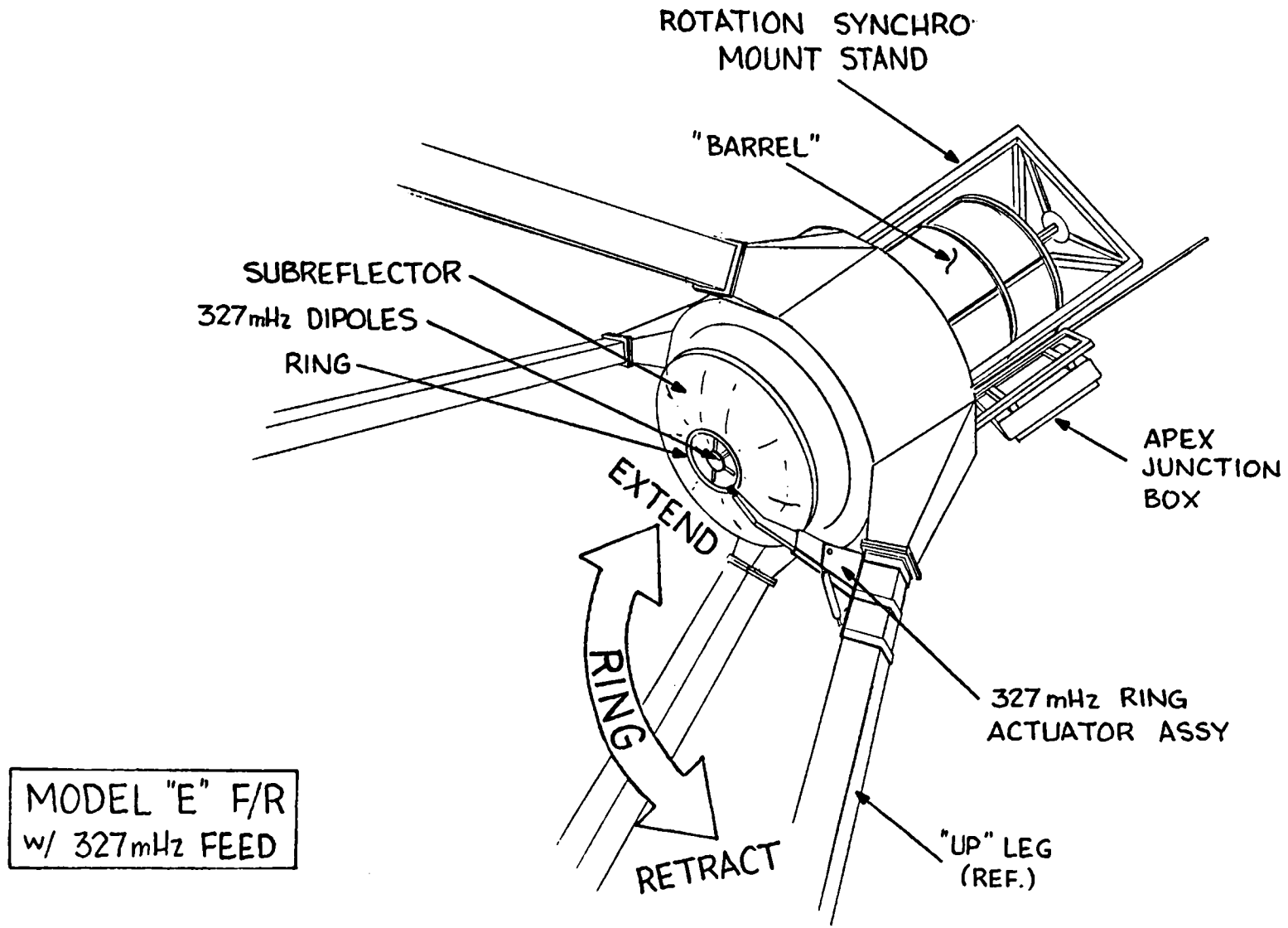


FIG. 4 - APEX F/R COMPONENTS

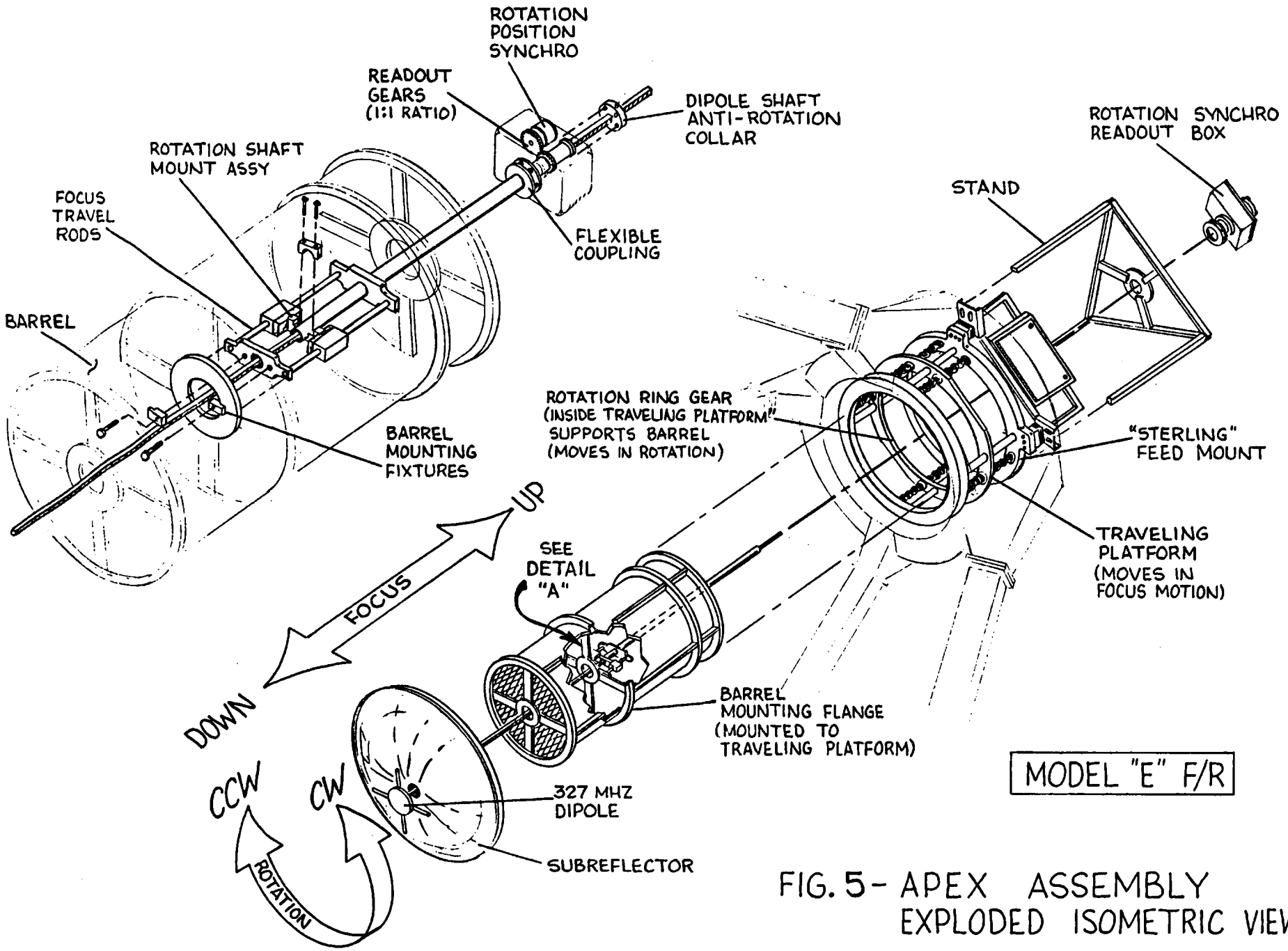


FIG. 5 - APEX ASSEMBLY
EXPLODED ISOMETRIC VIEW

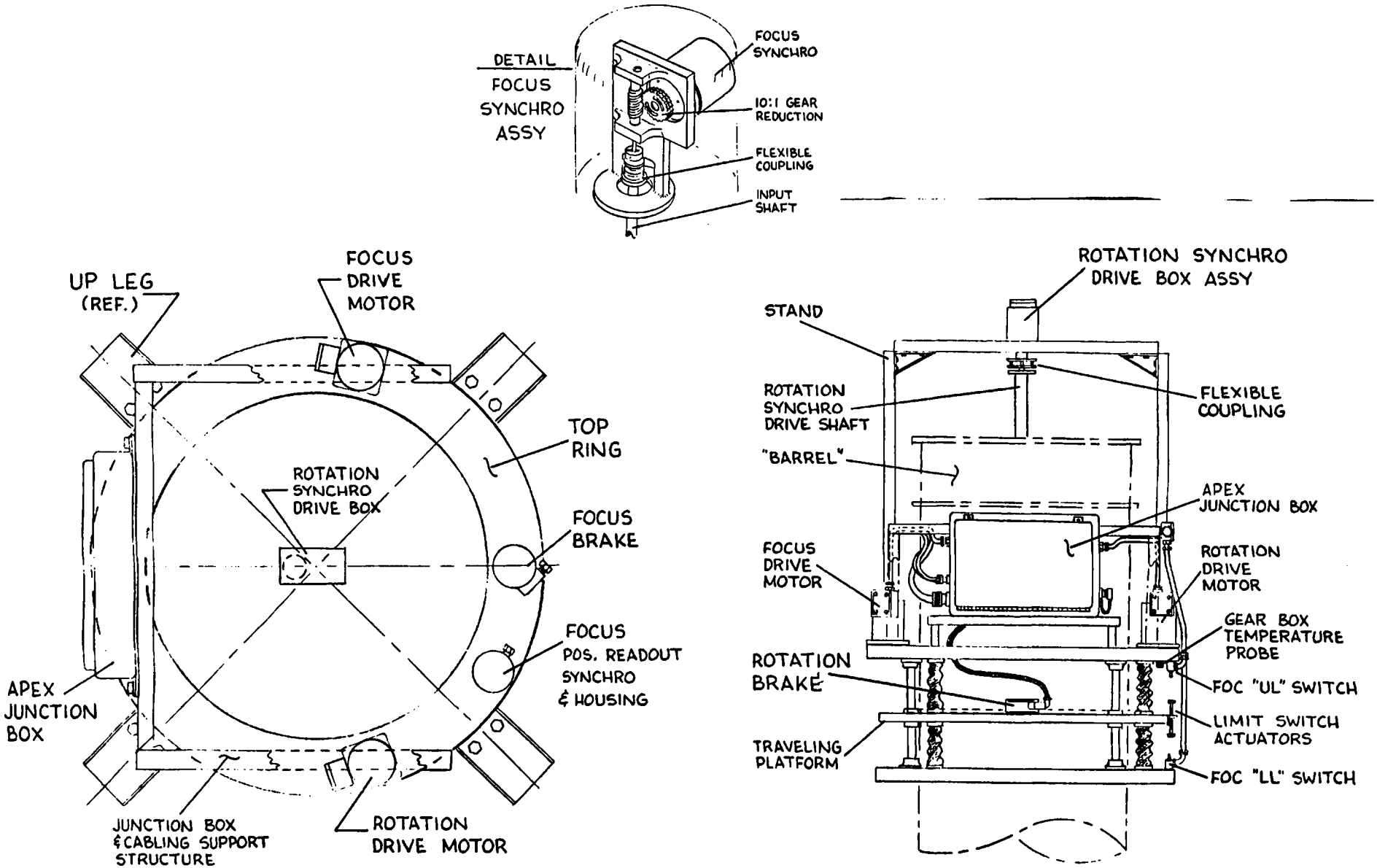


FIG. 6 - F/R MOUNT - LOCATIONS OF MAJOR COMPONENTS

1.5 DRIVE DYNAMICS

The purpose of all this mechanical and electronic hardware is to position the Subreflector; the control system design must deal with the dynamics of the drives which involve large work, inertial and frictional loads. This section describes aspects of these dynamics which are important to electronics maintenance personnel because the considerations outlined below determined the characteristics of the control programs. These considerations were the result of analysis by the writers and many years of experience with the F/R Mount.

The drive motors are stepper motors which are high torque, low shaft speed devices (compared to conventional DC or AC motors) which are frequently used to implement drive systems with minimal or no gear trains. The motors are caused to rotate by time-sequencing the four motor winding currents with high power transistor switches. The center-tapped motor windings are connected to the power supply; the switches sink these currents to ground in accordance to a sequence of states which determine the direction of rotation. Each state change is called a "step" which causes the shaft to rotate by a discrete angular increment (1.8 degrees in these motors). The motors are driven by an electronic package called a Translator which contains a set of four transistor switches, associated logic and power supplies. The Translator switches state changes are caused by applying a drive pulse to either of two inputs which cause the motor to rotate in the cw or ccw direction by one angular increment for each drive pulse.

An important characteristic of these motors is torque breakage which occurs when the imposed load exceeds the motor torque producing capabilities (particularly pronounced at higher speeds). These motors have two torque/speed curves which fall off with increasing speed; the lower curve is the maximum motor load (at a given speed) at which the motor will always start from a dead stop and the upper curve is the maximum load which the motor can drive if it is started at zero or low speed and gently ramped up in stepping rate. When torque breakage occurs, the motor stops and the only way to get it to drive again is to either reduce the load or reduce the stepping speed to a rate where the motor can resume stepping. Torque breakage does not gradually increase with the load; it is a threshold-like effect in which a slight increase in load at the critical torque causes the motor to intermittently fail to respond to translator drive signals. In this narrow torque-speed region the motor shaft motion is very erratic and jerky; another slight increase in load torque results in abrupt stoppage of the motor.

Figure 7 shows the HS1500 (Ant 1 - 20) & FD309 (Ant 21 - 28) Torque/Speed curves. These curves are the upper, (start at a low stepping rate & gently accelerate) curves and are based upon bench torque tests and Superior Electric data. The lower curve has not been determined for these motors because of the difficulty of making these measurements with the primitive equipment on site, but; it has been observed that the motors will not start in the F/R Mount if the initial drive rate is above 300 Hz.

This torque breakage phenomena has happened to the VLA F/R System many times due to unusually heavy loads (such as cold weather viscous friction drag) with the result that the drive is "stuck" and can only be (maybe) moved by repeated commands to move back and forth in a small region. Ice loading of the Subreflector and barrel can also cause sticking. One of the shortcomings of the old F/R Controller design is that it does not contain provisions to deal with the problem other than to abort the command after a time-out. Drive rates

in the old controller have been set to values which (usually) work in the worst case drive situation - winter.

Does torque breakage harm the translators? Yes; repeated attempts to move a stuck drive can cause driver board failure although Superior Electric (the manufacturer) says that it shouldn't happen. A stuck drive motor does not generate a back EMF so the driver boards must sink a great deal more current during the switching transient time.

The torque developed by these motors is very sensitive to the line resistance between the motors and translators; if the motors are connected directly to the translators they develop about 20% more torque than is shown on these curves. The cable resistance is about 1 ohm for the 125 foot run of #10 cable; it would take a lot of copper to significantly reduce the line resistance.

A second important property of these motors is motor resonance: literally a mechanical resonance in which the magnetic field acts as a torsional spring and the rotor moment of inertia acts as the mass. At the motor resonant frequency, the torque delivered by the motor is greatly reduced and the rotor vibrates (in shaft angle) at each step; the amplitude of the oscillation and decay are dependent upon damping resistors in the Translators. In the antenna 1 - 20 motors the resonance occurs at about 550 Hz and the available motor torque is reduced to about 450 oz-in, - about one-third of the available torque at 500 & 600 Hz. The Ant 21 - 28 motors and translators are a newer design with no pronounced resonances (at least we have not noticed any resonances in bench torque tests).

A third important property of these motors is the large holding torque which they exhibit when stopped with a steady state current in the windings. This condition exists with the older version of the F/R control system.

The primary task of the controller is to get the drives into motion and to gently ramp the motors up to the maximum speed so as to quickly get to the commanded set point. Near the set point the drives are to be quickly ramped down and driven to the set point at low speed; attempting to stop at the set point at high speed results in an overshoot of several tens of steps because of mount inertia. Because of the large work and cold weather vicous friction loads, the drive acceleration profiles have been made very gentle so that the inertial loads are never more than about 10% of the available motor torque.

Ideallly one would like to start the drives at a very low initial rate, - say a few Hz, and proceed up from there. However; drive motion has been constrained to start at 100 Hz. Experience has shown that operating the drive trains at rates much lower than 100Hz causes excessive gear train rattle. Gear train rattle is a mechanical oscillation caused by the stepping motion of the motor shaft; the intermittent motion causes multiple impacts of the gear teeth which reduces their life. The low mechanical resonant frequency of the drives aggravate this effect; the resonant frequency is about 6 to 8 Hz and is determined by the spring rate of the rubber coupling (low) and the composite moment of inertia of the gears and drive.

The speed ramp-up profile is a sequence of 50 Hz step increases in stepping rate, starting at 100 HZ and going up to a maximum of 1000 Hz in Rotation and 500 Hz in Focus. The duration of these steps is 100 pulses so

the drive acceleration increases with each step. The ramp-down profile is a sequence of 50 Hz steps to the convergence speed of 100 Hz with a step duration of 48 pulses; it is easier to decelerate than accelerate the drives.

The rubber spring coupling between the motor and drive plays a vital role; without it the motors would be unable to drive the heavy work and inertial loads. Stepper motor manufacturers recommend that the load inertia be less than three times the motor inertia for motors which are rigidly coupled to the drive; this ratio is 4:1 in the Rotation drive. The spring buffers the motor; it is deflected in proportion to the drive load. Consider the following: ---- for simplicity assume that the Rotation drive is only an inertial load; in accelerating the drive the motor sees the rotor moment of inertia and the drive moment of inertia on the other end of the spring. What happens when the motor speed is increased? The motor shaft follows the stepping rate change but the drive end of the spring lags behind the motor because the spring must first deflect (ie wind up) to apply torque accelerate the drive. The amount of wind-up depends upon the acceleration to be imparted to the drive. Because of the large moment of inertia of the drive, the drive position will lag behind the motor position as a function of the amount of motor acceleration, coupling spring rate and drive moment of inertia. If the speed change is a step change, the drive will eventually accelerate to the motor speed and unwind the spring to a zero deflection. When this happens the motor and drive will continue at the new motor speed with the spring undeflected (ie unwound). If the speed change is a constant acceleration, the spring winds up to a constant deflection and the drive position lags a constant amount behind the motor position as a function of the spring torque constant. To summarize: there is a transient deflection of the spring coupling which depends upon the nature of the acceleration (ie step, ramp etc), the moment of inertia of the drive and the spring constant. The result of this wind-up is that the drive position lags behind the motor position.

In the real world situation, the spring deflection is the sum of the transient deflection (described above) and the work (lifting), viscous and coulomb friction wind-ups.

When the stepping speed is changed, the motor rotor moment of inertia absorbs a portion of the motor torque; that is, not all of the torque shown on the curve above is available at the motor shaft. In the case of the Rotation drive the motor inertia is 0.055 oz-in-sec**2 and the drive inertia is 1.941 oz-in-sec**2, a ratio of about 4:1. Thus during acceleration, only 80% of the Rotation motor torque which goes into acceleration is available for drive acceleration. After the acceleration torque requirements are met, the remaining torque is available for the work, viscous and coulomb friction loads. This is the reason why the ramp-up profile has been made so gentle.

For a step change in stepping rate the transient wind-up torque is approximatly given by: Ttr = Twu*exp(-(Kv + Kc)*time/Id) where Twu is the spring wind-up torque, Id is the drive moment of inertia, and Kv and Kc are viscous and coulomb friction factors. This is similar to the voltage developed across an inductance in an RL circuit for a step voltage input. For the ramp up sequence of this new F/R Controller, the worst case transient torque occurs at the initial step to 100 Hz and is about 175 oz-in. The 50 Hz step transient torque is half this value. The transient decay time depends upon (mostly) viscous friction which varies with temperature; this has not been measured or calculated because of practical difficulties. The 100 pulse

period of each step is more than adequate for this decay. These figures are based upon a difference equation model of the F/R Mount.

The spring torque constant is 103.7 oz-in/step. At the peak motor torque (1500 oz-in @ 250 Hz, Ant 1 - 20) the coupling could wind up to as many as 14 motor steps before motor torque breakage. Thus the Focus and Rotation motors could be ahead of the drive as much as 19 arc - min in Rotation and 0.006 inches in Focus. Why is it important to consider the wind-up? At the completion of a command, the brake is engaged and the translator power is turned off; this allows the spring wind-up to release. A second reason is that at the start of a command execution, there is a lag in drive motion because of spring wind-up. One of the shortcomings of the older controller is that the wind-up is not released (because of the large motor holding torque) and remains as a steady-state torque between the motor and brake. The magnitude of this wind-up is the sum of all the drive loads at the time that the brake is engaged. If there is a large wind-up, it may gradually relax due to antenna vibration-induced brake slippage, - with consequent drive position shifts.

The actual load on the motor (and spring) is the sum of the work, inertial, viscous friction and coulomb friction so the total spring deflection is determined by this sum.

Viscous friction is proportional to velocity; the higher the drive rate the greater the viscous friction. Viscous friction is also an inverse logarithmic function of temperature: $Kv = K1+(K2/lnT)$. This temperature dependence causes great changes in the F/R Mount viscous friction. With a hydrocarbon-based grease, over the +100 to -20 deg F temperature range, Kv can be expected to change by a factor of about 650. An unobtrusive Kv load at summer temperatures becomes a huge load at freezing temperatures; at about +30 deg F, it's a toss-up as to whether the Focus drives will stick. This temperature sensitivity is the reason that the renovated F/R Mounts have heaters to warm the Focus and Rotation drive gears. Prior to the use of heaters, the Focus positions were made identical for all bands in antennas in which the Focus drive had a strong tendency to stick in cold weather; as a result, for these Antennas, Focus is never driven in the winter. The heater controller puts about 600 watts into the drives when the ambient temperature is below about 45 deg F. A temperature sensor on the bottom of the gear box monitors the temperature which is typically about 5 to 10 deg C above ambient when the heaters are in operation. Kv could be modeled for these drives but would be difficult because of the many complicated lubricant shearing surfaces. The actual viscous friction drag is not known for these drives because of the practical difficulties of instrumenting the requisite torque measurements. These measurements would have to be performed over a wide range of speeds and temperatures.

The choice of a F/R Mount lubricant is something of a dilemma: the gearboxes are not sealed, so that a lubricant which has a lower viscosity in the winter will leak out of the gearbox holes in the spring; this leaves the drives without lubricant. On the other hand a lubricant stiff enough to stay in place in the summer has too much viscous drag in the winter. It is impossible the change the lubricant without a dis-assembly of the F/R Mount.

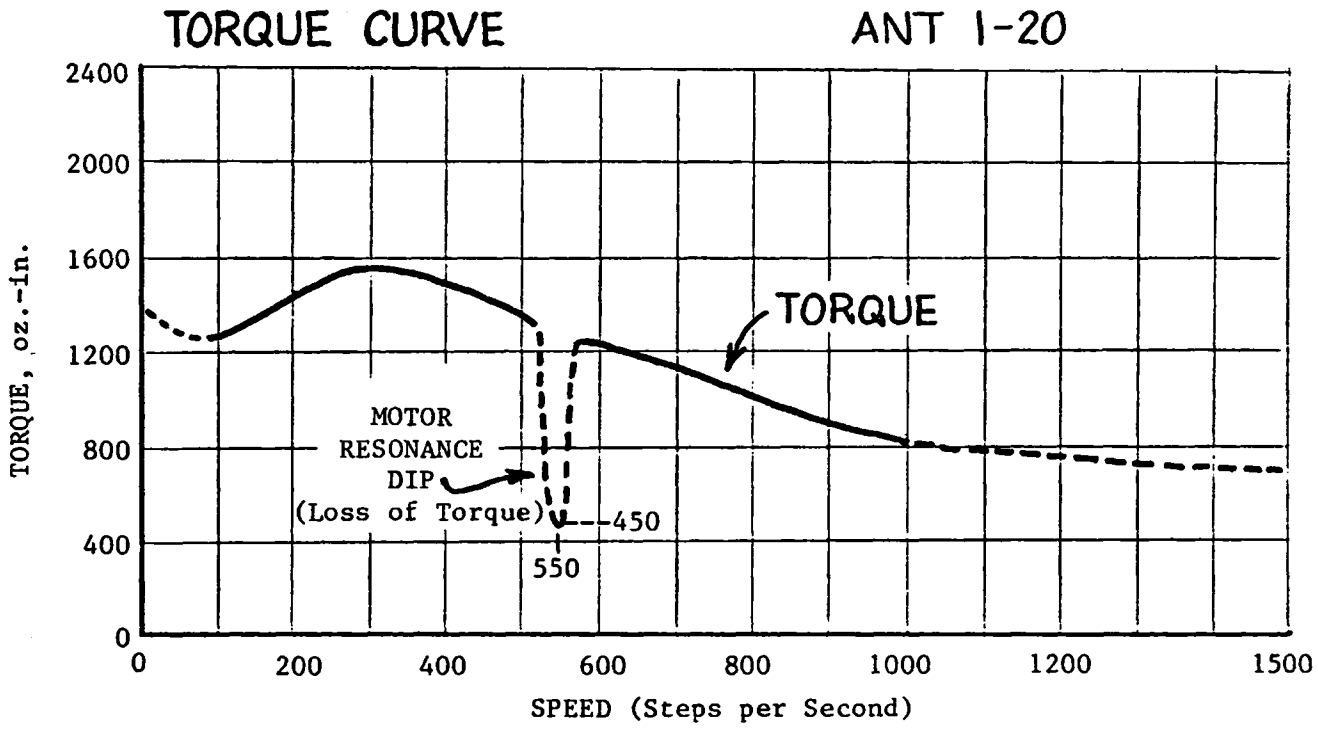
Coulomb (rubbing) friction depends upon the force pressing the surfaces together, the roughness of the surfaces and a friction factor

dependent upon properties of the two materials. Coulomb friction of the drives has been observed (by the writer) to be about 25 oz-in at the motor shaft inputs to the drives; the barrel & subreflector were not installed during these measurements so the actual values would have been higher because of the additional ~ 300 pound load.

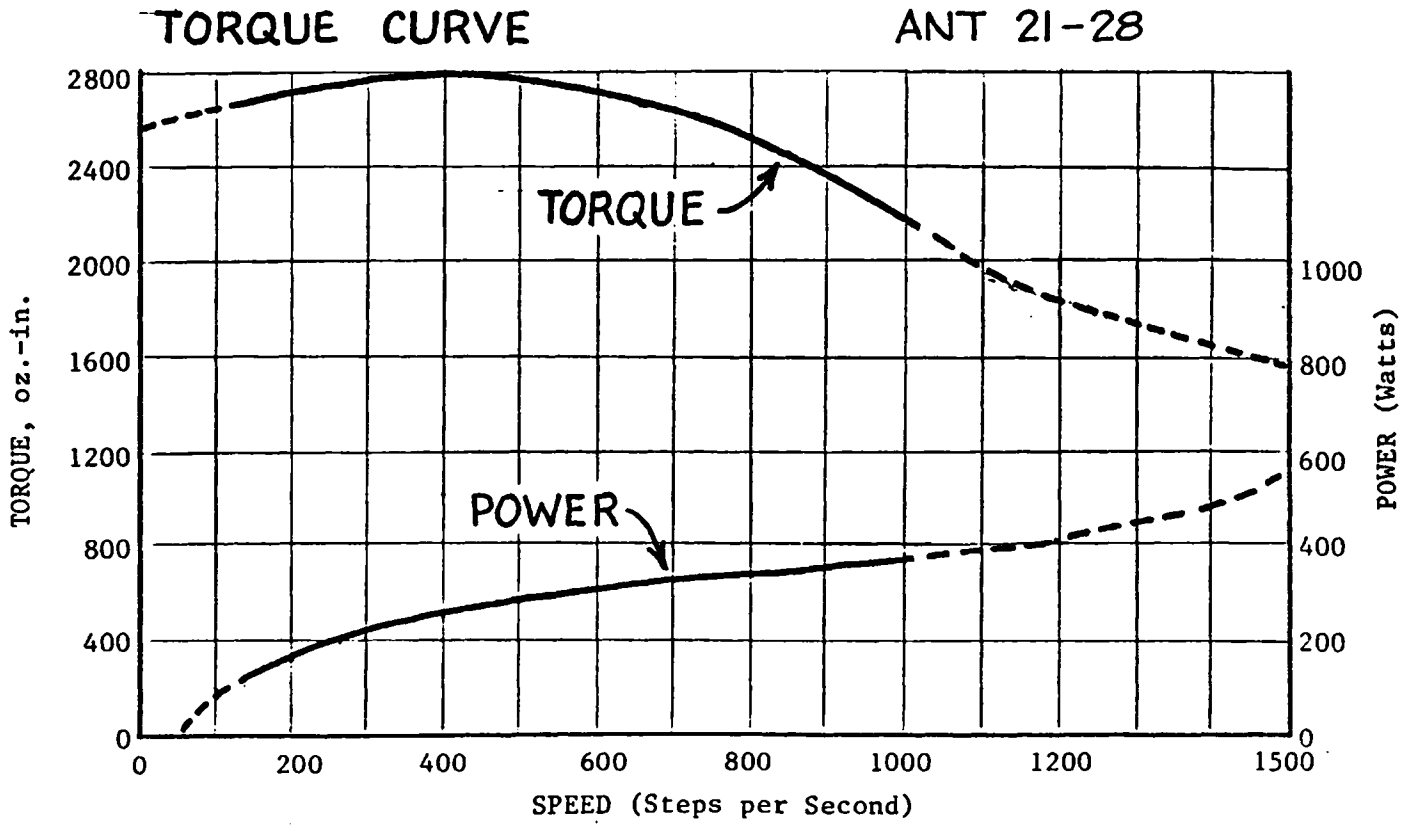
Although the dynamics of the Focus and Rotation drives are very similar, the load parameters are quite different: Rotation has a small work load (about 100 oz-in of subreflector unbalance at the motor shaft) whereas Focus has a huge (drive up) work load (about 600 lb) consisting of the heavy moving platform, the drum, subreflector and 327 MHz feed hardware. Viscous friction is more of a problem in Focus because the Focus ring gear (where most of the viscous friction occurs) is only a gear ratio of 1:2.54 down from the motor in comparison to the Rotation ring gear which is down 1:8 from the motor. The ring gears and race clearances are of similar size so the viscous frictions (at the gears) are similar. Winter experience shows that the Focus drive is much more vulnerable to cold weather sticking than Rotation. Both drives have roughly comparable inertial loads. In summary, the Focus is in general much more heavily loaded than Rotation; for this reason the maximum drive speed for Focus has been restricted to 500 Hz to avoid the bad torque dip at 550 Hz.

The new controller utilizes a motion analysis algorithm which detects torque breakage and causes the drive rates to be reduced to 100 Hz and then ramped back up to 250 Hz, the peak torque for these motors. If the torque breaks again , the drive is shut down. This motion analysis is a very powerful feature as the Rotation drive can be ramped to 1000 Hz (versus 400 Hz in the old controller) for fast response to band changes and the relialability of the system under adverse conditions is greatly improved because the motion analysis fallback drive insures that the controller will re-attempt drive at the speed which produces the maximum motor torque. The failure rate of the Translators should decrease since the driver transistors do not have to attempt to drive stuck mechanisms.

Finally, in conclusion it should be pointed out that the torque requirements of the F/R Mount have never been fully characterized, either by mathematical modeling or by actual measurements. This should be done for the full range of operating temperature and drive speed. Some calculations have been done on simple aspects such as the work and inertial loads but the extremely variable viscous friction and coulomb frictional loads are unknown.



HTR 1500/1008/HS1500 TORQUE vs. SPEED CHARACTERISTICS



TM600/M172-FD306 TORQUE vs. SPEED CHARACTERISTICS

FIG. 7 - TORQUE/SPEED CURVES

2.0 M7 MODEL E, F/R CONTROLLER DESCRIPTION

This section describes the F/R Controller digital logic and the control programs. The control programs are the control logic of the system; the digital logic of the controller is the vehicle which is manipulated by the programs to implement the control functions.

2.1 F/R CONTROLLER LOGIC DESCRIPTION

During the following discussion the reader should refer to the M7 logic schematics which follow this section. The reader is also referred to the data sheets in the Appendix which describe the 8085 microprocessor, support chips and instruction set; this background is vital to understanding the operation of the controller.

The F/R Controller has been implemented with two independent microprocessors (one for each axix) consisting of an 8085A microprocessor, an 8156A RAM/I/O port/Timer, two 8755A EPROM/I/O ports, address decode logic and two 2716 EPROMs for program expansion and antenna peculiar-control argument memory. The configuration of the processor(sheets 1,2 & 5,6), RAM and EPROMs is conventional and similar to that depicted in INTEL microprocessor data books to which the reader is referred for details on timing, memory and I/O read/write and instruction usage. Because the multiplexed ADDRESS/DATA BUS accesses many registers it is buffered by 74LS245 tri-state, bi-directional drivers. Both processors have identical architectures and are almost independent except for the power reset logic (sheet 10) and the 5 MHz processor clock which are common. Address decode logic (sheets 2&6) provide address enables for the RAM, EPROMs and serial Input/Output Registers. These decodes are also used as strobes to reset interrupt request flip-flops, single step drive motors and initiate data input from the Apex Interface.

The Timer logic in the RAM can be driven by any (or none) of 10 KHz, 1 KHz or 100 Hz clocks as selected by the RAM Port C and a 74LS153. The 0 - 2K EPROM I/O ports are configured to operate as output ports to output control discretes (eg Foc trans power cmd, etc) and clock control states to control the motor stepping rates. The 2 - 4K EPROM I/O ports are configured to operate as an input ports: PORT A reads response discrete states and PORT B reads manual control discretes.

74LS373 latches are clocked by ALE to store the 8 bit lsb of the address for the 2716 EPROMs.

The Data Set interface logic is shown on sheet 9; the reader is referred to the Data Set Manual for details on the serial operations of loading a command from or reading data to a Data Set. In operation, a command is serially loaded into a 24 bit command input shift register by CLKO shift pulses, the processor is then interrupted by the command strobe STRO which then enters the RST 7.5 interrupt routine to read the SMA address, command and data flags, and command argument by a series of byte reads from the command and SMA registers via the tri-state ADDRESS/DATA BUS. The four Data Set SMA bits are trapped and stored in a 74LS174 latch by the command or data strobes. The SMA bits are decoded by the program to identify the command address. The command strobes and clocks are qualified by the SMA 3 ("8") bit so that addresses 320 - 327 (octal) activate the Focus processor and the addresses 330 - 337 activate the Rotation processor.

Monitor Data readout is address qualified and output in a similar manner; the Data Set STRI pulse interrupts the addressed (ie Foc or Rot) processor which enters the RST 7.5 interrupt routine to read the SMA bits and command and data flags to identify the specific data being requested and outputs the requested data by a sequence of three byte writes via the tri-state ADDRESS/DATA BUS to the data output registers. The Data Set then emits CLKI pulses to serially read the Monitor Data. The data output operation is the only time-constrained processor operation; the code must respond to the interrupt and output the requested data within 100 microseconds before the Data Set CLKI pulses unload the data. The SMA-3 bit qualifies the data readout logic in that mux addresses 220 - 227 activate the Focus processor and mux addresses 230 - 237 activate the Rotation processor.

An 8 channel, single-ended analog multiplexer selects power supply, translator power, bin temperature and the synchro excitation current for A/D conversion by the Data Set.

Data is serially input from the Apex Interface when the controller outputs a DATA REQUEST strobe pulse (address 38H) to the Apex Interface which activates the readout logic to cause a serial train of 6 bytes of data to be loaded into the Apex Focus and Rotation Data Registers, (sheets 3&7) by clocks provided by the Apex Interface. The data and clocks are isolated from the Apex Interface by optical isolators for lightning glitch protection. The registers are cleared during the initial stages of the data requesting operation by outputting zeros on the ADDRESS/DATA BUS which are then parallel-loaded by the 38H strobe which sets the C1 & C2 bits to the parallel load mode. The processor then reads the Apex Interface data by a sequence of 6 byte read operations via the ADDRESS/DATA BUS.

A time base (sheet 10) provides processor and system clocks and a 5MHz clock for the Data Set. Processor Reset logic on this sheet causes the 8085 reset line to be activated to re-initialize the processor. The 9602 one-shot is fired as a result of a SYSTEM RESET command, (Mux 337, octal), actuation of the COMPUTER/LOCAL switch, a power reset circuit or processor halt resets generated by a decode of the S0 & S1 8085 processor states. The latter logic is a protective measure that senses that the processor is halted (perhaps through power glitches) to trigger the processor back into operation. During the year that Ant 27 had an experimental controller (without this S0/S1 logic) there were two occasions where power glitches halted the controller.

A YOWP! input from the Apex Interface and connector interlock signals develop a DRIVE ENABLE term to halt drive when something bad is sensed by the Apex Interface or a cable is disconnecated.

Processor-to-processor communication is provided by four DM8551 tri-state latches which are loaded by one processor's ADDRESS/DATA BUS and readable by the other processor's ADDRESS/DATA BUS. This feature is not presently used.

The M7 module temperature is sensed by an LM3911 and op-amp circuit and read out as Bin Temperature. The scaling is 100 mv/deg C.

Sheets 4 & 8 contain the control interface logic to provide drive pulses to the Translators and turn on solid state relays (in the M22 Switching Module) to apply AC power to Translators, brakes and Ring actuator. The DRIVE ENABLE term (mentioned above) inhibits all outputs in the event that the Apex

Interface sends over a YOWP! signal. Inhibit logic on the Ring EXTEND and Ring RETRACT lines sense the concurrent presence of these commands and inhibit the SSR drive when both are active.

The stepper motor clock rate is generated by two decade counters on sheets 4 & 8. Clock rate control terms from the 0 - 2K EPROMs determine the counter radix. The minimum stepping rate is 100 Hz and maximum is 1000 Hz with many intermediate rates selectable via program control. A divide by 4 counter driven by the stepper clock causes interrupt RST 6.5 to be set to enable the program to analyze drive motion. The RST 6.5 request flip flop is reset by a 3BH strobe.

One-shot activity sensors on the Translator drive pulse outputs (sheets 4 & 8) drive LEDs on the M8 panel to provide a monitor output and visual indication of the translator drive and polarity.

Limit switch inputs (sheets 4 & 8) provide direct inhibits to the UP/DOWN and CW/CCW Translator drive outputs.

A voltage clamping network on Dip Header A3 limits the 15 volt swing of the Translator drive pulses to a TTL high when the M7 is used in antennas 21 - 28 which use a newer version of Translator that requires TTL drive levels. When the controller is used in Antennas 1 - 20 this Dip Header should be removed.

A strobed one-shot generates a single stepper drive pulse for use in single-stepping the motors during convergence.

The Translator power is monitored by a divider circuit which reduces the voltage to a TTL level for monitoring by an EPROM I/O port bit. The M8 Translator LED displays are also driven by this circuit.

Front panel test points on the DB25 connector enable observation of important clock and control discretes. These signals and test points are:

Signal	Test Point	Signal	Test Point
Logic Common	1		
Apex Foc Data	2	Apex Rot Data	14
Apex Foc Load Clock	3	Apex Rot Load Clock	15
Foc SSR Brake Drive	4	Rot SSR Brake Drive	16
Foc SSR Transl Drive	5	Rot SSR Transl Drive	17
Foc Drive UP	6	Rot Drive CW	18
Foc Drive DOWN	7	Rot Drive CCW	19
Foc RST 6.5	8	Rot RST 6.5	20
Foc Data	9	Rot Data	21
spare	10	Ring EXTEND SSR Drive	22
spare	11	Ring RETRACT SSR Drive	23
Analog Data To Data Set	12	spare	24
5 MHz Clock	13	Drive Enable	25

2.2 ROTATION AND RING CONTROL PROGRAM DESCRIPTION

INTRODUCTION

The following discussion assumes that the reader is familiar with 8085 assembly language; this is vital to understanding the program operations. The programs are straightforward, well commented and easy to follow but also require an understanding of the control task, F/R Mount mechanism, control system hardware and Data Set interactions. The preceding sections of this manual provide descriptions of these items.

The Focus and Rotation control programs are very similar and differ in only a few (but important) respects such as the fact that the Rotation drive can rotate continuously, therefore the Rotation program drives in either direction to null the error; the Focus drive cannot do so. Other differences are: Focus command limit tests, Ring commands (handled by the Rotation controller) and the maximum drive speeds, but; the number of similarities far outnumber the differences. Since these programs are so similar, the Rotation program is described since it is more complicated; this is followed by a description of aspects peculiar to the Focus program. Program listings are included in the Appendix. Memory and I/O Port maps follow this discussion.

The description is not instruction-by-instruction but rather a commentary outline of the logic of control flow and description of the hardware/software interactions. The reader should carefully study the associated portions of the programs during the commentary.

To minimize repititious in-line code, subroutines are used to perform functions that are used more than once: examples are device drivers to control the Translators, brakes, etc or to perform arithmetic comparisons of two 14 bit values.

There are two ways that the F/R Mount can be driven: COMPUTER mode (ie the central control computers via the Data Set) and LOCAL via the switches on the M8 panel. The section labeled LOCAL DRIVE HANDLER inputs and processes manual commands from these switches. This code and the COMPUTER mode code invoke the same subroutines and device drivers because of the similarities of the functions to be performed. The COMPUTER mode portion of the program will be discussed first followed by a discussion of the LOCAL mode.

There are 4 commands that are recognized and executed by the F/R Controller: POSITION, RESET, NAP AND RING. The RESET command terminates the execution of POSITION, NAP and RING commands. The NAP command inhibits execution of POSITION and RING commands. The asynchronous execution of these commands is interrupted by the higher priority 39.2 Hz monitor data requests from the Data Set.

The program has been organized into logical chunks which are delimited by asterisks. As you scan the listing you will see the following sequence of chunks: RESET & INTERRUPT, INIATIALIZATION, SYSTEM HANDLING, COMMAND POSITION HANDLER, LOCAL DRIVE HANDLER, CHECK RING STATUS, RAMP UP & DOWN, TRANSLATOR & BRAKE CONTROL, ERROR HANDLING ROUTINES, SUBROUTINES, APEX & CONTROLLER DATA GATHERING ROUTINES, INTERRUPT ROUTINES AND ANALOG AND RAMP TABLES. These titles indicate the functions performed by the associated code.

You will note that the listings start with a series of EQUATES to assign mnemonic names to the otherwise obscure numbers such as addresses and I/O Port control codes.

The DATA SET TABLE is a set of Ram locations which are used to store formatted data to be output to the Data Set Data Register in sets of three bytes/data word. Section 10 details the data and command formats. The format description is keyed to the table location by labels such as POSD which is the drive position. An important point is that the central computer outputs commands as 2's complement values while the processor operates on straight binary integer arithmetic. As a consequence, the processor must complement bit 13 (msb) of the command in order to use it in arithmetic operations. Correspondingly, monitor data values output to the Data Set must be transformed to 2's complement format from the integer format by complementing bit 13.

The states of all control discretes and the responses to these discretes are read out in the monitor data; this provides good visibility of the behavior of the F/R System.

The VALUES & ARGUMENTS tables are RAM locations in which program parameters are stored during program operation.

The FLAG table are RAM locations in which program status flags are stored during program operation.

INITIALIZATION --- The initialization code (INIT) is actuated by the processor RESET line as the result of a power reset or by a RESET command. In INIT the I/O port directions are set up, all control discrete outputs are cleared and the RAM tables are cleared.

INTERRUPT VECTORS -- The RESET & INTERRUPT code provides interrupt vectors to interrupt service code. TRAP interrupt has the highest priority, cannot be disabled and is used with the 8156 Timer logic function. RST 6.5 is used in motion analysis to signal that four drive pulses have been output and that it is time for the program to test the motion. RST 7.5 is used to signal that the Data Set has a new command or wants monitor data. RST 5.5 and INT interrupts are not used. When an interrupt has been sensed the Interrupt system is disabled by a DI (disable interrupts) instruction and the processor jumps to the appropriate interrupt-handling code.

SYSTEM CONTROL

BOSS is the control portion of the code which manages all tasks and is in continuous looping execution. BOSS begins by calling for fresh data from the Apex Interface (via DSTOR), tests for a branch to the LOCAL mode, tests the command status to see if service is required for: RESCMD (an active RESET command); CHKDRV (an active POSITION command); CHKRNG (an active RING command); NAPATV (an active NAP command); tests requests for POSITION, RESET and NAP command modes to be established and if so sets them active. Next, BOSS tests (via APAOK) an Apex Interface analog value against high and low limits on each pass-through (a fault flag bit is set in the output data area if out of limit results), clears the flag if the fault goes away and finally returns to repeat the scan. In these tests the ORA A instruction is used to set the flags for the following jump instruction.

In testing the Apex analogs (in APAOK), a 16 bit comparison routine (RANGER) is called in which the 16 bit contents of registers DE are subtracted from the 16 bit contents of HL with the resultant difference in HL and the arithmetic sign of the diference in C, (0 = +). A table of high and low limits (ANATAB), and 8 Apex analog data values (APATAB) are accesed by an address index (APAPTR, 0 - 7). In the lower limit test, the lower limit is placed in DE and the analog value is loaded into HL for the RANGER comparison. In the upper limit test the analog data is placed in DE and the high limit is placed in HL for the RANGER comparison. The results of these comparisons either set or clear an Apex Interface fault bit in the FLTSFT code.

In executing a RESET command the timer is stopped (via TSTOP) and the drives are ramped to a stop via DRVSTOP.

COMPUTER COMMAND EXECUTION

CHKDRV -- CHKDRV manages the motion of the drives in CMP (central computer mode). At the start of CHKDRV, the mechanism is moving, executing a position command; the DRVREQ flag is tested to see if a new, over-riding POSITION command has been received, if so, the new command argument (in CMDTMP) is compared with the current active command (in ACTVCMD) to see if the new position is different than the command in process. This comparison is done by loading the new argument in DE and the current argument in HL and calling VECTOR which will return with the absolute value of the difference in HL. CLOSE is called next to see if the position difference is less than 4 counts. If so, the command request (CMDREQ) is cleared by CLRREQ and the program falls into DRVTST.

If the difference is greater than 3 counts, the drives are first slowed to a stop by calling DRVSTP, the timer is reset via TSTOP and the program falls into DRVINT which determines the drive direction, acceleration parameters, initializes the motion counter, makes the temporary command the active command etc. If the new commanded position differs by less than 4 counts (via CLOSE) from the present position, the new command is ignored and control reverts to BOSS. DSTOR is called which sets the correct direction to drive to null the error in DIR, the direction flag.

DRVIN1 is the entry point for the get-it-there-somehow code; control has been transferred to this point from ERDRV which has determined that over a 100 pulse period the realized drive motion is not consistent with what it should be and the controller is being conditioned to attempt drive at the peak torque drive rate. This entry point provides an orderly restart of drive motion with the constraint that the maximum drive rate is 250 Hz; the peak torque speed for the Ant 1-20 motors. EDRV has set a flag (GETIT) which is tested in determining the maximum drive rate step number. If GETIT is true, the maximum step number is 5 which is set in B. If GETIT is false, B is set to 18 (17 + 1 steps).

The number of velocity steps to execute is calculated by DIV, (the max is 17 steps if there is a long way to go) and stored in RMPTO. The DIV algorithm is that -114 (decimal) is set in DE, the absolute value of the position error is set in HL, FFH (or minus 1)is set in A. Minus 114 is sucessively added to HL (the error) and A is incremented until the carry flag is no longer set. If this happens, A contains the number of ramp-up steps to accelerate the drive through. Next, B is compared with A, if A is greater than or equal to B (either a large distance to travel or B has been set to 5, the result of a

motion analysis fault), A will be set to B-1. If A is less than B, A is left unchanged and control is transferred to AOK.

AOK saves the step count in RAMPTO. If A=0, the distance to travel is small and control is transferred to NORMP without setting the ACCEL flag true. This causes the drive rate to be 100 Hz (only) and bypasses the call to RAMPUP. If A is greater than 0, the distance to be traversed is large, the ACCEL and RMPUP flags are set and control falls into NORMP.

NORMP initializes the stepping rate clock to produce 100 Hz, the translator and brake power turn-on subroutines are called, the convergence flag (CONVRG) is cleared, the direction flag (DIR) is tested to determine the direction to drive, (if DIR = 1, drive CCW) and the program falls into MOVIT. The time-out error handling address is loaded into the TRAP location for use by BLAP, the timer is set to 15 seconds via a call to TIMER, the drive is set active (DRVATV) and control reverts to BOSS.

DRVTST is the next set of control code in the CHKDRV control sequence and is entered at the beginning of CHKDRV when a position command is being executed but there is no new, over-riding command to deal with. DRVTST manages the sequence of control states which determine the stepping rate through the command execution. DRVTST first tests the ACCEL flag to see if the drive is to be ramped up in speed (ACCEL is true if the commanded set point is over 114 counts from the present position), if not; control is transferred to PLOD which drives to null the error at 100 Hz. If the distance to be traversed is over 114 counts, the ACCEL flag will be set and the drive must be ramped up to a high speed to get to the set point rapidly.

In this high drive speed sequence, the first state is acceleration, in which the stepping rate is ramped up to the maximum speed from 100 Hz; the associated flag is ACCEL. The next state is main drive in which the drive runs at the maximum speed, (not necessarily 1000 Hz, it depends upon the highest step in the ramp sequence); the associated flag is MAIN. The next state is rampdown in which the drive rate is reduced to 100 Hz; the associated flag is RAMPDN. The last state is convergence which nulls the remnant error; the associated flag is CONVRG. System control resides in each of these states for up to several seconds (depending on the distance to be traversed), when the end of the state is reached, control reverts to BOSS which initiates the next state. Although control resides in these states, they are frequently interrupted by the Data Set interrupt (RST 7.5) and the motion count interrupt, RST 6.5.

DRVTST starts with a sequence of tests of these flags to determine which state of the sequence is operative. DRVTST begins with a call to DSTOR for fresh data and first checks that the brake is disengaged; if not, control is transferred to an error routine. ACCEL is tested next; if the drive should be accelerating, control is transferred to ZIPUP which puts the top step number of the ramping sequence in C and calls the RMPUP subroutinme which manages the process of ramping up the drive speed. When the ramp-up process has been completed, ZIPUP will clear the RAMPUP flag and set the MAIN flag which signals that the drive is at maximum speed and control returns to BOSS.

On the next pass through DRVTST control will be assumed by MAINCK in which the drives run at maximum speed and the position is tested to see if the drive has reached the ramp-down point. This point is determined by subtracting

276H from the present position using the RANGER subroutine. If the ramp-down point has been reached (or passed), the MAIN flag is cleared, the RAMPDN flag is set and control returns to BOSS.

On the next pass through DRVTST, control will be assumed by ZIPDN which calls the RMPDN subroutine which manages the ramp-down process. At the completion of the ramp-down, the RAMPDN flag is cleared, the CONVRG flag is set and control reverts to BOSS.

On the next pass through DRVTST, control will be assumed by MOVIN which manages the convergence process. The magnitude of the error is loaded in HL and CLOSE is called. If the Carry flag is set by CLOSE, the drive is at the commanded set point, the CONVGG flag is cleared and control reverts to BOSS. On the next pass through DRVTST, PLOD will stop the TIMER via TSTOP and shut down the drive via DRVSTOP. If the drive has not quite reached or has overshot the commanded set point, control is transferred to MOV1 which reverses the driving direction (if necessary), outputs the direction steering on PROM1 PORT A, updates the output data states and control reverts to BOSS. More than one pass through MOVIN may be required to finally stop the drive at the commanded set point.

A slight digression here: -- The convergence algorithm is based upon the assumptions that there is a one-to-one correspondance between the motor shaft position and the drive position (ie no gear backlash) and that the drive will not shift position during the ~ 300 milliseconds it takes for the brakes to engage. There is in fact, some gear train lost motion, (ie backlash) and a rubber spring motor coupling; therefore the Subreflector is not rigidly held in position when the motor is stopped and can move by the amount of the backlash (which is never zero) and the spring windup. This slackness can occasionally enable slight shifts in drive position during the brake engagement period. A shift (if it occurs) is manifested as a change in position of a few counts (at most) at the completion of a command. The driving force for these shifts are antenna vibrations or accelerations acting upon the mechanism or Subreflector unbalances. The effect is most pronounced in Rotation and barely discernable in Focus. A series of repeatability tests were performed on Antenna 12 after it had been in service for a year. 700 position commands were output (mostly Rotation) and the results were that the RMS error for Rotation was about 1.5 counts and the RMS Focus error was about probably possible to devise a better convergence algorithm which stubbornly insists (within a reasonable number of tries) upon achieving no more than 1 count error but there is presently no perceived need for it.

DRVSTP is the terminal phase of execution of a POSITION command and clears the DRVATV flag, updates the monitor data status, clears the control discretes in PROM1, PORTA and jumps to the BRKOFF subroutine, (not BOSS).

The RAMP UP & DOWN subroutines are called by both the CMP (central computer control) and LOCAL portions of the program.

RAMP UP -- RMPUP is a subroutine called by ZIPUP in DRVTST and executes the process of modulating the motor clock control states, keeping track of the number of drive pulses in each step and terminating the ramping process at the proper stepping rate. Upon initial entry, the RAMP flag is set which indicates that ramping is in process. The initial clock rate is set to 100 Hz from the RAMP TABLE, the step number counter is cleared, the clock rate is set

in the output data and PROM1, PORTB control lines. A count of 25 RST 6.5 interrupts is put in B and WT65 is called from RPUP2. WT65 calls DSTOR for data, loops & looks for the DRVPLS flag which indicates that 4 drive pulses have occurred, (DRVPLS is set by RST 6.5). 25 RST 6.5 interrupts are counted by decrementing B, (ie 100 motor pulses), then the next stepping rate is read from the RAMP TABLE, the step number is incremented and compared with C to see if the step number is equal to the top step number. If it is, control is returned to ZIPUP which clears the RAMP flag, sets the MAIN flag and returns control to BOSS.

RAMP DOWN -- RMPDN is a subroutine called by ZIPDN in DRVTST and executes the process of reducing the motor stepping rate to 100 Hz in steps of 48 drive pulses/step. The procedure is almost identical to the ramp-up procedure and differs only in that the number of motor drive pulses/step is fewer and the clock rates are decreased. Upon entry the RAMP flag is tested to see if the drive has been ramped up, (it may not have been), the flag is cleared, the number of steps to ramp down is added to the base address of the ramp clock control state table, (CK100) and set in HL. The number of steps +1 to execute is set in C, the motor pulse count (of 12 RST65) is set in B and the clock control state for next lower frequency is read from the table. The RPDN1 and RPDN2 loop reduce the clock rate to the base rate of 100 HZ and control reverts to ZIPDN. The reason that RMPDN has fewer motor clock pulses than RMPUP is that it is easier to decelerate the drives (because of friction) than to accelerate them.

ERROR HANDLERS

ETRN -- ETRN handles the problem of turning off the Translator power if it has not responded properly to the turn on control discrete. The control discrete is turned off, the TRANSLATOR fault bit is set in the output data area and the command is reset by a jump to RSCMD.

EBRK -- EBRK handles the problem of turning off the brake power if it has not responded to the turn on control discrete; the actions taken are very similar to those of ETRN above.

EDRV -- EDRV is discussed in the DRIVE PULSE INTERRUPT & MOTION ANALYSIS discussion.

RING DRIVE HANDLER

CHKRNG -- CHKRNG is entered from BOSS during the test of the RING ACTIVE bit (80H in ERRO+2) in the output data area and is analogous to the CHKDRV or LOCAL functions in POSITION commands in that it tests for the attainment of the commanded state within a specified actuation period. Since Rotation POSITION and RING commands may be executed concurrently there are two possible cases for the use of the timer: 1) If the Rotation command arrives first followed by a RING command, Rotation execution is started (which ties up the Timer), and the RING command execution is initiated, the appropriate Ring actuator lines are energized etc. At the completion of the execution of the Rotation command (a maximum of 16 seconds) control is transferred to CHKRNG from the BOSS scan and if either the EXT or RET switch bit is set (indicating that the commanded state has been attained), an additional 3 seconds of power on delay is added to CHKRNG just to insure that the actuator motion is completed. 2) If there is no Rotation command active, on the pass through BOSS, control is

immediately transferred to CHKRNG which sets the Timer for a 16 second period and the code is executed as described below.

The RING command is initiated from the Data Set command initiation code in response to a RST 7.5 interrupt which determines the direction to drive and energizes the appropriate motor lines. These operations are discussed in the Data Set Ring Command Initiation section.

Upon entry, the command direction flag EXTFLG is tested to see if the Ring is to be extended or retracted. If EXTFLG is true the command is extend, if false it is retract. EXTFLG determines whether to test the EXTEND or RETRACT flags (in ECHO+2) which indicate the state of the switches which are actuated by the drive mechanism at the completion of the motion. DSTOR updates the status of these two flags. If the designated switch is not actuated, a 16 second delay argument is loaded into DE and set in TIMER by RNGWIT which also sets the jump address of RNGWT1 in TRAP, (see the discussion of time-out errors in the TIMER INTERRUPT section), and the program loops in RNGWT1 until the time-out interrupt. When the 16 seconds have elapsed program control is transferred to RNGWT2. RNGWT2 first clears the RING FAULT flag (if set), determines the commanded direction from EXTFLG and tests the RING EXTEND bit in ECHO+2 to see if the Ring Extend switch has been actuated. If the command is RETRACT, the RETRACT bit is tested. If the appropriate bit has not been set, a RING FAULT bit is set in ECHO+2 and the RNGCMD flag is cleared in CHKRN2.

If the designated switches are actuated, indicating that the command has been completed, a 3 second delay (instead of 16) is set in TIMER and the code executes as described above.

If the command is successfully executed, the RING ACTIVE flag in ERRO+2 is cleared, the Ring motor power is turned off and the RNGCMD flag is tested to see if a new Ring command has just arrived. If not control is returned to BOSS. If so the new command is to be initiated, the RING ACTIVE flag is set, the registers are pushed and control is transferred to EXTRT1 (in the Data Set command initiation code) to reinitiate the command under the normal conditions of Ring command execution.

ARITHMETIC SUBROUTINES

RANGER -- RANGER is a general purpose 16 bit arithmetic comparison subroutine which determines the absolute value of the difference of two 16 bit arguments, the sign of the difference and whether or not the arguments are identical. In calling RANGER the contents of DE are subtracted from the contents of HL with the resultant difference in HL and the arithmetic sign of the difference in C, (0 = +). If HL = DE the Zero flag will be set.

The A register, (accumulator) is loaded with the contents of L (the least significant byte) and E is subtracted from A and the resultant difference is loaded into L. If the subtraction caused a borrow out of the high order bit, the Carry flag is set. The A register is loaded with the upper byte (in H); D and the borrow from the first subtraction are subtracted from A. The resultant difference is loaded into H and C is initialized to 0. If the result of the two-byte subtraction is positive, (ie HL greater than DE), the JP (positive) transfers control to RNGR1 which tests for H & L = 0 by orring H with L. If

the Zero flag is set HL = 0. These positive results return control to the location from which RANGER was called.

If the result of the subtraction was negative, control falls through the JP instruction, C is made 1's and CMPHL is called to complement HL. The complements are 1's complements so HL is incremented to complete the representation of the resultant difference if it is a negative value. Control is returned to the location from which RANGER was called.

VECTOR -- VECTOR is called from DSTOR to determine direction to drive to reach the commanded set point by the shortest physical path. VECTOR is called with HL = destination and DE = present position. RANGER is called upon entry. Upon return from RANGER, HL contains the absolute value of the difference between command and present position. If upon return from RANGER, HL = 0, the commanded set point is the present position; no direction decision can be made so control returns to DSTOR.

To determine the shortest direction, a value equal to half the total numeric range is subtracted from the difference and the state of the Carry flag determines the direction to drive. If you think of the positions as numbers wrapped around a circle, position 0000H is adjacent to 3FFFH; for example, if the drive were at position 3000H and it was commanded to position 100H, it is obvious that the best way to go is through 3FFFH and 0000H to 100H. You and I see that but the mathematics of a simple subtraction by the processor to determine direction would try to drive to 100H by driving the long way around through decreasing numbers. To implement this best direction algorithm, -2000H (in DE, half the numeric range) is added to the position difference (in HL). If the Carry flag is not set, the best direction to drive is in the direction of increasing numbers (ie CW). Control is transferred to VEC1 which adds back the 2000H subtracted above, L is set in A and orred with H which sets the Zero flag if HL = 0. Control is returned to the calling location (DSTOR) with the C =0 flag set which designates that the CW direction is the best direction to drive.

If the Carry flag is set (CCW direction), C is complemented in CMPHL and control is returned to the location from which VECTOR was called (ie DSTOR).

CLOSE -- CLOSE is a simple subroutine which determines whether a position error in HL is less than 3 counts. If H is not 0, control is returned immediately since the error is greater than 256. Next, L is compared with 3 and the Carry flag is set if the error is less than 3. The calling code will test the Carry flag upon return.

DEVICE DRIVERS

DSTOR -- DSTOR is an important subroutine which gathers data from the Apex Interface and pedestal room, formats and stores this data for use by the control programs and for output to the Data Set, drives the LED display on the M8 and senses fault conditions in the Apex Interface. Virtually all operations of the control programs are dependent upon data gathered by DSTOR; this single subroutine minimizes the data access function through the entire body of code.

DSTOR begins by pushing the contents of the registers onto the stack. The Apex Data Registers are cleared by the request, B is set to 10 and the

processor enters a test loop which tests for the appearance of a 10 in the top two bits of the Apex Data Register. In the event that the Apex data does not show up within the alloted count, a fault bit is set in the output data area, Apex data storage operations are aborted and control is transferred to LP3-LP5 which does a lot of bit swapping.

If the data shows up within the alloted time, the Apex fault bit is cleared (if it was set), the position data is masked and stored (in both Data Set and internal formats), the difference between current and commanded position (ATVCMD) is calculated, (even if the command has been completed) and the absolute value of the difference is stored in the command error (ERRO) location in the Data Set data table. VECTOR is called which determines the direction to drive to null the error. Upon return from VECTOR the sign of the difference (in the C register) is placed in DIR. If C = 0, the direction is CW. When a new command is about to be initiated, this direction initialization in DSTOR establishes the direction to drive to null the error.

The 8-bit drive velocity data is formatted as 12 bit data and stored in the Data Set data table.

The Rotation Apex Discretes are next read & stored; these are the Rot lim switches (currently non-existent) and the brake V*I discrete. The data format for Mux 234 (Section 10) shows the four Lambda code signals; these are actually not not read (from M8) at present but if the index pin were ever to re-appear these bits would be assigned to these functions.

The Apex Analog/Discretes data is read next which consists of the Apex Analog data(10 bits), associated mux address (3 bits), Ring discretes (EXTEND, RETRACT), and CW,CCW limit switches, (not presently used). These are processed as follows:

The Ring discretes (EXTEND & RETRACT) are read and extracted by masking all other bits, shifted to the lsb position and merged with the old echo word to retrieve the old RING FAULT bit (set by RNGCHK). The result is stored as the new command echo (ECHO + 2) in the Data Set data table.

The Apex anlog data and associated mux address bits are read again, this time masking the RING discretes. The 10 bit data is formatted to be read out as 12 bit data. The 3-bit mux address is divided by 4 and added to the base address of the Apex Data table (APATAB) and set into HL. The Apex Analog data (in DE) is stored in the table at this address.

The mux address of the Apex Analog data to be read out to the Data Set (ANAMX, not the mux address of the data stored above) is added to the table base address and this data is stored in the Data Set Apex Analog data table for subsequent readout.

The command status (DRVATV) is tested and if true is merged with the Ring Active, Nap Active, Timeout, cable interlock, Apex Interface fault, System fault and CMP/LOC mode switch bit.

After this reading and formatting, the registers are popped and control is returned to the location from which DSTOR was called.

TRNON -- TRNON is a subroutine called to turn on the Translator and test for

the detection of the Translator power supply voltage within 1 second from turnon. At entry, the address of the Translator error handling routine is set in location TRAP, the count for one second is set in TIMER, the command state is set in the monitor data table (DSCR+1), and the control discrete is set on the PROM1, PORT A line. TRNON loops and tests for the arrival of this discrete on PROM2, PORT A. If the discrete arrives before the 1 second period, TIMER is stopped and control reverts to NORMP or LOCAL via TSTOP which executes a return to the calling source.

TRNOF -- TRNOF is called by PLOD to turn off the translator and is almost identical to TRNON except that it turns off the Translator and returns control to via TSTOP as in TRNON.

BRKON -- BRKON is called to turn on the brake (ie release) and test for the detection of brake voltage and current within 1 second. The brake error hanling address is loaded into location TRAP, the TIMER is set to 1 second, the brake command bit is set in the output data area (DSCR+1) and the control discrete line is set high on PROM 1, PORT A. DSTOR is called and the brake V*I bit is tested in a loop. If it is true within 1 second (ie before the TIMER TRAP interrupt), TSTOP is called to stop the timer and return control to DRVINT (via NORMP) to complete the initialization before returning to BOSS.

BRKOF is called to turn off the brake and test for the attainment of the command within 1 second as in BRKON. The operations are almost identical with BRKON except for the turned off discrete line.

INTERRUPT DRIVEN SUBROUTINES

Some processor operations are Interrupt-driven because they are asynchronous with the command execution and are of a transcendent nature which requires immediate processor action. The interrupt service routines perform the following functions:

MOTION ANALYSIS -- This interrupt-driven subroutine performs the very important function of analyzing the drive motion to determine if the drive is dragging or sticking - a frequent problem with these motors & Translators which have marginal torques for this application. The drives frequently stick in the winter time during cold snaps; a bad Translator driver or logic board will also cause dragging or sticking.

TRPR is entered when the controller has output 4 drive pulses to the motor. Upon entry, the registers are saved on the stack and the DRVPLS flag is set (DRVPLS is tested by WT65 in the RAMP up/down code to determine when a drive step has ended), if the controller is in LOCAL mode, the MOTION counter is cleared by TRPR1, the registers are popped and control reverts to the location which was interrupted. If in CMP (central computer mode), the CW/CCW steering direction discretes are tested and if both are zero (implying that a POSITION execution is not in process), MOTION is cleared, the registers are popped and control reverts to the location where the interrupt occurred.

If a POSITION command is being executed, the change of drive position is compared with what it should be to determine drive sticking. The analysis is done by accumulating 25 drive pulse interrupts (RST 6.5) in MOTION; this corresponds to 100 motor drive pulses. If MOTION = 25, the last position

(LSTPOS) is compared with the present position (POSTN) by calling VECTOR, if the difference is 0 the drive is stuck, if the difference is less than 60 counts (ie 45 motor pulses) the drive is dragging. The selection of the 60 count threshold is arbitrary and not very critical; at the torque breakage threshold the effect is very pronounced and the motors do not respond to most of the drive pulses. If either of these conditions occur control is shifted to EDRV (get it there if you can code) which attempts to complete the commanded motion at a lower drive rate.

EDRV sets the STACK pointer to the top RAM address, (the contents of the PSW,B,D,H registers pushed onto the STACK are forgotten in doing so), the DRIVE FAULT bit is set in the output data area and the ramp step number is tested. If the motor stepping rate is less than 300 Hz (peak torque is about 250 Hz) the command is aborted via RSCMD. If the drive rate is above 300 HZ, the motion analysis flag GETIT is set true, the timer is stopped by a call to TSTOP, the drive is stopped by a call to DRVSTP, and the acceleration flag (ACCEL) is set false. The command is initialized again by jumping to DRVIN1 which is the the command initialion entry point for the get-it-there-somehow function. There is a good chance that the command can be completed at the expense of execution speed which is much better than staying stuck.

Motion analysis is not performed during the first 100 pulses of drive motion; during this period the drive coupling spring is winding up (see F/R Dynamics) and there is a net deficiency in the amount of realized drive motion. The deferral action is controlled by the state of the step counter; motion analysis starts at the 150 Hz stepping rate.

DATA SET INTERRUPT -- This code services the Data Set interrupts which input the commands and access monitor data from the F/R System.

BURP is an RST 7.5 interrupt resulting from a Data Set command input or a request for monitor data. When the interrupt occurs, the Sub-Mux Address and a Command or Data Flag are stored In the SMAEV register. The flags enable the processor to identify the interrupt as a command or data request and the address identifies the command or data argument. In the case of a command, the Data Set has shifted the command into the command input shift register and the command strobe requests the processor to read the command, the Sub Mux Address and the Command flag. In the case of a monitor data request, the data strobe signals the processor that it is expected to read the Sub Mux Address and Monitor data flag, to identify the requested data and load it into the output registers for the Data Set to read via shift clocks.

On entering BURP the registers are pushed onto the stack, the Sub Mux event register (SMAEV) is read, the Sub-Mux address is saved and the command/data flags are decoded. In the case of commands, the command arguments are saved and the sign bit (bit 13) is complemented and saved in DE. The mux address is decoded to determine if it is a POSITION command (mux 0, ie 330 in Data Set format), a software RESET command (mux 1 - 331), a NAP command (mux 2 - 332), or a RING command (mux 6 - 336). Undefined commands are stored in a bit bucket. After identification of these types of commands, control is transferred to code which sets command request flags.

POSITION COMMAND INITIATION -- If the decoded command is a POSITION command, control is transferred to DRVCMD which stores the unaltered command argument (in HL) in ECHO, the output data table. The argument is saved in CMDTMP for

subsequent use in initiating the command, the request flag, DRVREQ is set (to 1), the registers are popped in SKIP, the interrupts are enabled and control returns to the place where the interrupt occurred.

RESET & NAP COMMAND INITIATION -- In a similar manner the RESET and NAP command flags are set, the registers popped via SKIP and control returns to the interrupted code.

The process of initiating the execution of these three commands is started in BOSS when the command request flags are tested. The reason that command initiation is handled by BOSS is that the initiation process may be complicated and require slowing the drives etc which is best handled in a controlled sequential manner.

RING COMMAND INITIATION -- In the event that the command is a RING command, the commanded action is initiated immediately in EXTRTC, (after testing for the NAP mode to see if the command should be ignored).

If the code is not in NAP and the Ring command is not active, the RING ACTIVE bit is set in the output data word ERRO+2 and the lsb of the command argument is tested (from ERRO+2) to see if the command is active, if so the command argument is tested (in EXTRT2) against the EXTFLG (set as a result of initiating the EXTEND command) to see if the RING EXTEND command is already being executed from a previous command. If so, control returns to the place where the program was interrupted via SKIP. If not, the RNGCMD flag (which indicates an over-riding ring command to EXTEND the ring during the process of executing a RETRACT command) is set and control is returned as above via SKIP.

In EXTRT1 the argument is tested (lsb = 1 for EXTEND, 0 for RETRACT) to determine the commanded action. If EXTEND, the extend data flag bit is tested to see if the Ring is already there, if so, nothing more needs to be done and control returns to the place where the interrupt occurred via SKIP. If the Ring is not at the EXTEND position, the EXTEND flag is set, the EXTEND power bit is set in DSCR+1 and the Ring Extend control bit is turned on in PROM1, PORT A which turns on the Ring Extend relay. The RNGCMD flag is cleared and control returns to the interrupted code via SKIP.

If the Ring command is RETRACT, the same sequence occurs but the Retract flag and data bit are set and the Ring Retract control bit is set which turns on the Ring Retract relay. Control returns as above via SKIP.

MONITOR DATA REQUEST -- Now for the monitor data output path of BURP. If the request is for Apex Analog data (Mux 225), the most recently used Apex Data table address (ANAMUX) is incremented so that the next Apex Analog data readout will be the next value. The mux address is multiplied by three to form an index which is added to L. H is set to 1800H (the base address of the DATA SET TABLE) for the data output sequence. The Data Set output registers addresses are: DSDT1, DSDT2 and DSDT3. The data readout process must be expeditious as only 100 microseconds elapse between the STRI pulse and the unload clocks (CLKI).

TIMER INTERRUPT SERVICE -- BLAP is entered from the TRAP interrupt which cannot be disabled, has the highest priority and is used with the 8156 Timer for execution time-out functions which test for the attainment of important states within a specified time. If the tested state is not attained, the program

logic presumes a malfunction.

In setting up the timer/TRAP interrupt, a device driver enters the address of the associated error handling code into the error handling address, (ie TRAP) so that in the event of a time-out TRAP interrupt, the TRAP interrupt handling code (BLAP) has an address vector to the this error handling code.

BLAP first sets the Stack Pointer to the top of the stack and loads the error handling address (TRAP) into HL which is then pushed onto the stack, the timer is stopped via the TSTOP subroutine, a TIME-OUT fault bit is merged into the output status data, the RST 6.5 interrupt flip flop is cleared, the RST 7.5 interrupt is cleared, interrupts are enabled and a the RET instruction pops the error handling address off the stack into the program counter.

LOCAL COMMAND EXECUTION

The LOCAL section manages the motion of the drives when the controller is in the LOCAL mode. The M8 front panel switches are read to determine the operator's commands. In LOCAL the Translator is turned on, the drive rate is initialized to 100 Hz, the drive position and Apex discretes are read via a call to DSTOR and if there are no faults, the M8 switches are read to determine direction and whether or not to ramp the drive. If the distance to be traversed is small the operator will (probably) not ask for ramping so the drive will be driven at 100 Hz as long as a switch is actuated. If both direction switches are actuated the drive will be driven in the CW direction.

LCW1 turns on the brake, sets the CW drive direction bit in the output data area and tests the ramp switch; if ramping is called for RMPUP is called with a top step number of 17 (ie 1000 Hz). Upon completion of the ramp-up LCW1 is entered. DSTOR is called to read the state of the CW switch and if it is still actuated the program continues to loop and drive the motor until the switch is released. When the switch is released the program jumps to LSTOP which calls RMPDN which slows the drive to 100 Hz, the brake is turned off, the drive status bits are updated in the output data area and the program jumps to LOCAL for continued looping.

LCCW and LCCW1 operate in an a similar manner in driving in the CCW direction.

While looping in the LOCAL mode, the BOSS scanning is inhibited.

2.3 FOCUS CONTROL PROGRAM

The FOCUS control program is almost identical to the ROTATION control program; the instructions compare 1:1 throughout most of the code. This section addresses the areas in which FOCUS differs from ROTATION.

The FOCUS program is not involved in RING control; this affects CHKDRV in that CHKRNG is not present. Correspondingly the Data SET command initiation is simpler in that EXTRTC and RETRCT are not present.

The output data formats are almost identical except that the RING ACTIVE bit is not present in mux 221, and RING FAULT,RING RETRACT & RING EXTEND bits in mux are not present in mux 222. These bits are set by DSTOR and the Ring

handling code.

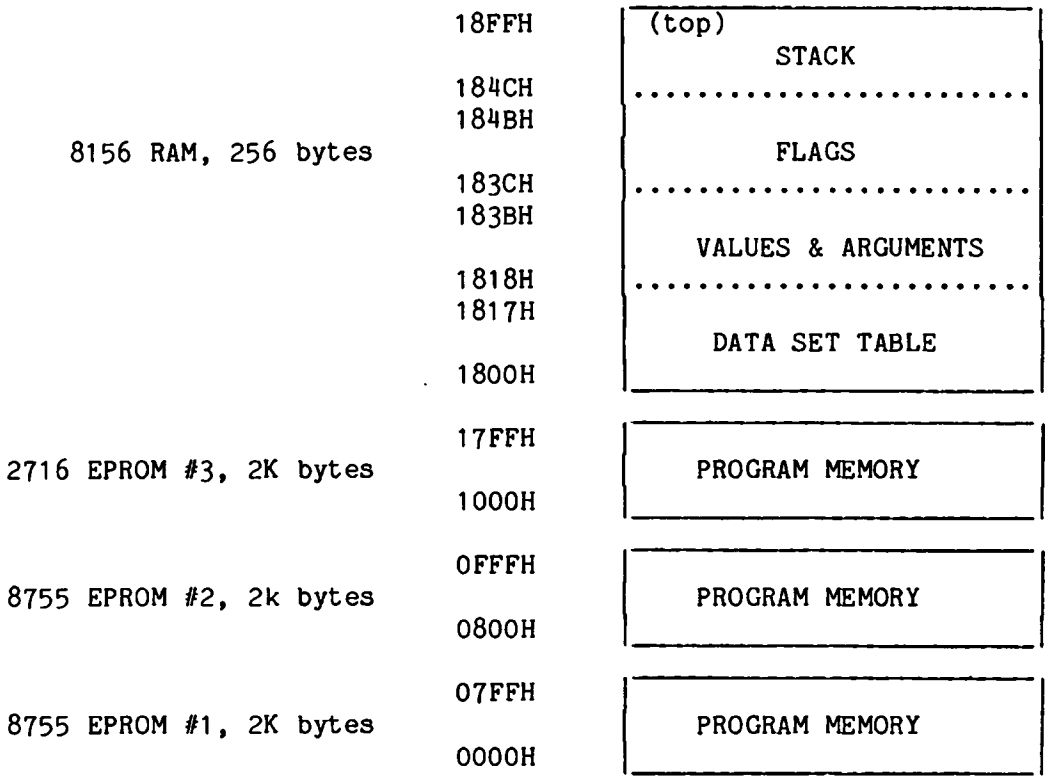
Because the Focus drive motor is heavily loaded in driving UP, experience has shown that it is best to restrict the maximum Focus drive rate to 500 HZ because of the severe resonance hole in the motor torque curve at 550 HZ. Therefore; in calculating the number of steps to ramp the Focus drive in DIV, the maximum number is restricted to 7, the pointer to the 500 Hz rate in the RAMP TABLE.

VECTOR is not in the FOCUS program arithmetic subroutines as there is only one possible direction to drive to null a position error. These FOCUS subroutines have CMDCHK which tests the command arguments against hi and lo limits to prevent the subreflector from being driven into the limits in CMP control. It is possible to drive Focus into the limits in the LOCAL mode. The upper limit is tested first, if the command msb is less than 3A00H (35000 octal), the argument is next compared with 0500H (2400 octal). If the argument is greater than the high limit or is less than the lower limit, control is returned to DRVINT with the Carry flag set. This condition aborts the command initiation and sets the OPERATOR ERROR fault.

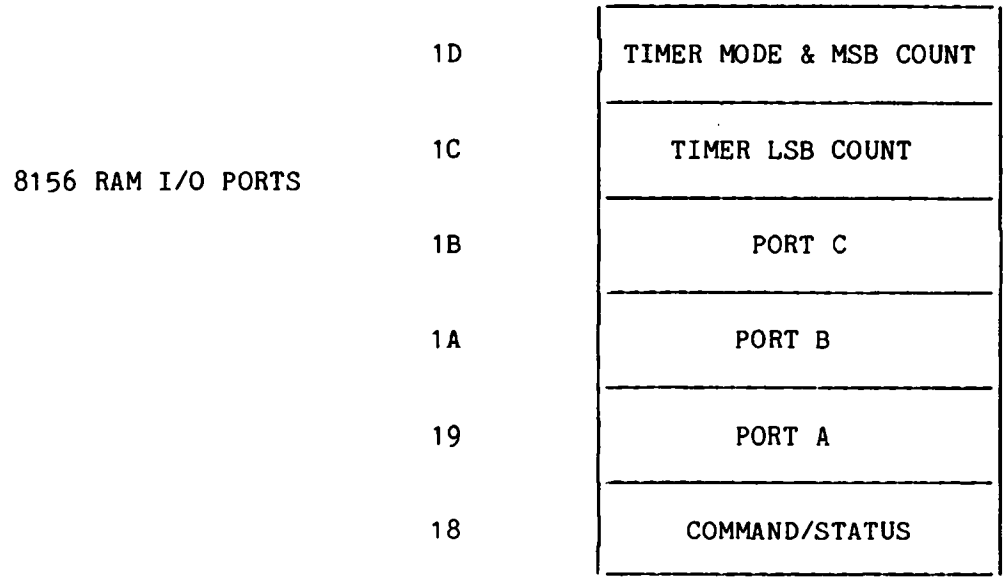
DSTOR does not read the RING EXTEND & RETRACT bits from the Apex Interface data.

The motion analysis code in TRPR tests for motion greater than 43 counts and is based upon the Focus drive motion of 1.318 steps/bit. This value is 60 in TRPR in the ROTATION code since the the Rotation drive moves 1.318 steps/bit.

Memory Map:



I/O Port Map:

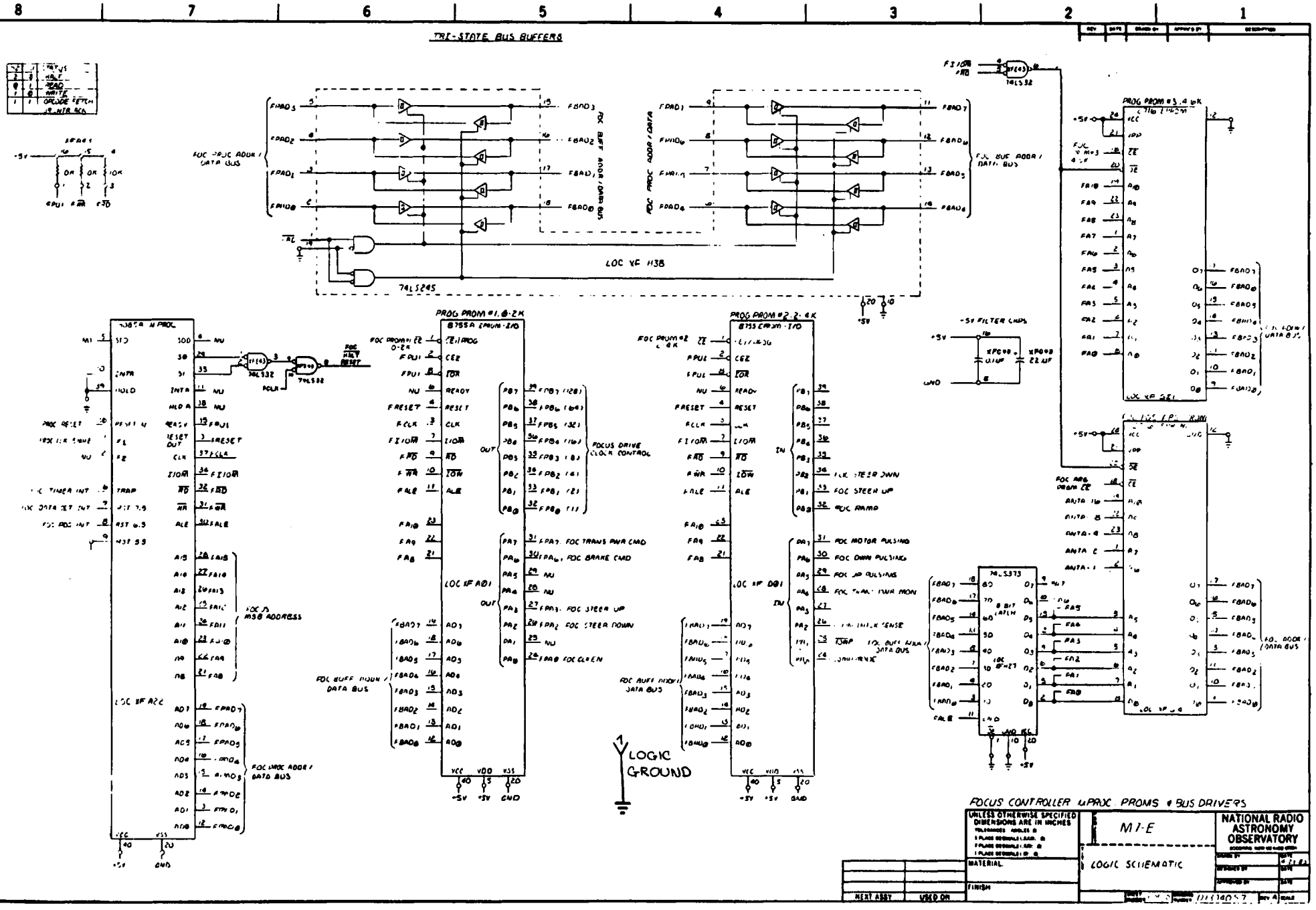


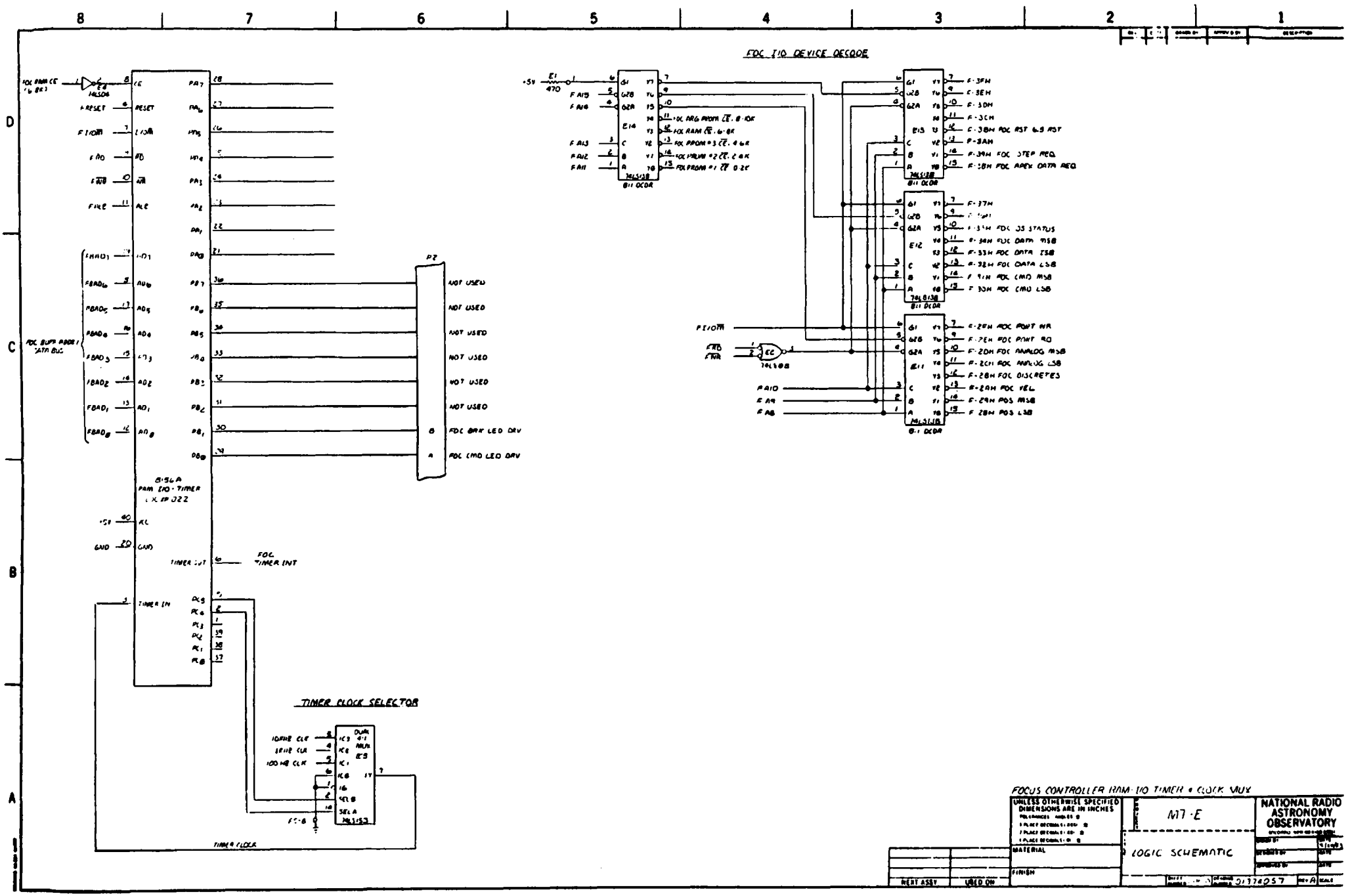
8755 EPROM #2 I/O PORTS

0B	PORT B DIR
0A	PORT A DIR
09	PORT B
08	PORT A

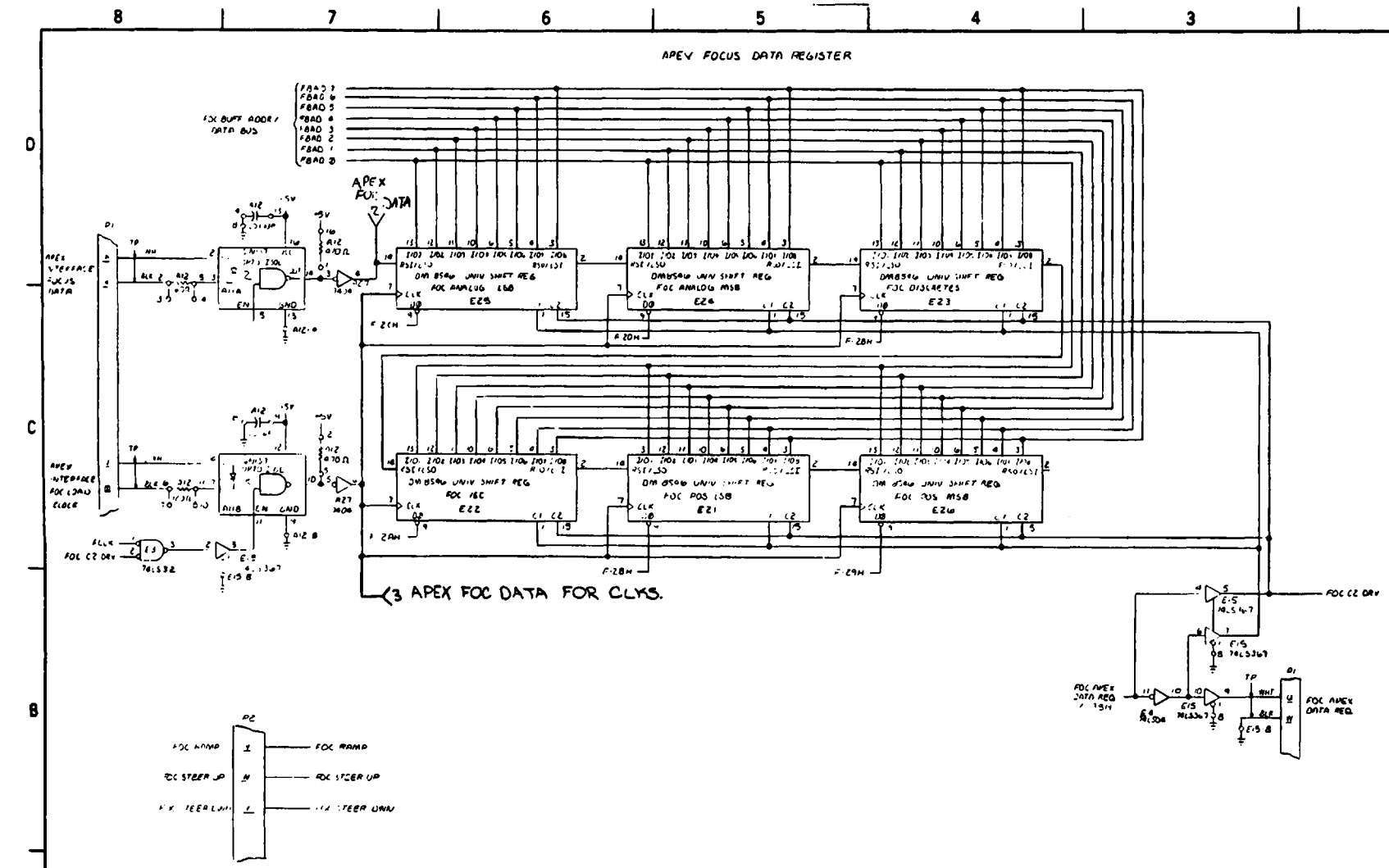
8755 EPROM #1 I/O PORTS

03	PORT B DIR
02	PORT A DIR
01	PORT B
00	PORT A


TRI-STATE BUS BUFFERS
FOC PROC ADDR / DATA BUS
FOC BUFF ADDR / DATA BUS
LOC IF H38
74LS245
FOC BUF ADDR / DATA BUS
PROG PROM #1 0-2K
PROG PROM #2 2-4K
PROG PROM #3 4-6K
FOCUS DRIVE CLOCK CONTROL
FOC STEER DOWN
FOC STEER UP
FOC RAMP
FOC MOTOR PULSING
FOC DWN PULSING
FOC UP PULSING
FOC BUFF ADDR / DATA BUS
LOGIC GROUND
FOCUS CONTROLLER µPROC PROMS & BUS DRIVERS
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL
FINISH
NEXT ASSY
USED ON
M1-E
LOGIC SCHEMATIC
NATIONAL RADIO ASTRONOMY OBSERVATORY

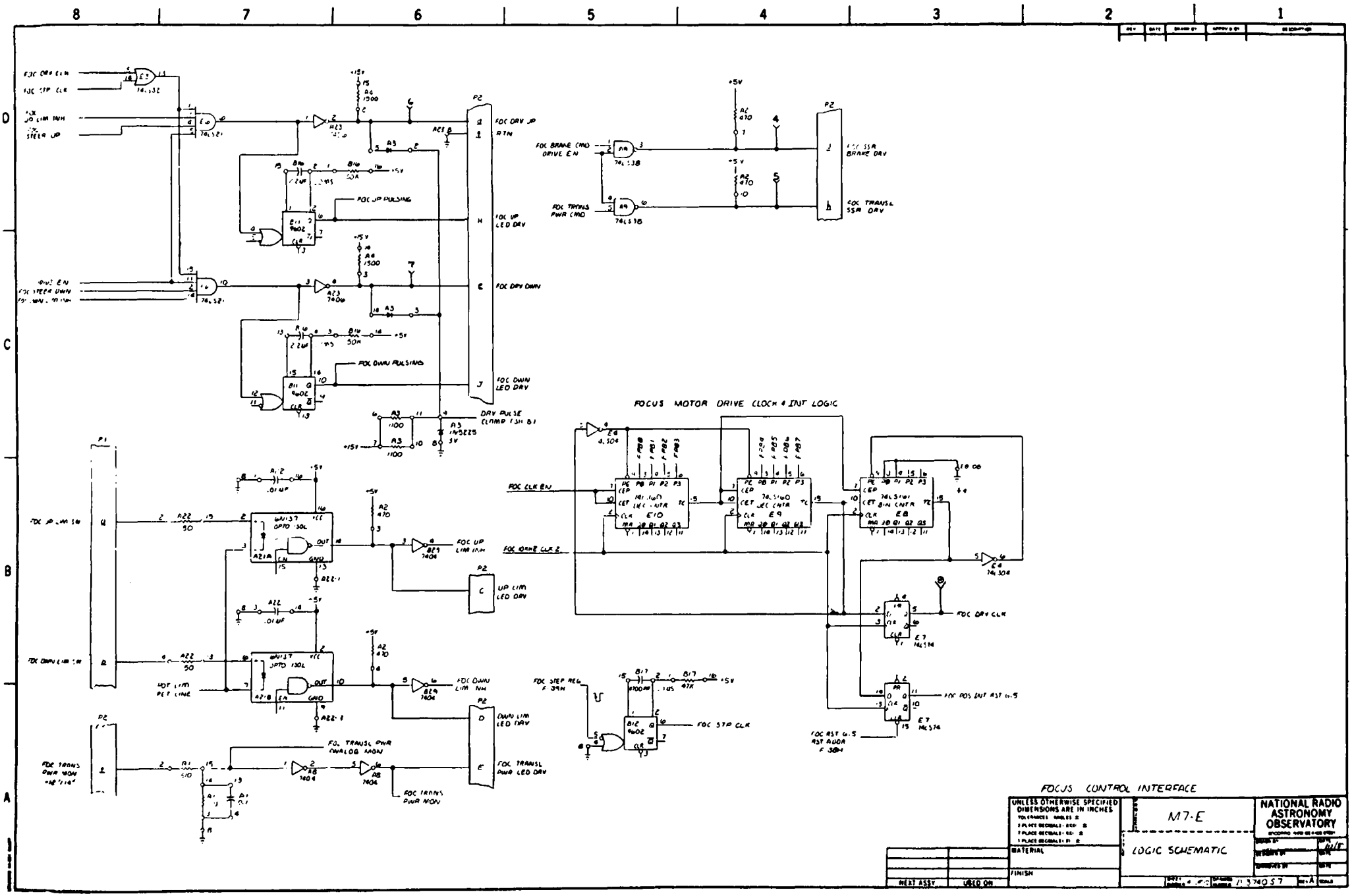

FDC I/O DEVICE DECODE
TIMER CLOCK SELECTOR
P2
NOT USED
FDC BRK LED DRV
FDC CMD LED DRV
FDC TIMER INT
TIMER CLK
FOCUS CONTROLLER RAM-I/O TIMER & CLOCK MUX
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL
FINISH
NEXT ASSY
USED ON
M7-E
LOGIC SCHEMATIC
NATIONAL RADIO ASTRONOMY OBSERVATORY
D1174057

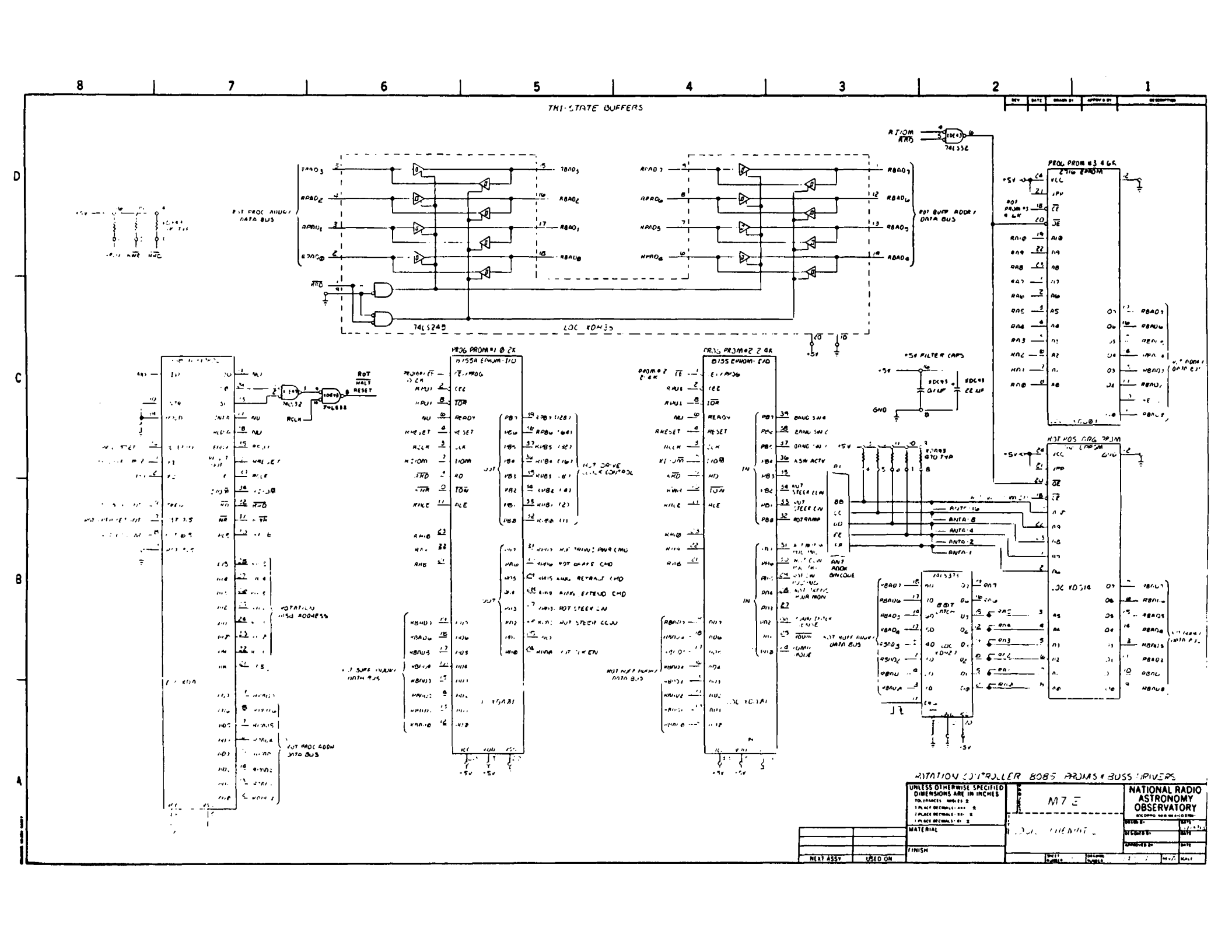
APEX FOCUS DATA REGISTER

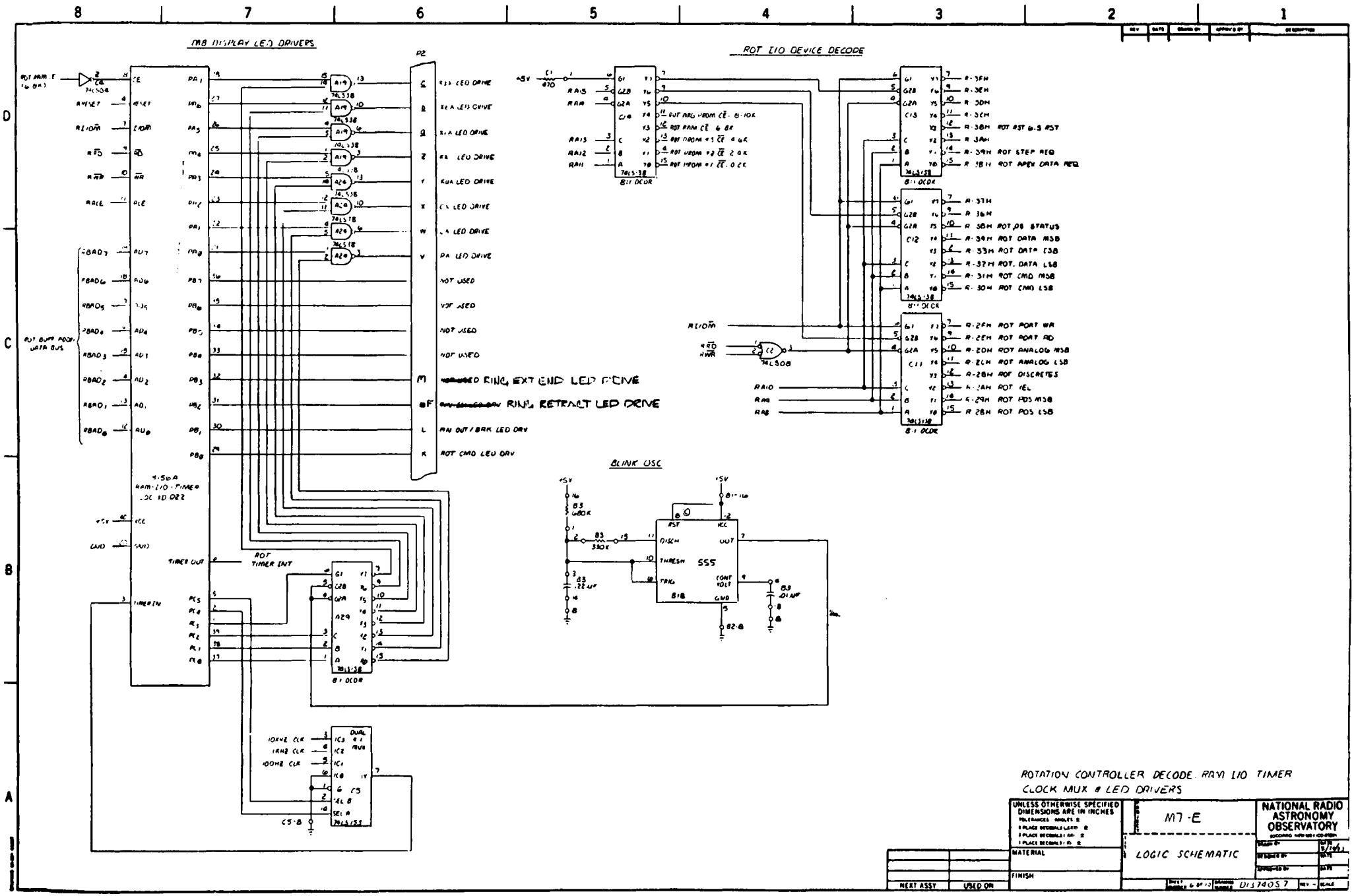


FOCUS APEX DATA & CNTL ROOM INTERFACE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	M7-E
MATERIAL	LOGIC SCHEMATIC
FINISH	NATIONAL RADIO ASTRONOMY OBSERVATORY
NEXT ASSY / USED ON	


FOCUS MOTOR DRIVE CLOCK & INT LOGIC
FOCUS CONTROL INTERFACE
M7-E
LOGIC SCHEMATIC
NATIONAL RADIO ASTRONOMY OBSERVATORY
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL
FINISH
NEXT ASSY
USED ON
FOC DRV JP
FOC DRV DWN
FOC UP LED DRV
FOC DWN LED DRV
FOC BRAKE CMD DRIVE EN
FOC TRANS PWR CMD
FOC BRAKE DRV
FOC TRANSL SSR DRV
FOC CLK EN
FOC HOME CLR 2
FOC DRV CLR
FOC STEP CLR
FOC STEP REQ F 39H
FOC RST U-5 RST AUDR F 38H
FOC UP LIM SW
FOC DWN LIM SW
UP LIM LED DRV
DWN LIM LED DRV
FOC TRANS PWR MON
FOC TRANSL PWR LED DRV


TRI-STATE BUFFERS
74LS245
LOC ROM #3
74LS32
74LS08
PROG PROM #1 @ 2K
PROG PROM #2 2 4K
PROG PROM #3 4 6K
ROT PROC ADDR/ DATA BUS
ROT BUFF ADDR/ DATA BUS
ROTATION CONTROLLER BOBS PROMS & BUSS DRIVERS
NATIONAL RADIO ASTRONOMY OBSERVATORY
M7E


MB DISPLAY LED DRIVERS
ROT I/O DEVICE DECODE
BLINK OSC
P2
M RING EXTEND LED DRIVE
F RING RETRACT LED DRIVE
L PAN OUT / BRK LED DRV
R ROT CMD LED DRV
NOT USED
8:1 DCDR
74LS138
74LS08
555
ROTATION CONTROLLER DECODE RAM I/O TIMER
CLOCK MUX & LED DRIVERS
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL
FINISH
NEXT ASSY
USED ON
M7-E
LOGIC SCHEMATIC
NATIONAL RADIO ASTRONOMY OBSERVATORY
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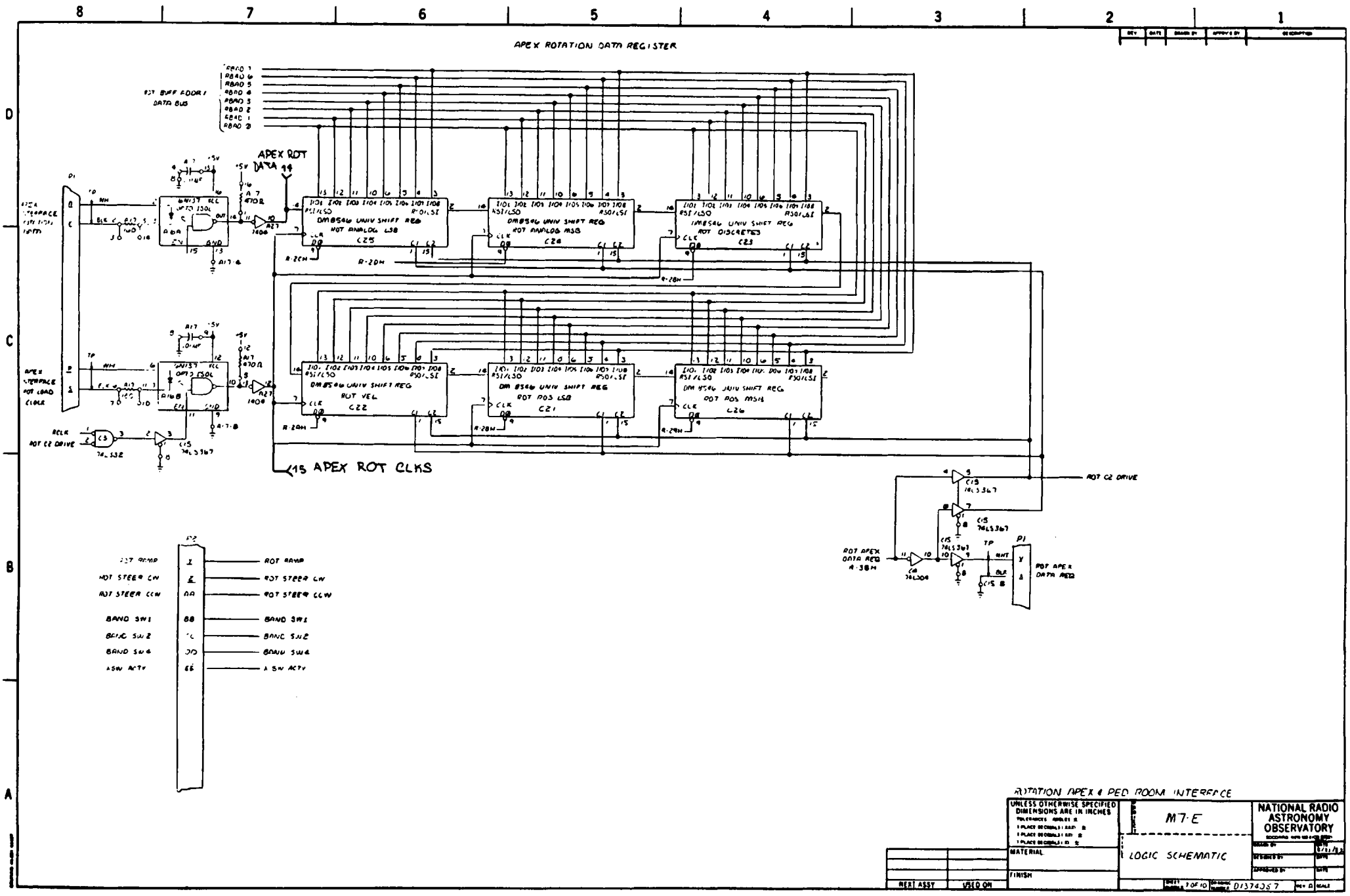


ROTATION APEX & PED ROOM INTERFACE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL

FINISH

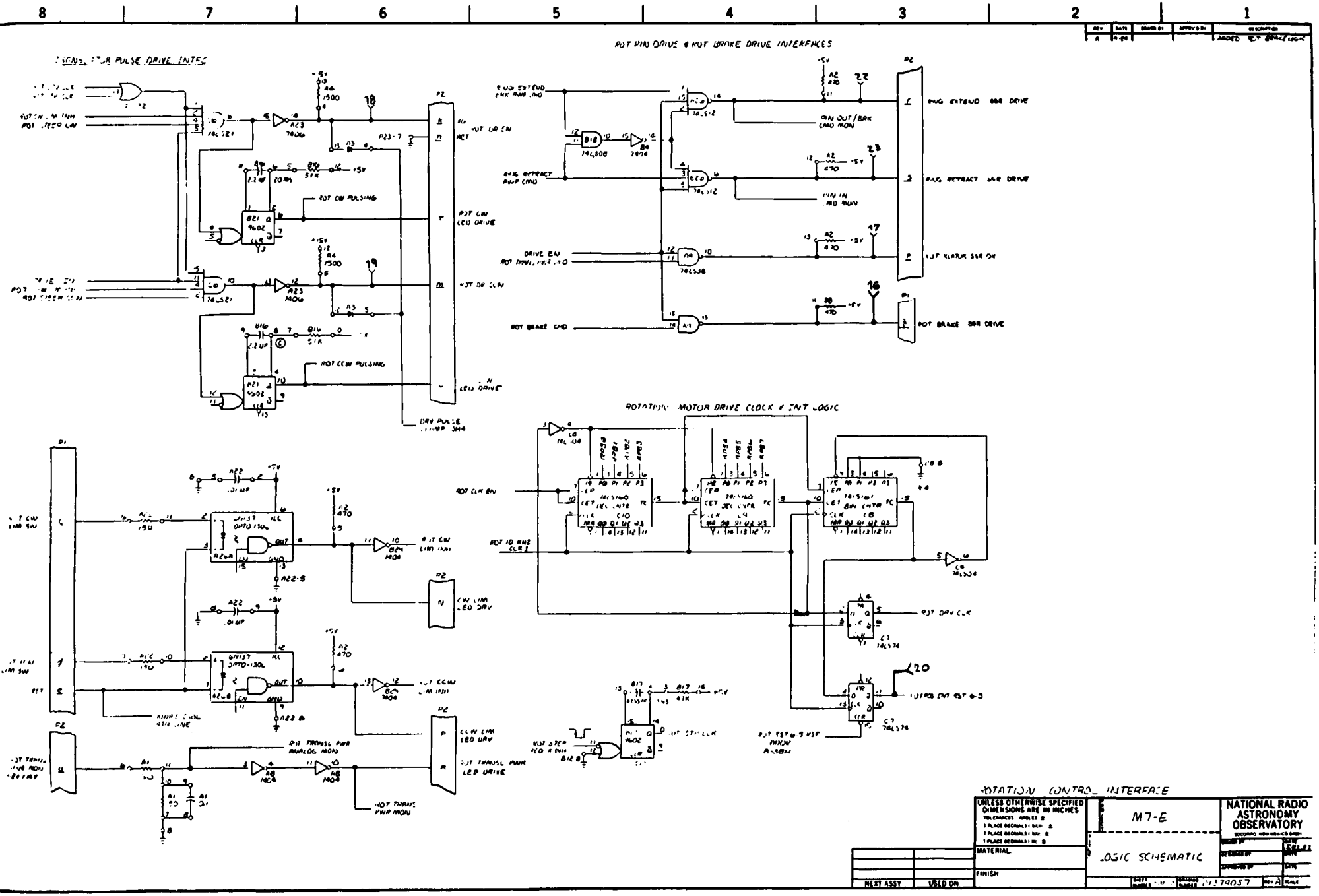
NEXT ASSY | USED ON

M7-E

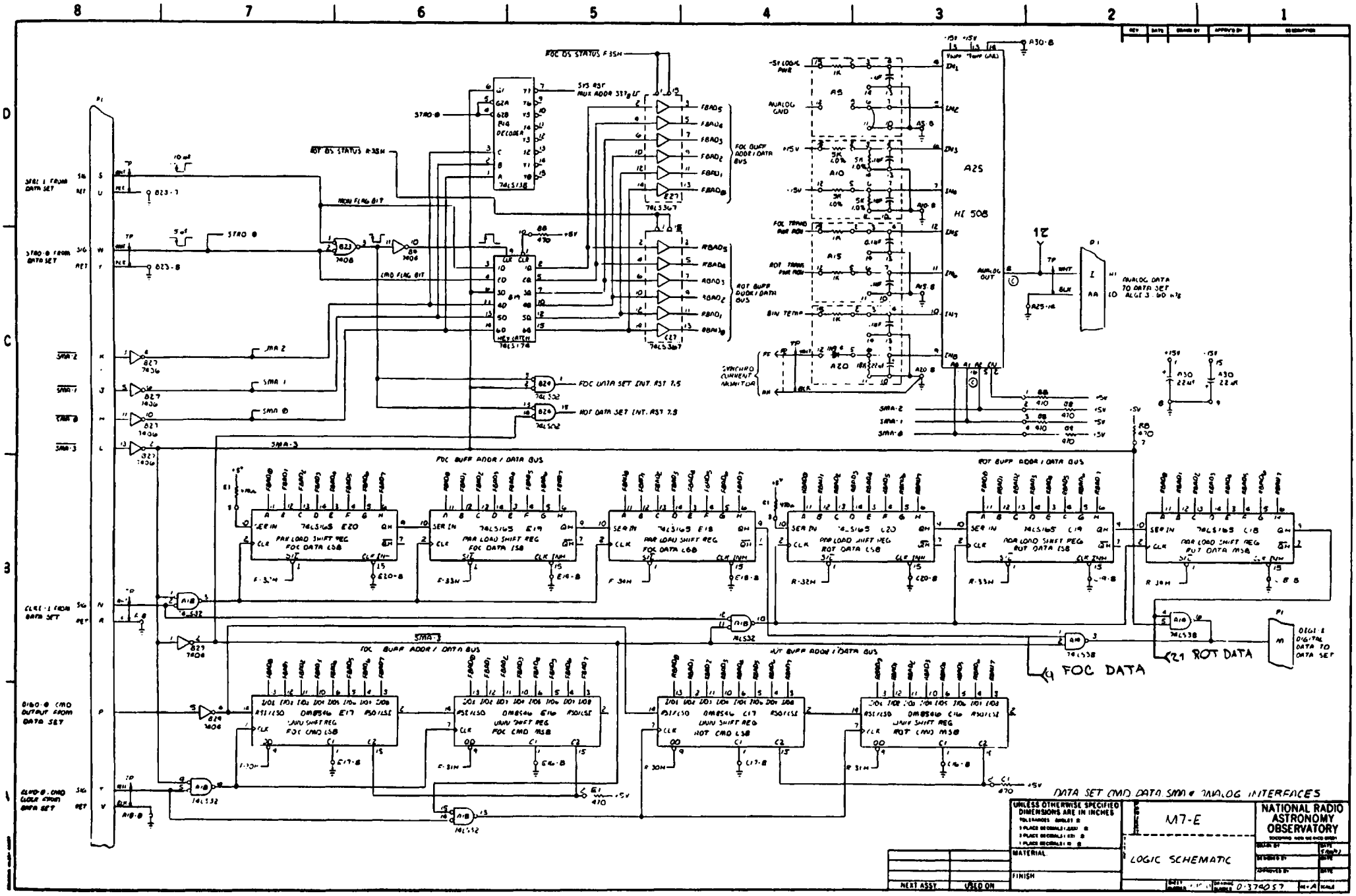
LOGIC SCHEMATIC

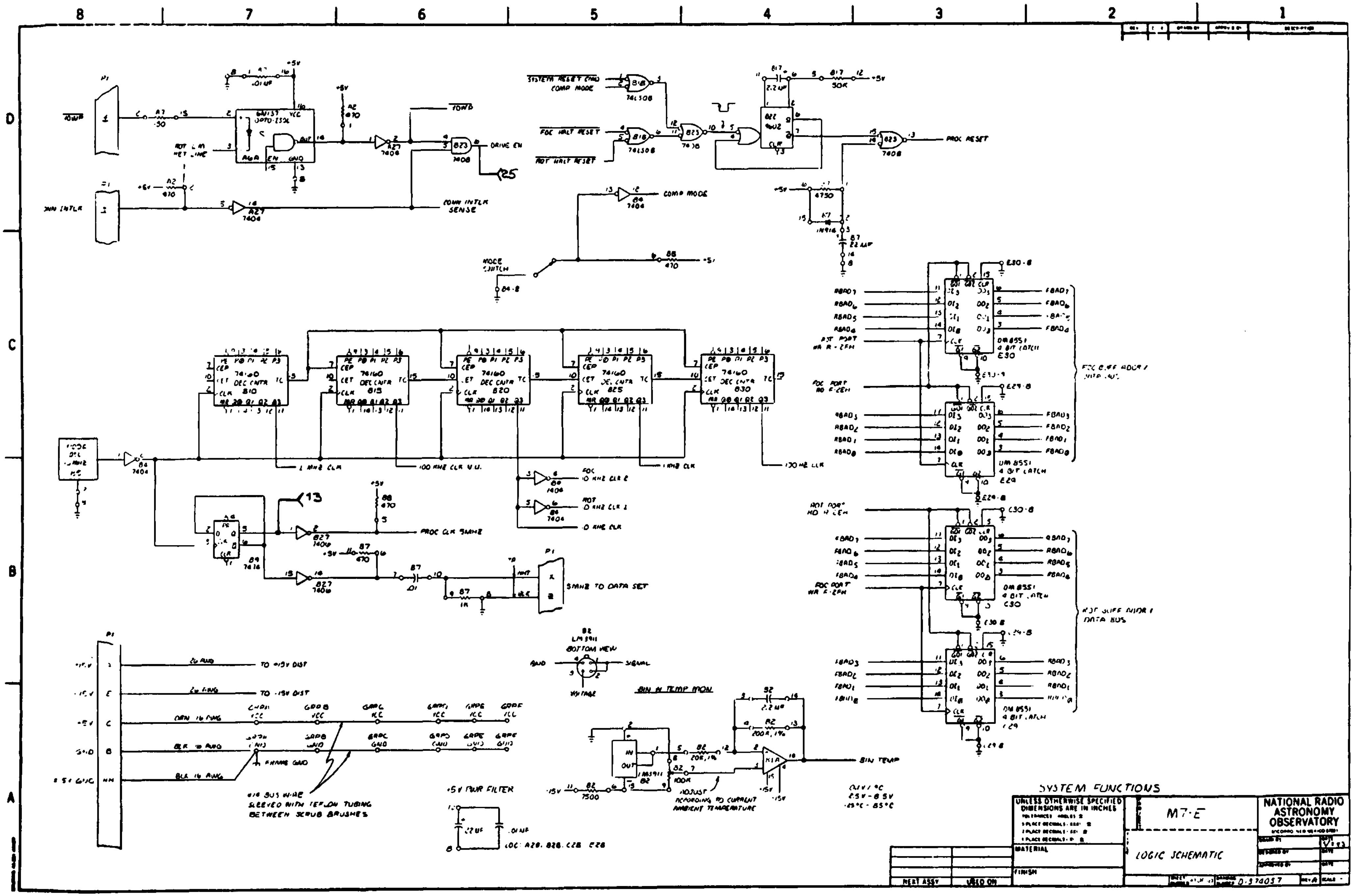
NATIONAL RADIO ASTRONOMY OBSERVATORY

SHEET 7 OF 10 | D1374057



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	M7-E	NATIONAL RADIO ASTRONOMY OBSERVATORY		
MATERIAL	LOGIC SCHEMATIC			
FINISH				
NEXT ASSY	USED ON			


FOC DS STATUS F35H
ROT DS STATUS F38H
STRO·0
SYS RST
MUX ADDR 3
FBAD5
FBAD4
FBAD3
FBAD2
FBAD1
FBAD0
FOC BUFF ADDR / DATA BUS
RBAD5
RBAD4
RBAD3
RBAD2
RBAD1
RBAD0
ROT BUFF ADDR / DATA BUS
74LS138
74LS367
74LS174
HEX LATCH
MON FLAG BIT
CMD FLAG BIT
SYNCHRO CURRENT MONITOR
HI 508
A25
A10
A20
-5V LOOP PWR
ANALOG GND
+15V
-15V
FOC TRANS PWR RTN
ROT TRANS PWR RTN
BIN TEMP
ANALOG OUT
ANALOG DATA TO DATA SET ALGE 3 · 60 m/s
SMA·2
SMA·1
SMA·0
SMA·3
FOC DATA SET INT. RST 7.5
ROT DATA SET INT. RST 7.5
74LS32
74LS08
74LS04
74LS27
74LS38
74LS00
SEL 1 FROM DATA SET
STRO·0 FROM DATA SET
CLR·1 FROM DATA SET
CLEAR·0 CMD FROM DATA SET
DIBO·0 CMD OUTPUT FROM DATA SET
74LS165 E20
74LS165 E19
74LS165 E18
74LS165 C20
74LS165 C19
74LS165 C18
PAR LOAD SHIFT REG FOC DATA LSB
PAR LOAD SHIFT REG FOC DATA MSB
PAR LOAD SHIFT REG ROT DATA LSB
PAR LOAD SHIFT REG ROT DATA MSB
74LS194
UNIV SHIFT REG FOC CMD LSB
UNIV SHIFT REG FOC CMD MSB
UNIV SHIFT REG ROT CMD LSB
UNIV SHIFT REG ROT CMD MSB
FOC DATA
ROT DATA
DIGITAL DATA TO DATA SET
DATA SET CMD DATA SMA & ANALOG INTERFACES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL
FINISH
NEXT ASSY
USED ON
M7-E
LOGIC SCHEMATIC
NATIONAL RADIO ASTRONOMY OBSERVATORY
D-374057


SYSTEM RESET CMD
COMP MODE
FOC HALT RESET
ROT HALT RESET
PROC RESET
DRIVE EN
COMP INTLK SENSE
PROC CLK 5MHZ
5MHZ TO DATA SET
1 MHZ CLK
100 KHZ CLK
+5V PWR FILTER
BIN N TEMP MON
BIN TEMP
SIGNAL
BOTTOM VIEW
FRAME GND
#14 BUS WIRE SLEEVED WITH TEFLON TUBING BETWEEN SCRUB BRUSHES
ADJUST ACCORDING TO CURRENT AMBIENT TEMPERATURE
DM 8551 4 BIT LATCH
74160 DEC CNTR
SYSTEM FUNCTIONS
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
M7-E
NATIONAL RADIO ASTRONOMY OBSERVATORY
LOGIC SCHEMATIC
MATERIAL
FINISH
NEXT ASSY
USED ON
D-374057

3.0 M11 APEX INTERFACE LOGIC

The Apex Interface contains the logic and conversion equipment to sense conditions in the Apex and serially transmit this data to the F/R Controller upon request. Except for the common time base, analog multiplexer-A/D logic and display logic, the logic is partitioned into two independant, asynchronous sections associated with the Focus and Rotation processors in the F/R Controller.

The Apex Interface logic schematics follow this text.

The Apex Interface is powered by a dedicated power supply in the M8 to isolate all Apex signal lines to the Apex Interface. The links between it and the F/R Controller are isolated by optical isolators to protect the balance of the system from disagreeable phenomena associated with lightning.

The Time base logic on Sheet 1 generates system clocks, scan clocks for the multiplexed front panel numeric display, Sample/Hold & A/D Blank/Convert terms and the multiplexer address terms for the analog multiplexer. The A/D conversion sequence operates continuously at a 10 KHz rate and is initiated by -10 (not 10) term which sets flip flop D17 which in turn sets the S/H to the Hold mode, 10 us later the trailing edge of -10 triggers the second half of D17 which initiates the A/D conversion. The A/D -DRDY (A/D EOC) term triggers a one-shot delay pair to provide a delay for the A/D bits to settle. The delay pair generates an A/D load strobe which parallel-loads the A/D data into static storage register D22 & D23 and advances the multiplex address counter D28. The leading edge of the 80 term clocks flip flop D17 off to cause the S/H to revert to the Sample mode so the multiplexer has 45 us of settling time before the next Hold command. When the A/D converter is converting Focus or Rotation velocity data, the converted value is strobed into storage register B18/B19 & C18/C19 for subsequent readout.

The Synchro/Digital Readout Control logic for the two axes are identical, so the following description applies to both sets of logic. This logic causes the position values, A/D data and discretes to be sequentially unloaded to the F/R Controller in response to a data request from the controller via the optical isolator B1. The request sets a control flip flop B30 to initiate the readout sequence and if the A/D is not in the process of conversion, the sequencer control flip flop B30 is triggered on by gate B23. If the A/D converter is busy, the trailing edge of -Sample/Hold turns on B30. This action insures that the data is never read out during the A/D conversion process which takes about 35 us. The sequencer control flip flop B30 inhibits the Rotation Synchro to Digital converter to keep it from converting during data readout and enables a train of ones to travel down shift register B29 which is clocked by a 5 MHZ clock. Four clock pulses later, gate B23 generates a the -Rot Data load strobe which parallel-loads registers B22 through B11 with the A/D data, analog mux address, Apex discretes, Rotation velocity and Rotation position data. On the fifth clock pulse, the shift register Q4 term enables the shift counter (B26&B27) to begin counting and also enables shift clocks to be output by gate B23. The shift clock train unloads the Rotation Data register and provides a load clock to the F/R Controller via differential driver B6. The shift counter shuts down the unload sequence at a count of 64 (it was preset to a count of 21) by clocking control flip flop B30. The four B24 inverters provide about 50 ns of delay in the shift clock to prevent a B30,B29 propagation delay glitch from being output with the clocks. One-shot

D12 is triggered by the -Rot S/D Inh term to provide a discrete front panel indication that the Rotation data readout/conversion process is active.

The data unload time is 9.8 microseconds and the unload logic may be delayed by as much as 35 microseconds due to A/D delay so the maximum readout delay after the data request is 45 us and the minimum is 10 us.

Sheets 2 & 3 are the data unload registers, Apex switch inputs and fault logic. Apex discretes are shown at the top of the sheets and drive Schmidt input inverters for enhanced level discrimination. All discretes are sensed via contact closures to ground and sink .5 ma of current during the non-activated state of the switch. Fault logic senses illegal states such as the concurrent sensing of both Upper and Lower Focus limits or more than one Pin switch. In the event that this sort of immoral (it has happened) behavior is sensed, an alarm term - YOWP! is sent directly to the controller to inhibit all action. Focus and Rotation limits are also sent directly to the controller. Rotation CW/CCW limits are wired in the module and bin inputs but no longer exist in the mount or cabling between the Apex & bin.

Sheet 5 contains the front panel display logic which consists of a 3-line, 10 channel multiplexer to drive the numeric display segment encoder on the display board. The inputs to the multiplexer are the Focus and Rotation position storage registers and the position data is multiplexed by the scan term as a sequence of 10 octal characters. A digit selector, driven by the four bit scan terms enables the cathode of each digit in succession while the anodes are driven by the 7-segment encoder. The Scan counter driven by the 10 KHz scan clock.

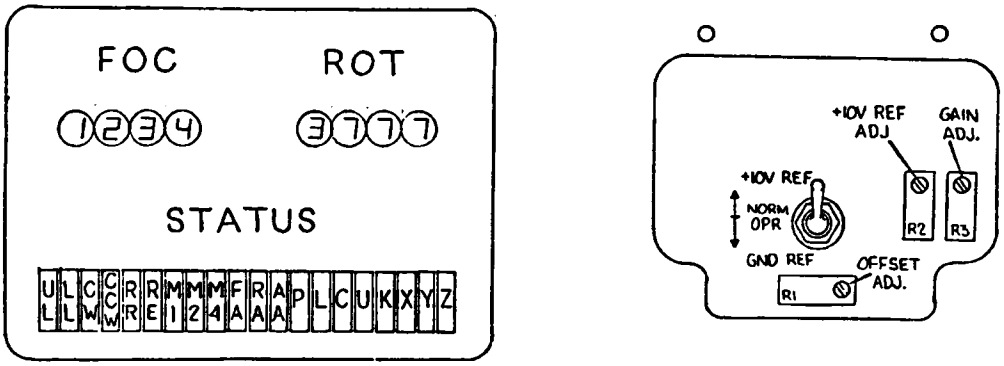
All the analog and conversion circuitry is contained on Sheet 4 and consists of an 8-channel single-ended multiplexer, Sample and Hold, A/D Converter and Integrating Synchro to Digital Converters. The operation of these devices is described in the Data Sheet section of this manual so they will not be described here. For an in-depth discussion of the Integrating Synchro to Digital converter see the DDC "Synchro Conversion Handbook" or the Analog Devices "Synchro & Resolver Conversion" book. The operation of these devices is quite simple and the logic to interact with them was described above. The alignment process for the analog components is quite simple and can be done by removing the front panel adjustment panel cover. The +10 volt reference is set first. A high quality DMM is plugged in to test connector pins 1 & 13 on the front panel connector and pot R2 is adjusted to produce +10 volts +/- 2 mv. Next, momentary switch S1 is actuated down to feed analog ground into the Sample & Hold input to set the A/D zero. Pot R2 is adjusted to produce a 0 volts reading on the Data Tap (set to Mux address 225 or 235, DS#3). Next the switch is actuated up to feed the +10 volt reference voltage into the Sample & Hold input and the A/D gain is adjusted by pot R3 for a +10.000 reading on the Data Tap (addresses 225 & 235). The 10 bit A/D Converter is scaled at 10 mv/bit and is a 10 volt span device so the Data Tap readout will change in steps of 20 mv.

There are no gain or zero adjustments for the S/D converters. Differential amplifiers E15 read out the synchro argument velocity; these should be set for zero output by offset pots E13 & E14 on the bench when synchros and the 400 Hz inputs are connected to the module.

The F/R Mount temperature is sensed by an AD590 temperature sensor

mounted in a metal box bolted to the underside of the F/R Mount gearbox. The temperature verifies the operation of the heaters and is scaled to produce 100 mv/deg C. The scaling and offset resistance values should be set up on the bench before installation in the antenna.

Figure 8 (below) depicts the location of these analog data adjustments and the display messages.



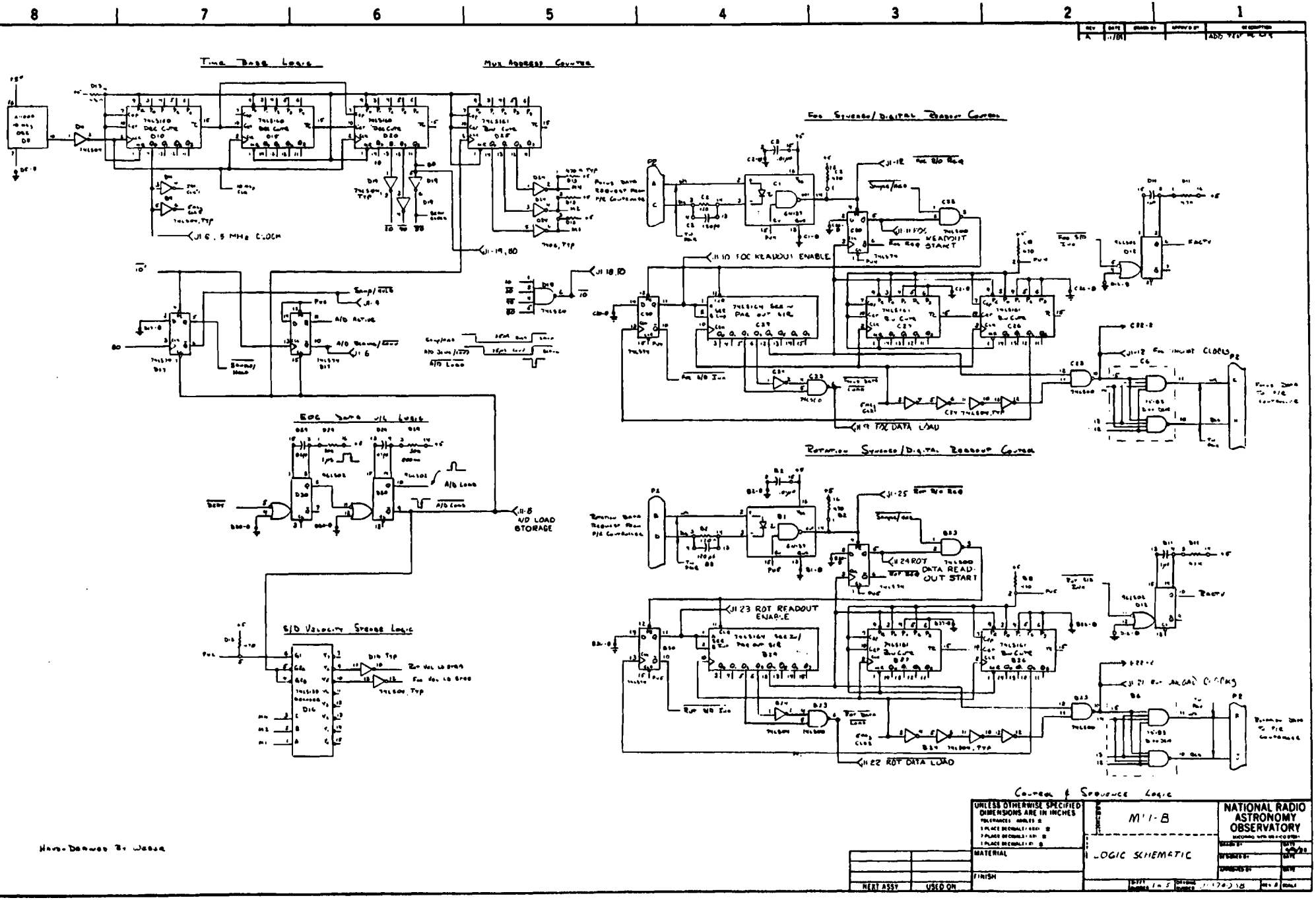
The numeric displays show positions as 4 digit octal values derived from the S/D converter 14 bit straight binary code output; the value may range between 0000 (full DOWN/CCW) and 3777 (full UP/CW). The associated values seen on the Data Tap octal display will be: 2000 and 1777 respectively since the msb is inverted to make the monitor data a 2's complement value.

The discretes display indicate the following when illuminated:

UL & LL - Focus Upper or Lower limit switch actuated
CW & CCW - Rotation CW or CCW limit switch actuated
RR & RE - Ring Retract or Ring Extend switch actuated
M1,M2,M3 - Apex Interface analog mux address bits
FA - Focus Data readout to controller active
RA - Rotation Data readout to controller active
AA - A/D Converter active
P,L,C,U,K,X,Y,Z - Band Pin Switch Actuated (not presently used)

The test point connector permits observation of the following functions:

PIN	FUNCTION	PIN	FUNCTION
1	A/D align switch output	14	analog spare
2	S/H output	15	analog spare
3	YOWP!	16	A/D blank/-conv
4	S/H state	17	A/D data ready
5	-A/D load strobe	18	-10 time base term
6	5 MHZ clock	19	80 time base term
7	Focus output data stream stream	20	Rotation output data stream
8	Focus unload clocks	21	Rotation unload clocks
9	-Focus data load	22	-Rotation data load
10	Focus readout enable	23	Rotation readout enable
11	Focus readout start	24	Rotation readout start
12	Focus readout request	25	Rotation readout request
13	Analog ground		



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL

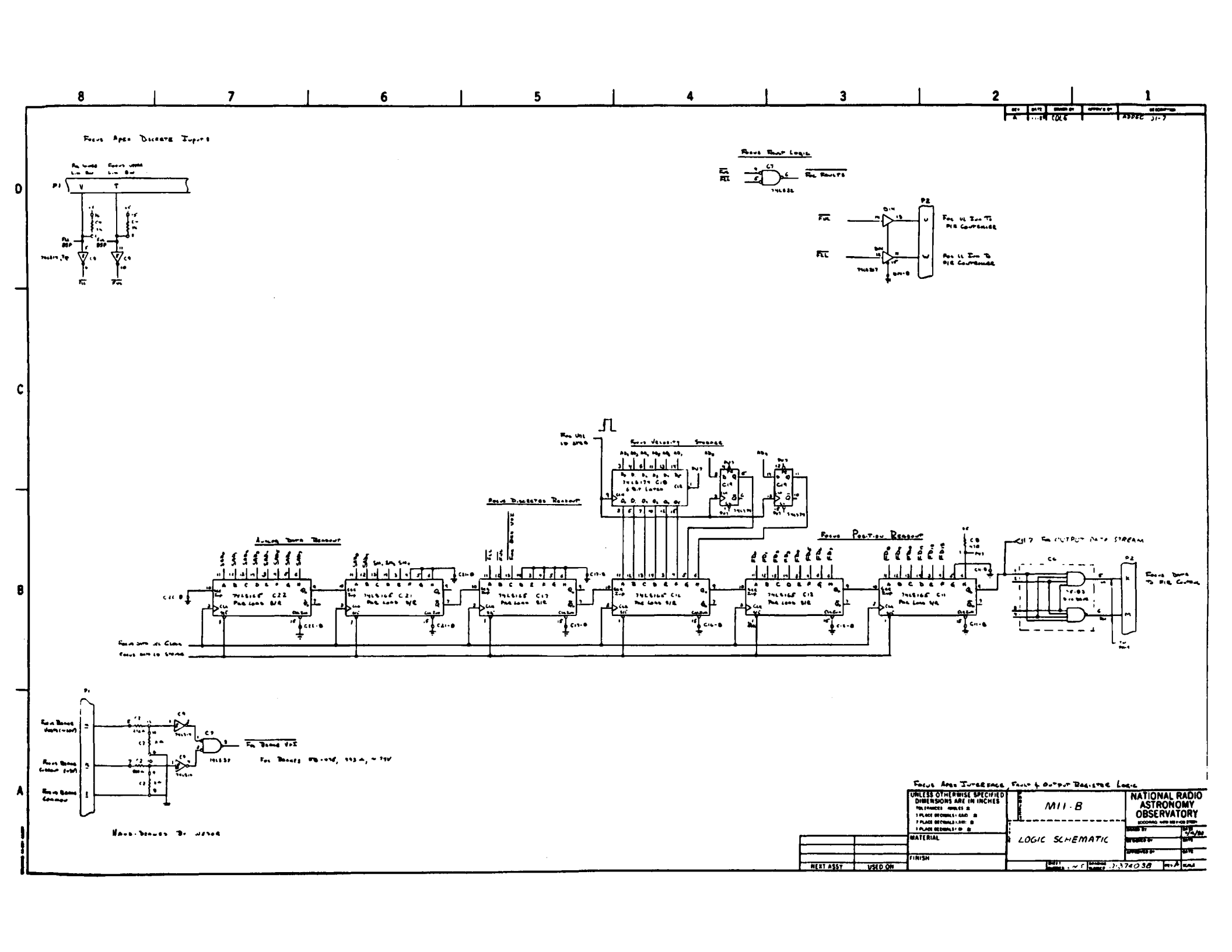
FINISH

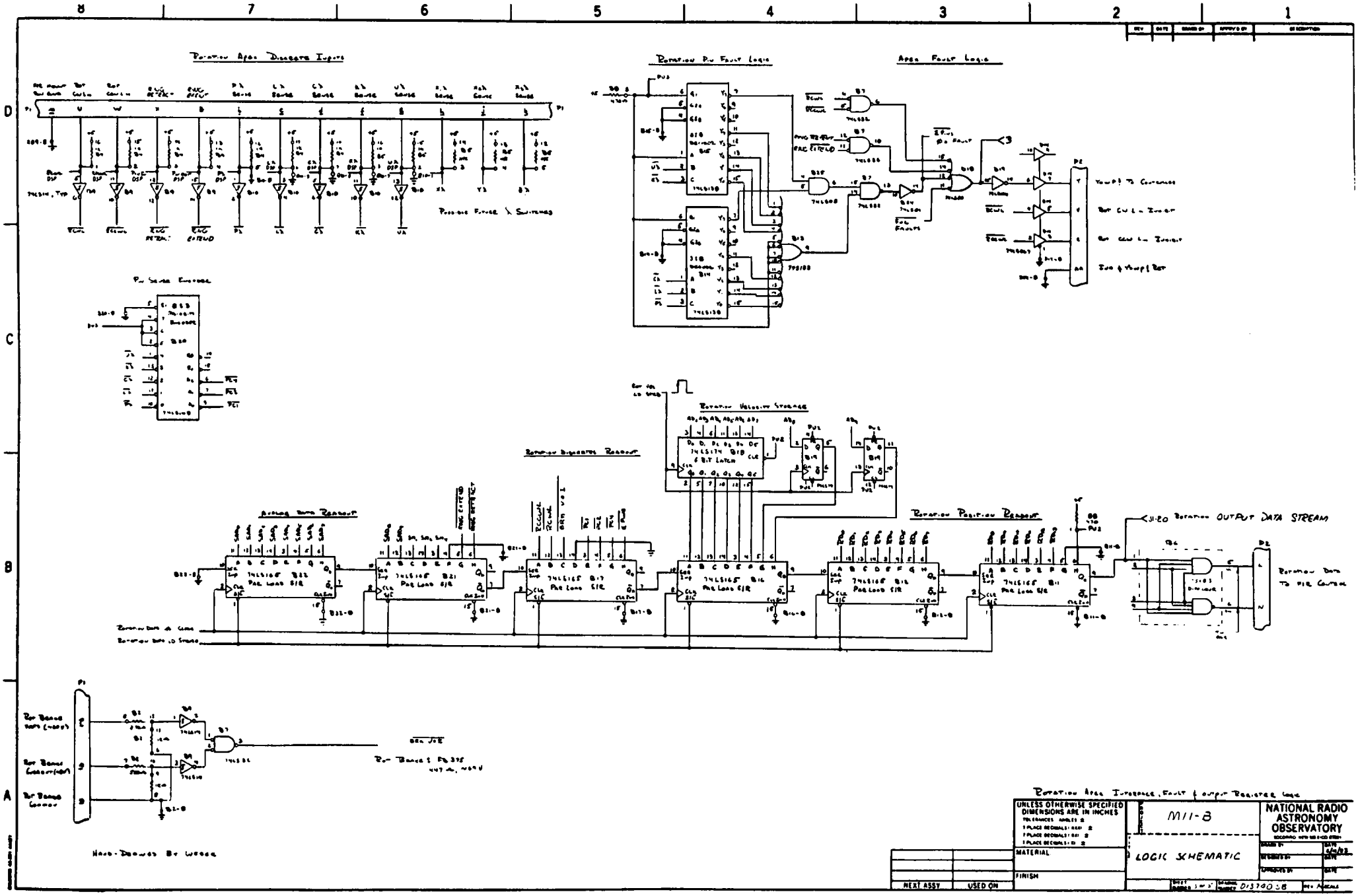
NEXT ASSY | USED ON

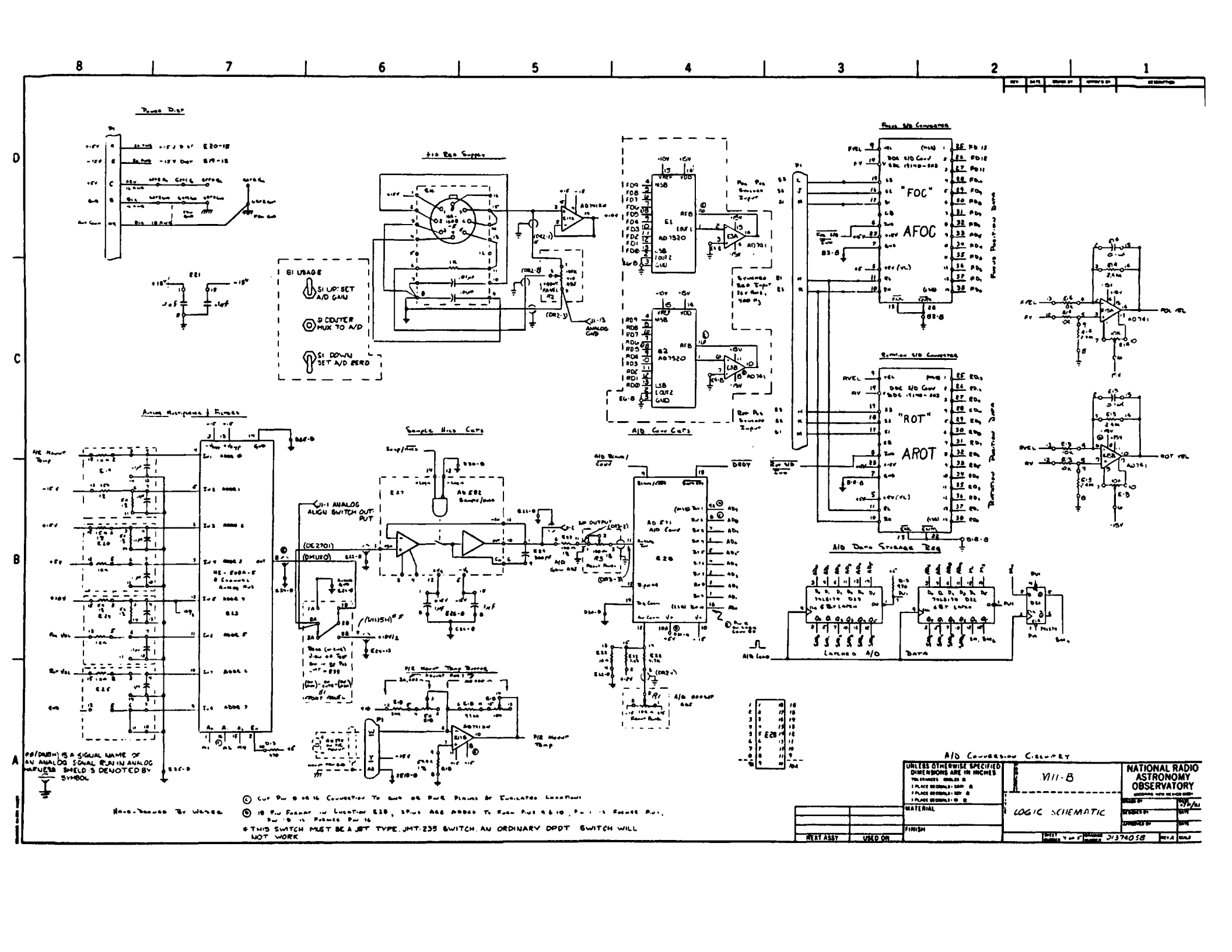
M11-B

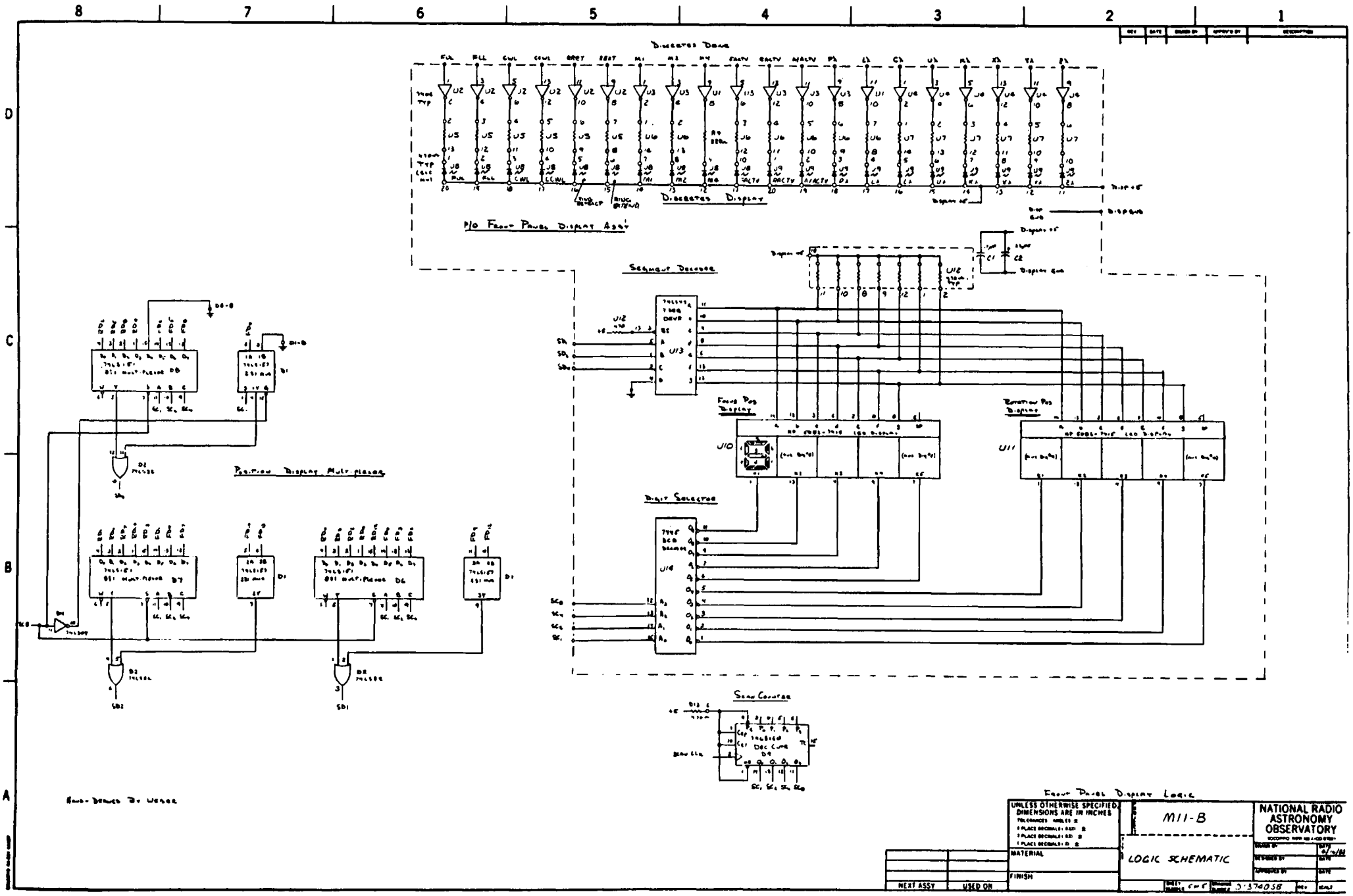
LOGIC SCHEMATIC

NATIONAL RADIO ASTRONOMY OBSERVATORY


Focus Apex Discrete Inputs
Focus Limit Logic
Focus Velocity Storage
Focus Position Register
Analog Data Transmit
Focus Digitizer Register
Focus Apex Interface, Input & Output Register Logic
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL
FINISH
NEXT ASSY
USED ON
M11-B
LOGIC SCHEMATIC
NATIONAL RADIO ASTRONOMY OBSERVATORY


Rotation Area Discrete Inputs
Rotation PU Fault Logic
Area Fault Logic
PU Select Encoder
Rotation Velocity Storage
Rotation Discrete Readout
Analog Data Readout
Rotation Position Readout
J1-20 Rotation OUTPUT DATA STREAM
Rotation Data to PIR Control
Hand-Drawn By Wires
Rotation Area Interface, Fault & Output Register Logic
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL
FINISH
NEXT ASSY
USED ON
M11-B
LOGIC SCHEMATIC
NATIONAL RADIO ASTRONOMY OBSERVATORY
D13790-B


8
7
6
5
4
3
2
1
D
C
B
A
Power Dist
A/D Bus Buffer
SI USAGE
SI UP: SET A/D GAIN
SI CENTER MUX TO A/D
SI DOWN SET A/D ZERO
A/D Gain Ckts
Power A/D Converter
"FOC"
AFOC
"ROT"
AROT
Antenna Multiplexer & Filters
Sample Hold Ckts
A/D Data Storage Reg
Latched A/D Data
A/D Conversion Circuitry
NATIONAL RADIO ASTRONOMY OBSERVATORY
VIII-B
LOGIC SCHEMATIC
D1374058


Discrete Drive
Discretes Display
P/O Front Panel Display Assy
Segment Decode
Front Pos Display
Correlator Pos Display
Digit Selector
Position Display Multiplexer
Scan Counter
Front Panel Display Logic
M11-B
LOGIC SCHEMATIC
NATIONAL RADIO ASTRONOMY OBSERVATORY
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL
FINISH
NEXT ASSY
USED ON
5374058

4.0 M8 F/R POWER SUPPLY

The M8 F/R Power Supply contains the system logic +5, +/- 15 volt and Apex Interface +5 and +/- 15 power supplies. This unit also serves as a control/display panel for processor-driven display LEDs to indicate important discrete states such as Command Active, Translator power on, Brake V*I ok, Up drive line pulsing, etc. Figure 9 depicts the M8 panel and the associated states. Manual control switches enable manual slew control of the Focus and Rotation axes at either a 100 Hz stepping rate or by ramping to travel long distances. Band select switches and associated LEDs enable future manual control of an Index Locking Pin if the need should arise. To reduce wire count the 8 band switches are encoded into a 3 bit code by a 74LS148 encoder on the display board. The F/R Power Supply schematic diagrams follow this text.

The number of DC output lines on the module I/O connector exceeds the number of modules presently powered; the extra wire capacity has been installed for future expansion in the event that more modules are to be installed in the bins.

Monitor States & Controls:

UL/LL - Focus limits
CW/CCW - Rotation limits
UP/DWN -Focus drive dir
CW/CCW - Rot drive dir
BRK - Brake voltage*amps
TRANS - Trans power on
CMD - Command active
MOT - not used
EXT - Ring Extend
RET - Ring Retract

P,L,C,U,K Pin select switches & LEDs, not used
Drive UP/DWN - slew Focus when depressed
Ramp/100 Hz - ramp speed or drive @ 100 Hz
Drive CW/CCW - slew Rot when depressed

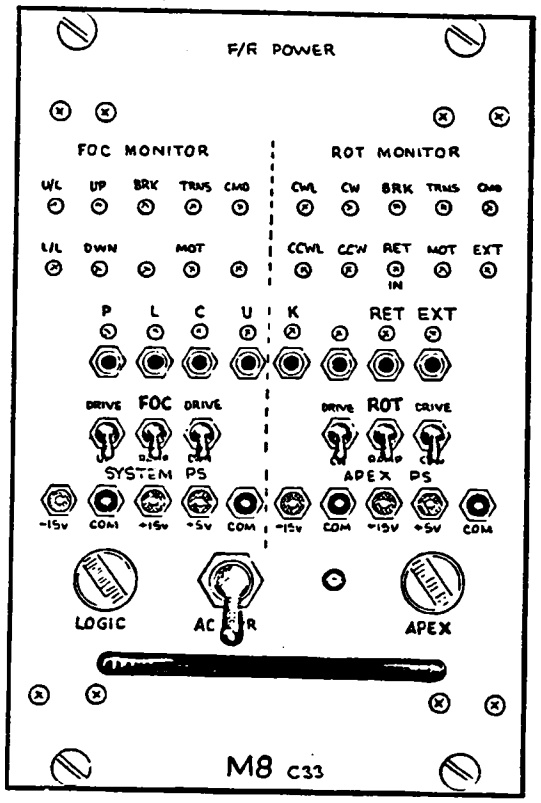
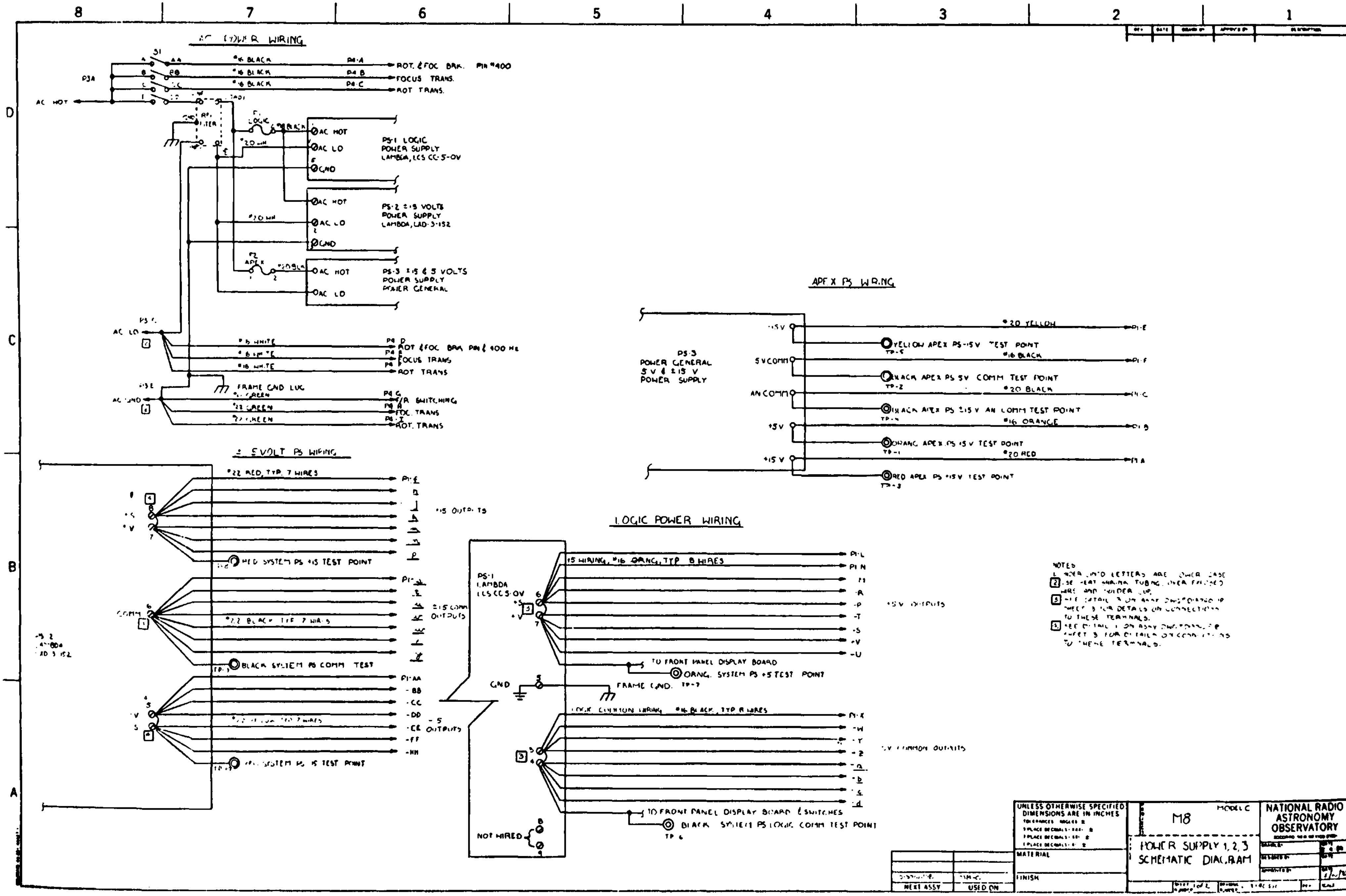
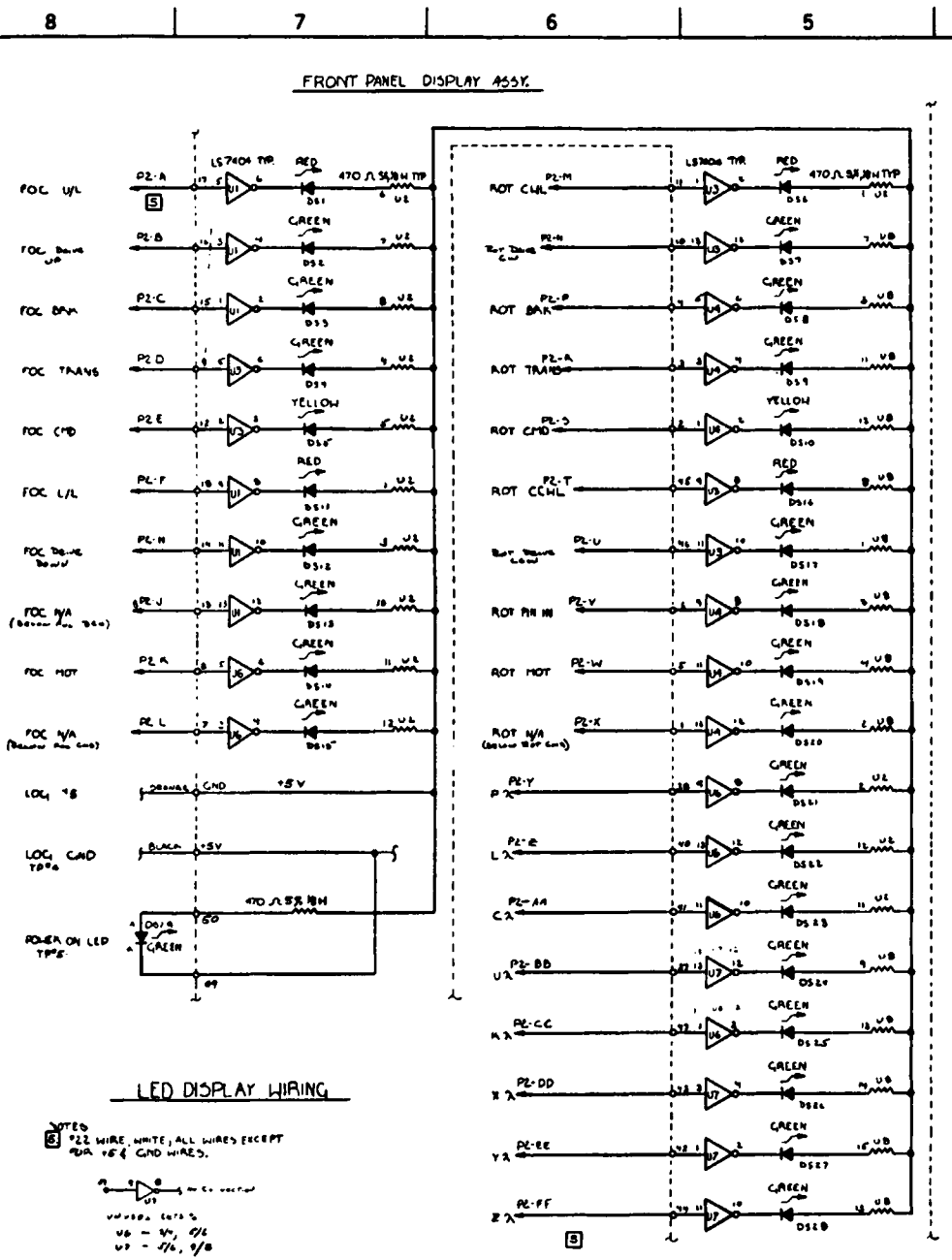


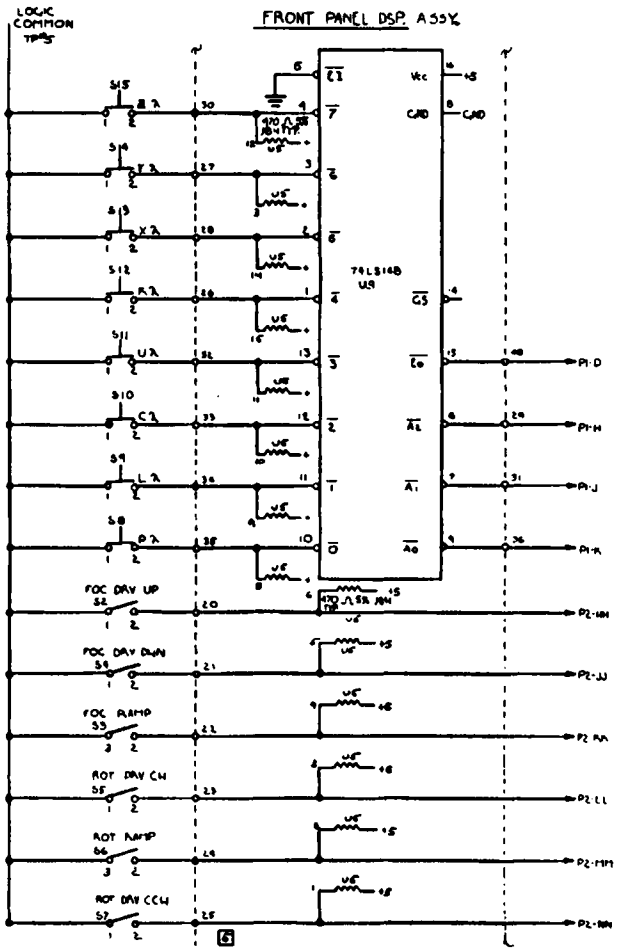
Figure 9, M8 Displays & Controls


AC POWER WIRING
ROT. & FOC. BRK. PIN #400
FOCUS TRANS.
ROT. TRANS.
AC HOT
PS-1 LOGIC POWER SUPPLY LAMBDA, LCS CC-5-OV
PS-2 ±15 VOLTS POWER SUPPLY LAMBDA, LAD-3-152
PS-3 ±15 & 5 VOLTS POWER SUPPLY POWER GENERAL
FRAME GND LUG
APEX PS WIRING
PS-3 POWER GENERAL 5 V & ±15 V POWER SUPPLY
YELLOW APEX PS +15V TEST POINT
BLACK APEX PS 5V COMM TEST POINT
BLACK APEX PS ±15 V AN COMM TEST POINT
ORANG. APEX PS 5 V TEST POINT
RED APEX PS +15V TEST POINT
± 5VOLT PS WIRING
#22 RED, TYP. 7 WIRES
+15 OUTPUTS
RED SYSTEM PS +15 TEST POINT
±15 COMM OUTPUTS
BLACK SYSTEM PS COMM TEST
-5 OUTPUTS
LOGIC POWER WIRING
+5 WIRING, #16 ORANG, TYP. 8 WIRES
+5V OUTPUTS
TO FRONT PANEL DISPLAY BOARD
ORANG. SYSTEM PS +5 TEST POINT
FRAME GND.
LOGIC COMMON WIRING #16 BLACK, TYP. 8 WIRES
5V COMMON OUTPUTS
TO FRONT PANEL DISPLAY BOARD & SWITCHES
BLACK SYSTEM PS LOGIC COMM TEST POINT
NOT WIRED
NOTES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL
FINISH
NEXT ASSY
USED ON
M8
POWER SUPPLY 1, 2, 3 SCHEMATIC DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY



LED DISPLAY WIRING

NOTES
6. #22 WIRE, WHITE; ALL WIRES EXCEPT +5V & GND WIRES.



DISCRETES WIRING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	M8 MODEL C
MATERIAL	POWER SUPPLY SCHEMATIC DIAGRAM
FINISH	NATIONAL RADIO ASTRONOMY OBSERVATORY
NEXT ASSY / USED ON	SHEET 2 OF 2 — DIS7405II

5.0 M22 F/R SWITCHING MODULE

The switching module contains solid state relays to power the Translators, brakes and Ring actuator, Brake controllers to power the F/R Mount brakes and a 400 Hz Synchro Exciter to power the position readout synchros. The relays are optically (internally) isolated and are driven by providing a current sink from an open collector power nand or open collector buffer gate in the F/R Controller logic. The Brake controller is the standard Warner Electric MCS 805 unit which has been removed from the wall of the Pedestal room and installed in the M22 to make them easier to change in the event of failure. During the installation in M22, the output voltage adjustment pot is removed from the Brake Controller PC board and installed on the M22 front panel with longer wires to enable the brake voltage to be adjusted on the front panel. A manual switch and test points on the panel enable manual actuation and adjustment.

The F/R Switching Module schematics follow this text.

BRAKE CONTROLLER ADJUSTMENT PROCEDURE

The following procedure has been abstracted from the Warner Electric MCS-805-1 Manual:

"Brake Release Adjustment: Prior to operating the Fail Safe Brake, the proper electrical release adjustment must be made as follows:

With the brake mounted and ready for operation, turn the potentiometer adjustment screw on the MCS-805-1 Power Supply counterclockwise as far as possible. Turn on power to provide AC input to the power supply. Next, slowly turn the adjustment screw clockwise until the Fail Safe Brake armature completely disengages from the magnet. Armature release and engagement must be checked by hand until the autogap adjustment is made. Using a DC voltmeter, note the voltage reading at this point, which is determined the instant the armature disengages. If this point is overshot by two volts or more, reset the potentiometer to its full counterclockwise position and repeat the adjustment procedure. Complete the set point adjustment by turning the adjustment screw to a setting six volts higher than the disengagement voltage. Lock the adjustment screw by tightening the locknut provided on the potentiometer. This adjustment must be made with the brake at room temperature for an expected operating range of -50 deg F to 250 deg F. The MCS-805-1 control output changes to track the brake release point as it varies over the -50 deg F to 250 deg F temperature range."

The bin cooling fans, brake, 400 Hz Synchro Exciter, Translator and Ring Actuator power are fused and distributed from the M22.

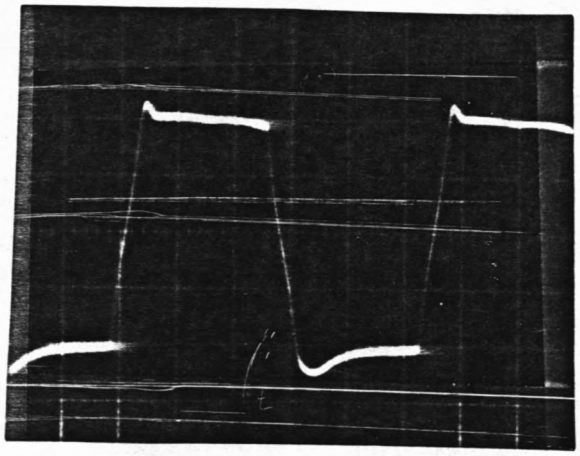
The Synchro Exciter is a 400 Hz power oscillator powered by a 12 volt, 8 amp transformer mounted on the Synchro Exciter Chassis. The exciter circuitry is contained on a removeable PC board mounted on the Synchro Exciter chassis. The exciter circuit consists of a bridge rectifier, 723 voltage regulator, 900 HZ oscillator, flip flop and a push pull, class B power amplifier which drives a 400 Hz, 30 VA, 24V CT (primary) to 26 volt secondary transformer. In operation a DC voltage of about +10 volts (set by a front panel 500 ohm pot) is produced by the 723 regulator; this is the power switching voltage. An LM 340T regulator generates +5 volt logic power for the logic on the board. A 555 timer connected as an oscillator generates a 900 Hz (approximatly) clock which toggles a 7474 to generate a square wave 450 Hz signal which in turn drive 7406 open collector buffers. The 7406s drive 2N2219 transistors which

in turn drive 2N3055 power transistors to produce the power switching signals.

A current transformer (the primary is 9 turns of #26 wire through a Magnetico 13960 current transformer) generate a voltage proportional to the synchro load current. This signal is fed to a rectifier/filter in the M7 where it is read as monitor data. The termination circuit in M7 scales the voltage at 1 volt/synchro load thus enabling a confirmation that currents are present in both synchro rotors.

The front panel synchro excitation level should be set to produce about 20 volts peak; it is not at all critical since the Synchro to Digital converters/synchro combination will operate with voltages as low as 5 volts. Bench tests have confirmed this. An adjustable 25 ohm power resistor is installed in the primary of the transformer to reduce the transformer output voltage so as to lower the dissipation in the regulator circuit. This resistor should set to about 10 ohms. Four 4.7 uf, ceramic capacitors across the transformer secondary (roughly) tune the output circuit to about 400 Hz.

A photograph of the 400 Hz waveform at the M22 front panel test points is shown below. The scales are: 10 volts/div and 500 us/div.



6.0 SYSTEM TROUBLE-SHOOTING

An important system design consideration is the ablity to monitor the conditions in the electronics and the F/R Mount to identify malfunctions and diagnose faults. There are two places in which this is done: locally within the F/R Controller and remotely at the control center via Data Checker and the Operator F/R Overlay. A great deal of diagnostic information is brought back in the Monitor data. This section describes some trouble-shooting guidelines for the system based upon remote observations via the monitor data and direct measurements at the antenna; section 9 describes the usage of the Operator F/R Overlay.

The maintainance technician's credo: THE ESSENCE OF TROUBLE-SHOOTING IS TO OBSERVE THE CONDITIONS OF THE SYSTEM AND RELATE THEM TO THE CONDITIONS WHICH SHOULD EXIST FOR THE MODE OF THE SYSTEM. THIS COMPARISON IS THE ONLY BASIS FOR EFFECTIVE TROUBLE SHOOTING.

A) CHECK COMMUNICATIONS WITH CONTROLLER
This is the most basic aspect of fault isolation.

a. Is analog data present? -- look at mux 0 - 7, power supply voltages, also see MW1.

b. Is analog data within limits? -- check for bad power supplies.

c. Is digital data present? --- examine DS #3, 220 - 227, Foc; 230 - 237, Rot. If missing or bad, send a RESET to restart the processor; does the data reappear? If not the controller is bad or is not hearing the Data Set.

d. Is the digital data reasonable? --- evaluate as shown in D.

B) CHECK FAULT & MODE FLAGS
Are there fault or mode flags coming back from the controller? These are major descriptors of the conditions seen by the F/R Controller.

OPERATOR -- the opertor has sent an out of range Foc command.

CONTROLLER -- the controller has sensed an illegal condition during program execution.

DRIVE -- the mechanism is not driving properly, probably a bad translator, cold sticking, mechanical drag or jam.

TRANSLATOR -- translator did not turn on or off within 1 sec.

BRAKE -- brake voltage*current bad or did turn on or off within 1 sec.

UPPER/LOWER LIMIT -- limit switch activated, should never happen under Computer control, result of some malfunction.

TIMEOUT -- commanded position has not been attained within

allotted time.

APEX INTERFACE DEAD -- Apex Interface has not responded to a data request from F/R Controller.

CABLE INTERLOCK -- a bin I/O cable is loose or disconnected.

SYSTEM -- a system malfunction has been sensed by controller.

RING -- 327 MHz ring is not moving.

APEX ANALOG FAULT -- one of the Apex Interface signals is out of range.

YOWP! -- Some serious fault has been sensed by Apex Interface, all brake, translator & Ring drive is inhibited.

LOCAL mode -- the controller will not accept commands in the LOCAL mode, go set the M7 switch to CMP mode.

APEX INTERFACE DEAD -- the Apex Interface is not responding to data requests from the F/R Controller

CMD ACTIVE -- a position command is being executed

NAP ACTIVE -- position and ring commands are being ignored, send a RESET command to clear NAP mode.

C) CHECK COMMAND-F/R RESPONSE

The analysis of the controller response to a command is a very important aspect of system trouble shooting. The digital monitor data should be examined in these tests as the command and response discretes provide detailed information about what is happening in the system.

a. Send a position command, does ECHO = CMD ?
   - -- yes: command input logic is working, the controller responded to a CMD from the Data Set, interpreted as it properly & initialized the control program.
   - -- no: command not being heard, may be bad F/R Controller, Data Set, Ant Buffer, IF/LO problem.

b. Does a position command cause any drive movement ?
   - -- yes: but slow & with a DRIVE, TRANS or BRAKE fault, check the digital data for conditions. The drive appears to be sticking, check the translator.
   - -- no: & with DRIVE, TRANS or BRAKE faults, indicates a drive problem, bad translator, stuck drive, check the digital data for conditions. Check the translator, wire a substitute motor into the pedastal room junction box. Will it run in the LOCAL mode? Climb up to F/R Mount & disengage motor from the mount, will it run in the LOCAL mode?

c. Will controller accept a NAP command? Test by sending a POSITION command after a NAP command.
   -- no: F/R Controller is not working properly, NAP command is a very simple command to execute.

d. Will the controller accept a soft reset command? (mux 321 & 331). RESET causes Apex data to be all zeros until updated.
   -- no: F/R Controller is not working properly, a soft RESET is the simplest command to execute.

e. Will the controller respond to a hardware RESET command, MUX 337?
   -- no: F/R Controller is really busted.

D) CHECK MONITOR DATA VALUES AND STATES

All discrete control states, all sensible response states and analog monitor data from the F/R Controller and Apex Interface are available for fault analysis. Section 5.0 details the data formats. In general any command will activate several of these control and response discretes; if there is a problem these states should be examined on a Data Tap. If a Position command is to be executed, the translator power, brake, steer up/down (cw/ccw) and clock enable control discretes should be 1's. The clock rate control discretes should sequence through a lot of states if the drive is to be ramped up in speed. The response discretes should show brake V*I,translator power on and drive up/down (cw/ccw) pulsing.

The following analog/digital data values should be examined:

a. Is synchro: = 2 V? -- yes: synchro excitor in M22 is ok
   = 1 V? -- yes: one synchro rotor lead open
   = 0 V? -- yes: synchro excitor in M22 bad or fuse blown

b. Is the position readback stable?
   -- yes: synchro & S/D converter probably working, drive a little, does the position change?
   -- no: S/D converter bad, no synchro excitation or a synchro wiring problem.

c. Is mount temp ~ 10 deg above ambient when ambient is <45 F?
   -- yes: heaters & temp probe ok.
   -- no: mount heaters may not be working, is drive sticking?

d. Is bin temp > 30 deg C?
   -- yes: damage can result, go check the fans.

e. Are power supply voltages within tolerance?
   -- no: go fix the problem.

7.0 TELESCOPE OPERATOR CRT OVERLAY DESCRIPTION

A replica of the new F/R System Overlay is shown below; all fault flags are shown.

```
                    NEW FOCUS/ROTATION AND  (22)

SYSTEM          FOCUS           ROTATION          APEX INTERFACE
LOCAL                                              MOUNT TEMP 16.900
TIMED OUT       NAP             NAP                -15 V    -15.010
SYSTEM FAULT                                       +15 V     15.020
I/O CABLES      UP TRANSL       CW TRANSL           +5 V      5.005
YOWP!           DRIVE PULSES    DRIVE PULSES       +10 V     10.000
RING            LOWER LIMIT                        FOC VEL    0.000
EXTENDED                                           ROT VEL    0.000
                BRAKE           BRAKE              GROUND     0.000
                DRIVE           DRIVE                ANALOGS NOT OK
                TRANSLATOR      TRANSLATOR           INACTIVE
                CONTROLLER      CONTROLLER

                                                   F/R CONTROLLER
POSITION        7469            -3471              +5 V      5.005
COMMAND         7469            -3471              +15 V    15.005
CMD ECHO        7469            -3471              -15 V   -15.010
ERROR              0                0              FOC TRAN  2.600
                                                   ROT TRAN  2.550
                                                   SYNCHRO   2.010
                                                   BIN TEMP  24.00
                                                   GROUND    0.000

F=FOCUS, R=ROTATION, (N=NAP), (RING CMDS) E=EXTEND, W=RETRACT
S=STOP, ESC-M=MASTER CLEAR
```

Section 6.0 of this manual details a fault isolation procedure which may be referred to for an expansion of the the information discussed below.

F/R FAULT MESSAGES

SYSTEM FAULT - The F/R Controller has detected a serious system fault.

I/O CABLES - Some bin I/O cable has been disconnected or is loose.

RING FAULT - The 327 MHz ring has not attained the commanded state within the allotted time.

TIMED OUT - The commanded position has not been attained within the allotted time.

BRAKE - The brake V*I has not reached the commanded state within 1 second.

TRANSLATOR - The translator has not reached the commanded state

within 1 second.

LOCAL - Although not a real malfunction the CMP/LOCAL switch was left in LOCAL. CMP should normally be displayed here.

CONTROLLER - CONTROLLER indicates that the controller has sensed a malfunction in its operation.

ANALOGS NOT OK - Indicates that an Apex Analog fault has been reported by the F/R Controller.

INACTIVE - Indicates that the Apex Interface is not responding to data requests from the F/R Controller. This is a major malfunction

F/R DISCRETES DISPLAY

UP TRANSLATOR - The Focus translator is being driven with UP pulses. Down is the complementary case.

CW TRANSLATOR - The Rotation translator is being driven with CW pulses. CCW is the complementary case.

LOWER LIMIT - The Focus drive has driven to a limit switch, this should never happen under central computer control, something is really wrong. UPPER LIMIT is the complementary case.

RING EXTENDED - The 327 MHz Ring has been extended into position and has actuated the position sensing switch. RING RETRACTED is the complementary case. When the Ring is traveling between the two positions neither switch should be actuated; there is no other readout of Ring position.

NAP - NAP indicates that the processor is ignoring position and ring commands. A RESET command clears this mode.

COMMAND/POSITION DATA

POSITION - POSITION is a decimal value which ranges between + 8191 to - 8192. Typical (Ant 20) Rotation command arguments are: L --xxxx; C --zzzz; K -- yyyy; U -- vvvv; X -- tttt.

COMMAND - COMMAND is the decimal value of the position command set point.

COMMAND ECHO - COMMAND ECHO is the command argument heard by the F/R Controller and is returned as monitor data to verify command reception.

COMMAND ERROR - The controller calculates the difference between the commanded position and the present position; this is read out as monitor data.

APEX INTERFACE ANALOG DATA

MOUNT TEMPERATURE is the temperature sensed on the middle of the bottom of the gear-box and serves to verify that the gear-box and platform heaters are working in cold weather. The heater controller switches on when the ambient temperature is below about 45 deg F. The temperature readout is in degrees C and should be about 10 deg C above ambient when the ambient is below 45 F. When the F/R Mount temperature drops below 0 deg, the controller signals an Apex Analog fault.

APEX INTERFACE POWER SUPPLIES indicate the voltages which operate this interface. The +/- 15 volts should be within +/- .3 volts and the +5 volt tolerance is +/- .15 volts. The +10 volt tolerance is +/- 0.040 volts. This data has a granularity of .020 volts/bit. Ground is a measure of A/D zero drift and should be less than +/- 0.040 volts. Foc and Rot velocities are a measure of drive velocity and are scaled 13 volts/in/sec for Focus and 5.2 volts/deg/sec for Rotation.

F/R CONTROLLER ANALOG DATA

F/R POWER SUPPLIES indicate the voltages which operate the F/R Controller and associated logic. The +/- 15 volts should be within +/- .1 volt and the +5 should be within +/- .2 volts. The translator power should be +2.6 +/- .2 volts. These translator voltages are present only during command execution. The Synchro voltage should read +2 +/- .5 volts. Ground is a measure of the Data Set A/D zero drift and should be less than +/ .010 volts. Bin temperature reads out directly in deg C and should be less than 30 deg.

8.0 CONTROL/DATA FORMATS

Mux refers to the multiplex address in octal format. RAM loc denotes the byte symbolic address in RAM memory.

COMMAND FORMATS:

Mux addr	320/Foc	330/Rot	336/Ring
Ram loc	rampas	rampas	none
Data	null	null	null
b23 80H	0	0	0
b22 40H	0	0	0
b21 20H	0	0	0
b20 10H	0	0	0
b19 08H	0	0	0
b18 04H	0	0	0
b17 02H	0	0	0
b16 01H	0	0	0
Ram loc	rampbs	rampbs	none
Data	Foc arg	Rot arg	null
b15 80H	0	0	0
b14 40H	0	0	0
b13 20H	2**13,msb	2**13,msb	0
b12 10H	2**12	2**12	0
b11 08H	2**11	2**11	0
b10 04H	2**10	2**10	0
b9 02H	2**9	2**9	0
b8 01H	2**8	2**8	0
Ram loc	rampcs	rampcs	none
Data	Foc arg	Rot arg	Ring arg
b7 80H	2**7	2**7	0
b6 40H	2**6	2**6	0
b5 20H	2**5	2**5	0
b4 10H	2**4	2**4	0
b3 08H	2**3	2**3	0
b2 04H	2**2	2**2	0
b1 02H	2**1	2**1	0
b0 01H	2**0	2**0	ext/ret, 1=ext

A SYSTEM RESET command (Mux 337)causes abortion of active commands and re-initiallizes the two processors. A software RESET command (Mux 321 & 331) resets the addressed processor. The control argument is not used in RESET commands.

NAP commands (Mux 322/Foc & 332/Rot) cause all subsequent position commands to be ignored until cancelled by a RESET command. The command argument is not used.

DIGITAL MONITOR DATA

Digital monitor data formats are a composite of values and associated discrete or fault data. A 1 in a fault bit denotes a fault state.

Focus Digital Monitor Data:

Mux addr	220/Foc	221/Foc	222/Foc
Ram loc	posd+2	erro+2	echo+2
Data	faults	modes	null
b23 80H	operator	0	0
b22 40H	controller	cmd active	0
b21 20H	drive	nap active	0
b20 10H	translator	timeout	0
b19 08H	synchro, = 0	Apex Int dead	0
b18 04H	brake	cable int'lk *	0
b17 02H	upper lim	system *	0
b16 01H	lower lim	cmp/loc, 0 = loc	0
Ram loc	posd+1	erro+1	echo+1
Data	Foc pos	Foc pos error	Foc cmd echo
b15 80H	0	0	Cmd bit echoed
b14 40H	0	0	Cmd bit echoed
b13 20H	2**13, msb	2**13, msb	2**13, msb
b12 10H	2**12	2**12	2**12
b11 08H	2**11	2**11	2**11
b10 04H	2**10	2**10	2**10
b9 02H	2**9	2**9	2**9
b8 01H	2**8	2**8	2**8
Ram loc	posd	erro	echo
Data	Foc pos	Foc pos error	Cmd echo
b7 80H	2**7	2**7	2**7
b6 40H	2**6	2**6	2**6
b5 20H	2**5	2**5	2**5
b4 10H	2**4	2**4	2**4
b3 08H	2**3	2**3	2**3
b2 04H	2**2	2**2	2**2
b1 02H	2**1	2**1	2**1
b0 01H	2**0	2**0	2**0

* 1 = no fault, low true

Mux	223/Foc	224/Foc	225/Foc
Ram loc	dscr+2	adcr+2	anad+2
Data	clock control	Apex Foc Discr	Apex Anlg Faults
b23 80H	2**7,msb	0	gnd
b22 40H	2**6	0	0
b21 20H	2**5	0	foc vel
b20 10H	2**4	0	+10 volts
b19 08H	2**3	0	+5 volts
b18 04H	2**2	Foc brk V*I	+15 volts
b17 02H	2**1	Foc upper lim	-15 volts
b16 01H	2**0	Foc lower lim	mount temp
Ram loc	dscr+1	adcr+1	anad+1
Data	cmd sense	Foc vel	Apex analog data
b15 80H	Foc trans pwr	0	0
b14 40H	Foc brake pwr	0	Mux addr 4
b13 20H	0	0	Mux addr 2
b12 10H	0	0	Mux addr 1
b11 08H	Foc drv up	2**11,msb	2**11,msb
b10 04H	Foc drv down	2**10	2**10
b9 02H	0	2**9	2**9
b8 01H	Foc clock en	2**8	2**8
Ram loc	dscr	adcr	anad
Data	activity sense	Foc vel	Apex analog data
b7 80H	motor pulsing,=0	2**7	2**7
b6 40H	down pulsing	2**6	2**6
b5 20H	up pulsing	2**5	2**5
b4 10H	trans pwr mon	2**4,lsb	2**4
b3 08H	0	0	2**3
b2 04H	cable intl'k	0	2**2,lsb
b1 02H	Yowp!	0	0
b0 01H	loc/comp	0	0

Rotation Digital Monitor Data:

Mux	230/Rot	231/Rot	232/Rot
Ram loc	posd+2	erro+2	echo+2
Data	faults	modes	Ring mon
b23 80H	operator	ring active	0
b22 40H	controller	cmd active	0
b21 20H	drive	nap active	0
b20 10H	translator	timeout	0
b19 08H	synchro, =0	Apex Int dead	0
b18 04H	brake	cable int'lk *	ring fault
b17 02H	0	system *	ring retract
b16 01H	0	cmp/loc, 0=loc	ring extend
Ram loc	posd+1	erro+1	echo+1
Data	Rot pos	Rot pos error	Rot cmd echo
b15 80H	0	0	Cmd bit echoed
b14 40H	0	0	Cmd bit echoed
b13 20H	2**13,msb	2**13,msb	2**13,msb
b12 10H	2**12	2**12	2**12
b11 08H	2**11	2**11	2**11
b10 04H	2**10	2**10	2**10
b9 02H	2**9	2**9	2**9
b8 01H	2**8	2**8	2**8
Ram loc	posd	erro	echo
Data	Rot pos	Rot pos error	Rot cmd echo
b7 80H	2**7	2**7	2**7
b6 40H	2**6	2**6	2**6
b5 20H	2**5	2**5	2**5
b4 10H	2**4	2**4	2**4
b3 08H	2**3	2**3	2**3
b2 04H	2**2	2**2	2**2
b1 02H	2**1	2**1	2**1
b0 01H	2**0	2**0	2**0

* 1 = no fault, low true

Mux	233/Rot	234/Rot	235/Rot
Ram loc	dscr+2	adcr+2	anad+2
Data	clock control	discretes	apex an faults
b23 80H	2**7, msb	sum pins, =0	gnd
b22 40H	2**6	pc4, =0	rot vel
b21 20H	2**5	pc2 "	0
b20 10H	2**4	pc1 "	+10 volts
b19 08H	2**3	0	+5 volts
b18 04H	2**2	brake V*I	+15 volts
b17 02H	2**1	Rot cw lim, =0	-15 volts
b16 01H	2**0	Rot ccw lim, =0	mount temp
Ram loc	dscr+1	adcr+1	anad+1
Data	cmd sense	rot vel	apex analogs
b15 80H	Rot trns pwr	0	0
b14 40H	Rot brk pwr	0	ana mux 4
b13 20H	Ring ret pwr	0	ana mux 2
b12 10H	Ring ext pwr	0	ana mux 1
b11 08H	Rot drv cw	2**12,msb	2**12, msb
b10 04H	Rot drv ccw	2**11	2**11
b9 02H	0	2**10	2**10
b8 01H	Rot clk en	2**9	2**9
Ram loc	dscr	adcr	anad
Data	activity sense	rot vel	apex analogs
b7 80H	mot pulsing	2**8	2**8
b6 40H	ccw pulsing	2**7	2**7
b5 20H	cw pulsing	2**6	2**6
b4 10H	trans pwr mon	2**5,lsb	2**5
b3 08H	0	0	2**4
b2 04H	cable intl'k	0	2**3
b1 02H	Yowp!	0	2**2,lsb
b0 01H	loc/comp	0	0

ANALOG MONITOR DATA:

Mux	Parameter	Nominal Value & Tolerance
0H	5 logic pwr	+5 volts, +/- .2 volts.
1H	analog gnd	0 volts +/- 10 mv.
2H	+15 volts/2	+7.5 volts +/- 100 mv.
3H	-15 volts/2	-7.5 volts +/- 100 mv.
4H	Foc Trans pwr	+2.5 volts +/- .2 volts
5H	Rot Trans pwr	+2.5 volts +/- .2 volts
6H	Bin Temp	.1 volt/deg C
7H	Synchro current	+2.5 volts +/- 1 volt

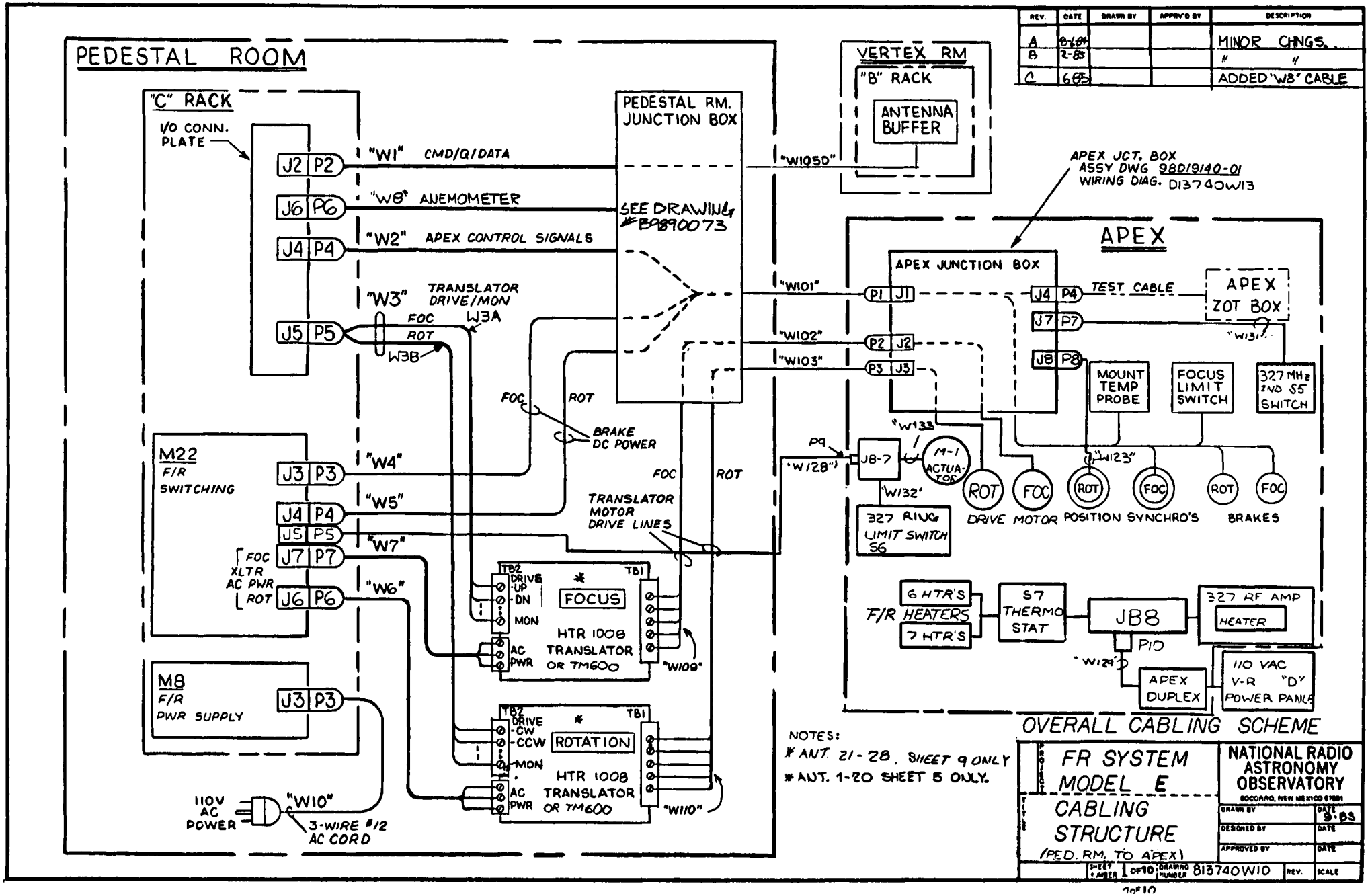
SPECIAL PURPOSE MONITOR DATA

Fault monitor data is a selection of the data listed above which has been formatted to combine all fault data into one single word for convenience in examining fault bits. The F/R Mount temperature data has been put into a dedicated monitor word for convenience in driving a strip chart recorder.

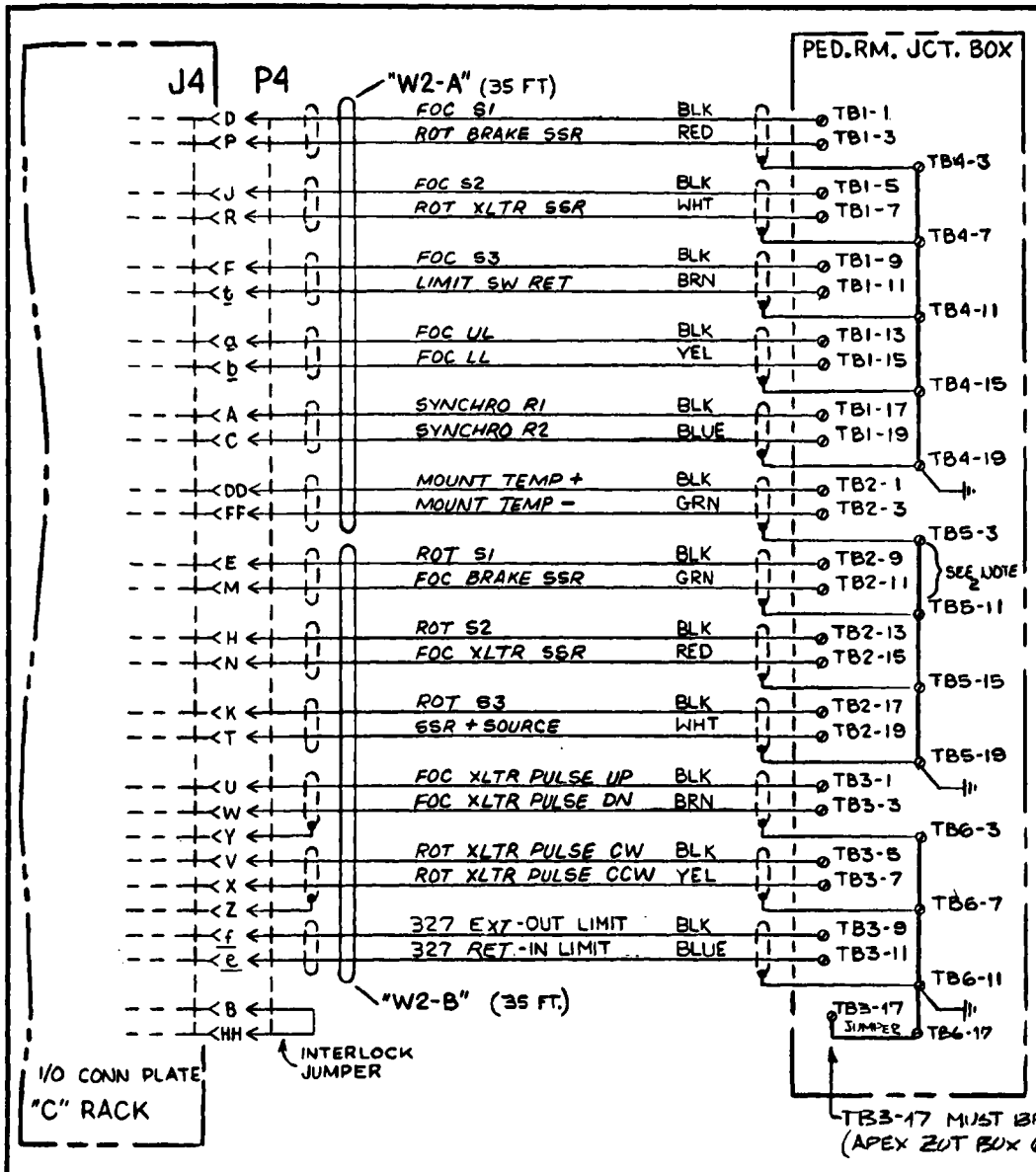
Focus and Rotation Special Purpose Monitor Data

Mux addr	226/Foc	236/Rot	227/Foc
Ram loc	faul+2	faul+2	temp+2
Data	faults	faults	F/R Mount Temp
b23 80H	lab test	lab test	0
b22 40H	lab test	lab test	0
b21 20H	lab test	lab test	0
b20 10H	timeout	timeout	0
b19 08H	Apex Int dead	Apex Int dead	0
b18 04H	cable Int'lk	cable Int'lk	0
b17 02H	system	system	0
b16 01H	Motion Analysis	Motion Analsis	0
Ram loc	faul+1	faul+1	temp+1
Data	Apex Analog	Apex Analog	F/R Mount Temp
b15 80H	gnd	gnd	0
b14 40H	0	0	0
b13 20H	Foc vel	Rot vel	0
b12 10H	+10 volts	+10 volts	0
b11 08H	+5 volts	+5 volts	2**11,msb
b10 04H	+15 volts	+15 volts	2**10
b9 02H	-15 volts	-15 volts	2**9
b8 01H	mount temp	mount temp	2**8
Ram loc	faul	faul	temp
Data	faults	faults	F/R Mount Temp
b7 80H	operator	operator	2**7
b6 40H	controller	controller	2**6
b5 20H	drive	drive	2**5
b4 10H	translator	translator	2**4
b3 08H	synchro, = 0	synchro, = 0	2**3
b2 04H	brake	brake	2**2,lsb
b1 02H	upper lim	0	0
b0 01H	lower lim	0	0

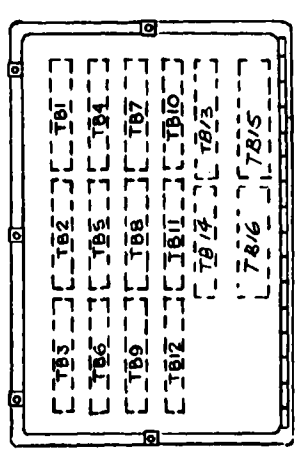
9.0 SYSTEM CABLE DRAWINGS, TRANSLATOR SCHEMATICS & MOTOR DRIVE WAVEFORMS

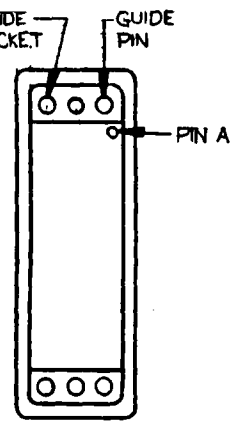


REV.	DATE	DRAWN BY	APPR'D BY	DESCRIPTION
A	6-84			MINOR CHNGS.
B	2-85			" "
C	6-85			ADDED "W8" CABLE



PEDESTAL ROOM JUNCTION BOX





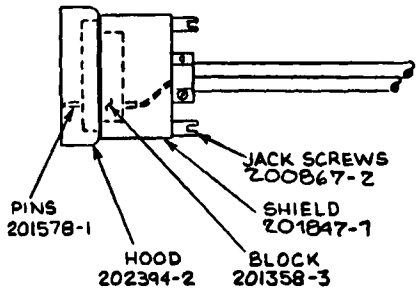
LOOKING AT FRONT OF CONNECTOR

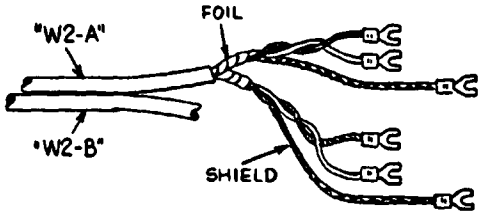
NOTES:
1. 327 FEED INSTALLED ON ANT. 13, 20, & 21 ONLY.
2. WIRES MUST BE RELOCATED UPON REWIRE FOR SYLCHRO EXS. FROM TB3-17-19

CABLE ASSY "W2"

BELDEN #8778 OR EQUIV.
6 SHIELDED PAIRS PER CABLE
(2 REQ'D)

P4
AMP 50 PIN PLUG





APEX CONTROL SIGNALS

REV	DATE	DRAWN BY	APPR'D BY	DESCRIPTION
B	6-88			TB3-17 JUMPER ADDED
A	2-85			ADDED NOTE 2

VLA

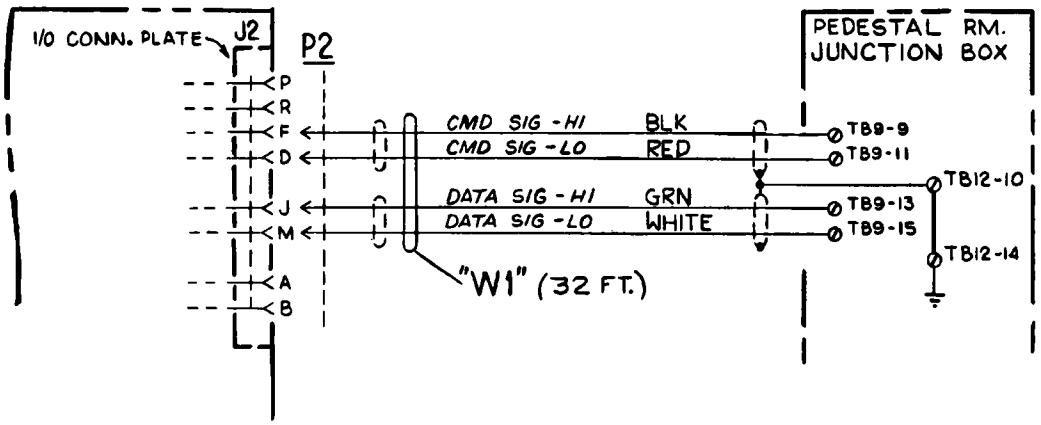
FR SYSTEM MODEL "E"

CABLING STRUCTURE

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

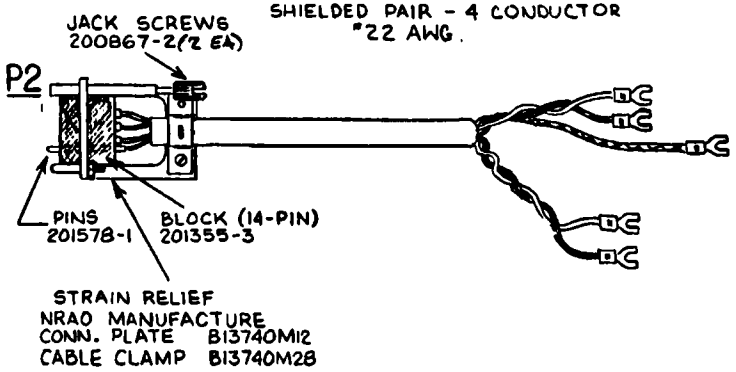
DRAWN BY — DATE 2-83
DESIGNED BY — DATE
APPROVED BY — DATE

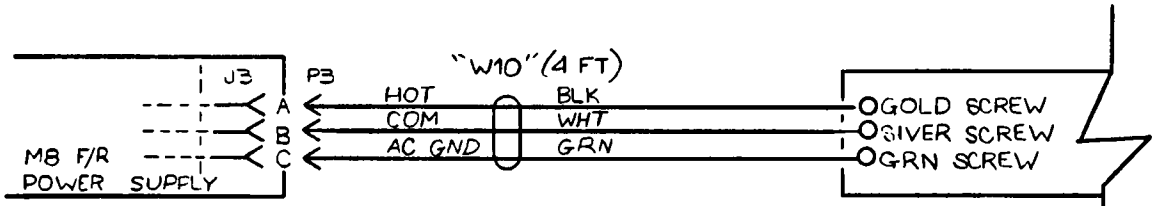
SHEET NUMBER 2 OF 10 | DRAWING NUMBER B13740W10 | REV | SCALE



CABLE "W1"

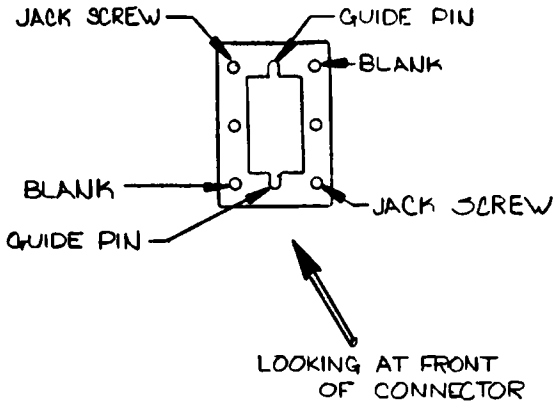
BELDEN #8723 OR EQUIV.
SHIELDED PAIR - 4 CONDUCTOR
#22 AWG.





P3 CONNECTOR MS3108A-24-10S
CABLE CLAMP MS3057A-16A
CABLE 12 AWG S.O.

HUBBLE TIWST LOCK
AC CONNECTOR 30 A



W10 POWER CABLE AND CMD/MON LINES

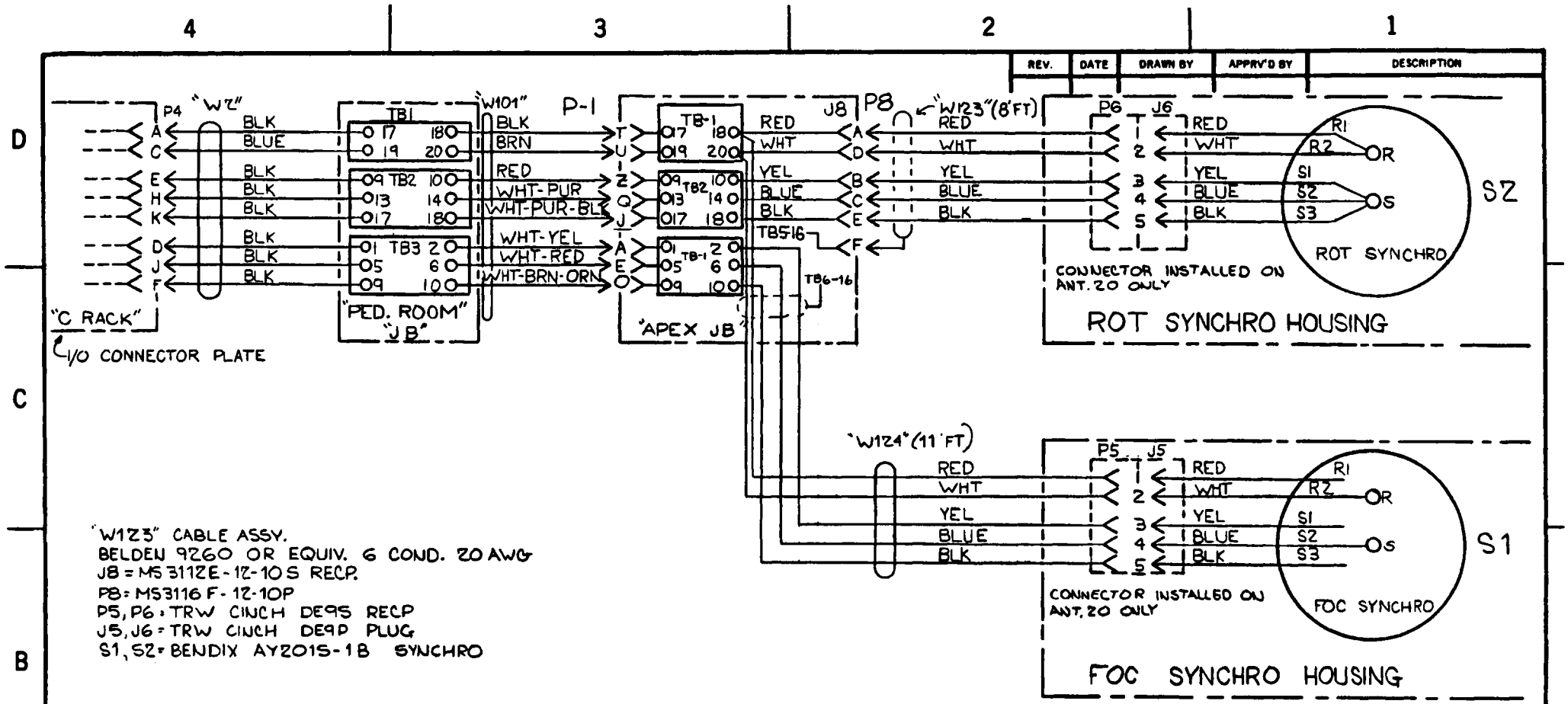
REV	DATE	DRAWN BY	APPR'D BY	DESCRIPTION
C	2-85			CHG. "W1" CABLE
B	8288			DRAWN AS WIRED

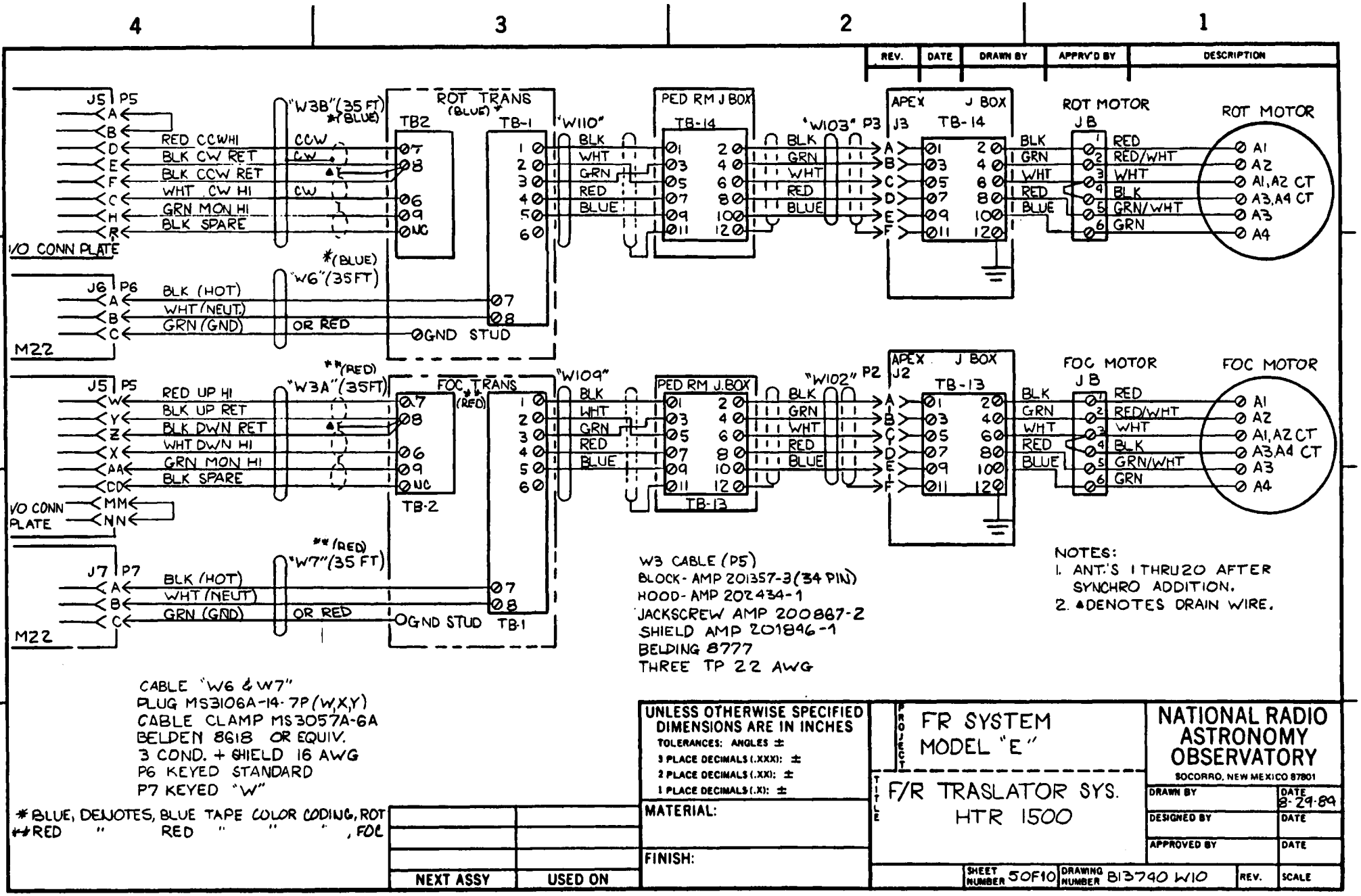
FR SYSTEM
MODEL "E"
CABLING
STRUCTURE

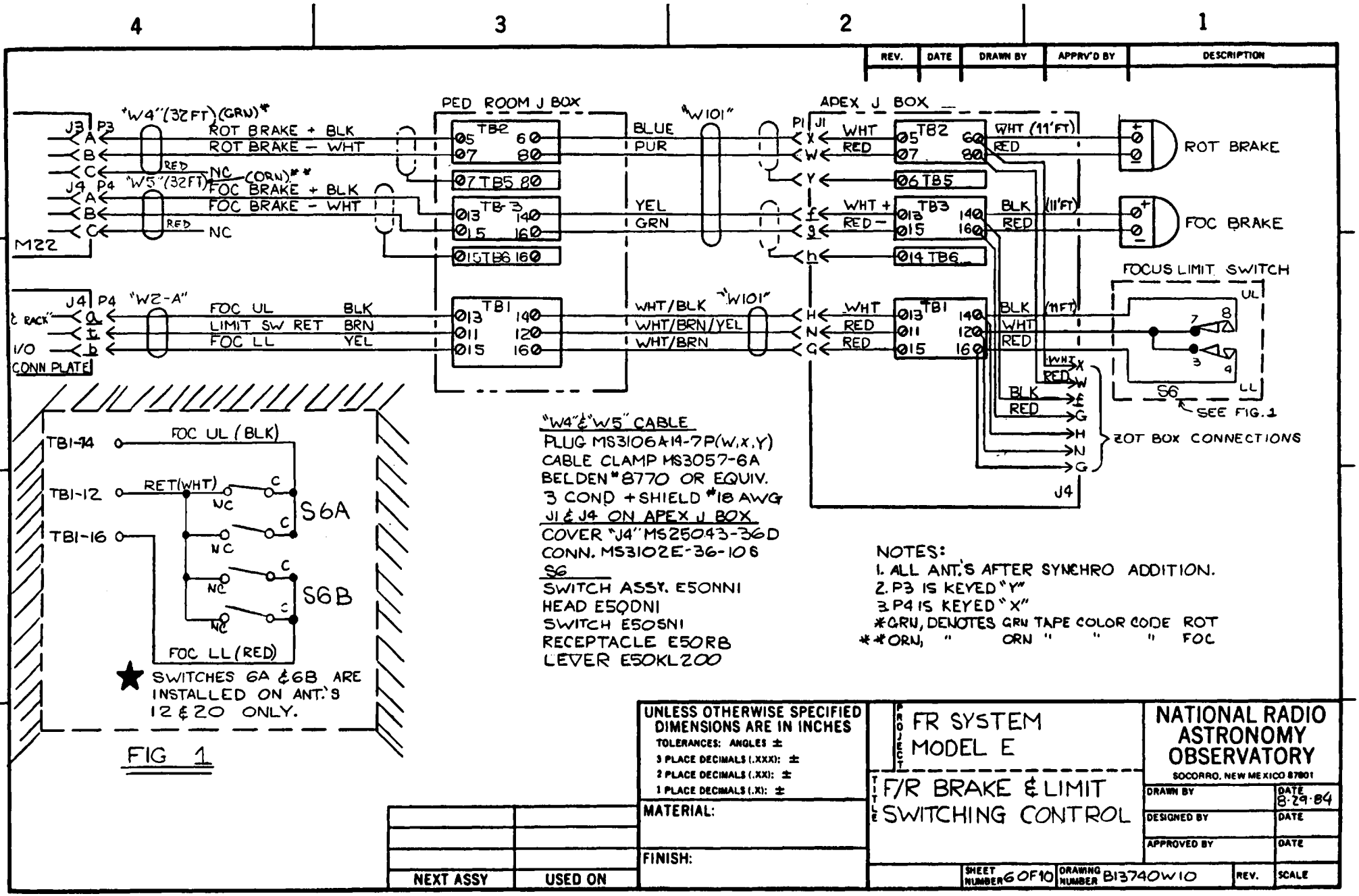
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY — DATE 9-83
DESIGNED BY — DATE
APPROVED BY — DATE

SHEET NUMBER 3 OF 10 | DRAWING NUMBER B13740W10 | REV. | SCALE


4
3
2
1
D
C
B
A
REV.
DATE
DRAWN BY
APPR'D BY
DESCRIPTION
P4
"W2"
BLK
BLUE
BLK
BLK
BLK
BLK
BLK
BLK
A
C
E
H
K
D
J
F
TB1
017 180
019 200
09 TB2 100
013 140
017 180
01 TB3 20
05 60
09 100
"W101"
BLK
BRN
RED
WHT-PUR
WHT-PUR-BLK
WHT-YEL
WHT-RED
WHT-BRN-ORN
P-1
T
U
Z
Q
J
A
E
O
TB-1
017 180
019 200
09 TB2 100
013 140
017 180
01 TB-1 20
05 60
09 100
J8
P8
"W123" (8'FT)
RED
WHT
YEL
BLUE
BLK
TB5-16
F
TB6-16
"C RACK"
I/O CONNECTOR PLATE
"PED. ROOM"
"JB"
"APEX JB"
P6
J6
RED
WHT
YEL
BLUE
BLK
1
2
3
4
5
RI
R2
OR
SI
S2
S3
OS
S2
ROT SYNCHRO
CONNECTOR INSTALLED ON ANT. 20 ONLY
ROT SYNCHRO HOUSING
"W124" (11'FT)
P5
J5
RED
WHT
YEL
BLUE
BLK
1
2
3
4
5
RI
R2
OR
SI
S2
S3
OS
S1
FOC SYNCHRO
CONNECTOR INSTALLED ON ANT. 20 ONLY
FOC SYNCHRO HOUSING
"W123" CABLE ASSY.
BELDEN 9260 OR EQUIV. 6 COND. 20 AWG
J8 = MS 3112E-12-10S RECP.
P8 = MS3116 F-12-10P
P5, P6 = TRW CINCH DE9S RECP
J5, J6 = TRW CINCH DE9P PLUG
S1, S2 = BENDIX AYZ01S-1B SYNCHRO
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
NEXT ASSY
USED ON
PROJECT
FR SYSTEM
MODEL E
TITLE
FR SYNCHRO SYSTEM
W123,
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY
DATE 8-28-84
DESIGNED BY
DATE
APPROVED BY
DATE
SHEET NUMBER 4 OF 10
DRAWING NUMBER B13740W10
REV.
SCALE


4
3
2
1
D
C
B
A
REV. DATE DRAWN BY APPRV'D BY DESCRIPTION
J5 P5
RED CCWHI
BLK CW RET
BLK CCW RET
WHT CW HI
GRN MON HI
BLK SPARE
I/O CONN PLATE
"W3B" (35 FT) *(BLUE)
CCW
CW
CW
ROT TRANS (BLUE)*
TB2
TB-1
"W110"
BLK
WHT
GRN
RED
BLUE
PED RM J BOX
TB-14
"W103" P3
APEX J BOX
J3 TB-14
ROT MOTOR
J B
RED
RED/WHT
WHT
BLK
GRN/WHT
GRN
A1
A2
A1,A2 CT
A3,A4 CT
A3
A4
J6 P6
BLK (HOT)
WHT (NEUT.)
GRN (GND)
OR RED
GND STUD
M22
*(BLUE)
"W6" (35FT)
J5 P5
RED UP HI
BLK UP RET
BLK DWN RET
WHT DWN HI
GRN MON HI
BLK SPARE
I/O CONN PLATE
MM
NN
**(RED)
"W3A" (35FT)
FOC TRANS (RED)*
TB-2
"W109"
PED RM J.BOX
TB-13
"W102" P2
APEX J BOX
J2 TB-13
FOC MOTOR
J B
J7 P7
BLK (HOT)
WHT (NEUT)
GRN (GND)
OR RED
GND STUD
TB-1
M22
**(RED)
"W7" (35 FT)
CABLE "W6 & W7"
PLUG MS3106A-14-7P (W,X,Y)
CABLE CLAMP MS3057A-6A
BELDEN 8618 OR EQUIV.
3 COND. + SHIELD 16 AWG
P6 KEYED STANDARD
P7 KEYED "W"
W3 CABLE (P5)
BLOCK- AMP 201357-3 (34 PIN)
HOOD- AMP 207434-1
JACKSCREW AMP 200887-2
SHIELD AMP 201896-1
BELDING 8777
THREE TP 22 AWG
NOTES:
1. ANT.'S 1 THRU 20 AFTER SYNCHRO ADDITION.
2. ▲DENOTES DRAIN WIRE.
*BLUE, DENOTES, BLUE TAPE COLOR CODING, ROT
**RED " RED " " " , FOC
NEXT ASSY
USED ON
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
PROJECT
FR SYSTEM
MODEL "E"
TITLE
F/R TRASLATOR SYS.
HTR 1500
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY
DATE 8-29-89
DESIGNED BY
DATE
APPROVED BY
DATE
SHEET NUMBER 5OF10
DRAWING NUMBER B13740 W10
REV.
SCALE


4
3
2
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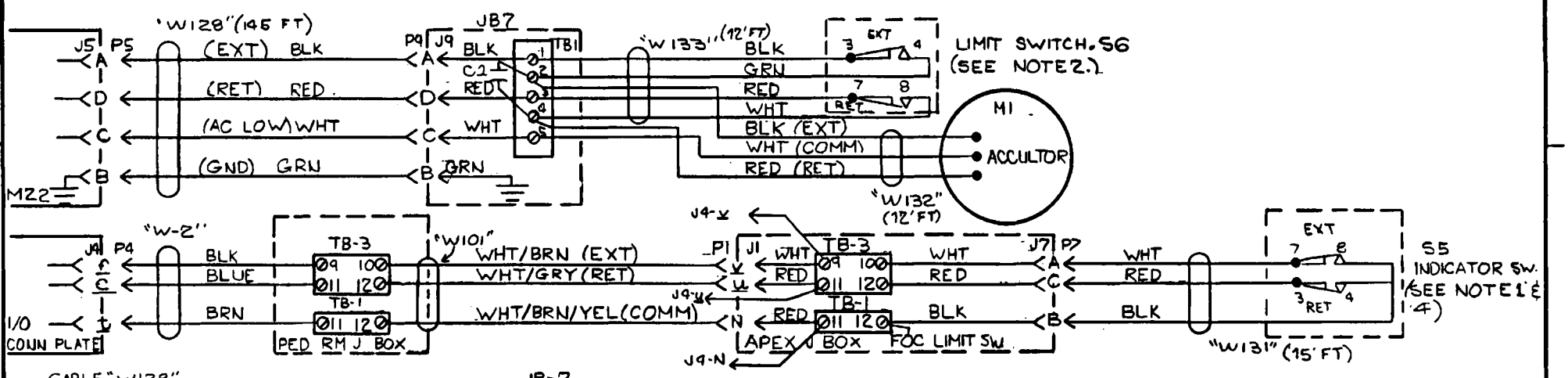
D
C
B
A
REV. | DATE | DRAWN BY | APPR'D BY | DESCRIPTION
PED ROOM J BOX
APEX J BOX
"W4" (32FT) (GRN)*
"W5" (32FT) (ORN)**
"W101"
J3 P3
J4 P4
M22
ROT BRAKE + BLK
ROT BRAKE - WHT
FOC BRAKE + BLK
FOC BRAKE - WHT
NC
TB2
TB3
TB5
TB6
BLUE
PUR
YEL
GRN
J1 P1
WHT (11'FT)
RED
BLK (11'FT)
ROT BRAKE
FOC BRAKE
FOCUS LIMIT SWITCH
UL
LL
S6
SEE FIG. 1
J4 P4 "W2-A"
I/O CONN PLATE
FOC UL BLK
LIMIT SW RET BRN
FOC LL YEL
TB1
WHT/BLK
WHT/BRN/YEL
WHT/BRN
BLK (1FT)
WHT
RED
ZOT BOX CONNECTIONS
J4
TBI-14
TBI-12
TBI-16
FOC UL (BLK)
RET (WHT)
FOC LL (RED)
S6A
S6B
SWITCHES 6A & 6B ARE INSTALLED ON ANT.'S 12 & 20 ONLY.
FIG 1
"W4" & "W5" CABLE
PLUG MS3106A-14-7P(W,X,Y)
CABLE CLAMP MS3057-6A
BELDEN #8770 OR EQUIV.
3 COND + SHIELD #18 AWG
J1 & J4 ON APEX J BOX
COVER "J4" MS25043-36D
CONN. MS3102E-36-10S
S6
SWITCH ASSY. E50NN1
HEAD E50DN1
SWITCH E50SN1
RECEPTACLE E50RB
LEVER E50KL200
NOTES:
1. ALL ANT.'S AFTER SYNCHRO ADDITION.
2. P3 IS KEYED "Y"
3. P4 IS KEYED "X"
*GRN, DENOTES GRN TAPE COLOR CODE ROT
**ORN, " ORN " " " FOC
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
NEXT ASSY | USED ON
PROJECT: FR SYSTEM MODEL E
TITLE: F/R BRAKE & LIMIT SWITCHING CONTROL
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY | DATE 8-29-84
DESIGNED BY | DATE
APPROVED BY | DATE
SHEET NUMBER 6 OF 10
DRAWING NUMBER B13740W10
REV.
SCALE



CABLE "W128"
P5 MS3106F-14S-2P, PLUG
P9 MS3106F-14S-2S, PLUG
BELDEN 8620 OR EQUIV. 16 AWG 4 COND
CABLE "W132", "W133"
BELDEN 8620 OR EQUIV. 16 AWG 4 COND.
CABLE "W131"
P7 MS3106F-14-2P PLUG
J7 MS3102A-14-2S RECEPTICAL
BELDEN 8770 OR EQUIV 18 AWG 3 COND
SWITCH S5, & S6
E50KL200 LEVER
E50NNI SWITCH ASSY.
- E50NI HEAD
- E50SN BODY
- E50RB RECEPTICAL

JB-7
HOFFMAN A606LP ENCLOSURE (6X6X4)
KULKA TYPE 601-6 TERMINAL BOARD
HOFFMAN A6P6 PANEL
KULKA M5601-6 MARKER STRIP
T&B B14-250A TERMINAL FEMALE 90°
LITTON-VEAM 16952 GASKET F/#14 SHELL
J9 MS3102A-14-2P CONNECTOR
MALLORY PSU2730 CAPACITOR 330 VAC, 27-32 MFD
MALLORY HB4 BRACKET FOR ABOVE CAP
MALLORY PLA6 END CAP FOR ABOVE CAP.
MI ACCULATOR
P/N 6K6405-14
TYPE PC26A36C35V

NOTES:
1. INDICATOR SWITCH IS INSTALLED ON LEFT SIDE OF 327 RING. (LOOKING DOWN)
2. LIMIT SWITCH IS INSTALLED ON RIGHT SIDE OF 327 RING MOUNT. (LOOKING DOWN)
3. ANT.'S 13, 20, & 21 ONLY.
4. S5 MUST BE SET TO ACTIVATE JUST PRIOR TO S6 IN BOTH DIRECTIONS

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:

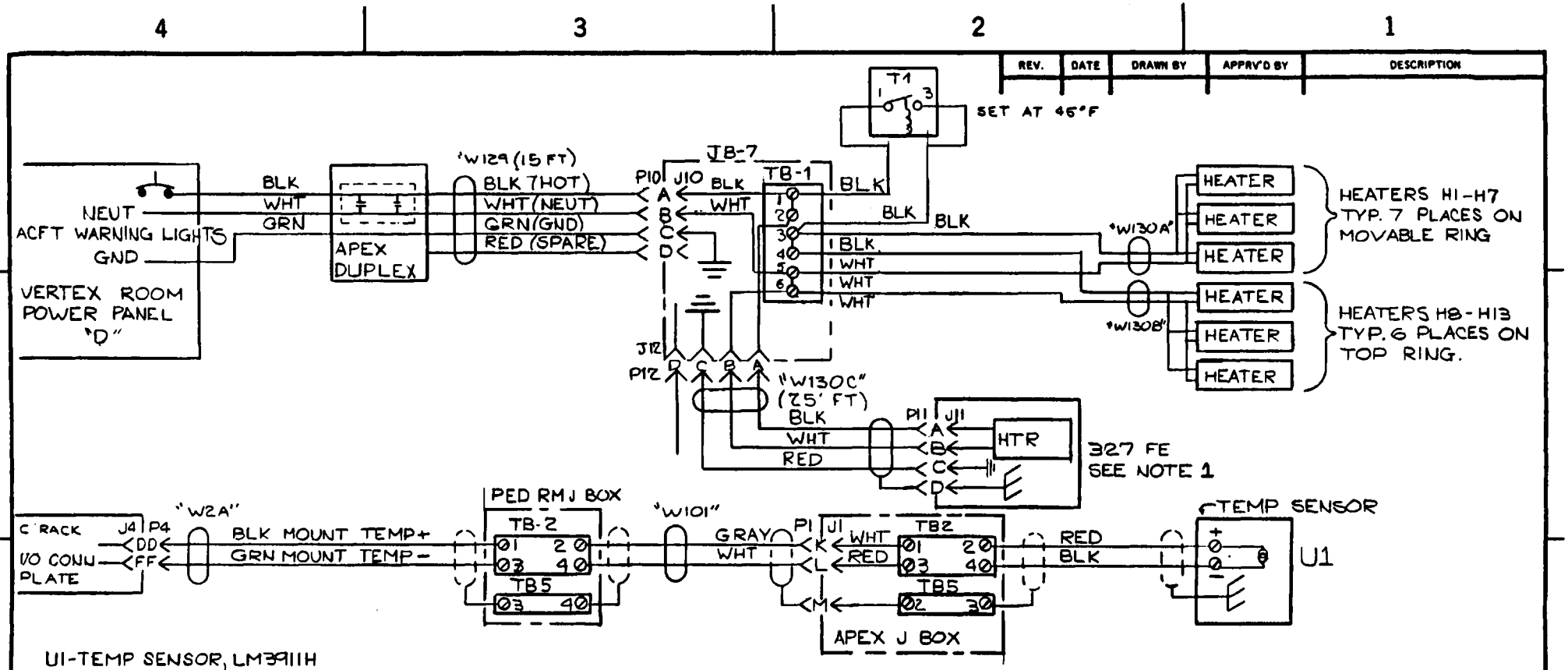
NEXT ASSY	USED ON

PROJECT: FR SYSTEM MODEL "E"
TITLE: 327 MHz FEED RING ACTUATOR

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 8-30-84
DESIGNED BY	DATE
APPROVED BY	DATE

SHEET NUMBER 7 OF 10 | DRAWING NUMBER B13740W10 | REV. | SCALE



U1-TEMP SENSOR, LM3911H
S1-THERMO SWITCH, PIT,-15 CHROMALOX
TB1- TERMINAL BOARD, TYPE 601-6, MARKER STRIP-MS601-6
JB7- ENCLOSURE, A6044LP
J10, J11-RECEPTICLE, MS3102R-14-2P
P10, P11-PLUG, MS3106F14-2S, GASKET#14-16952
*W129"-BELDEN 8618 OR EQUIV. 16 AWG 3 COND.
"W130"-BELDEN 8719 OR EQUIV. 16 AWG 2 COND
H1 THRU H6-HEATER, SH 2X12X 2.5-115
H7-HEATER, SH2X 8X2.5-115
H8 THRU 13- HEATER, SH1X12X5-115
J12: MS3102A-14-2S
P12: MS3106F-14-2P
P11: MS3106F-14-2S
T&B 2520 STRAIN RELIEF 1/2X1/4, 2 EA

NOTES
1. RF AMP INSTALLED ON ANT. THAT HAS 327 MHz FEED

NEXT ASSY	USED ON

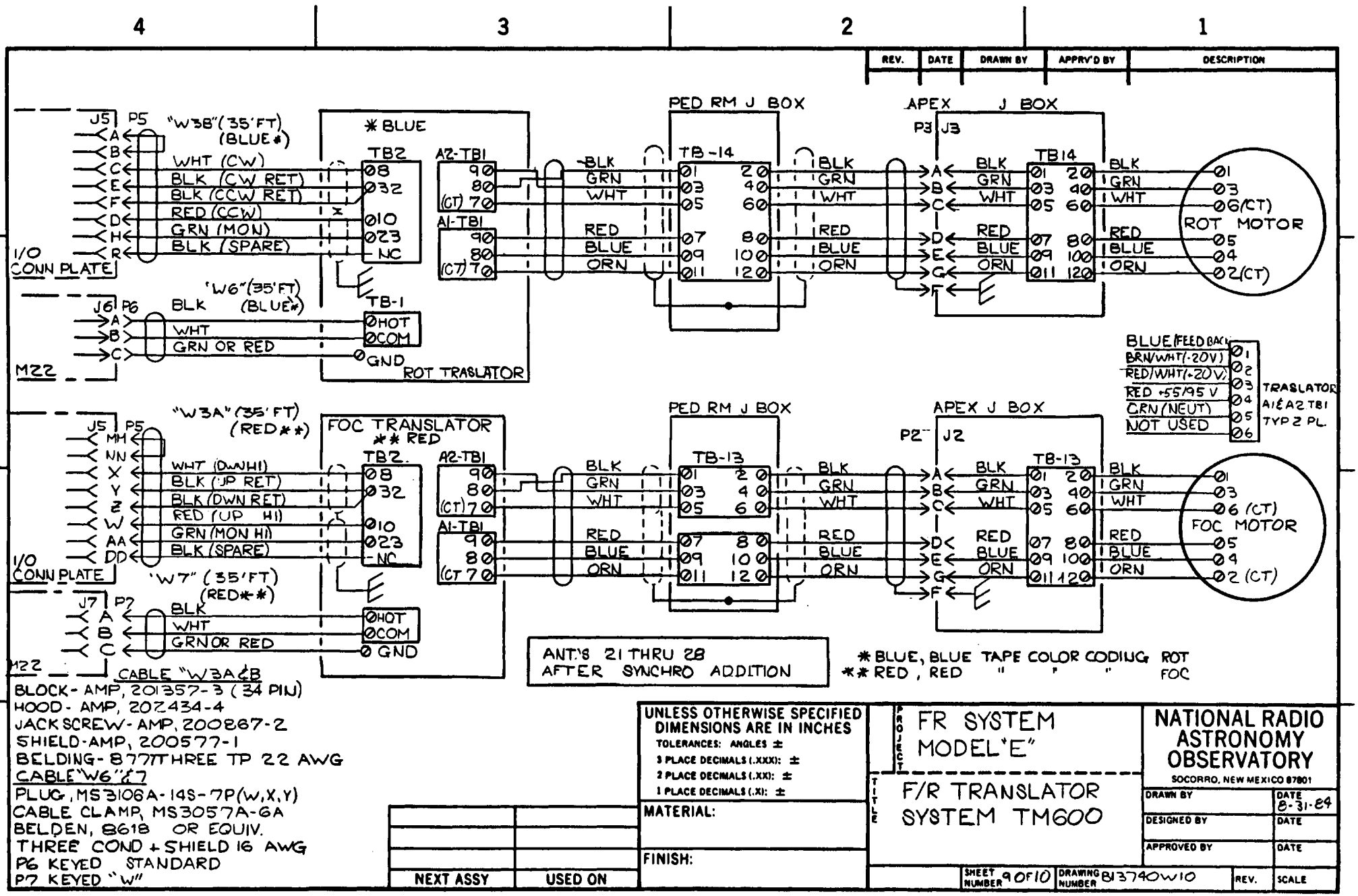
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:

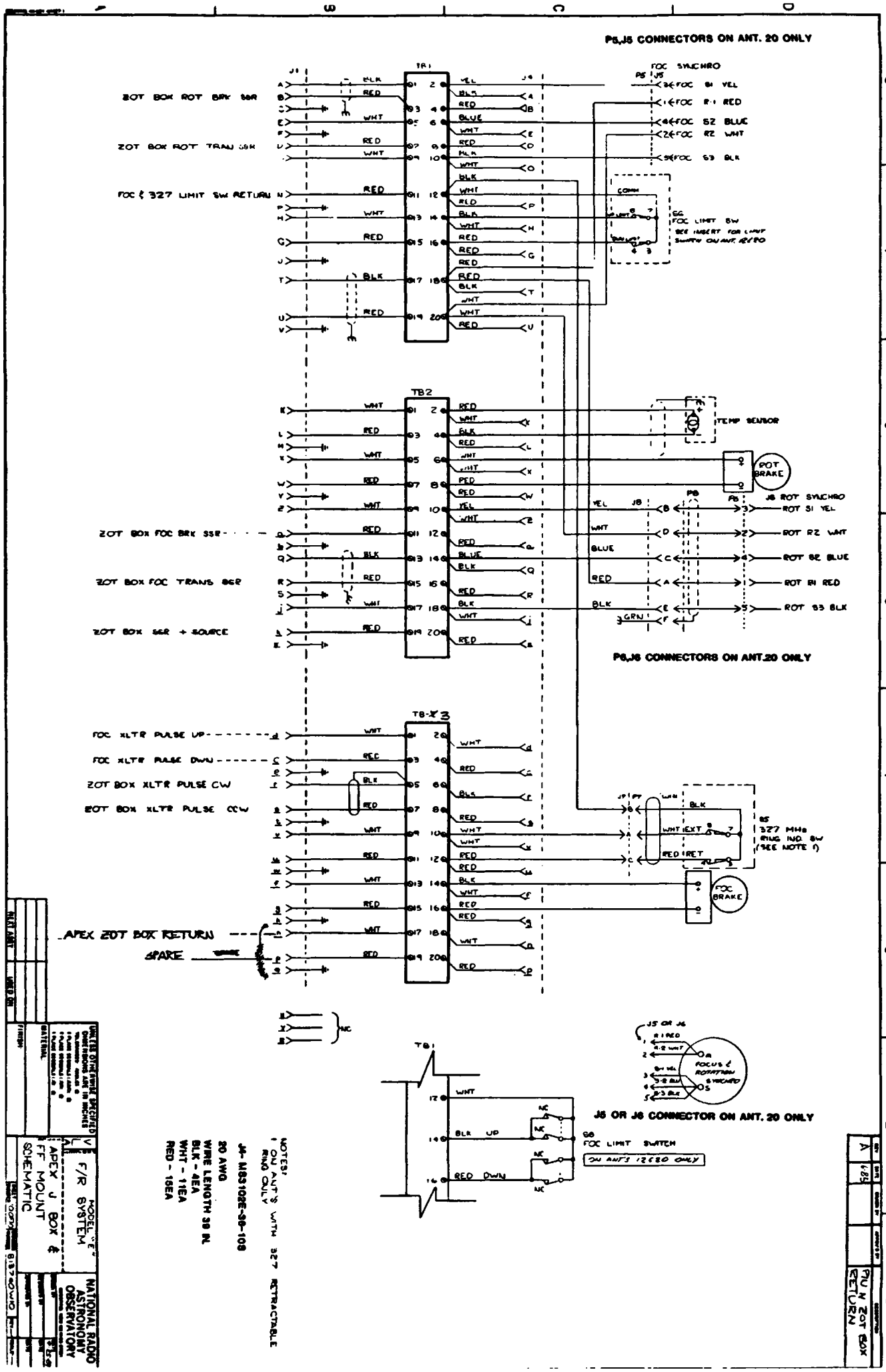
PROJECT: FR SYSTEM MODEL "E"
TITLE: PRIME FEED MOUNT HEATER CONTROL & SENSOR SYSTEM

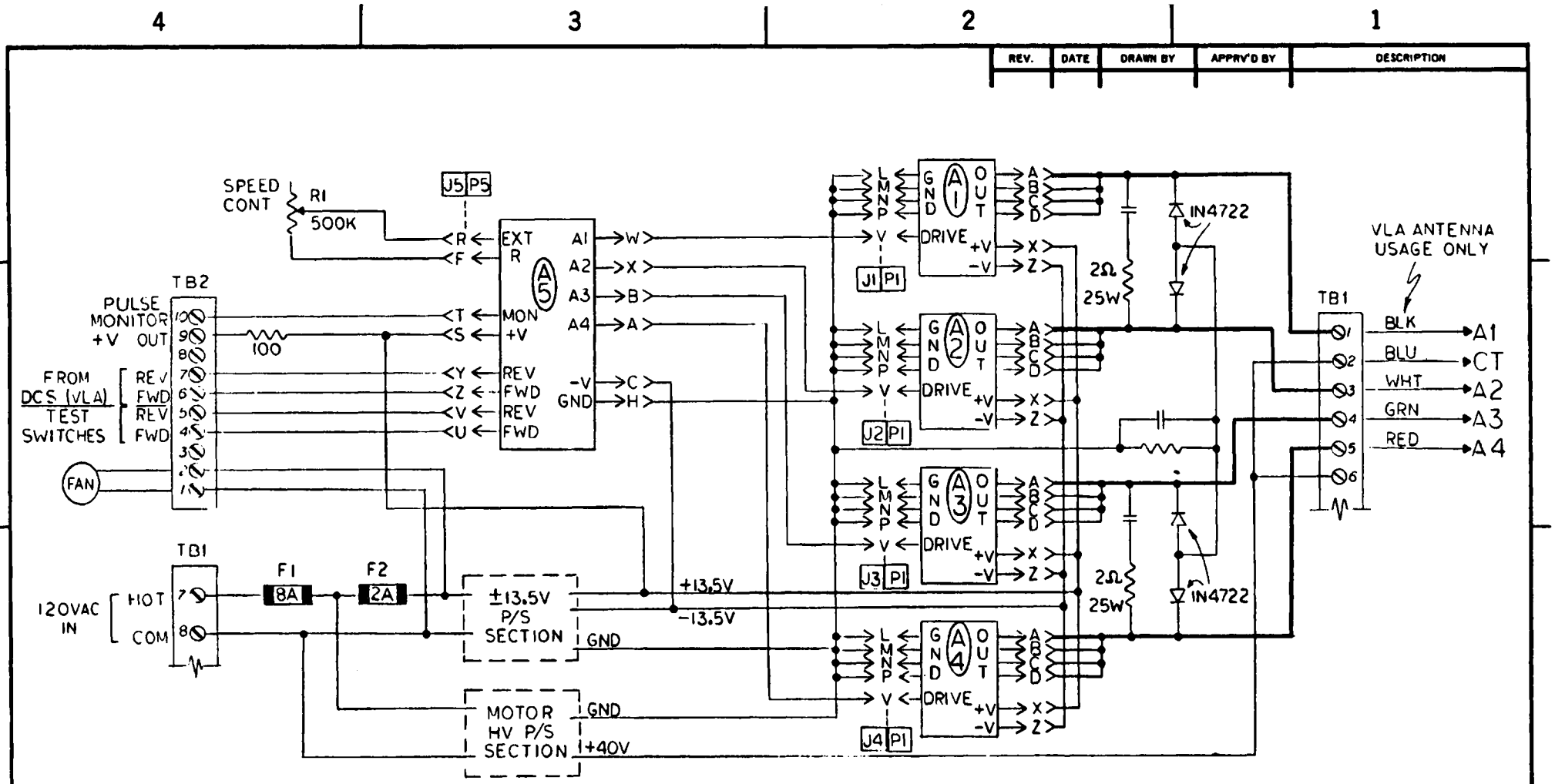
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 5-30-84
DESIGNED BY	DATE
APPROVED BY	DATE

SHEET NUMBER 8 OF 10 | DRAWING NUMBER B13790W10 | REV. | SCALE


4
3
2
1
D
C
B
A
REV. DATE DRAWN BY APPRV'D BY DESCRIPTION
J5 P5 "W3B" (35' FT) (BLUE*)
WHT (CW)
BLK (CW RET)
BLK (CCW RET)
RED (CCW)
GRN (MON)
BLK (SPARE)
I/O CONN PLATE
* BLUE
TB2
A2-TBI
A1-TBI
TB-1
J6 P6 "W6" (35' FT) BLK (BLUE*)
WHT
GRN OR RED
HOT
COM
GND
M22
ROT TRASLATOR
PED RM J BOX
TB-14
APEX J BOX
P3 J3
TB14
ROT MOTOR
BLUE (FEED BACK)
BRN/WHT (-20V)
RED/WHT (+20V)
RED +55/95 V
GRN (NEUT)
NOT USED
TRASLATOR A1 & A2 TBI TYP 2 PL.
J5 P5 "W3A" (35' FT) (RED**)
FOC TRANSLATOR ** RED
WHT (DWN HI)
BLK (UP RET)
BLK (DWN RET)
RED (UP HI)
GRN (MON HI)
BLK (SPARE)
I/O CONN PLATE
J7 P7 "W7" (35' FT) (RED**)
TB-13
P2 J2
FOC MOTOR
ANT'S 21 THRU 28 AFTER SYNCHRO ADDITION
* BLUE, BLUE TAPE COLOR CODING ROT
** RED, RED " " " FOC
CABLE "W3A&B
BLOCK - AMP, 201357-3 (34 PIN)
HOOD - AMP, 207434-4
JACK SCREW - AMP, 200867-2
SHIELD - AMP, 200577-1
BELDING - 8777 THREE TP 22 AWG
CABLE "W6" & 7
PLUG, MS3106A-14S-7P (W, X, Y)
CABLE CLAMP, MS3057A-6A
BELDEN, 8618 OR EQUIV.
THREE COND + SHIELD 16 AWG
P6 KEYED STANDARD
P7 KEYED "W"
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
NEXT ASSY
USED ON
PROJECT FR SYSTEM MODEL "E"
TITLE F/R TRANSLATOR SYSTEM TM600
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY
DATE 8-31-84
DESIGNED BY
DATE
APPROVED BY
DATE
SHEET NUMBER 9 OF 10
DRAWING NUMBER 813740W10
REV.
SCALE


P5,J5 CONNECTORS ON ANT. 20 ONLY
TB1
TB2
TB3
FOC SYNCHRO
ZOT BOX ROT BRK SSR
ZOT BOX ROT TRANS SSR
FOC & 327 LIMIT SW RETURN
ZOT BOX FOC BRK SSR
ZOT BOX FOC TRANS SSR
ZOT BOX SSR + SOURCE
ZOT BOX XLTR PULSE CW
ZOT BOX XLTR PULSE CCW
APEX ZOT BOX RETURN
SPARE
FOC XLTR PULSE UP
FOC XLTR PULSE DWN
TEMP SENSOR
POT BRAKE
FOC BRAKE
J6 ROT SYNCHRO
ROT S1 YEL
ROT R2 WHT
ROT S2 BLUE
ROT R1 RED
ROT S3 BLK
P6,J6 CONNECTORS ON ANT.20 ONLY
J5 OR J6
J5 OR J6 CONNECTOR ON ANT. 20 ONLY
FOC LIMIT SWITCH
ON ANT'S 12&20 ONLY
NOTES:
1 ON ANT'S WITH 327 RETRACTABLE RING ONLY
J4- MS3102E-20-10S
20 AWG
WIRE LENGTH 30 IN.
BLK - 4EA
WHT - 11EA
RED - 18EA
APEX J BOX & SCHEMATIC
F/R SYSTEM
NATIONAL RADIO ASTRONOMY OBSERVATORY
RUN ZOT BOX RETURN



NOTES:

1. FOR DETAILED SCHEMATIC REFER TO SUPERIOR ELECTRIC CO. DWG EM185201 SIZE C

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY	USED ON

VLA PROJECT: FOC/ROT SYSTEM

TITLE: HTR1008 TRANSLATOR
HTR1500 TRANSLATOR
SCHEMATIC

SHEET NUMBER 1 OF 3

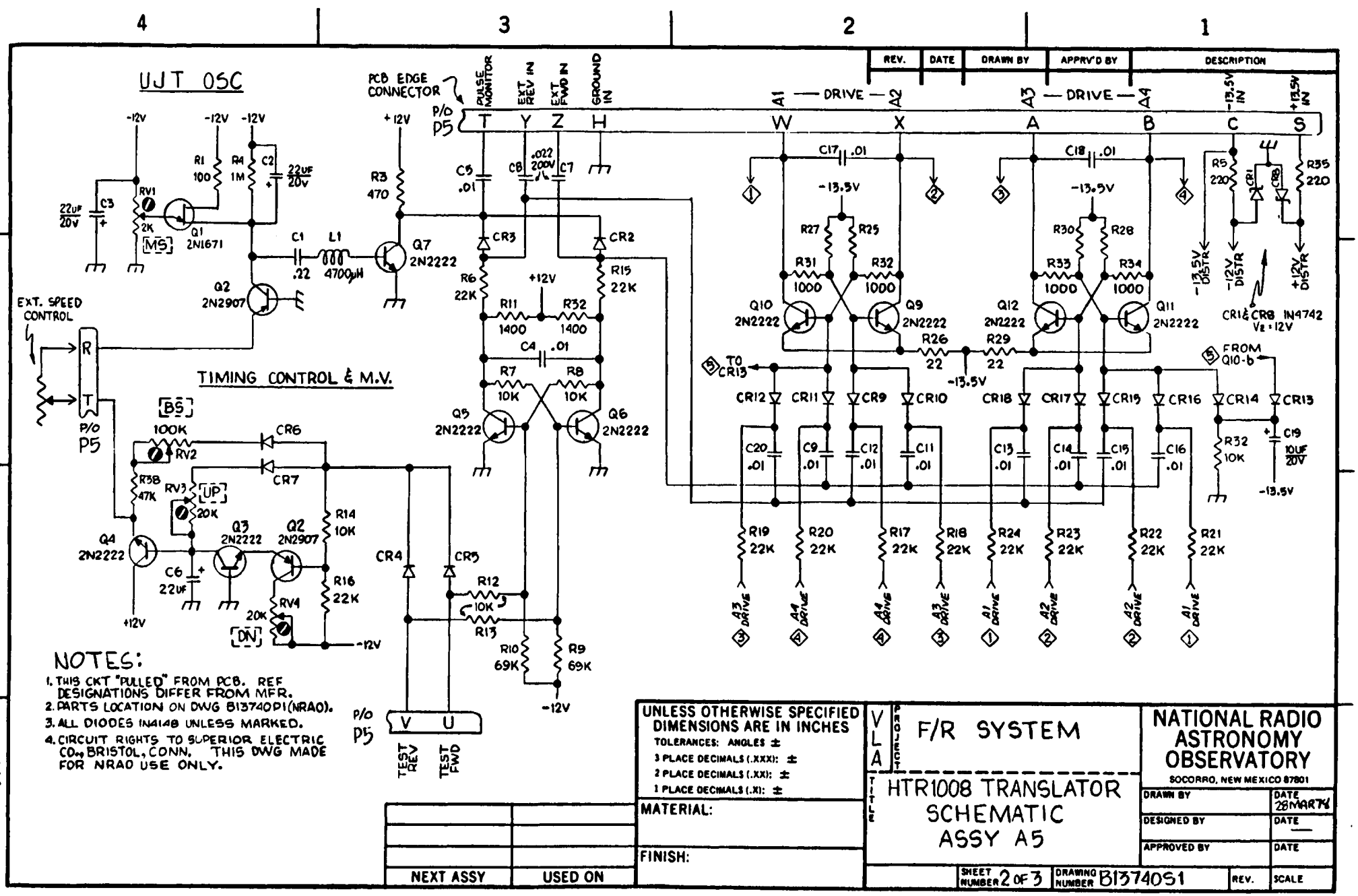
DRAWING NUMBER B1374051

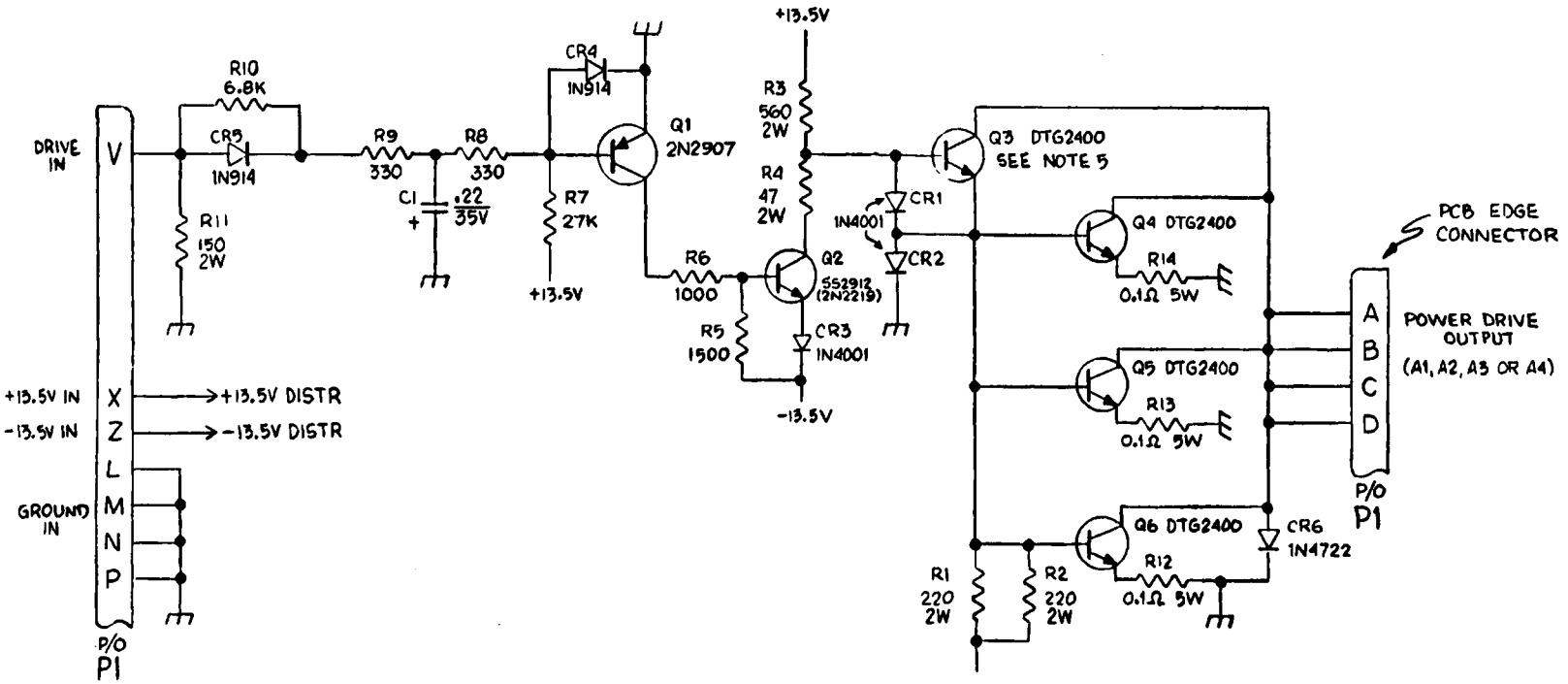
REV.

SCALE

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 3/14/AR 78
DESIGNED BY	DATE —
APPROVED BY	DATE


UJT OSC
TIMING CONTROL & M.V.
PCB EDGE CONNECTOR
P/O P5
PULSE MONITOR
EXT REV IN
EXT FWD IN
GROUND IN
A1 — DRIVE — A2
A3 — DRIVE — A4
-13.5V IN
+13.5V IN
EXT. SPEED CONTROL
TEST REV
TEST FWD
NOTES:
1. THIS CKT "PULLED" FROM PCB. REF DESIGNATIONS DIFFER FROM MFR.
2. PARTS LOCATION ON DWG B1374OP1(NRAO).
3. ALL DIODES IN4148 UNLESS MARKED.
4. CIRCUIT RIGHTS TO SUPERIOR ELECTRIC CO., BRISTOL, CONN. THIS DWG MADE FOR NRAO USE ONLY.
REV. | DATE | DRAWN BY | APPR'D BY | DESCRIPTION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:
NEXT ASSY
USED ON
VLA
F/R SYSTEM
TITLE
HTR1008 TRANSLATOR SCHEMATIC ASSY A5
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801
DRAWN BY
DESIGNED BY
APPROVED BY
DATE 28MAR74
SHEET NUMBER 2 OF 3
DRAWING NUMBER B1374051
REV.
SCALE



NOTES:

1. THIS CKT "PULLED" FROM PCB. REF DESIG DIFFER FROM MFR.
2. PARTS LOCATION ON NRAO DWG B13740P1.
3. CIRCUIT RIGHTS TO SUPERIOR ELECTRIC CO., BRISTOL, CONN. THIS DWG MADE FOR NRAO USE ONLY.
4. ALL UNMARKED RESISTORS 1/2 W.
5. Q3 THRU Q6 — DELCO DTG-2400, AVAILABLE FROM MS ELECTRONICS, 322 N. STONE STREET, ROCKVILLE, MD 20850 NO KNOWN DIRECT SUBSTITUTE.

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY	USED ON

VLA PROJECT: FOC/ROT SYSTEM

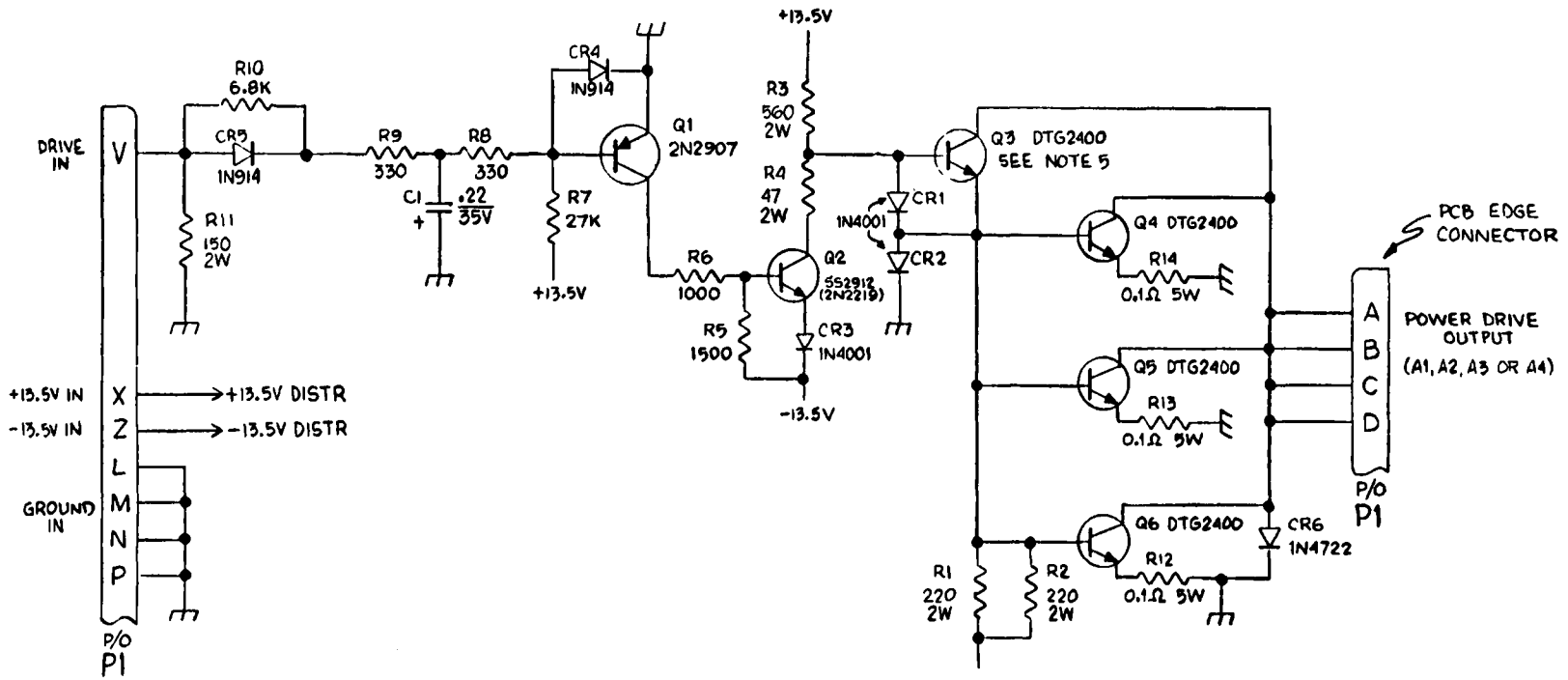
TITLE: HTR1008 TRANSLATOR SCHEMATIC
DRIVER ASSY A1, A2, A3, A4

SHEET NUMBER 3 OF 3 | DRAWING NUMBER B1374051 | REV. | SCALE

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 29MAR78
DESIGNED BY	DATE —
APPROVED BY	DATE

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION



NOTES:

1. THIS CKT "PULLED" FROM PCB. REF DESIG DIFFER FROM MFR.
2. PARTS LOCATION ON NRAO DWG B13740P1.
3. CIRCUIT RIGHTS TO SUPERIOR ELECTRIC CO., BRISTOL, CONN. THIS DWG MADE FOR NRAO USE ONLY.
4. ALL UNMARKED RESISTORS 1/2 W.
5. Q3 THRU Q6 — DELCO DTG-2400, AVAILABLE FROM MS ELECTRONICS, 322 N. STONE STREET, ROCKVILLE, MD 20850 NO KNOWN DIRECT SUBSTITUTE.

NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

VLA PROJECT: FOC/ROT SYSTEM

TITLE: HTR1008 TRANSLATOR SCHEMATIC DRIVER ASSY A1,A2,A3,A4

SHEET NUMBER 3 OF 3 | DRAWING NUMBER B1374051 | REV. | SCALE

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 29MAR78
DESIGNED BY	DATE —
APPROVED BY	DATE

INSTRUCTIONS
for
SLO-SYN® TRANSLATOR
Type TM600

INSPECTION

When unpacking the SLO-SYN Translator, examine the unit carefully for any shipping damage. The "Damage and Shortage" instruction packed with the unit outlines the procedure to follow if any parts are missing or damaged. Check to see that the following items have been received.

1. SLO-SYN Translator Type TM600.
2. Eight terminals for #14 — #16 wire, Superior Electric part number 8244-009.
3. One terminal for #14 — #16 wire, Superior Electric part number 8244-002.
4. Base speed control potentiometer, 10K ohms, ½ watt, linear taper, Superior Electric part number 144664-004.
5. High speed control potentiometer, 500K ohms, ¼ watt, CCW audio taper, 10 turn, Superior Electric part number 201893-001.

DESCRIPTION

The TM600 is an open chassis unit which incorporates a d-c power supply together with the sequencing and switching logic needed for bidirectional control of a SLO-SYN Stepping Motor. It will drive a SLO-SYN motor in either the half-step (0.9° increments) or the full-step (1.8° increments) mode and is intended for base mounting.

The TM600 receives pulses from a minicomputer, microprocessor or similar pulse source and converts the pulses into the switching sequence needed to drive a SLO-SYN motor in steps. The external pulse source controls the step rate, direction, acceleration, deceleration and the number of steps taken. An internal oscillator is also provided for manual or "off-line" positioning.

THE SUPERIOR ELECTRIC COMPANY
Bristol, Connecticut 06010

SPECIFICATIONS

Dimensions (Maximum)	length: 15¾" (400mm) width: 13⅛" (333mm) height: 10¼" (260mm)
Weight (Maximum)	54 lbs. (24.5 kg)
Power Input Requirement	120/220/240 VAC $^{+10\%}_{-15\%}$ 50/60 hertz, 12 amperes maximum
Temperature Range	operating: 0°C to +55°C air temperature at fan intake port storage: —40°C to +85°C
Internal Oscillator	
Range	base speed: 0 to 1000 pulses per second (0 to 2000 pulses per second in half-step mode) high speed: 200 to 10,000 pulses per second (400 to 20,000 pulses per second in half-step mode)
Stability	±15% or ±50 pulses per second, whichever is greater, over stated temperature and voltage ranges
Acceleration and Deceleration Ranges	0.05 to 1.7 seconds, potentiometer adjustable
Base Speed Control	10k ohm, single-turn, linear taper potentiometer
High Speed Control	500k ohm, ten-turn, CCW audio taper potentiometer

TTL Compatible Input/Output Signals

Pulse Output	
High Level	open collector, rated at 30 VDC
Low Level	0 to 0.7 VDC
Loading	30mA sink max.
Fall Time	2 microseconds max., 1000 ohms to +30 VDC max.
Rise Time	2 microseconds max., 1000 ohms to +30 VDC max.
Pulse Width	10 to 25 microseconds
Pulse Input Terminals	
High Level	open circuit, 3 VDC to 6 VDC
Low Level	0 to 0.5 VDC
Loading	4mA sink max.
Pulse Input Requirements	
Fall Time	2 microseconds maximum
Rise Time	2 microseconds maximum
Pulse Width	10 microseconds min.
Trigger Edge	0 to 1 level transition (Trailing edge) advances motor shaft
Direction Control	
High Level	open circuit, 3.2 VDC to 6 VDC
Low Level	0 to 0.5 VDC
Loading	4mA sink max.
Base Speed and High Speed On/Off Controls	
High Level	open circuit, 3.2 VDC to 6 VDC
Low Level	0 to 0.5 VDC
Loading	4mA sink max.
Half-Step/Full-Step Mode Selection	
High Level	open circuit, 3.2 VDC to 6 VDC
Low Level	0 to 0.5 VDC
Loading	4mA sink max.
Low Voltage Sense	
High Level	open collector output rated at 30 VDC max.
Low Level	0 to 0.7 VDC
Loading	30mA sink max.
Fall Time	2 microseconds max., 1000 ohms to 30 VDC max.
Rise Time	2 microseconds max., 1000 ohms to 30 VDC max.
Fault Condition	motor voltage below 40 VDC +12 VDC bias voltage below +9.5 VDC —12 VDC bias voltage above —8.5 VDC
High Temperature Monitor	
High Level	open collector output rated at 30 VDC max.
Low Level	0 to 0.7 VDC
Loading	30mA sink max.
Fall Time	2 microseconds max., 1000 ohms to 30 VDC max.
Rise Time	2 microseconds max., 1000 ohms to 30 VDC max.
Temperature Trigger Conditions	logic 1 to logic 0 transition when heat sink temperature rises to 195°F ±9°F (90°C ±5°C) logic 0 to logic 1 transition when heat sink temperature drops to 165°F ±9°F (74°C ±5°C)

RS232C Compatible Input/Output Signals

Pulse Output	
High Level	+8 VDC to +12 VDC
Low Level	—8 VDC to —12 VDC
Loading	3k ohm min.
Fall Time*	1 microsecond max.
Rise Time*	1 microsecond max.
Pulse Width	10 microseconds min.
Pulse Input Terminals	
High Level	+3 VDC to +25 VDC
Low Level	—3 VDC to —25 VDC
Loading	3k ohm min.
Pulse Input Requirements	
Fall Time*	3 microseconds max. for 25 VDC input
Rise Time*	3 microseconds max. for 25 VDC input
Pulse Width	10 microseconds min.
Trigger Edge	0 to 1 transition (trailing edge) advances motor shaft
Direction Control	
High Level	+3 VDC to +25 VDC
Low Level	—3 VDC to —25 VDC
Loading	3k ohms to 7k ohms

Base Speed and High Speed On/Off Controls

High Level	+3 VDC to +25 VDC
Low Level	−3 VDC to −25 VDC
Loading	3k ohms to 7k ohms

Half-Step/Full-Step Mode Selection

High Level	+3 VDC to +25 VDC
Low Level	−3 VDC to −25 VDC
Loading	3k ohms to 7k ohms

Low Voltage Sense

High Level	+8 VDC to +12 VDC
Low Level	−8 VDC to −12 VDC
Loading	3k ohms min.
Rise Time	1 microsecond max.
Fall Time	1 microsecond max.
Fault Condition	motor voltage below 40 VDC +12 VDC bias voltage below +9.5 VDC −12 VDC bias voltage above −8.5 VDC

High Temperature Monitor

High Level	+8 VDC to +12 VDC
Low Level	−8 VDC to −12 VDC
Loading	3k ohms min.
Rise Time	1 microsecond max.
Fall Time	1 microsecond max.
Temperature Trigger Conditions	logic 0 to logic 1 transition when heat sink temperature rises to 195°F ±9°F (90°C ±5°C) logic 1 to logic 0 transition when heat sink temperature falls below 165°F ±9°F (74°C ±5°C)

*The rise or fall time may be calculated as follows:

$$T\ rise\ or\ T\ fall = \frac{90\%\ of\ high\ level - 90\%\ of\ low\ level}{slope}$$

$$where\ slope = \frac{6\ volts}{4\%\ of\ pulse\ width}$$

for example, if the high level is +12 VDC, low level is −12 VDC and pulse width is 10 microseconds.

$$slope = \frac{6}{.04 \times 10} = 15\ volts/\mu sec.$$

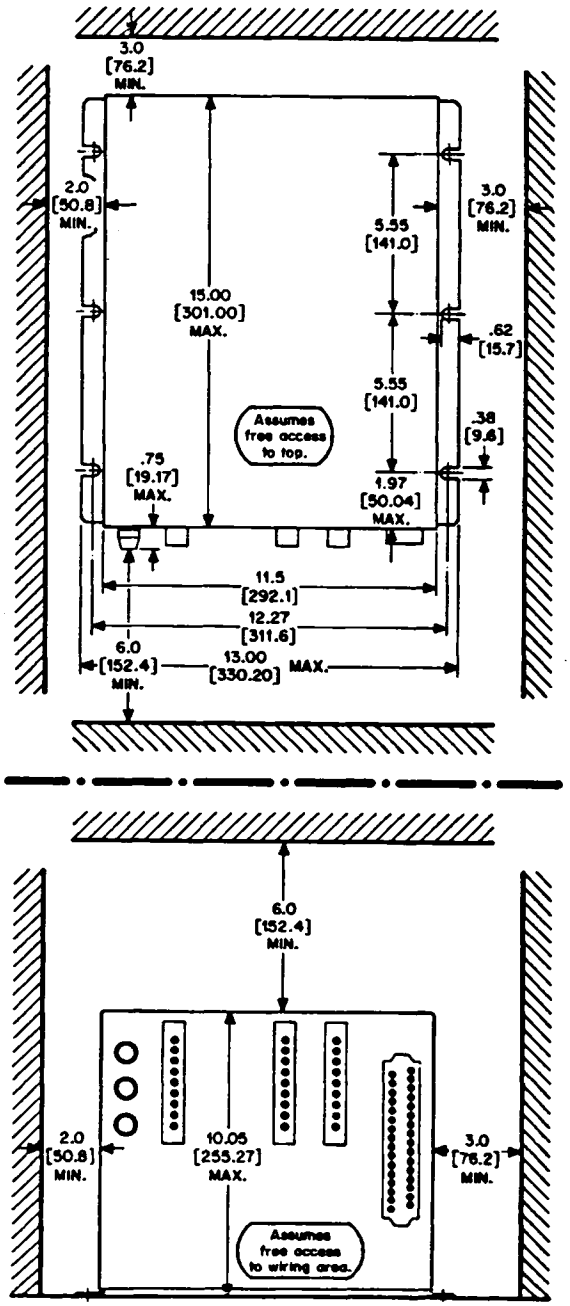
$$T\ rise\ or\ T\ fall = \frac{(12 \times 0.9) - (-12 \times 0.9)}{15} = 1.44\ \mu sec.\ max.$$

MOUNTING

The TM600 is an open chassis unit designed for base mounting. Horizontal mounting on the floor of an enclosure is the preferred method due to weight and accessibility considerations. Mounting holes are provided in the flanges at the base of the unit.

When planning the installation, it is important to allow sufficient room for servicing the unit. Figure 1 shows the minimum clearances required to allow removal of the cover and printed circuit boards. In any case, a minimum clearance of 2 inches must be provided all around the unit to allow proper air circulation. Details on replacing the circuit boards are given in the Service section of this manual.

A kit to allow rack mounting of the TM600 is also available. The kit, part number 207800-001, includes a 19" (483mm) wide by 10½" (267mm) high panel, two mounting brackets and the necessary hardware.



MOUNTING DIMENSIONS
FIGURE 1

ELECTRICAL INSTALLATION *

The electrical installation consists of three parts: Motor Connections; Control Interface; and AC Input Connections. Figure 2 shows a typical installation and identifies the Motor, Control and AC Input wiring.

MOTOR CONNECTIONS

Six of the eight terminals for #14 — #16 wire provided with the TM600 should be used for making the motor connections. As shown in the Connection Diagram, Figure 3, one phase of the motor should be connected to terminals 7, 8 and 9 of one motor drive circuit board and the other phase to terminals 7, 8 and 9 of the other motor drive board.

CAUTION: It is extremely important that the motor be connected correctly. Double check the wiring at the motor terminals and at the drive boards before energizing the translator.

The three leads for each motor phase must be twisted together their entire length to avoid stray inductance. For distances up to 15 feet, use #14 wire. For distances between 15 feet and 50 feet use #10 wire. If motor leads longer than 50 feet are necessary, consult the factory for recommendations.

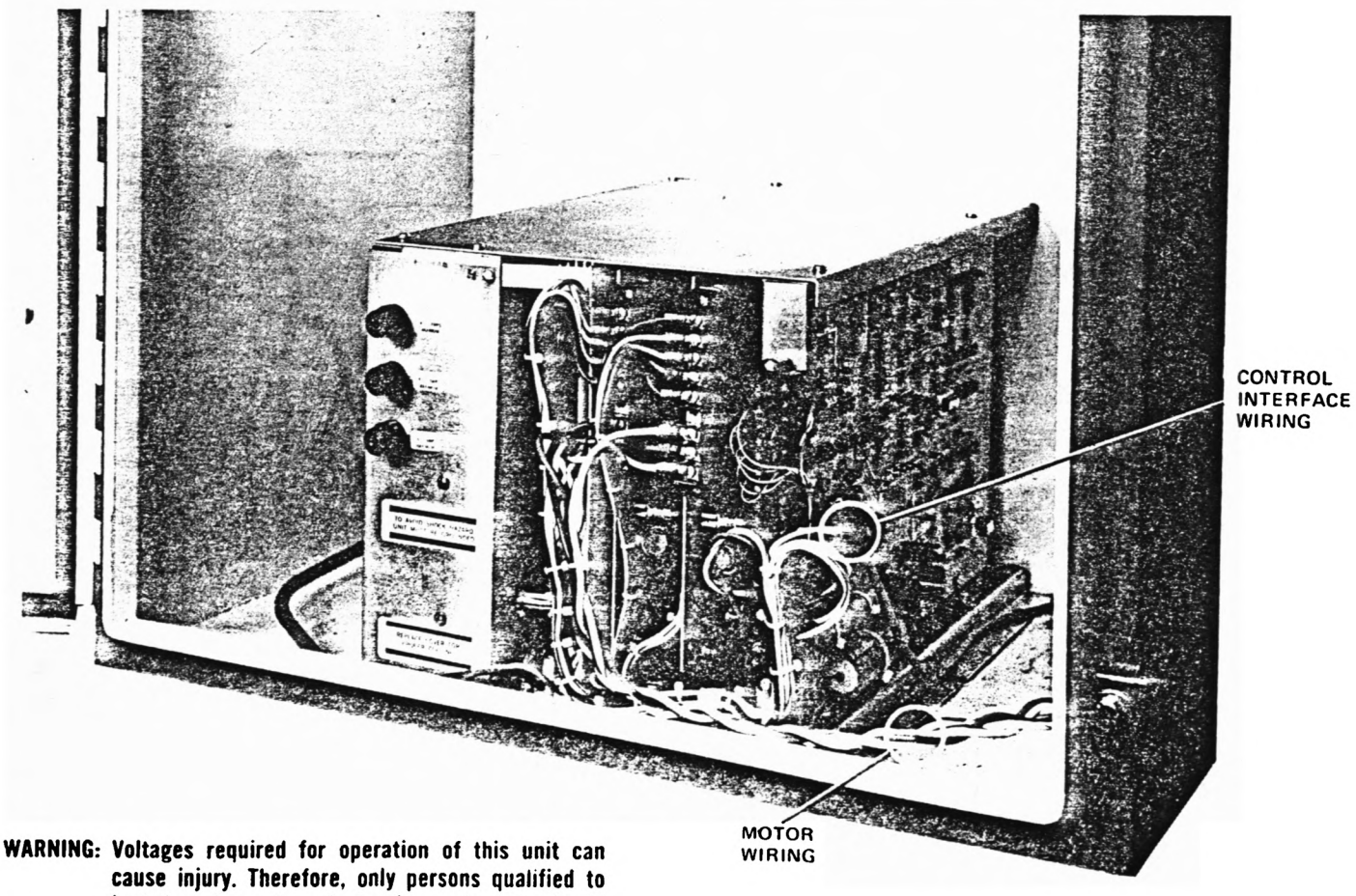
The motor shell must be connected to earth ground by a separate lead or via the machine to which it is attached. The motor leads should be routed along an axis 90° to 180° with respect to the axis along which the power leads are routed to provide maximum noise immunity and minimum emi (radiated or conducted noise).

INTERFACE

The TM600 uses two distinct interface methods. The first is called negative logic which means that the control will carry out the intended command when that input is at a low voltage level. The requirements of this low level are given in the specification for the respective input terminal. Each terminal is pulled up to +12 VDC. Any device which pulls the input to the specified low level, such as an open-collector TTL device, a transistor or a switch is capable of activating the input.

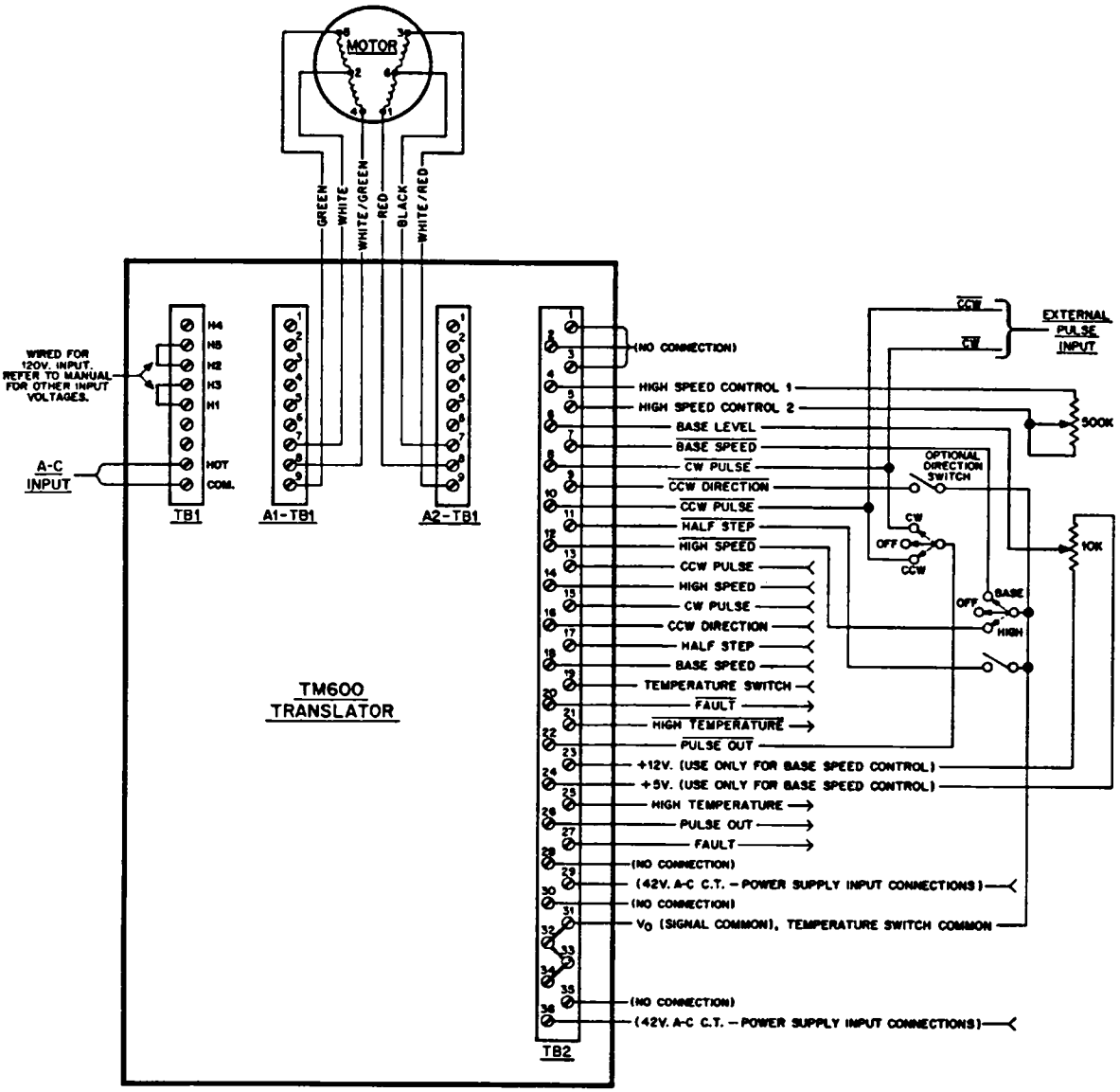
The three recommended interfacing techniques are shown in Figures 4, 5 and 6 using the CCW PULSE input as an example.

The second interface method is one which is compatible with applicable paragraphs of the Electronic Industries Association Standard RS232C. Basically RS232C defines voltage and load requirements for interface circuits. These requirements are reflected in the TM600 specifications for the RS232C I/O terminals. The recommended interfacing technique uses integrated circuits specifically designed to meet RS232C requirements. Using the CCW PU (RS232C) input of the TM600 as an example, Figure 7 shows the recommended interface technique.

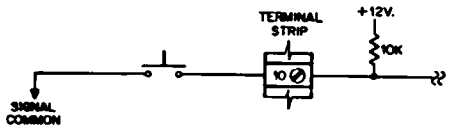


TYPICAL INSTALLATION
FIGURE 2

* **WARNING: Voltages required for operation of this unit can cause injury. Therefore, only persons qualified to install and service electronic equipment should perform installation or servicing procedures on this unit.**

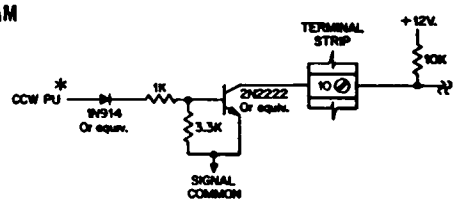


CONNECTION DIAGRAM
FIGURE 3



NEGATIVE LOGIC INTERFACE
SWITCH CLOSURE TO SIGNAL COMMON

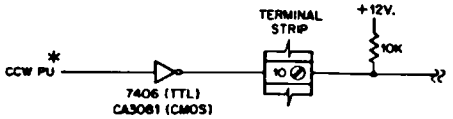
SWITCH CLOSURE TO SIGNAL GROUND
FIGURE 4



NEGATIVE LOGIC INTERFACE
DISCRETE OPEN COLLECTOR

* Must be positive signal since transistor acts as an inverter.

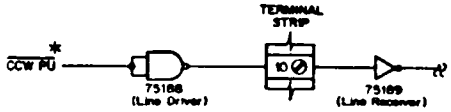
DISCRETE OPEN CONNECTOR
FIGURE 5



NEGATIVE LOGIC INTERFACE
TTL or CMOS
OPEN COLLECTOR INTEGRATED CIRCUIT

* Must be positive signal since device acts as an inverter.

TTL OR CMOS INTEGRATED CIRCUIT INTERFACE
FIGURE 6



EIA-RS232C LOGIC INTERFACE

* Must be negative signal since device acts as an inverter.

EIA — RS232C INTERFACE TECHNIQUE
FIGURE 7

INTERFACE CONNECTIONS

All interface connections are made to the 36-terminal connector on the Oscillator/Translator board. It is recommended that these connections be made with shielded cable (Alpha Wire Corporation #5313 or #5303; Beldon Corporation #9541 or equivalent). #22 or #24 wire is suggested. The wire need only be stripped and tinned. Connect one end of the shield to signal common (pin 31 or 32 on the connector). Terminal numbers for RS232C connections are given in parentheses.

For the purposes of this discussion, the following terms are defined.

"low level" for negative logic interface	0 to 0.5 VDC
"high level" for negative logic interface	3.2 to 6 VDC
"low level" for RS232C	−25 to −3 VDC
"high level" for RS232C	3 to 25 VDC

For the negative logic interface, the function is activated when the input is at a low level. For RS232C logic, the function is considered activated when the input is at a high level.

Base Speed Controls

The 10k ohm potentiometer for base speed control should be connected to terminals 6, 23 and 24 as shown in Figure 3. This control adjusts the internal oscillator base frequency within a range of 0 to 1000 full-steps or 0 to 2000 half-steps per second. The oscillator will run at the base frequency setting when the BASE SPEED input, terminal 7 (18) is activated. The translator will drive the motor at base speed whenever the PULSE OUTPUT terminal 22 (26) is connected to the CW PULSE input, terminal 8 (15) or to the CCW PULSE input, terminal 10 (13). The required sequence is to first connect the pulse output terminal to the desired pulse input terminal and then activate the base speed input.

Acceleration and deceleration are not provided in the base speed mode since the base speed, by definition, is a rate at which the motor will start and stop without error. The optimum base speed setting is dependent on motor frame size as well as external frictional and inertial loading.

High Speed Control

Connect the 500k ohm 10-turn potentiometer supplied to terminals 4 and 5 as shown in Figure 3. This control adjusts the high frequency of the oscillator within a range of 200 to 10,000 pulses per second in the full-step mode or 400 to 20,000 pulses per second in the half-step mode. Changing the setting of the base speed control will affect the high frequency to a small degree. The oscillator will run at the high frequency setting when the HIGH SPEED input, terminal 12 (14) is activated. The correct sequence is to first connect the pulse output terminal to the desired input pulse terminal and then to activate the high speed input. Since the base speed setting will affect the high speed frequency, recheck the high speed after adjusting the base speed.

Acceleration and deceleration are provided when operating in the high speed range. Activating the high speed input will cause the motor to ramp up from the preset base speed to the high frequency setting. When the high speed terminal is deactivated the motor will ramp down and stop.

Direction Control

As an alternative to supplying pulses to CCW PULSE input, terminal 10 (13), for counterclockwise rotation, the CCW DIRECTION input, terminal 9 (16) can be used to control direction with pulses being supplied only to CW PULSE input, terminal 8 (15). With pulses supplied to the CW PULSE input the motor will turn clockwise (as determined facing the nameplate end of the motor) when CCW DIRECTION is deactivated and counterclockwise when CCW DIRECTION is activated.

Step-Mode Selection

The translator is normally in the full-step mode. The half-step mode is selected by activating the HALF-STEP input, terminal 11 (17). In the full-step mode each input pulse results in a motor step increment of 1.8°. In the half-step mode, the step increment will be 0.9°.

In the full-step mode, the windings are energized in a four-step sequence as shown in the following chart.

SWITCHING SEQUENCE
FULL-STEP, TWO WINDINGS ON MODE

SWITCHING STEP †	MOTOR LEAD OR TERMINAL			
	RED (1)	WHITE/RED (3)	WHITE/GREEN (4)	GREEN (5)
1	ON	OFF	OFF	ON
2	ON	OFF	ON	OFF
3	OFF	ON	ON	OFF
4	OFF	ON	OFF	ON
1	ON	OFF	OFF	ON

† Provides clockwise shaft rotation as viewed from nameplate end of motor. For counterclockwise rotation, switching steps will be performed in the reverse order.

When the translator is operating in the half-step mode, the windings are energized in an eight-step sequence as shown in the switching sequence chart for half-stepping.

HALF STEP MODE

SWITCHING STEP †	MOTOR LEAD OR TERMINAL			
	RED (1)	WHITE/RED (3)	WHITE/GREEN (4)	GREEN (5)
1	OFF	OFF	OFF	ON
2	ON	OFF	OFF	ON
3	ON	OFF	OFF	OFF
4	ON	OFF	ON	OFF
5	OFF	OFF	ON	OFF
6	OFF	ON	ON	OFF
7	OFF	ON	OFF	OFF
8	OFF	ON	OFF	ON
1	OFF	OFF	OFF	ON

† Provides clockwise shaft rotation as viewed from nameplate end of motor. For counterclockwise rotation, switching steps will be performed in the reverse order.

Use of the half step operating mode provides greater positioning resolution together with a lessening of the effect of primary motor resonance.

Since mode selection must not be switched while the motor is stepping, it is suggested that this function be hard-wired. For half-step mode selection, connect the HALF-STEP input terminal 11 to Vo terminal 31, or connect the RS232C HALF-STEP input terminal (17) to +12V, terminal 23.

External Pulse Inputs
As mentioned previously, pulses must be supplied to the CW PULSE input, terminal 8 (15), for clockwise rotation of the motor shaft and to CCW PULSE input, terminal 10 (13), for counterclockwise rotation. Input pulse requirements are given in the specifications section.

Pulse Output
Pulse output of the internal oscillator is available on PULSE OUT, terminal 22 (26).

Low Voltage Monitor
This function monitors the various internal voltage supplies and is activated when these voltages go below a safe operating level. The signal itself is labeled FAULT and is brought out on terminal 20 (27). Whenever a low voltage condition exists the Fault signal will latch even though the actual condition may be momentary.

High Temperature Monitor
This signal is activated by a thermostatic switch mounted on one of the drive board heat sinks. The HIGH TEMPERATURE output is on terminal 21 (25). The temperature switching levels are defined in the specifications.

INPUT VOLTAGE CONNECTION
WARNING: Voltages required for operation of this unit can cause injury. Therefore, only persons qualified to install and service electronic equipment should perform installation or servicing procedures on this unit.

The TM600 is wired at the factory for operation from a 120 volt $^{+10\%}_{-15\%}$, 50/60 hertz, power source capable of providing up to 12 amperes. The unit can also be operated from 220 or 240 volt a-c, 50/60 hertz sources by making the proper wiring changes to the primary of the power transformer. These changes are made at terminal strip TB1 and are shown in the TM600 Schematic Diagram, Figure 13.

Once the transformer primary connections have been matched to the voltage of the power source, the input power connections can be made to terminal strip TB1 as shown in Figure 3.

Be sure to connect the chassis grounding stud to a suitable ground. Terminal lugs are provided for making these connections. Use two smaller lugs for the a-c input connections and the larger lug for connecting to the grounding stud. It is recommended that #14 wire be used for the power connections.

The a-c input leads should be routed along an axis 90° to 180° with respect to the path of the motor leads.

Check for proper a-c input and transformer primary connections before energizing the translator. Energize the unit and check to see that there is full supply voltage between the hot and common leads and between the hot lead and the chassis. There should be zero volts between the common lead and the chassis.

OPERATION
The functions of the controls for the TM600 are as follows:

Base Speed Control
This control adjusts the internal oscillator base speed within a 0 to 1000 pulse per second range in the full-step mode and a 0 to 2000 pulse per second range in the half-step mode. Acceleration and deceleration are not provided since the base speed, by definition, is a rate at which the motor will start and stop without error. The optimum base speed setting is dependent on motor frame size as well as on external frictional and inertial loading.

Recommended maximum base speeds for each motor type are given in the table.

RECOMMENDED MAXIMUM BASE SPEED

MOTOR TYPE	MAXIMUM BASE SPEED, NO LOAD (STEPS PER SECOND)
M092-FD-310	550
M093-FD-301	475
M112-FJ-326	350
M172-FD-306	210
M172-FD-308	175

High Speed Control
This control adjusts the oscillator high frequency within a 200 to 10,000 step per second range in the full-step mode and within a 400 to 20,000 step per second range in the half-step mode. Since the base speed setting will affect the high speed frequency output, the high speed setting should be rechecked whenever the base speed is readjusted.

Base Speed/High Speed Switch
The translator will drive the motor in the base speed mode when the base speed terminal is activated and in the high speed mode when the high speed terminal is activated. A direction must be selected before actuating the base speed or the high speed.

Direction Switch
This function selects either the clockwise or the counterclockwise direction of motor shaft rotation (facing nameplate end of motor). When operating from the internal oscillator, the direction must be selected before activating the base speed or high speed.

Half-Step Control
This function determines whether the motor will be driven in the half-step or the full-step mode. The motor will take 0.9° steps in the half-step mode and 1.8° steps in the full-step mode. The stepping mode must not be changed while the motor is stepping. Therefore, it is recommended that this be a hard-wired function.

SEQUENCE OF OPERATION
Operating From The Internal Oscillator
The Connection Diagram, Figure 3, shows a recommended method of using toggle switches to operate the translator from the internal oscillator. Proceed as follows:

a. Select the half-step or the full-step mode of operation. The mode selection should be hard-wired.

b. Place the Direction switch in the CW or the CCW position.

c. Place the Base Speed/High Speed switch in the Base Speed position. The Translator will drive the motor at the base speed. Start and stop the motor by moving the switch between Base Speed and Off.

d. Adjust the Base Speed control to select the fastest rate at which the translator will reliably start and stop the motor. Then decrease the base speed by 20 steps or 10%, whichever is greater, to provide a safety margin. It is recommended that a larger safety margin be provided if load variations are anticipated or if a very low base speed is used. The base speed should be adjusted above the range shown with a dotted line in the performance curve for the motor used. If it is necessary to operate the motor in the dotted area of the speed range, refer to the discussion of resonance control in the performance section.

e. To operate in the high speed range place the Base Speed/High Speed switch in the High Speed position. The oscillator will accelerate the motor from base speed up to the selected high speed and will decelerate the motor when the switch is moved to the Off position.

   Acceleration and deceleration are factory adjusted to their maximum settings. In many applications these ramps can be reduced, depending on the combination of motor and load. Refer to "Adjusting Acceleration and Deceleration" for instructions on changing the ramp times.

Operating From External Pulse Input

To operate the TM600 from an external pulse source, proceed as follows:

a. Select the half-step or the full-step mode. This should be a hard-wired function since the stepping mode must not be changed while the translator is driving the motor.

b. Apply pulses to terminal 8 (15) for CW rotation (facing nameplate end of motor) or to terminal 10 (13) for CCW rotation. Pulses must meet the Pulse Input Requirements given in the Specifications section. Since the motor cannot instantaneously follow a pulse train at a frequency higher than its maximum base speed, the pulse rate must be accelerated and decelerated at rates compatible with the specific motor frame size and the load characteristics.

Adjusting Acceleration and Deceleration

CAUTION: Voltages are present on this unit which can cause injury. Therefore, only persons qualified to service electronic equipment should perform adjustments or servicing procedures on this unit.

Note: The Base Speed adjustment must be completed before adjusting acceleration and deceleration.

To adjust the ramps, connect an oscilloscope probe to TP12 on the Oscillator/Translator circuit board (see Figure 11). Connect the scope probe common to TP7 and trigger the scope externally using the HIGH SPEED INPUT, TERMINAL 12. When the Base Speed/High Speed switch is placed in the High Speed position, the voltage on TP10 will rise from 4 volts to a nominal of 11 volts. The time required for this voltage rise to occur is the acceleration time. Conversely, the time required for the voltage to drop from 11 volts to 4 volts when the switch is moved from High Speed to Off is the deceleration time. The acceleration or deceleration time may be changed by adjusting the appropriate potentiometer on the Oscillator/Translator circuit board (Figure 11). Turn the potentiometers clockwise (facing screw end) to increase the ramp times or counterclockwise to reduce the times. Adjust R36 to change acceleration and R24 to change deceleration.

Recommended minimum acceleration times for each motor are listed in the chart.

RECOMMENDED MINIMUM ACCELERATION TIMES

MOTOR TYPE	ROTOR INERTIA, LB-IN² (kgcm²)	INITIAL VELOCITY, (FULL STEPS PER SECOND)	FINAL VELOCITY, (FULL STEPS PER SECOND)	MINIMUM ACCELERATION TIME, (SECONDS)
M092-FD-310	0.42 (1.23)	550	10,000	0.164
M093-FD-301	0.64 (1.87)	475	10,000	0.252
M112-FJ-326	2.75 (8.05)	350	10,000	0.372
M172-FD-306	21 (61)	210	6,000	0.766
M172-FD-308	21 (61)	175	5,500	1.132

PERFORMANCE CHARACTERISTICS

Performance characteristics for motors compatible with the TM600 are given in the performance curves.

The part of each speed vs. torque curve represented with a dotted line is an area of possible resonance. Depending on the amount of friction and inertia in the system. The motor may not operate satisfactorily at the speeds shown in the dotted area. Operating in the half-step mode may provide satisfactory operation in this range, but again this is dependent on the load characteristics.

Pulse Position Control

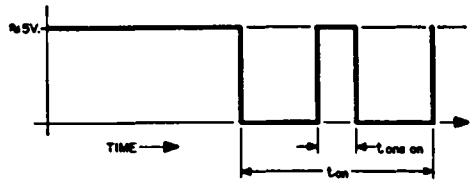
An alternate method of controlling this motor characteristic is a feature of the TM600 called "Pulse Positioning". This technique utilizes a form of electronic damping to virtually eliminate motor resonance. The "One Winding On" mode is used as the braking mode for this technique, so there will be some loss of motor torque.

For example, the full-step torque shown in the performance curves is based on the fact that each winding (A, A', B, B') is on 50% of the time and off 50% of the time. This timing is commonly known as a 50/50 translator duty cycle. When pulse positioning is used the 50% on time will decrease, thus lowering motor torque when compared with the full-step mode. The curve in Figure 8 indicates approximate torque loss when the Pulse Position control is fully counterclockwise.

The following technique can be used to calculate torque loss at a given speed with any adjustment of the Pulse Position Control. Connect a scope probe to R83, R84, R85 or R35 on the Oscillator/Translator circuit board (Figure 11) and connect the scope probe ground to Vo (terminal 31 or 32). The translator waveform shown on the oscilloscope will allow calculation of the percentage of "on" time which is necessary in order to determine torque loss.

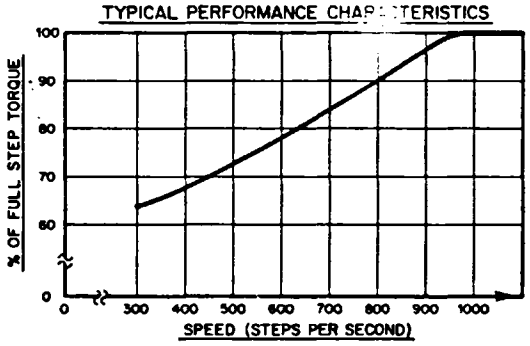
Figure 9 represents a typical translator logic waveform. The "on time" is designated "t on" and the amount of "on time" lost because of the Pulse Position control adjustment is designated "t one on". The ratio of t one on/t on is the percentage of on time lost due to the Pulse Position control adjustment. Subtract this percentage from 100% and use the resulting number to determine actual torque loss from the curve in Figure 10.

In Figure 9, t one on is one division and t on is five divisions, therefore the ratio of t one on to t on is 20%. Subtracting 20% from 100% gives a Percentage Of Translator On Time value of 80%. Figure 10 shows that 75% of full-step torque is available at this setting of the Pulse Position control.

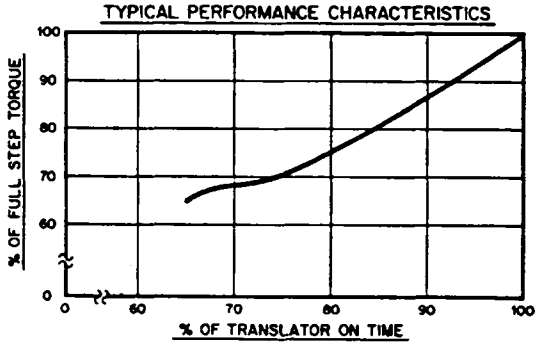


TRANSLATOR LOGIC WAVEFORM

TYPICAL TRANSLATOR LOGIC WAVEFORM
FIGURE 9

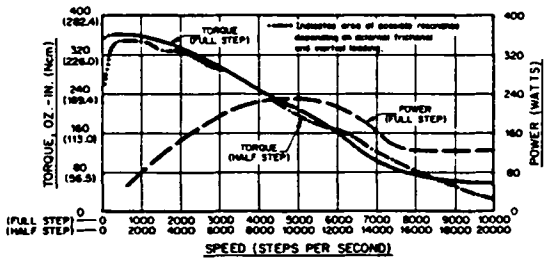


APPROXIMATE TORQUE LOSS WITH PULSE POSITION CONTROL FULLY COUNTERCLOCKWISE
FIGURE 8

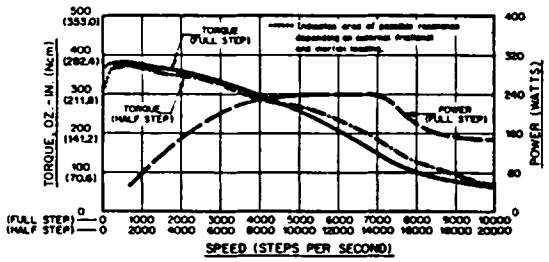


PERCENT TORQUE VS. TRANSLATOR ON TIME
FIGURE 10

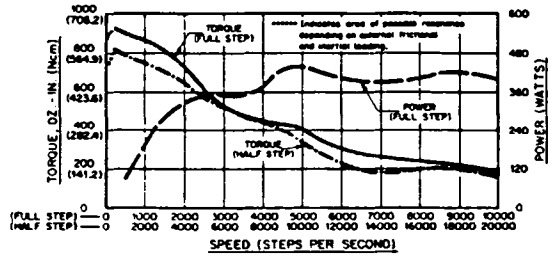
TYPICAL PERFORMANCE CHARACTERISTICS



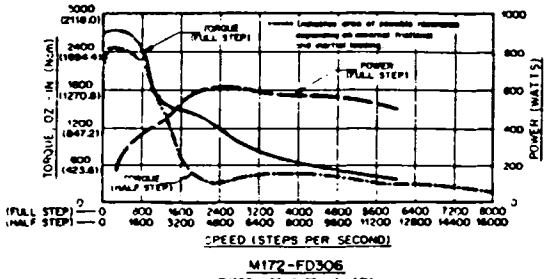
M092-FD310
TMR00 - 120-VOLTS A-C - 60HZ
4-AMPS./ø AVERAGE CURRENT



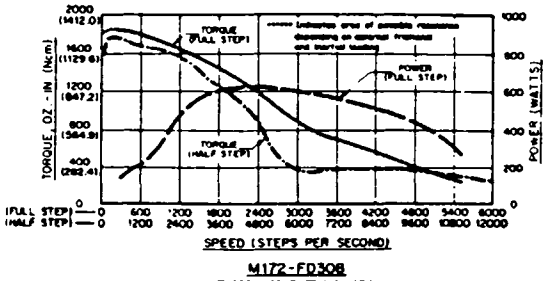
M093-FD301
TMR00 - 120-VOLTS A-C - 60HZ
4-AMPS./ø AVERAGE CURRENT



M112-FJ326
TMR00 - 120-VOLTS A-C - 60HZ
5-AMPS./ø AVERAGE CURRENT



M172-FD306
TMR00 - 120-VOLTS A-C - 60HZ
5-AMPS./ø AVERAGE CURRENT



M172-FD308
TMR00 - 120-VOLTS A-C - 60HZ
5-AMPS./ø AVERAGE CURRENT

Mid-Range Stability Control

All stepping motors exhibit an instability in speeds ranging upward from 1000 steps per second which can result in "holes" in the speed-vs. torque curves due to loss of synchronization or rotor velocity modulation. The TM600 is equipped with a Stability Control which utilizes velocity information obtained from the electronics to compensate for rotor velocity modulation. Since each motor requires a different amount of stabilization, a 4-position DIP switch (SW1) is provided on the Oscillator/Translator board (Figure 11) to allow the circuit to be adjusted for each motor. The switch positions for each motor are listed in the chart.

CAUTION: Voltages are present on this unit which can cause injury. Therefore, only persons qualified to service electronic equipment should perform adjustments or servicing procedures on this unit.

MOTOR	POSITION 1	POSITION 2	POSITION 3	POSITION 4
M172-FD-306	OFF	OFF	OFF	OFF
M172-FD-308	OFF	OFF	OFF	ON
M112-FJ-326	OFF	OFF	OFF	ON
M093-FD-301	OFF	OFF	ON	OFF
M092-FD-310	OFF	ON	OFF	OFF

Due to their larger size, M112 and M172 motors must be run at a higher current level. A DIP switch on each motor drive board (Figure 12) provides this increase. The unit is adjusted for 4 amperes per phase. To change the level to 5 amperes per phase for M112 and M172 motors, set positions 1 and 2 of SW1 on the motor drive board to OFF. The power must be off when making this change.

Duty Cycle

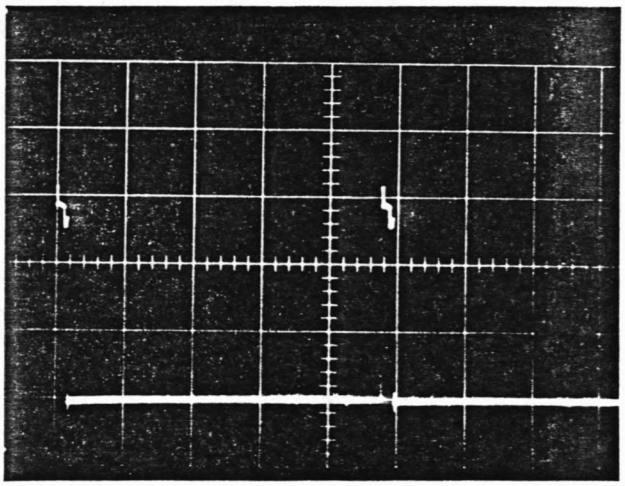
It is difficult to specify a meaningful Duty cycle rating for each motor because of the variety of mounting configurations, speeds and loads encountered in each possible application. None of the motors specified for this drive will operate continuously under all speed and load conditions without adequate heat sinking. The limiting factor, in any case, is the maximum motor shell temperature which must not exceed 90°C.

INITIAL INSTALLATION CHECKOUT

If the Installation and Operation instructions have been followed carefully, the TM600 translator should operate properly with no further adjustments. Should the unit fail to step the motor properly, perform the following checks.

CAUTION: Voltages are present on this unit which can cause injury. Therefore, only persons qualified to service electronic equipment should perform adjustments or servicing procedures on this unit.

1. Check all installation wiring carefully for wiring errors or poor connections.
2. Check to see that the correct a-c power level is being supplied to the translator and that the power transformer primary connections are correct for the input voltage.
3. Be sure that the SLO-SYN motor is a correct model for use with the TM600 translator.
4. Be sure that the proper procedure is being used in operating the translator.
5. Check to see that triggering pulses are being received at terminal 8 (15) for clockwise motion. For CW motion, pulses must be received at terminal 10 (13) or, alternately, a CCW Direction signal must be present on terminal 9 (16). Pulses must not be present on Terminals 8 (15) and 10 (13) simultaneously.
6. With an oscilloscope, check the collector to emitter waveform (Vce) of the power output transistors to see that the motor windings are being energized in the proper sequence. Connect the probe ground to terminal 5 of either Motor Drive circuit board. Connect the scope probe to terminals 8 and 9 on each Motor Drive Board one at a time and check the waveform. A typical waveform is shown in Figure 16. Each division on the vertical scale equals 50 volts.



TYPICAL WAVEFORM
FIGURE 16

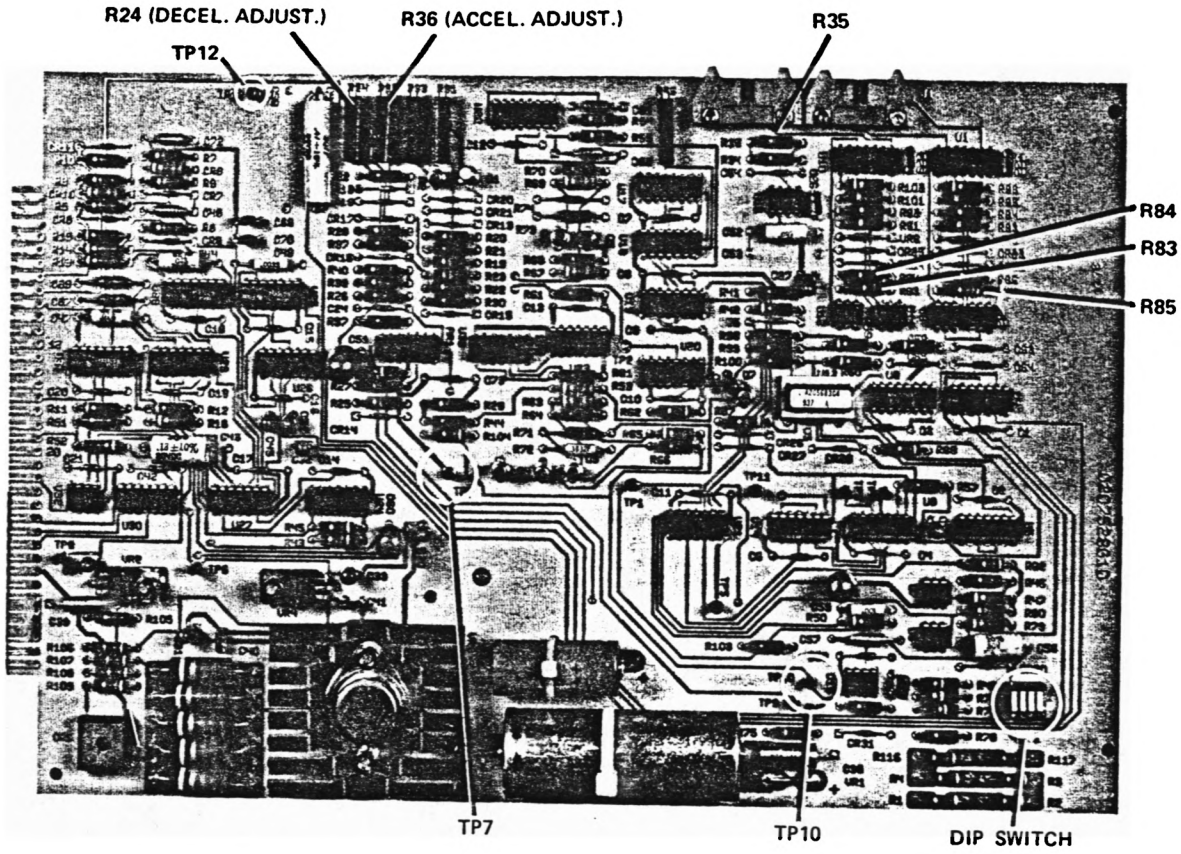
7. If the motor will not drive the load at the desired speed and the preceding checks indicate the translator is operating correctly, the combination of friction load and inertia may be too great for the motor to overcome. This situation can usually be overcome by reducing the operating speed. In severe cases, it may be necessary to use a motor having a higher torque rating or to drive the load through a speed reduction gear train.

SERVICE

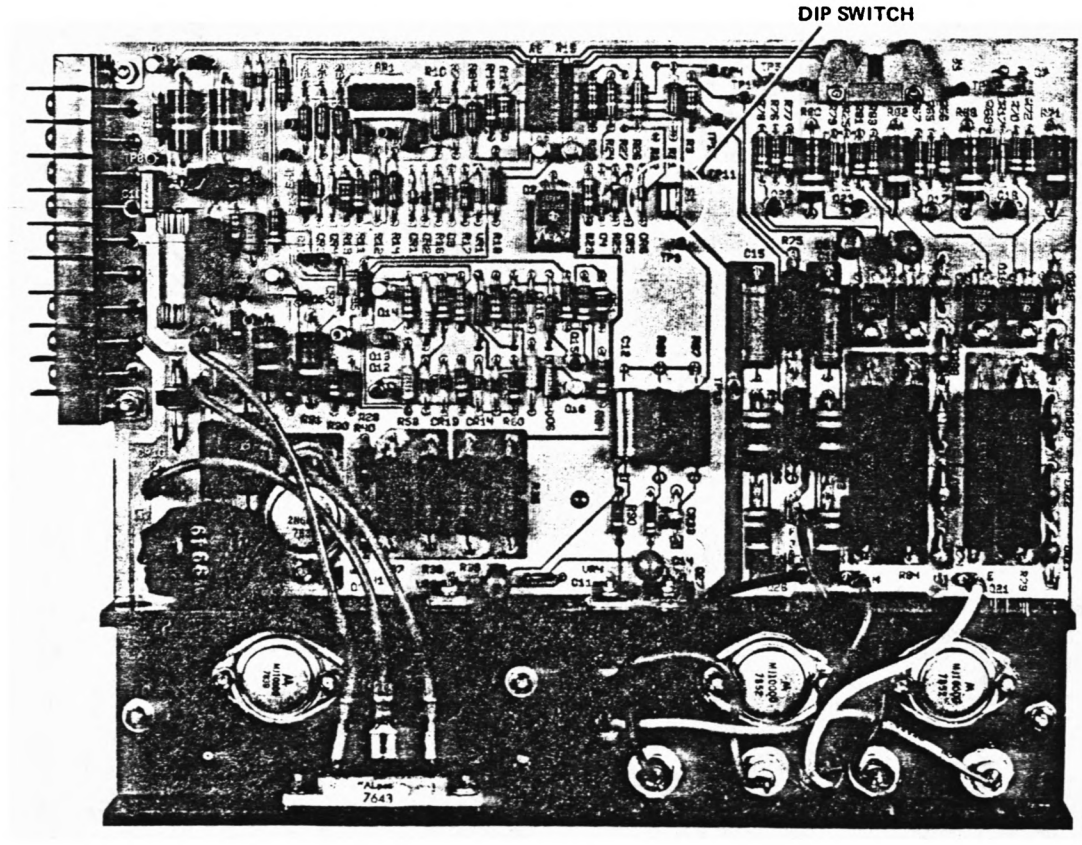
If a problem develops with a circuit board, the board should be removed and returned to the factory for service. Consult the factory if a malfunction occurs that cannot be cured by the preceding checks. To remove the circuit boards proceed as follows:

CAUTION: Voltages are present on this unit which can cause injury. Therefore, only persons qualified to service electronic equipment should perform adjustments or servicing procedures on this unit.

1. Turn off the a-c power to the translator and wait 30 seconds for the d-c power supply to discharge.
2. Remove four screws in the top cover and remove the cover.



OSCILLATOR/TRANSLATOR CIRCUIT BOARD
FIGURE 11



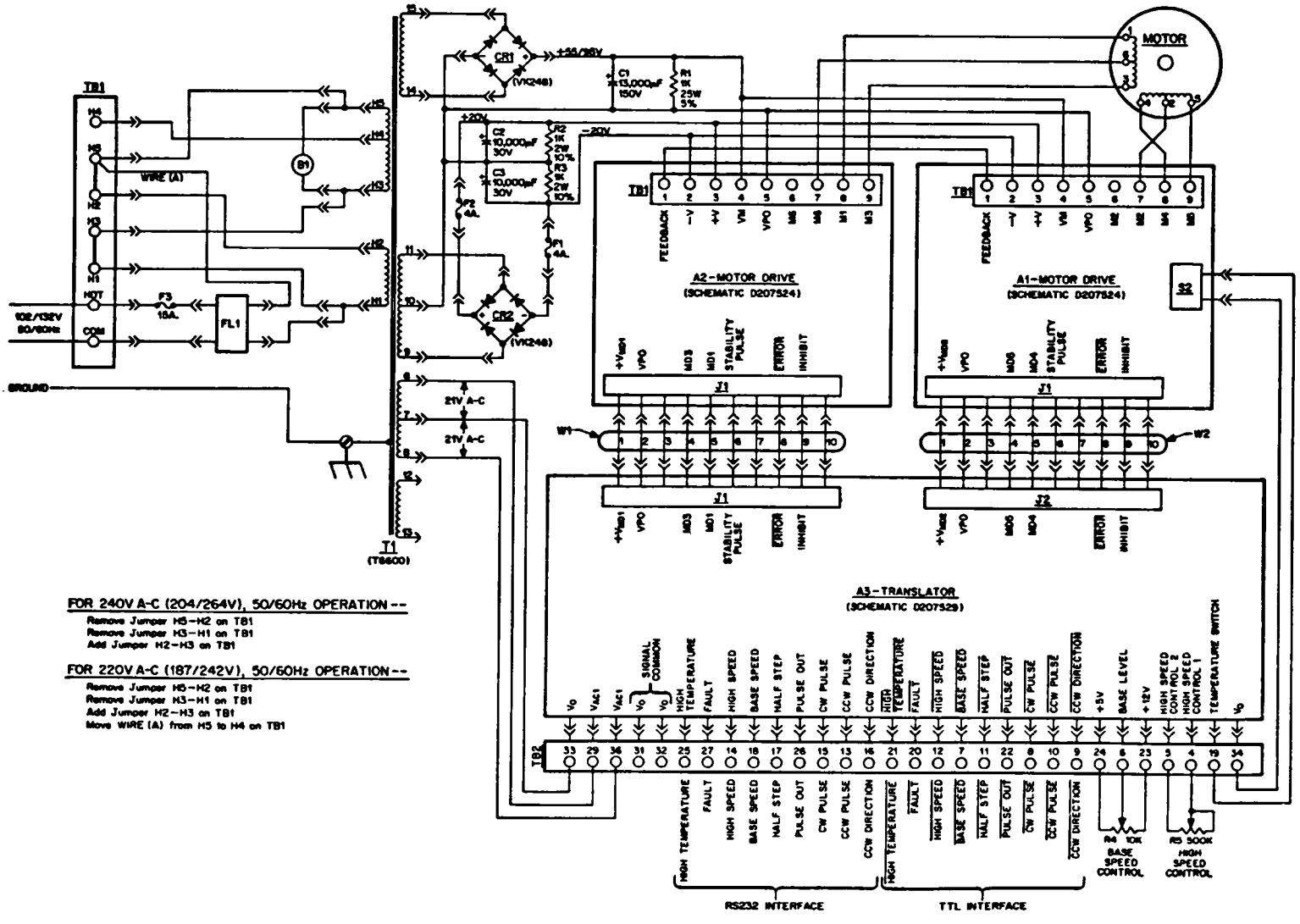
MOTOR DRIVE CIRCUIT BOARD
FIGURE 12

SERVICE (Cont'd.)

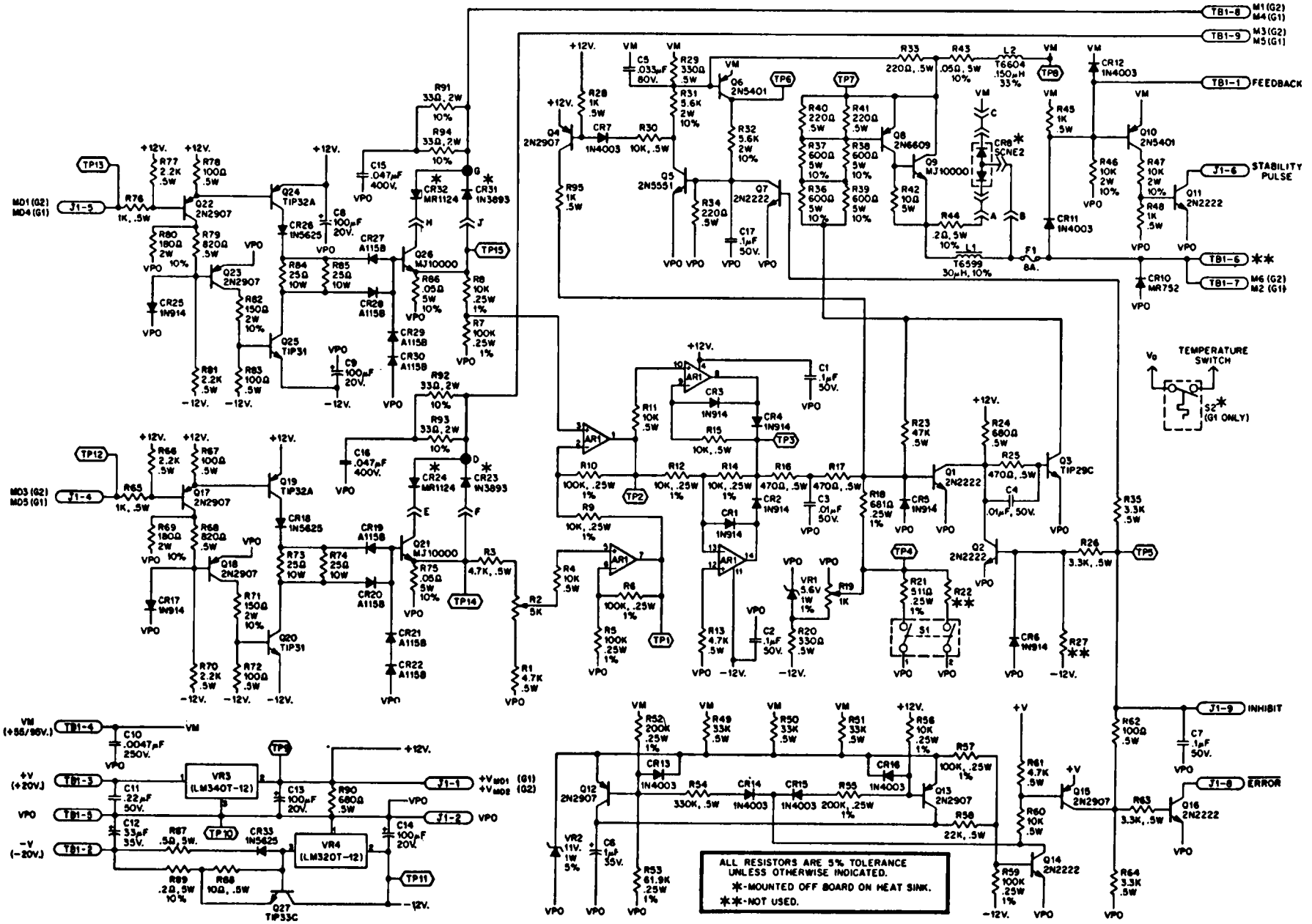
3. To remove either Motor Drive circuit board, proceed as follows:
   a. Disconnect the flat cable connector at the top of the board.
   b. Disconnect the motor and power supply leads from the terminal strip mounted at the rear of the board.
   c. Remove the screw which fastens the "U" channel heat sink at the lower part of the board to the chassis.
   d. Slide the board approximately ½ inch rearward to clear the mounting slot. Then either lift straight up or remove the board toward the rear of the unit.

4. To remove the Oscillator/Translator circuit board, proceed as follows:
   a. Disconnect the flat cable connector at the top of the circuit board.
   b. Remove the two screws holding the interface connector in place and remove the connector by sliding it to the right to clear the mounting bracket.
   c. Grasp the board firmly and remove the 36-position connector from the board.
   d. Remove the board toward the rear of the unit to clear the mounting spaces at the front of the board.

If any unusual problems are encountered in the installation or operation of the SLO-SYN Translator, contact the factory or the nearest Superior Electric sales office.

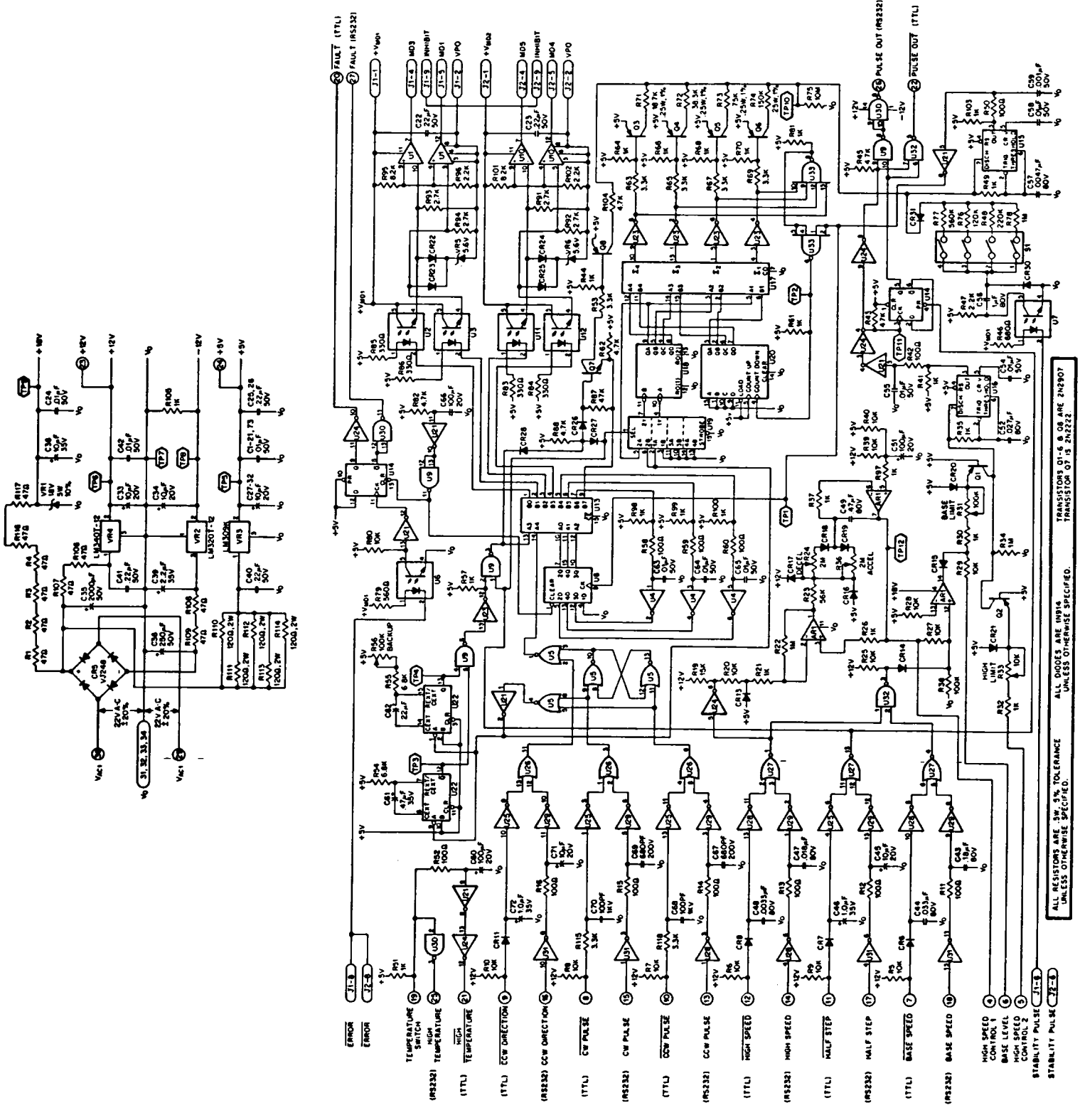


SCHEMATIC DIAGRAM
TM600 TRANSLATOR
FIGURE 13



SCHEMATIC DIAGRAM
MOTOR DRIVE CIRCUIT BOARD

FIGURE 14

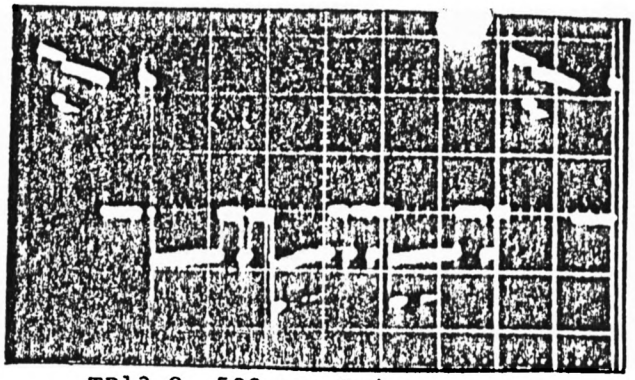


SCHEMATIC DIAGRAM
OSCILLATOR/TRANSLATOR CIRCUIT BOARD

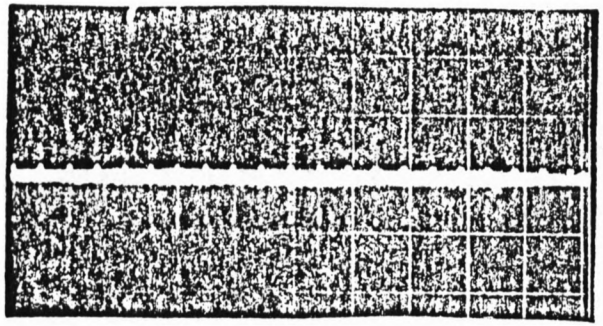
FIGURE 15

TB13-9, Blue, Quiescent Drive
50 V/DIV, 5 ms/DIV

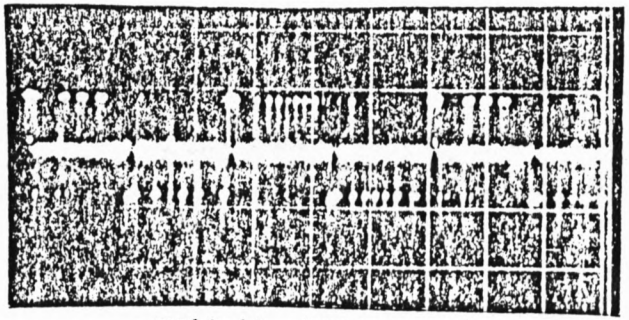
TB13-9, 100 pps Drive
50 V/DIV, 5 ms/DIV



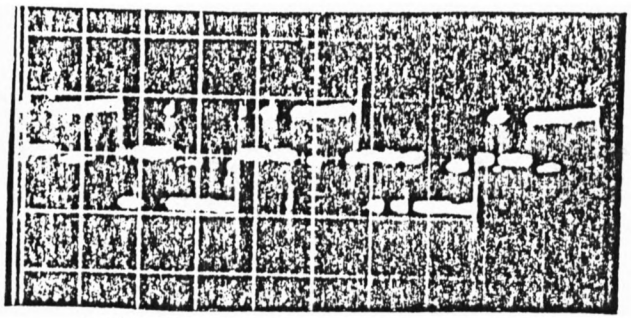
TB13-9, 500 pps Drive
50 V/DIV, 1 ms/DIV



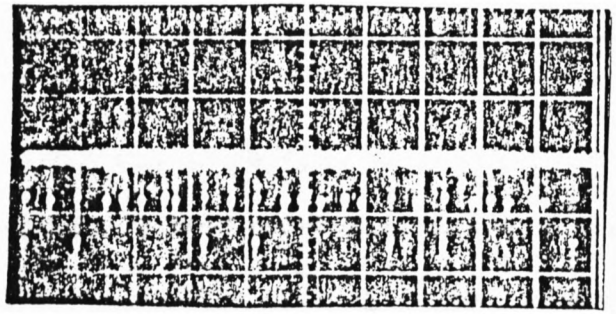
TB13-11, Orange, Quiescent Drive



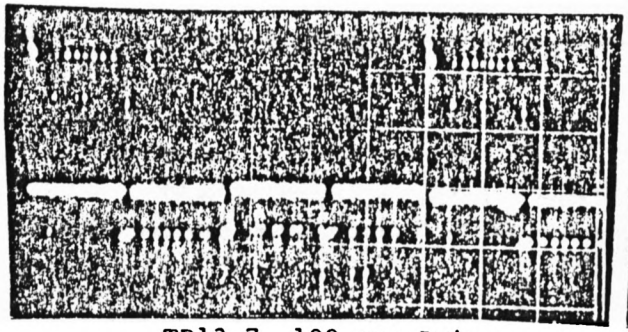
TB13-11, 100 pps Drive



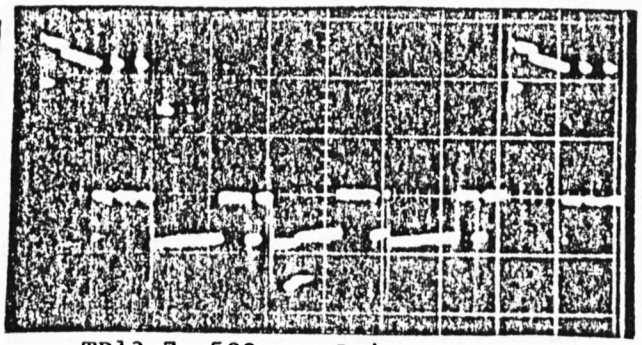
TB13-11, 500 pps Drive



TB13-7, Red, Quiescent Drive

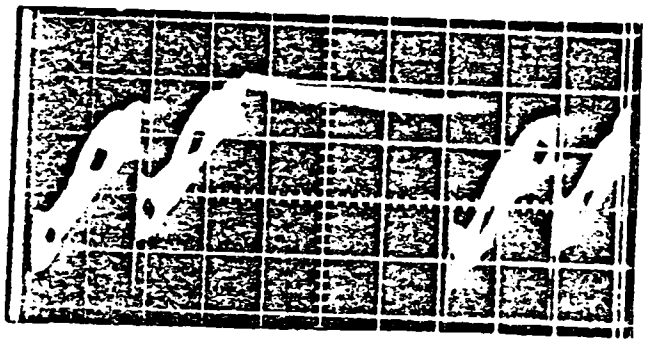


TB13-7, 100 pps Drive

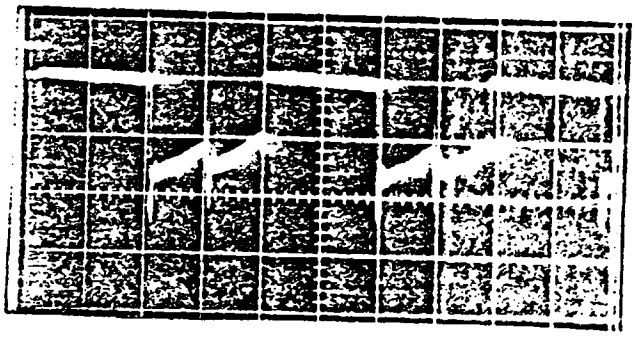


TB13-7, 500 pps Drive

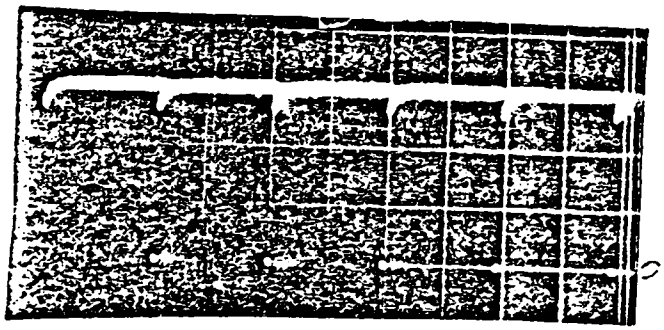
FIGURE 33a: TM-600 TRANSLATOR DRIVE WAVEFORMS IN PEDESTAL ROOM JUNCTION BOX, ANTENNA 21 THROUGH 28



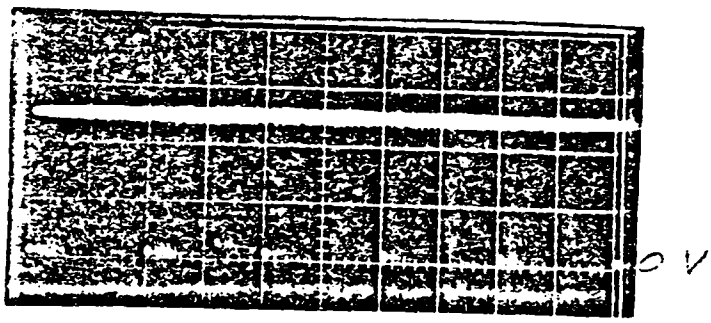
TB13-9 100 pps Drive
10 V/cm, 5 ms/cm



TB13-9 500 pps Drive
10 V/cm, 5 ms/cm



HTR-1008/1500 Drive Pulses
at F/R Control TP-14
500 pps, 5 V/cm, 1 ms/cm



TM-600 Drive Pulses
at F/R Control TP-14
500 pps, 2 V/cm, 1 ms/cm

FIGURE 33b: HTR-1008/1500 TRANSLATOR DRIVE WAVEFORMS, ANTENNA 1 THROUGH 20

10.0 SYSTEM FUNCTIONAL SPECIFICATIONS

SUBREFLECTOR POSITION EFFECTS ON ANTENNA POINTING ERROR

The following specifications were abstracted from a note by Peter Napier, 20/2/81 and are the design criteria for the F/R Controller and F/R Mount. These specifications are adequate for 22 GHz normal operation, or very high dynamic range observations at 1.5 and 5 GHz. The specifications result in some loss of performance if the VLA is used at 44 GHz.

Definitions:

$\Delta\theta$ = pointing error on sky
ΔX = movement of subreflector transverse to main reflector axis
$\Delta\alpha$ = tilt of subreflector orthogonal to main reflector axis
$\Delta\Theta$ = rotation of subreflector around main reflector axis
F = focal length of main reflector
M = cassegrain magnification
R = feed circle radius

Subreflector Transverse Movement Sensitivity:

$\Delta\theta = \Delta X/F$ for $\Delta\theta$ = 5 arc-sec, ΔX = 0.009 in.

Subreflector Tilt Sensitivity:

$\Delta\theta = 2*\Delta\alpha / M$ for $\Delta\theta$ = 5 arc-sec, $\Delta\alpha$ = 20 arc-sec.

Subreflector Rotation Sensitivity:

$\Delta\theta = \Delta\Theta*R/M*F$ for $\Delta\theta$ = 5 arc-sec, $\Delta\Theta$ = 6.8 arc-min

Focus Position Sensitivity:

A 0.20 wavelength position error causes a 5% gain loss. At a wavelength of 1.2 cm, ΔZ = 0.09 in, 2.25 mm.
Barry Clark says ΔZ should be less than 0.01 in, 0.25mm.

These last two parameters are associated with the two drive motions.

F/R CONTROL SYSTEM SPECIFICATIONS -- The F/R Control System design shall be sufficiently general so as to enable alteration of the control algorithms by changes to the control firmware and (if necessary), minor alteration of the hardware.

The controller shall be designed such that the F/R Mount hardware is given maximum protection from damaging conditions such as over-drive into the stops, sensing of dragging or stuck drives etc.

The controller shall be capable of concurrent, asynchronous control of two subreflector axes and ring position. There shall be two commands for each Subreflector axis: a 14 bit, 2's complement, right justified POSITION command (Mux 320/Focus, Mux 330/Rot) and a NAP command (Mux 322/Foc, 332/Rot) to cause position commands to be ignored until cleared by a RESET command. The SYSTEM RESET command (Mux 337) aborts active commands in both processors and re-initializes the programs. A software RESET command (Mux 321 & 331) performs the same functions in the addressed processor without affecting the other one. The Ring command (Mux 336/Rot) argument shall be a right justified (lsb) single bit arguement of 1 to EXTEND the ring and a 0 to RETRACT the Ring.

The controller shall be capable of accepting over-riding commands during command execution. If the over-riding command is to a different set point than the command in execution, the controller shall first slow the drive to a stop and then initiate execution of the new command.

The controller shall have both COMPUTER (ie central control computer) and LOCAL manual modes to permit manual slew of the drives from the local control panel. In the LOCAL mode, all components are driven under processor control to provide fault sensing and protection to the F/R Mount.

Zot-Box provisions shall be made to permit manual control of the drives from both the Apex and Pedestal Room.

Position Readout resolution shall be 14 bit. One lsb = 1.318 arc-min in Rotation and 0.0007324 inches (0.0188 mm) in Focus.

Position Readout repeatability of the synchro/converter combination shall be +/- 1 count.

Linearity of the synchro/converter combination shall be 10 arc-min or less, rms, (principally determined by the synchro linearity)

Common-mode noise rejection of Synchro-to-Digital Converters shall be > 80 db.

Position Readout transducers shall be size 15, 400 Hz, 26 VRMS, (rotor voltage) synchro transmitters.

The controller position servo control repeatability shall be +/- 1 count (mechanism slop not included in this spec.)

The controller shall continuously sense all limit sensor states and hardware-inhibit further drive into the limit (but not out of the limit) in the event that these limits are reached.

The Apex Interface shall continuously sense obviously erroneous fault conditions (such as sensing concurrent limits, multiple pin switch actuation, etc). In the event that such conditions occur all drive outputs shall be inhibited.

The controller shall be protected from lightning effects by the use of an Apex Interface Unit which presents position and discrete data to the F/R Controller via optically-isolated lines. Lightning mitigating surge arrestors shall be used in all lines to the Apex.

Mechanism motion shall start at 100 Hz and the controller shall ramp the Rotation drive rate to 1000 Hz in 50 HZ steps. After ramp up, the drive shall move at 1000 Hz until a calculated ramp-down point is reached at which time the drives shall be ramped down to 100 Hz for convergence to the commanded set point. The ramp up duration is 5.1 seconds and the ramp down period is 2.5 seconds.

The Focus ramp up duration is 3.9 seconds and the ramp down period is 1.8 seconds.

The controller shall continuously analyze drive motion to sense motor torque breakage with a 50% motion analysis tolerance. In the event that torque breakage is detected, the controller shall reduce the drive rate to 100 Hz and attempt to complete the commanded motion by ramping drives up to 250 Hz (peak torque speed for these motors). In the event that the torque breaks again, the command shall be aborted. If torque breakage occurs, a fault flag shall be sent to the central control computers via Monitor Data.

In executing a position command, the controller shall determine that the Translator and brake are activated when commanded on and that the Translator voltage and Brake voltage and current are above test thresholds. In the event that these conditions are not met the controller shall set a fault flag for the central computers.

The controller shall continuously monitor analog voltages in the Apex Interface and shall set a fault flag in the event that any values are out of tolerance. Mechanism drive velocities shall be read out as Monitor Data.

The controller shall test the state of the Ring position discrete sensors when a Ring position command is in process. In the event that the sensors do not signal attainment of the commanded state within 16 seconds after command initiation, a fault flag shall be set. The state of the Ring position sensors shall be read out as monitor data.

The controller shall monitor the 400 Hz synchro excitor current load as an analog signal.

The controller shall have provisions to sense Antenna ID number to use as an address for antenna-peculiar control arguments.

The controller shall have up to 6k of control program memory EPROM sockets wired for each axis, (present usage is less than 2k).

The controller shall have provisions for each processor to pass arguments to the other. An example of a possible use is for the Rotation Controller to

pass position arguments to the Focus Controller to inhibit Focus drive when the Rotation drive is in a certain region.

The Apex Interface shall display the position of both axes in octal numeric displays and the state of Apex discretes on an LED array.

The M8 Power Supply shall have an LED display to indicate the state of processor functions such as Command Active, Translator power sensed, Brake voltage and current sensed, drive pulses present on the UP or Down etc lines to the Translators, etc.

The M8 Power Supply shall have hardware provisions to permit manual command of 8 wavelength Index Locking locations and display the PIN IN/OUT states and actuation of the 8 socket switches. These features shall also be capable of central computer control by modification of the Rotation Controller firmware, (not presently installed).

The Apex Interface shall sense and read out the temperature of the F/R Mount gear box to verify operation of the gear box heaters in cold weather.

When the controller receives a Focus command it shall test the argument against software limits and if found to be outside these limits the command shall be rejected. The purpose of this test is to prevent the Focus drive from being driven into the limits under computer control.

The controller shall contain a background timer to shut down the drives and abort the command in the event that a command is taking too long to execute. A time-out flag shall be set in the Monitor Data.

The controller shall have protective logic on multiple-line drive outputs in which there could be potentially damaging conditions resulting from more than one output being active at any given time. This is a protective feature to protect the mechanical hardware from the inadverdant effects of noise glitches etc. Examples of such devices are the Ring motor in which the Ring Extend And Ring Retract command outputs should not be concurrent.

A connector interlock line shall sense that any Bin I/O cable has been disconnected; in this event all drive outputs shall be inhibited.

11 APPENDIX

Rotation and Ring Control Program
Focus Control Program
List of related drawings
M7, M11, M8, M22 Assembly Drawings, IC location maps
Bin Wire list
Special Function Module Data Sheets: 8085, 8156, 8755, A/D, S/H, +10 reference, S/D Converter, temperature sensors, analog multiplexer

```
                ;       F/R MODULE-E CODE FOR FOCUS
                ;       MAY 30, 1985

                ;EQUATES

0000 =          PIPTA:  EQU     00H     ;PROM 1, PORT A
0001 =          PIPTB:  EQU     01H     ;PROM 1, PORT B
0002 =          PIDDA:  EQU     02H     ;PROM 1, PORT A DIR
0003 =          PIDDB:  EQU     03H     ;PROM 1, PORT B DIR
0008 =          P2PTA:  EQU     08H     ;PROM 2, PORT A
0009 =          P2PTB:  EQU     09H     ;PROM 2, PORT B
000A =          P2DDA:  EQU     0AH     ;PROM 2, PORT A DIR
000B =          P2DDB:  EQU     0BH     ;PROM 2, PORT B DIR
0010 =          RCMD:   EQU     10H     ;RAM CMD/STAT REG ADDR
0019 =          RMPTA:  EQU     19H     ;RAM PORT A
001A =          RMPTB:  EQU     1AH     ;RAM PORT B
001B =          RMPTC:  EQU     1BH     ;RAM PORT C
001C =          TIMLO:  EQU     1CH     ;TIMER LSB
001D =          TIMHI:  EQU     1DH     ;TIMER MSB
0028 =          POSL:   EQU     28H     ;POS LSB
0029 =          POSH:   EQU     29H     ;POS MSB
002A =          VEL:    EQU     2AH     ;VELOCITY
002B =          APDCR:  EQU     2BH     ;APEX DISCRETS
002C =          ANAL:   EQU     2CH     ;APEX ANA LSB
002D =          ANAH:   EQU     2DH     ;APEX ANA MSB
0030 =          DSCDL:  EQU     30H     ;DS CMD LSB
0031 =          DSCDH:  EQU     31H     ;DS CMD MSB
0032 =          DSDT1:  EQU     32H     ;DS DATA LSB
0033 =          DSDT2:  EQU     33H     ;DS DATA
0034 =          DSDT3:  EQU     34H     ;DS DATA MSB
0035 =          SHAEV:  EQU     35H     ;SHA EVENT
0038 =          AIPT:   EQU     38H     ;APEX DATA REQ
003B =          RES65:  EQU     3BH     ;RST 6.5 RESET
004F =          RMODE:  EQU     4FH     ;RAM MODE PORT: A,B,&C OUT
00FF =          PROUT:  EQU     0FFH    ;PROM PORT OUTPUT
0000 =          PRIN:   EQU     00H     ;PROM PORT INPUT
0019 =          RSTEN:  EQU     19H     ;SIM MASK, DISABLE 5.5
0000 =          FALSE:  EQU     0
00FF =          TRUE:   EQU     0FFH

                ;DATA SET TABLE

1500                    ORG     1500H   ;START OF RAM MEMORY

1500            POSD:   DS      3       ;MUX 220 - POSITION & STATUS BITS
1503            EAPD:   DS      3       ;    221 - ECHO-POS. & STATUS
1506            ECHO:   DS      3       ;    222 - CMD ECHO
1509            DSCR:   DS      3       ;    223 - RESPONES & CMD SENSE, CLK CONTROL
150C            ADCR:   DS      3       ;    224 - APEX DISCRETS & VELOCITY
150F            ANAD:   DS      3       ;    225 - ANALOG FAULTS & VOLTAGES
1512            FAUL:   DS      3       ;    226
1515            MUX:    DS      3       ;MUX 227

                ;VALUES & ARGUEMENTS

1518            FISTH:  DS      2       ;POSITION, UNSIGNED
```

```
181A            LSTPOS: DS      2       ;LAST POSITION
181C            CMDTMP: DS      2       ;TEMPARARY CMD
181E            ATVCMD: DS      2       ;ACTIVE CMD
1820            PIPAST: DS      1       ;EPROM PORT IMAGE
1821            PIPBST: DS      1       ;  "    "    "
1822            RMPAS:  DS      1       ;RAM PORT IMAGE
1823            RMPBS:  DS      1       ;  "    "    "
1824            RMPCS:  DS      1       ;  "    "    "
1825            MOTION: DS      1       ;MOTION ANALYSIS COUNTER
1826            RMPTO:  DS      1       ;RAMP TO THIS STEP
1827            STEP:   DS      1       ;CURRENT RAMP STEP
1828            TRAP:   DS      2       ;ADDRESS OF ERRO CODE
182A            AMUX:   DS      1       ;APEX MUX CNTR
182B            APAPTR: DS      1       ;APEX MUX POINTER
182C            APATAB: DS      16      ;APEX ANALOG STORAGE TABLE

                FLAGS:

183C            RESCMD: DS      1       ;RESET REQUEST
183D            DRVATV: DS      1       ;DRIVE ACTIVE
183E            MAPATV: DS      1       ;MAP ACTIVE
183F            DRVREQ: DS      1       ;DRIVE REQUEST
1840            MAPREQ: DS      1       ;MAP REQUEST
1841            ACCEL:  DS      1       ;OK TO ACCELERATE
1842            RAMPUP: DS      1       ;RAMP UP STAGE
1843            MAIN:   DS      1       ;MAIN DRIVE STAGE
1844            RAMPDN: DS      1       ;RAMP DOWN STAGE
1845            CONVRG: DS      1       ;CONVERGANCE STAGE
1846            DRVPLS: DS      1       ;4TH DRIVE PULSE OCCURED
1847            DIR:    DS      1       ;CURRENT DIRECTION
1848            LDIR:   DS      1       ;LAST DIRECTION
1849            RAMP:   DS      1       ;RAMPED UP OR NOT
184A            GETIT:  DS      1       ;GET IT THERE SOMEHOW
184B =          ENDFLG: EQU     $       ;END OF FLAGS

                ;RESET & INTERUPT

0000                    ORG     0
0000 F3                 DI
0001 C34000             JMP     INIT    ;GET THINGS ORGANIZED

0024                    ORG     24H     ;TRAP SERVICE
0024 F3                 DI
0025 C32006             JMP     BLAP    ;STOP, WHAT'S WRONG

002C                    ORG     2CH     ;RST 5.5
002C FB                 EI
002D C9                 RET             ;NOT USED

0034                    ORG     34H     ;RST 6.5 SEVICE
0034 F3                 DI
0035 C32306             JMP     TRPR    ;ACK CLKS

0038                    ORG     38H     ;OUT-OF-BOUNDS
0038 F3                 DI
0039 C34000             JMP     INIT

003C                    ORG     3CH     ;RST 7.5 SERVICE
003C F3                 DI
003D C37706             JMP     BURP    ;SERVICE D.S. REQ
```

```
                ;INITIALIZATION

0040                    ORG     40H

                INIT:
0040 311019             LXI     SP,1910H;SET STACK
0043 3E4F               MVI     A,RMODE
0045 D318               OUT     RCMD    ;SET RAM PORTS FOR OUTPUT
0047 3EFF               MVI     A,PROUT
0049 D302               OUT     P1DDA   ;SET PROM PORTS FOR OUTPUT
004B D303               OUT     P1DDB
004D 3E00               MVI     A,PRIN
004F D30A               OUT     P2DDA   ;SET PROM PORTS FOR INPUT
0051 D30B               OUT     P2DDB
0053 AF                 XRA     A
0054 D319               OUT     RMPTA   ;ZERO PORTS
0056 D31A               OUT     RMPTB
0058 D31B               OUT     RMPTC
005A D300               OUT     P1PTA
005C D301               OUT     P1PTB
005E 211018             LXI     H,1810H
0061 47                 MOV     B,A
                LOOP:                   ;CLEAR MEMORY
0062 77                 MOV     M,A
0063 23                 INX     H
0064 05                 DCR     B
0065 C26200             JNZ     LOOP
0068 D33B               OUT     RES65   ;SETUP INTERRUPTS
006A 3E19               MVI     A,RSTEN
006C 30                 DB      30H     ;SIM
006D FB                 EI

                ;****************************************
                ; SYSTEM HANDLING

                BOSS:
006E CDF904             CALL    DSTOR   ;GATHER DATA
0071 3A0518             LDA     ERRO+2
0074 E608               ANI     08H     ;CHECK IF APEX OK
0076 C21D01             JNZ     RSCMD   ;RESET SYSTEM IF NOT
0079 DB00               IN      P2PTA
007B E601               ANI     01H     ;CHECK FOR LOCAL MODE
007D CAC202             JZ      LOCAL
0080 3A3C18             LDA     RESCMD
0083 B7                 ORA     A       ;CHECK FOR SOFT RESET
0084 C20B01             JNZ     CMDRS
0087 3A3D18             LDA     DRVATV
008A B7                 ORA     A       ;CHECK FOR DRIVE ACTIVE
008B C23301             JNZ     CHKDRV
008E 3A3E18             LDA     MAPATV
0091 B7                 ORA     A       ;CHECK FOR MAP ACTIVE
0092 C2AE00             JNZ     APAOK   ;IF YES, IGNOR REQUESTS
0095 3A3F18             LDA     DRVREQ
0098 B7                 ORA     A       ;DRIVE REQUEST
0099 C25501             JNZ     DRVINT
009C 3A4018             LDA     MAPREQ
009F B7                 ORA     A       ;MAP REQUEST
00A0 CAAE00             JZ      APAOK
00A3 323E18             STA     MAPATV  ;SET ACTIVE
```

```
00A6 3A0518          LDA     ERR0+2
00A9 F620            ORI     20H     ;SHOW ACTIVE
00AB 320518          STA     ERR0+2
                APA0K:               ;CHECK APEX VOLTAGES
00AE 3A2B18          LDA     APAPTR  ;GET MUX POINTER
00B1 3C              INR     A       ;NEXT ANALOG TO LOOK AT
00B2 E607            ANI     07H     ; MOD 8
00B4 322B18          STA     APAPTR  ;SAVE NEW VALUE FOR NEXT PASS
00B7 F5              PUSH    PSW     ;SAVE FOR FURTHER USE
00B8 07              RLC             ;SHIFT LEFT FOR WORD INDEXING
00B9 4F              MOV     C,A     ;SAVE IN C
00BA 07              RLC             ;SHIFT AGAIN FOR 2 WORD INDEXING
00BB 5F              MOV     E,A     ;SAVE IN E
00BC 21FF06          LXI     H,ANATAB;VOLTAGE RANGES
00BF 1600            MVI     D,0     ;SET DE FOR INDEXING
00C1 19              DAD     D       ;POINT TO & GET LOW LIMIT IN DE
00C2 5E              MOV     E,M
00C3 23              INX     H
00C4 56              MOV     D,M
00C5 23              INX     H
00C6 E5              PUSH    H       ;SAVE POINTER
00C7 212C18          LXI     H,APATAB;APEX ANALOG STORAGE
00CA 0600            MVI     B,0     ;SET BC
00CC 09              DAD     B       ;FORM INDEX
00CD 4E              MOV     C,M     ;GET ADJUSTED VALUE INTO HL
00CE 23              INX     H
00CF 7E              MOV     A,M
00D0 E60F            ANI     0FH     ;MASK UNSED BITS
00D2 EE08            XRI     08H     ;FLIP SIGN BIT
00D4 67              MOV     H,A
00D5 69              MOV     L,C
00D6 E5              PUSH    H       ;SAVE ANALOG
00D7 CD9B04          CALL    RANGER  ;CHECK LOW LIMIT
00DA D1              POP     D       ;GET ANALOG
00DB E1              POP     H       ;GET POINTER
00DC 79              MOV     A,C
00DD B7              ORA     A       ;IF OUT-OF-RANGE, SET FAULT
00DE C2E800          JNZ     AHAFLT
00E1 7E              MOV     A,M     ;GET HIGH LIMIT
00E2 23              INX     H
00E3 66              MOV     H,M
00E4 6F              MOV     L,A
00E5 CD9B04          CALL    RANGER  ;CHECK HIGH LIMIT
                AHAFLT:
00E8 F1              POP     PSW     ;GET MUX POINTER BACK
00E9 47              MOV     B,A
00EA 04              INR     B
00EB 3E80            MVI     A,80H   ;BIT MASK
                FLTSFT:
00ED 07              RLC             ;ROTATE BIT TO POSITION
00EE 05              DCR     B
00EF C2ED00          JNZ     FLTSFT
00F2 57              MOV     D,A     ;OR MASK
00F3 2F              CMA
00F4 5F              MOV     E,A     ;AND MASK
00F5 79              MOV     A,C
00F6 B7              ORA     A       ;HAVE A FAULT
00F7 3A1118          LDA     AHAD+2
00FA C20101          JNZ     SETFLT
00FD A3              ANA     E       ;RESET BIT
```

```
00FE C30201          JMP     STRFLT
             SETFLT:
0101 B2              ORA     D       ;SET BIT
             STRFLT:
0102 321118          STA     ANAD+2
0105 321318          STA     FAUL+1  ;*ADDED FOR MUX 226
0108 C36E00          JMP     BOSS

             CMDR3:
010B AF              XRA     A
010C 320218          STA     POSD+2
010F 321218          STA     FAUL    ;*ADDED FOR MUX 226
0112 320518          STA     ERRO+2
0115 3A1418          LDA     FAUL+2  ;*ADDED FOR MUX 226
0118 E6E0            ANI     0E0H
011A 321418          STA     FAUL+2
             RSCMD:
011D 3100D9          LXI     SP,19D0H        ;RESET STACK POINTER
0120 CDE404          CALL    TSTOP
0123 CDAE02          CALL    DRVSTP
0126 CDD203          CALL    TRNOF
0129 213C18          LXI     H,FLAGS
012C 060F            MVI     B,(ENDFLG-FLAGS) AND 255
012E AF              XRA     A
             CLRLP:
012F 77              MOV     M,A
0130 23              INX     H
0131 05              DCR     B
0132 C22F01          JNZ     CLRLP
0135 C36E00          JMP     BOSS

             ;*************************************
             ; COMMAND POSITION HANDLER

             CHKDRV:
0138 3A3F18          LDA     DRVREQ
013B B7              ORA     A       ;DO WE HAVE A NEW CMD?
013C CA1002          JZ      DRVTST  ;IF NOT, WORK ON OLD CMD
013F 2A1C18          LHLD    CMDTMP  ;TEMPARAY CMD
0142 EB              XCHG
0143 2A1E18          LHLD    ATVCMD  ;GET ACTIVE CMD
0146 CD9B04          CALL    RANGER  ;CHECK IF |NEW-OLD| < 3
0149 CDB504          CALL    CLOSE
014C DA8C02          JC      CLRREQ  ;IF YES, CLEAR REQUEST
014F CDE404          CALL    TSTOP   ;STOP TIMER & DRIVE
0152 CDAE02          CALL    DRVSTP
             DRVINT:
0155 AF              XRA     A       ;CLEAR REQUESTS, FLAGS, & FAULTS
0156 324A18          STA     GETIT
0159 320218          STA     POSD+2
015C 321218          STA     FAUL    ;*ADDED FOR MUX 226
015F 322718          STA     STEP
0162 323F18          STA     DRVREQ
0165 324118          STA     ACCEL
0168 320518          STA     ERRO+2
016B 322518          STA     MOTION  ;INIT MOTION COUNTER
016E 3A1418          LDA     FAUL+2  ;*ADDED FOR MUX 226
0171 E6E0            ANI     0E0H
0173 321418          STA     FAUL+2
0176 2A1C18          LHLD    CMDTMP
```

```
0179 CD8C04          CALL    CMDCHK  ;CHECK COMMAND FOR OUT-OF-BOUNDS
017C D28D01          JNC     CMDOK
017F 3A0218          LDA     POSD+2
0182 F680            ORI     80H     ;IF NOT, SET OPERATOR FAULT
0184 320218          STA     POSD+2
0187 321218          STA     FAUL    ;*ADDED FOR MOUX 226
018A C36E00          JMP     BOSS
                CMDOK:
018D 221E18          SHLD    ATVCMD  ;MAKE TEMP CMD THE ACTIVE CMD
0190 CDF904          CALL    DSTOR
0193 3A4718          LDA     DIR
0196 324818          STA     LDIR    ;SETUP LAST DIRECTION
0199 2A1818          LHLD    POSTN
019C 221A18          SHLD    LSTPOS  ;SETUP LAST POSITION
019F 2A2318          LHLD    ERRD
01A2 CD0504          CALL    CLOSE   ;ERRD < 3
01A5 DA6E00          JC      BOSS    ;IF YES, NOT DO ANYTHING
01A8 210AFF          LXI     D,-83   ;FIND STEP TO RAMP TOO
01AB 0608            MVI     B,8
01AD 3A4A18          LDA     GETIT           ;GET IT THERE SOMEHOW?
01B0 B7              ORA     A
01B1 CABB01          JZ      DIV             ;IF NOT
01B4 0605            MVI     B,5
                DIV:
01B6 3EFF            MVI     A,-1 AND 255    ; A  WILL CONTIAN STEP TO RAMP TOO
                DIV1:
01B8 3C              INR     A
01B9 19              DAD     D
01BA D2B801          JC      DIV1
01BD B6              CMP     B
01BE D2C301          JC      AOK
01C1 05              DCR     B
01C2 78              MOV     A,B     ;IF A>B THEN A=B-1
                AOK:
01C3 322618          STA     RAMPD   ;SAVE RESULT
01C6 B7              ORA     A       ;IF A=0 DON'T RAMP
01C7 CAD201          JZ      NORMP
01CA 3EFF            MVI     A,TRUE
01CC 324118          STA     ACCEL   ;SETUP FOR RAMP
01CF 324218          STA     RAMPUP
                NORMP:
01D2 2F              CMA
01D3 324518          STA     CONVRG
01D6 CDF503          CALL    BRKON   ;DISENGAGE BRAKE & ACTIVATE TRANSLATOR
01D9 CDAF03          CALL    TRNON
01DC AF              XRA     A
01DD 329B18          STA     DSCR+2  ;UPDATE CLK IMAGE
01E0 D301            OUT     PIPTB   ;SET 100HZ
01E2 3A4718          LDA     DIR
01E5 B7              ORA     A       ;WHICH DIRECTION?
01E6 3A9A18          LDA     DSCR+1  ;GET CONTROL IMAGE
01E9 C2F101          JNZ     DOWN
01EC F608            ORI     08H     ;DRIVE UP
01EE C3F301          JMP     MOVIT
                DOWN:
01F1 F605            ORI     05H     ;DRIVE DOWN
                MOVIT:
01F3 329A18          STA     DSCR+1  ;UPDATE IMAGE
01F6 D300            OUT     PIPTA   ;SEND IT
01F8 210B04          LXI     H,EDRV
```

```
01FB 222818          SHLD    TRAP    ;SETUP ERROR HANDLER
01FE 21983A          LXI     H,15000 ;150 SECS
0201 CDC804          CALL    TIMER
0204 3EFF            MVI     A,TRUE
0206 323D18          STA     DRVATV  ;SET DRIVE ACTIVE
0209 C36E00          JMP     BOSS

             CLRREQ:
020C AF              XRA     A
020D 323F18          STA     DRVREQ  ;CLEAR CMD REQUEST
             DRVTST:
0210 CDF904          CALL    DSTOR   ;GET LATEST DATA
0213 DB28            IN      APDCR
0215 E604            ANI     04H     ;CHECK FOR BRAKE DISENGAGED
0217 CA5304          JZ      EBRK    ;BRAKE ERROR HANDLING
021A 3A4118          LDA     ACCEL
021D B7              ORA     A       ;CHECK FOR ACCELERATION
021E CA3602          JZ      PLOD    ;IF NOT, PLOD ALONG
0221 3A4218          LDA     RAMPUP
0224 B7              ORA     A       ;IN RAMP UP
0225 C24902          JNZ     ZIPUP   ;IF YES, RAMP UP
0228 3A4318          LDA     MAIN
022B B7              ORA     A       ;IN MAIN DRIVE
022C C25B02          JNZ     MAINCK  ;IF YES, CHECK WHEN TO RAMP DOWN
022F 3A4418          LDA     RAMPDN
0232 B7              ORA     A       ;IN RAMP DOWN
0233 C27402          JNZ     ZIPDN   ;IF YES, RAMP DOWN
             PLOD:
0236 3A4518          LDA     CONVRG
0239 B7              ORA     A       ;CONVERGING?
023A C28202          JNZ     MOVIN   ;IF YES, MOVE IN
023D CDE404          CALL    TSTOP   ;STOP TIMER
0240 CDAE02          CALL    DRVSTP  ;STOP DRIVE
0243 CDD203          CALL    TRNOF   ;TURN OFF TRANSLATOR
0246 C36E00          JMP     BOSS    ;SEE WHAT'S NEXT

             ZIPUP:
0249 3A2618          LDA     RMPTO   ;GET STEP TO RAMP TO
024C 4F              MOV     C,A
024D CD4D03          CALL    RMPUP   ;RAMP TO IT
0250 AF              XRA     A       ;RAMPUP TO MAIN
0251 324218          STA     RAMPUP
0254 2F              CMA
0255 324318          STA     MAIN
0258 C36E00          JMP     BOSS

             MAINCK:
025B 2A0318          LHLD    ERRD
025E 118700          LXI     D,0087H
0261 CD9B04          CALL    RANGER  ;AT THE RAMP DOWN POINT?
0264 79              MOV     A,C
0265 B7              ORA     A
0266 CA6E00          JZ      BOSS    ;NOT YET
0269 AF              XRA     A       ;IF YES, MAIN TO RAMPDN
026A 324318          STA     MAIN
026D 2F              CMA
026E 324418          STA     RAMPDN
0271 C36E00          JMP     BOSS

             ZIPDN:
```

```
0274 CD76#3          CALL    RMPDN   ;RAMP DOWN FROM CURRENT STEP
0277 AF              XRA     A       ;SET RAMPDN TO CONVERGE
0278 324418          STA     RAMPDN
027B 2F              CMA
027C 324518          STA     CONVRG
027F C36E#0          JMP     BOSS

             MOV1M:
0282 2A#318          LHLD    ERR0
0285 CD6504          CALL    CLOSE   ;WITHIN 3 COUNTS
0288 D292#2          JNC     MOV1
028B AF              XRA     A       ;IF YES, SET FOR SHUTDOWN
028C 324518          STA     CONVRG
028F C36E#0          JMP     BOSS
             MOV1:
0292 3A4718          LDA     DIR     ;CURRENT DIRECTION
0295 4F              MOV     C,A
0296 3A4818          LDA     LDIR    ;LAST DIRECTION
0299 B9              CMP     C       ;THE SAME?
029A CA6E#0          JZ      BOSS
029D 79              MOV     A,C     ;IF NOT, CHANGE DIRECTIONS
029E 324818          STA     LDIR    ;LAST DIR = CURRENT DIR
02A1 3A#A18          LDA     DSCR+1
02A4 EE#C            XRI     #CH     ;FLIP DIRECTION BITS
02A6 32#A18          STA     DSCR+1
02A9 D3##            OUT     PIPTA   ;CHANGE DIRECTION
02AB C36E#0          JMP     BOSS

             DRVSTP:
02AE CD76#3          CALL    RMPDN   ;MAKE SURE RAMPED DOWN
02B1 AF              XRA     A       ;CLEAR DRIVE ACTIVE
02B2 323D18          STA     DRVATV
02B5 3A#A18          LDA     DSCR+1
02B8 E6F2            ANI     #F2H    ;SHUT DOWN CLKS & DIR
02BA 32#A18          STA     DSCR+1
02BD D3##            OUT     PIPTA
02BF C31804          JMP     BRKOF   ;ENGAGE BRAKE

             ;**************************************
             ; LOCAL DRIVE HANDLER

             LOCAL:
02C2 CDAF#3          CALL    TRNON   ;TRANSLATOR ON WHILE IN LOCAL
02C5 AF              XRA     A
02C6 32#B18          STA     DSCR+2
02C9 D3#1            OUT     P1PTB   ;SET FOR 100HZ DRIVE
             LCL1:
02CB CDF?#4          CALL    DSTOR   ;GET DATA
02CE 3AJ518          LDA     ERR0+2
02D1 E6#8            ANI     08H     ;APEX FAULT
02D3 C21D#1          JNZ     RSCRD   ;IF YES, RESET SYSTEM
02D6 DB#9            IN      P2PTB   ;GET DIRECTION
02D8 E6#6            ANI     6
02DA FE#4            CPI     4
02DC CAF102          JZ      LUP     ;MOVE UP
02DF FE#2            CPI     2
02E1 CA1703          JZ      LDWN    ;MOVE DOWN
02E4 DB#8            IN      P2PTA
02E6 E6#1            ANI     #1H     ;STILL IN LOCAL?
02E8 CACB#2          JZ      LCL1
```

```
02EB CDD203          CALL    TRNOF   ;IF NOT, TRANSLATOR OFF
02EE C31D01          JMP     RSCMD   ;RESET SYSTEM

                     LUP:
02F1 CDF503          CALL    BRKON   ;DISENGAGE BRAKE
02F4 3A0A18          LDA     DSCR+1
02F7 F609            ORI     9       ;SETUP UP DIR
02F9 320A18          STA     DSCR+1
02FC D320            OUT     P1PTA
02FE DB09            IN      P2PTB
0300 E601            ANI     1       ;RAMP?
0302 CA0A03          JZ      LUP1
0305 0E07            MVI     C,7     ;IF YES, RAMP TO 400HZ
0307 CD4D03          CALL    RMPUP
                     LUP1:
030A CDF904          CALL    DSTOR   ;GET DATA
030D DB09            IN      P2PTB
030F E602            ANI     2       ;STILL MOVING UP
0311 CA0A03          JZ      LUP1
0314 C33A03          JMP     LSTOP   ;IF NOT, SHUT DOWN

                     LDWN:
0317 CDF503          CALL    BRKON   ;DISENGAGE BRAKE
031A 3A0A18          LDA     DSCR+1
031D F605            ORI     5       ;SETUP DOWN DRIVE
031F 320A18          STA     DSCR+1
0322 D320            OUT     P1PTA
0324 DB09            IN      P2PTB
0326 E601            ANI     1       ;RAMP?
0328 CA3003          JZ      LDWN1
032B 0E07            MVI     C,7     ;IF YES, RAMP TO 400HZ
032D CD4D03          CALL    RMPUP
                     LDWN1:
0330 CDF904          CALL    DSTOR
0333 DB09            IN      P2PTB
0335 E604            ANI     4       ;STILL MOVING DOWN
0337 CA3003          JZ      LDWN1
                     LSTOP:          ;IF NOT, SHUT DOWN
033A CD7603          CALL    RMPDN   ;RAMP DOWN
033D 3A0A18          LDA     DSCR+1
0340 E6F2            ANI     0F2H    ;TURN OFF CLKS & DIR
0342 320A18          STA     DSCR+1
0345 D300            OUT     P1PTA
0347 CD1804          CALL    BRKOF   ;ENGAGE BRAKE
034A C3C202          JMP     LOCAL

                     ;**************************************
                     ; RAMP UP & DOWN
                     ;ENTER WITH C=STEP TO AT, 1=100HZ >> 7=400HZ

                     RMPUP:
034D 3A4918          LDA     RAMP
0350 B7              ORA     A       ;RAMPED UP?
0351 C0              RNZ             ;RETURN IF RAMPED UP
0352 2F              CMA
0353 324918          STA     RAMP    ;SET TRUE
0356 211F07          LXI     H,CK100 ;START RAMP TABLE
0359 AF              XRA     A       ;CLEAR RAMP STEP
                     RPUP1:
035A 322718          STA     STEP    ;SAVE LATEST STEP
```

```
0350 0619           MVI     B,25    ;WAIT 100 DRIVE PULSES
035F 7E             MOV     A,M     ;GET STEP FREQUENCY
0360 32DB18         STA     DSCR+2
0363 D301           OUT     P1PTB   ;EXECUTE IT
                RPUP2:
0365 CDA003         CALL    WT65    ;WAIT FOR INTERUPT
0368 05             DCR     B
0369 C26503         JNZ     RPUP2
036C 23             INX     H       ;NEXT FREQUENCY
036D 3A2718         LDA     STEP
0370 3C             INR     A       ;NEXT STEP
0371 B9             CMP     C       ;HAVE DONE NUMBER OF STEPS?
0372 C25A03         JNZ     RPUP1
0375 C9             RET             ;IF YES

                RMPDN:
0376 3A4918         LDA     RAMP
0379 B7             ORA     A       ;RAMPED DOWN?
037A C8             RZ              ;RETURN IF RAMPED DOWN
037B AF             XRA     A
037C 324918         STA     RAMP    ;GET RAMP FALSE
037F 110700         LXI     D,CK100 ;POINT TO RAMP TABLE
0382 3A2718         LDA     STEP    ;GET STEP COUNT
0385 6F             MOV     L,A
0386 2600           MVI     H,0
0388 19             DAD     D       ;FORM POINTER
0389 3C             INR     A
038A 4F             MOV     C,A     ;NUMBER OF STEPS TO RAMP DOWN
                RPDN1:
038B 060C           MVI     B,12    ;WAIT 48 PULSES
038D 7E             MOV     A,M     ;GET FREQUENCY
038E 32DB18         STA     DSCR+2
0391 D301           OUT     P1PTB   ;SET IT
                RPDN2:
0393 CDA003         CALL    WT65    ;WAIT FOR INERUPT
0396 05             DCR     B
0397 C29303         JNZ     RPDN2
039A 2B             DCX     H       ;NEXT FREQUENCY
039B 0D             DCR     C       ;DONE STEPPING?
039C C28B03         JNZ     RPDN1
039F C9             RET             ;IF YES

                WT65:
03A0 CDF904         CALL    DSTOR   ;GET DATA
03A3 3A4618         LDA     DRVPLS
03A6 B7             ORA     A       ;INTERUPT?
03A7 CAA003         JZ      WT65
03AA AF             XRA     A       ;IF YES, CLEAR FLAG & RETURN
03AB 324618         STA     DRVPLS
03AE C9             RET

                ;****************************************
                ; TRANSLATOR & BRAKE CONTROL

                TRNON:
034F 213B04         LXI     H,ETRN
0352 2D3818         SHLD    TRAP
0355 21C400         LXI     H,100   ;ONE SEC
0358 CDC504         CALL    TIMER
035B 3A0A18         LDA     DSCR+1
```

```
03BE F680           ORI     80H
03C0 320A18         STA     DSCR+1
03C3 D300           OUT     P1PTA
                TRON:
03C5 CDF904         CALL    DSTOR
03C8 DB08           IN      P2PTA
03CA E610           ANI     10H
03CC CAC503         JZ      TRON
03CF C3E404         JMP     TSTOP

                TRNOF:
03D2 213E04         LXI     H,ETRN
03D5 222818         SHLD    TRAP
03D8 216400         LXI     H,100   ;ONE SEC
03DB CDCB04         CALL    TIMER
03DE 3A0A18         LDA     DSCR+1
03E1 E67F           ANI     7FH
03E3 320A18         STA     DSCR+1
03E6 D300           OUT     P1PTA
                TROFF:
03E8 CDF904         CALL    DSTOR
03EB DB08           IN      P2PTA
03ED E610           ANI     10H
03EF C2E803         JNZ     TROFF
03F2 C3E404         JMP     TSTOP

                BRKON:
03F5 215304         LXI     H,EBRK
03F8 222818         SHLD    TRAP
03FB 216400         LXI     H,100   ;ONE SEC
03FE CDCB04         CALL    TIMER
0401 3A0A18         LDA     DSCR+1
0404 F640           ORI     40H
0406 320A18         STA     DSCR+1
0409 D300           OUT     P1PTA
                BRK01:
040B CDF904         CALL    DSTOR
040E DB2B           IN      APDCR
0410 E604           ANI     4
0412 CA0B04         JZ      BRK01
0415 C3E404         JMP     TSTOP

                BRKOF:
0418 215304         LXI     H,EBRK
041B 222818         SHLD    TRAP
041E 216400         LXI     H,100   ;ONE SEC
0421 CDCB04         CALL    TIMER
0424 3A0A18         LDA     DSCR+1
0427 E6BF           ANI     0BFH
0429 320A18         STA     DSCR+1
042C D300           OUT     P1PTA
                BRKF1:
042E CDF904         CALL    DSTOR
0431 DB2B           IN      APDCR
0433 E604           ANI     4
0435 C22E04         JNZ     BRKF1
0438 C3E404         JMP     TSTOP

                ;*************************************
```

```
                ETRN:
043B 3A0A18             LDA     DSCR+1
043E E67F               ANI     7FH
0440 320A18             STA     DSCR+1
0443 D300               OUT     PIPTA
0445 3A0218             LDA     POSD+2
0448 F610               ORI     10H
044A 320218             STA     POSD+2
044D 321218             STA     FAUL    ;*ADDED FOR HUX 226
0450 C31D01             JMP     RSCMD

                EBRK:
0453 3A0A18             LDA     DSCR+1
0456 E6BF               ANI     0BFH
0458 320A18             STA     DSCR+1
045B D300               OUT     PIPTA
045D 3A0218             LDA     POSD+2
0460 F604               ORI     04H
0462 320218             STA     POSD+2
0465 321218             STA     FAUL    ;*ADDED FOR HUX 226
0468 C31D01             JMP     RSCMD

                EDRV:
046B 210019             LXI     H,1900H ;RESET STACK
046E 3A1418             LDA     FAUL+2  ;*ADDED FOR HUX 226
0471 F601               ORI     1
0473 321418             STA     FAUL+2
0476 3A2718             LDA     STEP
0479 FE04               CPI     4
047B DA8D04             JC      EDRV1
047E 3EFF               MVI     A,TRUE
0480 324A18             STA     GETIT   ;SET GET IT THERE SOMEHOW
0483 CDE404             CALL    TSTOP   ;STOP TIMER AND DRIVE
0486 CDAE02             CALL    DRVSTP
0489 AF                 XRA     A       ;CLEAR ACC FOR ENTRY
048A C35F01             JMP     DRVINI  ;INTO DRVINT
                EDRV1:
048D 3A0218             LDA     POSD+2  ;SET DRIVE FAULT
0490 F620               ORI     20H
0492 320218             STA     POSD+2
0495 321218             STA     FAUL    ;*ADDED FOR HUX 226
0498 C31D01             JMP     RSCMD   ;SYSTEM RESET

                ;************************************

                RANGER:                 ;HL=(HL-DE)
049B 7D                 MOV     A,L
049C 93                 SUB     E
049D 6F                 MOV     L,A
049E 7C                 MOV     A,H
049F 9A                 SBB     D
04A0 67                 MOV     H,A
04A1 0E00               MVI     C,0     ;C => +
04A3 F2AA04             JP      RNGR1
04A6 0D                 DCR     C
04A7 CDAD04             CALL    CMPHL
                RNGR1:
04AA 7D                 MOV     A,L
04AB B4                 ORA     H       ;ZERO FLAG SET IF HL=0
04AC C9                 RET             ;C=0 => +DIR
```

```
                CMPHL:
04AD 7C         MOV     A,H
04AE 2F         CMA
04AF 67         MOV     H,A
04B0 7D         MOV     A,L
04B1 2F         CMA
04B2 6F         MOV     L,A
04B3 23         INX     H
04B4 C9         RET

                CLOSE:                  ;HL < 3 ?
04B5 7C         MOV     A,H
04B6 B7         ORA     A
04B7 C0         RNZ
04B8 7D         MOV     A,L
04B9 FE02       CPI     2
04BB C9         RET

                CADCHK:
04BC 7C         MOV     A,H
04BD FE3A       CPI     3AH
04BF DAC404     JC      HIOK
04C2 37         STC
04C3 C9         RET
                HIOK:
04C4 FE05       CPI     05H
04C6 D8         RC
04C7 3F         CMC
04C8 C8         RZ
04C9 3F         CMC
04CA C9         RET

                TIMER:
04CB 3ECF       MVI     A,0CFH  ;ENABLE TIMER AFTER COUNT LOADED
04CD D318       OUT     RCMD
04CF 7D         MOV     A,L     ;HL CONTAIN TIMER PERIOD
04D0 D31C       OUT     TIMLO
04D2 7C         MOV     A,H
04D3 E63F       ANI     3FH
04D5 F680       ORI     80H     ;STOP ON TERMINAL COUNT
04D7 D31D       OUT     TIMHI
04D9 3A2418     LDA     RMPCS
04DC F610       ORI     10H     ;SET FOR 100HZ CLK
04DE 322418     STA     RMPCS
04E1 D318       OUT     RMPTC   ;START IT
04E3 C9         RET

                TSTOP:
04E4 3A2418     LDA     RMPCS
04E7 E6CF       ANI     0CFH    ;TURN CLK OFF
04E9 322418     STA     RMPCS
04EC D318       OUT     RMPTC
04EE 3E4F       MVI     A,4FH   ;STOP COUNTER
04F0 D318       OUT     RCMD
04F2 210000     LXI     H,INIT
04F5 222818     SHLD    TRAP    ;SHOULD TRAP HAPPEN
04F8 C9         RET

                ;****************************************
```

```
                DSTOR:
04F9 F5                 PUSH    PSW
04FA C5                 PUSH    B
04FB D5                 PUSH    D
04FC E5                 PUSH    H
04FD AF                 XRA     A
04FE D338               OUT     AIPT
0500 060A               MVI     B,10
                LP1:
0502 DB29               IN      PDSH
0504 E6C0               ANI     0C0H
0506 FE80               CPI     80H
0508 CA2405             JZ      LP2
050B 05                 DCR     B
050C C20205             JNZ     LP1
050F 3A0518             LDA     ERRO+2
0512 F608               ORI     08H
0514 320518             STA     ERRO+2
0517 E61E               ANI     1EH     ;*ADDED FOR HUX 226
0519 47                 MOV     B,A
051A 3A1418             LDA     FAUL+2
051D B0                 ORA     B
051E 321418             STA     FAUL+2
0521 C3C305             JMP     LP3
                LP2:
0524 3A0518             LDA     ERRO+2
0527 E6F7               ANI     0F7H
0529 320518             STA     ERRO+2
052C 3A1418             LDA     FAUL+2  ;*ADDED FOR HUX 226
052F E6F7               ANI     0F7H
0531 321418             STA     FAUL+2
0534 DB28               IN      POSL
0536 6F                 MOV     L,A
0537 DB29               IN      POSH
0539 E63F               ANI     3FH
053B 67                 MOV     H,A
053C 221818             SHLD    POSTN
053F EE20               XRI     20H
0541 67                 MOV     H,A
0542 220818             SHLD    POSD
0545 EE20               XRI     20H
0547 57                 MOV     D,A
0548 5D                 MOV     E,L
0549 2A1E18             LHLD    ATVCMD
054C CD9B04             CALL    RANGER
054F 220318             SHLD    ERRO
0552 79                 MOV     A,C
0553 324718             STA     DIR

0556 DB2A               IN      VEL
0558 EE80               XRI     80H
055A 6F                 MOV     L,A
055B 2600               MVI     H,0
055D 29                 DAD     H
055E 29                 DAD     H
055F 29                 DAD     H
0560 29                 DAD     H
0561 220C18             SHLD    ADCR
0564 DB2B               IN      APDCR
```

```
0566 E607           ANI     07H
0568 320E18         STA     ADCR+2
056B E603           ANI     03H
056D 47             MOV     B,A
056E 3A0218         LDA     POSD+2
0571 E6FC           ANI     0FCH
0573 B0             ORA     B
0574 320218         STA     POSD+2
0577 DB28           IN      APDCR
0579 E604           ANI     04H     ;BRAKE I*E
057B 0F             RRC
057C 47             MOV     B,A
057D 3A2318         LDA     RMPBS
0580 E6FD           ANI     0FDH
0582 B0             ORA     B
0583 322318         STA     RMPBS
0586 D31A           OUT     RMPTB

0588 DB2C           IN      ANAL
058A 6F             MOV     L,A
058B DB2D           IN      ANAH
058D EE02           XRI     2
058F 47             MOV     B,A
0590 E61E           ANI     1EH
0592 87             ADD     A
0593 67             MOV     H,A
0594 78             MOV     A,B
0595 E603           ANI     3
0597 B4             ORA     H
0598 67             MOV     H,A
0599 29             DAD     H
059A EB             XCHG            ;SAVE IN DE
059B E638           ANI     38H
            ;
059D B7             ORA     A
059E C2A605         JNZ     AROUND
05A1 EB             XCHG
05A2 221518         SHLD    NU2
05A5 EB             XCHG
            AROUND:
            ;
05A6 0F             RRC             ; /4
05A7 0F             RRC
05AB 6F             MOV     L,A     ;SETUP HL
05A9 2600           MVI     H,0
05AB 012C18         LXI     B,APATAB        ;GET APEX ANALOG TABLE ADDR
05AE 09             DAD     B       ;FORM INDEX
05AF 73             MOV     M,E     ;SAVE APEX ANALOG IN IT
05B0 23             INX     H
05B1 72             MOV     M,D
05B2 3A2A18         LDA     ANAMX
05B5 E607           ANI     07H     ; MOD 8
05B7 87             RLC             ; * 2
05B8 6F             MOV     L,A     ;SETUP HL
05B9 2600           MVI     H,0
05BB 09             DAD     B       ;FORM INDEX
05BC 7E             MOV     A,M     ;GET VALUE INTO HL
05BD 23             INX     H
05BE 66             MOV     H,M
05BF 6F             MOV     L,A
```

```
05C0 220F18          SHLD    AHAD    ;STORE IT FOR DATA SET
                     LP3:
05C3 3A3D18          LDA     DRVATV
05C6 B7              ORA     A
05C7 3A2318          LDA     RHPBS
05CA CAD405          JZ      LP4
05CD F601            ORI     01H
05CF 0E40            MVI     C,40H
05D1 C3D805          JMP     LP5
                     LP4:
05D4 E6FE            ANI     0FEH
05D6 0E00            MVI     C,0
                     LP5:
05D8 322318          STA     RHPBS
05DB D31A            OUT     RHPTB
05DD DB08            IN      P2PTA
05DF 320918          STA     DSCR
05E2 E607            ANI     07H
05E4 EE07            XRI     07H
05E6 47              MOV     B,A
05E7 3A0518          LDA     ERR0+2
05EA E688            ANI     088H
05EC B0              ORA     B
05ED B1              ORA     C
05EE 320518          STA     ERR0+2
05F1 E61E            ANI     1EH     ;*ADDED FOR MUX 226
05F3 47              MOV     B,A
05F4 3A1418          LDA     FAUL+2
05F7 E689            ANI     089H    ;STRIP INFO
05F9 B0              ORA     B       ;AND UPDATE INFO
05FA 321418          STA     FAUL+2
05FD E1              POP     H
05FE D1              POP     D
05FF C1              POP     B
0600 F1              POP     PSW
0601 C9              RET

                     ;****************************************

                     BLAP:
0602 310019          LXI     SP,1900H
0605 2A2818          LHLD    TRAP
0608 E5              PUSH    H
0609 CDE404          CALL    TSTOP
060C 3A0518          LDA     ERR0+2
060F F610            ORI     10H
0611 320518          STA     ERR0+2
0614 3A1418          LDA     FAUL+2  ;*ADDED FOR MUX 226
0617 F610            ORI     10H
0619 321418          STA     FAUL+2
061C D338            OUT     RES65
061E 3E19            MVI     A,RSTEN ;RESET 7.5, DISABLE 5.5
0620 30              DB      30H     ;SIM
0621 FB              EI
0622 C9              RET             ;GOTO ERROR HANDLER

                     TRPR:
0623 D338            OUT     RES65   ;RESET 6.5
0625 FB              EI
0626 F5              PUSH    PSW
```

```
0627 C5             PUSH   B
0628 D5             PUSH   D
0629 E5             PUSH   H
062A 3EFF           MVI    A,TRUE
062C 324618         STA    DRVPLS
062F DB08           IN     P2PTA   ;IN LOCAL?
0631 E601           ANI    01H
0633 CA6E06         JZ     TRPR1
0636 3A0A18         LDA    DSCR+1
0639 E60C           ANI    0CH
063B CA6E06         JZ     TRPR1
063E 3A2518         LDA    MOTION
0641 3C             INR    A
0642 FE19           CPI    25
0644 C26F06         JNZ    TRPR2
0647 2A1A18         LHLD   LSTPOS
064A EB             XCHG
064B 2A1818         LHLD   POSTN
064E 221A18         SHLD   LSTPOS
0651 3A4A18         LDA    GETIT           ;IN GET IT THERE?
0654 B7             ORA    A
0655 C26006         JNZ    TRPR0           ;IF IN GET IT THERE
0658 3A2718         LDA    STEP            ;GET STEP
065B FE02           CPI    2
065D DA6E06         JC     TRPR1
            TRPR0:
0660 CD9304         CALL   RANGER
0663 7C             MOV    A,H
0664 B7             ORA    A
0665 C26B04         JNZ    EDRV    ;ERROR IN MOTION
0668 7D             MOV    A,L
0669 FE2B           CPI    43
066B DA6B04         JC     EDRV    ;ERROR IN MOTION
            TRPR1:
066E AF             XRA    A
            TRPR2:
066F 322518         STA    MOTION
0672 E1             POP    H
0673 D1             POP    D
0674 C1             POP    B
0675 F1             POP    PSW
0676 C9             RET

            BURP:
0677 F5             PUSH   PSW
0678 C5             PUSH   B
0679 D5             PUSH   D
067A E5             PUSH   H
067B DB35           IN     SHAEV   ;READ SHA-EVENT REG
067D 47             MOV    B,A
067E E607           ANI    07H
0680 4F             MOV    C,A
0681 78             MOV    A,B
0682 E638           ANI    38H
0684 FE20           CPI    20H
0686 CA9C06         JZ     CHDRQ
0689 FE10           CPI    10H
068B CADF06         JZ     DTAPQ
068E 3A0218         LDA    POSD+2
0691 F640           ORI    40H     ;SET CONTROLLER FAULT
```

```
0693 320218          STA     FOSD+2
0696 321218          STA     FAUL    ;*ADDED FOR MUX 226
0699 C3F906          JMP     SKIP
                CMDRQ:
069C DB30            IN      DSCDL
069E 6F              MOV     L,A
069F DB31            IN      DSCDH
06A1 67              MOV     H,A
06A2 E63F            ANI     3FH
06A4 EE20            XRI     20H
06A6 57              MOV     D,A
06A7 5D              MOV     E,L
06A8 06FF            MVI     B,TRUE
06AA 79              MOV     A,C
06AB B7              ORA     A
06AC CAC306          JZ      DRVCMD
06AF FE01            CPI     1
06B1 CAD106          JZ      CMDRST
06B4 FE02            CPI     2
06B6 CAD806          JZ      MAPSET
06B9 221518          SHLD    MU2
06BC 79              MOV     A,C
06BD 321718          STA     MU2+2
06C0 C3F906          JMP     SKIP
                DRVCMD:
06C3 220618          SHLD    ECHO
06C6 EB              XCHG
06C7 221C18          SHLD    CMDTMP
06CA 78              MOV     A,B
06CB 323F18          STA     DRVREQ
06CE C3F906          JMP     SKIP
                CMDRST:
06D1 76              MOV     A,B
06D2 323C18          STA     RESCMD
06D5 C3F906          JMP     SKIP
                MAPSET:
06D8 78              MOV     A,B
06D9 324018          STA     MAPREQ
06DC C3F906          JMP     SKIP
                DTARQ:
06DF 79              MOV     A,C
06E0 FE05            CPI     5
06E2 C2E906          JNZ     DRQ1
06E5 212A18          LXI     H,AMAMX ;POINT TO COUNTER
06E8 34              INR     M       ;INCREMENT POINTER
                DRQ1:
06E9 07              RLC
06EA 81              ADD     C
06EB 6F              MOV     L,A
06EC 2618            MVI     H,18H
06EE 7E              MOV     A,M
06EF D332            OUT     DSDT1
06F1 23              INX     H
06F2 7E              MOV     A,M
06F3 D333            OUT     DSDT2
06F5 23              INX     H
06F6 7E              MOV     A,M
06F7 D334            OUT     DSDT3
                SKIP:
06F9 E1              POP     H
```

```
06FA D1             POP     D
06FB C1             POP     B
06FC F1             POP     PSW
06FD FB             EI
06FE C9             RET

                    ;**************************************

                    ;ANALOG TABLE   LO    HI
                    ANATAB:
06FF EA07FE0B       DW      07EAH,0BFEH     ;MOUNT TEMP
0703 FC042805       DW      04FCH,0528H     ;-15/4
0707 D86A840B       DW      0AD8H,0B04H     ;+15/4
070B B60BFE0B       DW      0BB6H,0BFEH     ;+ 5
070F E40EEC0B       DW      0BE4H,0BECH     ;+10/2
0713 0000FF0F       DW      0000H,0FFFH     ;FOC VEL
0717 0000FF0F       DW      0000H,0FFFH     ;ROT VEL
071B FC079408       DW      07FCH,0804H     ;GND

                    ;RAMP TABLE

        071F 00     CK100:  DB      00H
        0720 34     CK150:  DB      34H
        0721 50             DB      50H
        0722 60             DB      60H
        0723 67             DB      67H
        0724 71             DB      71H
        0725 75     CK400:  DB      75H
        0726 78             DB      78H
        0727 80             DB      80H
        0728 82             DB      82H
        0729 83             DB      83H
        072A 85             DB      85H
        072B 86             DB      86H
        072C 87             DB      87H
        072D 88             DB      88H
        072E 89             DB      89H
        072F 90     CK1000: DB      90H

                    ;**************************************

        0730                END     0
```

```
                ;       F/R MODLE-E CODE FOR ROTATION
                ;       MAY 30, 1985

                ;EQUATES

0000 =          P1PTA:  EQU     00H     ;PROM 1, PORT A
0001 =          P1PTB:  EQU     01H     ;PROM 1, PORT B
0002 =          P1DDA:  EQU     02H     ;PROM 1, PORT A DIR
0003 =          P1DDB:  EQU     03H     ;PROM 1, PORT B DIR
0008 =          P2PTA:  EQU     08H     ;PROM 2, PORT A
0009 =          P2PTB:  EQU     09H     ;PROM 2, PORT B
000A =          P2DDA:  EQU     0AH     ;PROM 2, PORT A DIR
000B =          P2DDB:  EQU     0BH     ;PROM 2, PORT B DIR
0018 =          RCMD:   EQU     18H     ;RAM CMD/STAT REG ADDR
0019 =          RAPTA:  EQU     19H     ;RAM PORT A
001A =          RAPTB:  EQU     1AH     ;RAM PORT B
001B =          RAPTC:  EQU     1BH     ;RAM PORT C
001C =          TIMLO:  EQU     1CH     ;TIMER LSB
001D =          TIMHI:  EQU     1DH     ;TIMER MSB
0028 =          POSL:   EQU     28H     ;POS LSB
0029 =          POSH:   EQU     29H     ;POS MSB
002A =          VEL:    EQU     2AH     ;VELOCITY
002B =          APDCR:  EQU     2BH     ;APEX DISCRETS
002C =          AHAL:   EQU     2CH     ;APEX AHA LSB
002D =          AHAH:   EQU     2DH     ;APEX AHA MSB
0030 =          DSCDL:  EQU     30H     ;DS CMD LSB
0031 =          DSCDH:  EQU     31H     ;DS CMD MSB
0032 =          DSDT1:  EQU     32H     ;DS DATA LSB
0033 =          DSDT2:  EQU     33H     ;DS DATA
0034 =          DSDT3:  EQU     34H     ;DS DATA MSB
0035 =          SHAEV:  EQU     35H     ;SHA EVENT
0038 =          AIPT:   EQU     38H     ;APEX DATA REQ
003B =          RES65:  EQU     3BH     ;RST 6.5 RESET
004F =          RMODE:  EQU     4FH     ;RAM MODE PORT: A,B,&C OUT
00FF =          PROUT:  EQU     0FFH    ;PROM PORT OUTPUT
0000 =          PRIN:   EQU     00H     ;PROM PORT INPUT
0019 =          RSTEN:  EQU     19H     ;SIM MASK, DISABLE 5.5 ONLY
0000 =          FALSE:  EQU     0
00FF =          TRUE:   EQU     0FFH

                ;DATA SET TABLE

1800                    ORG     1800H   ;START OF RAM MEMORY

1800            POSD:   DS      3       ;MUX 230 - POSITION & STATUS BITS
1803            ERRD:   DS      3       ;    231 - CMD-POS & STATUS BITS
1806            ECHD:   DS      3       ;    232 - CMD ECHO
1809            DSCR:   DS      3       ;    233 - RESPONES & CMD SENSE, CLK CONTROL
180C            ADCR:   DS      3       ;    234 - APEX DISCRETS & VELOCITY
180F            AHAD:   DS      3       ;    235 - ANALOG FAULTS & VOLTAGES
1812            FAUL:   DS      3       ;    236
1815            MUX:    DS      3       ;MUX 237

                ;VALUES & REQUEMENTS

1818            POSTN:  DS      2       ;POSITION, UNSIGNED
```

```
181A            LSTPOS: DS      2       ;LAST POSITION
181C            CMDTMP: DS      2       ;TEMPARARY CMD
181E            ATVCMD: DS      2       ;ACTIVE CMD
1820            PIPAST: DS      1       ;EPROM IMAGE
1821            PIPBST: DS      1       ;EPROM IMAGE
1822            RMPAS:  DS      1       ;RAM IMAGE
1823            RMPBS:  DS      1       ;RAM IMAGE
1824            RMPCS:  DS      1       ;RAM IMAGE
1825            MOTION: DS      1       ;MOTION ANALYSIS COUNTER
1826            STEP:   DS      1       ;FREQUENCY STEP FOR RAMP
1827            RMPTO:  DS      1       ;RAMP TO THIS SPEED
1828            TRAP:   DS      2       ;ADDRESS OF ERRO CODE
182A            ANAMX:  DS      1       ;APEX MUX CNTR
182B            APAPTR: DS      1       ;APEX MUX POINTER
182C            APATAB: DS      16      ;APEX ANALOG STORAGE

                FLAGS:

183C            RESCMD: DS      1       ;RESET CMD
183D            DRVATV: DS      1       ;DRIVE ACTIVE
183E            MAPATV: DS      1       ;MAP ACTIVE
183F            DRVREQ: DS      1       ;DRIVE REQUEST
1840            MAPREQ: DS      1       ;MAP REQUEST
1841            ACCEL:  DS      1       ;OK TO ACCELERATE
1842            RAMPUP: DS      1       ;RAMP UP STAGE
1843            MAIN:   DS      1       ;MAIN DRIVE STAGE
1844            RAMPDN: DS      1       ;RAMP DOWN STAGE
1845            CONVRG: DS      1       ;CONVERGANCE STAGE
1846            DRVPLS: DS      1       ;4TH DRIVE PULSE OCCURED
1847            DIR:    DS      1       ;CURRENT DIRECTION
1848            LDIR:   DS      1       ;LAST DIRECTION
1849            RAMP:   DS      1       ;RAMPED UP OR NOT
184A            GETIT:  DS      1       ;GET IT THERE SOMEHOW
184B            RNGCMD: DS      1       ;WAITING RING COMMAND
184C            EXTFLG: DS      1       ;RING EXTEND FLAG
184D =          ENDFLG: EQU     $       ;END OF FLAGS

                ;RESET & INTERUPT

0000                    ORG     0
0000 F3                 DI
0001 C34000             JMP     INIT    ;GET THINGS ORGANIZED

0024                    ORG     24H     ;TRAP SERVICE
0024 F3                 DI
0025 C31307             JMP     BLAP    ;STOP, WHAT'S WRONG

002C                    ORG     2CH     ;RST 5.5
002C FB                 EI
002D C9                 RET             ;NOT USED

0034                    ORG     34H     ;RST 6.5 SEVICE
0034 F3                 DI
0035 C33407             JMP     TRPR    ;ACKNOLEDGE DRIVE PULSES

0038                    ORG     38H     ;OUT-OF-BOUNDS
0038 F3                 DI
0039 C34000             JMP     INIT

003C                    ORG     3CH     ;RST 7.5 SERVICE
```

```
003C F3             DI
003D C3B807         JMP     BURP    ;SERVICE D.S. REQ

                    ;INITIALIZATION

0040                ORG     40H

                    INIT:
2040 310919         LXI     SP,1900H;SET STACK
0043 3E4F           MVI     A,RMODE
0045 D318           OUT     RCMD    ;SET RAM PORTS FOR OUTPUT
0047 3EFF           MVI     A,PROUT
0049 D302           OUT     P1DDA   ;SET PROM PORTS FOR OUTPUT
004B D303           OUT     P1DDB
004D 3E00           MVI     A,PRIN
004F D30A           OUT     P2DDA   ;SET PROM PORTS FOR INPUT
0051 D30B           OUT     P2DDB
0053 AF             XRA     A
0054 D319           OUT     RMPTA   ;ZERO PORTS
0056 D31A           OUT     RMPTB
0058 D31B           OUT     RMPTC
005A D300           OUT     P1PTA
005C D301           OUT     P1PTB
005E 211918         LXI     H,1800H
0061 47             MOV     B,A
                    LOOP:               ;CLEAR MEMORY
0062 77             MOV     M,A
0063 23             INX     H
0064 05             DCR     B
0065 C26200         JNZ     LOOP
0068 D33B           OUT     RES65   ;SETUP INTERRUPTS
006A 3E19           MVI     A,RSTEN
006C 30             DB      30H     ;SIM
006D FB             EI

                    ;****************************************
                    ; SYSTEM HANDLING

                    BOSS:
006E CDFE05         CALL    DSTOR   ;GATHER DATA
0071 3A0518         LDA     ERRO+2
0074 E608           ANI     08H     ;CHECK APEX INTERFACE OK
0076 C22501         JNZ     RSCMD   ;RESET SYSTEM IF NOT
0079 DB32           IN      P2PTA
007B E601           ANI     01H     ;CHECK FOR LOCAL MODE
007D CAB602         JZ      LOCAL
0080 3A3C18         LDA     RESCMD
0083 B7             ORA     A       ;CHECK FOR SOFT RESET
0084 C21301         JNZ     CMDRS
0087 3A3D18         LDA     DRVATV
008A B7             ORA     A       ;CHECK DRIVE ACTIVE
008B C24001         JNZ     CHKDRV
008E 3A0518         LDA     ERRO+2
0091 E680           ANI     80H     ;CHECK RING ACTIVE
0093 C23305         JNZ     CHKRNG
0096 3A3E18         LDA     MAPATV
0099 B7             ORA     A       ;CHECK MAP ACTIVE
009A C2B600         JNZ     APROK   ;IGNOR REQUESTS
009D 3A3F18         LDA     DRVREQ
00A0 B7             ORA     A       ;DRIVE REQUEST
```

```
00A1 C25D01          JNZ     ORVINT
00A4 3A4018          LDA     MAPREQ
00A7 B7              ORA     A       ;MAP REQUEST
00A8 CAB600          JZ      APAOK
00AB 323E18          STA     MAPATV  ;SET ACTIVE
00AE 3A0518          LDA     ERR0+2
00B1 F620            ORI     20H     ;SHOW ACTIVE
00B3 320518          STA     ERR0+2
                APAOK:               ;CHECK APEX VOLTAGES
00B6 3A2B18          LDA     APAPTR  ;GET MUX POINTER
00B9 3C              INR     A       ;NEXT ANALOG TO LOOK AT
00BA E607            ANI     07H     ; MOD 8
00BC 322B18          STA     APAPTR  ;SAVE NEW VALUE FOR NEXT PASS
00BF F5              PUSH    PSW     ;SAVE FOR FURTHER USE
00C0 07              RLC             ;SHIFT LEFT FOR WORD INDEXING
00C1 4F              MOV     C,A     ;SAVE IN C
00C2 07              RLC             ;SHIFT AGAIN FOR 2 WORD INDEXING
00C3 5F              MOV     E,A     ;SAVE IN E
00C4 213B00          LXI     H,ANATAB;VOLTAGE RANGES
00C7 1600            MVI     D,0     ;SET DE FOR INDEXING
00C9 19              DAD     D       ;POINT TO & GET LOW LIMIT IN DE
00CA 5E              MOV     E,M
00CB 23              INX     H
00CC 56              MOV     D,M
00CD 23              INX     H
00CE E5              PUSH    H       ;SAVE POINTER
00CF 212C18          LXI     H,APATAB;APEX ANALOG STORAGE
00D2 0600            MVI     B,0     ;SET BC
00D4 09              DAD     B       ;FORM INDEX
00D5 4E              MOV     C,M     ;GET ADJUSTED VALUE INTO HL
00D6 23              INX     H
00D7 7E              MOV     A,M
00D8 E60F            ANI     0FH
00DA EE08            XRI     08H
00DC 67              MOV     H,A
00DD 69              MOV     L,C
00DE E5              PUSH    H       ;SAVE ANALOG
00DF CDAF05          CALL    RANGER  ;CHECK LOW LIMIT
00E2 D1              POP     D       ;GET ANALOG
00E3 E1              POP     H       ;GET POINTER
00E4 79              MOV     A,C
00E5 B7              ORA     A       ;IF OUT-OF-RANGE, GO SET FAULT
00E6 C2F000          JNZ     ANAFLT
00E9 7E              MOV     A,M     ;GET HIGH LIMIT
00EA 23              INX     H
00EB 66              MOV     H,M
00EC 6F              MOV     L,A
00ED CDAF05          CALL    RANGER  ;CHECK HIGH LIMIT
                ANAFLT:
00F0 F1              POP     PSW     ;GET MUX POINTER BACK
00F1 47              MOV     B,A
00F2 04              INR     B
00F3 3E80            MVI     A,80H   ;BIT MASK
                FLTSFT:
00F5 07              RLC             ;ROTATE BIT TO POSITION
00F6 05              DCR     B
00F7 C2F500          JNZ     FLTSFT
00FA 57              MOV     D,A     ;OR MASK
00FB 2F              CMA
00FC 5F              MOV     E,A     ;AND MASK
```

```
00FD 79             MOV     A,C
00FE B7             ORA     A       ;HAVE A FAULT
00FF 3A1118         LDA     AHAD+2
0102 C20901         JNZ     SETFLT
0105 43             MOV     E       ;RESET BIT
0106 C30A01         JMP     STRFLT
                    SETFLT:
0109 B2             ORA     D       ;SET BIT
                    STRFLT:
010A 321118         STA     AHAD+2
010D 321319         STA     FAUL+1  ;*ADDED FOR MUX 236
0110 C36E00         JMP     BOSS

                    CHDRS:
0113 AF             XRA     A       ;CLEAR FAULTS
0114 320218         STA     POSD+2
0117 321218         STA     FAUL    ;*ADDED FOR MUX 236
011A 320518         STA     ERRO+2
011D 3A1416         LDA     FAUL+2  ;*ADDED FOR MUX 236
0120 E6E0           ANI     0E0H
0122 321418         STA     FAUL+2
                    RSCMD:
0125 310019         LXI     SP,1900H;RESET STACK
0128 CDE905         CALL    TSTOP   ;STOP TIMER & DRIVE
012B CDA202         CALL    DRVSTP
012E CDCE04         CALL    TRNOF   ;TURN OFF TRANSLATOR
0131 213C18         LXI     H,FLAGS
0134 0611           MVI     B,(ENDFLG-FLAGS) AND 255
0136 AF             XRA     A
                    CLRLP:          ;CLEAR FLAG TABLE
0137 77             MOV     M,A
0138 23             INX     H
0139 05             DCR     B
013A C23701         JNZ     CLRLP
013D C36E00         JMP     BOSS

                    ;****************************************
                    ; COMMAND POSITION HANDLER

                    CHKDRV:
0140 3A3F18         LDA     DRVREQ
0143 B7             ORA     A       ;DO WE HAVE A NEW CMD
0144 CA8402         JZ      DRVTST  ;IF NO WORK ON OLD CMD
0147 2A1C18         LHLD    CMDTMP
014A EB             XCHG
014B 2A1E18         LHLD    ATVCMD
014E CD9705         CALL    VECTOR  ;CHECK IF (NEW-OLD) < 4
0151 CDC905         CALL    CLOSE
0154 DA0002         JC      CLRREQ  ;IF YES CLEAR REQUEST
0157 CDE905         CALL    TSTOP   ;STOP TIMER AND DRIVE
015A CDA202         CALL    DRVSTP
                    DRVINT:
015D AF             XRA     A       ;CLEAR REQUESTS,FLAGS, AND FAULTS
015E 324A18         STA     GETIT
0161 320218         STA     POSD+2
0164 321218         STA     FAUL    ;*ADDED FOR MUX 236
0167 322618   DRVINI: STA    STEP
016A 323F18         STA     DRVREQ
016D 324118         STA     ACCEL
0170 320518         STA     ERRO+2
```

```
0173 322518          STA     MOTION  ;INITIALIZE MOTION COUNTER
0176 3A1418          LDA     FAUL+2  ;*ADDED FOR MUX 236
0179 E6E0            ANI     0E0H
017B 321418          STA     FAUL+2
017E 2A1C18          LHLD    CMDTMP
0181 221E18          SHLD    ATVCMD  ;MAKE TEMP CMD THE ACTIVE CMD
0184 CDFE05          CALL    DSTOR
0187 3A4718          LDA     DIR
018A 324818          STA     LDIR    ;SETUP LAST DIRECTION
018D 2A1618          LHLD    POSTN
0190 221A18          SHLD    LSTPOS  ;SETUP LAST POSTION
0193 2A0318          LHLD    ERRO
0196 CDC705          CALL    CLOSE   ;ERRO < 4
0199 DA6E00          JC      BOSS    ;IF CLOSE DON'T DO ANYTHING
019C 118EFF          LXI     D,-114  ;FIND STEP TO RAMP TO
019F 0612            MVI     B,18
01A1 3A4A18          LDA     GETIT           ;GET IT THERE SOMEHOW?
01A4 B7              ORA     A
01A5 CAAA01          JZ      DIV             ;IF NOT
01A8 0605            MVI     B,5
                DIV:
01AA 3EFF            MVI     A,-1 AND 255    ;A WILL CONTAIN STEP TO RAMP TO
                DIV1:
01AC 3C              INR     A
01AD 19              DAD     D
01AE DAAC01          JC      DIV1
01B1 B9              CMP     B
01B2 DAB701          JC      AOK
01B5 05              DCR     B
01B6 78              MOV     A,B     ;IF A>B THEN A=B-1
                AOK:
01B7 322718          STA     RMPTG   ;SAVE RESULT
01BA B7              ORA     A       ;IF A=0 DON'T RAMP
01BB CAC601          JZ      NORMP
01BE 3EFF            MVI     A,TRUE
01C0 324118          STA     ACCEL   ;SETUP FOR RAMP
01C3 324218          STA     RAMPUP
                NORMP:
01C6 2F              CMA
01C7 324518          STA     CONVRG
01CA CDF104          CALL    BRKON   ;ACTIVATE BRAKE & TRANSLATOR
01CD CDAB04          CALL    TRNON
01D0 AF              XRA     A
01D1 320B18          STA     DSCR+2  ;UPDATE IMAGE
01D4 D301            OUT     PIPTB   ;SET FOR 100HZ
01D6 3A4718          LDA     DIR
01D9 B7              ORA     A       ;WHICH DIRECTON
01DA 3A0A18          LDA     DSCR+1  ;GET IMAGE
01DD C2E501          JNZ     CCW
01E0 F609            ORI     09H     ;DRIVE CW
01E2 C3E701          JMP     MOVIT
                CCW:
01E5 F605            ORI     05H     ;DRIVE CCW
                MOVIT:
01E7 320A18          STA     DSCR+1  ;UPDATE IMAGE
01EA D300            OUT     PIPTA   ;SEND IT
01EC 216705          LXI     H,EDRV
01EF 222818          SHLD    TRAP    ;SETUP ERROR HANDLER
01F2 21983A          LXI     H,15000 ;15 SECS TO GET THERE
01F5 CD0005          CALL    TIMER
```

```
01F8 3EFF           MVI     A,TRUE
01FA 323D18         STA     DRVATV  ;SET DRIVE ACTIVE
01FD C36E00         JMP     BOSS

                    CLRREQ:
0200 AF             XRA     A
0201 323F18         STA     DRVREQ  ;CLEAR REQUEST
                    DRVTST:
0204 CDFE05         CALL    DSTOR   ;GET LATEST DATA
0207 DB2B           IN      APDCR
0209 E604           ANI     04H     ;CHECK FOR BRAKE DISENGAGED
020B CA4F05         JZ      EBRK    ;IF NOT, JUMP TO ERROR ROUTINE
020E 3A4118         LDA     ACCEL
0211 B7             ORA     A       ;CHECK FOR ACCELERATION
0212 CA2A02         JZ      PLOD    ;IF NOT, PLOD ALONG
0215 3A4218         LDA     RAMPUP
0218 B7             ORA     A       ;IN RAMP UP
0219 C23D02         JNZ     ZIPUP   ;IF YES, RAMP UP
021C 3A4318         LDA     MAIN
021F B7             ORA     A       ;IN MAIN DRIVE
0220 C24F02         JNZ     MAINCK  ;IF YES, CHECK WHEN TO RAMP DOWN
0223 3A4418         LDA     RAMPDN
0226 B7             ORA     A       ;RAMP DOWN?
0227 C26302         JNZ     ZIPDN   ;IF YES, DO IT
                    PLOD:
022A 3A4518         LDA     CONVRG
022D B7             ORA     A       ;CONVERGING?
022E C27602         JNZ     MOVIN   ;IF YES, CONVERGE
0231 CDE905         CALL    TSTOP   ;STOP TIMER
0234 CDA202         CALL    DRVSTP  ;STOP DRIVE
0237 CDCE04         CALL    TRNOF   ;TURN OFF TRANSLATOR
023A C36E00         JMP     BOSS    ;SEE WHAT'S NEXT

                    ZIPUP:
023D 3A2718         LDA     RMPTO   ;GET STEP TO RAMP TO
0240 4F             MOV     C,A
0241 CD4904         CALL    RMPUP   ;RAMP TO IT
0244 AF             XRA     A       ;RAMPUP TO MAIN
0245 324218         STA     RAMPUP
0248 2F             CMA
0249 324318         STA     MAIN
024C C36E00         JMP     BOSS

                    MAINCK:
024F 2A0318         LHLD    ERRO
0252 117602         LXI     D,0276H
0255 CDAF05         CALL    RANGER  ;AT THE RAMP DOWN POINT?
0258 79             MOV     A,C
0259 B7             ORA     A
025A CA6E00         JZ      BOSS
025D AF             XRA     A       ;IF YES, MAIN TO RAMPDN
025E 324318         STA     MAIN
0261 2F             CMA
0262 324418         STA     RAMPDN
0265 C36E00         JMP     BOSS

                    ZIPDN:
0268 CD7204         CALL    RMPDN   ;RAMP DOWN FROM CURRENT STEP
026B AF             XRA     A       ;SET RAMPDN TO CONVERGE
026C 324418         STA     RAMPDN
```

```
026F 2F             CMA
0270 324518         STA     CONVRG
0273 C36E00         JMP     BOSS

                    MOVIN:
0276 2A0318         LHLD    ERRO
0279 CDC905         CALL    CLOSE   ;WITHIN 4 COUNTS
027C D28602         JNC     MOV1
027F AF             XRA     A       ;IF YES, GO SHUTDOWN DRIVE
0280 324518         STA     CONVRG
0283 C36E00         JMP     BOSS
                    MOV1:
0286 3A4718         LDA     DIR     ;CURRENT DIRECTION
0289 4F             MOV     C,A
028A 3A4818         LDA     LDIR    ;LAST DIRECTION
028D B9             CMP     C       ;THE SAME?
028E CA6E00         JZ      BOSS
0291 79             MOV     A,C     ;IF NO, CHANGE DIRECTIONS
0292 324818         STA     LDIR    ;MAKE LAST DIR THE CURRENT DIR
0295 3A0A18         LDA     DSCR+1
0298 EE0C           XRI     0CH     ;FLIP DIRECTON BITS
029A 320A18         STA     DSCR+1
029D D360           OUT     P1PTA
029F C36E00         JMP     BOSS

                    DRVSTP:
02A2 CD7204         CALL    RAMDN   ;MAKE SURE RAMPED DOWN
02A5 AF             XRA     A       ;CLEAR DRIVE ACTIVE
02A6 323D18         STA     DRVATV
02A9 3A0A18         LDA     DSCR+1
02AC E6F2           ANI     0F2H    ;SHUT DOWN CLKS & DIRECTION
02AE 320A18         STA     DSCR+1
02B1 D300           OUT     P1PTA
02B3 C31405         JMP     BRKOF

                    ;***************************************
                    ; LOCAL DRIVE HANDLER

                    LOCAL:
02B6 CDAB04         CALL    TRNON   ;TRANSLATOR ON WHILE IN LOCAL
02B9 AF             XRA     A
02BA 320B18         STA     DSCR+2
02BD D301           OUT     P1PTB   ;SET FOR 100HZ
                    LCL1:
02BF CDFE05         CALL    DSTOR   ;GET DATA
02C2 3A0518         LDA     ERRO+2
02C5 E608           ANI     08H     ;APEX FAULT
02C7 C22501         JNZ     RSCMD   ;IF YES, RESET SYSTEM
02CA DB09           IN      P2PTB   ;GET DIRECTION
02CC E606           ANI     6
02CE FE04           CPI     4
02D0 CA2703         JZ      LCW     ;MOVE CW
02D3 FE02           CPI     2
02D5 CA4003         JZ      LCCW    ;MOVE CCW
02D8 DB09           IN      P2PTB   ;GET BAND SW
02DA E6F0           ANI     0F0H    ;STRIP EXTRANEOUS
02DC 47             MOV     B,A
02DD E610           ANI     10H     ;SWITCH HIT?
02DF CAED03         JZ      LCL4    ;IF NOT
02E2 2E01           MVI     L,1     ;ASSUME EXTEND
```

```
02E4 78             MOV     A,B
02E5 FE10           CPI     10H
02E7 CAF002         JZ      LCL2    ;IF EXTEND
02EA 2D             DCR     L       ;SET RETRACT
02EB FE30           CPI     30H
02ED C20003         JNZ     LCL4    ;IF SOME OTHER SWITCH
                LCL2:
02F0 CDF507         CALL    EXTR00
02F3 7D             MOV     A,L     ;GET FLAG
02F4 B7             ORA     A
02F5 3E80           MVI     A,80H   ;SET EXTEND LIGHT
02F7 0E0F           MVI     C,0FH   ;SET LIGHT BLINK
02F9 C2FF02         JNZ     LCL3    ;IF NOT EXTEND
02FC 3E40           MVI     A,40H   ;SET RETRACT LIGHT
02FE 0D             DCR     C       ;SET NEW LIGHT BLINK
02FF D319       LCL3:   OUT     RMPTA   ;LIGHT ON
0301 3A2418         LDA     RMPCS
0304 B1             ORA     C
0305 322418         STA     RMPCS
0308 D31B           OUT     RMPTC   ;START IT BLINKING
030A C36303         JMP     CHKRNG
                LCL4:
030D AF             XRA     A
030E D319           OUT     RMPTA   ;CLEAR LIGHT
0310 3A2418         LDA     RMPCS
0313 E630           ANI     30H     ;STRIP BLINK
0315 322418         STA     RMPCS
0318 D31B           OUT     RMPTC
031A DB08           IN      P2PTA
031C E601           ANI     01H     ;STILL IN LOCAL?
031E CABF02         JZ      LCL1
0321 CDCE04         CALL    TRNOF   ;IF NOT, TRANSLATOR OFF
0324 C32501         JMP     RSCHD   ;RESET SYSTEM

                LCW:
0327 CDF104         CALL    BRKON   ;DISENGAGE BRAKE
032A 3A0A18         LDA     DSCR+1
032D F609           ORI     9       ;SETUP CW DIR
032F 320A18         STA     DSCR+1
0332 D300           OUT     P1PTA
0334 DB09           IN      P2PTB
0336 E601           ANI     1       ;RAMP?
0338 CA4003         JZ      LCW1
033B 0E11           MVI     C,17    ;IF YES, RAMP TO 1000HZ
033D CD4904         CALL    RMPUP
                LCW1:
0340 CDFE05         CALL    DSTOR   ;GET DATA
0343 DB09           IN      P2PTB
0345 E602           ANI     2       ;STILL MOVING CW?
0347 CA4003         JZ      LCW1
034A C37003         JMP     LSTOP   ;IF NOT, SHUT DOWN

                LCCW:
034D CDF104         CALL    BRKON   ;DIENGAGE BRAKE
0350 3A0A18         LDA     DSCR+1
0353 F605           ORI     5       ;SETUP CCW DIR
0355 320A18         STA     DSCR+1
0358 D300           OUT     P1PTA
035A DB09           IN      P2PTB
035C E601           ANI     1       ;RAMP?
```

```
035E CA6603          JZ      LCCW1
0361 0E11            MVI     C,17    ;IF YES, RAMP TO 1000HZ
0363 CD4904          CALL    RMPUP
                     LCCW1:
0366 CDFE05          CALL    DSTOR   ;GET DATA
0369 DB09            IN      P2PTB
036B E604            ANI     4       ;STILL MOVING CCW
036D CA6603          JZ      LCCW1
                     LSTOP:          ;IF NOT, SHUT DOWN
0370 CD7204          CALL    RMPDN
0373 3A0A18          LDA     DSCR+1
0376 E6F2            ANI     0F2H    ;TURN OFF CLKS & DIR
0378 320A18          STA     DSCR+1
037B D308            OUT     P1PTA
037D CD1405          CALL    BRKOF   ;ENGAGE BRAKE
0380 C3BC02          JMP     LOCAL

                     ;**************************************
                     ; RING CHECK STATUS
                     ;

0383 3A4C18          CHKRNG: LDA     EXTFLG  ;IN RING EXTEND?
0386 B7                      ORA     A
0387 CA4104                  JZ      CHKRET
038A 3A0818                  LDA     ECHO+2  ;GET RING STATUS
038D E601                    ANI     1       ;THERE YET?
038F 114006          CHKRN1: LXI     D,1600  ;16 SEC WAIT
0392 CA9F03                  JZ      RNGWIT
0395 112C01                  LXI     D,300   ;3 SEC WAIT
0398 DB08                    IN      P2PTA
039A E601                    ANI     01H     ;STILL IN LOCAL?
039C CAAF03                  JZ      RNGWI2
039F 21AF03          RNGWIT: LXI     H,RNGWI2
03A2 220818                  SHLD    TRAP    ;SET TRAP POINT
03A5 EB                      XCHG
03A6 CDD005                  CALL    TIMER
03A9 CDFE05          RNGWI1: CALL    DSTOR
03AC C3A903                  JMP     RNGWI1  ;WAIT UNTIL TIMEOUT
03AF 3A0518          RNGWI2: LDA     ERRO+2  ;RESET TIMEOUT FAULT
03B2 E6EF                    ANI     0EFH
03B4 320518                  STA     ERRO+2
03B7 3A1418                  LDA     FAUL+2  ;*ADDED FOR MUX 236
03BA E6EF                    ANI     0EFH
03BC 321418                  STA     FAUL+2
03BF 3A4C18                  LDA     EXTFLG  ;GET EXTEND FLAG
03C2 B7                      ORA     A
03C3 3A0818                  LDA     ECHO+2
03C6 CAE303                  JZ      RNGWI3  ;IF NOT EXTEND
03C9 E603                    ANI     3
03CB FE03                    CPI     3
03CD CAFF03                  JZ      RNGWI4
03D0 E601                    ANI     1
03D2 CAFF03                  JZ      RNGWI4
03D5 320818                  STA     ECHO+2
03D8 3A1418                  LDA     FAUL+2  ;*ADDED FOR MUX 236
03DB E6DF                    ANI     0DFH
03DD 321418                  STA     FAUL+2
03E0 C31004                  JMP     CHKRN2
03E3 E603            RNGWI3: ANI     3
03E5 FE03                    CPI     3
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03E7 CAFF03           JZ      RNGWI4
03EA E602             ANI     2
03EC CAFF03           JZ      RNGWI4
03EF 3E02             MVI     A,2
03F1 320818           STA     ECHO+2
03F4 3A1418           LDA     FAUL+2  ;*ADDED FOR MUX 236
03F7 E60F             ANI     0DFH
03F9 321418           STA     FAUL+2
03FC C31004           JMP     CHKRN2
03FF F604     RNGWI4: ORI     4
0401 320818           STA     ECHO+2
0404 3A1418           LDA     FAUL+2  ;*ADDED FOR MUX 236
0407 F620             ORI     20H
0409 321418           STA     FAUL+2
040C AF               XRA     A
040D 324B18           STA     RNGCMD
0410 AF       CHKRN2: XRA     A
0411 324C18           STA     EXTFLG  ;CLEAR FLAGS
0414 3A0518           LDA     ERRO+2
0417 E67F             ANI     7FH
0419 320518           STA     ERRO+2  ;CLEAR ACTIVE
041C 3A0A18           LDA     DSCR+1
041F E6CF             ANI     0CFH
0421 320A18           STA     DSCR+1  ;TURN OFF
0424 D300             OUT     PIPTA
0426 3A4B18           LDA     RNGCMD  ;PENDING RING COMMMAND?
0429 B7               ORA     A
042A CA6E00           JZ      BOSS    ;IF NOT
042D 3A0518           LDA     ERRO+2
0430 F680             ORI     80H
0432 320518           STA     ERRO+2  ;RESTORE ACTIVE
0435 3A4B18           LDA     RNGCMD
0438 E601             ANI     1
043A F5               PUSH    PSW
043B C5               PUSH    B
043C D5               PUSH    D
043D E5               PUSH    H       ;SET STACK UP
043E C31100           JMP     EXTAT1
0441 3A0818   CHKRET: LDA     ECHO+2  ;GET RING STATUS
0444 E602             ANI     2       ;THERE YET?
0446 C33F03           JMP     CHKRN1


                      ;*************************************
                      ; RAMP UP & DOWN
                      ;ENTER WITH C=STEP TO STOP AT, 1=100HZ TO 17=1000HZ

                      RAMPUP:
0449 3A4918           LDA     RAMP
044C B7               ORA     A       ;RAMPED UP?
044D C8               RNZ             ;RETURN IF RAMPED UP
044E 2F               CMA
044F 324918           STA     RAMP    ;SET TRUE
0452 21A300           LXI     H,CK100 ;START OF RAMP TABLE
0455 AF               XRA     A       ;CLR RAMP STEP
                      RMUP1:
0456 325618           STA     STEP    ;SAVE LATEST STEP
0459 0619             MVI     B,25    ;WAIT 100 PULSES
045B 7E               MOV     A,M     ;STEP SPEED
045C 320B18           STA     DSCR+2
```

```
045F D301           OUT     PIPTB   ;EXECUTE IT
                RPUP2:
0461 CD9C04         CALL    WT65    ;WAIT FOR INTERUPT
0464 05             DCR     B
0465 C26104         JNZ     RPUP2
0468 23             INX     H       ;NEXT FREQUENCY
0469 3A2618         LDA     STEP
046C 3C             INR     A       ;NEXT STEP
046D B9             CMP     C       ;DONE THE NUMBER OF STEPS TO DO?
046E C25604         JNZ     RPUP1
0471 C9             RET             ;IF YES

                RMPDN:
0472 3A4918         LDA     RAMP
0475 B7             ORA     A       ;RAMPED DOWN?
0476 C8             RZ              ;RETURN IF RAMPED DOWN
0477 AF             XRA     A
0478 324918         STA     RAMP    ;SET RAMP FALSE
047B 11A308         LXI     D,CK100 ;POINT TO RAMP TABLE
047E 3A2618         LDA     STEP    ;GET STEP COUNT
0481 6F             MOV     L,A
0482 2600           MVI     H,0
0484 19             DAD     D       ;FORM POINTER
0485 3C             INR     A
0486 4F             MOV     C,A     ;NUMBER OF STEPS TO RAMP DOWN
                RPDN1:
0487 060C           MVI     B,12    ;WAIT 48 PULSES
0489 7E             MOV     A,M     ;GET FREQUENCY
048A 329B18         STA     DSCR+2
048D D301           OUT     PIPTB   ;START IT
                RPDN2:
048F CD9C04         CALL    WT65    ;WAIT FOR INERUPT
0492 05             DCR     B
0493 C28F04         JNZ     RPDN2
0496 2B             DCX     H       ;NEXT FREQUENCY
0497 0D             DCR     C       ;DONE STEPPING?
0498 C28704         JNZ     RPDN1
049B C9             RET             ;IF YES

                WT65:
049C CDFE05         CALL    DSTOR   ;GET DATA
049F 3A4618         LDA     DRVPLS
04A2 B7             ORA     A       ;INTERUPT?
04A3 CA9C04         JZ      WT65
04A6 AF             XRA     A       ;IF YES, CLR FLAG & RETURN
04A7 324618         STA     DRVPLS
04AA C9             RET

                ;****************************************
                ; TRANSLATOR & BRAKE CONTROL

                TRNON:
04AB 213705         LXI     H,ETRN  ;TRANSLATOR ERROR HANDLING
04AE 222818         SHLD    TRAP
04B1 216400         LXI     H,100   ;ONE SEC
04B4 CDC005         CALL    TIMER   ;START TIMER
04B7 3A0A18         LDA     DSCR+1
04BA F680           ORI     80H     ;SET TRANS ON BIT
04BC 320A18         STA     DSCR+1  ;UPDATE IMAGE
04BF D300           OUT     PIPTA   ;DO IT
```

```
                TRON:
04C1 CDFE05             CALL    DSTOR
04C4 DB08               IN      P2PTA
04C6 E610               ANI     10H     ;IS IT ON YET
04C8 CAC104             JZ      TRON
04CB C3E905             JMP     TSTOP   ;IF YES, STOP TIMER & RETURN

                TRNOF:
04CE 213705             LXI     H,ETRN
04D1 222818             SHLD    TRAP
04D4 216400             LXI     H,100   ;ONE SEC
04D7 CDD005             CALL    TIMER
04DA 3A0A18             LDA     DSCR+1
04DD E67F               ANI     7FH     ;RESET TRANS POWER BIT
04DF 320A18             STA     DSCR+1
04E2 D300               OUT     P1PTA   ;TURN OFF
                TROFF:
04E4 CDFE05             CALL    DSTOR
04E7 DB08               IN      P2PTA
04E9 E610               ANI     10H     ;IS IT OFF YET
04EB C2E404             JNZ     TROFF
04EE C3E905             JMP     TSTOP   ;IF YES, STOP TIMER & RETURN

                BRKON:
04F1 214F05             LXI     H,EBRK  ;BRAKE ERROR HANDLING ADDR
04F4 222818             SHLD    TRAP
04F7 216400             LXI     H,100   ;ONE SEC
04FA CDD005             CALL    TIMER
04FD 3A0A18             LDA     DSCR+1
0500 F640               ORI     40H     ;SET BRAKE DISENGAGE BIT
0502 320A18             STA     DSCR+1
0505 D300               OUT     P1PTA   ;DISENGAGE
                BRKO1:
0507 CDFE05             CALL    DSTOR
050A DB2B               IN      APDCR
050C E604               ANI     4       ;READY YET
050E CA0705             JZ      BRKO1
0511 C3E905             JMP     TSTOP   ;YES, STOP TIMER & RET

                BRKOF:
0514 214F05             LXI     H,EBRK  ;ERROR ADDR
0517 222818             SHLD    TRAP
051A 216400             LXI     H,100   ;ONE SEC
051D CDD005             CALL    TIMER
0520 3A0A18             LDA     DSCR+1
0523 E66F               ANI     0BFH    ;RESET BIT
0525 320A18             STA     DSCR+1
0528 D300               OUT     P1PTA   ;ENGAGE BRAKE
                BRKF1:
052A CDFE05             CALL    DSTOR
052D DB2B               IN      APDCR
052F E604               ANI     4       ;ENGAGED YET
0531 C22A05             JNZ     BRKF1
0534 C3E905             JMP     TSTOP

                ;***************************************
                ; ERROR HANDLING ROUTINES

                ETRN:                   ;TRANSLATOR
0537 3A0A18             LDA     DSCR+1
```

```
053A E67F            ANI     7FH     ;RESET POWER BIT
053C 320A18          STA     DSCR+1
053F D300            OUT     PIPTA   ;TURN OFF
0541 3A0218          LDA     POSD+2
0544 F610            ORI     10H     ;SET FAULT BIT
0546 320218          STA     POSD+2
0549 321218          STA     FAUL    ;*ADDED FOR HUX 236
054C C32501          JMP     RSCMD   ;RESET SYSTEM

                     EBRK:           ;BRAKE
054F 3A0A18          LDA     DSCR+1
0552 E6BF            ANI     0BFH    ;RESET BIT
0554 320A18          STA     DSCR+1
0557 D300            OUT     PIPTA   ;ENGAGE BRAKE
0559 3A0218          LDA     POSD+2
055C F604            ORI     04H     ;SET FAULT BIT
055E 320218          STA     POSD+2
0561 321218          STA     FAUL    ;*ADDED FOR HUX 236
0564 C32501          JMP     RSCMD   ;RESET SYSTEM

                     EDRV:           ;DRIVE
0567 310019          LXI     SP,1900H        ;RESET STACK
056A 3A1418          LDA     FAUL+2  ;*ADDED FOR HUX 236
056D F601            ORI     1H      ;SET DRIVE FAULT BIT
056F 321418          STA     FAUL+2
0572 3A2018          LDA     STEP
0575 FE04            CPI     4       ;CHECK RAMP STEP
0577 DA8905          JC      EDRV1   ;STEP < 300HZ, SYSTEM RESET
057A 3EFF            MVI     A,TRUE  ;OTHERWISE TRY RAMPING TO 250HZ
057C 324A18          STA     GETIT   ;SET GET IT THERE SOMEHOW
057F CDE905          CALL    TSTOP   ;STOP TIMER AND DRIVE
0582 CDA202          CALL    LRVSTP
0585 AF              XRA     A       ;CLEAR ACC FOR ENTRY
0586 C36701          JMP     DRVINI  ;INTO DRVINT
                     EDRV1:
0589 3A0218          LDA     POSD+2  ;SET DRIVE FAULT
058C F620            ORI     20H
058E 320218          STA     POSD+2
0591 321218          STA     FAUL    ;*ADDED FOR HUX 236
0594 C32501          JMP     RSCMD

                     ;************************************
                     ; SUBROUTINES

                     VECTOR:         ;HL=DESTINATION
0597 CDAF05          CALL    RANGER  ;DE=POSITION
059A C8              RZ              ;IF HL=0
059B 1100E0          LXI     D,-2000H
059E 19              DAD     D
059F D2A805          JNC     VEC1
05A2 79              MOV     A,C
05A3 2F              CMA             ;CHANGE DIRECTION
05A4 4F              MOV     C,A
05A5 CDC105          CALL    CMPHL
                     VEC1:
05A8 112020          LXI     D,2000H
05AB 19              DAD     D
05AC 7D              MOV     A,L     ;HL=MINIMUM MAGNITUDE
05AD B4              ORA     H       ;C=DIRECTION, 0 IS POSITIVE
05AE C9              RET             ;ZERO FLAG SET FOR HL=0
```

```
                RANGER:                 ;HL=|HL-DE|
05AF 7D                 MOV     A,L
05B0 93                 SUB     E
05B1 6F                 MOV     L,A
05B2 7C                 MOV     A,H
05B3 9A                 SBB     D
05B4 67                 MOV     H,A
05B5 0E00               MVI     C,0     ;C => +
05B7 F2BE05             JP      RNGR1
05BA 0D                 DCR     C
05BB CDC105             CALL    CMPHL
                RNGR1:
05BE 7D                 MOV     A,L
05BF B4                 ORA     H       ;ZERO FLAG SET IF HL=0
05C0 C9                 RET             ;C=0 => +DIR

                CMPHL:                  ;TWO'S COMPLIMENT HL
05C1 7C                 MOV     A,H
05C2 2F                 CMA
05C3 67                 MOV     H,A
05C4 7D                 MOV     A,L
05C5 2F                 CMA
05C6 6F                 MOV     L,A
05C7 23                 INX     H
05C8 C9                 RET

                CLOSE:                  ;HL < 4
05C9 7C                 MOV     A,H
05CA B7                 ORA     A
05CB C0                 RNZ
05CC 7D                 MOV     A,L
05CD FE03               CPI     3
05CF C9                 RET             ;CARRY SET IF LESS THAN 4

                TIMER:
05D0 3ECF               MVI     A,0CFH  ;ENABLE TIMER AFTER COUNT LOADED
05D2 D318               OUT     RCMD
05D4 7D                 MOV     A,L     ;HL CONTAIN TIMER PERIOD
05D5 D31C               OUT     TIMLO
05D7 7C                 MOV     A,H
05D8 E63F               ANI     3FH
05DA F640               ORI     40H     ;STOP ON TERMINAL COUNT
05DC D31D               OUT     TIMHI
05DE 3A2418             LDA     RMPCS
05E1 F610               ORI     10H     ;SET FOR 100HZ CLK
05E3 322418             STA     RMPCS
05E6 D31B               OUT     RMPTC   ;START IT
05E8 C9                 RET

                TSTOP:
05E9 3A2418             LDA     RMPCS
05EC E6CF               ANI     0CFH    ;TURN CLK OFF
05EE 322418             STA     RMPCS
05F1 D31B               OUT     RMPTC
05F3 3E4F               MVI     A,4FH   ;STOP COUNTER
05F5 D318               OUT     RCMD
05F7 210000             LXI     H,INIT
05FA 222818             SHLD    TRAP    ;SHOULD TRAP HAPPEN
05FD C9                 RET
```

```
                ;****************************************
                ; APEX & CONTROLLER DATA GATHERING & FORMATTING

                DSTOR:
05FE F5                 PUSH    PSW     ;SAVE REGISTERS
05FF C5                 PUSH    B
0600 D5                 PUSH    D
0601 E5                 PUSH    H
0602 AF                 XRA     A
0603 D358               OUT     AIPT    ;REQUEST APEX DATA & CLEAR SHIFT REGISTERS
0605 060A               MVI     B,10    ;DATA SHOULD SHOW UP IN TEN LOOPS
                LP1:
0607 DB29               IN      POSH
0609 E6C0               ANI     0C0H    ;MASK
060B FE80               CPI     80H     ;LOOK FOR THIS PATTERN
060D CA2906             JZ      LP2
0610 05                 DCR     B
0611 C20706             JNZ     LP1
0614 3A0518             LDA     ERRO+2
0617 F608               ORI     08H     ;SET APEX FAULT BIT
0619 320518             STA     ERRO+2
061C E61E               ANI     1EH     ;*ADDED FOR MUX 236
061E 47                 MOV     B,A
061F 3A1418             LDA     FAUL+2
0622 B0                 ORA     B
0623 321418             STA     FAUL+2
0626 C30406             JMP     LP3     ;SKIP APEX DATA GATHERING
                LP2:
0629 3A0518             LDA     ERRO+2
062C E6F7               ANI     0F7H    ;RESET FAULT BIT
062E 320518             STA     ERRO+2
0631 3A1418             LDA     FAUL+2  ;*ADDED FOR MUX 236
0634 E6F7               ANI     0F7H
0636 321418             STA     FAUL+2

0639 DB28               IN      POSL    ;POSITION LOW BYTE
063B 6F                 MOV     L,A
063C 5F                 MOV     E,A
063D DB29               IN      POSH    ;POSITION HIGH BYTE
063F E63F               ANI     3FH     ;MASK FOR 14 BIT
0641 67                 MOV     H,A
0642 57                 MOV     D,A
0643 221818             SHLD    POSTN   ;STORE UNSIGNED POSITION
0646 EE20               XRI     20H     ;FLIP SIGN BIT
0648 67                 MOV     H,A
0649 220818             SHLD    POSD    ;STORE SIGNED POSTION
064C 2A1E18             LHLD    ATVCMD  ;GET ACTIVE COMMAND
064F CD9705             CALL    VECTOR  ;DISTANCE FROM CURRENT TO NEW POSITION
0652 221318             SHLD    ERRO    ;SHOW DISTANCE
0655 79                 MOV     A,C
0656 324718             STA     DIR     ;STORE NEW DIRECTION

0659 DB24               IN      VEL     ;GET VELOCITY DATA
065B EE80               XRI     80H     ;FLIP SIGN BIT
065D 6F                 MOV     L,A     ;MOVE INTO HL
065E 2600               MVI     H,0
0660 29                 DAD     H       ;SHIFT 4* TO FORM 12 BIT ANALOG
0661 29                 DAD     H
0662 29                 DAD     H
```

```
0663 29             DAD   H
0664 220C18         SHLD  ADCR    ;SHOW RESULT
0667 DB2B           IN    APDCR   ;GET APEX DISCRETES
0669 E697           ANI   97H     ;MASK UNUSED BITS
066B 32ØE18         STA   ADCR+2  ;SHOW THEM
066E E603           ANI   03H     ;MASK LIMITS
0670 47             MOV   B,A
0671 3A3218         LDA   POSD+2  ;GET IMAGE
0674 E6FC           ANI   0FCH    ;RESET LIMITS
0676 B0             ORA   B       ;FORM NEW IMAGE
0677 323218         STA   POSD+2  ;SHOW IT
067A DB2B           IN    APDCR
067C E604           ANI   04H     ;BRAKE I*E
067E 0F             RRC           ;SHIFT FOR DISPLAY
067F 47             MOV   B,A
0680 3A2318         LDA   RMPBS   ;GET IMAGE
0683 E6F1           ANI   0F1H    ;RESET BIT
0685 B0             ORA   B       ;FORM NEW IMAGE
0686 47             MOV   B,A

0687 DB2D           IN    ANAH    ;GET RING INFO
0689 EEC0           XRI   0C0H    ;FLIP BITS
068B E6C0           ANI   0C0H    ;STRIP
063D 07             RLC
068E 07             RLC
068F 4F             MOV   C,A
0690 3A0818         LDA   ECHO+2
0693 E604           ANI   4
0695 B1             ORA   C       ;MERGE POS AND FAULT
0696 320818         STA   ECHO+2
0699 79             MOV   A,C
069A 07             RLC
069B 07             RLC
069C B0             ORA   B
069D 322318         STA   RMPBS
06A0 D31A           OUT   RMPTB   ;DISPLAY ON M8
06A2 DB2C           IN    ANAL    ;APEX ANALOG LOW BYTE
06A4 6F             MOV   L,A
06A5 DB2D           IN    ANAH    ;APEX ANALOG HIGH BYTE
06A7 EE02           XRI   2       ;FLIP SIGN BIT
06A9 47             MOV   B,A     ;SAVE RESULT IN B
06AA E61E           ANI   1EH     ;MASK MUX & SIGN BIT
06AC 87             ADD   A       ;SHIFT LEFT ONCE
06AD 67             MOV   H,A     ;SAVE IN H
06AE 78             MOV   A,B     ;GET B BACK
06AF E603           ANI   3       ;MASK OUT MUX
06B1 B4             ORA   H       ;FORM NEW HIGH BYTE WITH EXTENDED SIGN
06B2 67             MOV   H,A     ;PUT IT IN H
06B3 29             DAD   H       ;SHIFT ONCE MORE TO FORM 12 BIT ANALOG
06B4 EB             XCHG          ;SAVE IN DE
06B5 E638           ANI   38H     ;MASK THE MUX
06B7 0F             RRC           ; / 4
06B8 0F             RRC
06B9 6F             MOV   L,A     ;SETUP HL
06BA 2600           MVI   H,0
06BC 012C18         LXI   B,APATAB;GET APEX ANALOG TABLE ADDR
06BF 09             DAD   B       ;FORM INDEX
06C0 73             MOV   M,E     ;SAVE APEX ANALOG IN IT
06C1 23             INX   H
06C2 72             MOV   M,D
```

```
06C3 3A2A18          LDA     ANAMX   ;GET MUX COUNTER
06C6 E607            ANI     07H     ; MOD 8
06C8 07              RLC             ; * 2
06C9 6F              MOV     L,A     ;SETUP HL
06CA 2600            MVI     H,0
06CC 09              DAD     B       ;FORM INDEX
06CD 7E              MOV     A,M     ;GET VALUE INTO HL
06CE 23              INX     H
06CF 66              MOV     H,M
06D0 6F              MOV     L,A
06D1 220F18          SHLD    ANAD    ;STORE IT FOR DATA SET
                LP3:
06D4 3A3D18          LDA     DRVATV
06D7 B7              ORA     A       ;IS DRIVE ACTIVE
06D8 3A2318          LDA     RMPBS   ;GET M8 DISPLAY IMAGE
06DB CAE506          JZ      LP4
06DE F601            ORI     01H     ;IF YES,SET BITS
06E0 0E40            MVI     C,40H
06E2 C3E906          JMP     LP5
                LP4:
06E5 E6FE            ANI     0FEH    ;IF NOT, RESET BITS
06E7 0E00            MVI     C,0
                LP5:
06E9 322318          STA     RMPBS   ;SAVE IMAGE
06EC D31A            OUT     RMPTB   ;DISPLAY ON M8
06EE D508            IN      P2PTA   ;GET PEDESTAL ROOM DISCRETES
06F0 320918          STA     DSCR    ;SHOW'EM
06F3 E607            ANI     07H     ;MASK COMP,YOMP, & CABLE INTERLINK
06F5 EE07            XRI     07H     ;FLIP THE BITS
06F7 47              MOV     B,A     ;SAVE IN B
06F8 3A0518          LDA     ERRO+2  ;GET IMAGE
06FB E688            ANI     088H    ;RESET THESE BITS
06FD B0              ORA     B       ;BRING IN THESE BITS
06FE B1              ORA     C       ;BRING IN DRIVE ACTIVE
06FF 320518          STA     ERRO+2  ;SHOW RESULT
0702 E61E            ANI     1EH     ;*ADDED FOR MUX 236
0704 47              MOV     B,A
0705 3A1418          LDA     FAUL+2
0708 E6E9            ANI     0E9H    ;STRIP OLD INFO
070A B0              ORA     B       ;UPDATE INFO
070B 321418          STA     FAUL+2
070E E1              POP     H       ;BRING BACK REGISTERS
070F D1              POP     D
0710 C1              POP     B
0711 F1              POP     PSW
0712 C9              RET

                ;****************************************
                ; INTERUPT ROUTINES

                BLAP:                   ;TRAP INTERUPT
0713 310019          LXI     SP,1900H;RESET STACK
0716 2A2618          LHLD    TRAP    ;GET ERROR HANDLING ADDR
0719 E5              PUSH    H       ;ON STACK FOR RET
071A CDE905          CALL    TSTOP   ;STOP TIMER
071D 3A0518          LDA     ERRO+2
0720 F610            ORI     10H     ;SET TIME-OUT FAULT BIT
0722 320518          STA     ERRO+2  ;SHOW IT
0725 3A1418          LDA     FAUL+2  ;*ADDED FOR MUX 236
0728 E610            ANI     10H
```

```
072A 321418          STA     FAUL+2
072D D33B            OUT     RES65   ;RESET 6.5
072F 3E19            MVI     A,RSTEN ;RESET 7.5. DISABLE 5.5
0731 30              DB      30H     ;SIM, SETUP INTERUPTS
0732 FB              EI
0733 C9              RET             ;GOTO ERROR HANDLER

                TRPR:                ;6.5 INTERUPT
0734 D33B            OUT     RES65   ;RESET 6.5
0736 FB              EI              ;ENABLE INTERUPTS FOR INTR 7.5
0737 F5              PUSH    PSW     ;SAVE REGISTERS
0738 C5              PUSH    B
0739 D5              PUSH    D
073A E5              PUSH    H
073B 3EFF            MVI     A,TRUE
073D 324618          STA     DRVPLS  ;SHOW INTERUPT OCCURED
0740 DB08            IN      P2PTA
0742 E601            ANI     01H
0744 CA7F07          JZ      TRPR1   ;SKIP IF IN LOCAL
0747 3A0A18          LDA     DSCR+1
074A E60C            ANI     0CH     ;LOOK AT DIRECTION BITS
074C CA7F07          JZ      TRPR1   ;SKIP IF NO DIRECTION
074F 342518          LDA     MOTION  ;GET MOTION COUNTER
0752 3C              INR     A
0753 FE19            CPI     25      ;IS IT 25
0755 C25907          JNZ     TRPR2   ;IF NOT, SKIP MOTION ANALYSIS
0758 2A1A18          LHLD    LSTPOS  ;GET LAST POSITION
075B EB              XCHG
075C 2A1818          LHLD    POSTN   ;GET CURRENT POSITION
075F 221A18          SHLD    LSTPOS  ;UPDATE LAST POSITION
0762 3A4A18          LDA     GETIT   ;IN GET IT THERE?
0765 B7              ORA     A
0766 C27107          JNZ     TRPR0   ;IF IN GETIT
0769 3A2618          LDA     STEP    ;INITIAL STEP?
076C FE02            CPI     2
076E DA7F07          JC      TRPR1   ;IF BELOW STEP 2
                TRPR0:
0771 CD9705          CALL    VECTOR  ;GET THE DELTA
0774 7C              MOV     A,H
0775 B7              ORA     A       ;IS IT 0
0776 C26705          JNZ     EDRV    ;IF NOT, ERROR IN DRIVE
0779 7D              MOV     A,L
077A FE3C            CPI     60      ;LESS THAN 60
077C DA6705          JC      EDRV    ;IF YES, ERROR IN DRIVE
                TRPR1:
077F AF              XRA     A
                TRPR2:
0780 322518          STA     MOTION  ;UPDATE MOTION COUNTER
0783 E1              POP     H       ;RESTORE REGISTERS
0784 D1              POP     D
0785 C1              POP     B
0786 F1              POP     PSW
0787 C9              RET

                BUFF:                ;7.5 INERUPT
0788 F5              PUSH    PSW     ;SAVE REGISTERS
0789 C5              PUSH    B
078A D5              PUSH    D
078B E5              PUSH    H
078C DB35            IN      SHAEV   ;READ SHA-EVENT REG
```

```
078E 47             MOV     B,A     ;SAVE IN B
078F E607           ANI     07H     ;MASK SHA
0791 4F             MOV     C,A     ;SAVE IN C
0792 78             MOV     A,B     ;GET B BACK
0793 E638           ANI     38H     ;MASK TYPE OF REQUEST
0795 FE28           CPI     28H
0797 CAAD07         JZ      CMDRQ   ;A COMMAND REQUEST
079A FE18           CPI     18H
079C CA6308         JZ      DTARQ   ;A DATA REQUEST
079F 3A0218         LDA     POSD+2
07A2 F640           ORI     40H     ;SET CONTROLLER FAULT
07A4 320218         STA     POSD+2
07A7 321218         STA     FAUL    ;*ADDED FOR MUX 236
07AA C37D08         JMP     SKIP    ;ERROR
                CMDRQ:
07AD DB30           IN      DSCDL   ;COMMAND LOW BYTE
07AF 6F             MOV     L,A
07B0 DB31           IN      DSCDH   ;COMMAND HIGH BYTE
07B2 67             MOV     H,A
07B3 E63F           ANI     3FH     ;MASK FOR 14 BIT
07B5 EE20           XRI     20H     ;FLIP SIGN BIT
07B7 57             MOV     D,A     ;DE CONTAIN UNSIGNED COMMAND
07B8 5D             MOV     E,L
07B9 06FF           MVI     B,TRUE
07BB 79             MOV     A,C     ;GET MUX
07BC B7             ORA     A
07BD CAD907         JZ      DRVCMD  ;NEW POSITION COMMAND
07C0 FE01           CPI     1
07C2 CAE707         JZ      CMDRST  ;SYSTEM RESET
07C5 FE02           CPI     2
07C7 CAEE07         JZ      MAPSET  ;MAP REQUEST
07CA FE06           CPI     6
07CC CAF907         JZ      EXTRTC  ;RING EXTEND/RETRACT
07CF 221518         SHLD    MU2     ;STORE UNUSED COMMAND IN BIT BUCKET
07D2 79             MOV     A,C
07D3 321718         STA     MU2+2
07D6 C37D08         JMP     SKIP    ;AND LEAVE
                DRVCMD:
07D9 220618         SHLD    ECHO    ;SHOW RECEIVED COMMAND
07DC EB             XCHG
07DD 221C18         SHLD    CMDTMP  ;UPDATE TEMPARARY COMMAND
07E0 78             MOV     A,B
07E1 323F18         STA     DRVREQ  ;POSITION REQUEST ACTIVE
07E4 C37D08         JMP     SKIP
                CMDRST:
07E7 78             MOV     A,B
07E8 323C18         STA     RESCMD  ;RESET SYSTEM REQUEST
07EB C37D08         JMP     SKIP
                MAPSET:
07EE 78             MOV     A,B
07EF 324018         STA     MAPREQ  ;MAP REQUEST
07F2 C37D08         JMP     SKIP
                EXTR00:
07F5 F5             PUSH    PSW
07F6 C5             PUSH    B
07F7 D5             PUSH    D
07F8 E5             PUSH    H
                EXTRTC:
07F9 3A4018         LDA     MAPREQ  ;MAP MODE?
07FC B7             ORA     A
```

```
07FD C27D08          JNZ     SKIP    ;IF IN MAPTIME
0800 3A0518          LDA     ERRD+2  ;RING COMMAND ACTIVE?
0803 47              MOV     B,A     ;SAVE IN B
0804 E680            ANI     80H
0806 C24F08          JNZ     EXTRT2  ;IF ACTIVE
0809 78              MOV     A,B     ;RESTORE A
080A F680            ORI     80H     ;SET RING ACTIVE
080C 320518          STA     ERRD+2
080F 7D              MOV     A,L     ;GET LSB
0810 B7              ORA     A       ;EXTEND?
0811 CA3208  EXTRT1: JZ      RETRCT  ;IF NOT RETRACT
0814 3A0818          LDA     ECHO+2  ;GET POSITION
0817 E601            ANI     1       ;THERE?
0819 3EFF            MVI     A,0FFH  ;SET EXTEND FLAG
081B 324C18          STA     EXTFLG
081E C27D08          JNZ     SKIP
0821 3A0A18          LDA     DSCR+1  ;GET DISCRETES
0824 F610            ORI     10H
0826 320A18          STA     DSCR+1  ;UPDATE DISCRETES
0829 D300            OUT     PIPTA   ;START MOTOR AGAIN
082B AF              XRA     A       ;CLEAR SECOND COMMAND FLAG
082C 324518          STA     RNGCMD
082F C37D08          JMP     SKIP
0832 3A0818  RETRCT: LDA     ECHO+2  ;GET POSITION
0835 E602            ANI     2
0837 3E00            MVI     A,0     ;SET RETRACT FLAG
0839 324C18          STA     EXTFLG
083C C27D08          JNZ     SKIP
083F 324B18          STA     RNGCMD  ;CLEAR SECOND COMMAND FLAG
0842 3A0A18          LDA     DSCR+1  ;GET DISCRETES
0845 F620            ORI     20H
0847 320A18          STA     DSCR+1  ;UPDATE DISCRETES
084A D300            OUT     PIPTA   ;START MOTOR AGAIN
084C C37D08          JMP     SKIP
084F 3A4C18  EXTRT2: LDA     EXTFLG
0852 E601            ANI     1
0854 BD              CMP     L
0855 CA7D08          JZ      SKIP
0858 7D              MOV     A,L     ;GET LSB
0859 F602            ORI     2       ;SET FLAG
085B E603            ANI     3
085D 324B18          STA     RNGCMD  ;SET SECOND COMMAND FLAG
0860 C37D08          JMP     SKIP

                     DTARQ:
0863 79              MOV     A,C     ;GET MUX ADDR
0864 FE05            CPI     5
0866 C26908          JNZ     DRQ1    ;IF NOT, SKIP THE FOLLOWING
0869 211A18          LXI     H,ANAMX ;POINT TO MUX COUNTER
086C 34              INR     M       ;INCREMENT COUNTER
                     DRQ1:
086D 07              RLC             ;SETUP FOR INDEXING. 3 * A
086E 81              ADD     C
086F 6F              MOV     L,A     ;HL POINTS TO VALUE
0870 2618            MVI     H,18H
0872 7E              MOV     A,M     ;GET UP THE THREE BYTES FOR OUTPUT
0873 D332            OUT     DSDT1
0875 23              INX     H
0876 7E              MOV     A,M
0877 D333            OUT     DSDT2
```

```
0879 23             INX     H
087A 7E             MOV     A,M
087B D334           OUT     DSDT3
                SKIP:
087D E1             POP     H       ;RESTORE REGISTERS
087E D1             POP     D
087F C1             POP     B
0880 F1             POP     PSW
0881 FB             EI
0882 C9             RET

                ;**************************************

                ;ANALOG TABLE   LO    HI
                ; -5.12 <= V <= 5.11, 400H => 8FEH
                ; 2048 + TRUNC( V * 200 )
                ANATAB:
0883 EA87FE08           DW      07EAH,08FEH     ;MOUNT TEMP. 30 => 124 F
0887 FC0342005          DW      04FCH,0528H     ;-15/4
088B D30A040B           DW      0AD8H,0504H     ;+15/4
088F B600BFE0B          DW      0B56H,08FEH     ;+ 5
0893 E400BEC0B          DW      08E4H,08ECH     ;+10/2
0897 0000FF0F           DW      0000H,0FFFH     ;FOC VEL
089B 0000FF0F           DW      0000H,0FFFH     ;ROT VEL
089F FC070400           DW      07FCH,0004H     ;GND

                ;RAMP TABLE

08A3 00         CK100:  DB      00H     ;100HZ
08A4 34         CK150:  DB      34H     ;150
08A5 50                 DB      50H     ;200
08A6 60                 DB      60H     ;250
08A7 67                 DB      67H     ;300
08A8 71                 DB      71H     ;350
08A9 75                 DB      75H     ;400
08AA 78                 DB      78H     ;450
08AB 80                 DB      80H     ;500
08AC 80                 DB      80H     ;500
08AD 83                 DB      83H     ;600
08AE 85                 DB      85H     ;650
08AF 86                 DB      86H     ;700
08B0 87                 DB      87H     ;750
08B1 88                 DB      88H     ;850
08B2 89                 DB      89H     ;900
08B3 90         CK1000: DB      90H     ;1000HZ

                ;**************************************

08B4                    END     0
```

LIST OF RELATED DRAWINGS

M7, Model E F/R Controller

A13740Z08	Top Bill of Materiels
D13740P16	Top Assembly Drawing
D13740S07	Logic Schematic
A13740W06	Master Wire List
A13740W07	Hand Wire List
A13740W08	Machine Wire List
A13740W09	Connector Wire List
A13740P12	IC Module Ass'y (IC location matrix)
C13740M07	Front Panel
C13740AA09	Front Panel Silk Screen Artwork
C13740M21	Rear Panel
C13720M53	16 Pin Logic Connector Board
C13720M54	Universal Logic Connector Board
B13050M03	Support Bar, Top & Bottom
B13720M15-1,-2	Rail Modification, Top & Bottom
C13720M17	Insulated Spacer
B13720M49	Side Panel Insulation
C13720M50	Modified Side Panel
C13050M22-1	Perforated Cover
B13050M04	Guide Block

M08 Model C, F/R Power Supply

A13740Z11	Top Bill of Materiels
D13740P18	Top Assembly Drawing
A13740W11	Wire List
D13740S11	Schematic Diagram
C13740M35	Front Panel
C13740M36	Rear Panel
C13740M37	Mounting Bars, Top & Bottom
B13740P19	Front Panel PCB Assembly Dwg
A13740Z12	Front Panel PCB Bill of Materiels
B13740AB02	Front Panel Display PCB Artwork
C13740M26	Front Panel PCB Drill Dwg
B13740M38	PS2 Mounting Bracket, Version 1
B13740M39	PS2 Mounting Bracket, Version 2, for LND-Z-152
C13740AA02	Front Panel Silkscreen Artwork
C13740AA03	Rear Panel Silkscreen Artwork
B13050M04	Guide Block

M11 Model B, Apex Interface Unit

A13740Z09	Top Bill Of Materiels
D13740P15	Top Assembly Drawing
A13740W02	Master Wire List
A13740W03	Hand Wire List
A13740W04	Machine Wire List
A13740W05	Connector Wire List
D13740S08	Logic Schematic
C13740M23	Logic Connector Board Modification
C13720M53	Logic Connector Board

A13740P11	IC Module Ass'y (IC Location Matrix)
C13740P13	Front Panel PCB Assembly
A13740Z06	Front Panel PCB Bill of Materiels
B13740AB01	Front Panel Display PCB Artwork
A13740M24	Front Panel PCB Drill Drawing
D13740M06	Front Panel
C13740AA07	Front Panel Silk Screen Artwork
C13740M40	Rear Panel
C13740P17	S/D Converter PCB Assembly
C13740AB04	S/D Converter Artwork
C13740M31	S/D Converter Drill Drawing
C13740M17	Insulated Spacer
C13050M03	Support Bar, Top & Bottom
B13720M15-1,2	Rail Modification, Top & Bottom
C13050M22-1	Perforated Cover
C13720M50	Side Cover
C13720M49	Side Cover Insulation
B13722M05	Display Filter & Polarized Screen
A13740AD03	Front Panel Display Legend
B13050M04	Guide Block

M22 Model B, F/R Switching Module

A13740Z13	Top Bill Of Materiels
D13740P20	Top Assembly Drawing
C13740S10	F/R Switching Module Schematic Diagram
A13740W12	F/R Switching Wire List
C13740M41	Support Bar, Top & Bottom
C13740M32	Front Panel
C13740AA04	Front Panel Silkscreen Artwork
C13740M29	Rear Panel
C13740M33	Synchro Excitor Chassis
C13740M34	Brake Controller Mounting Bracket
D13740AB06	Synchro Excitor PCB Artwork
D13740M43	Synchro Excitor PCB Drill Drill Drawing
D13740P21	Synchro Excitor PCB Assembly Drawing

Bin Assembly

A13740W10	F/R System E, Bin Assembly & Wire List
A13740Z15	F/R System E, Bin Assembly Top Bill of Materiels
D13050M08	Bin Assembly
B13050M59	42/34 Bin Rear Panel
B13050M26	42 (single conn only) Bin Rear Panel
C13740M04	Fan Mounting Bracket
D13740D01	F/R Bin Wiring Geometry
C13740M16	Bin W I/O Panel Mtg Brkt, Left
C13740M15	Bin W I/O Panel Mtg Brkt, Right
C13740M17	Bin W Rear Protective Shield
C13740M14	Bin W Top Protective Shield
C13740M11	Bin W I/O Panel
B13740M28	Cable Clamp, Cmd/Data I/O Conn
C13050M54	Bin Rear Filler Panel
B13050M47	Bin Front Filler Panel, 2 - 4 Wide
B13740M1Z	Connector Lock Plate

F/R System Cabling

B13740W10	F/R System Model E, Cabling Structure
B13740P22	F/R Mount Temp Probe Assembly
B13740P42	F/R Mount Temp Probe Base Plate
D13740S16	Wiring Diagram Prime Focus Box, Ant 12 Only
D13740S17	Wiring Diagram Prime Focus Bos, Ant 20-Up
B13740W10	Simplified Wiring Diagram Prime Focus Box, Ant 20 - Up
D9890062	Anemometer System

Translator Drawings

B13740S01	Superior Electric HTR1008 & HTR 1500 Translator Schematic
206031	Superior Electric HTR1008 Schematic & Connection Diagram
EM185201	Superior Electric HTR1500 Schematic & Connection Diagram
D13740P02	TM600 Translator Slide Assembly
A13740Z01	TM600 Translator Slide Ass'y Bill of Materiels
D13740M02	TM600 Mounting Frame
D13740M03	TM600 Front Panel

F/R Mount Mechanical Drawings

C13740M93	Weber's Funny Bracket, Focus Synchro Gearbox
SD4601	Sterling-Detroit Focusing Feed Mount Mech Drawings

REVISIONS				
REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

DRAWN BY	DATE			
DESIGNED BY	DATE			
APPROVED BY	DATE		NEXT ASSY	USED ON

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

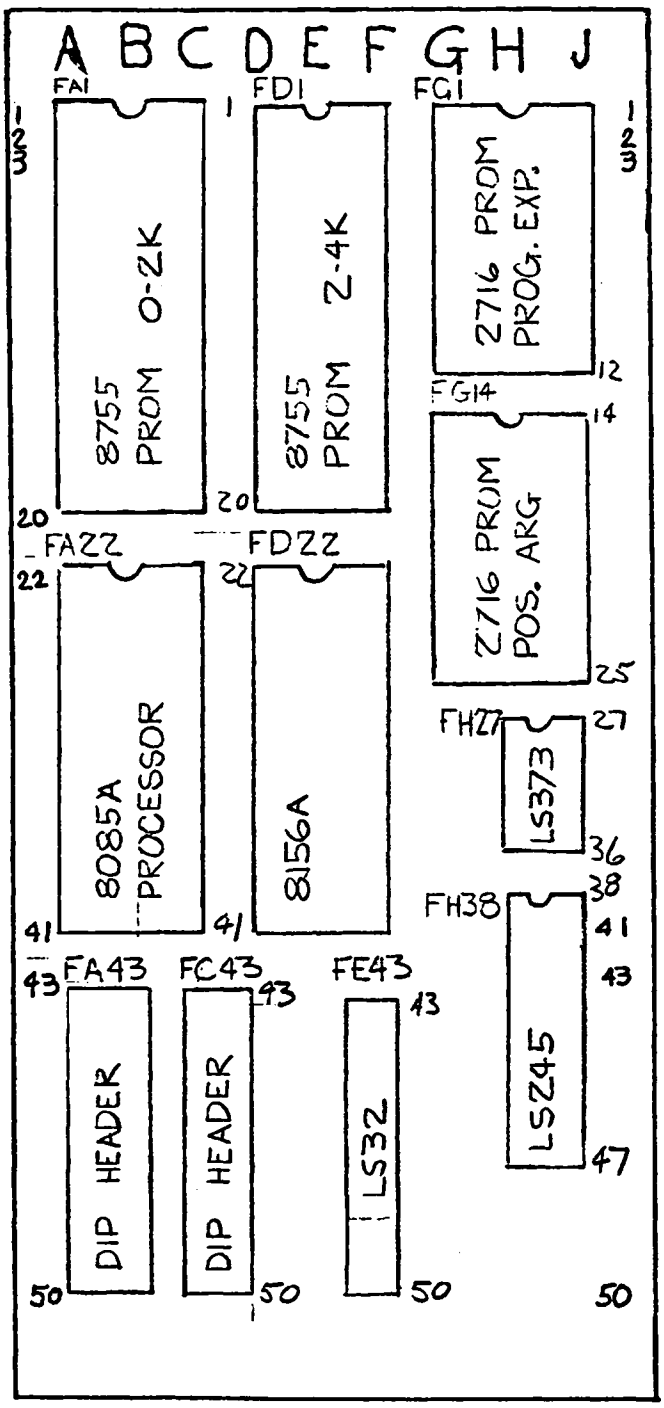
VLA

PROJECT M7-E

TITLE F/R CONTROL MODULE

DWG NO. A13740P12 SHEET 1 OF 7

LOCation F



Special sub ass'y

Item	Bom #	Dwg #

NOTES:

1. NUMBERS LIKE (FG1) INDICATE BOARD LOCATION & PIN 1 LOCATION.

NATIONAL RAIDIO ASTRONOMY OBSERVATORY
Socorro, New Mexico 87801

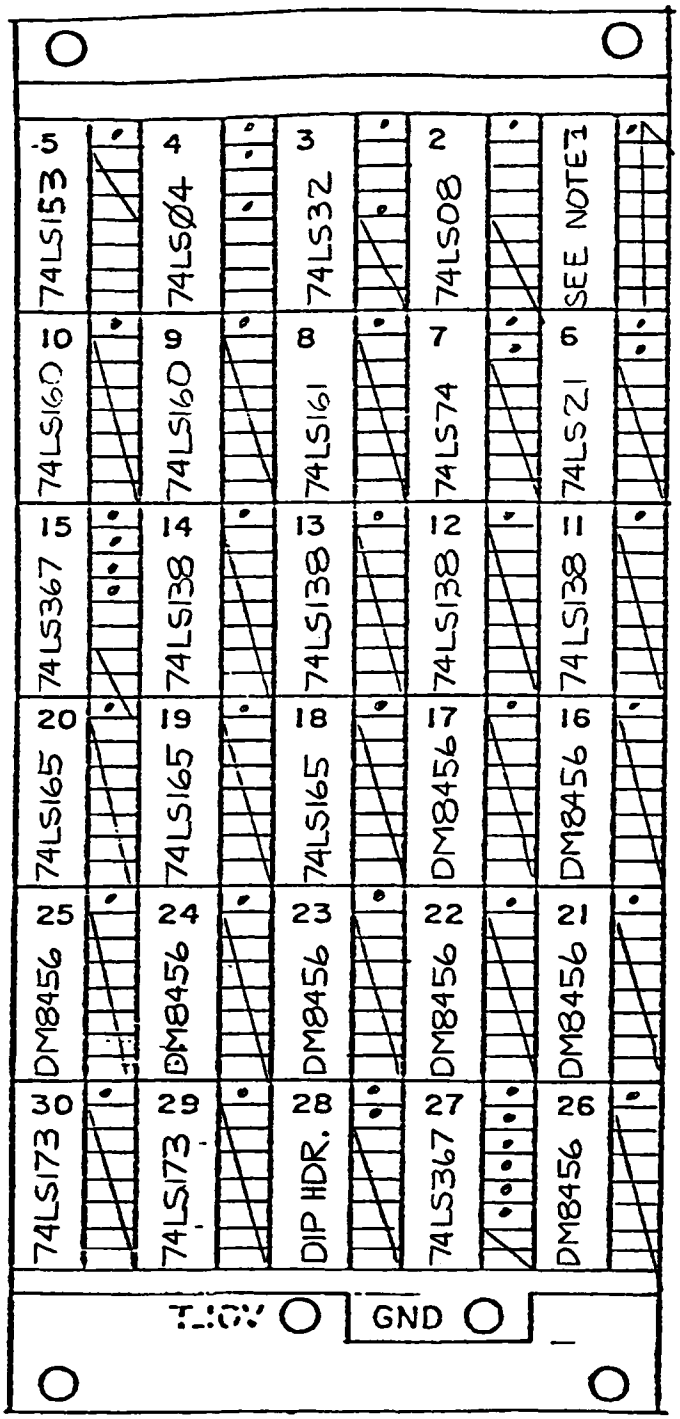
V L A

Project: M-7E

Title: F/R CONTROL MODULE

Dwg. NO. A13740P12 Sheet 2 of 7

LOC E



SPECIAL SUB ASSY'S

ITEM	BOM #	DWG #

NOTES:
PULL UP RESISTOR DIP NETWORK, BOURNS #4114R-002-470, 470 Ω

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

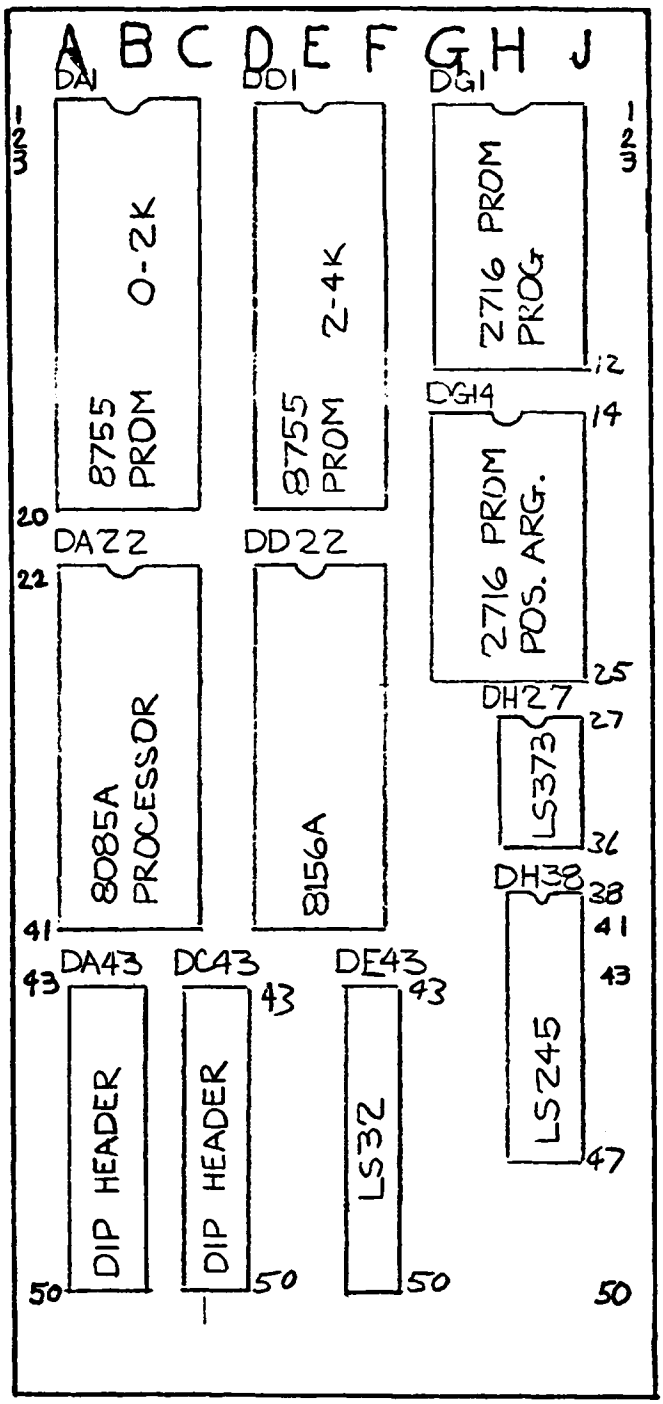
VLA

PROJECT

TITLE

DWG A13740 P12

LOCation D



Special sub ass'y

Item	Bom #	Dwg #

NATIONAL RAIDIO ASTRONOMY OBSERVATORY

Socorro, New Mexico 87801

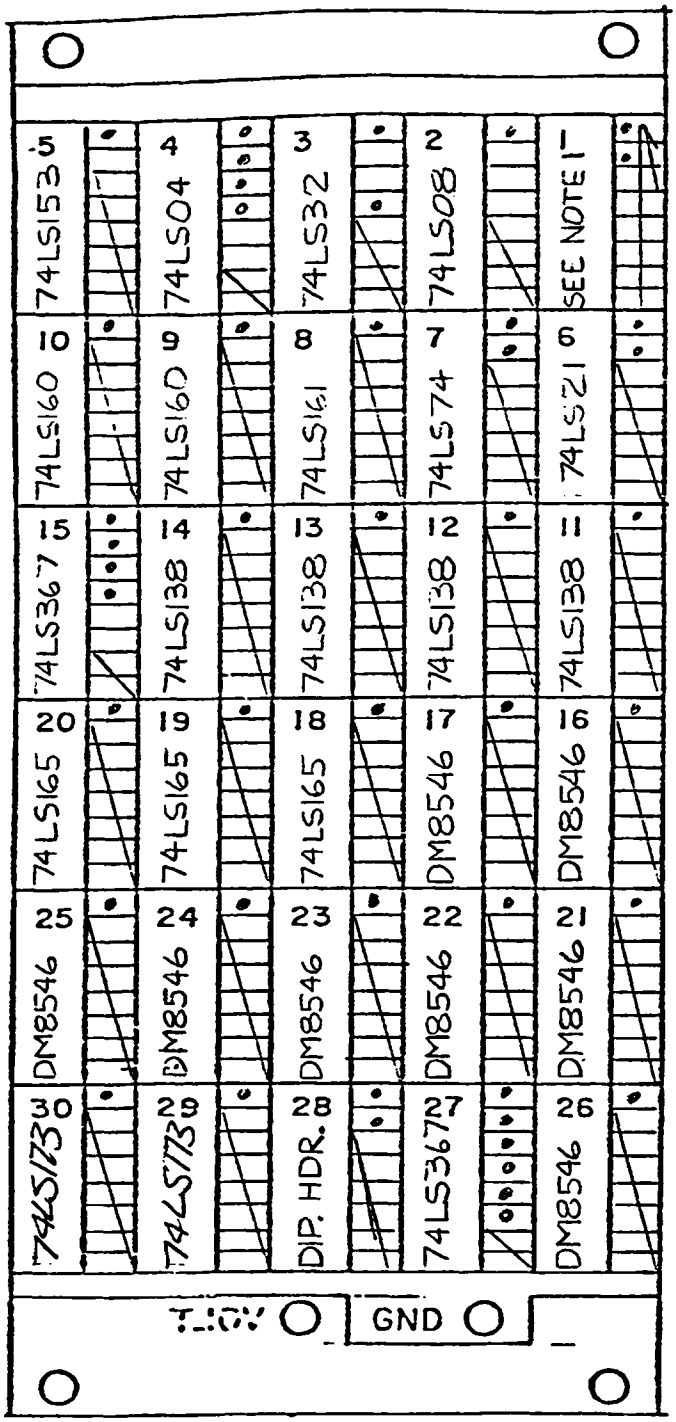
V L A

Project:

Title:

Dwg. NO. A13740P1-Z Sheet 4 of 7

LOC C



SPECIAL SUB ASSY'S

ITEM	BOM #	DWG #

NOTE

1. PULL UP RESISTOR DIP. NETWORK BOURNS #4114R-002-470, 470 Ω

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLA

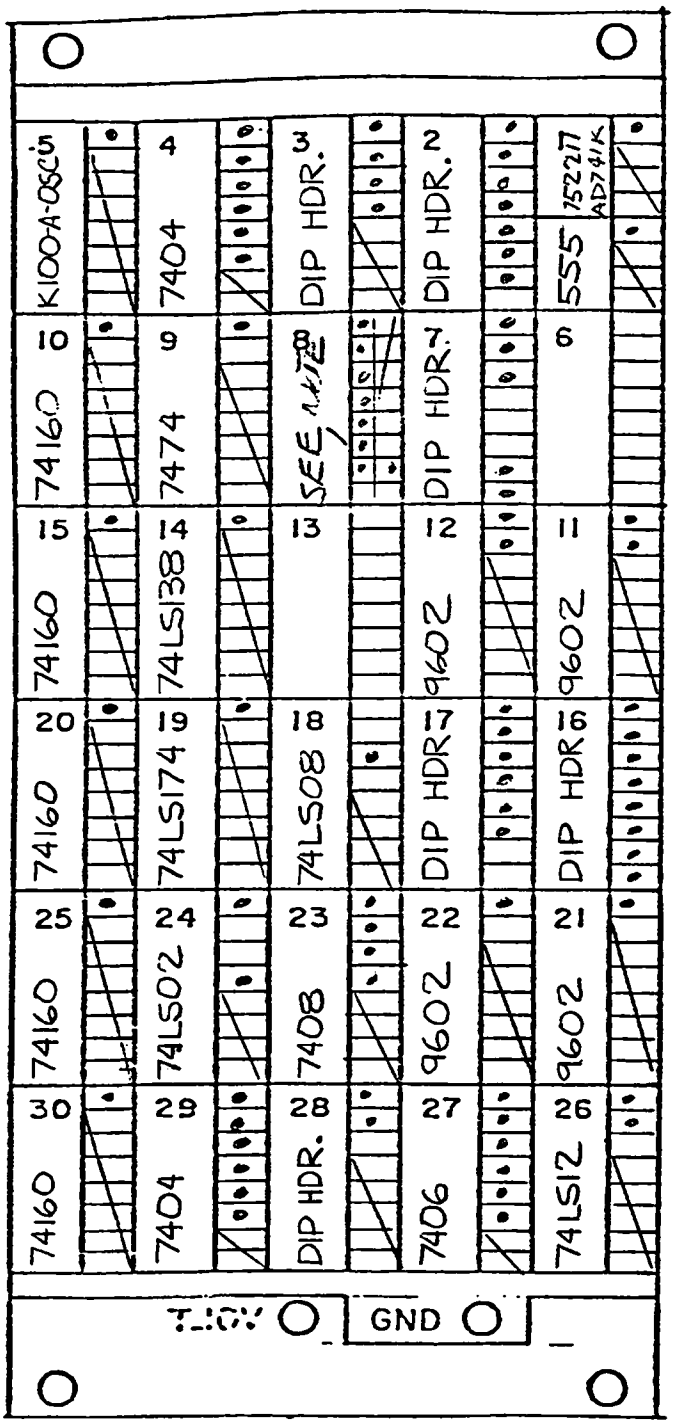
PROJECT

TITLE

DWG A13740

SHEET 5/7 D

LOC B



SPECIAL SUB ASSY'S

ITEM	BOM #	DWG #

NOTE1
1. PULL UP RESISTOR BOURNS #4114R-002-470 Ω

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLA

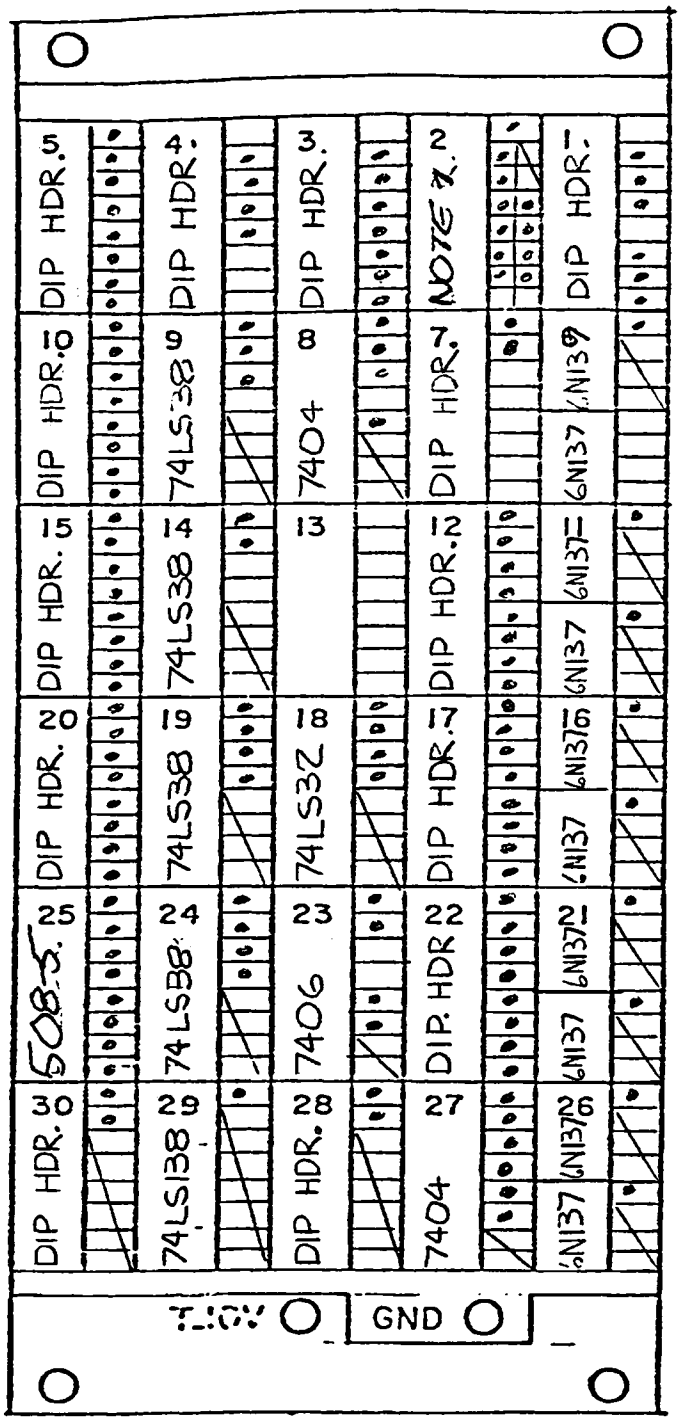
PROJECT

TITLE

DWG A1R74A.PIT

SHEET 6/7

LOC A



SPECIAL SUB ASSY'S

ITEM	BOM #	DWG #

NOTE,
1. PULL UP RESISTOR
BOURNS #4114R-002
470 Ω

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLA

PROJECT

TITLE

DWG A13740 P1Z

SHEET 7/7 OF

REV	DATE	DRAWN BY	APPROVED BY	DESCRIPTION
A	1068			ADDED NOTE 11, CHNG. FIG 1

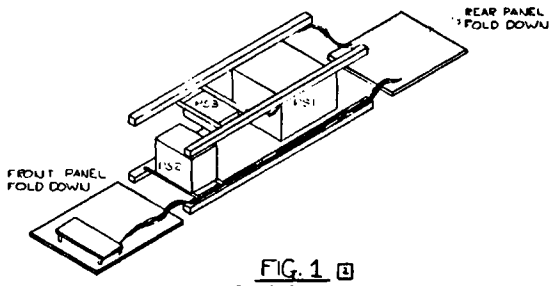
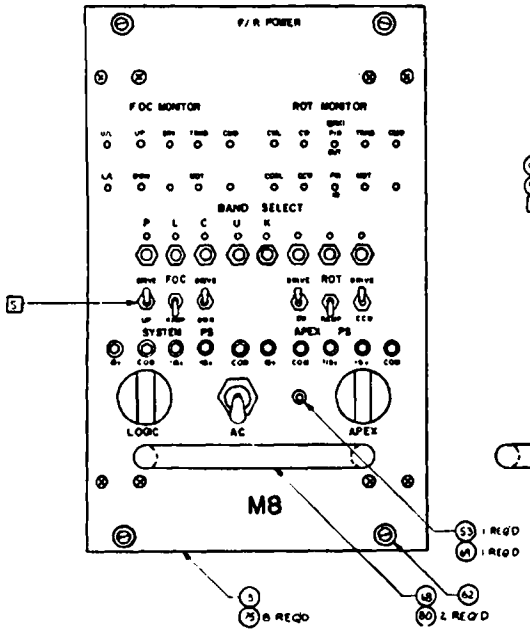
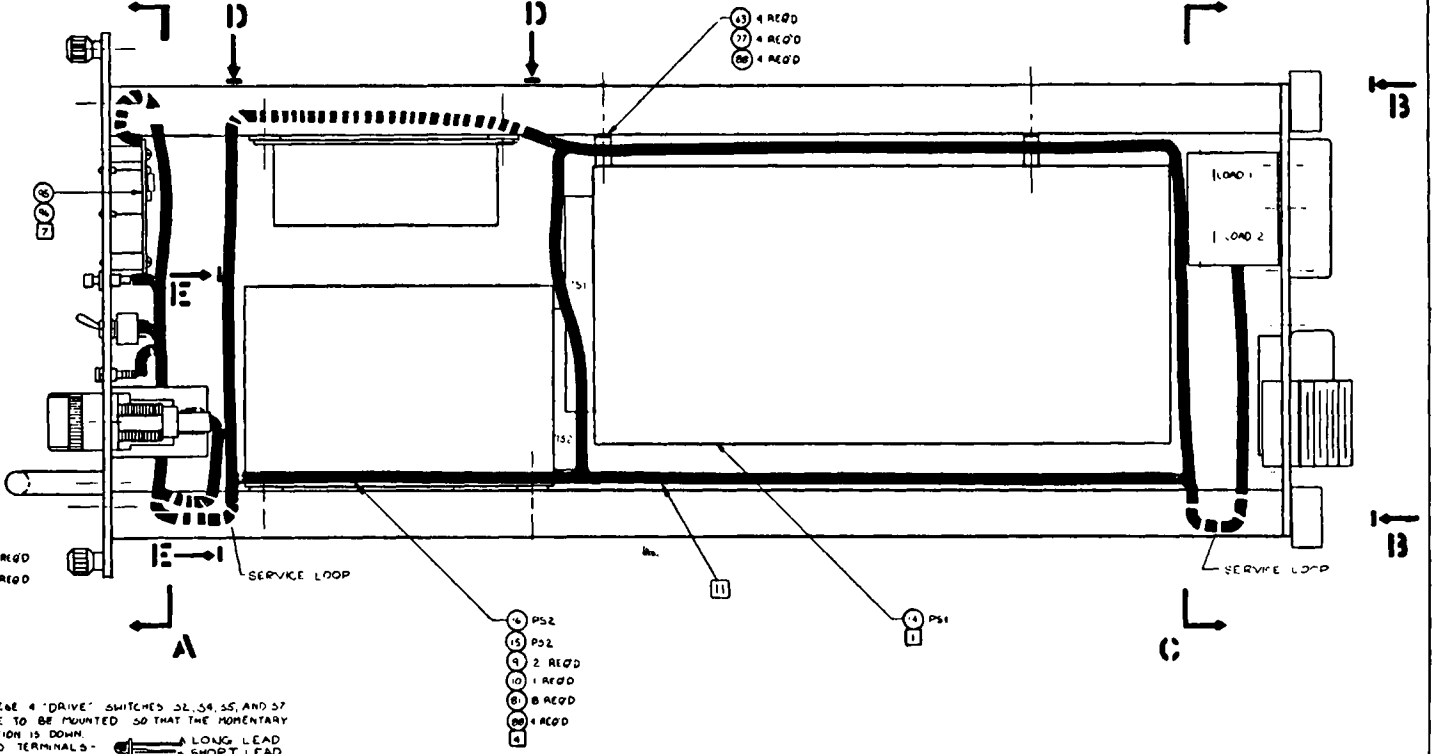


FIG. 1 [2]
SERVICE POSITION



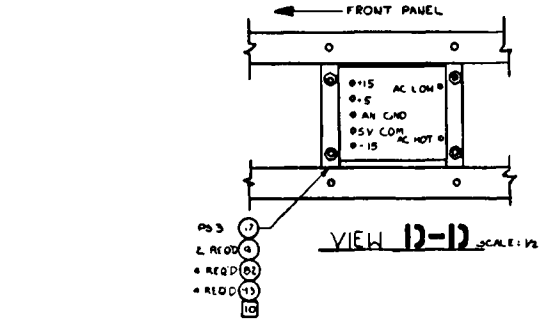


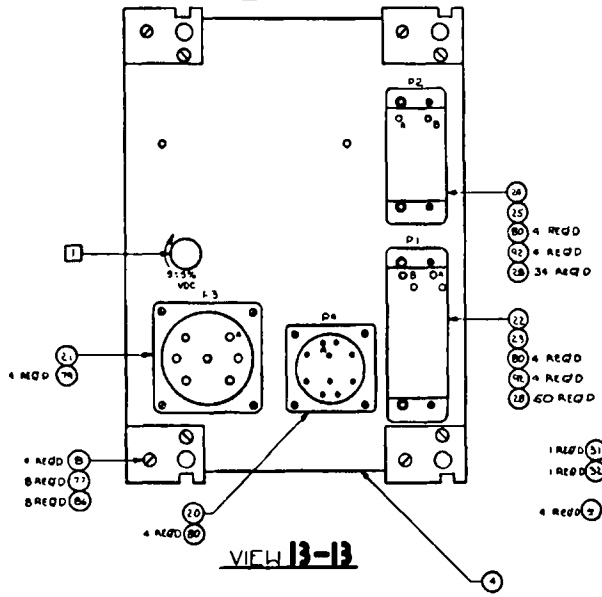
NOTES:
1. THE ADJ. POT ON PS1 MUST LINE UP WITH THE ADJUSTMENT ACCESS HOLE IN THE REAR PANEL.
2. THE COMPONENT AREAS SHOWN SHALL HAVE ENOUGH OF A WIRING SERVICE LOOP TO PIVOT THEM FROM THEIR NORMAL OPERATING POSITION TO THE SERVICE POSITION, AS SHOWN IN FIG1. WIRE RUNING BETWEEN THE VARIOUS AREAS SHALL FOLLOW ONE OF THE FOLLOWING ROUTES.
   AC. WIRING ALONG UNDERSIDE OF RAIL "A"
   D.C WIRING ALONG TOPSIDE OF RAIL "B".
3. ALL SOLDER TERMINATIONS ARE TO BE PROTECTED WITH SHRINK SLEEVING.
4. THERE ARE TWO VERSIONS OF POWER SUPPLY 2. SEE VIEW E-E FOR DETAILS. MOUNTING BRACKETS DIFFER GREATLY. SEE DRAWING NUMBERS D1S7401SB AND D1S7401SA
5. THESE 4 "DRIVE" SWITCHES S2, S4, S5, AND S7 ARE TO BE MOUNTED SO THAT THE MOMENTARY ACTION IS DOWN.
6. LED TERMINALS - A LONG LEAD, A SHORT LEAD
7. SEE FRONT PANEL DISPLAY BOARD ASSY DWG. "B1S7401P1" AND BILL OF MATERIALS "A1S7402-2"
11. DRESS HARNESS ON TOP OF BOTTOM BARS (ON BOTTOM OF TOP BARS), SO THAT AIR FLOW OF PS1 IS NOT IMPEDED

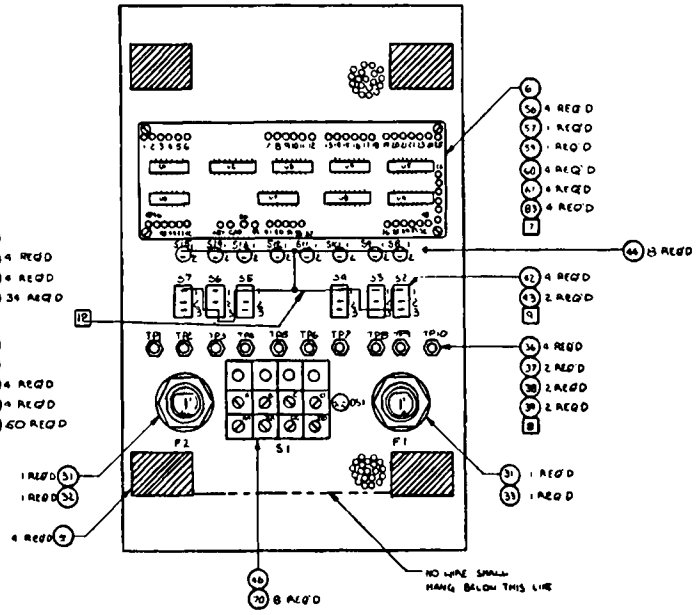
BILL OF MATERIALS NUMBER, A1S7402-11

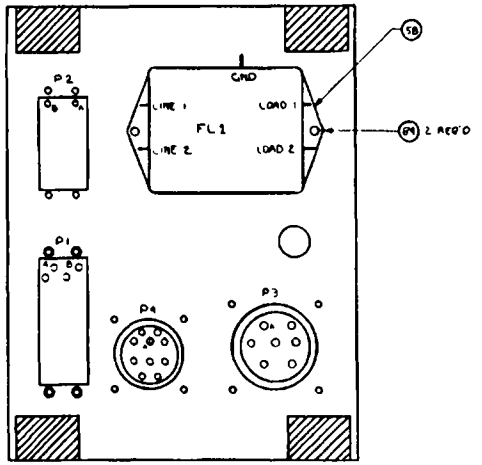
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	MODEL C M-8	NATIONAL RADIO ASTRONOMY OBSERVATORY
TOLERANCES ANGLES ±	MODULE ASSY. DRAWING	DRAWN BY
3 PLACE DECIMALS ±		CHECKED BY
2 PLACE DECIMALS ±		APPROVED BY
1 PLACE DECIMALS ±		DATE 6-5-69
MATERIAL		SHEET 1 OF 8
FINISH		DRAWING NUMBER D1S7401-B
NEXT ASSY	USED ON	REV

REV	DATE	DRAWN BY	APPROVED BY	DESCRIPTION
A	10 84			ADDED NOTE 12 & MADE MINOR CHANGE





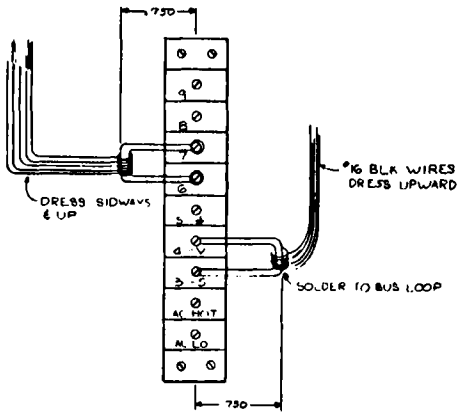




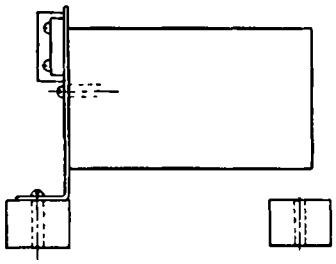
NOTES:
8. IN SECTION A-A TP1, 4, 6, 9 ARE BLACK, TP2, AND 7 ARE ORANGE, TP3 AND 8 ARE RED, TP5 AND 0 ARE YELLOW.
9. IN SECTION A-A S2, 4 S, AND 7 ARE MOMENTARY TOGGLE SWITCHES. (ON-NONE-ON MOM). S3 AND S6 ARE SINGLE POLE - SINGLE THROW. (ON-NONE-ON).
10. TO MOUNT P33 TO THE MOUNTING PLATE USE 4-40 SCREWS, CSK. THE MOUNTING HOLES Ø .25 DIA & .08R DEEP
11. #18 BUS WIRE, ON 2 ROWS OF SWITCHES

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	VLA	MODEL C	NATIONAL RADIO ASTRONOMY OBSERVATORY
TOLERANCES: ANGLES ± 2°; 3 PLACE DECIMALS ± .005; 2 PLACE DECIMALS ± .01; 1 PLACE DECIMALS ± .1		M8 MODULE ASSY. DRAWING	
MATERIAL			
FINISH			
NEXT ASSY	USED ON	SHEET 2 OF 8	D137460 P1B REV A

DETAIL 1
BUS WIRE LOOP PST

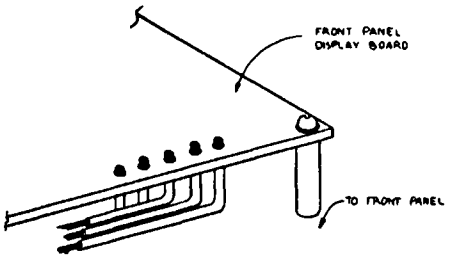


DETAIL 2
FRONT PANEL DISPLAY BOARD WIRE TERMINATION

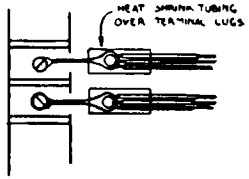


VIEW E-E

THIS IS THE MOUNTING VIEW FOR PSZ, VERSION 2 LAMBDA LND-Z-152

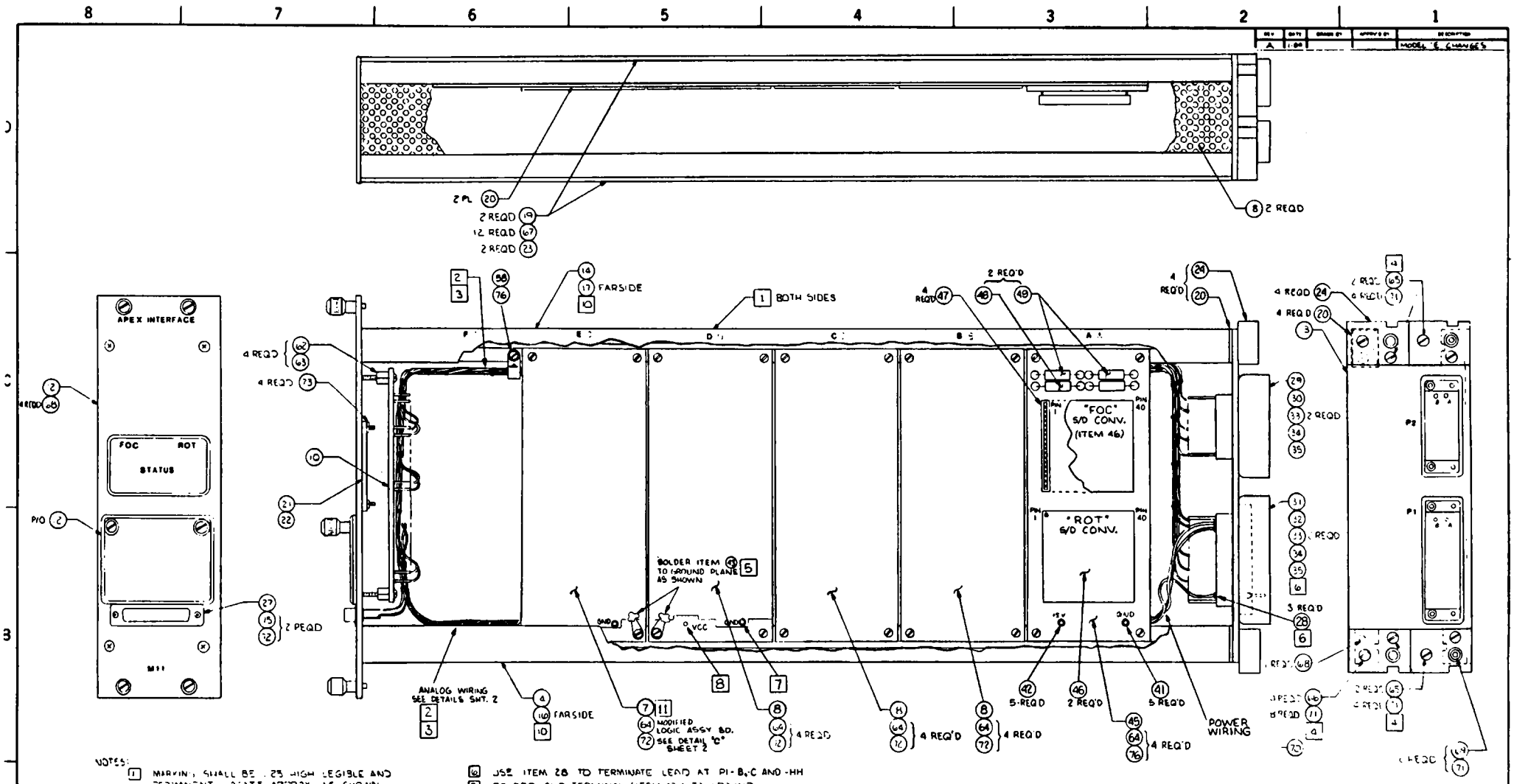


DETAIL 3
215 VOLT POWER SUPPLY OUTPUT TERMINATIONS



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	MODEL C
MATERIAL	MB
FINISH	MODULE ASSY. DRAWING
NEXT ASSY / USED ON	01-5740P18

NATIONAL RADIO ASTRONOMY OBSERVATORY



NOTES:

1. MARKING SHALL BE .25 HIGH LEGIBLE AND PERMANENT. LOCATE APPROX AS SHOWN.
2. A WIRING LOOP OF SUFFICIENT LENGTH TO ALLOW THE FRONT & REAR PANELS TO BE FOLDED FLAT MUST BE PROVIDED.
3. THE ANALOG INPUT HARNESS (USE ITEM 55) PER NRAO DWG D13720 SHT 7) IS TO BE ROUTED ALONG THE LOWER RAIL (ITEM 16) AND ALL OTHER I/O WIRING IS TO BE ROUTED ALONG THE UPPER RAIL (ITEM 7).
4. WIRE TWO WASHERS (ITEM 71) ARE REQUIRED PLACE ONE UNDER THE SCREW HEAD AND THE OTHER BETWEEN THE GUIDE (ITEM 20) AND THE REAR PANEL (ITEM 15).
5. SOLDER SOLDER LUG (ITEM 43) TO GROUND PLANE AND PLACE UNDER SCREW HEAD APPROX AS SHOWN.
6. USE ITEM 28 TO TERMINATE LEAD AT P1-B,C AND -HH
7. SOLDER GND TERMINAL (ITEM 42) TO GROUND PLANE (COMPONENT SIDE OF ITEMS 7,8 AND 9).
8. SOLDER PWR TERMINAL (ITEM 41) TO PWR PLANE (WIRE-WRAP SIDE OF ITEMS 7,8 AND 9).
4. THE PWR & GND BUS WIRING SHALL BE ON THE WIRE-WRAP TERM SIDE OF ITEMS 7,8 AND 9.
10. THE KAPTON TAPE (ITEM 57) SHALL RUN THE FULL LENGTH OF THE RAILS (ITEMS 16 & 17).
11. MODIFIED LOGIC CONNECTOR BOARD (D13720M23) SHALL BE INSTALLED IN LOCATION "E" ONLY. LOCATIONS "B" THRU "D" ARE TO USE STANDARD D13720M53.
12. USE ITEM 4 TO INSTALL I.C.'S ON ITEMS 7 AND 8.

BOM - A1374029

A1374029	BOM
NEXT ASSY	USED ON

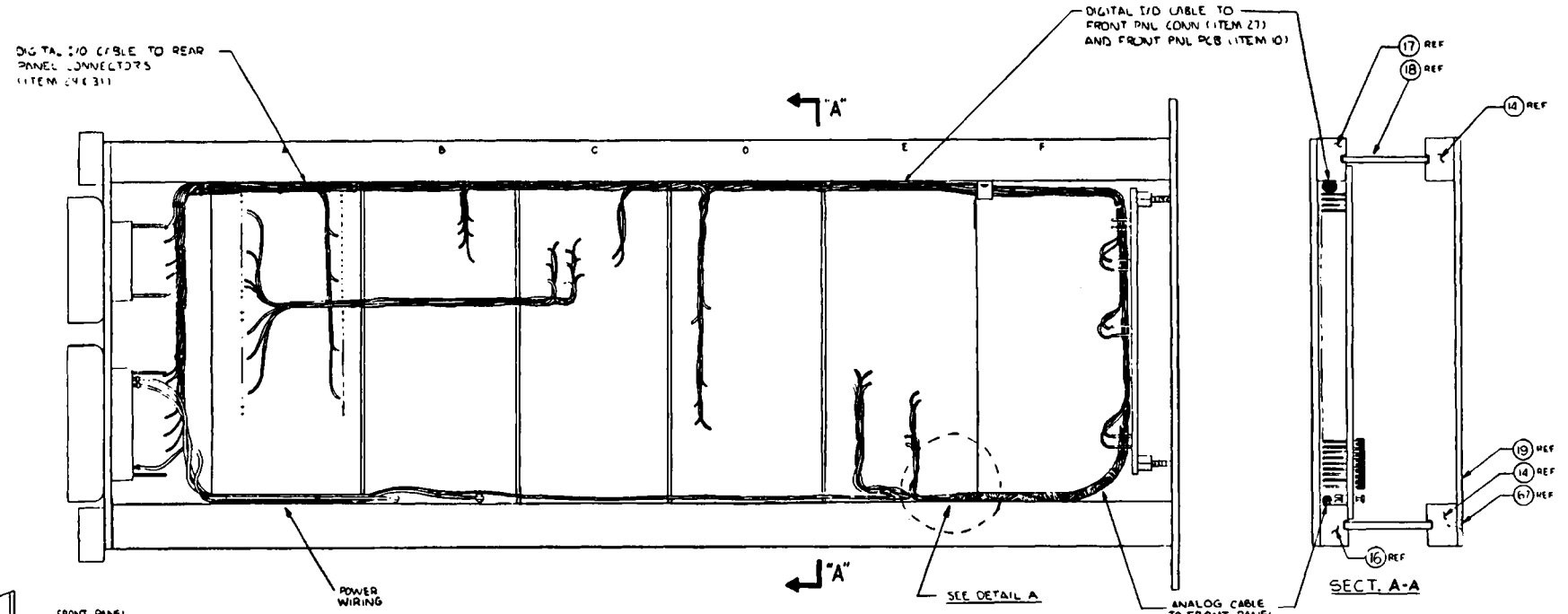
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
1 PLACE DECIMALS: ±
2 PLACE DECIMALS: ±
3 PLACE DECIMALS: ±
MATERIAL
FINISH

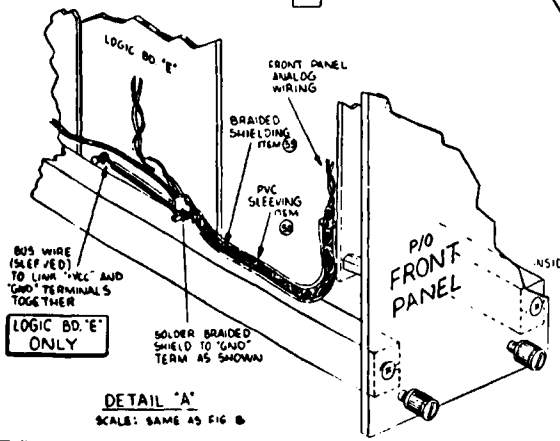
M11

F/R APEX INTERFACE MODULE

NATIONAL RADIO ASTRONOMY OBSERVATORY

D13745P15





DETAIL "A"
SCALE: SAME AS FIG B

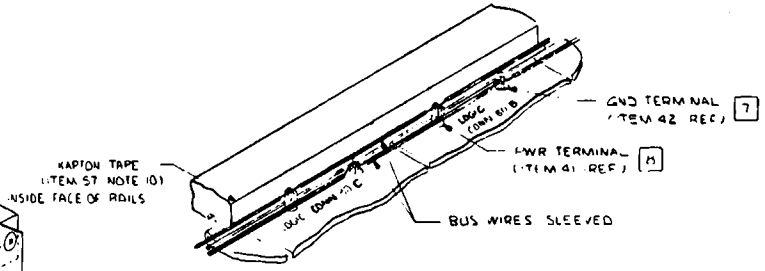
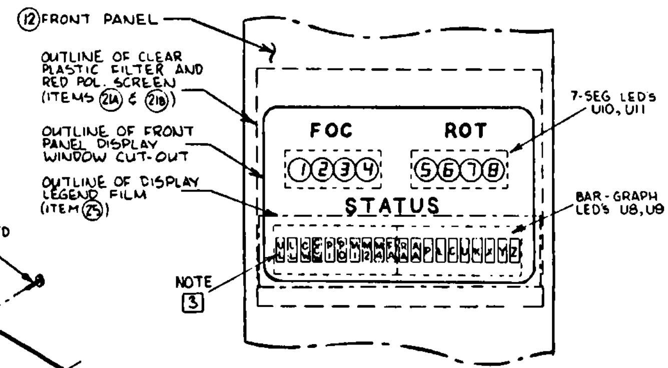


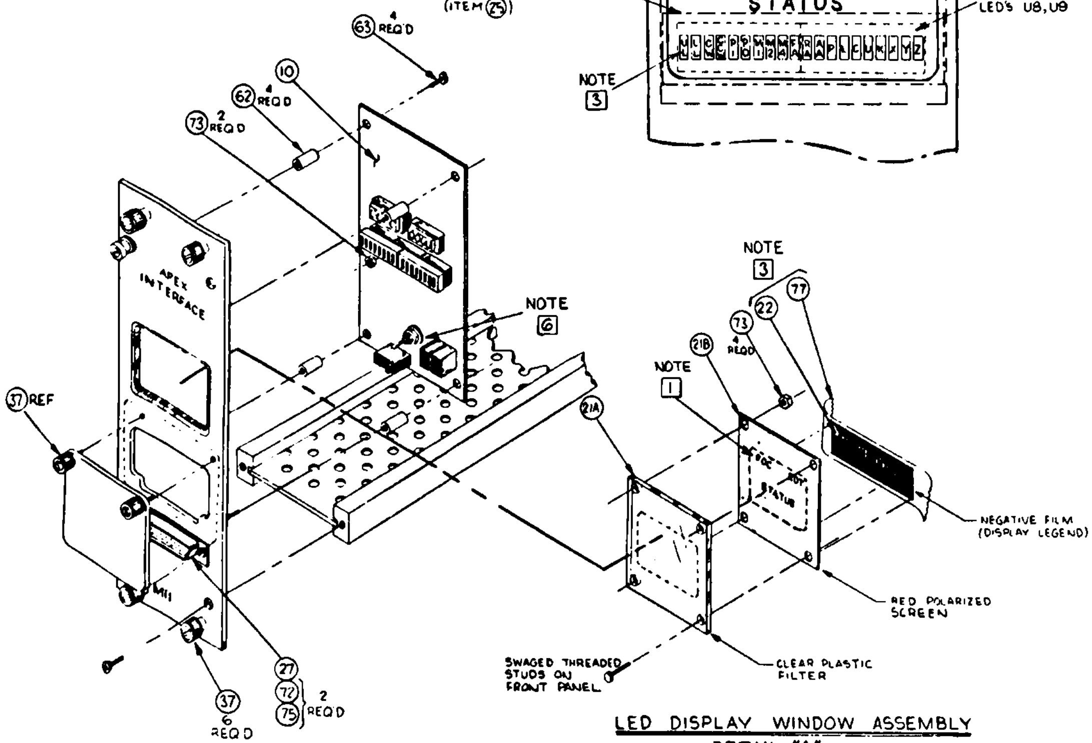
FIGURE B
SCALE: NONE
PARTIAL SECTION OF PWR GND BUS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	M11
MATERIAL	F/R APEX INTERFACE MODULE
FINISH	
NEXT ASSY / USED ON	DI3 740P15

NATIONAL RADIO ASTRONOMY OBSERVATORY

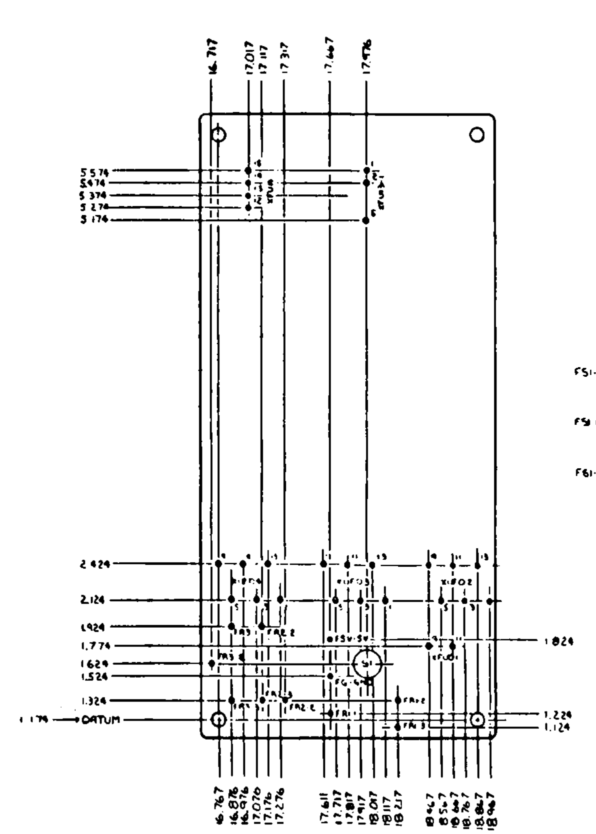
DISPLAY PLACEMENT
DETAIL "B"

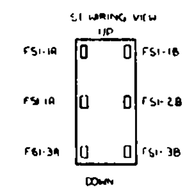




LED DISPLAY WINDOW ASSEMBLY
DETAIL "A"

DETAIL "C"
COMPONENT WIRING VIEW





SPECIAL ASSEMBLY INSTRUCTIONS
(MII FRONT PANEL DISPLAY)

[1] APPLY WHITE LETTERING, 1/8" HIGH FOR "FOC", "ROT" AND "STATUS" TO RED POLARIZING SCREEN, SIDE FACING OUT, USING RUB-OFF LETTERS OR SCREEN PROCESS. ALIGN LETTERS TO DISPLAY DEVICES U8-U11 AS SHOWN IN DETAIL "B" BY MAKING A PRE-ASSEMBLY OF FILTER, SCREEN AND ASSEMBLED DISPLAY P.C. BOARD (ITEM C) TO CORRESPONDING MOUNTING STUDS ON FRONT PANEL.

[2] MOUNT FILTER & SCREEN (ITEMS 21A, 21B) TO THREADED STUDS ON FRONT PANEL USING NYLON HEX NUTS (ITEM 73).

[3] MOUNT DISPLAY LEGEND NEGATIVE FILM STRIP (ITEM 22) TO INSIDE FACE OF RED POL. SCREEN USING TRANSPARENT TAPE. ALIGN LETTERING FOR EXACT POSITIONING WITHIN THE L.E.D. ILLUMINATED BAR WHEN DISPLAY P.C. BOARD IS PROPERLY MOUNTED. ENSURE "UL" IS INSIDE LEFT-MOST LED BAR. SEE DETAIL "B". THIS ALIGNMENT IS CRITICAL!

[4] PERMANENTLY MOUNT DISPLAY P.C. BOARD TO FRONT PANEL USING THREADED STUDS, THREADED SPACERS (ITEM 62) AND MACHINE SCREWS (ITEM 63).

[5] ENSURE L.E.D. DISPLAY DEVICES ARE FLUSH AGAINST FILTER & SCREEN AFTER MOUNTING DISPLAY P.C. BOARD FOR MAXIMUM DISPLAY VISABILITY. ILLUMINATE LED'S TO CHECK FINAL ALIGNMENT OF ALL COMPONENTS.

[6] ENSURE PROPER CLEARANCE BETWEEN REMOVABLE SUB-PANEL TO THE POTS AND SWITCH ON DISPLAY P.C. BOARD.

C13740P13	FP PCB ASSY
NEXT ASSY	USED ON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL

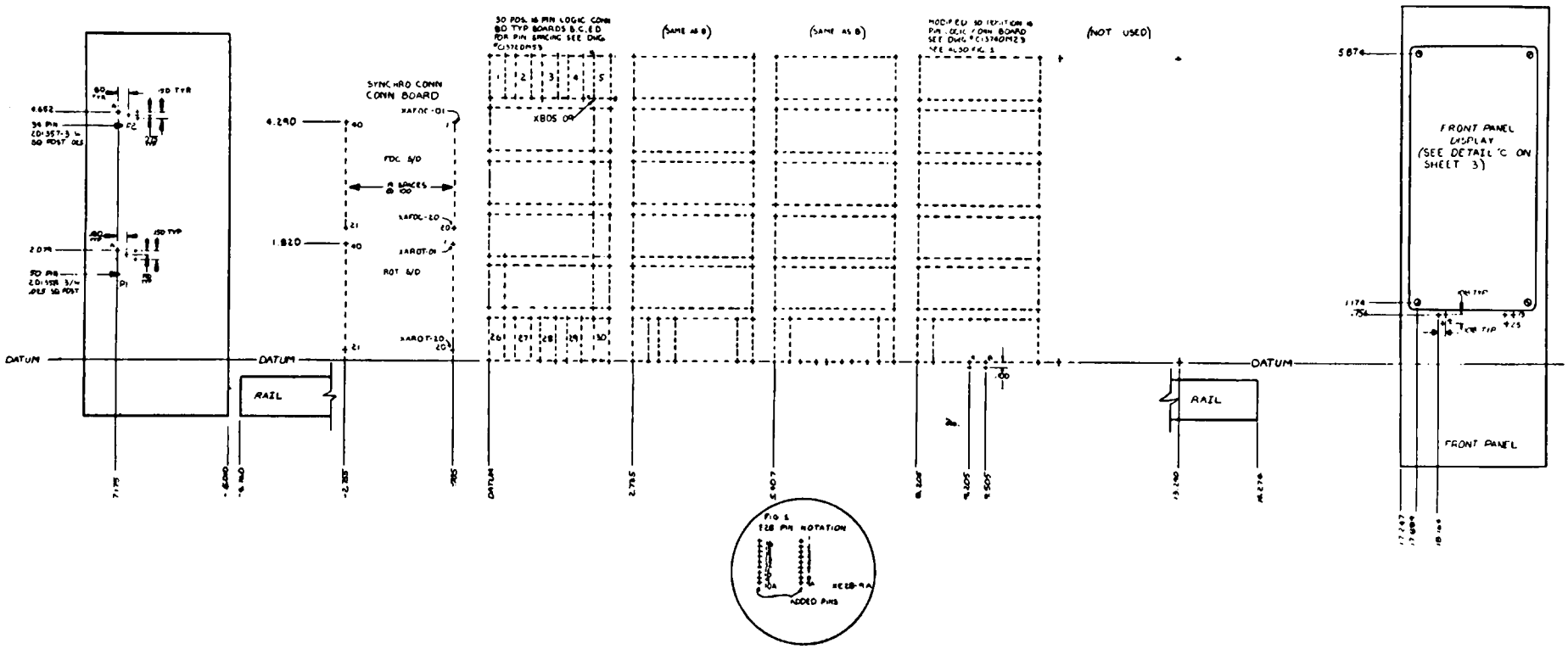
FINISH

MII - F/R APEX INTERFACE MDL

ASSEMBLY DWG

NATIONAL RADIO ASTRONOMY OBSERVATORY

SHEET 3 of 3 — DRAWING NUMBER D13740P15



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		M11	NATIONAL RADIO ASTRONOMY OBSERVATORY
MATERIAL		F/R APEX INTERFACE MODULE	
FINISH			
NEXT ASSY	USED ON		

VISIONS

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

DRAWN BY	DATE			
DESIGNED BY	DATE			
APPROVED BY	DATE		NEXT ASSY	USED ON

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

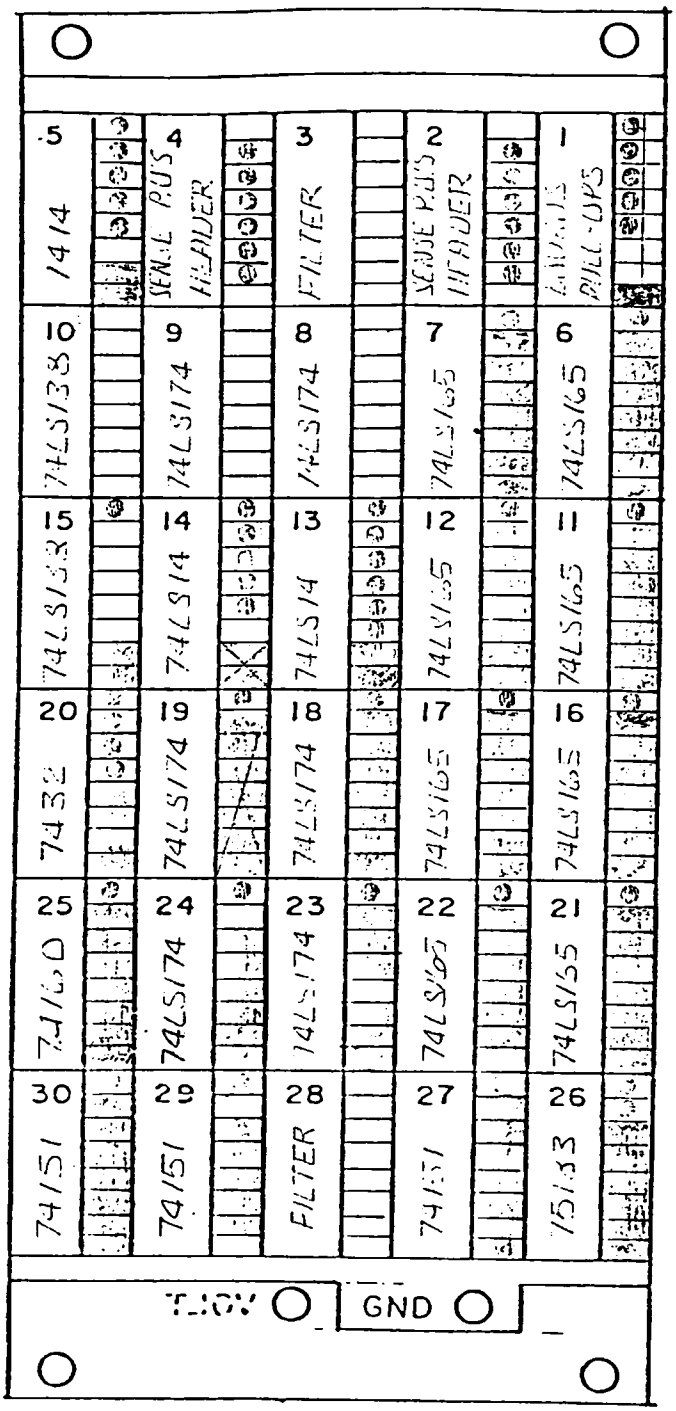
VLA

PROJECT M11

TITLE F/R APEX INTERFACE IC MODULE LOCATION

DWG NO. A13740-P11 SHEET 1 OF 4

LOC W - DIGITAL



SPECIAL SUB ASSY'S

ITEM	BOM #	DWG #

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

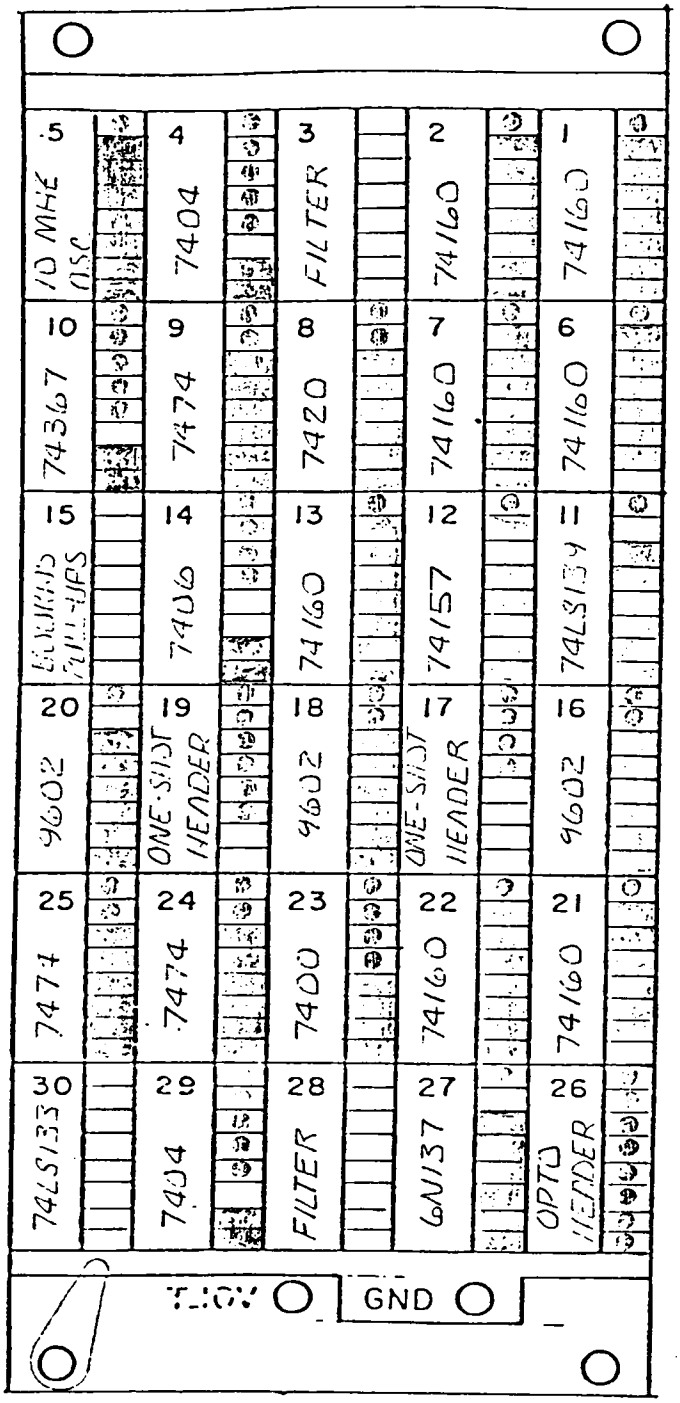
VLA

PROJECT M11

TITLE F/R APEX INTERFACE IC MODULE LOCATION

DWG NO. A1E-COP11 SHEET 2 OF

LOC C- DIGITAL



SPECIAL SUB ASSY'S

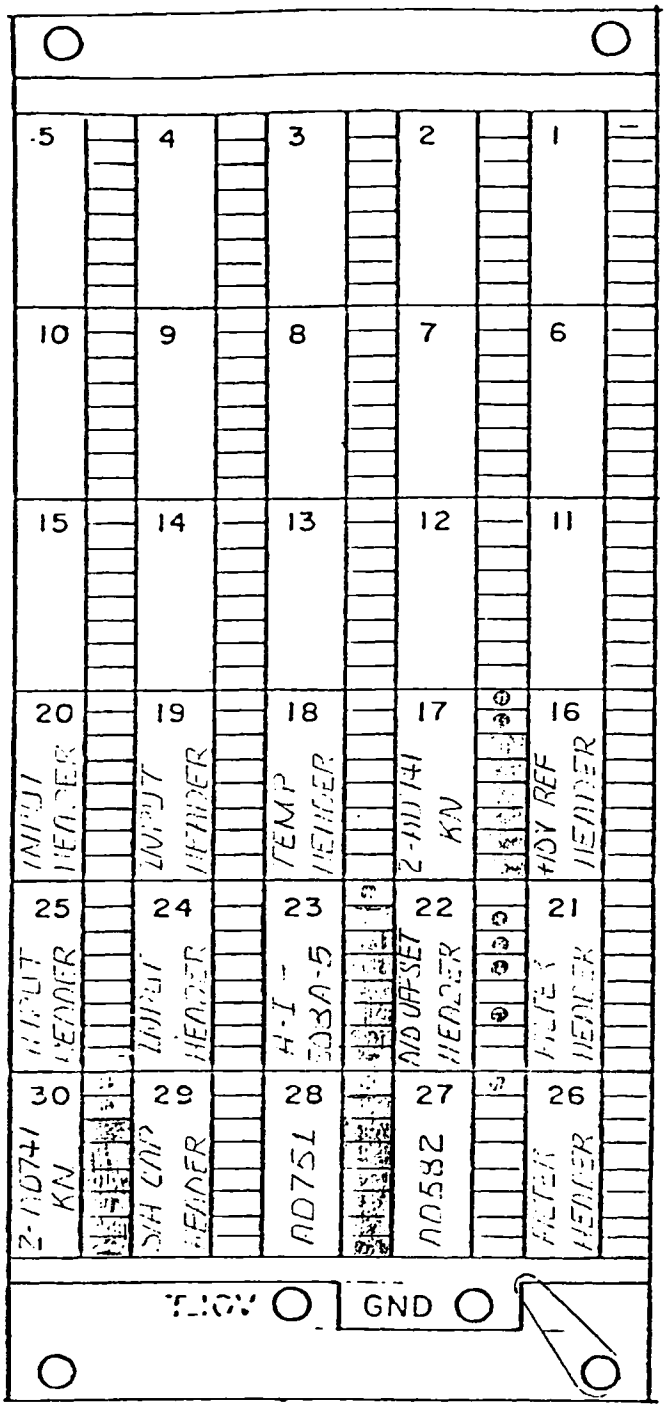
ITEM	BOM #	DWG #

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLA

PROJECT M11
TITLE F/R APEX INTERFACE
IC MODULE LOCATION
DWG NO. A13740P11 SHEET 2 OF

LOC D - ANALOG

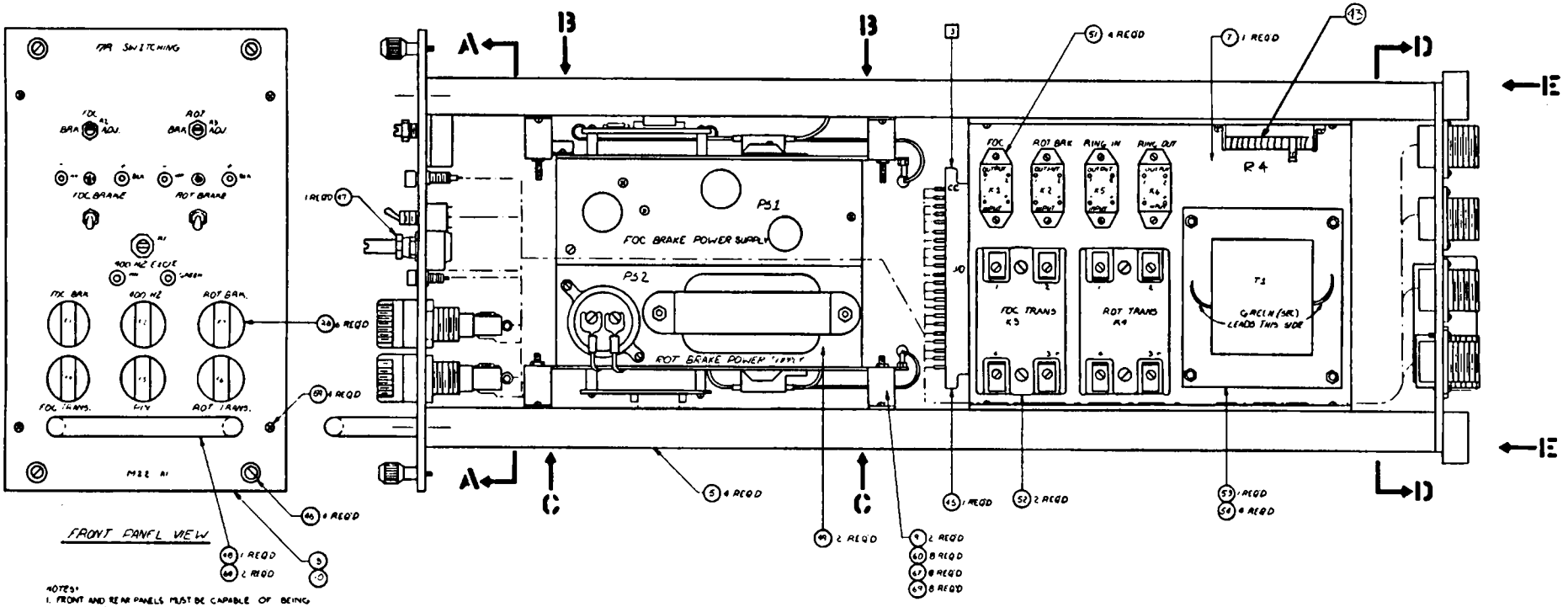


SPECIAL SUB ASSY'S

ITEM	BOM #	DWG #

NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801	VLA	PROJECT M&C TITLE FIR ADEX INTERFACE IC MODULE LOCATION DWG NO. A1376.P11 SHEET 4 OF

REV	DATE	DRAWN BY	APPROV'D BY	DESCRIPTION
A	7-14-89			CHANGED BOYE 8
B	1-11-91			ADDED R2



FRONT PANEL VIEW

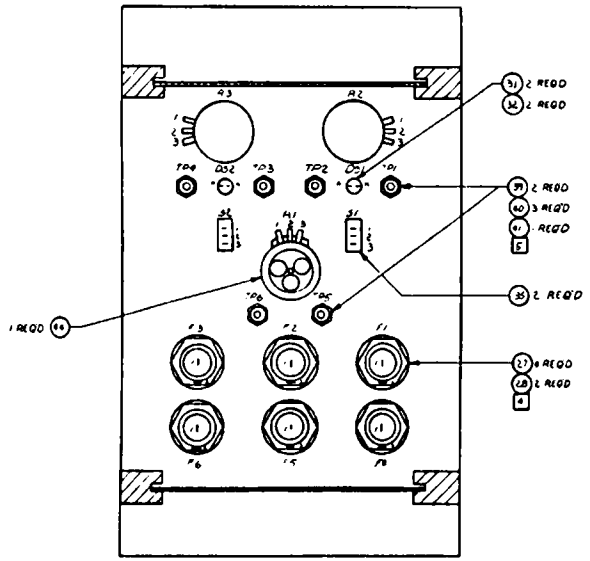
NOTES:
1. FRONT AND REAR PANELS MUST BE CAPABLE OF BEING SWUNG 90° TO THE SIDE FOR ACCESS TO THE COMPONENTS AND TO ENABLE THE TOP AND BOTTOM SCREEN COVERS TO BE SLID IN PLACE.
2. ALL SOLDER TERMINATIONS ARE TO BE COVERED WITH HEAT SHRINK.
3. ORIENT J10 AS SHOWN

BILL OF MATERIALS = D1370213

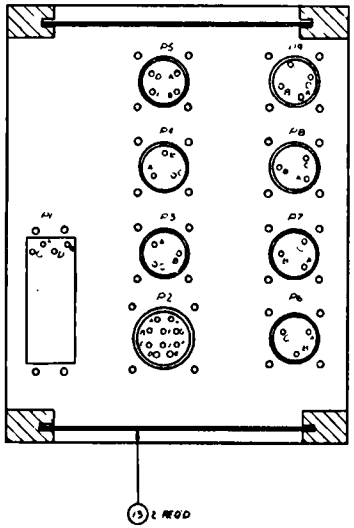
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	
MATERIAL	
FINISH	
NEXT ASSY	USED ON

SIZE	1722
TITLE	FIR SWITCHING MODULE, ASSY. DWG.
DRAWN BY	
APPROVED BY	
DATE	6-28-89
	1/11/91

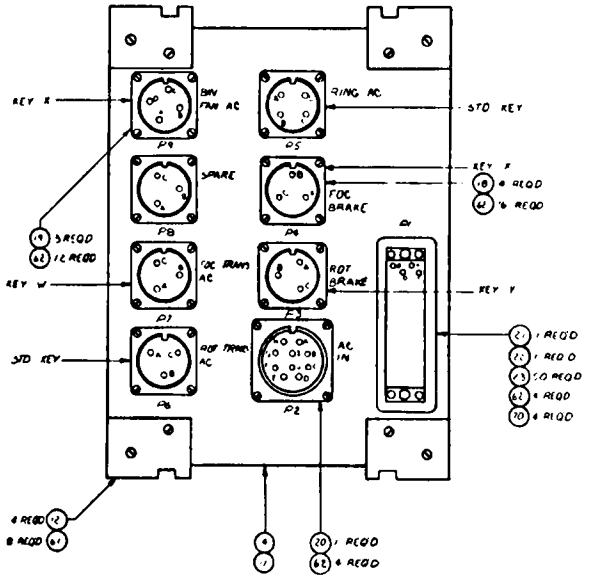
NATIONAL RADIO ASTRONOMY OBSERVATORY



SECTION A-A



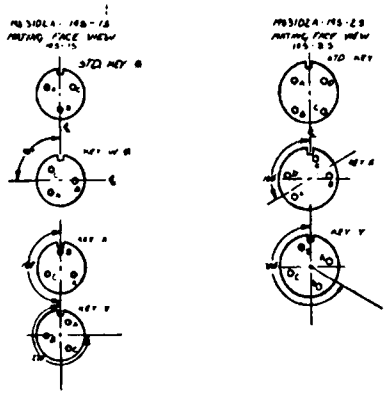
SECTION B-B



VIEW E-E

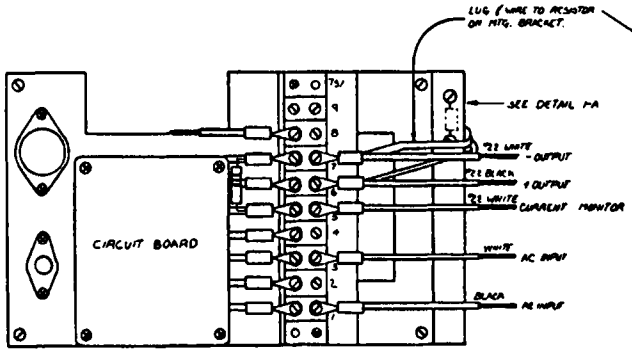
NOTES:
1. F1, F2, F3 AND F5 ARE 2 AMP, 250 VOLT FUSES. F4 AND F6 ARE 8 AMP 32 VOLT FUSES.
2. TP 2 AND TP 4 ARE BLACK, TP 1, 3 AND 5 ARE WHITE, TP 6 IS GREEN.

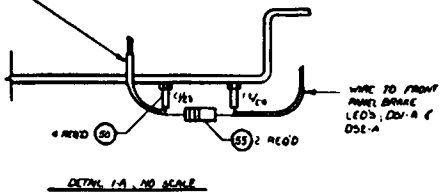
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	VLA	M22	NATIONAL RADIO ASTRONOMY OBSERVATORY
MATERIAL		F/R SWITCHING MODULE ASSY. DRAWING	
FINISH			
NEXT ASSY / USED ON			



REAR PANEL PLUG DETAIL
ALTERNATE INSERT POSITION

NOTE
1. STANDARD MS CONNECTOR KEYING CONFIGURATION.





DETAIL 1A, NO SCALE

VIEW B-B AND C-C

P5J & P5R TERMINAL VIEWS.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		M22	NATIONAL RADIO ASTRONOMY OBSERVATORY		
		MATERIAL	F/R SWITCHING MODULE ASSY. DWG.		
NEXT ASSY	USED ON	FINISH			

REVISIONS

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
—	6-83			NEW F/R SYSTEM MODEL-E DESIGN. SEE SHT "A-1" TO "A-5" FOR PICTORAL REPRESENTATION OF THIS CONFIGURATION
A	7/5/84			MANY WIRING CHANGES AS REQ'D TO MAKE SYSTEM WORK.
B	8/14/84			CORRECTED APEX TEMP PROBE WIRING ERRORS ON PAGES 48, 44 & 3
C	8/27/84			ADDED ROT RING RETRACT SSR DRIVE, MOVED ROT BRAKE SSR DRIVE TO W3J1-Z FROM W3J1-N PAGES AFFECTED: 7, 42, 46; 14, 26, 28, 9
D	10/01/84			CHANGED PART NO.'S FOR I/O CONN. PANEL SHEET A-5
E	1/28/85			ADDED ANEMOMETER (2 WIRES) FROM I/O-J5 TO J1 OF DATA SET VIA BIN to BIN JUMPER pg: 12, 20, 21, 24 ADDED PAGES 21A & 21 Block Dia. & wire list
F	1/28/85			ADC FRAME Gnd wire from M8 pg: 16 moved ALGI-3 to ALGI-0 pg: 20, 21, 27, 15, 7
G	2/5/85			Fire Led's on M8 pg: 6, 8, 18
H	5/22/85			ELIMINATED APEX SSR DRIVE FOR RING EXTEND & RETRACT & CORRECTED ERRORS SEE SHEET 52

DRAWN BY	DATE 8/11/83			
DESIGNED BY	DATE			
APPROVED BY	DATE 8/11/82		NEXT ASSY	USED ON

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

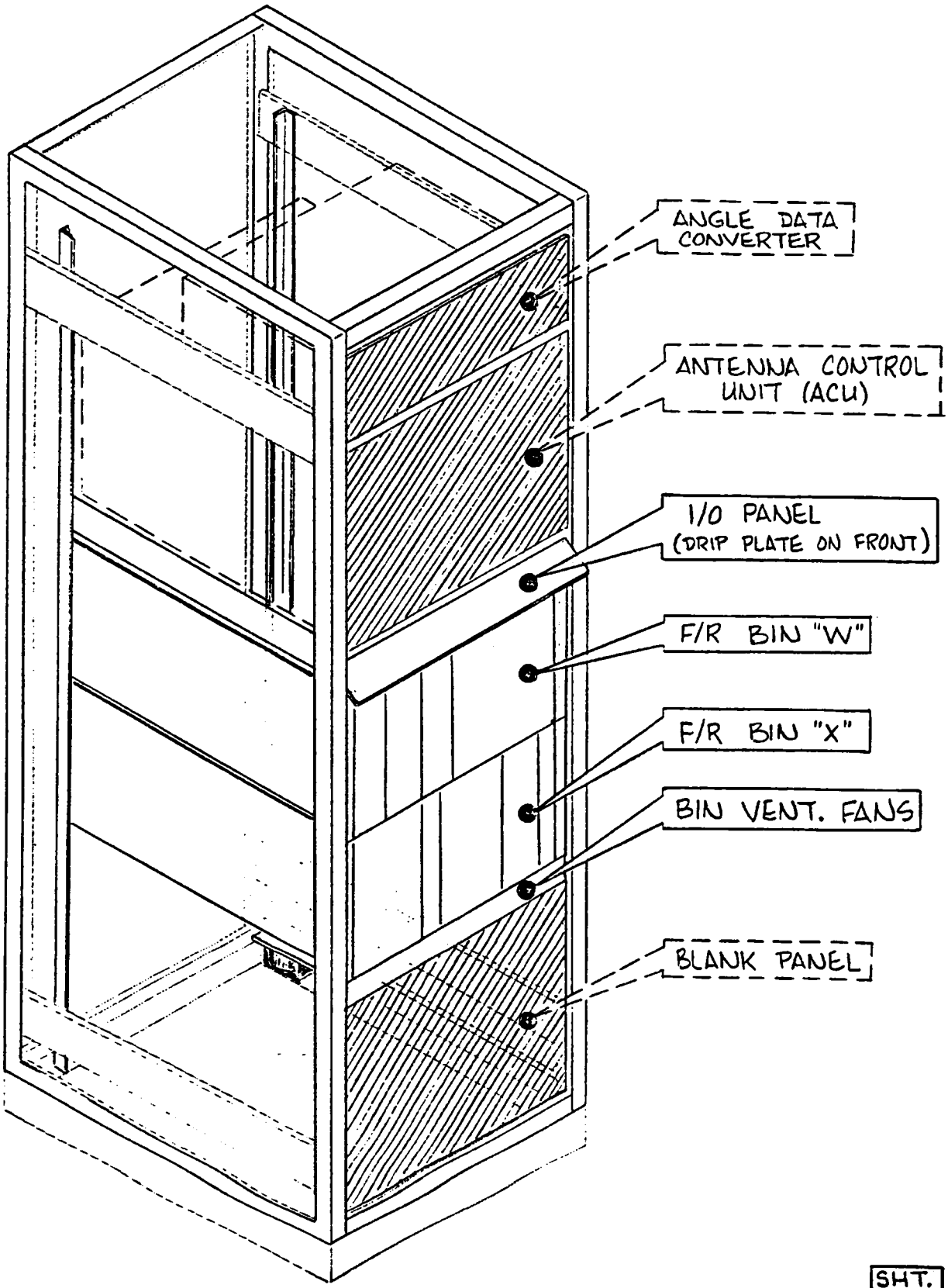
VLA

PROJECT F/R SYSTEM MODEL E

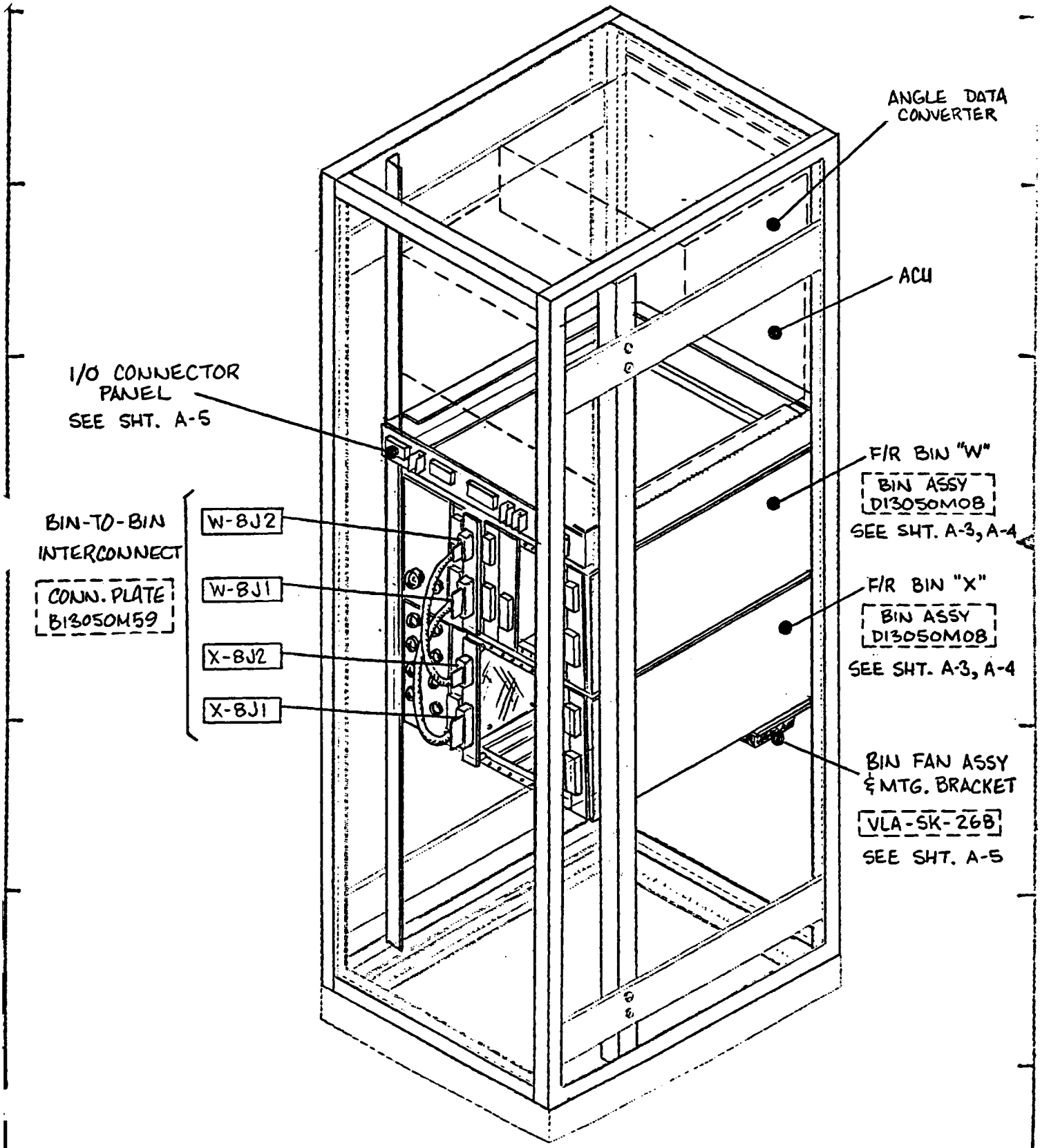
TITLE "C" RACK LAYOUT and WIRE LIST

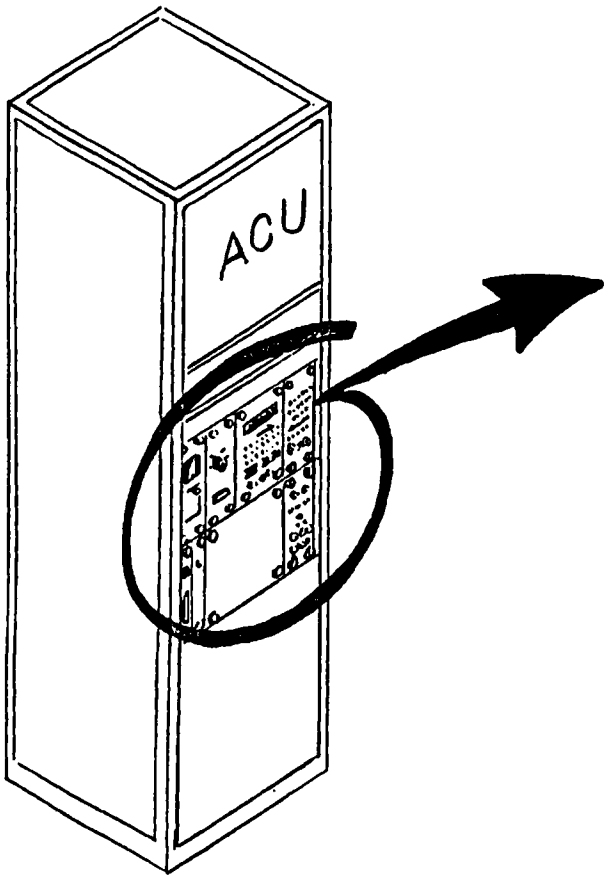
DWG NO. A13740W10 SHEET 1 OF 50

FOCUS-ROTATION RACK-"C" (F/R SYSTEM MODEL "D")



SHT. A-1


ANGLE DATA CONVERTER
ACU
I/O CONNECTOR PANEL
SEE SHT. A-5
F/R BIN "W"
BIN ASSY D13050M08
SEE SHT. A-3, A-4
F/R BIN "X"
BIN ASSY D13050M08
SEE SHT. A-3, A-4
BIN FAN ASSY & MTG. BRACKET
VLA-SK-26B
SEE SHT. A-5
BIN-TO-BIN INTERCONNECT
CONN. PLATE B13050M59
W-BJ2
W-BJ1
X-BJ2
X-BJ1



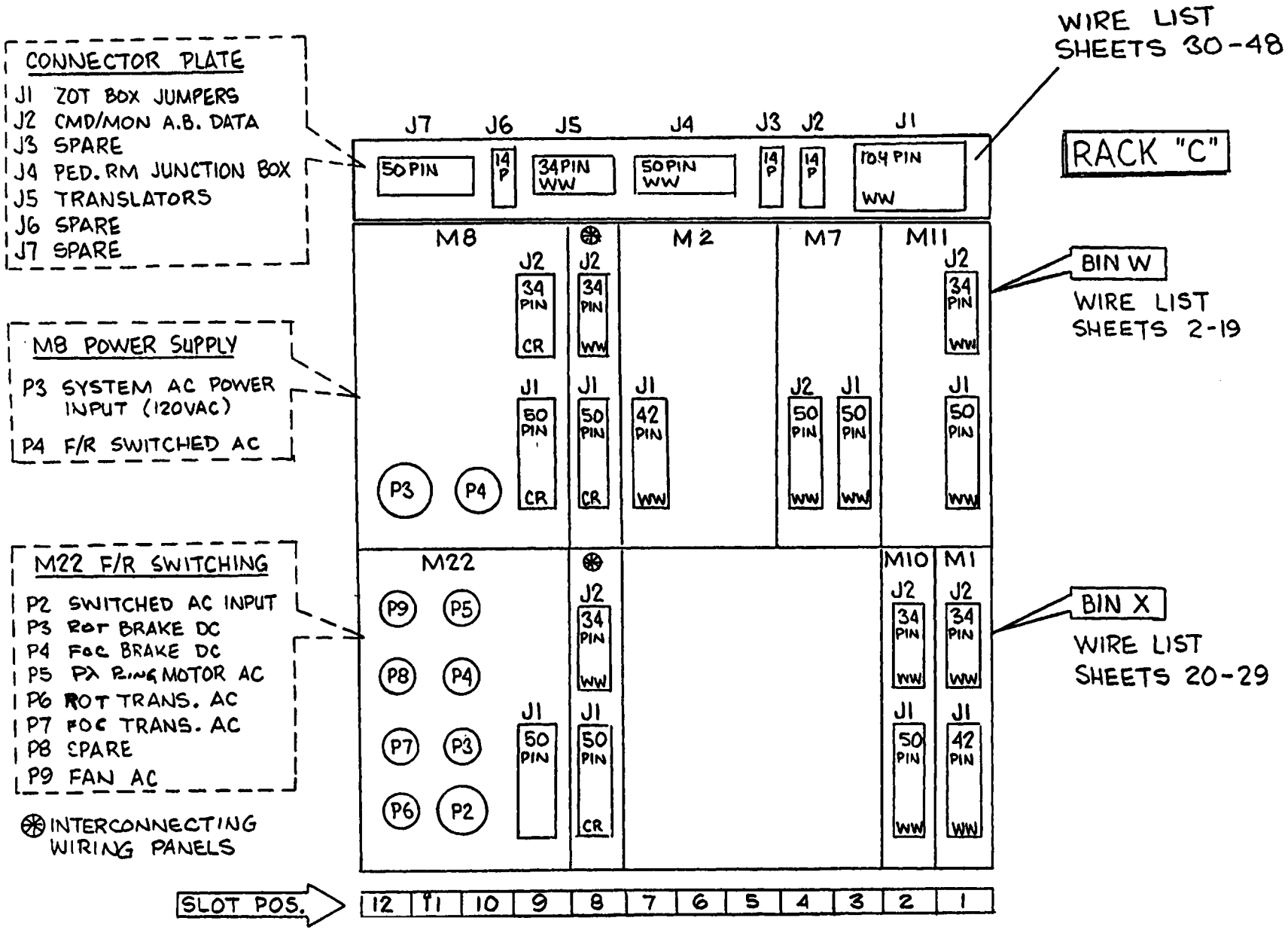
APEX INTER-FACE	F/R CONTROL	DATA TAP	F/R POWER SUPPLY
(2 WIDE)	(2W)	(4W)	(4W)
M11B	M7E	M2B	M8C

DATA SET (3)	CMD/MON INTER-FACE	BLANK	F/R SWITCHING
(1W)	(1W)		(4W)
M1			M22A

F/R ELECTRONIC BINS
(FRONT VIEW)

MODULE LOCATIONS & GENERAL ARRANGEMENT

SHT. A-3

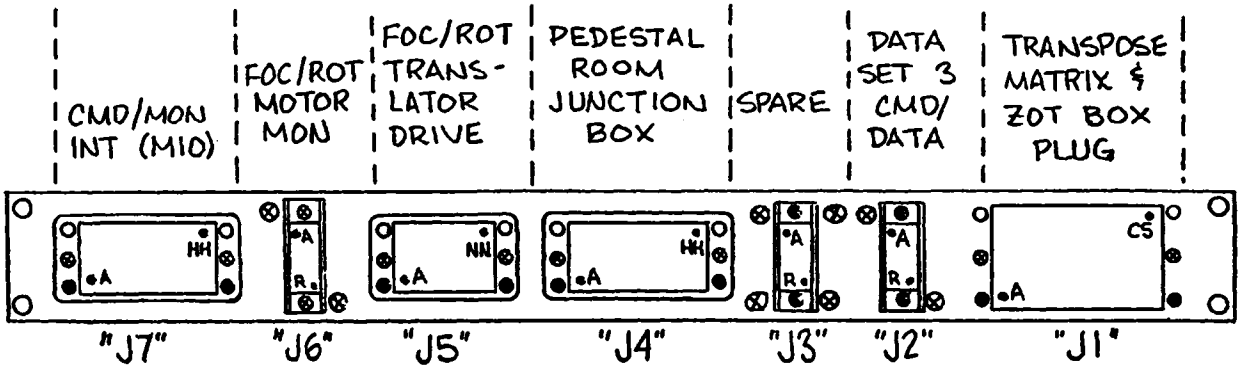


F/R ELECTRONIC BINS

(REAR VIEW)

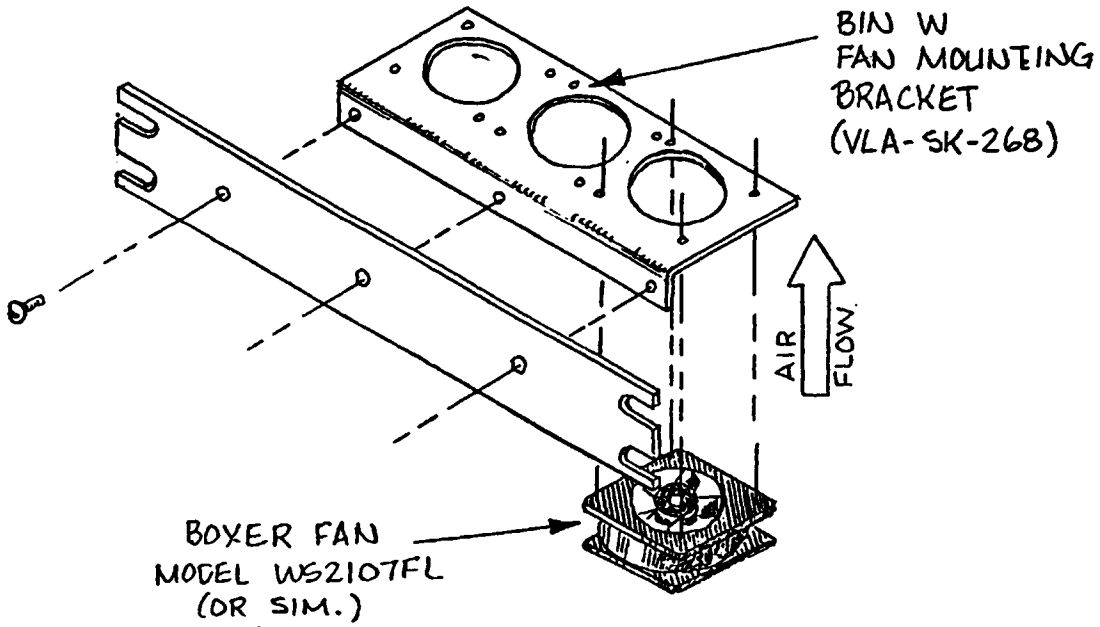
SHT. A-4

I/O CONNECTOR PANEL



PART	SYM	J1	J2-J3	J4	J5	J6	J7
BLOCK TYPE		104-PIN	14-PIN	50-PIN	34-PIN	SAME AS J2	SAME AS J4
BLOCK P/N		201037-1	201298-3	200277-4	200838-3		
PIN HOOD		NOT USED.	not used	202579-2	201350-2		
GUIDE PINS	○	201046-2	202514-1	200833-4	200833-4		
GUIDE SOCKETS	●	201047-2	202512-1	203964-6	203964-6		
CONTACT SOCKETS		← 66473-9 →					
JACK SCREW (MALE)	⊗	← 200871-2 →					

BIN VENTILATION FANS



SHT. A-5

WIRE LIST

RACK: C	BIN: W	SLOT: 1-J1	MODULE: M11, Apex Int	TYPE: 50 Pin
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 200277-4		CONNECTOR PAGE: 1		

PIN	FUNCTION	TYPE	FROM	TO
A	Apex Int +15 V	Red, #20	W-9J1-A	
B	Apex Int 5V Comm	Black, #16	W-9J1-F	
C	Apex Int +5 V	Orange, #16	W-9J1-B	
D	Spare			
E	Apex Int -15 V	Yellow, #20	W-9J1-E	
F	Foc S1		I/O-J1-BL	
H	Rot S1		I/O-J1-BP	
J	Foc S2		I/O-J1-BM	
K	Rot S2		I/O-J1-BV	
L	Foc S3		I/O-J1-BN	
M	Rot S3		I/O-J1-BW	
N	Synchro Exc R1	wh, #26, TP#12		W-8J2-S
P				
R	Synchro Exc R2	Blk, #26, TP#12		W-8J2-U
S				
T	Foc Upper Lim Sense			I/O-J1-Z
U	Rot CW Lim Sense			I/O-J1-AC
V	Foc Lower Lim Sense			I/O-J1-AA
W	Rot CCW Lim Sense			I/O-J1-AM
X	Pin In Sense			I/O-J1-AL
Y				
Z	Pin Out Sense			I/O-J1-AK
a				
b	Pλ Sense			I/O-J1-AJ
c	Lλ Sense			I/O-J1-AW
d	Cλ Sense			I/O-J1-AV
e	KUλ Sense			I/O-J1-AU
f	kλ Sense			I/O-J1-AT
h	Xλ Sense			I/O-J1-BE
j	Yλ Sense			I/O-J1-BD

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: JUN 83
TITLE: F/R SYSTEM D		REV:
DWG NO. A13740W10		SHEET 2 OF 50

WIRE LIST

RACK: C	BIN: W	SLOT: 1-J1	MODULE: M11, Apex Int	TYPE: 50 Pin
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 200277-4		CONNECTOR PAGE: 2		

PIN	FUNCTION	TYPE	FROM	TO
k	Z λ Sense			I/O -J1- BC
m	Apex Sense SW Gnd			I/O - J1 - BB
n	Foc Brake Volts +		I/O -J1-CK	W-8J1- H
p	Rot Brake Volts +		I/O - J1 -CL	W - 8J1 - E
r	Foc Brake Amps			W - 8J1 - J
s	Rot Brake Amps			W - 8J1 - r
t	Foc Brake Ret -		I/O -J1 - CP	W - 8J1 - k
u	Rot Brake Ret -		I/O - J1 - C R	W - 8J1 - 3
v				
w	F/R Mount Temp Sig +			I/O - J1 - BX
x				
y	F/R Mount Temp Ret -			I/O - J1 - BY
z				
AA				
BB				
CC				
DD				
EE				
FF				
HH	Apex Int Ana Comm	Black, # 16	W - 9J1 - C	

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: F/R SYSTEM D		REV:
DWG NO A13740W10		SHEET: 3 OF 50

WIRE LIST

RACK: C	BIN: W	SLOT: 1 – J2	MODULE: M11, Apex Int	TYPE: 34 Pin
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 200838-3		CONNECTOR PAGE: 1		

PIN	FUNCTION	TYPE	FROM	TO
A	Foc Data Req – Sig	Wh, #26 TP#1	W-3J1-u	
B	Rot Data Req – Sig	Wh, #26 TP#2	W-3J1-v	
C	Foc Data Req – Ret	Blk, #26, TP#1	W-3J1-w	
D	Rot Data Req – Ret	Blk #26, TP#2	W-3J1-x	
E	Foc AI Clk – Sig	Wh #26, TP#3	W-3J1-j	
F	Rot AI Clk – Sig	Wh #26, TP#4	W-3J1-p	
H	Foc AI Clk – Ret	Blk #26, TP#3	W-3J1-m	
J	Rot AI Clk – Ret	Blk #26, TP#4	W-3J1-q	
K	Foc AI Data – Sig	Wh #26, TP#5	W-3J1-h	
L	Rot AI Data – Sig	Wh #26, TP#6	W-3J1-n	
M	Foc AI Data – Ret	Blk #26, TP#5	W-3J1-k	
N	Rot AI Data – Ret	Blk #26, TP#6	W-3J1-r	
P				
R				
S				
T				
U	Foc Upper Lim Inh			W-3J1-a
V	Rot CW Lim Inh			W-3J1-c
W	Foc Lower Lim Inh			W-3J1-b
X	Rot CCW Lim Inh			W-3J1-d
Y	Yow Pl Inh – Sig			W-3J1-f
Z				
AA	Limit Inh – Ret			W-3J1-e
BB				
CC				
DD				
EE				
FF				
HH				
JJ				

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun83
TITLE: F/R SYSTEM D		REV:
	DWG NO A/3740W10	SHEET 4 OF 50

WIRE LIST

RACK: C	BIN: W	SLOT: 1-J2	MODULE: M11, APEX INT	TYPE: 34 Pin
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 200838-3		CONNECTOR PAGE: 2		

PIN	FUNCTION	TYPE	FROM	TO
KK				
LL				
MM				
NN				

NATIONAL RADIO ASTRONOMY OBSERVATORY		PROJ:	DATE: Jun 83
TITLE: F/R SYSTEM D			REV:
	DWG NO A13740W10		SHEET 5 OF 50

WIRE LIST

RACK: C	BIN: W1	SLOT: 3 – J1	MODULE: M7., F/R CONT	TYPE: 50 PIN
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 200 277-41		CONNECTOR PAGE: 1		

PIN	FUNCTION	TYPE	FROM	TO
A	+15V	RED, # 20	W-9J1-f	
B	GND	BLACK, # 16	W-9J1-W	
C	+5V	ORANGE, # 16	W-9J1-L	
D	Spare			
E	-15V	YELLOW # 20	W-9J1-AA	
F	Foc Motor control rtn			W-9J2-K
H	SMA-Ø ("1")		W-8J2-H	
J	SMA-1 ("2")		W-8J2-J	
K	SMA-2 ("4")		W-8J2-K	
L	SMA-3 ("8")		W-8J2-L	
M	DIGI-1 Sig			W-8J2-AA
N	CLKI-1 Sig	Wh, # 26, TP# 17	W-8J2-LL	
P	DIGO-Ø Sig		W-8J2-CC	
R	CLKI-1 Ret	BLK, # 26, TP # 17	W-8J2-NN	
S	STRI-1 Sig	Wh, # 26, TP # 18	W-8J2-EE	
T	CLKO-Ø Sig	Wh, # 26, TP # 19	W-8J2-FF	
U	STRI-1 Ret	BLK, # 26, TP # 18	W-8J2-HH	
V	CLKO-Ø Ret	BLK, # 26, TP # 19	W-8J2-JJ	
W	STRO-Ø Sig	Wh, # 26, TP # 20	W-8J2-DD	
X	5Mhz To DATA SET – Sig	Wh, # 26, TP # 27		W-8J2-M
Y	STRO-Ø Ret	BLK, # 26, TP # 20	W-8J2-BB	
Z	5Mhz To DATA SET – Ret	BLK, # 26, TP # 27		W-8J2-N
a	Foc upper Lim Inh		W-1J2-U	
b	Foc Lower Lim Inh		W-1J2-W	
c	Rot CW Lim Inh		W-1J2-V	
d	Rot CCW Lim Inh		W-1J2-X	
e	Limit Inh – Ret		W-1J2-AA	
f	YOWP! Inh		W-1J2-Y	
h	Foc AI DATA – Sig	Wh, # 26, TP # 5	W-1J2-K	
j	Foc AI Clock – Sig	Wh, # 26, TP # 3	W-1J2-E	

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: F/R SYSTEM D		REV:
	DWG NO. A13740W10	SHEET 6 OF 50

WIRE LIST

RACK: C	BIN: W	SLOT: 3 – J1	MODULE: M7, F/R CONT	TYPE: 50 PIN
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 200277-4		CONNECTOR PAGE: 2		

PIN	FUNCTION	TYPE	FROM	TO
b	FOC AI DATA – RET	BLACK, #26, TP#5	W-1J2-M	
m	FOC AI CLOCK – RET	BLACK, #26, TP#3	W-1J2-H	
n	ROT AI DATA – SIG	Wh, #26, TP#6	W-1J2-L	
p	ROT AI CLOCK – SIG	Wh, #26, TP#4	W-1J2-F	
r	ROT AI DATA – RET	BLK, #26, TP#6	W-1J2-N	
s	ROT AI CLOCK – RET	BLK, #26, TP#4	W-1J2-J	
t	CONN INTLK SENSE			I/O-J5-A
u	FOC DATA REQ – SIG	Wh, #26, TP#1		W-1J2-A
v	ROT DATA REQ – SIG	Wh, #26, TP#2		W-1J2-B
w	FOC DATA REQ – RET	BLK, #26, TP#1		W-1J2-C
x	ROT DATA REQ – RET	BLK, #26, TP#2		W-1J2-D
y	ALGI-Ø SIG/HI	Wh, #26, TP#16		W-8J2-KK
z	ROT BRAKE SSR DRIVE			I/O-J1-CM
AA	ALGI-C SIG/LO	BLK, #26, TP#16		W-8J2-MM
BB	ANTA-16 *			
CC	ANTA-8			
DD	ANTA-4			
EE	ANTA-2			
FF	ANTA-1			
HH	ANALOG (IIS) COMMON	BLACK #20	W-9J1-A	
	* TIE THESE POINTS			
	TO GND AS REQUIRED			
	FOR A SPECIFIC ANT			
	3AR # GND = "0",			
	FLOATING = "1"			

NATIONAL RADIO ASTRONOMY OBSERVATORY		PROJ:	DATE: Jun 83
TITLE: F/R SYSTEM D			REV:
	DWG NO A13740W10		SHEET 7 OF 50

WIRE LIST

RACK: C	BIN: W	SLOT: 4-J2	MODULE: M7, F/R Cont	TYPE: 50 Pin
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 200277-4		CONNECTOR PAGE: 1		

PIN	FUNCTION	TYPE	FROM	TO
A	Foc Cmd LCD Dev			W-9J2-E
B	Foc Brk " "			W-9J2-C
C	Foc Upper Lim " "			W-9J2-A
D	Foc Lower Lim " "			W-9J2-F
E	Foc Trans Pwr " "			W-9J2-D
F	Ring Extend " "			W-9J2-X
H	Foc Pulses Up " "			W-9J2-B
J	Foc Pulses Dwn " "			W-9J2-H
K	Rot Cmd " "			W-9J2-S
L	Rot Brk (P.O. out) " "			W-9J2-P
M	Ring Retract " "			W-9J2-V
N	Rot CW Lim " "			W-9J2-M
P	Rot CCW Lim " "			W-9J2-T
R	Rot Trans Pwr " "			W-9J2-R
S	Rot Motor Pulses " "			W-9J2-W
T	Rot Pulses CW " "			W-9J2-N
U	Rot Pulses CCW " "			W-9J2-U
V	P λ " "			W-9J2-Y
W	L λ " "			W-9J2-Z
X	C λ " "			W-9J2-AA
Y	U λ " "			W-9J2-BB
Z	K λ " "			W-9J2-CC
a	X λ " "			W-9J2-DD
b	Y λ " "			W-9J2-EE
c	Z λ " "			W-9J2-FF
d	Foc Trans Pulse Up	Wh, #26, TP#34		I/O-J1-P
e	Foc Trans Pulse Dwn	Wh, #26, TP#35		I/O-J1-R
f	Foc Trans Pulse Ret	Blk, #26, TP#34 TP#35		I/O-J1-c
h	Foc Trans SSR Dev			I/O-J1-A
j	Foc Brake SSR Dev			I/O-J1-n

NATIONAL RADIO ASTRONOMY OBSERVATORY		PROJ:	DATE: Jun 83
TITLE: F/R SYSTEM D			REV:
	DWG NO A13740W10		SHEET 8 OF 50

WIRE LIST

RACK: C	BIN: W	SLOT: 4-J2	MODULE: M7, F/R CONT	TYPE: 50 PIN
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 200277-4		CONNECTOR PAGE: 2		

PIN	FUNCTION	TYPE	FROM	TO
k	ROT TRANS PULSE CW	WH, #26, TP#36		I/O-J1-S
m	ROT TRANS PULSE CCW	WH, #26, TP#37		I/O-J1-T
n	ROT TRANS PULSE RET	BLK, #26, TP#36, TP#37		I/O-J1-d
p	ROT TRANS SSR DRV			I/O-J1-x
r	RING EXTEND SSR DRV			I/O-J1-k
s	RING RETRACT SSR DRV			I/O-J1-y
t	FOC TRANS MON		I/O-J5-AA	
u	ROT TRANS MON		I/O-J5-H	
v	FOC RAMP SW		W-9J2-KK	
w	FOC DRV UP SW		W-9J2-HH	
x	FOC DRV DWN SW		W-9J2-JJ	
y	ROT RAMP SW		W-9J2-MM	
z	ROT DRV CW SW		W-9J2-LL	
AA	ROT DRV CCW SW		W-9J2-NN	
BB	ROT BAND SW A_0		W-9J1-K	
CC	ROT " " A_1		W-9J1-J	
DD	ROT " " A_2		W-9J1-H	
EE	λ SWITCH ACTIVE		W-9J1-D	
FF	SYNCHRO MON - HI	WH #26, TP #41	W-8J1-m	
HH	SYNCHRO MON - LO	BLK #26, TP #41	W-8J1-r	

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: F/R SYSTEM 1		REV:
	DWG NO 4137401W10	SHEET 9 OF 50

WIRE LIST

RACK: C	BIN: W	SLOT: 7-J1	MODULE: M2, DATA TAP	TYPE: 42 P.N
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 202516-3		CONNECTOR PAGE: 1		

PIN	FUNCTION	TYPE	FROM	TO
1	Clock Cont Jmpr	Black, #22	W-7J1-2	
2	Clock Cont Jmpr	Black, #22		W-7J1-1
3				
4				
5C				
5SH				
6C				
6SH				
7C				
7SH				
8				
9				
10	+5V Logic Pwr	Orange, #16	W-9J1-M	
11				
12				
13				
14				
15				
16	+15V	Red, #22	W-9J1-h	
17	-15V	Yellow, #22	W-9J1-BB	
18				
19				
20				
21				
22				
23				
24				
25				
26	CMD/DATA To DT - Sig	Wh, #26, TP#30	W-8J1-A	
27	CMD/DATA To DT - Ret	Blk, #26, TP#30	W-8J1-C	

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: F/P SYSTEM D		REV:
	DWG NO A13740W10	SHEET 10 OF 50

WIRE LIST

RACK: C	BIN: W	SLOT: 7 - J1	MODULE: M2, DATA TAP	TYPE: 42 AWG
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 202516 - 3		CONNECTOR PAGE: 2		

PIN	FUNCTION	TYPE	FROM	TO
28				
29				
30				
31				
32				
33				
34	Logic Common	BLACK #16	W-9J1-X	
35				
36				
37				
38C				
38SH				
39C				
39SH				
40C				
40SH				
41				
42				

NATICNAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: FIR SYSTEM D		REV:
	DWG NO A13740W10	SHEET 11 OF 50

WIRE LIST

RACK: C	BIN: W	SLOT: 8 – J1	MODULE: BIN/BW Jmpr	TYPE: 50 PIN
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 200 277-41		CONNECTOR PAGE: 1		

PIN	FUNCTION	TYPE	FROM	TO
A	CMD/DATA TO DT - SIG	WH, #26, TP #30		W-7J1-26
B	CMD INPUT - SIG	WH, #26, TP #38	I/O-J2-F	
C	CMD/DATA TO DT_RET	BLK, #26, TP #30		W-7J1-27
D	CMD INPUT - RET	BLK, #26, TP #38	I/O-J2-D	
E	CONN INTLK		I/O-J1-CS	
F	DATA SET DATA TO BUFFER - SIG	WH, #26, TP #39		I/O-J2-J
H	FOC BRAKE VOLTS +			W-1J1-m
J	FOC BRAKE AMPS			W-1J1-r
K	FOC BRAKE VOLTS COMM			W-1J1-t
L	DATA SET DATA TO BUFFER - RET	BLK, #26, TP #39		I/O-J2-M
M				
N	+5V (FOR M1)	ORANGE, #16	W-9J1-N	
P	+5V (FOR M10)	ORANGE, #16	W-9J1-P	
R				
S				
T				
U	[illegible] #2 SIG	WH #26 TP #43	I/O-J5-B	
V	[illegible] #1 SIG	WH #26 TP #42	I/O-J6-A	
W	[illegible] #2 RET	BLK #26 TP #43	I/O-J6-E	
X	[illegible] RET	BLK #26 TP #42	I/O-J5-C	
Y	LOGIC COMMON (FOR M1)	BLACK #16	W-9J1-Y	
Z	LOGIC COMMON (FOR M10)	BLACK #16	W-9J1-Z	
a				
b				
c				
d				
e	ROT BRAKE VOLTS +			W-1J1-p
f				
h				
j	+15V (FOR M1)	RED, #20	W-9J1-j	

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: F/O SYSTEM D		REV:
	DWG NO A13740W10	SHEET 12 OF 50

WIRE LIST

RACK: C	BIN: W	SLOT: 8 – J1	MODULE: BIN/BIN JMPR	TYPE: 50 P.W
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 200277-4		CONNECTOR PAGE: 2		

PIN	FUNCTION	TYPE	FROM	TO
k	+15 V (FOR M10)	RED, # 20	W-9J1-k	
m	SYNCHRO MON – HI	WH, #26, TP #41		W-4J2-FF
n				
p	SYNCHRO MON – LO	BLK, #26, TP #41		W-4J2-HH
r	ROT BRAKE AMPS			W-1J1-r
s				
t	ANALOG (±15) COMMON (FOR M1)	BLACK # 20	W-9J1-t	
u	ANALOG (±15) COMMON (FOR M10)	BLACK # 20	W-9J1-u	
v				
w				
x				
y				
z	ROT BRAKE VOLTS RET –			W-1J1-u
AA				
BB				
CC	–15V (FOR M1)	YELLOW # 20	W-9J-CC	
DD	–15V (FOR M10)	YELLOW # 20	W-9J1-DD	
EE				
FF				
HH				

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: F/R SYSTEM D		REV:
	DWG NO A13740W10	SHEET 13 OF 50

WIRE LIST

RACK: C	BIN: W	SLOT: 8-J2	MODULE: BIN/BIN JMPR	TYPE: 34 PIN
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 200838-3		CONNECTOR PAGE: 1		

PIN	FUNCTION	TYPE	FROM	TO
A	+5 V, SSR +SOURCE	ORANGE #20	I/O-J1-f	
B	FOC BRAKE SSR DRV		I/O-J1-m	
C	FOC TRANS SSR DRV		I/O-J1-n	
D	RING EXTEND SSR DRV		I/O-J1-g	
E	RING RETRACT SSR DRV		I/O-J1-u	
F	ROT TRANS SSR DRV		I/O-J1-t	
H	$\overline{\text{SMA-0}}$ ("1")			W-3J1-H
J	$\overline{\text{SMA-1}}$ ("2")			W-3J1-J
K	$\overline{\text{SMA-2}}$ ("4")			W-3J1-K
L	$\overline{\text{SMA-3}}$ ("8")			W-3J1-L
M	5MHz SIG	WH, #26, TP#27		W-3J1-X
N	5MHz RET	BLK, #26, TP#27		W-3J1-Z
P	ROT BRAKE SSR DRIVE		I/O-J1-CH	
R	CONN INTLK			W-3J1-FRAME GND
S	SYNCHRO EXC R1	WH, #26, TP#12		W-1J1-N
T	SYNCHRO EXC R1	WH #26, TP#13		I/O-J4-A
U	SYNCHRO EXC R2	BLK #26, TP#12		W-1J1-R
V	SYNCHRO EXC R2	BLK #26, TP#13		I/O-J4-C
W	SYNCHRO EXC R1	WH, #26, TP#14		
X	SYNCHRO EXC R1			
Y	SYNCHRO EXC R2	BLK #26, TP#14		
Z	SYNCHRO EXC R2			
AA	DIGI-1 SIG		W-3J1-M	
DD	STRO-0 SIG	WH, #26, TP#20		W-3J1-W
CC	DIGO-0 SIG			W-3J1-P
BB	STRO-0 RET	BLK, #26, TP#20		W-3J1-Y
EE	STRI-1 SIG	WH, #26, TP#18		W-3J1-S
FF	CLKO-0 SIG	WH, #26, TP#19		W-3J1-T
HH	STRI-1 RET	BLK, #26, TP#18		W-3J1-U
JJ	CLKO-0 RET	BLK, #26, TP#19		W-3J1-V

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: F/R SYSTEM D		REV:
	DWG NO A13740W10	SHEET 14 OF 50

WIRE LIST

RACK: C	BIN: W	SLOT: 8-J2	MODULE: BIN/BIN JMPR	TYPE: 34 P.N
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 2-0 83[illegible]-3		CONNECTOR PAGE: 2		

PIN	FUNCTION	TYPE	FROM	TO
KK	ALGI-Ø SIG/HI	WH, #26, TP #16		W-3J1-Z
LL	CLKI-1 - SIG	WH, #26, TP #17		W-3J1-N
MM	ALGI-Ø RET/LO	BLK, #26, TP #16		W-3J1-AA
NN	CLKI-1 - RET	BLK #26, TP #17		W-3J1-R

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: F/R SYSTEM D		REV:
	DWG NO A13740W10	SHEET 15 OF 50

WIRE LIST

RACK: C	BIN: W	SLOT: 9 – J1	MODULE: M8, F/R PWR	TYPE: 50 PIN
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 200277-4		CONNECTOR PAGE: 1		

PIN	FUNCTION	TYPE	FROM	TO
A	APEX INT +15V	RED, #20		W-1J1-A
B	APEX INT +5V	ORANGE #16		W-1J1-C
C	APEX INT ANA COMM	BLACK #16		W-1J1-HH
D	λ SWITCH ACTIVE			W-4J2-EE
E	APEX INT -15V	YELLOW, #20		W-1J1-E
F	APEX INT 5V COMM	BLACK #16		W-1J1-B
H	PIN SW A_2			W-4J2-DD
J	PIN SW A_1			W-4J2-CC
K	PIN SW A_0			W-4J2-BB
L	+5V	ORANGE, #16		W-3J1-C
M	↓	↓ #16		W-7J1-10
N	↓	↓ #16		W-8J1-N
P	↓	↓ #16		W-8J1-P
R	↓ +5V TO SSR's	↓ #20		I/O-J1-Z
S	↓	↓		
T	↓	↓		
U	↓	↓		
V	+5V	ORANGE #16		
W	LOGIC COMMON	BLACK #16		W-3J1-B
X	↓	↓		W-7J1-34
Y	↓	↓		W-8J1-Y
Z	↓	↓		W-8J1-Z
a	↓	↓		
b	↓	↓		
c	↓	↓		
d	LOGIC COMMON	BLACK #16		FRAME GND
e	SPARE			
f	+15V	RED, #20		W-3J1-A
h	↓	↓		W-7J1-16
Z	↓	↓		W-8J1-Z

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: F/R SYSTEM D		REV:
	DWG NO A13740W10	SHEET: 16 OF 50

WIRE LIST

RACK: C	BIN: W	SLOT: 9-J1	MODULE: MB, FIR PWR	TYPE: 50 PIN
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 200277-4		CONNECTOR PAGE: 2		

PIN	FUNCTION	TYPE	FROM	TO
k	+15 V	Red # 20		W-8J1-k
m	↓	↓		
n	↓	↓		
p	+15V	Red # 20		
r	Spare			
s	Analog (±15) Common	Black, # 20		W-3J1-HH
t		↓		W-8J1-t
u		↓		W-8J1-u
v		↓		
w		↓		
x		↓		
y	Analog (±15) Common	Black, # 20		
z	Spare			
AA	-15 V	Yellow, # 20		W-3J1-E
BB	↓	↓		W-7J1-17
CC	↓	↓		W-8J1-CC
DD	↓	↓		W-8J1-DD
EE	↓	↓		
FF	↓	↓		
HH	-15V	Yellow, # 20		

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: FIR SYSTEM ①		REV:
	DWG NO A13740W10	SHEET 17 OF 50

WIRE LIST

RACK: C	BIN: W	SLOT: 9 – J2	MODULE: M&B, F/R PWR	TYPE: 34 PIN
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 200838-3		CONNECTOR PAGE: 1		

PIN	FUNCTION	TYPE	FROM	TO
A	FOC UPPER LIM LED DRV		W-4J2-C	
B	FOC PULSES UP "		W-4J2-H	
C	FOC BRK "		W-4J2-B	
D	FOC TRANS PWR "		W-4J2-E	
E	FOC CMD "		W-4J2-A	
F	FOC LOWER LIM "		W-4J2-D	
H	FOC PULSES DWN "		W-4J2-J	
J	FOC SPARE LED "			
K	FOC MOT PULSES "		W-4J2-F	
L	FOC SPARE LED "			
M	ROT CW LIM "		W-4J2-N	
N	ROT PULSES CW "		W-4J2-T	
P	ROT BRAKE "		W-4J2-L	
R	ROT TRANS PWR "		W-4J2-R	
S	ROT CMD "		W-4J2-K	
T	ROT CCW LIM "		W-4J2-P	
U	ROT PULSES CCW "		W-4J2-U	
V	ROT PIN IN "		W-4J2-M	
W	ROT MOT PULSES "		W-4J2-S	
X	ROT SPARE "			
Y	PA "			W-4J2-V
Z	LA "			W-4J2-W
AA	CA "			W-4J2-X
BB	UA "			W-4J2-Y
CC	KA "			W-4J2-Z
DD	XA "			W-4J2-a
EE	YA "			W-4J2-b
FF	ZA "			W-4J2-c
HH	FOC DRV UP SW			W-4J2-w
JJ	FOC DRV DWN SW			W-4J2-x

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: F/R SYSTEM D		REV:
	DWG NO A13740W10	SHEET 18 OF 50

WIRE LIST

RACK: C	BIN: W	SLOT: 9-J2	MODULE: MB, F/R PWR	TYPE: 34 P.W
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 200838-3		CONNECTOR PAGE: 2		

PIN	FUNCTION	TYPE	FROM	TO
KK	Foc Ramp SW			W-4J2-V
LL	Rot DRV CW SW			W-4J2-Z
MM	Rot Ramp SW			W-4J2-Y
NN	Rot DRV CCW SW			W-4J2-AA

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: F/R SYSTEM D		REV:
	DWG NO A13740W10	SHEET 19 OF 50

WIRE LIST

RACK: C	BIN: X	SLOT: 1—J1	MODULE: M1, DATA SET	TYPE: 42 P.W
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 202516-3		CONNECTOR PAGE: 1		

PIN	FUNCTION	TYPE	FROM	TO
1				
2				
3				
4	DIGI-2 — RET		X-1J1-11 X-1J1-28	
5C				
5SH				
6C				
6SH				
7C	Antenna #1 SIG	wh #26, TP #43	X-8J1-U	
7SH	Antenna #2 RET	BLK #26, TP #43	X-8J1-W	
8	CMD/DATA TO DT — SIG	Wh, #26, TP #28		X-8J1-A
9	CMD/DATA TO DT — RET	BLK, #26, TP #28		X-8J1-C
10	+5V	ORANGE, #16	X-8J1-N	
11	DSA-Ø ("1")			X-1J1-4
12				
13				
14	ALGI-Ø SIG	wh #26, tp #15	X-8J2-KK	
15	DATA OUTPUT TO BUFFER-HI	wh, #26, TP #29		X-8J1-F
16	+15V	RED, #20	X-8J1-J	
17	-15V	YELLOW, #20	X-8J1-CC	
18				
19				
20				
21				
22				
23				
24				
25	CMD INPUT — SIG	Wh, #26, TP #29	X-8J1-B	
26	CMD INPUT — RET	BLK, #26, TP #29	X-8J1-D	
27	DATA OUTPUT TO BUFFER-RET	BLK, #26, TP #29	X-8J1-L	

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: F/R SYSTEM D		REV:
	DWG NO A13740W10	SHEET 20 OF 50

WIRE LIST

RACK: C	BIN: X	SLOT: 1 - J1	MODULE: M1 - DATA SEL	TYPE: 42 P.J
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 202516 - 3		CONNECTOR PAGE: 2		

PIN	FUNCTION	TYPE	FROM	TO
28	DSA - 1 ("2")			X - 1J1 - 4
29				
30				
31				
32	A : G I - C Ret	BLK #26, Tp #1	X - 8J2 - 10M	
33	[illegible]	blk #24, Tp #42	X - 8J1 - V	
34	Logic Common	BLACK, #16	X - 8J1 - Y	
35				
36				
37				
38C				
38SH				
39C				
39SH				
40C				
40SH				
41	[illegible] : Ret	BLK #24, Tp #42	Y - 8J1 - Y	
42	ANALOG (±15) Common	BLACK #, 16	X - 8J1 - E	

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: F/R SYSTEM D		REV:
	DWG NO 413740W10	SHEET 21 OF 50

WIRE LIST

RACK: C	BIN: X	SLOT:	– J2	MODULE: M1, DATA SET	TYPE: 34 PIN
LIST BY:		WIRE BY:			
CONNECTOR TYPE: 200838-3		CONNECTOR PAGE: 1			

PIN	FUNCTION		TYPE	FROM	TO
A	DIGO – ϕ	RET			
B					
C	DIGO – ϕ	SIG			X – 8J2 – CC
D					
E	CLKO – ϕ	RET	BLK, # 26, TP # 23		X – 8J2 – JJ
F					
H	CLKO – ϕ	SIG	WH, # 26, TP # 23		X – 8J2 – FF
J					
K	STRO – ϕ	RET	BLK, # 26, TP # 21		X – 8J2 – BB
L					
M	STRO – ϕ	SIG	WH, # 26, TP # 21		X – 8J2 – DD
N					
P					
R	DIGI – 1	SIG		X – 8J2 – AA	
S					
T	DIGI – 1	RET			
U					
V	CLKI – 1	SIG	WH, # 26, TP # 24		X – 8J2 – LL
W					
X	CLKI – 1	RET	BLK, # 26, TP # 24		X – 8J2 – NN
Y					
Z	STRI – 1	SIG	WH, # 26, TP # 25		X – 8J2 – EE
AA					
BR	STRI – 1	RET	BLK, # 26, TP # 25		X – 8J2 – HH
CC					
DD	$\overline{\text{SMA – 2}}$	SIG			X – 8J2 – K
EE	$\overline{\text{SMA – 0}}$	SIG			X – 8J2 – H
FF					
HH					
JJ	$\overline{\text{SMA – 3}}$	SIG			X – 8J2 – L

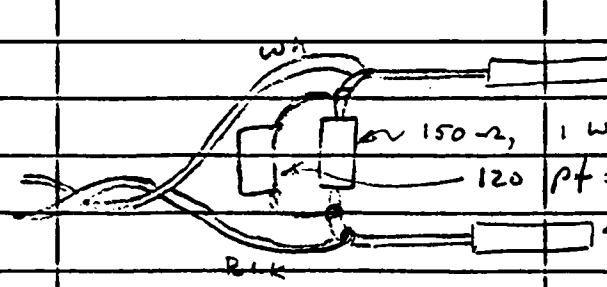
NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: F/R SYSTEM D		REV:
	DWG NO A13740W10	SHEET 22 OF 50

WIRE LIST

RACK: C	BIN: X	SLOT: 1-J2	MODULE: M1, DATA SET	TYPE: 34 PIN
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 200838-2		CONNECTOR PAGE:		

PIN	FUNCTION	TYPE	FROM	TO
KK	$\overline{\text{SMA-1}}$ SIG			X-8J2-J
LL				
MM	5Mhz SIG *	WH, #26, TP #25	X-8J2-M	
NN	5Mhz RET *	BLK, #26, TP #25	X-8J2-N	

* 5Mhz TERMINATION:



NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: F/R SYSTEM D		REV:
	DWG NO A13740W10	SHEET 23 OF 50

WIRE LIST

RACK: C	BIN: X	SLOT: 8 – J1	MODULE: BIN/BIU Jmpr	TYPE: 50 PIN
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 200277-4		CONNECTOR PAGE: 1		

PIN	FUNCTION	TYPE	FROM	TO
A	CMD/DATA TO DT – SIG	WH, #26, TP#28	X – 1J1 – 8	
B	CMD INPUT – SIG	WH, #26, TP#29		X – 1J1 – 25
C	CMD/DATA TO DT – RET	BLK, #26, TP#28	X – 1J1 – 9	
D	CMD INPUT – RET	BLK, #26, TP#29		X – 1J1 – 26
E	CON INTLK			X – 8J2 – R
F	DATA SET DATA TO BUFFER – SIG	WH, #26, TP#40	X – 1J1 – 15	
H	FOC BRAKE VOLTS +		X – 9J1 – N	
J	FOC BRAKE AMPS		X – 9J1 – X	
K	FOC BRAKE VOLTS RET –		X – 9J1 – Y	
L	DATA SET DATA TO BUFFER – RET	BLK, #26, TP#40	X – 1J1 – 27	
M				
N	+5V (FOR M1)	ORANGE #16		X – 1J1 – 10
P	+5V (FOR M10)	ORANGE #16		
R				
S				
T				
U	[illegible] #2 SIG	WH #26, TP#42		X – 1J1 – 7c
V	" #1 SIG	WH #26, TP#42		X – 1J1 – 33
W	" #2 RET	BLK #26, TP#43		X – 1J1 – 7sh
X	" #1 RET	BLK #26, TP#42		X – 1J1 – 41
Y	LOGIC COMMON (FOR M1)	BLACK, #16		X – 1J1 – 34
Z	LOGIC COMMON (FOR M10)	BLACK, #16		
a				
b				
c				
d				
e	ROT BRAKE VOLTS +		X – 9J1 – DD	
f				
h				
j	+15V (FOR M1)	RED, #20		X – 1J1 – 16

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: F/R SYSTEM D		REV:
	DWG NO A13740W10	SHEET 24 OF 50

WIRE LIST

RACK: C	BIN: X	SLOT: 8-J1	MODULE: Bin/Bin Jmpr	TYPE: 50 Pin
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 200277-4		CONNECTOR PAGE: 2		

PIN	FUNCTION	TYPE	FROM	TO
E	+15V (FOR M10)			
m	SYNCHRO MON -HI	WH, #26, TP#40	X-9J1-f	
n				
P	SYNCHRO MON-LO	BLK, #26, TP#40	X-9J1-Z	
R	ROT BRAKE Amps		X-9J1-FF	
A				
t	ANALOG(±15) COMMON (FOR M1)	BLACK, # 20		X-1J1-42
u	ANALOG(±15) COMMON (FOR M10)			
v				
w				
x				
y				
Z	ROT BRAKE VOLTS RET -		X-9J1-HH	
AA				
BB				
CC	-15V (FOR M1)	YELLOW, # 20		X-1J1-17
DD	-15V (FOR M10)			
EE				
FF				
HH				

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: F/R SYSTEM D		REV:
	DWG NO A13740W10	SHEET 25 OF 50

WIRE LIST

RACK: C	BIN: X	SLOT: 8-J2	MODULE: BIN/BIN JMPR	TYPE: 34 P.N
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 200838-2		CONNECTOR PAGE: 1		

PIN	FUNCTION	TYPE	FROM	TO
A	+5V, SSR +SOURCE	ORANGE, #20		X-9J1-A
B	FOC BRAKE SSR DRV			X-9J1-B
C	FOC TRANS SSR DRV			X-9J1-C
D	RING EXTEND SSR DRV			X-9J1-H
E	RING RETRACT SSR DEV			X-9J1-E
F	ROT TRANS SSR DEV			X-9J1-F
H	$\overline{\text{SMA-}\phi}$ ("1")		X-1J2-EE	
J	$\overline{\text{SMA-1}}$ ("2")		X-1J2-KK	
K	$\overline{\text{SMA-2}}$ ("4")		X-1J2-DD	
L	$\overline{\text{SMA-3}}$ ("8")		X-1J2-JJ	
M	5Mhz SIG	WH, #26, TP#26		X-1J2-MM
N	5Mhz RET	BLK, #26, TP#26		X-1J2-NN
P	ROT BRAKE SSR DRIVE			X-9J1-D
R	CONN INTL'K		X-8J1-E	
S	SYNCHRO EXC R_1	WH, #26, TP#8	X-9J1-S	
T	SYNCHRO EXC R_1	WH, #26, TP#9	X-9J1-T	
U	SYNCHRO EXC R_2	BLK, #26, TP#8	X-9J1-U	
V	SYNCHRO EXC R_2	BLK #26 TP#9	X-9J1-V	
W	SYNCHRO EXC R_1	WH, #26, TP#10	X-9J1-W	
X	SYNCHRO EXC R_1	WH #26, TP#11	X-9J1-X	
Y	SYNCHRO EXC R_2	BLK, #26, TP#10	X-9J1-Y	
Z	SYNCHRO EXC R_2	BLK, #26, TP#11	X-9J1-Z	
AA	DIGI-1 SIG			X-1J2-R
DD	STRO-ϕ SIG	WH, #26, TP#21	X-1J2-M	
CC	DIGO-ϕ SIG		X-1J2-C	
BB	STRO-ϕ RET	BLK, #26, TP#21	X-1J2-K	
EE	STRI-1 SIG	WH, #26, TP#22	X-1J2-Z	
FF	CLKO-ϕ SIG	WH, #26, TP#23	X-1J2-H	
HH	STRI-1 RET	BLK, #26, TP#22	X-1J2-BB	
JJ	CLKO-ϕ RET	BLK, #26, TP#23	X-1J2-E	

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun83
TITLE: F/R SYSTEM D		REV:
	DWG NO A13740W10	SHEET: 26 OF 50

WIRE LIST

RACK: C	BIN: X	SLOT: 8-J2	MODULE: Bin/Bin Jmpr	TYPE: 34 Pin
LIST BY: WEBER		WIRE BY:		
CONNECTOR TYPE: 2005126-2		CONNECTOR PAGE: 2		

PIN	FUNCTION	TYPE	FROM	TO
KK	ALGI-Ø SIG/HI	WH, #26, TP #15		X-1J1-40C
LL	CLKI-1 SIG	WH, #26, TP #24	X-1J2-V	
MM	ALGI-Ø RET/LO	BLK, #26, TP #15		X-1J1-40SH
NN	CLKI-1 RET	BLK, #26, TP #24	X-1J2-X	

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: D/R SYSTEM D		REV:
	DWG NO A3740W10	SHEET 27 OF 50

WIRE LIST

RACK: C	BIN: X	SLOT: 9 – J1	MODULE: M22, F/R SWTCH	TYPE: 50 PIN
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 200277-4		CONNECTOR PAGE: 1		

PIN	FUNCTION	TYPE	FROM	TO
A	+5V, SSR + Source		X – 8J2 – A	
B	Foc Brake SSR Drv		X – 8J2 – B	
C	Foc Trans SSR Drv		X – 8J2 – C	
D	Rot Brake SSR Drv		X – 8J2 – P	
E	Ring Retract SSR Drv		X – 8J2 – E	
F	Rot Trans SSR Drv		X – 8J2 – F	
H	Ring Extend SSR Drv		X – 8J2 – D	
J				
k				
L				
M				
N				
P				
R				
S	Synched Exc R1	Wh, #26 TP#8		X – 8J2 – S
T	Synched Exc R1	Wh, #26 TP#9		X – 8J2 – T
U	Synched Exc R2	Blk, #26, TP#8		X – 8J2 – U
V	Synched Exc R2	Blk, #26, TP#9		X – 8J2 – V
W	Synched Exc R1	Wh, #26, TP#10		X – 8J2 – W
X	Synched Exc R1	Wh, #26, TP#11		X – 8J2 – X
Y	Synched Exc R2	Blk, #26, TP#10		X – 8J2 – Y
Z	Synched Exc R2	Blk, #26, TP#11		X – 8J2 – Z
a				
b				
c				
d				
e				
f	Synched Mon – Hi	Wh, #26, TP#40		X – 8J1 – m
h				
j	Synched Mon – Lo	Blk, #26, TP#40		X – 8J1 – P

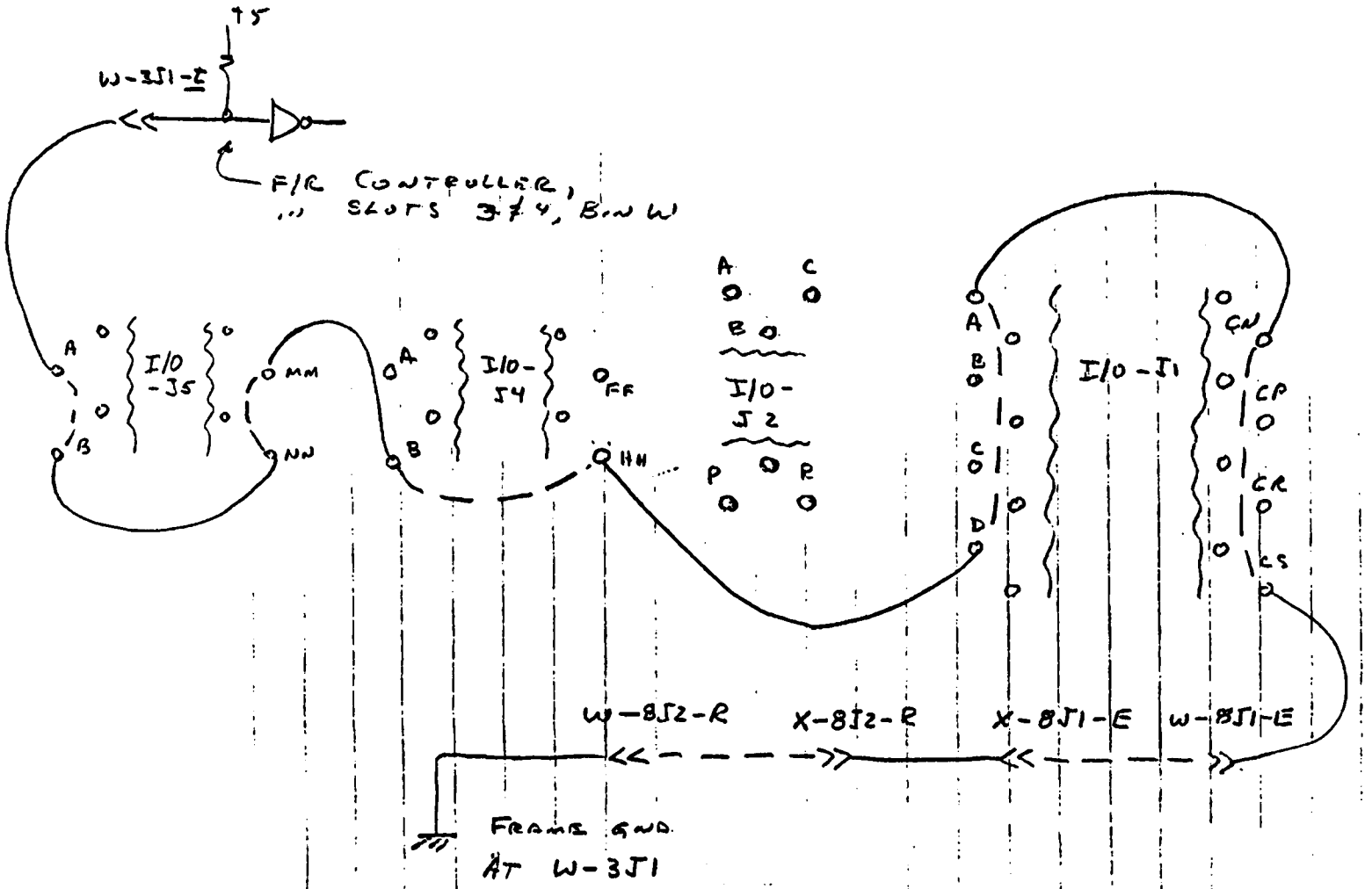
NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: F/R SYSTEM D		REV:
	DWG NO A13740W10	SHEET 28 OF 50

WIRE LIST

RACK: C	BIN: X	SLOT: 9 — J1	MODULE: M22, F/R SWITCH	TYPE: STD P.W.
LIST BY:		WIRE BY:		
CONNECTOR TYPE: 200277-4		CONNECTOR PAGE: 2		

PIN	FUNCTION	TYPE	FROM	TO
k				
m				
n				
p				
r				
s				
t				
u				
v	FOC BRAKE VOLTS +			X-8J1-H
w				
x	FOC BRAKE AMPS			X-8J1-J
y	FOC BRAKE RET -			X-8J1-K
z				
AA				
BB				
CC				
DD	ROT BRAKE VOLTS +			X-8J1-E
EE				
FF	ROT BRAKE AMPS			X-8J1-L
HH	ROT BRAKE RET -			X-8J1-Z

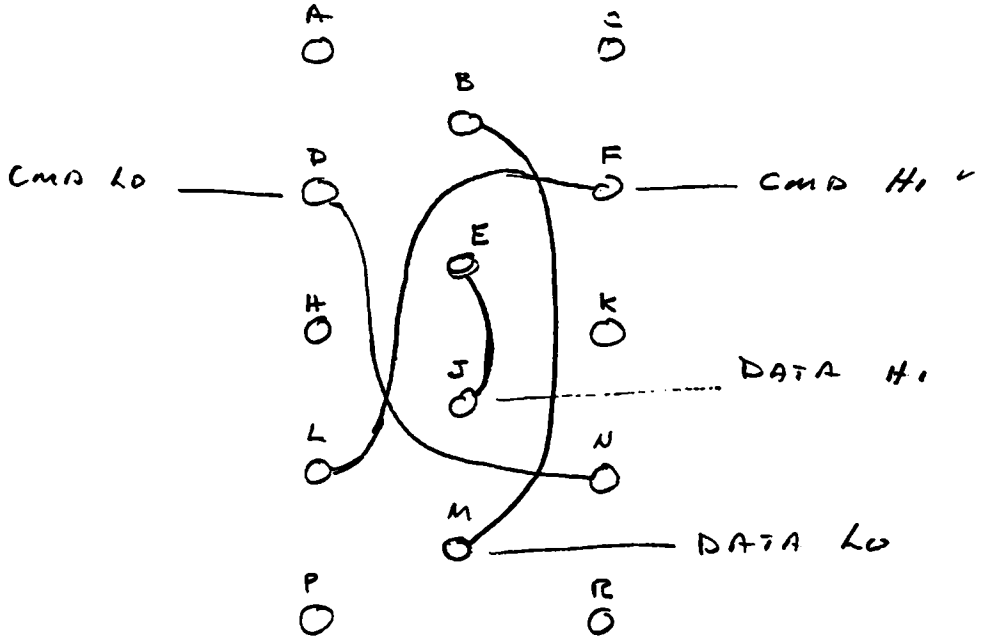
NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: F/R SYSTEM D		REV:
	DWG NO A03740W10	SHEET 29 OF 50



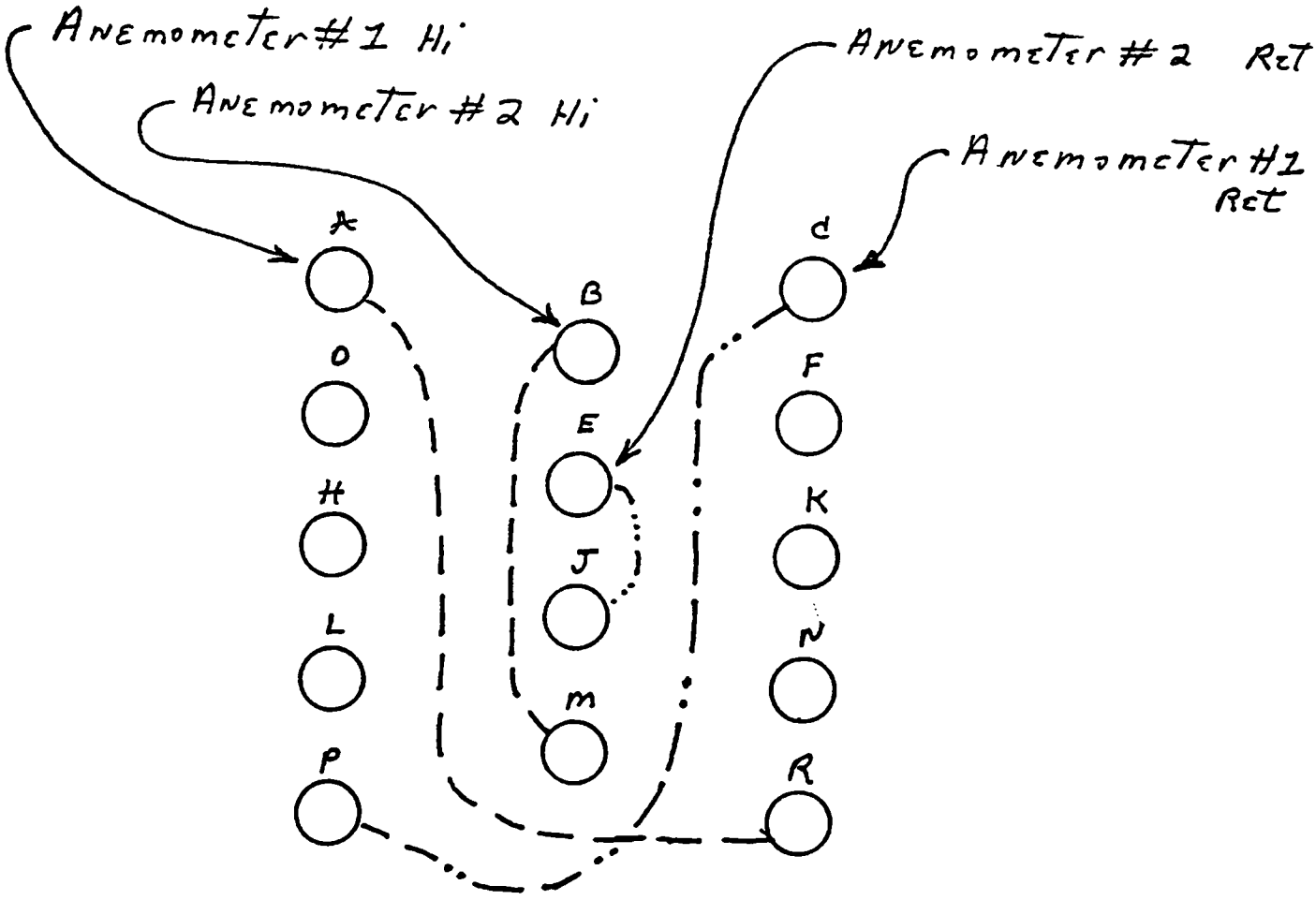
---- ⇒ MATING CABLE PLUG JUMPERS

BIN I/O & BIN TO BIN INTERLOCK CIRCUITS

J2 - CMD/DATA I/O SIGNALS
PANEL BLOCK - 201298-3
14 PIN SOCKETS



J6 Anemometer Inputs signals



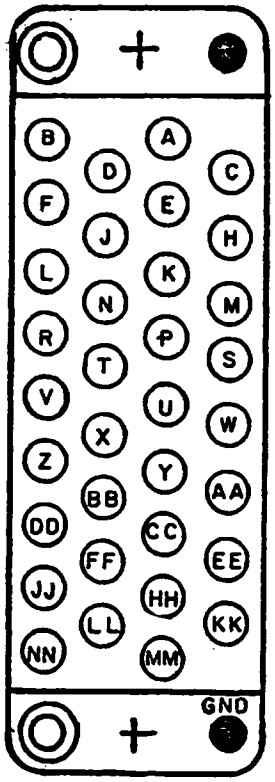
Panel Block – 201298-3
14 pin Socket

note:
a) not tobe put on interlock system

F/R System E A1374ø wiø

Sh. 31A of 5ø

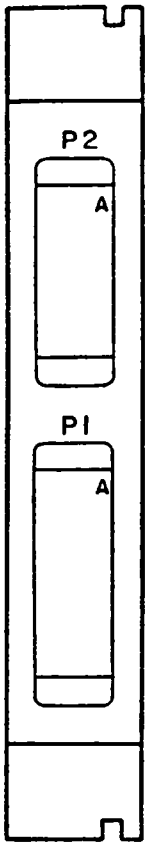
M8C Power Supply I/O
Signal Pin Assignments
Sheet 2
7/20/83/DW



P2 (REAR VIEW)

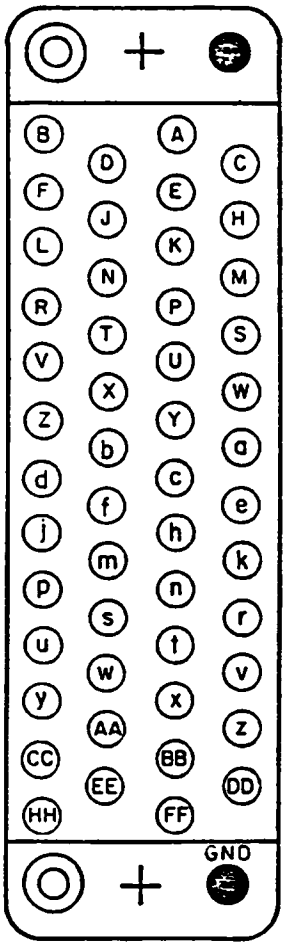
P2

PIN	FUNCTION	WIRE COLOR	PIN	FUNCTION	WIRE COLOR
A	Foc UP Lim LED DRV		V	Rot Pin In LED DRV	
B	Foc DRV UP " "		W	Rot Mot " "	
C	Foc Brake " "		X	Rot Spare " "	
D	Foc Trans " "		Y	P λ LED " "	
E	Foc Cmd " "		Z	L λ " " "	
F	Foc Low Lim " "		AA	C λ " " "	
H	Foc DRV Dwn " "		BB	U λ " " "	
J	Foc Spare " "		CC	K λ " " "	
K	Foc Mot " "		DD	X λ " " "	
L	Foc Spare " "		EE	Y λ " " "	
M	Rot CW Lim " "		FF	Z λ " " "	
N	Rot DRV CW " "		HH	Foc DRV UP SW	
P	Rot Brake " "		JJ	Foc " DWN "	
R	Rot Trans " "		KK	" Ramp "	
S	Rot Cmd " "		LL	Rot DRV CW "	
T	Rot CCW Lim " "		MM	Rot Ramp "	
U	Rot DRV CCW " "		NN	Rot DRV CCW "	



SINGLE WIDE MODULE
(REAR VIEW)

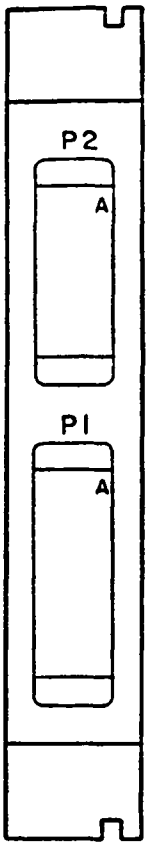
MBC Power Supply
DC & Signal I/O
Pin Assignments
Sheet 1
7/28/83/DW



P1 (REAR VIEW)

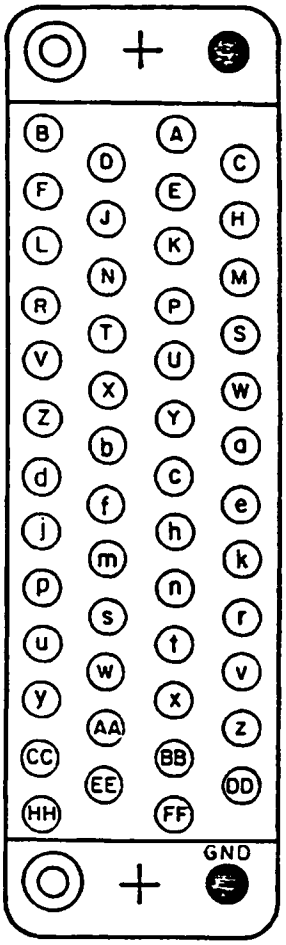
P1					
PIN	FUNCTION	WIRE COLOR	PIN	FUNCTION	WIRE COLOR
A	APEX JNT +15 V	RED	d	Logic Common	BLACK
B	" " +5 V	ORANGE	e	SPARE	
C	AN Comm	BLACK	f	+15 V	RED
D	> Switch Active		h	↓	↓
E	" " −15 V	YELLOW	j		
F	" " 5 V Comm	BLACK	k		
H	Pin Switch A2		m		
J	" " A1		n		
K	" " A0		p	+15 V	RED
L	+5 Volts	ORANGE	r	SPARE	
M			s	Analog (±15) Comm	BLACK
N	↓	↓	t	↓	↓
P			u		
R			v		
S			w		
T			x		
U			y	Analog (±15) Comm	BLACK
V	+5 Volts	ORANGE	z	SPARE	
W	Logic Common	BLACK	AA	−15 V	YELLOW
X			BB		
Y			CC		
Z			DD		
a			EE		
b			FF		
c			HH	−15 V	YELLOW

* INDICATES A FUNCTION NOT FOUND IN THIS MODULE



SINGLE WIDE MODULE
(REAR VIEW)

M11-B, APEX INTERFACE
CONNECTOR P1 PIN
ASSIGNMENTS
7/28/83/DW
SHEET 1

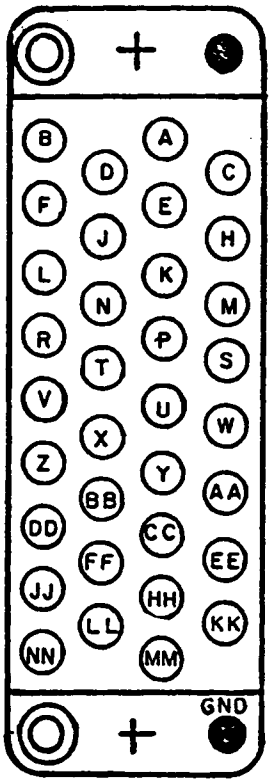


P1 (REAR VIEW)

P1					
PIN	FUNCTION	WIRE COLOR	PIN	FUNCTION	WIRE COLOR
A	+15 VOLTS	RED	d	C λ SENSE SW	
B	LOGIC GND	BLACK	e	U λ SENSE SW	
C	+5 VOLTS	ORANGE	f	K λ SENSE SW	
D			h	X λ SENSE SW	
E	-15 VOLTS	YELLOW	j	Y λ SENSE SW	
F	FOC S1		k	Z λ SENSE SW	
H	ROT S1		m	SENSE SW GND	
J	FOC S2		n	FOC BRAKE VOLTS	
K	ROT S2		p	ROT BRAKE VOLTS	
L	FOC S3		r	FOC BRAKE AMPS	
M	ROT S3		s	ROT BRAKE AMPS	
N	SYNCHRO R1		t	FOC BRAKE COMM	
P			u	ROT BRAKE COMM	
R	SYNCHRO P2		v		
S			w	F/R MOUNT TEMP +	
T	FOC UPPER LIM SENSE		x		
U	ROT CW LIM SENSE		y	F/R MOUNT TEMP -	
V	FOC LOWER LIM SENSE		z		
W	ROT CCW LIM SENSE		AA		
X	PIN IN SENSE SW		BB		
Y			CC		
Z	PIN OUT SENSE SW		DD		
a			EE		
b	P λ SENSE SW		FF		
C	L λ SENSE SW		HH	ANALOG (±15) GND	

* INDICATES A FUNCTION NOT FOUND IN THIS MODULE

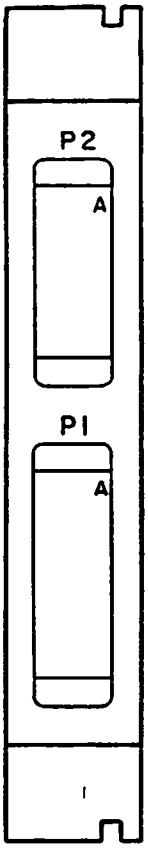
M11-B, Apex Interface
Connector P2 Pin
Assignments, 7/28/83/DW
Sheet 2



P2 (REAR VIEW)

P2

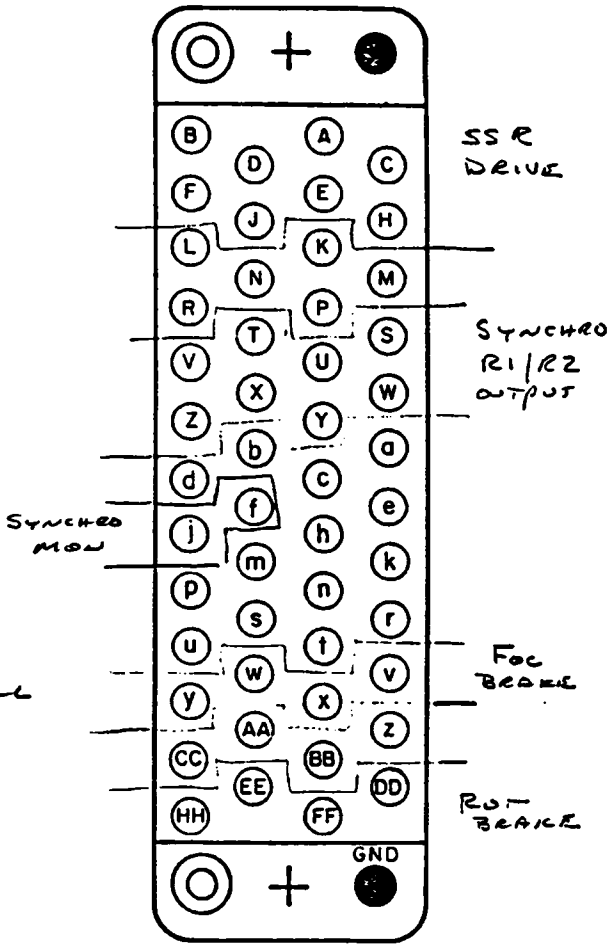
PIN	FUNCTION	WIRE COLOR	PIN	FUNCTION	WIRE COLOR
A	Foc Data Req – Sig		V	Rot CW Lim Inh	
B	Rot Data Req – Sig		W	Foc Lower Lim Inh	
C	Foc Data Req – Ret		X	Rot CCW Lim Inh	
D	Rot Data Req – Ret		Y	YawP! Signal	
E	Foc Load Clock – Sig		Z	YawP! & Inh Ret	
F	Rot Load Clock – Sig		AA		
H	Foc. Load Clock – Ret		BB		
J	Rot Load Clock – Ret		CC		
K	Foc Ser Data – Sig		DD		
L	Rot Ser Data – Sig		EE		
M	Foc Ser Data – Ret		FF		
N	Rot Ser Data – Ret		HH		
P			JJ		
R			KK		
S			LL		
T			MM		
U	Foc Upper Lim Inh		NN		



SINGLE WIDE MODULE
(REAR VIEW)

M22 SIGNAL
I/O PLUG

7/20/83/DW

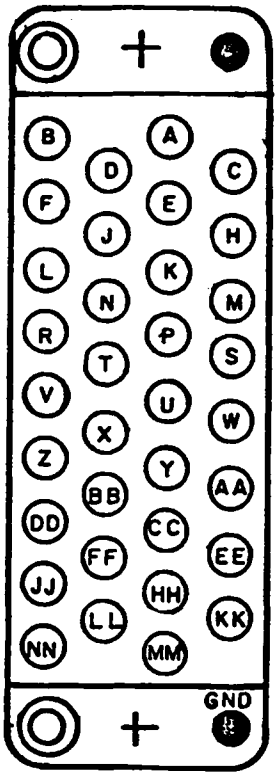


P1 (REAR VIEW)

P1					
PIN	FUNCTION	WIRE COLOR	PIN	FUNCTION	WIRE COLOR
A	+5V SOURCE		d		
B	FOC BRAKE SSR		e		
C	FOC TRANS SSR		f	SYNCHRO MON - HI	
D	ROT BRAKE (PIN OUT) SSR		h		
E	ROT PIN IN SSR		j	SYNCHRO MON - LO	
F	ROT TRANS SSR		k		
H			m		
J			n		
K			p		
L			r		
M			s		
N			t		
P			u		
R			v	FOC BRAKE VOLTS	
S	SYNCHRO R1		w		
T	SYNCHRO R1		x	FOC BRAKE AMPS	
U	SYNCHRO R2		y	FOC BRAKE RET	
V	SYNCHRO R2		z		
W	SYNCHRO R1		AA		
X	SYNCHRO R1		BB		
Y	SYNCHRO R2		CC		
Z	SYNCHRO R2		DD	ROT BRAKE VOLTS	
a			EE		
b			FF	ROT BRAKE AMPS	
c			HH	ROT BRAKE RET	

* INDICATES A FUNCTION NOT FOUND IN THIS MODULE

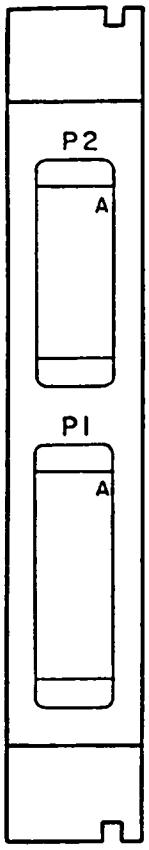
F/R BINS I/O
PANEL CONNECTOR
J5 TO FOC &
ROT TRANSLATORS



P2 (REAR VIEW)

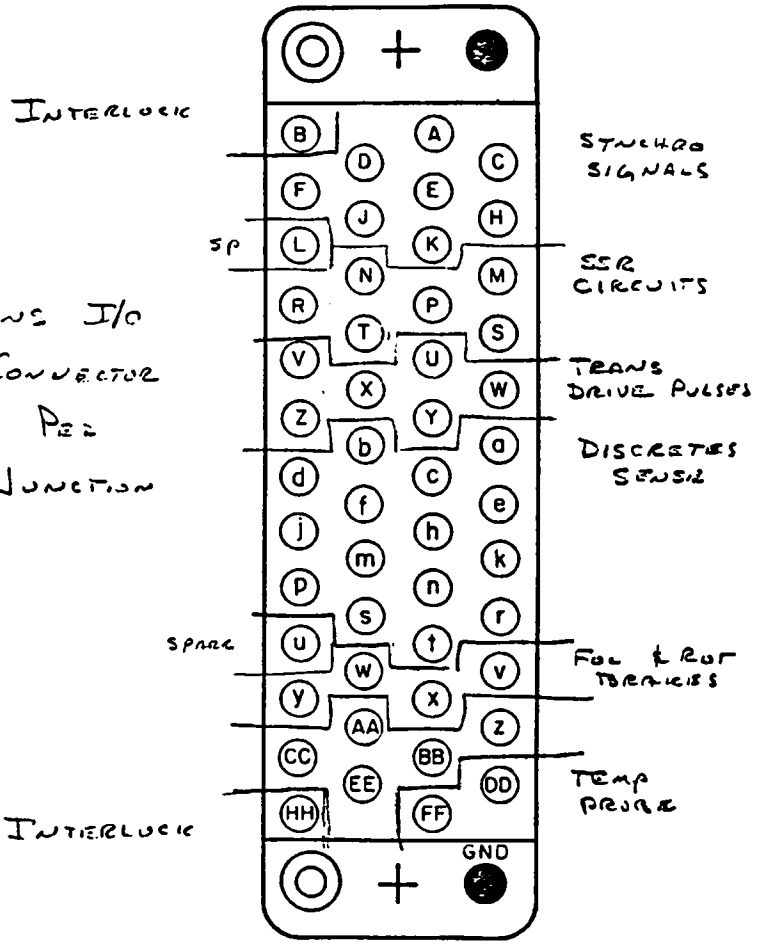
P2

PIN	FUNCTION	WIRE COLOR	PIN	FUNCTION	WIRE COLOR
A	INTLK LINE		V		
B	FST' LK LINE		W	FOC PULSE UP - HI	
C	ROT PULSE CW-HI		X	FOC PULSE DOWN-HI	
D	ROT PULSE CCW-HI		Y	FOC PULSE UP - RET	
E	ROT PULSE CW-RET		Z	FOC PULSE DOWN-RET	
F	ROT PULSE CCW-RET		AA	FOC TRANS PWR MON	
H	ROT. TRANS PWR MON		BB		
J			CC		
K			DD		
L			EE		
M			FF		
N			HH		
P			JJ		
R			KK		
S			LL		
T			MM		
U			NN		



SINGLE WIDE MODULE
(REAR VIEW)

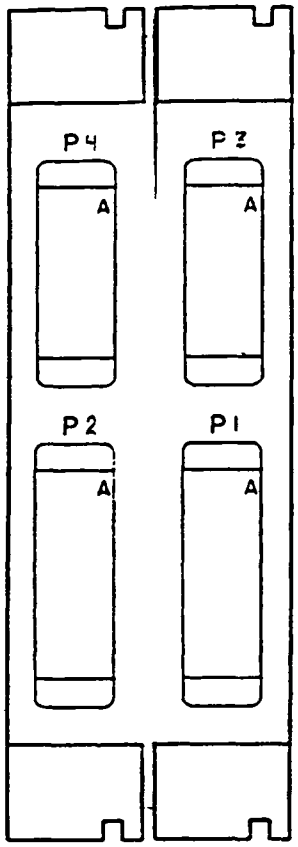
F/R RING I/O
PANEL CONNECTOR
J4, TO P2
ROOM JUNCTION
BOX



P1 (REAR VIEW)

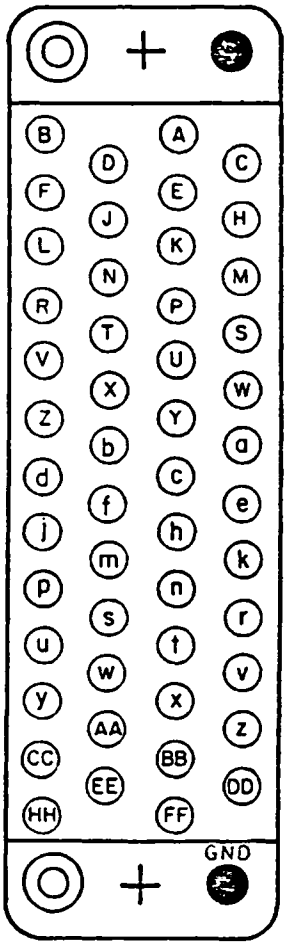
P1					
PIN	FUNCTION	WIRE COLOR	PIN	FUNCTION	WIRE COLOR
A	SYNCHRO EXC R1		d	ROT CCW LIM	
B	INTERLOCK PIN		e	PIN IN SW	
C	SYNCHRO EXC R2		f	PIN OUT SW	
D	FOC SYNCHRO S1		h	P λ SENSE SW	
E	ROT SYNCHRO S1		j	L λ " "	
F	FOC SYNCHRO S3		k	C λ " "	
H	ROT SYNCHRO S2		m	U λ " "	
J	FOC SYNCHRO S2		n	K λ " "	
K	ROT SYNCHRO S3		p	X λ " "	
L			r	Y λ " "	
M	FOC BRK SSR LEV		s	Z λ " "	
N	FOC TRANS " "		t	DISCRETES SENSE RET	
P	ROT BRK/PIN OUT " "		u		
R	ROT TRANS " "		v	FOC BRAKE +	
S	ROT PIN IN " "		w	ROT BRAKE +	
T	SSR + SOURCE		x	FOC BRAKE −	
U	FOC UP PULSE		y	ROT BRAKE −	
V	ROT CW PULSE		z		
W	FOC DWN PULSE		AA		
X	ROT CCW PULSE		BB		
Y	FOC PULSE RET		CC		
Z	ROT PULSE RET		DD	TEMP PROBE +	
a	FOC UP LIM		EE		
b	FOC DWN LIM		FF	TEMP PROBE −	
c	ROT CW LIM		HH	INTERLOCK	

* INDICATES A FUNCTION NOT FOUND IN THIS MODULE



DOUBLE WIDE MODULE
(REAR VIEW)

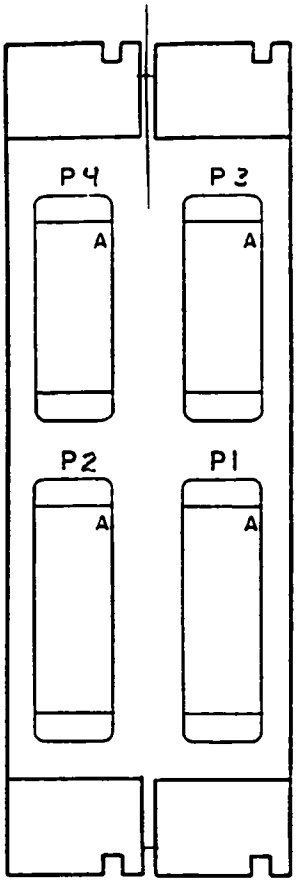
M7-E, F/R
CONTROL, P1 CONNECTOR
I/O SIGNAL/POWER
ASSIGNMENTS
8/11/83/DW
SHEET 1



P1 (REAR VIEW)

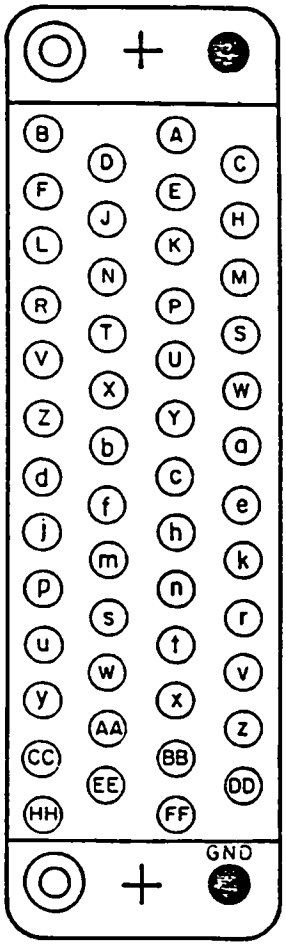
P1					
PIN	FUNCTION	WIRE COLOR	PIN	FUNCTION	WIRE COLOR
A	+15 VOLTS	RED	d	ROT CCW LIM INH	
B	LOGIC GND	BLACK	e	LIM INH RET	
C	+5 VOLTS	ORANGE	f	YOW P/	
D			h	FOC SER DATA, SIG	
E	-15 VOLTS	YELLOW	j	FOC LOAD CLOCK, SIG	
F			k	FOC SER DATA, RET	
H	$\overline{\text{SMA}-\phi}$		m	FOC LOAD CLOCK, RET	
J	$\overline{\text{SMA}-1}$		n	ROT SER DATA, SIG	
K	$\overline{\text{SMA}-2}$		p	ROT LOAD CLOCK, SIG	
L	$\overline{\text{SMA}-3}$		r	ROT SER DATA, RET	
M	DIGI-1, SIG		s	ROT LOAD CLOCK, RET	
N	CLKI-1, SIG		t	CONN INTLK SENSE	
P	DIGO-ϕ, SIG		u	FOC DATA REQ, SIG	
R	CLKI-1, RET		v	ROT DATA REQ, SIG	
S	STRI-1, SIG		w	FOC DATA REQ, RET	
T	CLKO-ϕ, SIG		x	ROT DATA REQ, RET	
U	STRI-1, RET		y	ALGI-3 SIG/HI	
V	CLKO-ϕ, RET		z	ROT BRAKE SER DRIVE	
W	STRO-ϕ, SIG		AA	ALGI-3 SIG/LO	
X	5 MHz TO DATA SET, SIG		BB	ANTA-16	
Y	STRO-ϕ, RET		CC	ANTA-8	
Z	5 MHz TO DATA SET, RET		DD	ANTA-4	
a	FOC UPPER LIM INH		EE	ANTA-2	
b	FOC LOWER LIM INH		FF	ANTA-1	
C	ROT CW LIM INH		HH	ANALOG GND	BLACK

* INDICATES A FUNCTION NOT FOUND IN THIS MODULE



DOUBLE WIDE MODULE
(REAR VIEW)

M7-E, F/R
CONTROL P2 CONNECTOR
I10 SIGNAL/POWER
ASSIGNMENTS, SHEET 2
8/11/83/DW



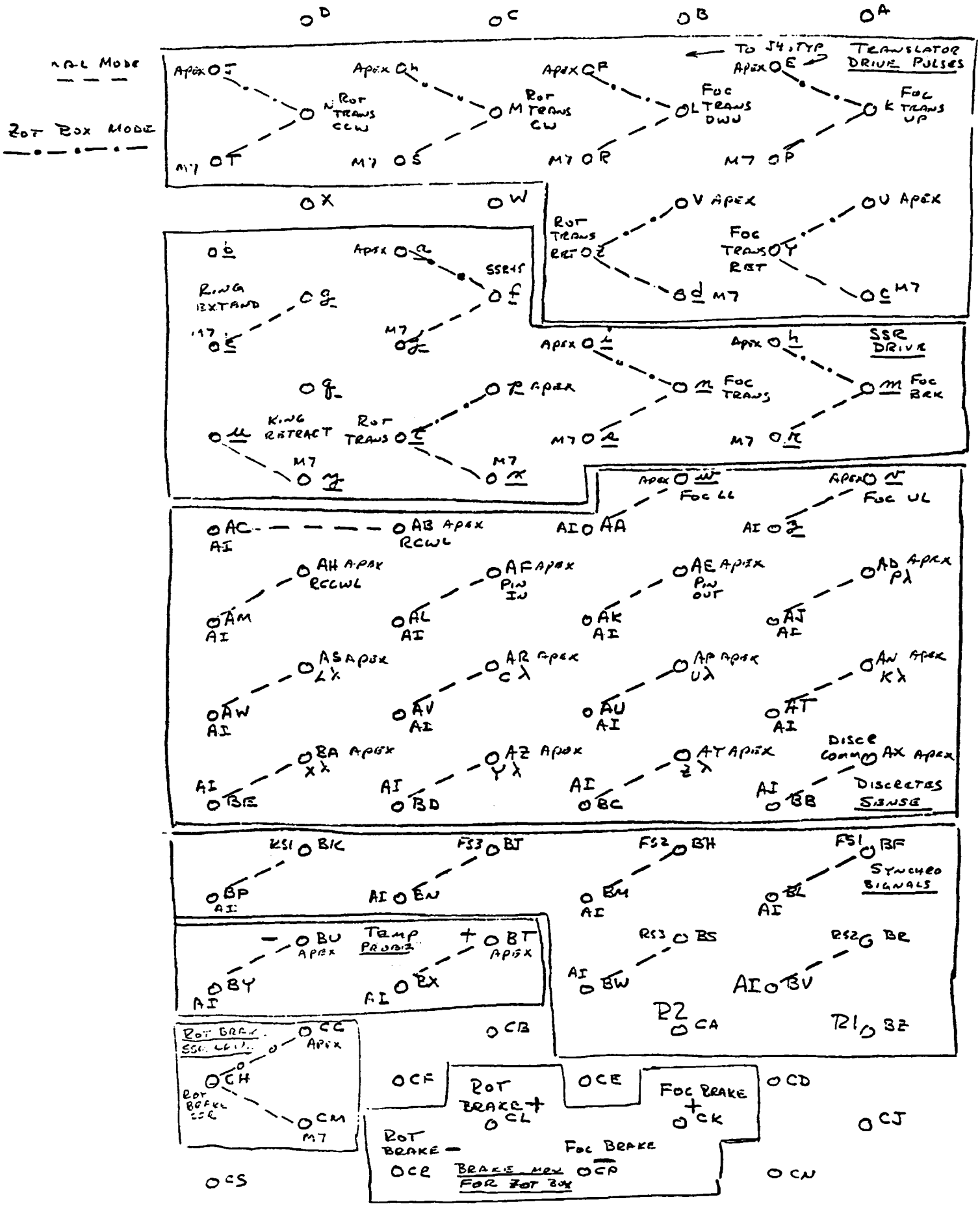
P2 (REAR VIEW)

P1

PIN	FUNCTION	WIRE COLOR	PIN	FUNCTION	WIRE COLOR
A	FOC CMD LOW DRIVE		d	FOC TRANS DRV UP, SIG	
B	FOC BRAKE " "		e	FOC TRANS DRV DWN, SIG	
C	FOC UPPER LIM " "		f	FOC. TRANS DRV, RET	
D	FOC LOWER LIM " "		h	FOC TRANS SSR DRIVE	
E	FOC TRANS POWER " "		j	FOC BRAKE SSR DRIVE	
F	FOC MOTOR PULSES " "		k	ROT TRANS DRV CW, SIG	
H	FOC DRV UP " "		m	ROT TRANS DRV CCW, SIG	
J	FOC DRV DOWN " "		n	ROT TRANS DRV, RET	
K	ROT CMD " "		p	ROT TRANS SSR DRV	
L	ROT BRAKE/PIN OUT " "		r	ROT BRAKE/PIN OUT SSR DRV	
M	ROT PIN IN " "		s	ROT PIN IN SSR DRV	
N	ROT CW LIM " "		t	FOC TRANS MON	
P	ROT CCW LIM " "		u	ROT TRANS MON	
R	ROT TRANS PWR " "		v	FOC RAMP SW	
S	ROT MOTOR PULSES " "		W	FOC DRV UP SW	
T	ROT DRV CW " "		X	FOC DRV DOWN SW	
U	ROT DRV CCW " "		y	ROT RAMP SW	
V	P λ " "		Z	ROT DRV CW SW	
W	L λ " "		AA	ROT DRV CCW SW	
X	C λ " "		BB	ROT PIN SW A0	
Y	U λ " "		CC	ROT PIN SW A1	
Z	K λ " "		DD	ROT PIN SW A2	
a	X λ " "		EE	λ SWITCH ACTIVE	
b	Y λ " "		FF	SYNCHRO MON — HI	
c	Z λ " "		HH	SYNCHRO MON — LO	

* INDICATES A FUNCTION NOT FOUND IN THIS MODULE
F/R SYSTEM D

Amp 201037-1, Rin I/O Conn



WIRE LIST

RACK: C	BIN: W/X	SLOT: I/O -J1	MODULE: I/O PANEL J1	TYPE: 104 PIN
LIST BY:	WIRE BY:		ZOT BOX / JUMPER	
CONNECTOR TYPE: 201037-1		CONNECTOR PAGE: 1		

PIN	FUNCTION	TYPE	FROM	TO
A	CONN INTLK			I/O -J1-CN
B				
C				
D	CONN INTLK		I/O - J4-HH	
E	APEX FOC PULSE - UP		I/O -J4 -U	
F	APEX FOC PULSE - DOWN		I/O -J4 - W	
H	APEX ROT PULSE - CW		I/O -J4 - V	
J	APEX ROT PULSE - CCW		I/O -J4 -X	
K	FOC TRANS PULSE - UP	WH, #26, TP#32	I/O -J5 -W	
L	FOC TRANS PULSE - DOWN	WH, #26, TP#33	I/O -J5 - X	
M	ROT TRANS PULSE - CW	WH, #26, TP#30	I/O -J5 -C	
N	ROT TRANS PULSE - CCW	WH, #26, TP#31	I/O -J5- D	
P	M7 FOC PULSE - UP	WH, #26, TP#34	W -4J2 -d	
R	M7 FOC PULSE - DOWN	WH, #26, TP#35	W -4J2 - e	
S	M7 ROT PULSE - CW	WH, #26, TP#36	W -4J2 - k	
T	M7 ROT PULSE - CCW	WH, #26, TP#37	W- 4J2 - m	
U	APEX FOC PULSE RET		I/O -J4 - Y	
V	APEX ROT PULSE RET		I/O -J4 - Z	
W				
X				
Y	FOC TRANS PULSE RET	BLK, #26, TP#32 TP#33	I/O -J5 - Y I/O -J5 - Z	
Z	ROT TRANS PULSE RET	BLK, #26, TP#30 TP#31	I/O -J5- E I/O -J5 - F	
a	APEX +5 SSR		I/O -J4 -T	
b				
c *	M22 +5 SSR			W-8J2-A
d	RING EXTEND SSR DRIVE			W-8J2 -D
h	APEX FOC LOCK SSR DRV		I/O -J4 - M	
i	APEX FOC TRANS SSR DRV		I/O -J4 - N	
j	F/R RING +5 SSR	ORANGE, #20	W - 9J1 - R	
k	M7 RING EXTEND SSR DRV		W - 4J2 - m	

* E-2 SHEET 4 ON c, d

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE:
TITLE: F/R SYSTEM D		REV:
	DWG NO A13748W10	SHEET 42 OF 50

WIRE LIST

RACK: C	BIN: W/X	SLOT: I/O – J1	MODULE: I/O PANEL J1	TYPE: 104 PIN
LIST BY:	WIRE BY:		Bot Box / Jumper	
CONNECTOR TYPE: 201037-1		CONNECTOR PAGE: 2		

PIN	FUNCTION	TYPE	FROM	TO
m	Foc Brake SSR Drive			W-8J2-B
n	Foc Trans SSR Drive			W-8J2-C
p	Apex Rot Trans SSR Drv		I/O-J4-R	
q				
r	M7 Foc Brake SSR Drv		W-4J2-j	
s	M7 Foc Trans SSR Drv		W-4J2-h	
t	Rot Trans SSR Drive			W-8J2-F
u	Rim Retract SSR Drive			W-8J2-E
v	Apex Foc U Lim		I/O-J4-a	
w	Apex Foc L Lim		I/O-J4-b	
x	M7 Rot Trans SSR Drv		W-4J2-p	
y	M7 Rim Retract SSR Drv		W-4J2-d	
z	AI Foc U Lim Input		W-1J1-T	
AA	AI Foc L Lim Input		W-1J1-V	
AB	Apex Rot CW Lim		I/O-J4-c	
AC	AI Rot CW Lim Input		W-1J1-U	
AD	Apex Pλ Sense		I/O-J4-k	
AE	Apex Pin out Sense		I/O-J4-f	
AF	Apex Pin In Sense		I/O-J4-e	
AH	Apex Rot CCW Lim Sense		I/O-1J4-d	
AJ	AI Pλ Input		W-1J1-b	
AK	AI Pin out Input		W-1J1-Z	
AL	AI Pin In Input		W-1J1-X	
AM	AI Rot CCW Lim Input		W-1J1-W	
AN	Apex Kλ Sense		I/O-J4-n	
AP	Apex Uλ Sense		I/O-J4-m	
AR	Apex Cλ Sense		I/O-J4-k	
AS	Apex Lλ Sense		I/O-J4-j	
AT	AI Kλ Input		W-1J1-f	
AU	AI Uλ Input		W-1J1-e	

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: FIR SYSTEM D		REV:
	DWG NO A13740W10	SHEET 43 OF 50

WIRE LIST

RACK: C	BIN: W/X	SLOT: I/O -J1	MODULE: I/O PANEL J1	TYPE: 104 P.N
LIST BY:		WIRE BY:		ROT BOX / JUMPER
CONNECTOR TYPE: 201037-1		CONNECTOR PAGE: 3		

PIN	FUNCTION	TYPE	FROM	TO
AV	AI CX INPUT		W-1J1-d	
AW	AI LX INPUT		W-1J1-c	
AX	APEX DISCR SENS COMM		I/O-J4-t	
AT	APEX ZX SENSE		I/O-J4-s	
AZ	APEX YX SENSE		I/O-J4-r	
BA	APEX XX SENSE		I/O-J4-p	
BB	AI DISCR SENSE COMM		W-1J1-m	
BC	AI ZX INPUT		W-1J1-k	
BD	AI YX INPUT		W-1J1-j	
BE	AI XX INPUT		W-1J1-h	
BF	APEX FOC S1		I/O-J4-D	
BH	APEX FOC S2		I/O-J4-J	
BJ	APEX FOC S3		I/O-J4-F	
BK	APEX ROT S1		I/O-J4-E	
BL	AI FOC S1 INPUT			W-1J1-F
BM	AI FOC S2 INPUT			W-1J1-J
BN	AI FOC S3 INPUT			W-1J1-L
BP	AI ROT S1 INPUT			W-1J1-H
BR	APEX ROT S2		I/O-J4-H	
BS	APEX ROT S3		I/O-J4-K	
BT	APEX TEMP PROBE +		I/O-J4-DD	
BU	APEX TEMP PROBE -		I/O-J4-FF	
BV	AI ROT S2 INPUT			W-1J1-K
BW	AI ROT S3 INPUT			W-1J1-M
BX	AI TEMP PROBE + INPUT		W-1J1-w	
BY	AI TEMP PROBE - INPUT		W-1J1-y	
CB	SHIELDED EXC R1	WH, #26, TP #42	I/O-J4-A	
CA	SHIELDED EXC R2	BLK #26, TP #42	I/O-J4-C	
CD				
CC	APEX ROT BLK SCR DRN	I/O J4-P from		

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun83
TITLE: F/R SYSTEM D		REV:
	DWG NO A13740W10	SHEET 44 OF 50

WIRE LIST

RACK: C	BIN: W/X	SLOT: I/O – J1	MODULE: I/O PANEL J1	TYPE: 104 PIN
LIST BY:		WIRE BY:		ROT BOX / JUMPER
CONNECTOR TYPE: 201037-1		CONNECTOR PAGE: 4		

PIN	FUNCTION	TYPE	FROM	TO
CD				
CE				
CF				
CH	ROT BRAKE SSR DRIVE			W-8J2-P
CJ				
CK	FOC BRAKE VOLTS +		W-1J1-m	
CL	ROT BRAKE VOLTS +		W-1J1-p	
CM	ROT BRAKE SSR DRIVE		W-3J1-3	
CN	CONN INTLK		I/O-J1-A	
CP	FOC BRAKE VOLTS –		W-1J1-t	
CR	ROT BRAKE VOLTS –		W-1J1-u	
CS	CONN INTLK			W-8J1-E
c	M7 FOC PULSE RET	BLK, #26, TP#34 TP#35	W-4J2-f	
d	M7 ROT PULSE RET	BLK #26, TP#36 TP#37	W-4J2-n	

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: F/R SYSTEM D		REV:
	DWG NO A13740W10	SHEET 45 OF 50

WIRE LIST

RACK: C	BIN: W/X	SLOT: I/O - J2	MODULE: I/O PANEL J2	TYPE: 14 Pin
LIST BY:		WIRE BY:		CMD/DATA I/O SIGNALS
CONNECTOR TYPE: 201298 - 3		CONNECTOR PAGE:		

PIN	FUNCTION	TYPE	FROM	TO
A				
B	DATA OUTPUT, RET		I/O - J2 - M	
C				
D	CMD INPUT RET	BLK #26, TP #38	I/O - J2 - N	W - 8J1 - D
E	DATA OUTPUT, SIG		I/O - J2 - J	
F	CMD INPUT, SIG	WH, #26, TP #38	I/O - J2 - L	W - 8J1 - B
H				
J	DATA OUTPUT, SIG	WH, #26, TP #39	W - 8J1 - F	I/O - J2 - E
K				
L	CMD INPUT, SIG		I/O - J2 - F	
M	DATA OUTPUT, RET	BLK, #26, TP #39	W - 8J1 - L	I/O - J2 - B
N	CMD INPUT, RET		I/O - J2 - D	
P				
R				

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: EIR SYSTEM D		REV:
	DWG NO A13740W10	SHEET 46 OF 50

WIRE LIST

RACK: C	BIN: W/X	SLOT: I/O - J4	MODULE: I/O PANEL J4	TYPE: 50 PIN
LIST BY:		WIRE BY:		PEC ROOM JUNCT BOX
CONNECTOR TYPE: 200277-4		CONNECTOR PAGE: 1		

PIN	FUNCTION	TYPE	FROM	TO
A	SYNCHRO EXC R1	WH, #26, TP#13	W-8J2-T	I/O-J1-BZ
B	INTERLOCK		I/O-J5-MM	
C	SYNCHRO EXC R2	BLK, #26, TP#13	W-8J2-V	I/O-J1-CA
D	FOC SYNCHRO S1			I/O-J1-BF
E	ROT SYNCHRO S1			I/O-J1-BK
F	FOC SYNCHRO S3			I/O-J1-BJ
H	ROT SYNCHRO S2			I/O-J1-BR
J	FOC SYNCHRO S2			I/O-J1-BH
K	ROT SYNCHRO S2			I/O-J1-BS
L				
M	FOC BRAKE SCR DRV			I/O-J1-h
N	FOC TRANS " "			I/O-J1-l'
P	ROT BRAKE SSR DRIVE			I/O-J1-CC
R	ROT TRANS " "			I/O-J1-k
S				
T	SSR + SOURCE			I/O-J1-a
U	APEX FOC PULSE-UP			I/O-J1-E
V	APEX ROT PULSE-CW			I/O-J1-H
W	APEX FOC PULSE-DOWN			I/O-J1-F
X	APEX ROT PULSE-CCW			I/O-J1-J
Y	APEX FOC PULSE-RET			I/O-J1-U
Z	APEX ROT PULSE-RET			I/O-J1-V
a	FOC UP LIM			I/O-J1-N
b	FOC DOWN LIM			I/O-J1-W
c	ROT CW LIM			I/O-J1-AB
d	ROT CCW LIM			I/O-J1-AH
e	PIN J1 CW			I/O-J1-AF
f	PIN OUT SW			I/O-J1-AE
h	F λ SENSE CW			I/O-J1-AD
i	L λ " "			I/O-J1-AS

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: F/R SYSTEM D		REV:
	DWG NO A13740W10	SHEET 47 OF 50

WIRE LIST

RACK: C	BIN: W/X	SLOT: I/O - J4	MODULE: I/O PANEL J4	TYPE: 50 PIN
LIST BY:		WIRE BY:		PED ROOM JUNCT BOX
CONNECTOR TYPE: 200277-4		CONNECTOR PAGE: 2		

PIN	FUNCTION	TYPE	FROM	TO
E	C λ SENSE SW			I/O - J1 - AR
m	U λ " "			I/O - J1 - AP
m	K λ " "			I/O - J1 - AN
Z	X λ " "			I/O - J1 - BA
Z	Y λ " "			I/O - J1 - AZ
Z	Z λ " "			I/O - J1 - AY
E	DISCRETES SENSE RET			I/O - J1 - AX
E				
E				
E				
E				
E				
E				
AA				
BB				
CC				
DD	TEMP PROBE +			I/O - J1 - BT
EE				
FF	TEMP PROBE -			I/O - J1 - BU
HH	INTERLOCK			I/O - J1 - D

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: F/R SYSTEM D		REV:
	DWG NO A13740W10	SHEET 48 OF 50

WIRE LIST

RACK: C	BIN: W/X	SLOT: I/O - J5	MODULE: I/O PANEL J5	TYPE: 34 PIN
LIST BY:		WIRE BY:		FOC & ROT TRANS DRIVE
CONNECTOR TYPE: 200836-3		CONNECTOR PAGE: 1		

PIN	FUNCTION	TYPE	FROM	TO
A	INT'LK LINE		W-3J1-t	
B	INT'LK LINE			I/O-J5-NN
C	ROT PULSE CW-HI	wh, #26, TP#30	I/O-J1-M	
D	ROT PULSE CCW-HI	wh, #26, TP#31	I/O-J1-N	
E	ROT PULSE CW-RET	Blk, #26, TP#30	I/O-J1-Z	
F	ROT PULSE CCW-RET	Blk, #26, TP#31	I/O-J1-Z	
H	ROT TRANS PWR MON			W-4J2-LL
J				
K				
L				
M				
N				
P				
R				
S				
T				
U				
V				
W	FOC PULSE UP - HI	wh, #26, TP#32	I/O-J1-K	
X	FOC PULSE DOWN-HI	wh, #26, TP#33	I/O-J1-L	
Y	FOC PULSE UP-RET	Blk, #26, TP#32	I/O-J1-Y	
Z	FOC PULSE DOWN-RET	Blk, #26, TP#33	I/O-J1-Y	
AA	FOC TRANS MON			W-4J2-t
BB				
CC				
DD				
EE				
FF				
HH				
JJ				

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: FIR SYSTEM D		REV:
	DWG NO A13740W10	SHEET 49 OF 59

WIRE LIST

RACK: 6	BIN: W/X	SLOT: I/O - J5	MODULE: I/O PANEL J5	TYPE: 34 PIN
LIST BY:		WIRE BY:		FOC & ROT TRANS DRIVE
CONNECTOR TYPE: 200938 - 3		CONNECTOR PAGE: 2		

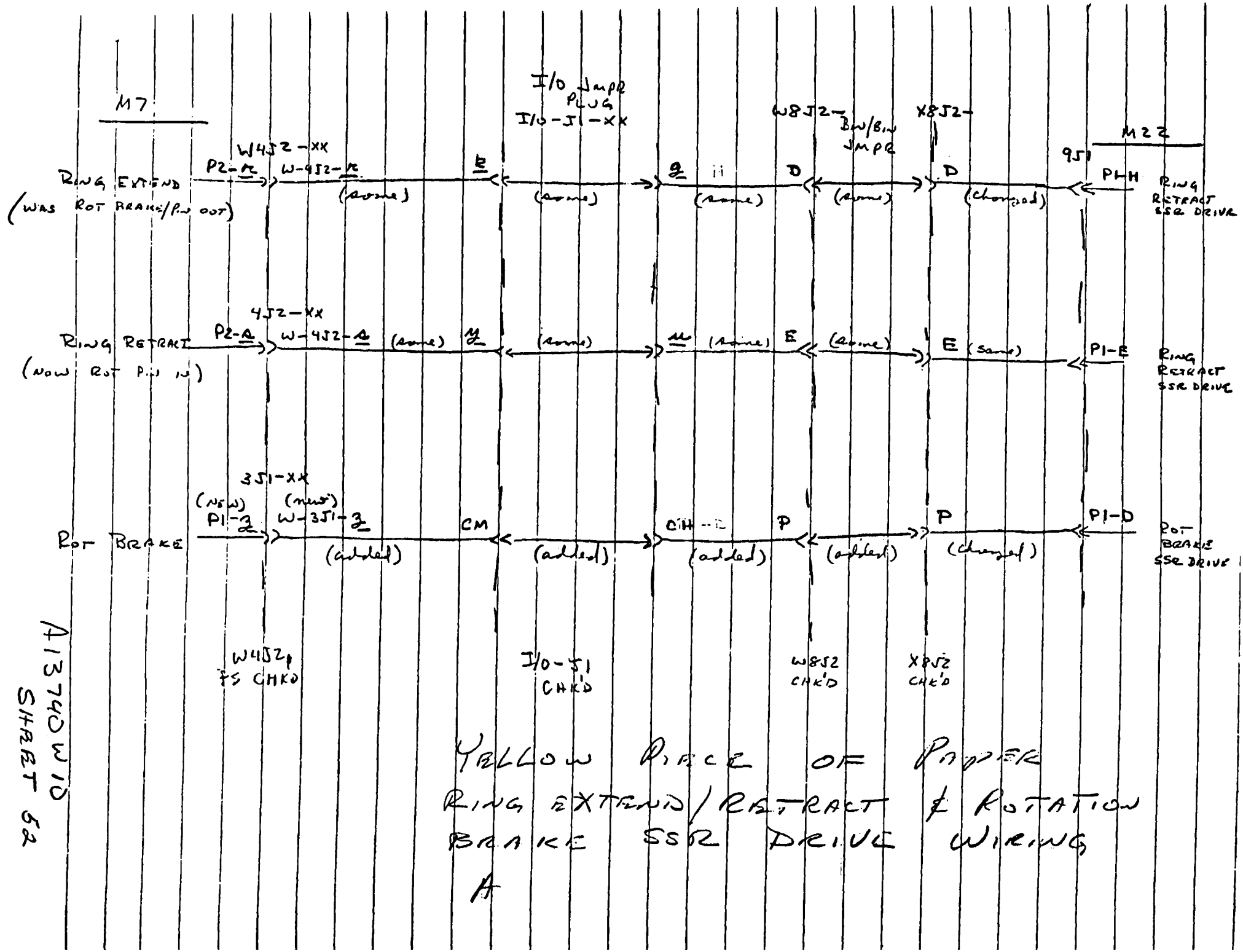
PIN	FUNCTION	TYPE	FROM	TO
KK				
LL				
MM	INT'LK LINE			I/O - J4 - B
NN	INT'LK LINE		I/O - J5 - B	

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE: Jun 83
TITLE: FIR SYSTEM 'D'		REV:
	DWG NO A13740W10	SHEET 50 OF 50

RACK: C	BIN: 401X	SLOT: I/O - J6	MODULE: I/O PANEL J6	TYPE: 14 PI
LIST BY:		WIRE BY:		ANEMOMETER SIGNA
CONNECTOR TYPE: 201299-3		CONNECTOR PAGE		

PIN	FUNCTION	WIRE TYPE	FROM	TO
A	ANEMOMETER #1 HI	WH, #26 . TP #42	W-BJ1-V	I/O-J6-F
B	ANEMOMETER #2 HI	WH, #26 . TP #43	W-BJ1-U	I/O-J6-P
C	ANEMOMETER #1 RET	BLK, #26, TP #42	W-BJ1-X	I/O-J6-K
D				
E	ANEMOMETER #2 RET	BLK, #26, TP #43	W-BJ1-W	I/O-J6-J
F				
H				
J	ANEMOMETER #2 RET		I/O-J6-E	
K				
L				
M	ANEMOMETER #2 HI		I/O-J6-B	
N				
P	ANEMOMETER #1 LO		I/O-J6-C	
R	ANEMOMETER #1 HI		I/O-J6-A	

NATIONAL RADIO ASTRONOMY OBSERVATORY	PROJ:	DATE:
TITLE:		REV:
	DWG. NO.	SHEET 51 OF 51


M7
I/O Jmpr Plug I/O-J1-XX
W8J2-
X8J2-
Bw/Bn Jmpr
M22
W4J2-XX
P2-K
W-4J2-K
K
g
D
D
9J1
PH-H
RING RETRACT SSR DRIVE
(WAS ROT BRAKE/Pin OUT)
RING EXTEND
(same)
(same)
(same)
(same)
(changed)
4J2-XX
P2-A
W-4J2-A
A
M
u
E
E
P1-E
RING RETRACT SSR DRIVE
RING RETRACT
(NOW ROT Pin 10)
(same)
(same)
(same)
(same)
(same)
3J1-XX
(NEW)
(NOW)
P1-2
W-3J1-Z
Z
CM
CH
P
P
P1-D
ROT BRAKE SSR DRIVE
ROT BRAKE
(added)
(added)
(added)
(added)
(changed)
W4J2 FS CHK'D
I/O-J1 CHK'D
W8J2 CHK'D
X8J2 CHK'D
YELLOW PIECE OF PAPER
RING EXTEND/RETRACT & ROTATION
BRAKE SSR DRIVE WIRING
A
A13740W10
SHEET 52

intel

8085A/8085A-2
SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSORS

- **Single +5V Power Supply**
- **100% Software Compatible with 8080A**
- **1.3 μs Instruction Cycle (8085A); 0.8 μs (8085A-2)**
- **On-Chip Clock Generator (with External Crystal, LC or RC Network)**
- **On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control**
- **Four Vectored Interrupt Inputs (One is Non-Maskable) Plus an 8080A-Compatible Interrupt**
- **Serial In/Serial Out Port**
- **Decimal, Binary and Double Precision Arithmetic**
- **Direct Addressing Capability to 64k Bytes of Memory**

The Intel® 8085A is a complete 8 bit parallel Central Processing Unit (CPU). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's (8085A (CPU), 8156 (RAM/IO) and 8355/8755A (ROM/PROM/IO)) while maintaining total system expandability. The 8085A-2 is a faster version of the 8085A.

The 8085A incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A, thereby offering a high level of system integration.

The 8085A uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of 8155/8156/8355/8755A memory products allow a direct interface with the 8085A.

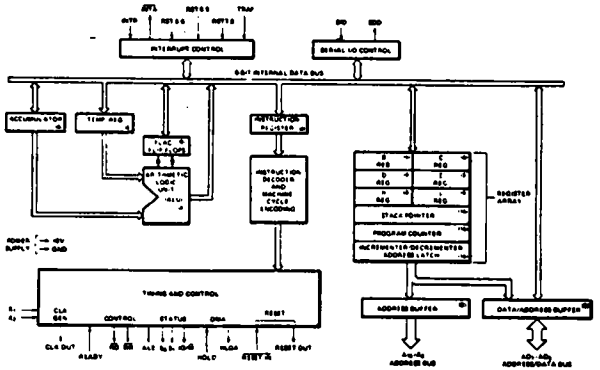


Figure 1. 8085A CPU Functional Block Diagram

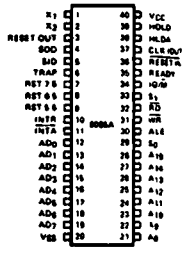


Figure 2. 8085A Pin Configuration

Table 1. Pin Description

Symbol	Type	Name and Function
A_8-A_{15}	O	**Address Bus:** The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.
AD_0—$_7$	I/O	**Multiplexed Address/Data Bus:** Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.
ALE	O	**Address Latch Enable:** It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.
S_0, S_1, and IO/$\overline{M}$	O	**Machine Cycle Status:** IO/$\overline{M}$ S_1 S_0 Status 0 0 1 Memory write 0 1 0 Memory read 1 0 1 I/O write 1 1 0 I/O read 0 1 1 Opcode fetch 1 1 1 Opcode fetch 1 1 1 Interrupt Acknowledge * 0 0 Halt * X X Hold * X X Reset * = 3-state (high impedance) X = unspecified S_1 can be used as an advanced R/$\overline{W}$ status. IO/$\overline{M}$, S_0 and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.
$\overline{RD}$	O	**Read Control:** A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer. 3-stated during Hold and Halt modes and during RESET.
$\overline{WR}$	O	**Write Control:** A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. 3-stated during Hold and Halt modes and during RESET
READY	I	**Ready:** If READY is high during a read or write cycle, it indicates that the memory or perpheral is ready to send or receive data. If READY is low, the cpu will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. READY must conform to specified setup and hold times
HOLD	I	**Hold:** Indicates that another master is requesting the use of the address and data buses. The cpu, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.
HLDA	O	**Hold Acknowledge:** Indicates that the cpu has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The cpu takes the bus one half clock cycle after HLDA goes low.
INTR	I	**Interrupt Request:** Is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.
$\overline{INTA}$	O	**Interrupt Acknowledge:** Is used instead of (and has the same timing as) $\overline{RD}$ during the instruction cycle after an INTR is accepted. It can be used to activate an 8259A interrupt chip or some other interrupt port.
RST 5.5 RST 6.5 RST 7.5	I	**Restart Interrupts:** These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in Table 2. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.

Table 1. Pin Description (Continued)

Symbol	Type	Name and Function
TRAP	I	**Trap:** Trap interrupt is a non-maskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5-7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt. (See Table 2.)
$\overline{\text{RESET IN}}$	I	**Reset In:** Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{\text{RESET IN}}$ is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay. The cpu is held in the reset condition as long as $\overline{\text{RESET IN}}$ is applied.

Symbol	Type	Name and Function
RESET OUT	O	**Reset Out:** Reset Out indicates cpu is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
X_1, X_2	I	X_1 and X_2: Are connected to a crystal, LC, or RC network to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
CLK	O	**Clock:** Clock output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.
SID	I	**Serial Input Data Line:** The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
SOD	O	**Serial Output Data Line:** The output SOD is set or reset as specified by the SIM instruction.
V_{CC}		**Power:** +5 volt supply.
V_{SS}		**Ground:** Reference.

Table 2. Interrupt Priority, Restart Address, and Sensitivity

Name	Priority	Address Branched To (1) When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge AND high level until sampled
RST 7.5	2	3CH	Rising edge (latched).
RST 6.5	3	34H	High level until sampled.
RST 5.5	4	2CH	High level until sampled.
INTR	5	See Note (2).	High level until sampled.

NOTES:
1. The processor pushes the PC on the stack before branching to the indicated address.
2. The address branched to depends on the instruction provided to the cpu when the interrupt is acknowledged.

FUNCTIONAL DESCRIPTION

The 8085A is a complete 8-bit parallel central processor. It is designed with N-channel depletion loads and requires a single +5 volt supply. Its basic clock speed is 3 MHz (8085A) or 5 MHz (8085A-2), thus improving on the present 8080A's performance with higher system speed. Also it is designed to fit into a minimum system of three IC's: The cpu (8085A), a RAM/IO (8156), and a ROM or EPROM/IO chip (8355 or 8755A).

The 8085A has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or as 16-bit register pairs. The 8085A register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8 bits
PC	Program Counter	16-bit address
BC,DE,HL	General-Purpose Registers; data pointer (HL)	8 bits x 6 or 16 bits x 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flags (8-bit space)

The 8085A uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle. of a machine cycle the low order address is sent out on the Address/Data bus. These lower 8 bits may be latched externally by the Address Latch Enable signal ALE. During the rest of the machine cycle the data bus is used for memory or I/O data.

The 8085A provides $\overline{\text{RD}}$, $\overline{\text{WR}}$, S_0, S_1, and IO/$\overline{\text{M}}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{\text{INTA}}$) is also provided. HOLD and all interrupts are synchronized with the processor's internal clock. The 8085A also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

In addition to these features, the 8085A has three maskable, vector interrupt pins and one nonmaskable TRAP interrupt.

INTERRUPT AND SERIAL I/O

The 8085A has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The non-maskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks. (See Table 2.)

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are *high level-sensitive* like INTR (and INT on the 8080) and are recognized with the same timing as INTR. RST 7.5 is *rising edge-sensitive*.

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request. See Section 5.2.7. The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a $\overline{\text{RESET IN}}$ to the 8085A. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and $\overline{\text{RESET IN}}$. (See SIM, Chapter 5.

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP — highest priority, RST 7.5, RST 6.5, RST 5.5, INTR — lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both *edge and level sensitive*. The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Figure 3 illustrates the TRAP interrupt request circuitry within the 8085A. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

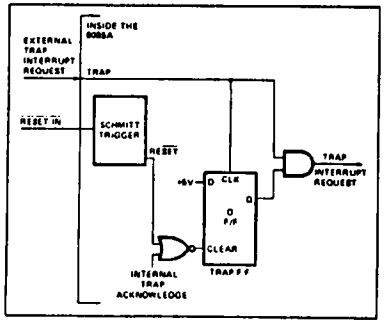


Figure 3. TRAP and RESET IN Circuit

The TRAP interrupt is special in that it disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR, or RST 5.5-7.5 will provide current Interrupt Enable status, revealing that interrupts are disabled. See the description of the RIM instruction in Chapter 5.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

DRIVING THE X_1 AND X_2 INPUTS

You may drive the clock inputs of the 8085A or 8085A-2 with a crystal, an LC tuned circuit, an RC network, or an external clock source. The driving frequency must be at least 1 MHz, and must be twice the desired internal clock frequency; hence, the 8085A is operated with a 6 MHz crystal (for 3 MHz clock), and the 8085A-2 can be operated with a 10 MHz crystal (for 5 MHz clock). If a crystal is used, it must have the following characteristics:

Parallel resonance at twice the clock frequency desired
C_L (load capacitance) ≤ 30 pF
C_S (shunt capacitance) ≤ 7 pF
R_S (equivalent shunt resistance): ≤ 75 Ohms
Drive level: 10 mW
Frequency tolerance: ±.005% (suggested)

Note the use of the 20 pF capacitor between X_2 and ground. This capacitor is required with crystal frequencies below 4 MHz to assure oscillator startup at the correct frequency. A parallel-resonant LC circuit may be used as the frequency-determining network for the 8085A, providing that its frequency tolerance of approximately ±10% is acceptable. The components are chosen from the formula:

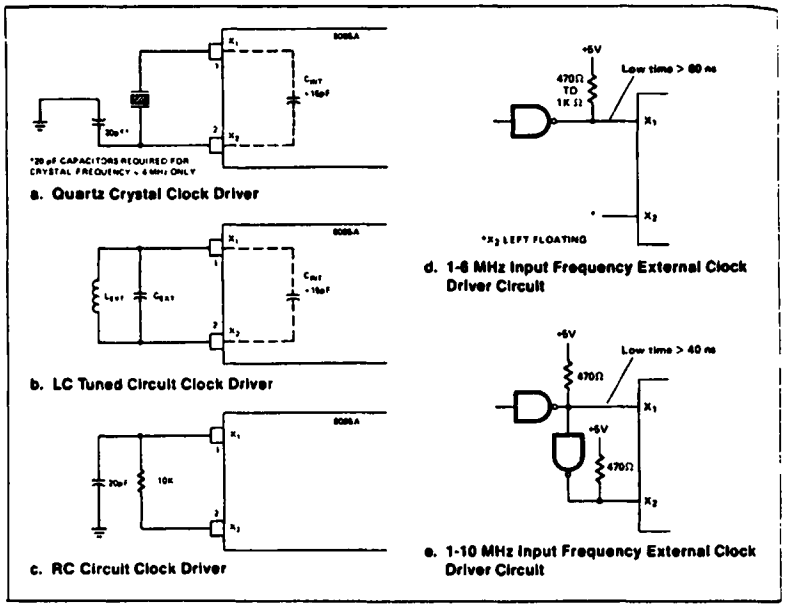
$$f = \frac{1}{2\pi\sqrt{L(C_{ext} + C_{int})}}$$

To minimize variations in frequency, it is recommended that you choose a value for C_{ext} that is at least twice that of C_{int}, or 30 pF. The use of an LC circuit is not recommended for frequencies higher than approximately 5 MHz.

An RC circuit may be used as the frequency-determining network for the 8085A if maintaining a precise clock frequency is of no importance. Variations in the on-chip timing generation can cause a wide variation in frequency when using the RC mode. Its advantage is its low component cost. The driving frequency generated by the circuit shown is approximately 3 MHz. It is not recommended that frequencies greatly higher or lower than this be attempted.

Figure 4 shows the recommended clock driver circuits. Note in D and E that pullup resistors are required to assure that the high level voltage of the input is at least 4 V.

For driving frequencies up to and including 6 MHz you may supply the driving signal to X_1 and leave X_2 open-circuited (Figure 4D). If the driving frequency is from 6 MHz to 10 MHz, stability of the clock generator will be improved by driving both X_1 and X_2 with a push-pull source (Figure 4E). To prevent self-oscillation of the 8085A, be sure that X_2 is not coupled back to X_1 through the driving circuit.



a. Quartz Crystal Clock Driver

b. LC Tuned Circuit Clock Driver

c. RC Circuit Clock Driver

d. 1-6 MHz Input Frequency External Clock Driver Circuit

e. 1-10 MHz Input Frequency External Clock Driver Circuit

Figure 4. Clock Driver Circuits

GENERATING AN 8085A WAIT STATE

If your system requirements are such that slow memories or peripheral devices are being used, the circuit shown in Figure 5 may be used to insert one WAIT state in each 8085A machine cycle.

The D flip-flops should be chosen so that:
- CLK is rising edge-triggered
- CLEAR is low-level active.

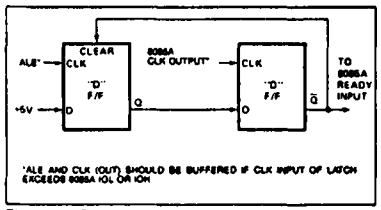


Figure 5. Generation of a Wait State for 8085A CPU

As in the 8080, the READY line is used to extend the read and write pulse lengths so that the 8085A can be used with slow memory. HOLD causes the cpu to relinquish the bus when it is through with it by floating the Address and Data Buses.

SYSTEM INTERFACE

The 8085A family includes memory components, which are directly compatible to the 8085A cpu. For example, a system consisting of the three chips, 8085A, 8156, and 8355 will have the following features:

- 2K Bytes ROM
- 256 Bytes RAM
- 1 Timer/Counter
- 4 8-bit I/O Ports
- 1 6-bit I/O Port
- 4 Interrupt Levels
- Serial In/Serial Out Ports

This minimum system, using the standard I/O technique is as shown in Figure 6.

In addition to standard I/O, the memory mapped I/O offers an efficient I/O addressing technique. With this technique, an area of memory address space is assigned for I/O address, thereby, using the memory address for I/O manipulation. Figure 7 shows the system configuration of Memory Mapped I/O using 8085A.

The 8085A cpu can also interface with the standard memory that does *not* have the multiplexed address/data bus. It will require a simple 8212 (8-bit latch) as shown in Figure 8.

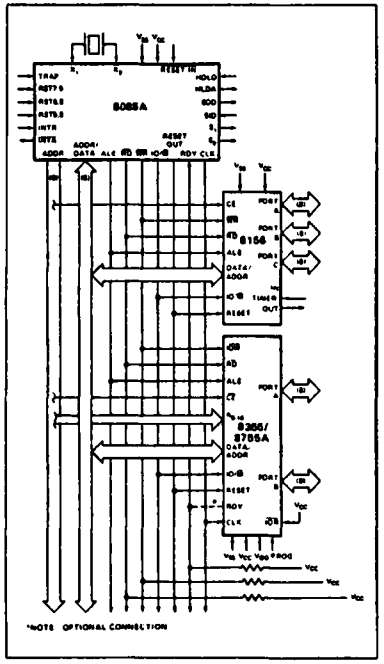


Figure 6. 8085A Minimum System (Standard I/O Technique)

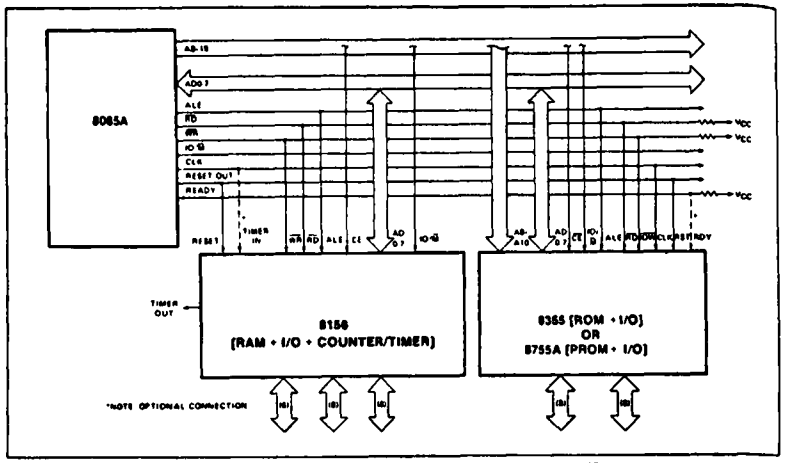


Figure 7. MCS-85™ Minimum System (Memory Mapped I/O)

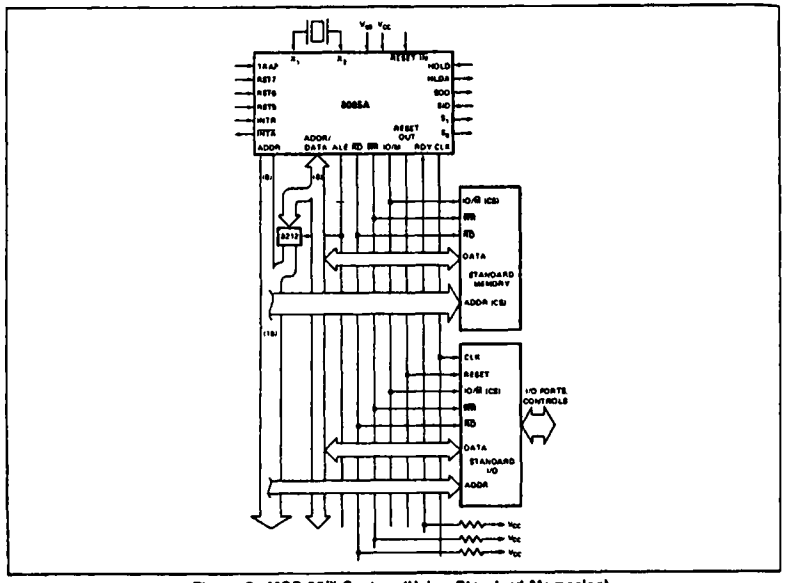


Figure 8. MCS-85™ System (Using Standard Memories)

BASIC SYSTEM TIMING

The 8085A has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure 9 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines ($IO/\overline{M}$, S_1, S_0) and the three control signals ($\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$). (See Table 3.) The status lines can be used as advanced controls (for device selection, for example), since they become active at the T_1 state, at the outset of each machine cycle. Control lines $\overline{RD}$ and $\overline{WR}$ become active later, at the time when the transfer of data is to take place, so are used as command lines.

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of $\overline{READY}$ or HOLD inputs). Any T state must be one of ten possible states, shown in Table 4.

Table 3. 8085A Machine Cycle Chart

MACHINE CYCLE			STATUS			CONTROL		
			IO/M	S1	S0	RD	WR	INTA
OPCODE FETCH	(OF)		0	1	1	0	1	1
MEMORY READ	(MR)		0	1	0	0	1	1
MEMORY WRITE	(MW)		0	0	1	1	0	1
I/O READ	(IOR)		1	1	0	0	1	1
I/O WRITE	(IOW)		1	0	1	1	0	1
ACKNOWLEDGE OF INTR	(INA)		1	1	1	1	1	0
BUS IDLE	(BI)	DAD	0	1	0	1	1	1
		ACK OF RST.TRAP	1	1	1	1	1	1
		HALT	TS	0	0	TS	TS	1

Table 4. 8085A Machine State Chart

Machine State	Status & Buses				Control		
	S1,S0	IO/M	A_8-A_{15}	AD_0-AD_7	RD WR	INTA	ALE
T_1	X	X	X	X	1	1	1*
T_2	X	X	X	X	X	X	0
T_{WAIT}	X	X	X	X	X	X	0
T_3	X	X	X	X	X	X	0
T_4	1	0†	X	TS	1	1	0
T_5	1	0†	X	TS	1	1	0
T_6	1	0†	X	TS	1	1	0
T_{RESET}	X	TS	TS	TS	TS	1	0
T_{HALT}	0	TS	TS	TS	TS	1	0
T_{HOLD}	X	TS	TS	TS	TS	1	0

0 = Logic "0"
1 = Logic "1"
TS = High Impedance
X = Unspecified

* ALE not generated during 2nd and 3rd machine cycles of DAD instruction
† IO/M = 1 during T_4-T_6 of INA machine cycle

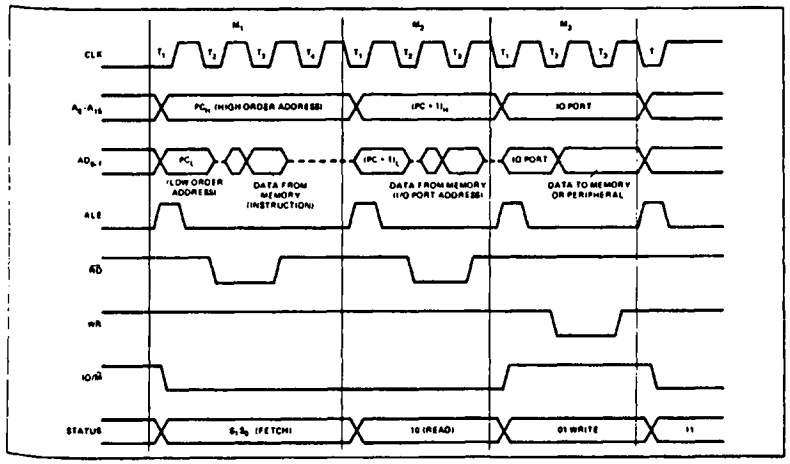


Figure 9. 8085A Basic System Timing

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . −0.5V to +7V
Power Dissipation . . . . . 1.5 Watt

*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 0V ±5%, V_{SS} = 0V; unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{CC}	Power Supply Current		170	mA	
I_{IL}	Input Leakage		±10	μA	$0 \le V_{IN} \le V_{CC}$
I_{LO}	Output Leakage		±10	μA	$0.45V \le V_{out} \le V_{CC}$
V_{ILR}	Input Low Level, RESET	-0.5	+0.8	V	
V_{IHR}	Input High Level, RESET	2.4	V_{CC}+0.5	V	
V_{HY}	Hysteresis, RESET	0.25		V	

A.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 0V ±5%, V_{SS} = 0V)

Symbol	Parameter	8085A[2]		8085A-2[2]		Units
		Min.	Max.	Min.	Max.	
t_{CYC}	CLK Cycle Period	320	2000	200	2000	ns
t_1	CLK Low Time (Standard CLK Loading)	80		40		ns
t_2	CLK High Time (Standard CLK Loading)	120		70		ns
t_r, t_f	CLK Rise and Fall Time		30		30	ns
t_{XKR}	X_1 Rising to CLK Rising	30	120	30	100	ns
t_{XKF}	X_1 Rising to CLK Falling	30	150	30	110	ns
t_{AC}	A_{8-15} Valid to Leading Edge of Control[1]	270		115		ns
t_{ACL}	A_{0-7} Valid to Leading Edge of Control	240		115		ns
t_{AD}	A_{0-15} Valid to Valid Data In		575		350	ns
t_{AFR}	Address Float After Leading Edge of READ (INTA)		0		0	ns
t_{AL}	A_{8-15} Valid Before Trailing Edge of ALE[1]	115		50		ns
t_{ALL}	A_{0-7} Valid Before Trailing Edge of ALE	90		50		ns
t_{ARY}	READY Valid from Address Valid		220		100	ns
t_{CA}	Address (A_{8-15}) Valid After Control	120		60		ns
t_{CC}	Width of Control Low (RD, WR, INTA) Edge of ALE	400		230		ns
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	50		25		ns
t_{DW}	Data Valid to Trailing Edge of WRITE	420		230		ns
t_{HABE}	HLDA to Bus Enable		210		150	ns
t_{HABF}	Bus Float After HLDA		210		150	ns
t_{HACK}	HLDA Valid to Trailing Edge of CLK	110		40		ns
t_{HDH}	HOLD Hold Time	0		0		ns
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	170		120		ns
t_{INH}	INTR Hold Time	0		0		ns
t_{INS}	INTR, RST, and TRAP Setup Time to Falling Edge of CLK	160		150		ns
t_{LA}	Address Hold Time After ALE	100		50		ns
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	130		60		ns
t_{LCK}	ALE Low During CLK High	100		50		ns
t_{LDR}	ALE to Valid Data During Read		460		270	ns
t_{LDW}	ALE to Valid Data During Write		200		120	ns
t_{LL}	ALE Width	140		80		ns
t_{LRY}	ALE to READY Stable		110		30	ns

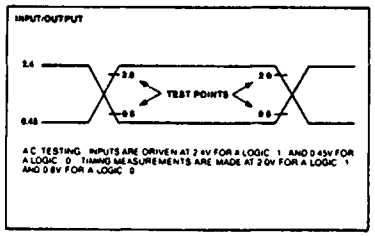
A.C. CHARACTERISTICS (Continued)

Symbol	Parameter	8085A[2]		8085A-2[2]		Units
		Min.	Max.	Min.	Max.	
t_{RAE}	Trailing Edge of $\overline{READ}$ to Re-Enabling of Address	150		90		ns
t_{RD}	$\overline{READ}$ (or $\overline{INTA}$) to Valid Data		300		150	ns
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	400		220		ns
t_{RDH}	Data Hold Time After $\overline{READ}$ $\overline{INTA}$[7]	0		0		ns
t_{RYH}	READY Hold Time	0		0		ns
t_{RYS}	READY Setup Time to Leading Edge of CLK	110		100		ns
t_{WD}	Data Valid After Trailing Edge of $\overline{WRITE}$	100		60		ns
t_{WDL}	LEADING Edge of WRITE to Data Valid		40		20	ns

NOTES:

1. A_8-A_{15} address Specs apply to IO/$\overline{M}$, S_0, and S_1 except A_8-A_{15} are undefined during T_4-T_6 of OF cycle whereas IO/$\overline{M}$, S_0, and S_1 are stable
2. Test conditions: t_{CYC} = 320 ns (8085A)/200 ns (8085A-2), C_L = 150 pF.
3. For all output timing where C_L = 150 pF use the following correction factors:
   25 pF ≤ C_L < 150 pF: −0.10 ns/pF
   150 pF < C_L ≤ 300 pF: +0.30 ns/pF
4. Output timings are measured with purely capacitive load
5. All timings are measured at output votage V_L = 0.8V, V_H = 2.0V, and 1.5V with 20 ns rise and fall time on inputs.
6. To calculate timing specifications at other values of t_{CYC} use Table 7.
7. Data hold time is guaranteed under all loading conditions.

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING LOAD CIRCUIT

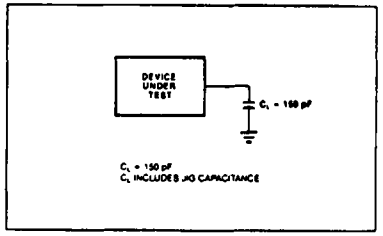


Table 5. Bus Timing Specification as a T_{CYC} Dependent

8085A			
t_{AL}	–	(1/2) T - 45	MIN
t_{LA}	–	(1/2) T - 60	MIN
t_{LL}	–	(1/2) T - 20	MIN
t_{LCK}	–	(1/2) T - 60	MIN
t_{LC}	–	(1/2) T - 30	MIN
t_{AD}	–	(5/2 + N) T - 225	MAX
t_{RD}	–	(3/2 + N) T - 180	MAX
t_{RAE}	–	(1/2) T - 10	MIN
t_{CA}	–	(1/2) T - 40	MIN
t_{DW}	–	(3/2 + N) T - 60	MIN
t_{WD}	–	(1/2) T - 60	MIN
t_{CC}	–	(3/2 + N) T - 80	MIN
t_{CL}	–	(1/2) T - 110	MIN
t_{ARY}	–	(3/2) T - 260	MAX
t_{HACK}	–	(1/2) T - 50	MIN
t_{HABF}	–	(1/2) T + 50	MAX
t_{HABE}	–	(1/2) T + 50	MAX
t_{AC}	–	(2/2) T - 50	MIN
t_1	–	(1/2) T - 80	MIN
t_2	–	(1/2) T - 40	MIN
t_{RV}	–	(3/2) T - 80	MIN
t_{LDR}	–	(4/2) T - 180	MAX

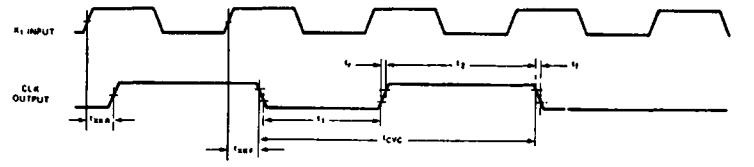
NOTE: N is equal to the total WAIT states.
T = t_{CYC}.

8085A-2			
t_{AL}	–	(1/2) T - 50	MIN
t_{LA}	–	(1/2) T - 50	MIN
t_{LL}	–	(1/2) T - 20	MIN
t_{LCK}	–	(1/2) T - 50	MIN
t_{LC}	–	(1/2) T - 40	MIN
t_{AD}	–	(5/2 + N) T - 150	MAX
t_{RD}	–	(3/2 + N) T - 150	MAX
t_{RAE}	–	(1/2) T - 10	MIN
t_{CA}	–	(1/2) T - 40	MIN
t_{DW}	–	(3/2 + N) T - 70	MIN
t_{WD}	–	(1/2) T - 40	MIN
t_{CC}	–	(3/2 + N) T - 70	MIN
t_{CL}	–	(1/2) T - 75	MIN
t_{ARY}	–	(3/2) T - 200	MAX
t_{HACK}	–	(1/2) T - 60	MIN
t_{HABF}	–	(1/2) T + 50	MAX
t_{HABE}	–	(1/2) T + 60	MAX
t_{AC}	–	(2/2) T - 85	MIN
t_1	–	(1/2) T - 60	MIN
t_2	–	(1/2) T - 30	MIN
t_{RV}	–	(3/2) T - 80	MIN
t_{LDR}	–	(4/2) T - 130	MAX

NOTE: N is equal to the total WAIT states.
T = t_{CYC}.

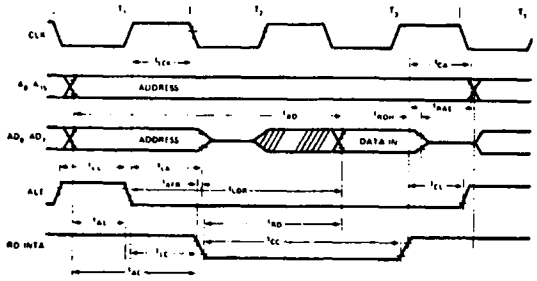
WAVEFORMS

CLOCK

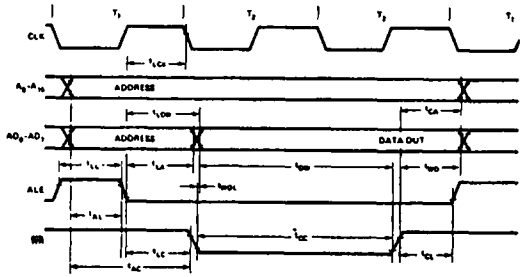


WAVEFORMS (Continued)

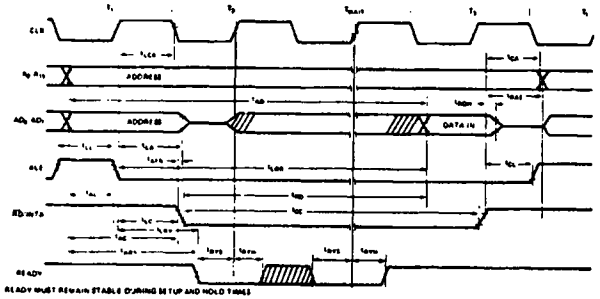
READ



WRITE

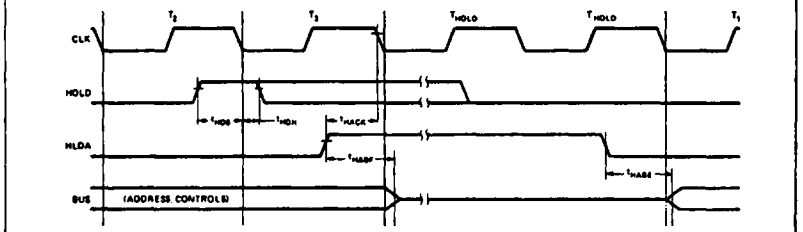


READ OPERATION WITH WAIT CYCLE (TYPICAL) — SAME READY TIMING APPLIES TO WRITE



WAVEFORMS (Continued)

HOLD



INTERRUPT AND HOLD

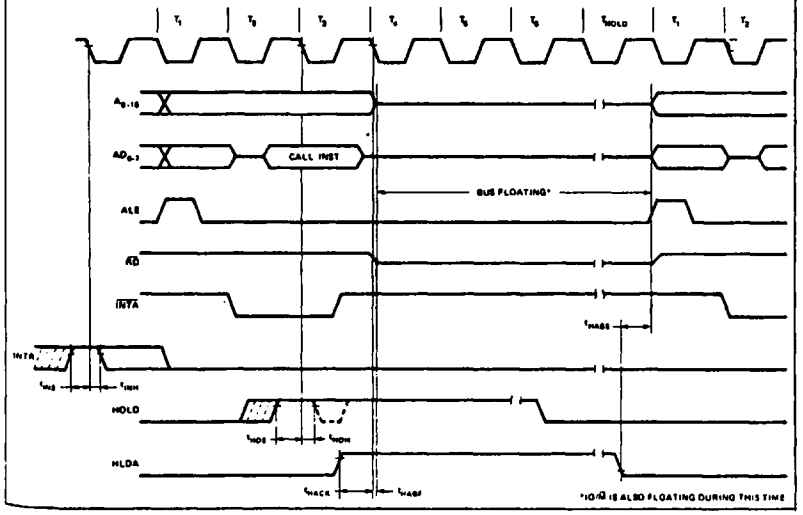


Table 6. Instruction Set Summary

Mnemonic	Instruction Code D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Operations Description
MOVE, LOAD, AND STORE		
MOV r1 r2	0 1 D D D S S S	Move register to register
MOV M r	0 1 1 1 0 S S S	Move register to memory
MOV r M	0 1 D D D 1 1 0	Move memory to register
MVI r	0 0 D D D 1 1 0	Move immediate register
MVI M	0 0 1 1 0 1 1 0	Move immediate memory
LXI B	0 0 0 0 0 0 0 1	Load immediate register Pair B & C
LXI D	0 0 0 1 0 0 0 1	Load immediate register Pair D & E
LXI H	0 0 1 0 0 0 0 1	Load immediate register Pair H & L
STAX B	0 0 0 0 0 0 1 0	Store A indirect
STAX D	0 0 0 1 0 0 1 0	Store A indirect
LDAX B	0 0 0 0 1 0 1 0	Load A indirect
LDAX D	0 0 0 1 1 0 1 0	Load A indirect
STA	0 0 1 1 0 0 1 0	Store A direct
LDA	0 0 1 1 1 0 1 0	Load A direct
SHLD	0 0 1 0 0 0 1 0	Store H & L direct
LHLD	0 0 1 0 1 0 1 0	Load H & L direct
XCHG	1 1 1 0 1 0 1 1	Exchange D & E, H & L Registers
STACK OPS		
PUSH B	1 1 0 0 0 1 0 1	Push register Pair B & C on stack
PUSH D	1 1 0 1 0 1 0 1	Push register Pair D & E on stack
PUSH H	1 1 1 0 0 1 0 1	Push register Pair H & L on stack
PUSH PSW	1 1 1 1 0 1 0 1	Push A and Flags on stack
POP B	1 1 0 0 0 0 0 1	Pop register Pair B & C off stack
POP D	1 1 0 1 0 0 0 1	Pop register Pair D & E off stack
POP H	1 1 1 0 0 0 0 1	Pop register Pair H & L off stack
POP PSW	1 1 1 1 0 0 0 1	Pop A and Flags off stack
XTHL	1 1 1 0 0 0 1 1	Exchange top of stack, H & L
SPHL	1 1 1 1 1 0 0 1	H & L to stack pointer
LXI SP	0 0 1 1 0 0 0 1	Load immediate stack pointer
INX SP	0 0 1 1 0 0 1 1	Increment stack pointer
DCX SP	0 0 1 1 1 0 1 1	Decrement stack pointer
JUMP		
JMP	1 1 0 0 0 0 1 1	Jump unconditional
JC	1 1 0 1 1 0 1 0	Jump on carry
JNC	1 1 0 1 0 0 1 0	Jump on no carry
JZ	1 1 0 0 1 0 1 0	Jump on zero
JNZ	1 1 0 0 0 0 1 0	Jump on no zero
JP	1 1 1 1 0 0 1 0	Jump on positive
JM	1 1 1 1 1 0 1 0	Jump on minus
JPE	1 1 1 0 1 0 1 0	Jump on parity even
JPO	1 1 1 0 0 0 1 0	Jump on parity odd
PCHL	1 1 1 0 1 0 0 1	H & L to program counter
CALL		
CALL	1 1 0 0 1 1 0 1	Call unconditional
CC	1 1 0 1 1 1 0 0	Call on carry
CNC	1 1 0 1 0 1 0 0	Call on no carry
CZ	1 1 0 0 1 1 0 0	Call on zero
CNZ	1 1 0 0 0 1 0 0	Call on no zero
CP	1 1 1 1 0 1 0 0	Call on positive
CM	1 1 1 1 1 1 0 0	Call on minus
CPE	1 1 1 0 1 1 0 0	Call on parity even
CPO	1 1 1 0 0 1 0 0	Call on parity odd
RETURN		
RET	1 1 0 0 1 0 0 1	Return
RC	1 1 0 1 1 0 0 0	Return on carry
RNC	1 1 0 1 0 0 0 0	Return on no carry
RZ	1 1 0 0 1 0 0 0	Return on zero
RNZ	1 1 0 0 0 0 0 0	Return on no zero
RP	1 1 1 1 0 0 0 0	Return on positive
RM	1 1 1 1 1 0 0 0	Return on minus
RPE	1 1 1 0 1 0 0 0	Return on parity even
RPO	1 1 1 0 0 0 0 0	Return on parity odd
RESTART		
RST	1 1 A A A 1 1 1	Restart
INPUT/OUTPUT		
IN	1 1 0 1 1 0 1 1	Input
OUT	1 1 0 1 0 0 1 1	Output
INCREMENT AND DECREMENT		
INR r	0 0 D D D 1 0 0	Increment register
DCR r	0 0 D D D 1 0 1	Decrement register
INR M	0 0 1 1 0 1 0 0	Increment memory
DCR M	0 0 1 1 0 1 0 1	Decrement memory
INX B	0 0 0 0 0 0 1 1	Increment B & C registers
INX D	0 0 0 1 0 0 1 1	Increment D & E registers
INX H	0 0 1 0 0 0 1 1	Increment H & L registers
DCX B	0 0 0 0 1 0 1 1	Decrement B & C
DCX D	0 0 0 1 1 0 1 1	Decrement D & E
DCX H	0 0 1 0 1 0 1 1	Decrement H & L
ADD		
ADD r	1 0 0 0 0 S S S	Add register to A
ADC r	1 0 0 0 1 S S S	Add register to A with carry
ADD M	1 0 C 0 0 1 1 0	Add memory to A
ADC M	1 0 0 0 1 1 1 0	Add memory to A with carry
ADI	1 1 0 0 0 1 1 0	Add immediate to A
ACI	1 1 0 0 1 1 1 0	Add immediate to A with carry
DAD B	0 0 0 0 1 0 0 1	Add B & C to H & L
DAD D	0 0 0 1 1 0 0 1	Add D & E to H & L
DAD H	0 0 1 0 1 0 0 1	Add H & L to H & L
DAD SP	0 0 1 1 1 0 0 1	Add stack pointer to H & L
SUBTRACT		
SUB r	1 0 0 1 0 S S S	Subtract register from A
SBB r	1 0 0 1 1 S S S	Subtract register from A with borrow
SUB M	1 0 0 1 0 1 1 0	Subtract memory from A
SBB M	1 0 0 1 1 1 1 0	Subtract memory from A with borrow
SUI	1 1 0 1 0 1 1 0	Subtract immediate from A
SBI	1 1 0 1 1 1 1 0	Subtract immediate from A with borrow

Table 6-1. Instruction Set Summary (Cont'd)

Mnemonic	Instruction Code D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Operations Description
LOGICAL		
ANA r	1 0 1 0 0 S S S	And register with A
XRA r	1 0 1 0 1 S S S	Exclusive OR register with A
ORA r	1 0 1 1 0 S S S	OR register with A
CMP r	1 0 1 1 1 S S S	Compare register with A
ANA M	1 0 1 0 0 1 1 0	And memory with A
XRA M	1 0 1 0 1 1 1 0	Exclusive OR memory with A
ORA M	1 0 1 1 0 1 1 0	OR memory with A
CMP M	1 0 1 1 1 1 1 0	Compare memory with A
ANI	1 1 1 0 0 1 1 0	And immediate with A
XRI	1 1 1 0 1 1 1 0	Exclusive OR immediate with A
ORI	1 1 1 1 0 1 1 0	OR immediate with A
CPI	1 1 1 1 1 1 1 0	Compare immediate with A
ROTATE		
RLC	0 0 0 0 0 1 1 1	Rotate A left
RRC	0 0 0 0 1 1 1 1	Rotate A right
RAL	0 0 0 1 0 1 1 1	Rotate A left through carry
RAR	0 0 0 1 1 1 1 1	Rotate A right through carry

Mnemonic	Instruction Code D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Operations Description
SPECIALS		
CMA	0 0 1 0 1 1 1 1	Complement A
STC	0 0 1 1 0 1 1 1	Set carry
CMC	0 0 1 1 1 1 1 1	Complement carry
DAA	0 0 1 0 0 1 1 1	Decimal adjust A
CONTROL		
EI	1 1 1 1 1 0 1 1	Enable interrupts
DI	1 1 1 1 0 0 1 1	Disable interrupt
NOP	0 0 0 0 0 0 0 0	No-operation
HLT	0 1 1 1 0 1 1 0	Halt
NEW 8085A INSTRUCTIONS		
RIM	0 0 1 0 0 0 0 0	Read Interrupt Mask
SIM	0 0 1 1 0 0 0 0	Set Interrupt Mask

NOTES:
1. DDS or SSS: B 000, C 001, D 010, E011, H 100, L 101, Memory 110, A 111.
2. Two possible cycle times (6/12) indicate instruction cycles dependent on condition flags.

intel

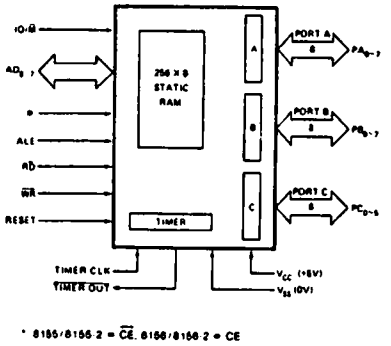
8155/8156/8155-2/8156-2
2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

- 256 Word x 8 Bits
- Single +5V Power Supply
- Completely Static Operation
- Internal Address Latch
- 2 Programmable 8 Bit I/O Ports
- 1 Programmable 6-Bit I/O Port
- Programmable 14-Bit Binary Counter/Timer
- Compatible with 8085A and 8088 CPU
- Multiplexed Address and Data Bus
- 40 Pin DIP

The 8155 and 8156 are RAM and I/O chips to be used in the 8085A and 8088 microprocessor systems. The RAM portion is designed with 2048 static cells organized as 256 x 8. They have a maximum access time of 400 ns to permit use with no wait states in 8085A CPU. The 8155-2 and 8156-2 have maximum access times of 330 ns for use with the 8085A-2 and the full speed 5 MHz 8088 CPU.

The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.



* 8155/8156-2 = $\overline{CE}$, 8156/8156-2 = CE

Figure 1. Block Diagram

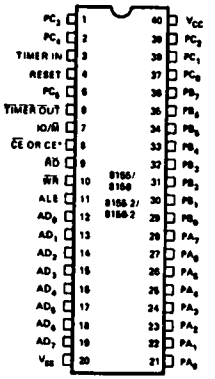


Figure 2. Pin Configuration

Table 1. Pin Description

Symbol	Type	Name and Function
RESET	I	**Reset:** Pulse provided by the 8085A to initialize the system (connect to 8085A RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two 8085A clock cycle times.
AD_{0-7}	I/O	**Address/Data:** 3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside the 8155/86 on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/$\overline{M}$ input. The 8-bit data is either written into the chip or read from the chip, depending on the $\overline{WR}$ or $\overline{RD}$ input signal.
CE or $\overline{CE}$	I	**Chip Enable:** On the 8155, this pin is $\overline{CE}$ and is ACTIVE LOW. On the 8156, this pin is CE and is ACTIVE HIGH.
$\overline{RD}$	I	**Read Control:** Input low on this line with the Chip Enable active enables and AD_{0-7} buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.
$\overline{WR}$	I	**Write Control:** Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register, depending on IO/$\overline{M}$.
ALE	I	**Address Latch Enable:** This control signal latches both the address on the AD_{0-7} lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.
IO/$\overline{M}$	I	**I/O Memory:** Selects memory if low and I/O and command/status registers if high.
PA_{0-7}(8)	I/O	**Port A:** These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PB_{0-7}(8)	I/O	**Port B:** These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PC_{0-5}(6)	I/O	**Port C:** These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PC_{0-5} are used as control signals, they will provide the following: PC_0 — A INTR (Port A Interrupt) PC_1 — $\overline{A}$BF (Port A Buffer Full) PC_2 — $\overline{A}$ $\overline{STB}$ (Port A Strobe) PC_3 — B INTR (Port B Interrupt) PC_4 — $\overline{B}$ BF (Port B Buffer Full) PC_5 — $\overline{B}$ $\overline{STB}$ (Port B Strobe)
TIMER IN	I	**Timer Input:** Input to the counter-timer.
TIMER OUT	O	**Timer Output:** This output can be either a square wave or a pulse, depending on the timer mode.
V_{CC}		**Voltage:** +5 volt supply
V_{SS}		**Ground:** Ground reference.

FUNCTIONAL DESCRIPTION

The 8155/8156 contains the following:

- 2k Bit Static RAM organized as 256 x 8
- Two 8-bit I/O ports (PA & PB) and one 6-bit I/O port (PC)
- 14-bit timer-counter

The IO/$\overline{M}$ (IO/Memory Select) pin selects either the five registers (Command, Status, PA_{0-7}, PB_{0-7}, PC_{0-5}) or the memory (RAM) portion.

The 8-bit address on the Address/Data lines, Chip Enable input CE or $\overline{CE}$, and IO/$\overline{M}$ are all latched on-chip at the falling edge of ALE.

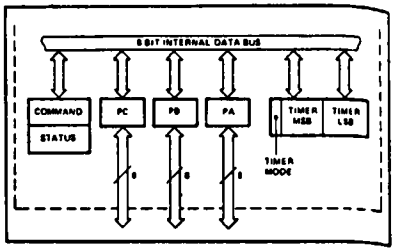


Figure 3. 8155/8156 Internal Registers

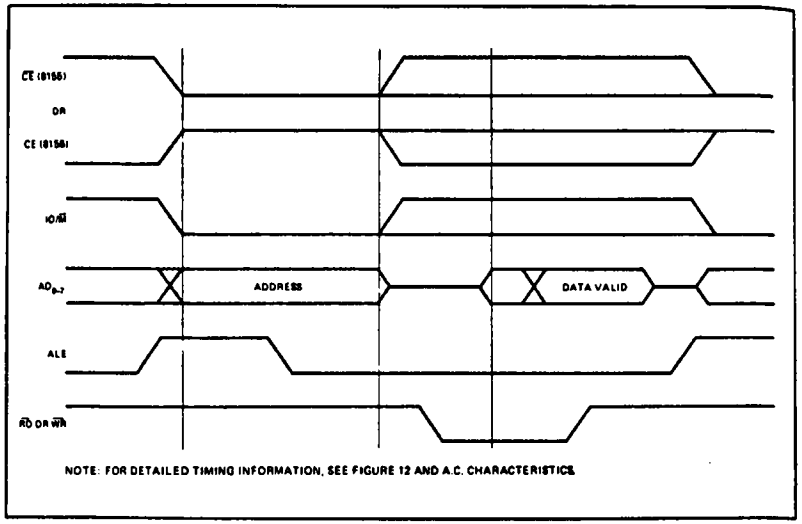


Figure 4. 8155/8156 On-Board Memory Read/Write Cycle

PROGRAMMING OF THE COMMAND REGISTER

The command register consists of eight latches. Four bits (0-3) define the mode of the ports, two bits (4-5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6-7) are for the timer.

The command register contents can be altered at any time by using the I/O address XXXXX000 during a WRITE operation with the Chip Enable active and IO/$\overline{M}$ = 1. The meaning of each bit of the command byte is defined in Figure 5. The contents of the command register may never be read.

READING THE STATUS REGISTER

The status register consists of seven latches, one for each bit; six (0-5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the Status Register (Address XXXXX000). Status word format is shown in Figure 6. Note that you may never write to the status register since the command register shares the same I/O address and the command register is selected when a write to that address is issued.

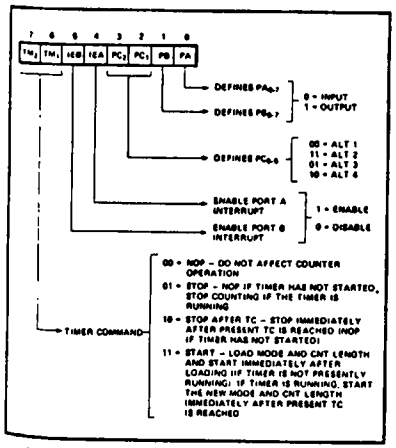


Figure 5. Command Register Bit Assignment

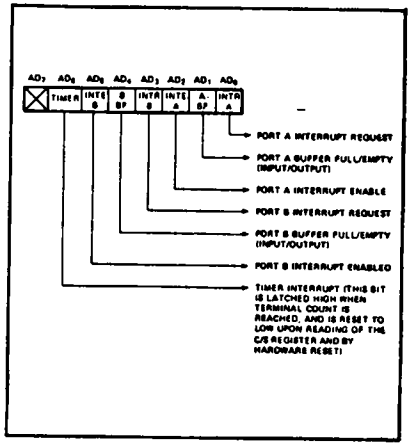


Figure 6. Status Register Bit Assignment

INPUT/OUTPUT SECTION

The I/O section of the 8155/8156 consists of five registers: (See Figure 7.)

- **Command/Status Register (C/S)** — Both registers are assigned the address XXXXX000. The C/S address serves the dual purpose.

  When the C/S registers are selected during WRITE operation, a command is written into the command register. The contents of this register are *not* accessible through the pins.

  When the C/S (XXXXX000) is selected during a READ operation, the status information of the I/O ports and the timer becomes available on the AD_{0-7} lines.

- **PA Register** — This register can be programmed to be either input or output ports depending on the status of the contents of the C/S Register. Also depending on the command, this port can operate in either the basic mode or the strobed mode (See timing diagram). The I/O pins assigned in relation to this register are PA_{0-7}. The address of this register is XXXXX001.

- **PB Register** — This register functions the same as PA Register. The I/O pins assigned are PB_{0-7}. The address of this register is XXXXX010.

- **PC Register** — This register has the address XXXXX011 and contains only 6 bits. The 6 bits can be programmed to be either input ports, output ports or as control signals for PA and PB by properly programming the AD_2 and AD_3 bits of the C/S register.

  When PC_{0-5} is used as a control port, 3 bits are assigned for Port A and 3 for Port B. The first bit is an interrupt that the 8155 sends out. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode. (See Table 2.)

When the 'C' port is programmed to either ALT3 or ALT4, the control signals for PA and PB are initialized as follows:

CONTROL	INPUT MODE	OUTPUT MODE
BF	Low	Low
INTR	Low	High
STB	Input Control	Input Control

I/O ADDRESS*								SELECTION
A7	A6	A5	A4	A3	A2	A1	A0	
X	X	X	X	X	0	0	0	Internal Command/Status Register
X	X	X	X	X	0	0	1	General Purpose I/O Port A
X	X	X	X	X	0	1	0	General Purpose I/O Port B
X	X	X	X	X	0	1	1	Port C — General Purpose I/O or Control
X	X	X	X	X	1	0	0	Low-Order 8 bits of Timer Count
X	X	X	X	X	1	0	1	High 6 bits of Timer Count and 2 bits of Timer Mode

X Don't Care

* I/O Address must be qualified by CE = 1 (8156) or $\overline{CE}$ = 0 (8155) and IO/$\overline{M}$ = 1 in order to select the appropriate register

Figure 7. I/O Port and Timer Addressing Scheme

Figure 8 shows how I/O PORTS A and B are structured within the 8155 and 8156:

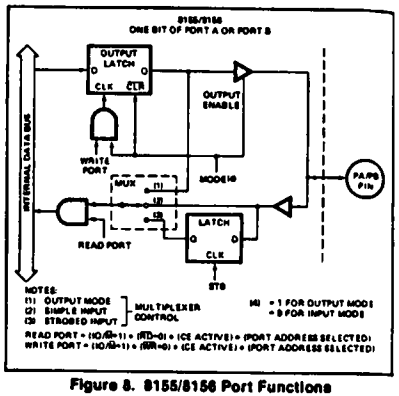


Figure 8. 8155/8156 Port Functions

Table 2. Port Control Assignment

Pin	ALT 1	ALT 2	ALT 3	ALT 4
PC0	Input Port	Output Port	A INTR (Port A Interrupt)	A INTR (Port A Interrupt)
PC1	Input Port	Output Port	A BF (Port A Buffer Full)	A BF (Port A Buffer Full)
PC2	Input Port	Output Port	A $\overline{STB}$ (Port A Strobe)	A $\overline{STB}$ (Port A Strobe)
PC3	Input Port	Output Port	Output Port	B INTR (Port B Interrupt)
PC4	Input Port	Output Port	Output Port	B BF (Port B Buffer Full)
PC5	Input Port	Output Port	Output Port	B $\overline{STB}$ (Port B Strobe)

Note in the diagram that when the I/O ports are programmed to be output ports, the contents of the output ports can still be read by a READ operation when appropriately addressed.

The outputs of the 8155/8156 are "glitch-free" meaning that you can write a "1" to a bit position that was previously "1" and the level at the output pin will not change.

Note also that the output latch is cleared when the port enters the input mode. The output latch cannot be loaded by writing to the port if the port is in the input mode. The result is that each time a port mode is changed from input to output, the output pins will go low. When the 8155/56 is RESET, the output latches are all cleared and all 3 ports enter the input mode.

When in the ALT 1 or ALT 2 modes, the bits of PORT C are structured like the diagram above in the simple input or output mode, respectively.

Reading from an input port with nothing connected to the pins will provide unpredictable results.

Figure 9 shows how the 8155/8156 I/O ports might be configured in a typical MCS-85 system.

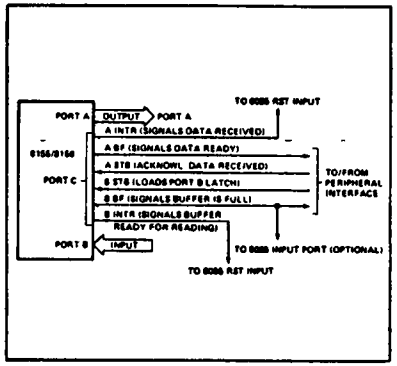


Figure 9. Example: Command Register = 00111001

TIMER SECTION

The timer is a 14-bit down-counter that counts the TIMER IN pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register (See Figure 7.)

To program the timer, the COUNT LENGTH REG is loaded first, one byte at a time, by selecting the timer addresses. Bits 0-13 of the high order count register will specify the length of the next count and bits 14-15 of the high order register will specify the timer output mode (see Figure 10). The value loaded into the count length register can have any value from 2H through 3FFH in Bits 0–13.

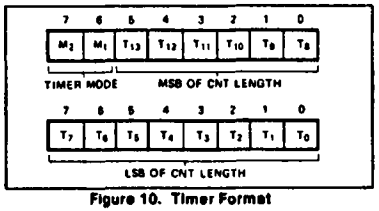


Figure 10. Timer Format

There are four modes to choose from: M2 and M1 define the timer mode, as shown in Figure 11.

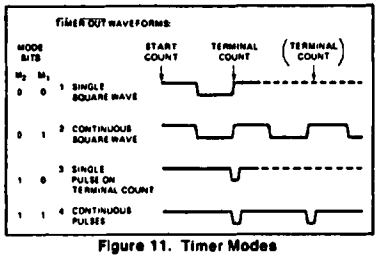


Figure 11. Timer Modes

Bits 6-7 TM_2 and TM_1 of command register contents are used to start and stop the counter. There are four commands to choose from:

TM_2	TM_1	
0	0	NOP — Do not affect counter operation.
0	1	STOP — NOP if timer has not started; stop counting if the timer is running.
1	0	STOP AFTER TC — Stop immediately after present TC is reached (NOP if timer has not started.
1	1	START — Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached.

Note that while the counter is counting, you may load a new count and mode into the count length registers. Before the new count and mode will be used by the counter, you must issue a START command to the counter. This applies even though you may only want to change the count and use the previous mode.

In case of an odd-numbered count, the first half-cycle of the squarewave output, which is high, is one count longer than the second (low) half-cycle, as shown in Figure 12.

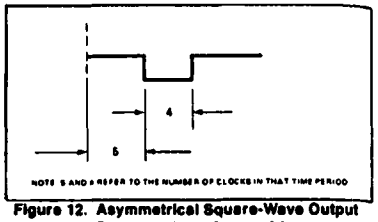


Figure 12. Asymmetrical Square-Wave Output Resulting from Count of 9

The counter in the 8155 is not initialized to any particular mode or count when hardware RESET occurs, but RESET does *stop* the counting. Therefore, counting cannot begin following RESET until a START command is issued via the C/S register.

Please note that the timer circuit on the 8155/8156 chip is designed to be a square-wave timer, not an event counter. To achieve this, it counts down by twos twice in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulses received. You cannot load an initial value of 1 into the count register and cause the timer to operate, as its terminal count value is 10 (binary) or 2 (decimal). (For the detection of single pulses, it is suggested that one of the hardware interrupt pins on the 8085A be used.) After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulses required to complete the timer cycle if desired. To obtain the remaining count, perform the following operations in order:

1. Stop the count
2. Read in the 16-bit value from the count length registers
3. Reset the upper two mode bits
4. Reset the carry and rotate right one position all 16 bits through carry
5. If carry is set, add 1/2 of the full original count (1/2 full count — 1 if full count is odd).

Note: If you started with an odd count and you read the count length register before the third count pulse occurs, you will not be able to discern whether one or two counts has occurred. Regardless of this, the 8155/56 always counts out the right number of pulses in generating the TIMER OUT waveforms.

EXAMPLE PROGRAM

Following is an actual sequence of program steps that adjusts the 8155/56 count register contents to obtain the count, extracted from Intel® Application Note AP38, "Application Techniques for the Intel 8085A Bus." First store the value of the full original count in register HL of the 8085A. Then stop the count to avoid getting an incorrect count value. Then sample the timer-counter, storing the lower-order byte of the current count register in register C and the higher-order count byte in register B. Then, call the following 8080A/8085A subroutine:

```
ADJUST, 78      MOV A,B     ;Load accumulator with upper half
                            ; of count.
      E63F      ANI 3F      ;Reset upper 2 bits and clear carry.
      1F        RAR         ;Rotate right through carry.
      47        MOV B,A     ;Store shifted value back in B.
      79        MOV A,C     ;Load accumulator with lower half.
      1F        RAR         ;Rotate right through carry.
      4F        MOV C,A     ;Store lower byte in C.
      D8        RNC         ;If in 2nd half of count, return.
                            ;If in 1st half, go on.
      3F        CMC         ;Clear carry.
      7C        MOV A,H     ;Divide full count by 2. (If HL
                            ;is odd, disregard remainder.)
      1F        RAR
      67        MOV H,A
      7D        MOV A,L
      1F        RAR
      6F        MOV L,A
      09        DAD B       ;Double-precision add HL and BC.
      44        MOV B,H     ;Store results back in BC.
      4D        MOV C,L
      C9        RET         ;Return.
```

After executing the subroutine, BC will contain the remaining count in the current count cycle.

8085A MINIMUM SYSTEM CONFIGURATION

Figure 13a shows a minimum system using three chips, containing:

- 256 Bytes RAM
- 2K Bytes ROM
- 38 I/O Pins
- 1 Interval Timer
- 4 Interrupt Levels

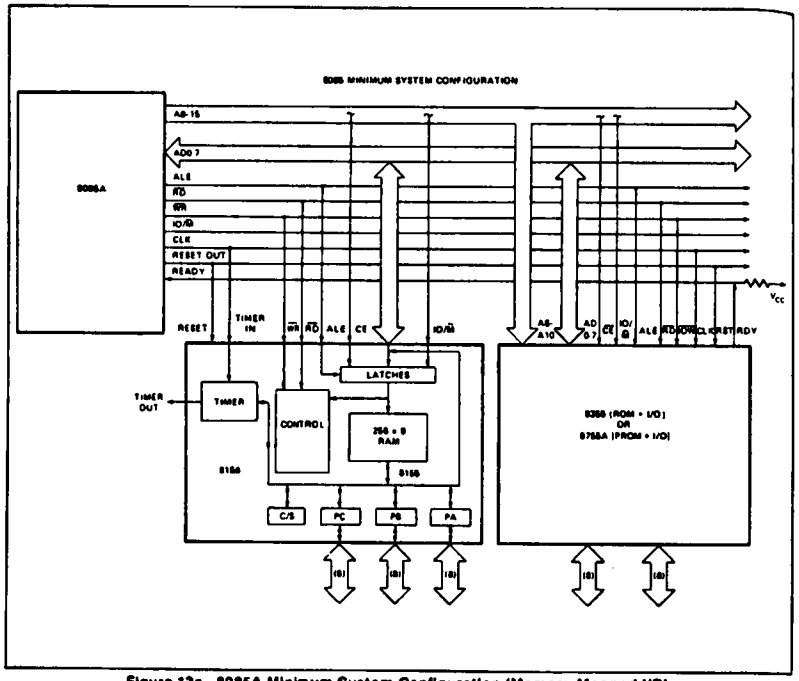


Figure 13a. 8085A Minimum System Configuration (Memory Mapped I/O)

8088 FIVE CHIP SYSTEM

Figure 13b shows a five chip system containing:

- 1.25K Bytes RAM
- 2K Bytes ROM
- 38 I/O Pins
- 1 Interval Timer
- 2 Interrupt Levels

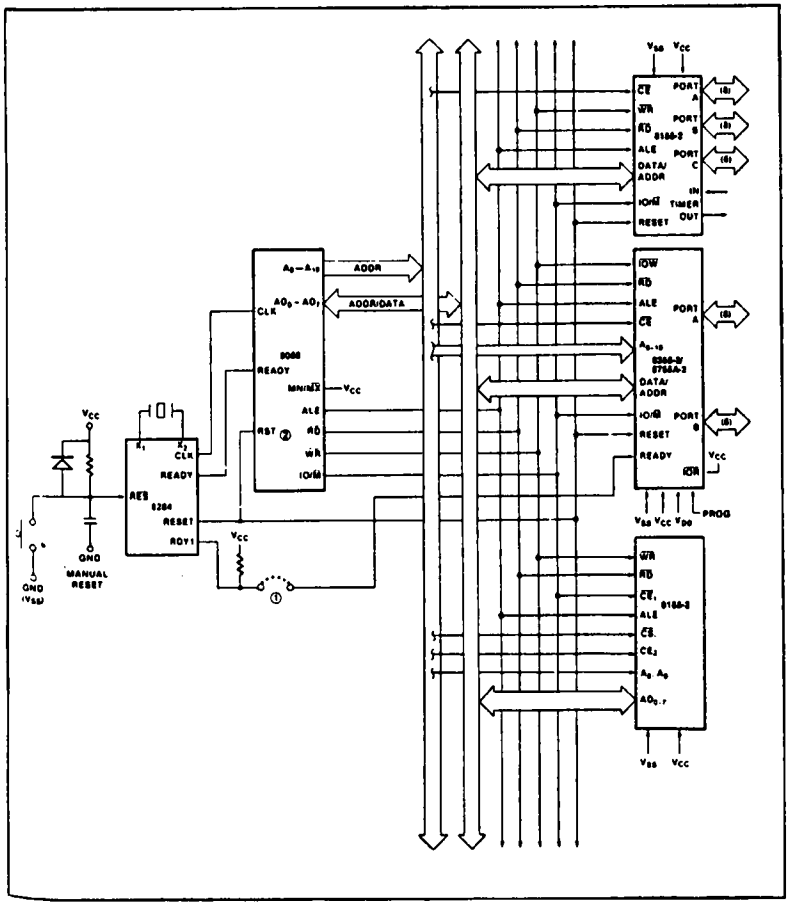


Figure 13b. 8088 Five Chip System Configuration

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	1.5W

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

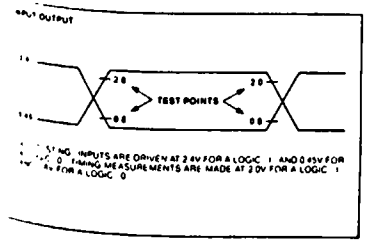
SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{IL}	Input Leakage		±10	μA	0V ≤ V_{IN} ≤ V_{CC}
I_{LO}	Output Leakage Current		± 10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
I_{CC}	V_{CC} Supply Current		180	mA	
I_{IL} (CE)	Chip Enable Leakage 8155 8156		 +100 -100	 μA μA	 0V ≤ V_{IN} ≤ V_{CC}

AFN-00201C

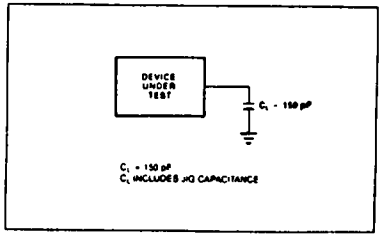
A.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

		8155/8156		8155-2/8156-2		
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	UNITS
t_{AL}	Address to Latch Set Up Time	50		30		ns
t_{LA}	Address Hold Time after Latch	80		30		ns
t_{LC}	Latch to READ/WRITE Control	100		40		ns
t_{RD}	Valid Data Out Delay from READ Control		170		140	ns
t_{AD}	Address Stable to Data Out Valid		400		330	ns
t_{LL}	Latch Enable Width	100		70		ns
t_{RDF}	Data Bus Float After READ	0	100	0	80	ns
t_{CL}	READ/WRITE Control to Latch Enable	20		10		ns
t_{CC}	READ/WRITE Control Width	250		200		ns
t_{DW}	Data In to WRITE Set Up Time	150		100		ns
t_{WD}	Data In Hold Time After WRITE	0		0		ns
t_{RV}	Recovery Time Between Controls	300		200		ns
t_{WP}	WRITE to Port Output		400		300	ns
t_{PR}	Port Input Setup Time	70		50		ns
t_{RP}	Port Input Hold Time	50		10		ns
t_{SBF}	Strobe to Buffer Full		400		300	ns
t_{SS}	Strobe Width	200		150		ns
t_{RBE}	READ to Buffer Empty		400		300	ns
t_{SI}	Strobe to INTR On		400		300	ns
t_{RDI}	READ to INTR Off		400		300	ns
t_{PSS}	Port Setup Time to Strobe Strobe	50		0		ns
t_{PHS}	Port Hold Time After Strobe	120		100		ns
t_{SBE}	Strobe to Buffer Empty		400		300	ns
t_{WBF}	WRITE to Buffer Full		400		300	ns
t_{WI}	WRITE to INTR Off		400		300	ns
t_{TL}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ Low		400		300	ns
t_{TH}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ High		400		300	ns
t_{RDE}	Data Bus Enable from READ Control	10		10		ns
t_1	TIMER-IN Low Time	80		40		ns
t_2	TIMER-IN High Time	120		70		ns

A.C. TESTING INPUT, OUTPUT WAVEFORM



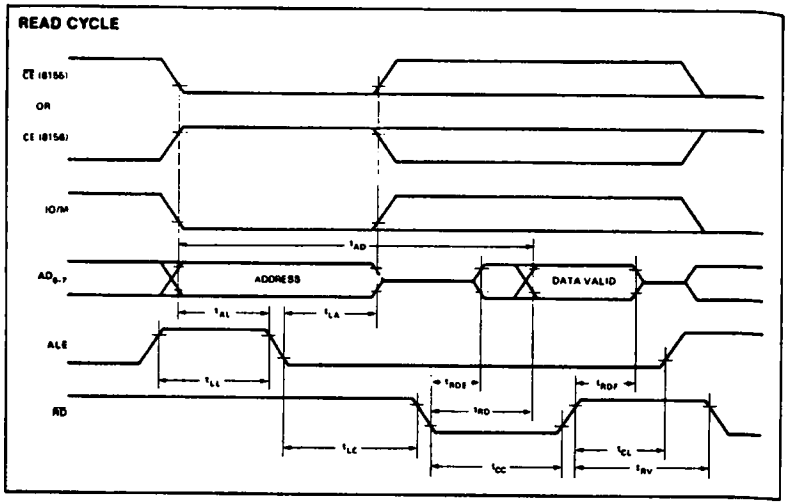
A.C. TESTING LOAD CIRCUIT



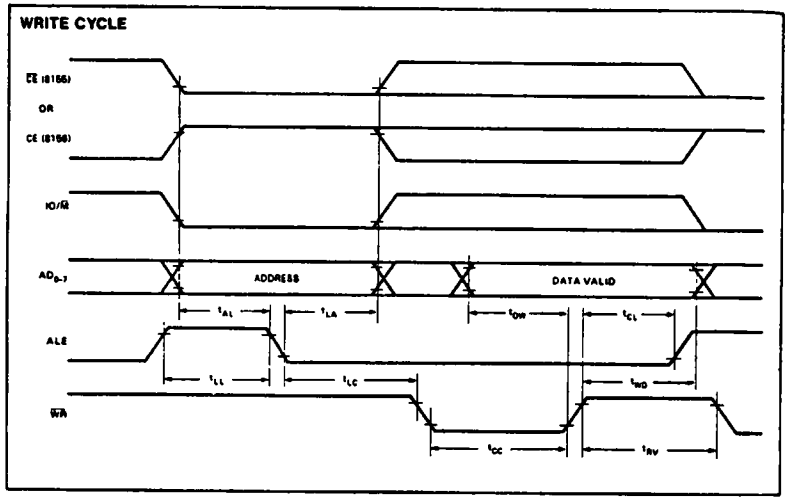
AFN-00201C

WAVEFORMS

READ CYCLE

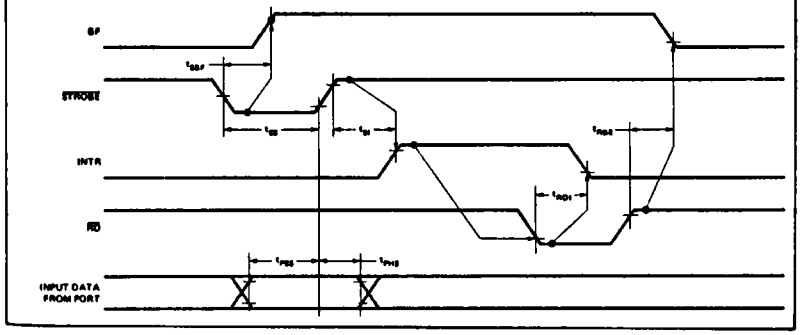


WRITE CYCLE

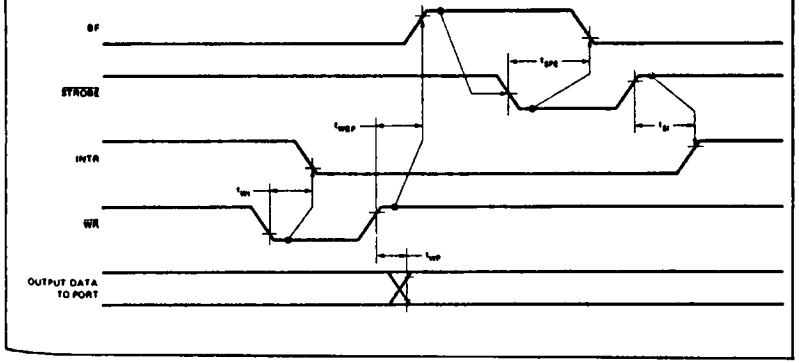


WAVEFORMS (Continued)

STROBED INPUT MODE



STROBED OUTPUT MODE



intel

8755A/8755A-2
16,384-BIT EPROM WITH I/O

- 2048 Words x 8 Bits
- Single +5V Power Supply (V_{CC})
- Directly Compatible with 8085A and 8088 Microprocessors
- U.V. Erasable and Electrically Reprogrammable
- Internal Address Latch
- 2 General Purpose 8-Bit I/O Ports
- Each I/O Port Line Individually Programmable as Input or Output
- Multiplexed Address and Data Bus
- 40-Pin DIP

The Intel® 8755A is an erasable and electrically reprogrammable ROM (EPROM) and I/O chip to be used in the 8085A and 8088 microprocessor systems. The EPROM portion is organized as 2048 words by 8 bits. It has a maximum access time of 450 ns to permit use with no wait states in an 8085A CPU.

The I/O portion consists of 2 general purpose I/O ports. Each I/O port has 8 port lines, and each I/O port line is individually programmable as input or output.

The 8755A-2 is a high speed selected version of the 8755A compatible with the 5 MHz 8085A-2 and the full speed 5 MHz 8088.

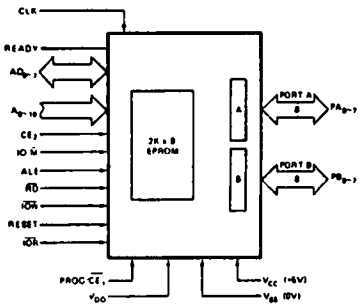


Figure 1. Block Diagram

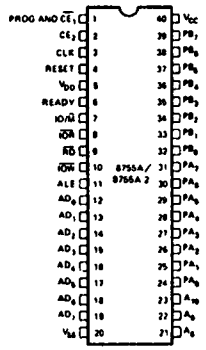


Figure 2. Pin Configuration

Table 1. Pin Description

Symbol	Type	Name and Function
ALE	I	**Address Latch Enable:** When Address Latch Enable goes *high*, AD_{0-7}, IO/M, A_{8-10}, CE_2, and $\overline{CE_1}$ enter the address latches. The signals (AD, IO/M, A_{8-10}, CE) are latched in at the trailing edge of ALE.
AD_{0-7}	I	**Bidirectional Address/Data Bus:** The lower 8-bits of the PROM or I/O address are applied to the bus lines when ALE is high. During an I/O cycle, Port A or B are selected based on the latched value of AD_0. If $\overline{RD}$ or $\overline{IOR}$ is low when the latched Chip Enables are active, the output buffers present data on the bus.
A_{8-10}	I	**Address:** These are the high order bits of the PROM address. They do not affect I/O operations.
PROG/$\overline{CE_1}$ CE_2	I	**Chip Enable Inputs:** $\overline{CE_1}$ is active low and CE_2 is active high. The 8755A can be accessed only when *both* Chip Enables are active at the time the ALE signal latches them up. If either Chip Enable input is not active, the AD_{0-7} and READY outputs will be in a high impedance state. $\overline{CE_1}$ is also used as a programming pin. (See section on programming.)
IO/$\overline{M}$	I	**I/O Memory:** If the latched IO/$\overline{M}$ is high when $\overline{RD}$ is low, the output data comes from an I/O port. If it is low the output data comes from the PROM.
$\overline{RD}$	I	**Read:** If the latched Chip Enables are active when $\overline{RD}$ goes low, the AD_{0-7} output buffers are enabled and output either the selected PROM location or I/O port. When both $\overline{RD}$ and $\overline{IOR}$ are high, the AD_{0-7} output buffers are 3-stated.
$\overline{IOW}$	I	**I/O Write:** If the latched Chip Enables are active, a low on $\overline{IOW}$ causes the output port pointed to by the latched value of AD_0 to be written with the data on AD_{0-7}. The state of IO/$\overline{M}$ is ignored.
CLK	I	**Clock:** The CLK is used to force the READY into its high impedance state after it has been forced low by $\overline{CE_1}$ low, CE_2 high, and ALE high.
READY	O	**Ready** is a 3-state output controlled by CE_2, $\overline{CE_1}$, ALE and CLK. READY is forced low when the Chip Enables are active during the time ALE is high, and remains low until the rising edge of the next CLK. (See Figure 6.)
PA_{0-7}	I/O	**Port A:** These are general purpose I/O pins. Their input/output direction is determined by the contents of Data Direction Register (DDR). Port A is selected for write operations when the Chip Enables are active and $\overline{IOW}$ is low and a 0 was previously latched from AD_0, AD_1. Read Operation is selected by either $\overline{IOR}$ low and active Chip Enables and AD_0 and AD_1 low, or IO/$\overline{M}$ high, $\overline{RD}$ low, active Chip Enables, and AD_0 and AD_1 low.
PB_{0-7}	I/O	**Port B:** This general purpose I/O port is identical to Port A except that it is selected by a 1 latched from AD_0 and a 0 from AD_1.
RESET	I	**Reset:** In normal operation, an input high on RESET causes all pins in Ports A and B to assume input mode (clear DDR register).
$\overline{IOR}$	I	**I/O Read:** When the Chip Enables are active, a low on $\overline{IOR}$ will output the selected I/O port onto the AD bus. $\overline{IOR}$ low performs the same function as the combination of IO/$\overline{M}$ high and $\overline{RD}$ low. When $\overline{IOR}$ is not used in a system, $\overline{IOR}$ should be tied to V_{CC} ("1").
V_{CC}		**Power:** +5 volt supply.
V_{SS}		**Ground:** Reference.
V_{DD}		**Power Supply:** V_{DD} is a programming voltage, and must be tied to V_{CC} when the 8755A is being read. For programming, a high voltage is supplied with V_{DD} = 25V, typical. (See section on programming.)

FUNCTIONAL DESCRIPTION

PROM Section

The 8755A contains an 8-bit address latch which allows it to interface directly to MCS-48, MCS-85 and iAPX 88/10 Microcomputers without additional hardware.

The PROM section of the chip is addressed by the 11-bit address and CE. The address $\overline{CE}_1$ and CE_2 are latched into the address latches on the falling edge of ALE. If the latched Chip Enables are active and IO/$\overline{M}$ is low when $\overline{RD}$ goes low, the contents of the PROM location addressed by the latched address are put out on the AD_{0-7} lines (provided that V_{DD} is tied to V_{CC}).

I/O Section

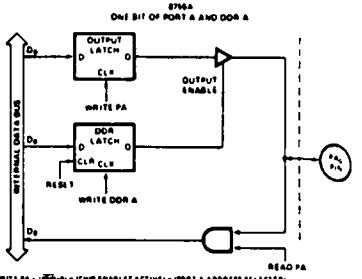
The I/O section of the chip is addressed by the latched value of AD_{0-1}. Two 8-bit Data Direction Registers (DDR) in 8755A determine the input/output status of each pin in the corresponding ports. A "0" in a particular bit position of a DDR signifies that the corresponding I/O port bit is in the input mode. A "1" in a particular bit position signifies that the corresponding I/O port bit is in the output mode. In this manner the I/O ports of the 8755A are bit-by-bit programmable as inputs or outputs. The table summarizes port and DDR designation. DDR's cannot be read.

AD_1	AD_0	Selection
0	0	Port A
0	1	Port B
1	0	Port A Data Direction Register (DDR A)
1	1	Port B Data Direction Register (DDR B)

When $\overline{IOW}$ goes low and the Chip Enables are active, the data on the AD is written into I/O port selected by the latched value of AD_{0-1}. During this operation all I/O bits of the selected port are affected, regardless of their I/O mode and the state of IO/$\overline{M}$. The actual output level does not change until $\overline{IOW}$ returns high (glitch free output).

A port can be read out when the latched Chip Enables are active and either $\overline{RD}$ goes low with IO/$\overline{M}$ high, or $\overline{IOR}$ goes low. Both input and output mode bits of a selected port will appear on lines AD_{0-7}.

To clarify the function of the I/O Ports and Data Direction Registers, the following diagram shows the configuration of one bit of PORT A and DDR A. The same logic applies to PORT B and DDR B.



Note that hardware RESET or writing a zero to the DDR latch will cause the output latch's output buffer to be disabled, preventing the data in the Output Latch from being passed through to the pin. This is equivalent to putting the port in the input mode. Note also that the data can be written to the Output Latch even though the Output Buffer has been disabled. This enables a port to be initialized with a value prior to enabling the output.

The diagram also shows that the contents of PORT A & PORT B can be read even when the ports are configured as outputs.

TABLE 1. 8755A PROGRAMMING MODULE CROSS REFERENCE

MODULE NAME	USE WITH
UPP 955	UPP(4)
UPP UP2(2)	UPP 855
PROMPT 975	PROMPT 80/85(3)
PROMPT 475	PROMPT 48(1)

NOTES:
1. Described on p. 13-34 of 1978 Data Catalog
2. Special adaptor socket.
3. Described on p. 13-39 of 1978 Data Catalog
4. Described on p. 13-71 of 1978 Data Catalog

ERASURE CHARACTERISTICS

The erasure characteristics of the 8755A are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 8755A in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 8755A is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 8755 window to prevent unintentional erasure.

The recommended erasure procedure for the 8755A is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000μW/cm² power rating. The 8755A should be placed within one inch from the lamp tubes during erasure. Some lamps have a filter on their tubes and this filter should be removed before erasure.

PROGRAMMING

Initially, and after each erasure, all bits of the EPROM portions of the 8755A are in the "1" state. Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The 8755A can be programmed on the Intel® Universal PROM Programmer (UPP), and the PROMPT™ 80/85 and PROMPT-48™ design aids. The appropriate programming modules and adapters for use in programming both 8755A's and 8755's are shown in Table 1.

The program mode itself consists of programming a single address at a time, giving a single 50 msec pulse for every address. Generally, it is desirable to have a verify cycle after a program cycle for the same address as shown in the attached timing diagram. In the verify cycle (i.e., normal memory read cycle) V_{DD} should be at +5V.

Preliminary timing diagrams and parameter values pertaining to the 8755A programming operation are contained in Figure 7.

SYSTEM APPLICATIONS

System Interface with 8085A and 8088

A system using the 8755A can use either one of the two I/O interface techniques:

- Standard I/O
- Memory Mapped I/O

If a standard I/O technique is used, the system can use the feature of both CE_3 and $\overline{CE}_1$. By using a combination of unused address lines A_{11-15} and the Chip Enable inputs, the 8085A system can use up to 6 each 8755A's without requiring a CE decoder. See Figure 2a and 2b.

If a memory mapped I/O approach is used the 8755A will be selected by the combination of both the Chip Enables and IO/$\overline{M}$ using the AD_{8-15} address lines. See Figure 1.

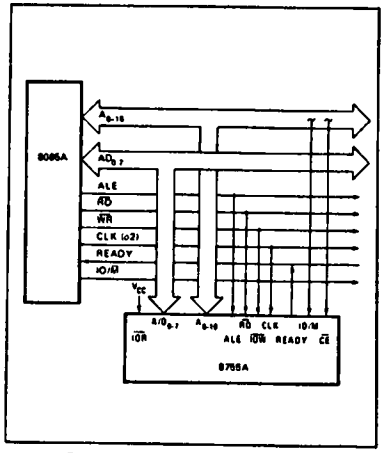


Figure 3. 8755A in 8085A System (Memory-Mapped I/O)

iAPX 88 FIVE CHIP SYSTEM

Figure 4 shows a five chip system containing:

- 1 25K Bytes RAM
- 2K Bytes ROM
- 38 I/O Pins
- 1 Interval Timer
- 2 Interrupt Levels

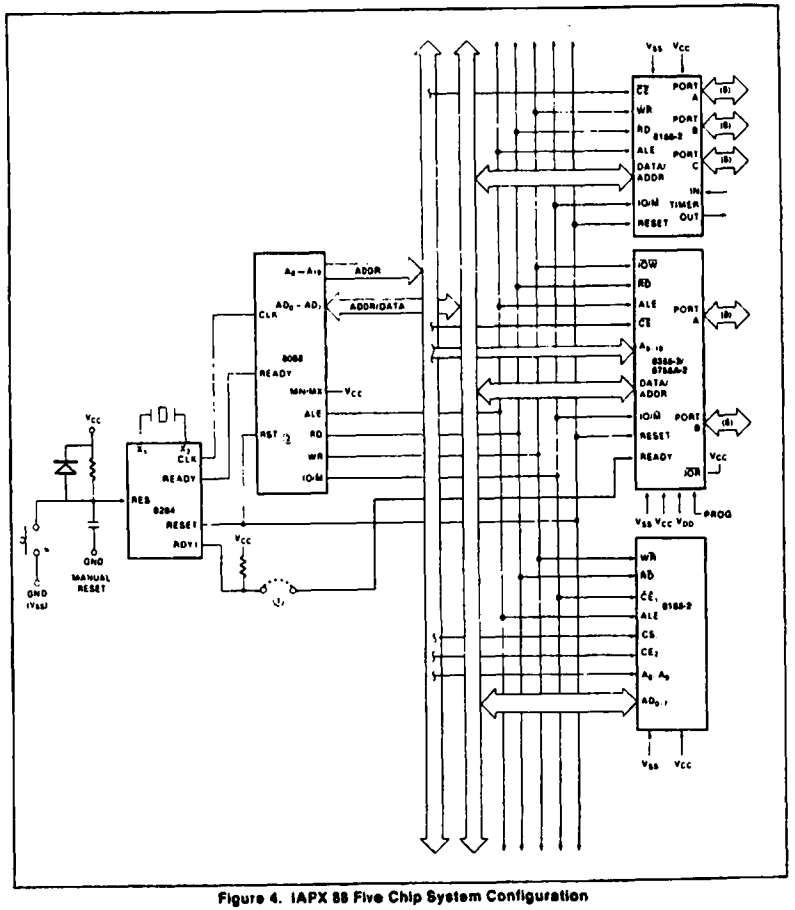


Figure 4. iAPX 88 Five Chip System Configuration

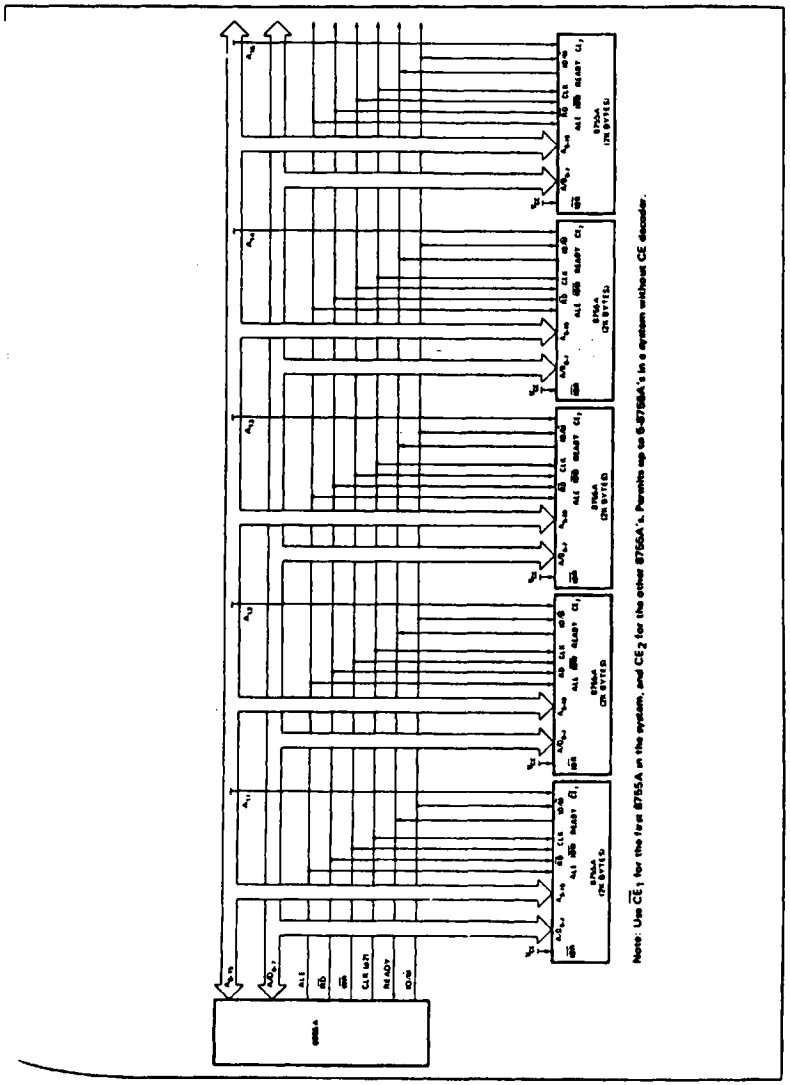


Figure 5. 8755A in 8085A System (Standard I/O)

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	1.5W

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°, V_{CC} = V_{DD} = 5V ± 5%; V_{CC} = V_{DD} = 5V ±10% for 8755A-2)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	V_{CC} = 5.0V
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	V_{CC} = 5.0V
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{IL}	Input Leakage		10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{LO}	Output Leakage Current		±10	μA	$V_{SS} \leq 0.45V \leq V_{OUT} \leq V_{CC}$
I_{CC}	V_{CC} Supply Current		180	mA	
I_{DD}	V_{DD} Supply Current		30	mA	V_{DD} = V_{CC}
C_{IN}	Capacitance of Input Buffer		10	pF	f_C = 1μHz
$C_{I/O}$	Capacitance of I/O Buffer		15	pF	f_C = 1μHz

D.C. CHARACTERISTICS — PROGRAMMING (T_A = 0°C to 70°, V_{CC} = 5V ± 5%, V_{SS} = 0V, V_{DD} = 25V ± 1V, V_{CC} = V_{DD} = 5V ±10% for 8755A-2)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Programming Voltage (during Write to EPROM)	24	25	26	V
I_{DD}	Prog Supply Current		15	30	mA

A.C. CHARACTERISTICS (T_A = 0°C to 70°, V_{CC} = 5V ± 5%; V_{CC} = V_{DD} = 5V ±10% for 8755A-2)

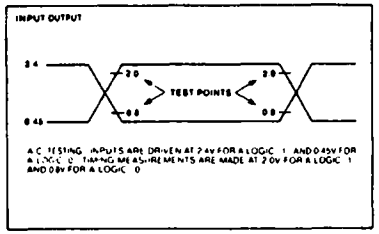
Symbol	Parameter	8755A Min.	8755A Max.	8755A-2 (Preliminary) Min.	8755A-2 (Preliminary) Max.	Units
t_{CYC}	Clock Cycle Time	320		200		ns
T_1	CLK Pulse Width	80		40		ns
T_2	CLK Pulse Width	120		70		ns
t_r, t_f	CLK Rise and Fall Time		30		30	ns
t_{AL}	Address to Latch Set Up Time	50		30		ns
t_{LA}	Address Hold Time after Latch	80		45		ns
t_{LC}	Latch to READ/WRITE Control	100		40		ns
t_{RD}	Valid Data Out Delay from READ Control		170*		140*	ns
t_{AD}	Address Stable to Data Out Valid		450		330	ns
t_{LL}	Latch Enable Width	100		70		ns
t_{RDF}	Data Bus Float after READ	0	100	0	85	ns
t_{CL}	READ/WRITE Control to Latch Enable	20		10		ns
t_{CC}	READ/WRITE Control Width	250		200		ns
t_{DW}	Data In to Write Set Up Time	150		150		ns
t_{WD}	Data In Hold Time After WRITE	30		10		ns
t_{WP}	WRITE to Port Output		400		300	ns
t_{PR}	Port Input Set Up Time	50		50		ns
t_{RP}	Port Input Hold Time to Control	50		50		ns
t_{RYH}	READY HOLD Time to Control	0	160	0	160	ns
t_{ARY}	ADDRESS CE to READY		160		160	ns
t_{RV}	Recovery Time Between Controls	300		200		ns
t_{RDE}	READ Control to Data Bus Enable	10		10		ns
t_{LD}	ALE to Data Out Valid		350		270	ns

NOTE:
C_{LOAD} = 150pF.
*For T_{AD} = (T_{AL} + T_{LC}), whichever is greater.

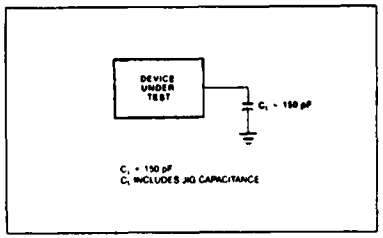
A.C. CHARACTERISTICS — PROGRAMMING (T_A = 0°C to 70°, V_{CC} = 5V ± 5%, V_{SS} = 0V, V_{DD} = 25V ± 1V; V_{CC} = V_{DD} = 5V ±10% for 8755A-2)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{PS}	Data Setup Time	10			ns
t_{PD}	Data Hold Time	0			ns
t_S	Prog Pulse Setup Time	2			μs
t_H	Prog Pulse Hold Time	2			μs
t_{PR}	Prog Pulse Rise Time	0.01	2		μs
t_{PF}	Prog Pulse Fall Time	0.01	2		μs
t_{PRG}	Prog Pulse Width	45	50		msec

A.C. TESTING INPUT, OUTPUT WAVEFORM

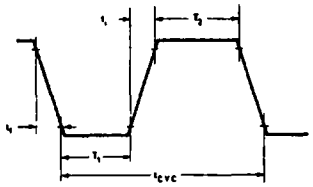


A.C. TESTING LOAD CIRCUIT

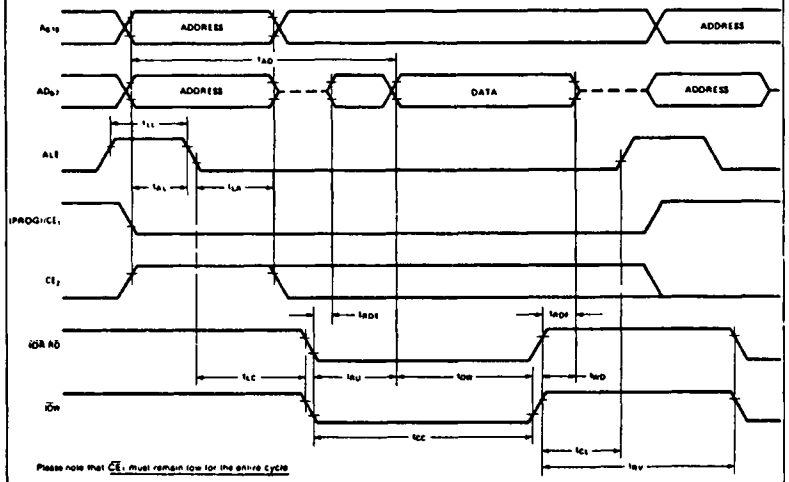


WAVEFORMS

CLOCK SPECIFICATION FOR 8755A



PROM READ, I/O READ AND WRITE



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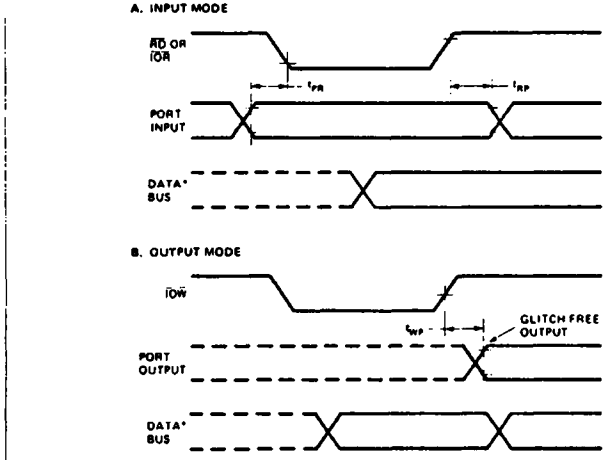
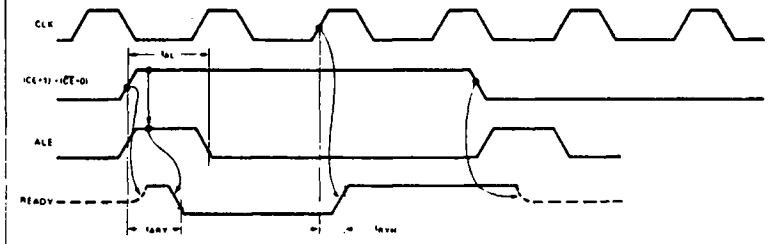
WAVEFORMS (Continued)

I/O PORT

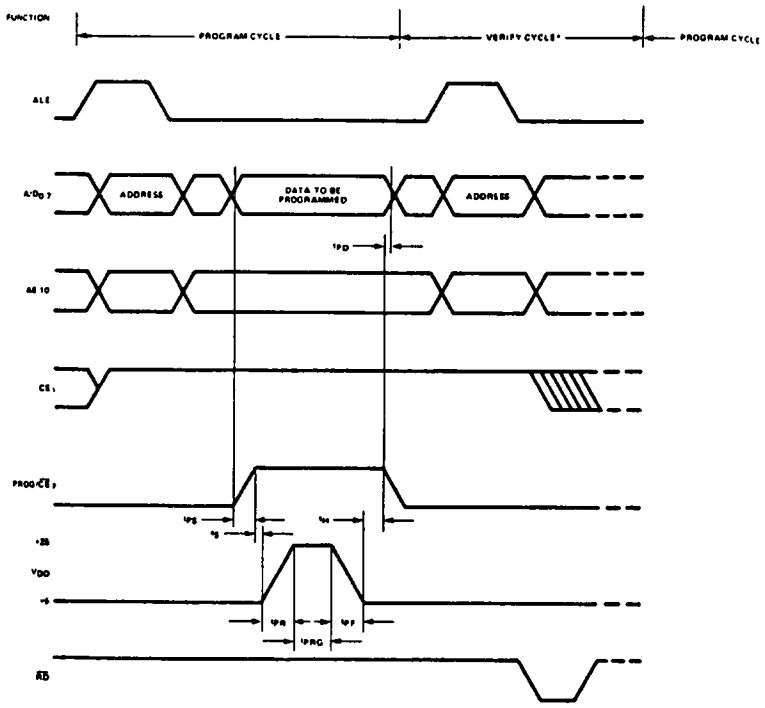


WAIT STATE (READY = 0)



WAVEFORMS (Continued)

8755A PROGRAM MODE



*VERIFY CYCLE IS A REGULAR MEMORY READ CYCLE (WITH V_{DD} = +5V FOR 8755A)

ANALOG DEVICES

Integrated Circuit 10-Bit Analog-to-Digital Converter

AD571*

FEATURES
- Complete A/D Converter with Reference and Clock
- Fast Successive Approximation Conversion – 25μs
- No Missing Codes Over Temperature
  - 0 to +70°C – AD571K
  - -55°C to +125°C – AD571S
- Digital Multiplexing – 3 State Outputs
- 18-Pin Ceramic DIP
- Low Cost Monolithic Construction

PRODUCT DESCRIPTION

The AD571 is a 10-bit successive approximation A/D converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register and output buffers – all fabricated on a single chip. No external components are required to perform a full accuracy 10-bit conversion in 25μs.

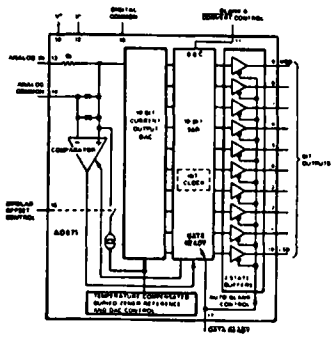
The AD571 incorporates the most advanced integrated circuit design and processing technology available today. It is the first complete converter to employ I^2L (integrated injection logic) processing in the fabrication of the SAR function. Laser trimming of the high stability SiCr thin film resistor ladder network at the wafer stage (LWT) insures high accuracy, which is maintained with a temperature compensated, subsurface Zener reference.

Operating on supplies of +5V to +15V and -15V, the AD571 will accept analog inputs of 0 to +10V, unipolar or ±5V bipolar, externally selectable. As the BLANK and $\overline{\text{CONVERT}}$ input is driven low, the three state outputs will be open and a conversion will commence. Upon completion of the conversion, the $\overline{\text{DATA READY}}$ line will go low and the data will appear at the output. Pulling the BLANK and $\overline{\text{CONVERT}}$ input high blanks the outputs and readies the device for the next conversion. The AD571 executes a true 10-bit conversion with no missing codes in approximately 25μs.

The AD571 is available in two versions for the 0 to +70°C temperature range, the AD571J and K. The AD571S guarantees 10-bit accuracy and no missing codes from -55°C to +125°C.

*Covered by Patent Nos. 3,940,760; 4,213,806; 4,136,349.

AD571 FUNCTIONAL BLOCK DIAGRAM



18-PIN DIP

PRODUCT HIGHLIGHTS

1. The AD571 is a complete 10-bit A/D converter. No external components are required to perform a conversion. Full scale calibration accuracy of ±0.3% is achieved without external trims.
2. The AD571 is a single chip device employing the most advanced IC processing techniques. Thus, the user has at his disposal a truly precision component with the reliability and low cost inherent in monolithic construction.
3. The AD571 accepts either unipolar (0 to +10V) or bipolar (-5V to +5V) analog inputs by simply grounding or opening a single pin.
4. The device offers true 10-bit accuracy and exhibits no missing codes over its entire operating temperature range.
5. Operation is guaranteed with -15V and +5V to +15V supplies. The device will also operate with a -12V supply.

10

SPECIFICATIONS

(T_A = 25°C, V+ = +5V, V− = −12V or −15V, all voltages measured with respect to digital common, unless otherwise indicated)

Model	AD571J Min	AD571J Typ	AD571J Max	AD571K Min	AD571K Typ	AD571K Max	AD571S Min	AD571S Typ	AD571S Max	Units
RESOLUTION		10			10			10		Bits
RELATIVE ACCURACY, T_A[1]			±1			±1/2			±1	LSB
T_{min} to T_{max}			±1			±1/2			±1	LSB
FULL SCALE CALIBRATION[2]		±2			±2			±2		LSB
UNIPOLAR OFFSET			±1			±1/2			±1	LSB
BIPOLAR OFFSET			±1			±1/2			±1	LSB
DIFFERENTIAL NONLINEARITY, T_A	10			10			10			Bits
T_{min} to T_{max}	9			10			10			Bits
TEMPERATURE RANGE	0		+70	0		+70	-55		+125	°C
TEMPERATURE COEFFICIENTS										
Unipolar Offset			±2			±1			±2	LSB
Bipolar Offset			±2			±1			±2	LSB
Full Scale Calibration[3]			±4			±2			±5	LSB
POWER SUPPLY REJECTION										
CMOS Positive Supply										
+13.5V≤V+≤+16.5V	-	-	-	-		±1	-	-	-	LSB
TTL Positive Supply										
+4.5V≤V+≤+5.5V			±2			±1			±2	LSB
Negative Supply										
-16.0V≤V−≤-13.5V			±2			±1			±2	LSB
ANALOG INPUT IMPEDANCE	3.0	5.0	7.0	3.0	5.0	7.0	3.0	5.0	7.0	kΩ
ANALOG INPUT RANGES										
Unipolar	0		+10	0		+10	0		+10	V
Bipolar	-5		+5	-5		+5	-5		+5	V
OUTPUT CODING										
Unipolar	Positive True Binary			Positive True Binary			Positive True Binary			
Bipolar	Positive True Offset Binary			Positive True Offset Binary			Positive True Offset Binary			
LOGIC OUTPUT										
Output Sink Current (V_{OUT} = 0.4V max, T_{min} to T_{max})	3.2			3.2			3.2			mA
Output Source Current[4] (V_{OUT} = 2.4V max, T_{min} to T_{max})	0.5			0.5			0.5			mA
Output Leakage			±40			±40			±40	μA
LOGIC INPUTS										
Input Current			±100			±100			±100	μA
Logic "1"	2.0			2.0			2.0			V
Logic "0"			0.8			0.8			0.8	V
CONVERSION TIME, T_A and T_{min} to T_{max}	15	25	40	15	25	40	15	25	40	μs
POWER SUPPLY										
V+	+4.5	+5.0	+7.0	+4.5	+5.0	+16.5	+4.5	+5.0	+7.0	V
V-	-12.0	-15	-16.5	-12.0	-15	-16.5	-12.0	-15	-16.5	V
OPERATING CURRENT										
V+		15	25		15	25		15	25	mA
V-		9	15		9	15		9	15	mA
PACKAGE[5]										
Ceramic DIP		D18A			D18A			D18A		
Plastic DIP		N18A			N18A					

NOTES

[1]Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[2]Full scale calibration is guaranteed trimmable to zero with an external 50Ω potentiometer in place of the 15Ω fixed resistor.

Full scale is defined as 10 volts minus 1LSB, or 9.990 volts.

[3]The data output lines have active pull-ups to source 0.5mA. The $\overline{\text{DATA READY}}$ line is open collector with a nominal 6kΩ internal pull-up resistor.

[4]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common	AD571J, S	0 to +7V
	AD571K	0 to +16.5V
V- to Digital Common		0 to -16.0V
Analog Common to Digital Common		±1V
Analog Input to Analog Common		±15V
Control Inputs		0 to V+
Digital Outputs (Blank Mode)		0 to V+
Power Dissipation		800mW

CIRCUIT DESCRIPTION

The AD571 is a complete 10-bit A/D converter which requires no external components to provide the complete successive-approximation analog-to-digital conversion function. A block diagram of the AD571 is shown in Figure 1. Upon receipt of the $\overline{\text{CONVERT}}$ command, the internal 10-bit current output DAC is sequenced by the I^2L successive-approximation register (SAR) from its most-significant bit (MSB) to least-significant bit (LSB) to provide an output current which accurately balances the input signal current through the 5kΩ input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less the bit is left on, if more, the bit is turned off. After testing all the bits, the SAR contains a 10-bit binary code which accurately represents the input signal to within ±½LSB (0.05%).

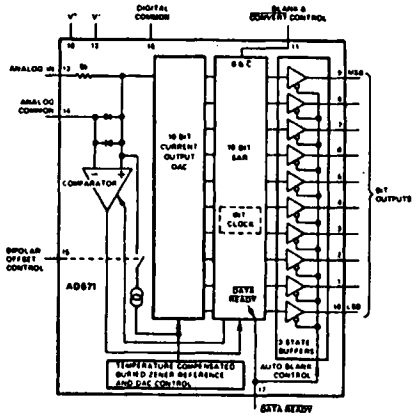


Figure 1. AD571 Functional Block Diagram

Upon completion of the sequence, the SAR sends out a $\overline{\text{DATA READY}}$ signal (active low), which also brings the three-state buffers out of their "open" state, making the bit output lines become active high or low, depending on the code in the SAR. When the BLANK and $\overline{\text{CONVERT}}$ line is brought high, the output buffers again go "open", and the SAR is prepared for another conversion cycle. Details of the timing are given further.

The temperature compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The bipolar offset input controls a switch which allows the positive bipolar offset current (exactly equal to the value of the MSB less ½LSB) to be injected into the summing (+) node of the comparator to offset the DAC output. Thus the nominal 0 to +10V unipolar input range becomes a -5V to +5V range. The 5kΩ thin film input resistor is trimmed so that with a full scale input signal, an input current will be generated which exactly matches the DAC output with all bits on. (The input resistor is trimmed slightly low to facilitate user trimming, as discussed on the next page.)

POWER SUPPLY SELECTION

The AD571 is designed for optimum performance using a +5V and -15V supply, for which the AD571J and AD571S are specified. AD571K will also operate with up to a +15V supply, which allows direct interface to CMOS logic. The input logic threshold is a function of V+ as shown in Figure 2. The supply current drawn by the device is a function of both V+ and the operating mode (BLANK or CONVERT). These supply current variations are shown in Figure 3. The supply currents change only moderately over temperature as shown in Figure 7.

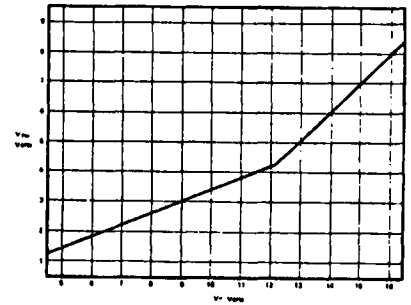


Figure 2. Logic Threshold (AD571K Only)

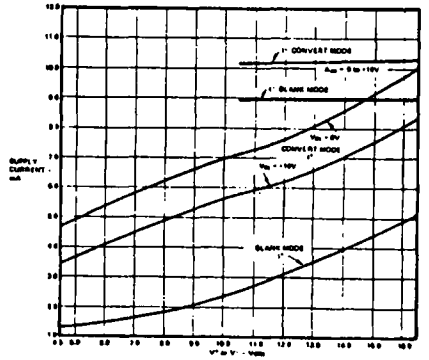


Figure 3. Supply Currents vs. Supply Levels and Operating Modes

CONNECTING THE AD571 FOR STANDARD OPERATION

The AD571 contains all the active components required to perform a complete A/D conversion. Thus, for most situations, all that is necessary is connection of the power supply (+5 and -15), the analog input, and the conversion start pulse. But, there are some features and special connections which should be considered for achieving optimum performance. The functional pin-out is shown in Figure 4.

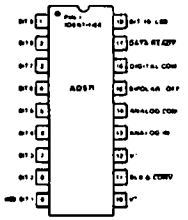


Figure 4. AD571 Pin Connections

FULL SCALE CALIBRATION

The 5kΩ thin-film input resistor is laser trimmed to produce a current which matches the full scale current of the internal DAC—plus about 0.3%—when a full scale analog input voltage of 9.990 volts (10 volts − 1 LSB) is applied at the input. The input resistor is trimmed in this way so that if a fine trimming potentiometer is inserted in series with the input signal, the input current at the full scale input voltage can be trimmed down to match the DAC full scale current as precisely as desired. However, for many applications the nominal 9.99 volt full scale can be achieved to sufficient accuracy by simply inserting a 15Ω resistor in series with the analog input to pin 13. Typical full scale calibration error will then be about ±2LSB or ±0.2%. If the more precise calibration is desired, a 50Ω trimmer should be used instead. Set the analog input at 9.990 volts, and set the trimmer so that the output code is just at the transition between 1111111110 and 1111111111. Each LSB will then have a weight of 9.766mV. If a nominal full scale of 10.24 volts is desired (which makes the LSB have weight of exactly 10.00mV), a 100Ω resistor in series with a 100Ω trimmer (or a 200Ω trimmer with good resolution) should be used. Of course, larger full scale ranges can be arranged by using a larger input resistor, but linearity and full scale temperature coefficient may be compromised if the external resistor becomes a sizeable percentage of 5kΩ.

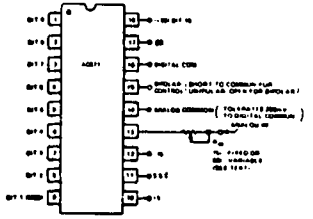


Figure 5. Standard AD571 Connections

BIPOLAR OPERATION

The standard unipolar 0 to +10V range is obtained by shorting the bipolar offset control pin to digital common. If the pin is left open, the bipolar offset current will be switched into the comparator summing node, giving a -5V to +5V range with an offset binary output code. (-5.00 volts in will give a 10-bit code of 0000000000; an input of 0.00 volts results in an output code of 1000000000 and 4.99 volts at the input yeilds the 1111111111 code). The bipolar offset control input is not directly TTL compatible, but a TTL interface for logic control can be constructed as shown in Figure 6.

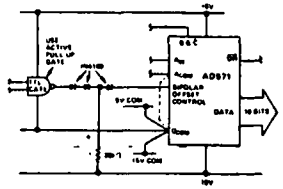


Figure 6. Bipolar Offset Controlled by Logic Gate

Gate Output = 1 Unipolar 0 - 10V Input Range
Gate Output = 0 Bipolar ±5V Input Range

COMMON MODE RANGE

The AD571 provides separate Analog and Digital Common connections. The circuit will operate properly with as much as ±200mV of common mode range between the two commons. This permits more flexible control of system common bussing and digital and analog returns.

In normal operation the Analog Common terminal may generate transient currents of up to 2mA during a conversion. In addition, a static current of about 2mA will flow into Analog Common in the unipolar mode after a conversion is complete. An additional 1mA will flow in during a blank interval with zero analog input. The Analog Common current will be modulated by the variations in input signal.

The absolute maximum voltage rating between the two commons is ±1 volt. We recommend the connection of a parallel pair of back-to-back protection diodes between the commons if they are not connected locally.

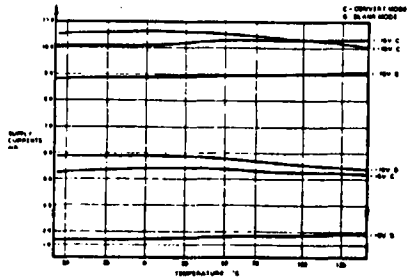


Figure 7. AD571 Power Supply Current vs. Temperature

ZERO OFFSET

The apparent zero point of the AD571 can be adjusted by inserting an offset voltage between the Analog Common of the device and the actual signal return or signal common. Figure 8 illustrates two methods of providing this offset. Figure 8A shows how the converter zero may be offset by up to ±3 bits to correct the device initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode. In bipolar mode R2 should be omitted to obtain a symmetrical range.

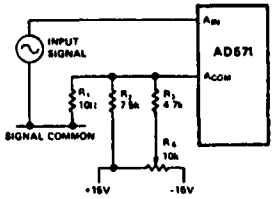


Figure 8. (A)

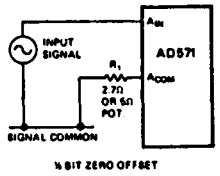


Figure 8. (B)

Figure 9 shows the nominal transfer curve near zero for an AD571 in unipolar mode. The code transitions are at the edges of the nominal bit weights. In some applications it will be preferable to offset the code transitions so that they fall between the nominal bit weights, as shown in the offset characteristics. This offset can easily be accomplished as shown in Figure 8B. At balance (after a conversion) approximately 2mA flows into the Analog Common terminal. A 2.7Ω resistor in series with this terminal will result in approximately the desired ½ bit offset of the transfer characteristics. The nominal 2mA Analog Common current is not closely controlled in manufacture. If high accuracy is required, a 5Ω potentiometer (connected as a rheostat) can be used as R1. Additional negative offset range may be obtained by using larger values of R1. Of course, if the zero transition point is changed, the full scale transition point will also move. Thus, if an offset of ½LSB is introduced, full scale trimming as described on previous page should be done with an analog input of 9.985 volts.

NOTE: During a conversion transient currents from the Analog Common terminal will disturb the offset voltage. Capacitive decoupling should not be used around the offset network. These transients will settle as appropriate during a conversion. Capacitive decoupling will "pump up" and fail to settle resulting in conversion errors. Power supply decoupling which returns to analog signal common, should go to the signal input side of the resistive offset network.

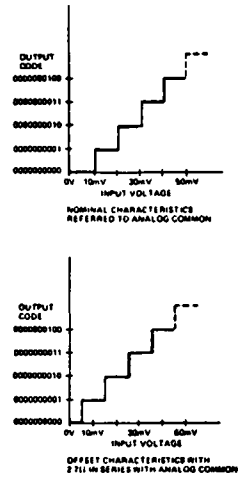


Figure 9. AD571 Transfer Curve - Unipolar Operation (Approximate Bit Weights Shown for Illustration, Nominal Bit Weights ~9.766mV)

BIPOLAR CONNECTION

To obtain the bipolar -5V to +5V range with an offset binary output code the bipolar offset control pin is left open.

A -5.0 volt signal will give a 10-bit code of 00000000 00; an input of 0.00 volts results in an output code of 10000000 00 and +4.99 volts at the input yields the 11111111 11 code. The nominal transfer curve is shown in Figure 10.

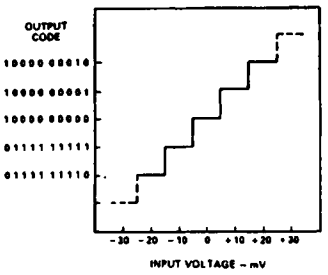


Figure 10. AD571 Transfer Curve — Bipolar Operation

Control and Timing of the AD571

CONTROL AND TIMING OF THE AD571

There are several important timing and control features on the AD571 which must be understood precisely to allow optimal interfacing to microprocessor or other types of control systems. All of these features are shown in the timing diagram in Figure 11.

The normal stand-by situation is shown at the left end of the drawing. The BLANK and $\overline{\text{CONVERT}}$ (B & $\overline{\text{C}}$) line is held high, the output lines will be "open", and the $\overline{\text{DATA READY}}$ ($\overline{\text{DR}}$) line will be high. This mode is the lowest power state of the device (typically 150mW). When the (B & $\overline{\text{C}}$) line is brought low, the conversion cycle is initiated; but the $\overline{\text{DR}}$ and Data lines do not change state. When the conversion cycle is complete (typically 25μs), the $\overline{\text{DR}}$ line goes low, and within 500ns, the Data lines become active with the new data.

About 1.5μs after the B & $\overline{\text{C}}$ line is again brought high, the $\overline{\text{DR}}$ line will go high and the Data lines will go open. When the B & $\overline{\text{C}}$ line is again brought low, a new conversion will begin. The minimum pulse width for the B & $\overline{\text{C}}$ line to blank previous data and start a new conversion is 2μs. If the B & $\overline{\text{C}}$ line is brought high during a conversion, the conversion will stop, and the $\overline{\text{DR}}$ and Data lines will not change. If a 2μs or longer pulse is applied to the B & C line during a conversion, the converter will clear and start a new conversion cycle.

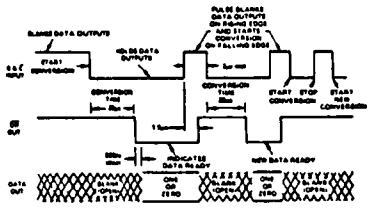


Figure 11. AD571 Timing and Control Sequences

CONTROL MODES WITH BLANK AND $\overline{\text{CONVERT}}$

The timing sequence of the AD571 discussed above allows the device to be easily operated in a variety of systems with differing control modes. The two most common control modes, the Convert Pulse Mode, and the Multiplex Mode, are illustrated here.

Convert Pulse Mode – In this mode, data is present at the output of the converter at all times except when conversion is taking place. Figure 12 illustrates the timing of this mode. The BLANK and $\overline{\text{CONVERT}}$ line is normally low and conversions are triggered by a positive pulse. A typical application for this timing mode is shown in Figure 15 in which μP bus interfacing is easily accomplished with three-state buffers.

Multiplex Mode – In this mode the outputs are blanked except when the device is selected for conversion and readout; this timing is shown in Figure 13. A typical AD571 multiplexing application is shown in Figure 16.

This operating mode allows multiple AD571 devices to drive common data lines. All BLANK and $\overline{\text{CONVERT}}$ lines are held high to keep the outputs blanked. A single AD571 is selected, its BLANK and $\overline{\text{CONVERT}}$ line is driven low and at the end of conversion, which is indicated by $\overline{\text{DATA READY}}$ going low, the conversion result will be present at the outputs. When this data has been read from the 10-bit bus, BLANK and $\overline{\text{CONVERT}}$ is restored to the blank mode to clear the data bus for other converters. When several AD571's are multiplexed in sequence, a new conversion may be started in one AD571 while data is being read from another. As long as the data is read and the first AD571 is cleared within 15μs after the start of conversion of the second AD571, no data overlap will occur.

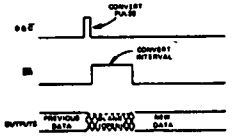


Figure 12. Convert Pulse Mode

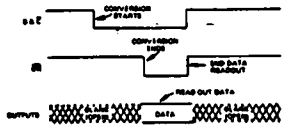


Figure 13. Multiplex Mode

SAMPLE-HOLD AMPLIFIER CONNECTION TO THE AD571

Many situations in high-speed acquisition systems or digitizing of rapidly changing signals require a sample-hold amplifier (SHA) in front of the A-D converter. The SHA can acquire and hold a signal faster than the converter can perform a conversion. A SHA can also be used to accurately define the exact point in time at which the signal is sampled. For the AD571, a SHA can also serve as a high input impedance buffer.

Figure 14 shows the AD571 connected to the AD582 monolithic SHA for high speed signal acquisition. In this configuration the AD582 will acquire a 10 volt signal in less than 10μs with a droop rate less than 100μV/ms. The control signals are arranged so that when the control line goes low, the AD582 is put into the "hold" mode, and the AD571 will begin its conversion cycle. (The AD582 settles to final value well in advance of the first comparator decision inside the AD571) The $\overline{\text{DATA READY}}$ line is fed back to the other side of the differential input control gate so that the AD582 cannot come out of the "hold" mode during the conversion cycle. At the end of the conversion cycle, the $\overline{\text{DATA READY}}$ line goes low, automatically placing the AD582 back into the sample mode. This feature allows simple control of both the SHA and the A-D converter with a single line. Observe carefully the ground, supply, and bypass capacitor connections between the two devices. This will minimize ground noise and interference during the conversion cycle to give the most accurate measurements.

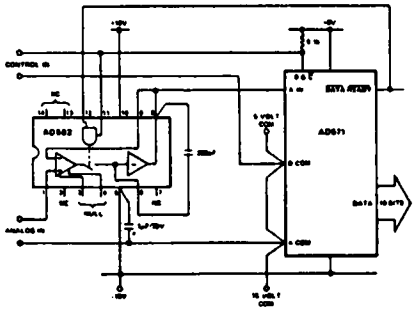


Figure 14. Sample-Hold Interface to the AD571

INTERFACING THE AD571 TO A MICROPROCESSOR

The AD571 can easily be arranged to be driven from standard microprocessor control lines and to present data to any standard microprocessor bus (4-, 8-, 12-or 16-bit) with a minimum of additional control components. The configuration shown in Figure 15 is designed to operate with 8-bit bus and standard 8080 control signals.

The input control circuitry shown is required to insure that the AD571 receives a sufficiently long B & $\overline{\text{C}}$ input pulse. When the converter is ready to start a new conversion, the B & $\overline{\text{C}}$ line is low, and $\overline{\text{DR}}$ is low. To command a conversion, the start address decode line goes low, followed by $\overline{\text{WR}}$. The B & $\overline{\text{C}}$ line will now go high, followed about 1.5μs later by $\overline{\text{DR}}$. This resets the external flip-flop and brings B & $\overline{\text{C}}$ back to low, which initiates the conversion cycle. At the end of the conversion cycle, the $\overline{\text{DR}}$ line goes low, the data outputs will become active with the new data and the control lines will return to the stand-by state. The new data will remain active until a new conversion is commanded. The self-pulsing nature of this circuit guarantees a sufficient convert pulse width.

This new data can now be presented to the data bus by enabling the three-state buffers when desired. A data word (8-bit or 2-bit) is loaded onto the bus when its decoded address goes low and the $\overline{\text{RD}}$ line goes low. This arrangement presents data to the bus "left-justified," with highest bits in the 8-bit word; a "right-justified" data arrangement can be set up by a simple re-wiring. Polling the converter to determine if conversion is complete can be done by addressing the gate which buffers the $\overline{\text{DR}}$ line, as shown. In this configuration, there is no need for additional buffer register storage since the data can be held indefinitely in the AD571, since the B & $\overline{\text{C}}$ line is continually held low.

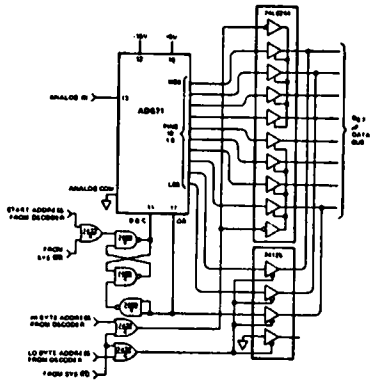


Figure 15. Interfacing AD571 to an 8-bit Bus (8080 Control Structure)

BUS INTERFACING WITH A PERIPHERAL INTERFACE CIRCUIT

An improved technique for interfacing to a μP bus involves the use of special peripheral interfacing circuits (or I/O devices), such as the MC6821 Peripheral Interface Adapter (PIA). Shown in Figure 16 is a straighforward application of a PIA to multiplex up to 8 AD571 circuits. The AD571 has 3-state outputs, hence the data bit outputs can be paralleled, provided that only one converter at a time is permitted to be the active state. The $\overline{\text{DATA READY}}$ output of the AD571 is an open collector with resistor pull-up, thus several $\overline{\text{DR}}$ lines can be wire-ored to allow indication of the status of the selected device. One of the 8-bit ports of the PIA is combined with 2-bits from the other port and programmed as a 10-bit input port. The remaining 6-bits of the second port are programmed as outputs and along with the 2 control bits (which act as outputs), are used to control the 8 AD571's. When a control line is in the "1" or high state, the ADC will be automatically blanked. That is, its outputs will be in the inactive open state. If a single control line is switched low, its ADC will convert and the outputs will automatically go active when the conversion is complete. The result can be read from the two peripheral ports; when the next conversion is desired, a different control line can be switched to zero, blanking the previously active port at the same time. Subsequently, this second device can be read by the microprocessor, and so-forth. The status lines are wire-ored in 2 groups and connected to the two remaining control pins. This allows a conversion status check to be made after a convert command, if necessary. The ADC's are divided into two groups to minimize the loading effect of the internal pull-up resistors on the $\overline{\text{DATA READY}}$ buffers. See the Motorola MC6821 data sheet for more application detail.

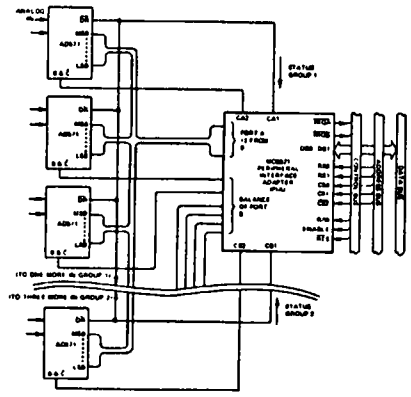


Figure 16. Multiplexing 8 AD571s Using Single PIA for μP Interface. No Other Logic Required (6800 Control Structure).

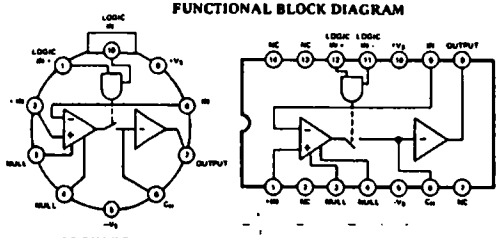
ANALOG DEVICES

Low Cost Sample/Hold Amplifier

AD582

FEATURES
- Suitable for 12-Bit Applications
- High Sample/Hold Current Ratio: 10^7
- Low Acquisition Time: 6μs to 0.1%
- Low Charge Transfer: < 2pC
- High Input Impedance in Sample and Hold Modes
- Connect in Any Op Amp Configuration
- Differential Logic Inputs

AD582 PIN CONFIGURATION AND FUNCTIONAL BLOCK DIAGRAM



10-PIN TO-100
TOP VIEW

14-PIN TO-116
TOP VIEW

PRODUCT DESCRIPTION

The AD582 is a low cost integrated circuit sample and hold amplifier consisting of a high performance operational amplifier, a low leakage analog switch and a JFET integrating amplifier – all fabricated on a single monolithic chip. An external holding capacitor, connected to the device, completes the sample and hold function.

With the analog switch closed, the AD582 functions like a standard op amp; any feedback network may be connected around the device to control gain and frequency response. With the switch open, the capacitor holds the output at its last level, regardless of input voltage.

Typical applications for the AD582 include sampled data systems, D/A deglitchers, analog de-multiplexers, auto null systems, strobed measurement systems and A/D speed enhancement.

The device is available in two versions: the "K" specified for operation over the 0 to +70°C commercial temperature range and the "S" specified over the extended temperature range, -55°C to +125°C. All versions may be obtained in either the hermetic sealed, TO 100 can or the TO-116 DIP.

PRODUCT HIGHLIGHTS

1. The specially designed input stage presents a high impedance to the signal source in both sample and hold modes (up to ±12V). Even with signal levels up to $\pm V_S$, no undesirable signal inversion, peaking or loss of hold voltage occurs.
2. The AD582 may be connected in any standard op amp configuration to control gain or frequency response and provide signal inversion, etc.
3. The AD582 offers a high, sample-to-hold current ratio: 10^7. The ratio of the available charging current to the holding leakage current is often used as a figure of merit for a sample and hold circuit.
4. The AD582 has a typical charge transfer less than 2pC. A low charge transfer produces less offset error and permits the use of smaller hold capacitors for faster signal acquisition.
5. The AD582 provides separate analog and digital grounds, thus improving the device's immunity to ground and switching transients.

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SPECIFICATIONS (typical @ +25°C, V_S = ±15V and C_H = 1000pF, A = +1 unless otherwise specified)

MODEL	AD582K	AD582S
SAMPLE/HOLD CHARACTERISTICS		
Acquisition Time, 10V Step to 0.1%, C_H = 100pF	6μs	*
Acquisition Time, 10V Step to 0.01%, C_H = 1000pF	25μs	*
Aperture Time, 20V p-p Input, Hold 0V	200ns	*
Aperture Jitter, 20V p-p Input, Hold 0V	15ns	*
Settling Time, 20V p-p Input, Hold 0V, to 0.01%	0.5μs	*
Droop Current, Steady State, $\pm 10V_{OUT}$	100pA max	*
Droop Current, T_{min} to T_{max}	1nA	150nA max
Charge Transfer	5pC max (1.5pC typ)	*
Sample to Hold Offset	0.5mV	*
Feedthrough Capacitance 20V p-p, 10kHz Input	0.05pF	*
TRANSFER CHARACTERISTICS		
Open Loop Gain V_{OUT} = 20V p-p, R_L = 2k	25k min (50k typ)	*
Common Mode Rejection V_{CM} = 20V p-p	60dB min (70dB typ)	*
Small Signal Gain Bandwidth V_{OUT} = 100mV p-p, C_H = 100pF	1.5MHz	*
Full Power Bandwidth V_{OUT} = 20V p-p, C_H = 100pF	70kHz	*
Slew Rate V_{OUT} = 20V p-p, C_H = 100pF	3V/μs	*
Output Resistance Hold Mode, I_{OUT} = ±5mA	12Ω	*
Linearity V_{OUT} = 20V p-p, R_L = 2k	±0.01%	*
Output Short Circuit Current	±25mA	*
ANALOG INPUT CHARACTERISTICS		
Offset Voltage	6mV max (2mV typ)	*
Offset Voltage, T_{min} to T_{max}	4mV	8mV max (5mV typ)
Bias Current	3μA max (1.5μA typ)	*
Offset Current	300nA max (75nA typ)	*
Offset Current, T_{min} to T_{max}	100nA	600nA max (100nA typ)
Input Capacitance, f = 1MHz	2pF	*
Input Resistance, Sample or Hold 20V p-p Input, A = +1	30MΩ	*
Absolute Max Diff Input Voltage	30V	*
Absolute Max Input Voltage, Either Input	$\pm V_S$	*
DIGITAL INPUT CHARACTERISTICS		
+Logic Input Voltage Hold Mode, T_{min} to T_{max}, -Logic @ 0V	+2V min	*
Sample Mode, T_{min} to T_{max}, -Logic @ 0V	+0.8V max	*
+Logic Input Current Hold Mode, +Logic @ +5V, -Logic @ 0V	1.5μA	*
Sample Mode, +Logic @ 0V, -Logic @ 0V	1mA	*
-Logic Input Current Hold Mode, +Logic @ +5V, -Logic @ 0V	24μA	*
Sample Mode, +Logic @ 0V, -Logic @ 0V	4μA	*
Absolute Max Diff Input Voltage, +L to -L	+15V/-6V	*
Absolute Max Input Voltage, Either Input	$\pm V_S$	*
POWER SUPPLY CHARACTERISTICS		
Operating Voltage Range	±9V to ±18V	±9V to ±22V
Supply Current, R_L = ∞	4.5mA max (3mA typ)	*
Power Supply Rejection, ΔV_S = 5V, Sample Mode (see next page)	60dB min (75dB typ)	*
TEMPERATURE RANGE		
Specified Performance	0 to +70°C	-55°C to +125°C
Operating	-25°C to +85°C	-55°C to +125°C
Storage	-65°C to +150°C	*
Lead Temperature (Soldering, 15 sec)	+300°C	*
PACKAGE OPTION[1]		
"H" Package TO-100	AD582KH	AD582SH
"D" Package TO 116 Style (D14A)	AD582KD	AD582SD

NOTES
*Specifications same as AD582K
[1] See Section 19 for package outline information
Specifications subject to change without notice.

APPLYING THE AD582

Both the inverting and non-inverting inputs are brought out to allow op amp type versatility in connecting and using the AD582. Figure 1 shows the basic non-inverting unity gain connection requiring only an external hold capacitor and the usual power supply bypass capacitors. An offset null pot can be added for more critical applications.

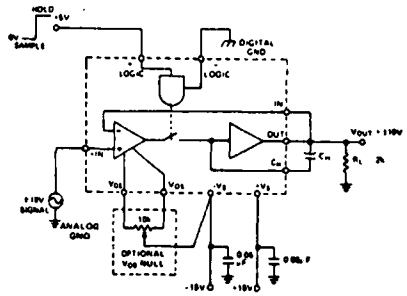


Figure 1. Sample and Hold with A = +1

Figure 2 shows a non-inverting configuration where voltage gain, A_V, is set by a pair of external resistors. Frequency shaping or non-linear networks can also be used for special applications.

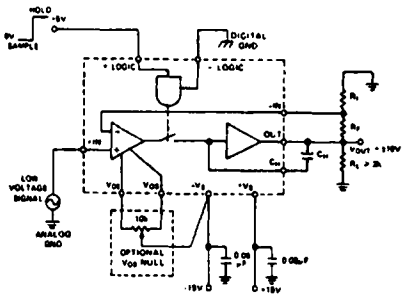


Figure 2. Sample and Hold with $A = (1 + R_F/R_I)$

The hold capacitor, C_H, should be a high quality polystyrene (for temperatures below +85°C) or Teflon type with low dielectric absorption. For high speed, limited accuracy applications, capacitors as small as 100pF may be used. Larger values are required for accuracies of 12 bits and above in order to minimize feedthrough, sample to hold offset and droop errors (see Figure 6). Care should be taken in the circuit layout to minimize coupling between the hold capacitor and the digital or signal inputs.

In the hold mode, the output voltage will follow any change in the $-V_S$ supply. Consequently, this supply should be well regulated and filtered.

Biasing the +Logic Input anywhere between -6V to +0.8V with respect to the -Logic will set the sample mode. The hold mode will result from any bias between +2.0V and $(+V_S - 3V)$. The sample and hold modes will be controlled differentially with the absolute voltage at either logic input ranging from $-V_S$ to within 3V of $+V_S$ (V_S - 3V). Figure 3 illustrates some examples of the flexibility of this feature.

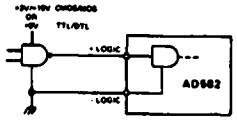


Figure 3A. Standard Logic Connection

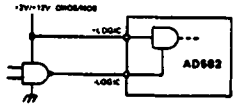


Figure 3B. Inverted Logic Sense Connection

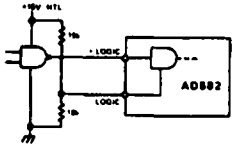


Figure 3C. High Threshold Logic Connection

14

DEFINITION OF TERMS

Figure 4 illustrates various dynamic characteristics of the AD582.

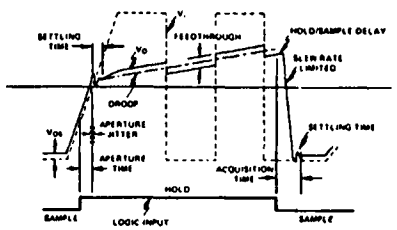


Figure 4. Pictorial Showing Various S/H Characteristics

Aperture Time is the time required after the "hold" command until the switch is fully open and produces a delay in the effective sample timing. Figure 5 is a plot giving the maximum frequency at which the AD582 can sample an input with a given accuracy (lower curve).

Aperture Jitter is the uncertainty in Aperture Time. If the Aperture Time is "tuned out" by advancing the sample-to-hold command 200ns with respect to the input signal, the Aperture Jitter now determines the maximum sampling frequency (upper curve of Figure 5).

Acquisition Time is the time required by the device to reach its final value within a given error band after the sample command has been given. This includes switch delay time, slewing time and settling time for a given output voltage change.

Droop is the change in the output voltage from the "held" value as a result of device leakage. In the AD582, droop can be in either the positive or negative direction. Droop rate may be calculated from droop current using the following formula:

$$\frac{\Delta V}{\Delta T}\,(\text{Volts/sec}) = \frac{I(\text{pA})}{C_H(\text{pF})}$$

(See also Figure 6.)

Feedthrough is that component of the output which follows the input signal *after* the switch is open. As a percentage of the input, feedthrough is determined as the ratio of the feedthrough capacitance to the hold capacitance (C_P/C_H).

Charge Transfer is the charge transferred to the holding capacitor from the interelectrode capacitance of the switch when the unit is switched to the hold mode. The charge transfer generates a sample-to-hold offset where:

$$\text{S/H Offset (V)} = \frac{\text{Charge (pC)}}{C_H(\text{pF})}$$

(See also Figure 6.)

Sample-to-Hold Offset is that component of D.C. offset independent of C_H (see Figure 6). This offset may be nulled using a null pot, however, the offset will then appear during the sampling mode.

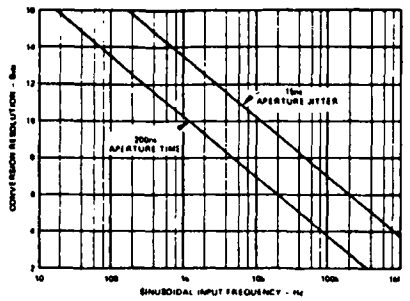


Figure 5. Maximum Frequency of Input Signal for ½LSB Sampling Accuracy

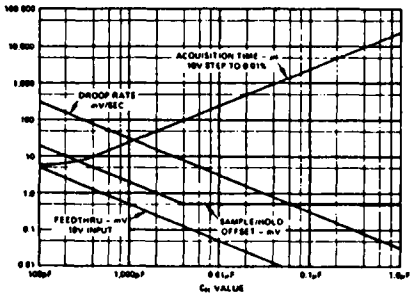


Figure 6. Sample-and-Hold Performance as a Function of Hold Capacitance

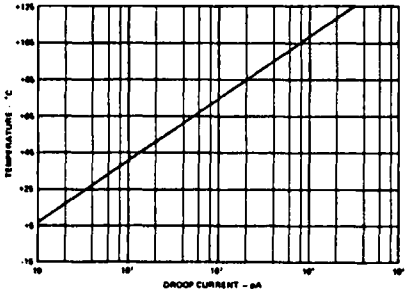


Figure 7. Droop Current vs. Temperature

HARRIS

HI-508/HI-509

Single 8/Differential 4 Channel CMOS Analog Multiplexer

FEATURES

- FAST ACCESS 220ns
- FAST SETTLING (0.01%) 600ns
- LOW R_{ON} 180Ω
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP
- TTL/CMOS COMPATIBLE 2.4V (LOGIC "1")

APPLICATIONS

- PRECISION INSTRUMENTS
- DATA ACQUISITION SYSTEMS
- TELEMETRY

DESCRIPTION

These monolithic CMOS multiplexers each include an array of eight analog switches, a digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latch-up. Also, DI offers much lower substrate leakage and parasitic capacitance than conventional junction-isolated CMOS (see Application Note 521). Combined with the low ON resistance (180Ω typical), these benefits allow low static error, fast channel switching rates, and fast settling.

Switches are guaranteed to break-before-make, so that two channels are never shorted together.

The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4V for "1" and Maximum 0.8V for "0". This allows direct interface without pull-up resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 2000Ω resistor and a diode clamp to each supply.

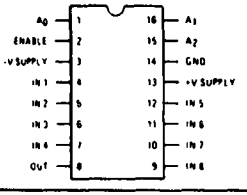
The HI-508 is an eight channel single-ended multiplexer, and the HI-509 is a four channel differential version. The recommended supply voltage is ± 15V, however, reasonable performance is available down to ± 7V. Each device is packaged in a 16 pin DIP.

The HI-508/509 is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix. For further information see Application Notes 520 and 521.

PINOUTS

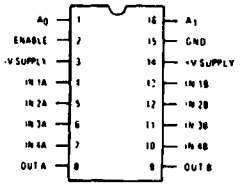
HI-508

TOP VIEW



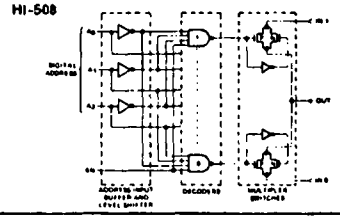
HI-509

TOP VIEW

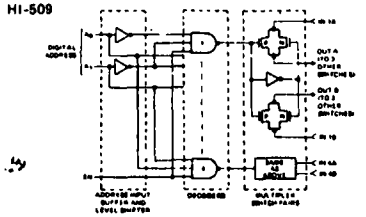


FUNCTIONAL DIAGRAMS

HI-508



HI-509



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

$V_{Supply}^{(+)}$ to $V_{Supply}^{(-)}$ 44V

$V_{Supply}^{(+)}$ to GND 22V

$V_{Supply}^{(-)}$ to GND 22V

Digital Input Overvoltage:

V_{EN}, V_A { $V_{Supply}^{(+)}$ +4V; $V_{Supply}^{(-)}$ -4V

Analog Input Overvoltage (Note 6):

V_D, V_S { $V_{Supply}^{(+)}$ +2V; $V_{Supply}^{(-)}$ -2V

Power Dissipation * 750mW

Operating Temperature Ranges:

HI-508/509-2, -8 -55°C to +125°C

HI-508/509-5, 0°C to 75°C

HI-508/509-1 -55°C to +200°C

Storage Temperature Range -65°C to +150°C

*Derate 9.6mW/°C above T_A = 95°C

ELECTRICAL CHARACTERISTICS Unless otherwise specified: Supplies = ± 15V, GND = 0V

		HI-508/HI-509-2 -55°C to +125°C			HI-508 HI-509-5 0°C to +70°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance	+25°C		180	300		180	400	Ω
	Full		230	400		230	500	Ω
ΔR_{ON}, Any Two Channels	+25°C		5			5		%
$I_{S(OFF)}$, Off Input Leakage Current (Note 2)	+25°C		0.01	10		0.01		nA
	Full			50			10	nA
$I_{D(OFF)}$, Off Output Leakage Current								
HI-508	Full		0.3	300		0.3	200	nA
HI-509	Full		0.3	100		0.3	100	nA
$I_{D(ON)}$, On Channel Leakage Current								
HI-508	Full		10	700		10	200	nA
HI-509	Full		10	100		10	100	nA
$I_{D(S)}$, Differential Off Output Leakage Current (HI-509 Only)	+25°C			5			5	nA
	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AH}, High Threshold	Full	2.4			2.4			V
V_{AL}, Low Threshold	Full			0.8			0.8	V
I_A, Input Leakage Current (High or Low) (Note 3)	Full			1			1	μA
SWITCHING CHARACTERISTICS								
t_A, Access (Transition) Time	+25°C		220	500		220		ns
	Full			1000			1000	ns
t_{OPEN}, Break-Before-Make Interval	+25°C	25	70		25	70		ns
$t_{ON(EN)}$, Enable Turn-On	+25°C		210	500		210		ns
	Full			1000			1000	ns
$t_{OFF(EN)}$, Enable Turn-Off	+25°C		180	500		180		ns
	Full			1000			1000	ns
t_S, Settling Time to 0.1%	+25°C		380			380		ns
to 0.01%	+25°C		600			600		ns
Off Isolation (Note 4)	+25°C	50	68		50	68		dB
$C_{S(OFF)}$, Channel Input Capacitance	+25°C		6			6		pF
$C_{D(OFF)}$, Channel Output Capacitance	+25°C		21			21		pF
C_A, Digital Input Capacitance	+25°C		3			3		pF
$C_{DS(OFF)}$, Input to Output Capacitance	+25°C		0.8			0.8		pF
POWER REQUIREMENTS								
I^+, Positive Supply Current (Note 5)	Full			2			2	mA
I^-, Negative Supply Current (Note 5)	Full			1			1	mA
P_D, Power Dissipation	Full			45			45	mW

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Test equipment is the practical limit for high speed measurement in the production test environment. Actually, I_S(off) is below 100pA for most devices at 25°C.
3. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25°C.
4. V_{EN} = 0.8V, R_S = 1K, C_L = 15pF, V_S = 7V_{RMS}, f = 500kHz. Worst case isolation occurs on channel 4 due to proximity of the output pins.
5. V_{EN} = 0V or 5V. All V_A = 0.
6. If an overvoltage condition is anticipated (analog input exceeds either power supply voltage), the HARRIS HI-508A/509A multiplexers are recommended.

TRUTH TABLES

HI-508

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

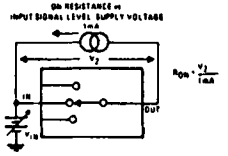
HI-509

A_1	A_0	EN	"ON" CHANNEL
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

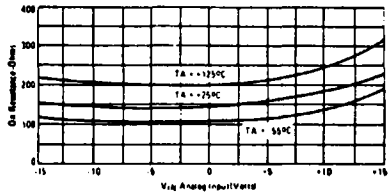
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

Unless Otherwise Specified, T_A = 25°C, V_{Supply} = ±15V, V_{AH} = 2.4V, V_{AL} = 0.8V.

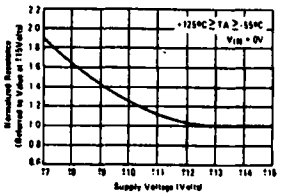
TEST CIRCUIT NO. 1



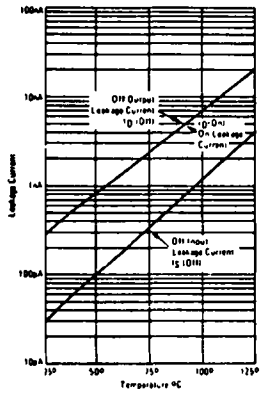
ON RESISTANCE vs. ANALOG INPUT VOLTAGE, TEMPERATURE



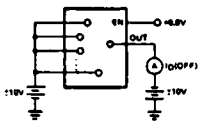
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



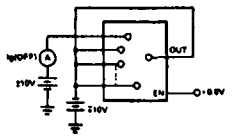
LEAKAGE CURRENT vs TEMPERATURE



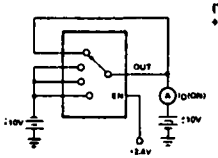
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

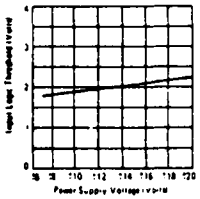


TEST CIRCUIT NO. 4*

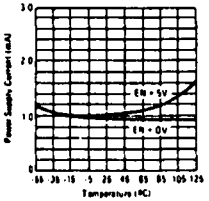


*Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for ID(OFF): +10V/-10V and -10V/+10V.)

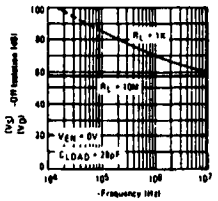
LOGIC THRESHOLD vs POWER SUPPLY VOLTAGE



POWER SUPPLY CURRENT vs. TEMPERATURE

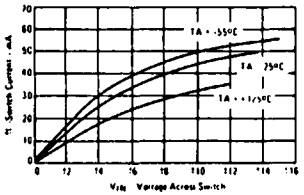


OFF ISOLATION vs. FREQUENCY

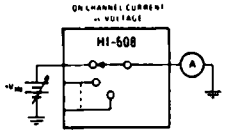


PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)

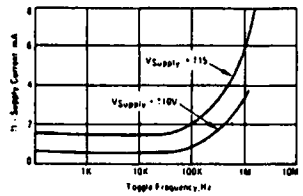
ON CHANNEL CURRENT vs VOLTAGE



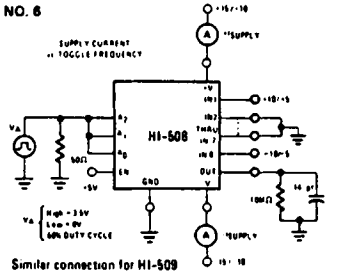
TEST CIRCUIT NO. 5



SUPPLY CURRENT vs TOGGLE FREQUENCY

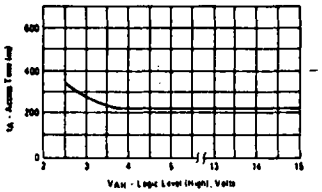


TEST CIRCUIT NO. 6

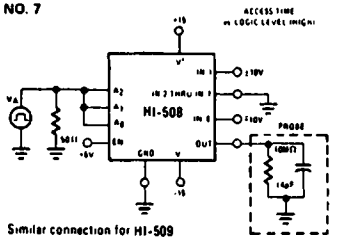


Similar connection for HI-509

ACCESS TIME vs LOGIC LEVEL (HIGH)

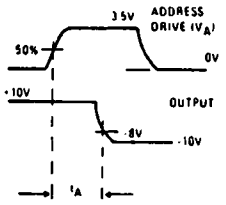


TEST CIRCUIT NO. 7

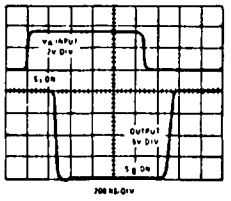


Similar connection for HI-509

SWITCHING WAVEFORMS

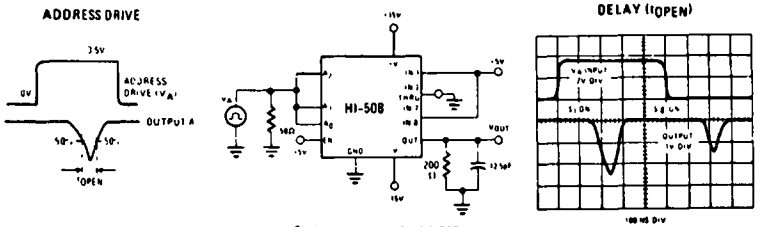


ACCESS TIME



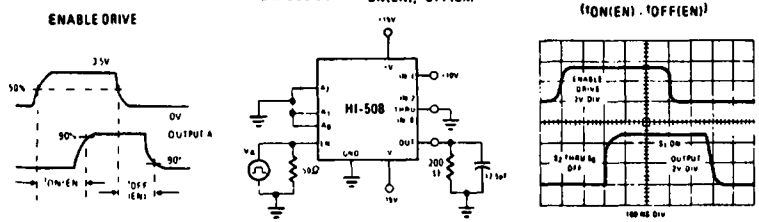
SWITCHING WAVEFORMS (continued)

TEST CIRCUIT
NO. 8



Similar connection for HI-509

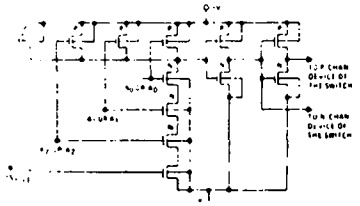
TEST CIRCUIT
NO. 9



Similar connection for HI-509

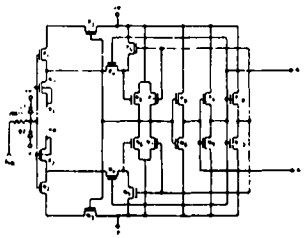
SCHEMATIC DIAGRAMS

ADDRESS DECODER



DELETE (A_2 OR $\overline{A}_2$) INPUT FOR HI-509

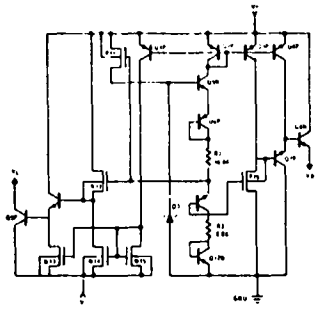
ADDRESS INPUT BUFFER
LEVER SHIFTER



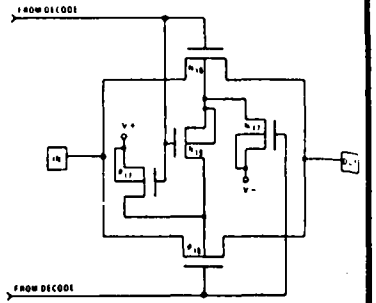
All N-Channel Bodies to V-
All P-Channel Bodies to V+ Unless Otherwise Indicated.

SCHEMATIC DIAGRAMS (continued)

TTL REFERENCE CIRCUIT

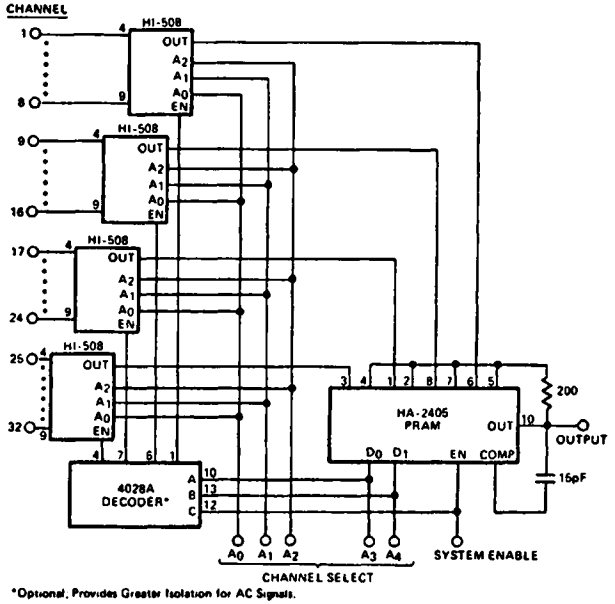


MULTIPLEX SWITCH



APPLICATIONS

32 CHANNEL BUFFERED MULTIPLEXER

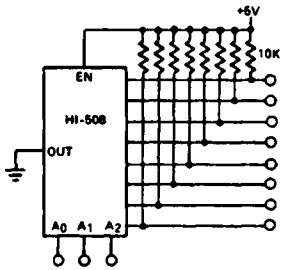


*Optional; Provides Greater Isolation for AC Signals.

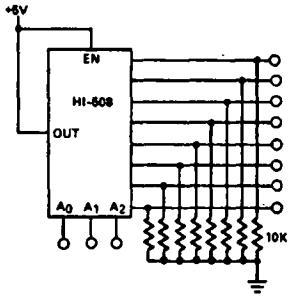
APPLICATIONS (continued)

ONE OF 8 DECODER

ACTIVE LOW



ACTIVE HIGH



DIE CHARACTERISTICS

Transistor Count		243
Die Size		86 x 79 mils
Thermal Constants	θ_{ja}	92°C/W
	θ_{jc}	37°C/W
Tie Substrate to:		$-V_{Supply}$
Process:		CMOS - DI

HARRIS

HA-1608

+10V Adjustable Voltage Reference

FEATURES

- MONOLITHIC CONSTRUCTION
- INITIAL ACCURACY +10V ± 0.010V
- OUTPUT VOLTAGE ERROR, TOTAL ± 1/4 LSB
- LOW NOISE $20\mu V_{p-p}$
- WIDE INPUT RANGE 12V TO 30V
- LOW POWER DISSIPATION 30mW
- OUTPUT SHORT CIRCUIT PROTECTION
- ADJUSTABLE OUTPUT

APPLICATIONS

- AN ECONOMICAL EXTERNAL REFERENCE FOR: HI-5608; DAC 08; AD1408, AD559
- VOLTAGE REGULATOR REFERENCE
- PORTABLE BATTERY OPERATED EQUIPMENT
- NEGATIVE 10V REFERENCE

DESCRIPTION

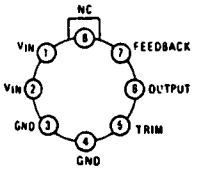
HA-1608 is a monolithic +10V adjustable voltage reference featuring accuracy and temperature stability specifications detailed exclusively for 8 bit data conversion systems. A stable +10V output is provided by a reference zener and buffer amplifier coupled with laser trimmed feedback and zener bias resistors. Long term stability is ensured through integration of all reference components into a monolithic design. Flexibility of HA-1608 is provided through an external trim control which allows the user to adjust the output voltage for binary or BCD applications without affecting overall performance.

These devices provide a total output voltage error of ± 1/4 LSB for 8 bit D/A or A/D converters. Low standby power (0.3mW) makes HA-1608 a natural selection for portable battery operated equipment, comparator references, and reference stacking circuits. These devices can also be used on -10V references.

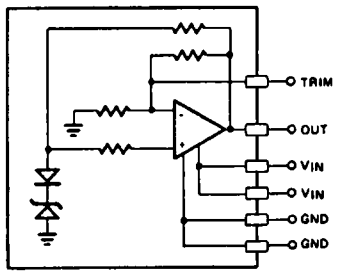
HA-1608 is packaged in 8 pin metal cans (TO-99) and the pinout is arranged for convenient replacement of other less accurate regulators in applications demanding minimal change with temperature and time. HA-1608-2 is specified for -55°C to +125°C operation while the HA-1608-5 operates from 0°C to +75°C.

PINOUT

TOP VIEW



FUNCTIONAL SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage	40V	Operating Temperature Range	
Output Short Circuit Duration	Indefinitely	HA-1608-2	-55°C to +125°C
Power Dissipation	500mW	HA-1608-5	0°C to +75°C
Storage Temperature Range	-65°C to +150°C		

ELECTRICAL CHARACTERISTICS (Note 2) (V_{IN} = +15V, I_L = 0mA, unless otherwise specified)

PARAMETER	TEMP	HA-1608-2 -55°C to +125°C MIN	TYP	MAX	HA-1608-5 0°C to +75°C MIN	TYP	MAX	UNITS
POWER INPUT CHARACTERISTICS								
Input Voltage Range, V_{IN}	Full	12	15	30	12	15	30	V
Quiescent Current, I_Q	25°C		1.9			1.9		mA
	Full			3.0			3.0	
REGULATED OUTPUT CHARACTERISTICS								
Output Voltage, V_O	25°C	9.990	10.00	10.010	9.990	10.00	10.010	V
Output Load Current, I_L	Full	10	20		10	20		mA
Line Regulation (V_{IN} = 12V to 30V)	25°C		0.006			0.006		%/V
	Full			0.015			0.015	
Load Regulation (I_L = Open to 10mA)	25°C		0.006			0.006		%/mA
	Full			0.015			0.015	
Output Voltage Error Total I_L = 0mA (Relative to 8-bit accuracy, see Definition #3)	Full			±1/4 LSB			±1/4 LSB	
Output Noise Voltage, E_N 0.1Hz to 10Hz	Full		35			35		μV_{p-p}
Dynamic Load Settling Time to ± 0.1%	25°C		2.5			2.5		μs
to ± 0.01%	25°C		5			5		
Warm-up Time (to ± 0.01%)	25°C		1			1		sec
	Full		3			3		

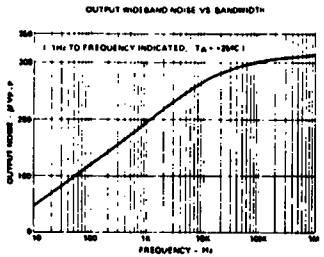
NOTES

1. Absolute maximum ratings are limiting values beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. The specified electrical characteristics apply to suggested hook-up only.

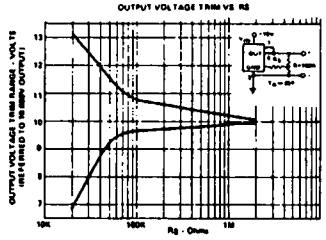
DEFINITIONS

1. Output Noise Voltage - the output noise voltage in a specified frequency band
2. Quiescent Current, I_Q - the current required from the supply to operate the device at no load condition after the device is warmed-up.
3. Output Voltage Error Total - Includes effects of Noise Voltage, Line Regulation, and $\Delta V_O TC$ relative to 8-bit (10V output) resolution where 1 LSB = one part in 256 or 39mV for a +10V output.
4. Line Regulation (%/V) - the ratio of the change in output voltage to the change in line voltage producing it; line regulation (%/V) = $[(\Delta V_O/10V) \times 100]/\Delta V_{IN}$.
5. Load Regulation (%/mA) - the ratio of the change in output voltage to the change in load current producing it, load regulation (%/mA) = $[(\Delta V_O/10V) \times 100]/\Delta mA$
6. Dynamic Load Settling Time - the time required for the output to settle to within the specified error band for a change in the load current of 1mA.

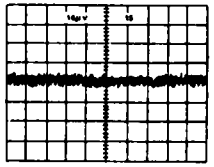
PERFORMANCE CURVES



OUTPUT WIDEBAND NOISE VS. BANDWIDTH



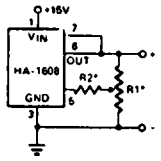
OUTPUT VOLTAGE TRIM VS. R_S



OUTPUT NOISE (0.1Hz TO 10Hz)

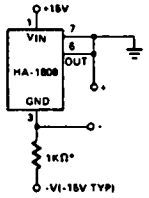
APPLICATIONS

TYPICAL HOOK-UP WITH OUTPUT TRIM



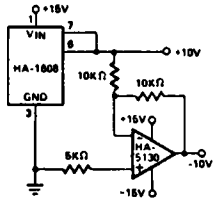
*NOTE: R_1 potentiometer value can be 10K to 100K R_2 can range from 10K to 2M

NEGATIVE 10 VOLT REFERENCE



*NOTE: The value of R may reduce the output current available to less than that specified on the data sheet.

±10V REFERENCE



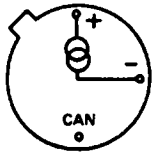
ANALOG DEVICES

Two-Terminal IC Temperature Transducer

AD590*

FEATURES
- Linear Current Output: 1μA/K
- Wide Range: -55°C to +150°C
- Probe Compatible Ceramic Sensor Package
- Two-Terminal Device: Voltage In/Current Out
- Laser Trimmed to ±0.5°C Calibration Accuracy (AD590M)
- Excellent Linearity: ±0.3°C Over Full Range (AD590M)
- Wide Power Supply Range: +4V to +30V
- Sensor Isolation from Case

AD590 FUNCTIONAL BLOCK DIAGRAM



TO-52
BOTTOM VIEW

8

PRODUCT DESCRIPTION

The AD590 is a two-terminal integrated circuit temperature transducer which produces an output current proportional to absolute temperature. For supply voltages between +4V and +30V the device acts as a high impedance, constant current regulator passing 1μA/K. Laser trimming of the chip's thin film resistors is used to calibrate the device to 298.2μA output at 298.2K (+25°C).

The AD590 should be used in any temperature sensing application below +150°C in which conventional electrical temperature sensors are currently employed. The inherent low cost of a monolithic integrated circuit combined with the elimination of support circuitry makes the AD590 an attractive alternative for many temperature measurement situations. Linearization circuitry, precision voltage amplifiers, resistance measuring circuitry and cold junction compensation are not needed in applying the AD590.

In addition to temperature measurement, applications include temperature compensation or correction of discrete components, biasing proportional to absolute temperature, flow rate measurement, level detection of fluids and anemometry. The AD590 is available in chip form making it suitable for hybrid circuits and fast temperature measurements in protected environments.

The AD590 is particularly useful in remote sensing applications. The device is insensitive to voltage drops over long lines due to its high impedance current output. Any well-insulated twisted pair is sufficient for operation hundreds of feet from the receiving circuitry. The output characteristics also make the AD590 easy to multiplex: the current can be switched by a CMOS multiplexer or the supply voltage can be switched by a logic gate output.

*Covered by Patent No. 4,123,698

PRODUCT HIGHLIGHTS

1. The AD590 is a calibrated two terminal temperature sensor requiring only a dc voltage supply (+4V to +30V). Costly transmitters, filters, lead wire compensation and linearization circuits are all unnecessary in applying the device.
2. State-of-the-art laser trimming at the wafer level in conjunction with extensive final testing insures that AD590 units are easily interchangeable.
3. Superior interference rejection results from the output being a current rather than a voltage. In addition, power requirements are low (1.5mW's @ 5V @ +25°C). These features make the AD590 easy to apply as a remote sensor.
4. The high output impedance (>10MΩ) provides excellent rejection of supply voltage drift and ripple. For instance, changing the power supply from 5V to 10V results in only a 1μA maximum current change, or 1°C equivalent error.
5. The AD590 is electrically durable: it will withstand a forward voltage up to 44V and a reverse voltage of 20V. Hence, supply irregularities or pin reversal will not damage the device.

SPECIFICATIONS (@ +25°C and V_S = 5V unless otherwise noted)

Model	AD590I			AD590J			AD590K			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
ABSOLUTE MAXIMUM RATINGS										
Forward Voltage (E + to E -)			+ 44			+ 44			+ 44	Volts
Reverse Voltage (E + to E -)			- 20			- 20			- 20	Volts
Breakdown Voltage (Case to E + or E -)			± 200			± 200			± 200	Volts
Rated Performance Temperature Range[1]	- 55		+ 150	- 55		+ 150	- 55		+ 150	°C
Storage Temperature Range[1]	- 65		+ 155	- 65		+ 155	- 65		+ 155	°C
Lead Temperature (Soldering, 10 sec)			+ 300			+ 300			+ 300	°C
POWER SUPPLY										
Operating Voltage Range	+ 4		+ 30	+ 4		+ 30	+ 4		+ 30	Volts
OUTPUT										
Nominal Current Output @ + 25°C (298.2K)		298.2			298.2			298.2		μA
Nominal Temperature Coefficient		1			1			1		μA/K
Calibration Error @ + 25°C			± 10			± 5.0			± 2.5	°C
Absolute Error (over rated performance temperature range)										
Without External Calibration Adjustment			± 20			± 10			± 5.5	°C
With + 25°C Calibration Error Set to Zero			± 5.0			± 3.0			± 2.0	°C
Nonlinearity			± 3.0			± 1.5			± 0.8	°C
Repeatability[2]			± 0.1			± 0.1			± 0.1	°C
Long Term Drift[3]			± 0.1			± 0.1			± 0.1	°C
Current Noise		40			40			40		pA/√Hz
Power Supply Rejection										
+ 4V ≤ V_S ≤ + 5V		0.5			0.5			0.5		μA/V
+ 5V ≤ V_S ≤ + 15V		0.2			0.2			0.2		μA/V
+ 15V ≤ V_S ≤ + 30V		0.1			0.1			0.1		μA/V
Case Isolation to Either Lead[4]		10^{10}			10^{10}			10^{10}		Ω
Effective Shunt Capacitance		100			100			100		pF
Electrical Turn-On Time		20			20			20		μs
Reverse Bias Leakage Current[4] (Reverse Voltage = 10V)		10			10			10		pA
PACKAGE OPTION[5]										
"H" Package TO-52		AD590IH			AD590JH			AD590KH		
"F" Package Flat Pack (F2A)		AD590IF			AD590JF			AD590KF		

NOTES

[1]The AD590 has been used at - 100°C and + 200°C for short periods of measurement with no physical damage to the device. However, the absolute errors specified apply to only the rated performance temperature range.

[2]Maximum deviation between + 25°C readings after temperature cycling between - 55°C and + 150°C, guaranteed not tested.

[3]Conditions: constant + 5V, constant + 125°C, guaranteed, not tested.

[4]Leakage current doubles every 10°C.

[5]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

TEMPERATURE SCALE CONVERSION EQUATIONS

$$°C = \frac{5}{9} \cdot (°F - 32) \qquad K = °C + 273.15$$

$$°F = \frac{9}{5} °C + 32 \qquad °R = °F + 459.7$$

Model	AD590L			AD590M			
	Min	Typ	Max	Min	Typ	Max	Units
ABSOLUTE MAXIMUM RATINGS							
Forward Voltage (E + to E −)			+44			+44	Volts
Reverse Voltage (E + to E −)			−20			−20	Volts
Breakdown Voltage (Case to E + or E −)			±200			±200	Volts
Rated Performance Temperature Range[1]	−55		+150	−55		+150	°C
Storage Temperature Range[1]	−65		+155	−65		+155	°C
Lead Temperature (Soldering, 10 sec)			+300			+300	°C
POWER SUPPLY							
Operating Voltage Range	+4		+30	+4		+30	Volts
OUTPUT							
Nominal Current Output @ +25°C (298.2K)		298.2			298.2		μA
Nominal Temperature Coefficient		1			1		μA/K
Calibration Error @ +25°C			±1.0			±0.5	°C
Absolute Error (over rated performance temperature range)							
Without External Calibration Adjustment			±3.0			±1.7	°C
With +25°C Calibration Error Set to Zero			±1.6			±1.0	°C
Nonlinearity			±0.4			±0.3	°C
Repeatability[2]			±0.1			±0.1	°C
Long Term Drift[3]			±0.1			±0.1	°C
Current Noise		40			40		pA$\sqrt{Hz}$
Power Supply Rejection							
+4V≤V$_S$≤ +5V		0.5			0.5		μA/V
+5V≤V$_S$≤ +15V		0.2			0.2		μA/V
+15V≤V$_S$≤ +30V		0.1			0.1		μA/V
Case Isolation to Either Lead		10^{10}			10^{10}		Ω
Effective Shunt Capacitance		100			100		pF
Electrical Turn-On Time		20			20		μs
Reverse Bias Leakage Current[4]							
(Reverse Voltage = 10V)		10			10		pA
PACKAGE OPTION[5]							
"H" Package TO-52		AD590LH			AD590MH		
"F" Package Flat Pack (F2A)		AD590LF			AD590MF		

CIRCUIT DESCRIPTION[1]

The AD590 uses a fundamental property of the silicon transistors from which it is made to realize its temperature proportional characteristic: if two identical transistors are operated at a constant ratio of collector current densities, r, then the difference in their base-emitter voltages will be (kT/q)(ln r). Since both k, Boltzman's constant and q, the charge of an electron, are constant, the resulting voltage is directly proportional to absolute temperature (PTAT).

In the AD590, this PTAT voltage is converted to a PTAT current by low temperature coefficient thin film resistors. The total current of the device is then forced to be a multiple of this PTAT current. Referring to Figure 1, the schematic diagram of the AD590, Q8 and Q11 are the transistors that produce the PTAT voltage. R5 and R6 convert the voltage to current. Q10, whose collector current tracks the collector currents in Q9 and Q11, supplies all the bias and substrate leakage current for the rest of the circuit, forcing the total current to be PTAT. R5 and R6 are laser trimmed on the wafer to calibrate the device at +25°C.

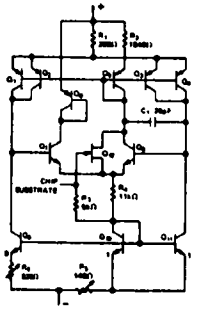


Figure 1. Schematic Diagram

Figure 2 shows the typical V−I characteristic of the circuit at +25°C and the temperature extremes.

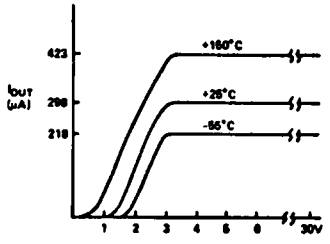


Figure 2. V−I Plot

[1] For a more detailed circuit description see M.P. Timko, "A Two-Terminal IC Temperature Transducer," IEEE J. Solid State Circuits, Vol. SC-11, p. 784-788, Dec. 1976.

EXPLANATION OF TEMPERATURE SENSOR SPECIFICATIONS

The way in which the AD590 is specified makes it easy to apply in a wide variety of different applications. It is important to understand the meaning of the various specifications and the effects of supply voltage and thermal environment on accuracy.

The AD590 is basically a PTAT (proportional to absolute temperature)[1] current regulator. That is, the output current is equal to a scale factor times the temperature of the sensor in degrees Kelvin. This scale factor is trimmed to 1μA/K at the factory, by adjusting the indicated temperature (i.e. the output current) to agree with the actual temperature. This is done with 5V across the device at a temperature within a few degrees of 25°C (298.2K). The device is then packaged and tested for accuracy over temperature.

CALIBRATION ERROR

At final factory test the difference between the indicated temperature and the actual temperature is called the calibration error. Since this is a scale factor error, its contribution to the total error of the device is PTAT. For example, the effect of the 1°C specified maximum error of the AD590L varies from 0.73°C at −55°C to 1.42°C at 150°C. Figure 3 shows how an exaggerated calibration error would vary from the ideal over temperature.

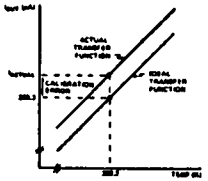


Figure 3. Calibration Error vs. Temperature

The calibration error is a primary contributor to maximum total error in all AD590 grades. However, since it is a scale factor error, it is particularly easy to trim. Figure 4 shows the most elementary way of accomplishing this. To trim this circuit the temperature of the AD590 is measured by a reference temperature sensor and R is trimmed so that V_T = 1mV/K at that temperature. Note that when this error is trimmed out at one temperature, its effect is zero over the entire temperature range. In most applications there is a current to voltage conversion resistor (or, as with a current input ADC, a reference) that can be trimmed for scale factor adjustment.

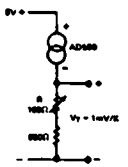


Figure 4. One Temperature Trim

[1] T(°C) = T(K) −273.2, Zero on the Kelvin scale is "absolute zero"; there is no lower temperature.

ERROR VERSUS TEMPERATURE: WITH CALIBRATION ERROR TRIMMED OUT

Each AD590 is also tested for error over the temperature range with the calibration error trimmed out. This specification could also be called the "variance from PTAT" since it is the maximum difference between the actual current over temperature and a PTAT multiplication of the actual current at 25°C. This error consists of a slope error and some curvature, mostly at the temperature extremes. Figure 5 shows a typical AD590K temperature curve before and after calibration error trimming.

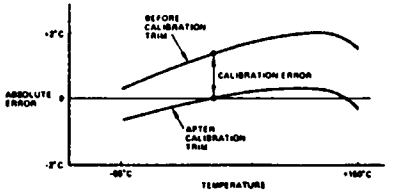


Figure 5. Effect of Scale Factor Trim on Accuracy

ERROR VERSUS TEMPERATURE: NO USER TRIMS

Using the AD590 by simply measuring the current, the total error is the "variance from PTAT" described above plus the effect of the calibration error over temperature. For example the AD590L maximum total error varies from 2.33°C at −55°C to 3.02°C at 150°C. For simplicity, only the larger figure is shown on the specification page.

NONLINEARITY

Nonlinearity as it applies to the AD590 is the maximum deviation of current over temperature from a best-fit straight line. The nonlinearity of the AD590 over the −55°C to +150°C range is superior to all conventional electrical temperature sensors such as thermocouples, RTD's and thermistors. Figure 6 shows the nonlinearity of the typical AD590K from Figure 5.

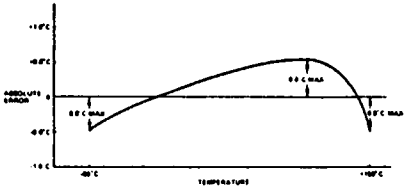


Figure 6. Nonlinearity

Figure 7A shows a circuit in which the nonlinearity is the major contributor to error over temperature. The circuit is trimmed by adjusting R_1 for a 0V output with the AD590 at 0°C. R_2 is then adjusted for 10V out with the sensor at 100°C. Other pairs of temperatures may be used with this procedure as long as they are measured accurately by a reference sensor. Note that for +15V output (150°C) the V+ of the op amp must be greater than 17V. Also note that V− should be at least −4V; if V− is ground there is no voltage applied across the device.

Understanding the AD590 Specifications

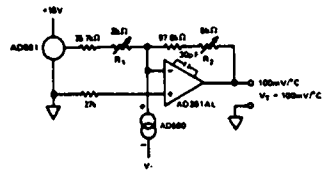


Figure 7A. Two Temperature Trim

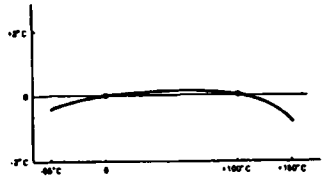


Figure 7B. Typical Two-Trim Accuracy

VOLTAGE AND THERMAL ENVIRONMENT EFFECTS

The power supply rejection specifications show the maximum expected change in output current versus input voltage changes. The insensitivity of the output to input voltage allows the use of unregulated supplies. It also means that hundreds of ohms of resistance (such as a CMOS multiplexer) can be tolerated in series with the device.

It is important to note that using a supply voltage other than 5V does not change the PTAT nature of the AD590. In other words, this change is equivalent to a calibration error and can be removed by the scale factor trim (see previous page).

The AD590 specifications are guaranteed for use in a low thermal resistance environment with 5V across the sensor. Large changes in the thermal resistance of the sensor's environment will change the amount of self-heating and result in changes in the output which are predictable but not necessarily desirable.

The thermal environment in which the AD590 is used determines two important characteristics: the effect of self heating and the response of the sensor with time.

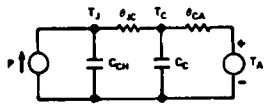


Figure 8. Thermal Circuit Model

Figure 8 is a model of the AD590 which demonstrates these characteristics. As an example, for the TO-52 package, θ_{JC} is the thermal resistance between the chip and the case, about 26°C/watt. θ_{CA} is the thermal resistance between the case and its surroundings and is determined by the characteristics of the thermal connection. Power source P represents the power dissipated on the chip. The rise of the junction temperature, T_J, above the ambient temperature T_A is:

$$T_J - T_A = P(\theta_{JC} + \theta_{CA}). \qquad \text{Eq. 1}$$

Table I gives the sum of θ_{JC} and θ_{CA} for several common thermal media for both the "H" and "F" packages. The heat-sink used was a common clip-on. Using Equation 1, the temperature rise of an AD590 "H" package in a stirred bath at +25°C, when driven with a 5V supply, will be 0.06°C. However, for the same conditions in still air the temperature rise is 0.72°C. For a given supply voltage, the temperature rise varies with the current and is PTAT. Therefore, if an application circuit is trimmed with the sensor in the same thermal environment in which it will be used, the scale factor trim compensates for this effect over the entire temperature range.

MEDIUM	$\theta_{JC} + \theta_{CA}$(°C/watt)		τ (sec)(Note 3)	
	H	F	H	F
Aluminum Block	30	10	0.6	0.1
Stirred Oil[1]	42	60	1.4	0.6
Moving Air[2]				
With Heat Sink	45	–	5.0	–
Without Heat Sink	115	190	13.5	10.0
Still Air				
With Heat Sink	191	–	108	–
Without Heat Sink	480	650	60	30

[1] Note: τ is dependent upon velocity of oil; average of several velocities listed above.
[2] Air velocity is 9ft/sec.
[3] The time constant is defined as the time required to reach 63.2% of an instantaneous temperature change.

Table I. Thermal Resistances

The time response of the AD590 to a step change in temperature is determined by the thermal resistances and the thermal capacities of the chip, C_{CH}, and the case, C_C. C_{CH} is about 0.04 watt-sec/°C for the AD590. C_C varies with the measured medium since it includes anything that is in direct thermal contact with the case. In most cases, the single time constant exponential curve of Figure 9 is sufficient to describe the time response, T(t). Table I shows the effective time constant, τ, for several media.

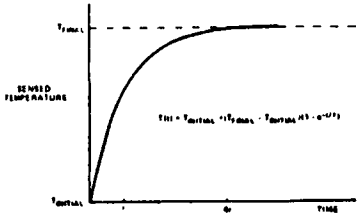


Figure 9. Time Response Curve

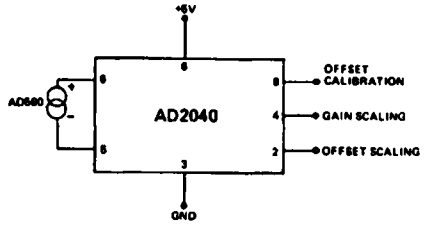


Figure 10. Variable Scale Display

Figure 10 demonstrates the use of a low-cost Digital Panel Meter for the display of temperature on either the Kelvin, Celsius or Fahrenheit scales. For Kelvin temperature Pins 9, 4 and 2 are grounded; and for Fahrenheit temperature Pins 4 and 2 are left open.

The above configuration yields a 3 digit display with 1°C or 1°F resolution, in addition to an absolute accuracy of ±2.0°C over the -55°C to +125°C temperature range if a one-temperature calibration is performed on an AD590K, L, or M.

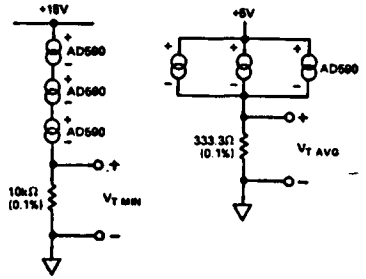


Figure 11. Series & Parallel Connection

Connecting several AD590 units in series as shown in Figure 11 allows the minimum of all the sensed temperatures to be indicated. In contrast, using the sensors in parallel yields the average of the sensed temperatures.

The circuit of Figure 12 demonstrates one method by which differential temperature measurements can be made. R_1 and R_2 can be used to trim the output of the op amp to indicate a desired temperature difference. For example, the inherent offset between the two devices can be trimmed in. If V+ and V- are radically different, then the difference in internal dissipation will cause a differential internal temperature rise. This effect can be used to measure the ambient thermal resistance seen by the sensors in applications such as fluid level detectors or anemometry.

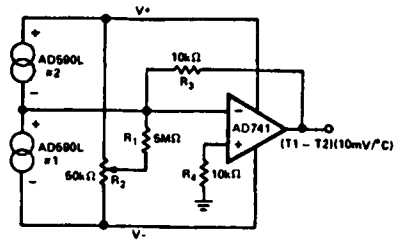


Figure 12. Differential Measurements

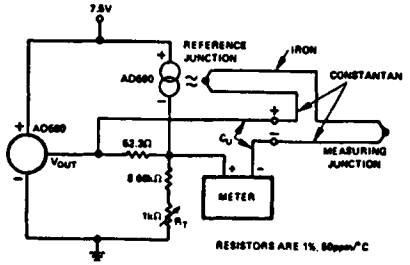


Figure 13. Cold Junction Compensation Circuit for Type J Thermocouple

Figure 13 is an example of a cold junction compensation circuit for a Type J Thermocouple using the AD590 to monitor the reference junction temperature. This circuit replaces an ice-bath as the thermocouple reference for ambient temperatures between +15°C and +35°C. The circuit is calibrated by adjusting R_T for a proper meter reading with the measuring junction at a known reference temperature and the circuit near +25°C. Using components with the T.C.'s as specified in Figure 13, compensation accuracy will be within ±0.5°C for circuit temperatures between +15°C and +35°C. Other thermocouple types can be accommodated with different resistor values. Note that the T.C.'s of the voltage reference and the resistors are the primary contributors to error.

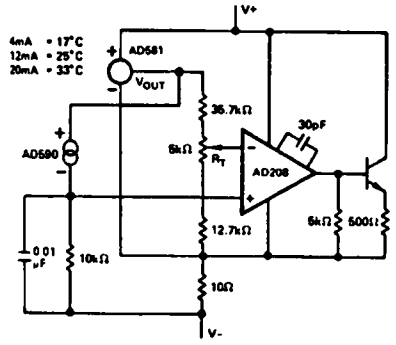


Figure 14. 4 to 20mA Current Transmitter

Figure 14 is an example of a current transmitter designed to be used with 40V, 1kΩ systems; it uses its full current range of 4mA to 20mA for a narrow span of measured temperatures. In this example the 1µA/K output of the AD590 is amplified to 1mA/°C and offset so that 4mA is equivalent to 17°C and 20mA is equivalent to 33°C. R_T is trimmed for proper reading at an intermediate reference temperature. With a suitable choice of resistors, any temperature range within the operating limits of the AD590 may be chosen.

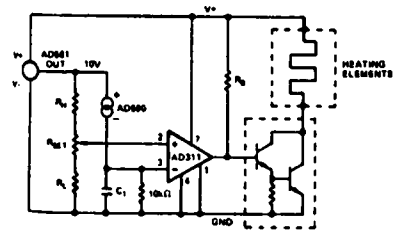


Figure 15. Simple Temperature Control Circuit

Figure 15 is an example of a variable temperature control circuit (thermostat) using the AD590. R_H and R_L are selected to set the high and low limits for R_{SET}. R_{SET} could be a simple pot, a calibrated multi-turn pot or a switched resistive divider. Powering the AD590 from the 10V reference isolates the AD590 from supply variations while maintaining a reasonable voltage (~7V) across it. Capacitor C_1 is often needed to filter extraneous noise from remote sensors. R_B is determined by the β of the power transistor and the current requirements of the load.

Figure 16 shows how the AD590 can be configured with an 8-bit DAC to produce a digitally controlled set point. This

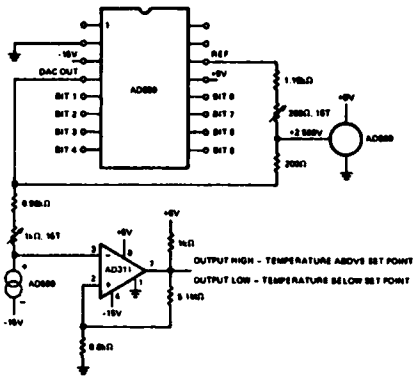


Figure 16. DAC Set Point

particular circuit operates from 0 (all inputs high) to +51°C (all inputs low) in 0.2°C steps. The comparator is shown with 1°C hysteresis which is usually necessary to guard-band for extraneous noise; omitting the 5.1MΩ resistor results in no hysteresis.

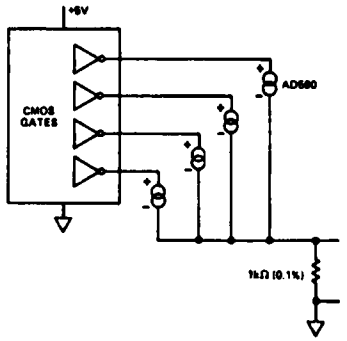


Figure 17. AD590 Driven from CMOS Logic

The voltage compliance and the reverse blocking characteristic of the AD590 allows it to be powered directly from +5V CMOS logic. This permits easy multiplexing, switching or pulsing for minimum internal heat dissipation. In Figure 17 any AD590 connected to a logic high will pass a signal current through the current measuring circuitry while those connected to a logic zero will pass insignificant current. The outputs used to drive the AD590's may be employed for other purposes, but the additional capacitance due to the AD590 should be taken into account.

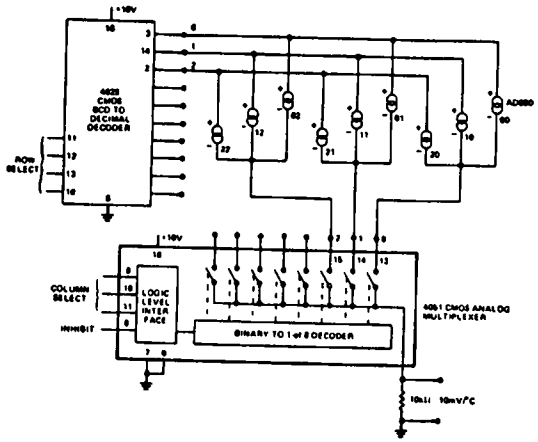


Figure 18. Matrix Multiplexer

CMOS Analog Multiplexers can also be used to switch AD590 current. Due to the AD590's current mode, the resistance of such switches is unimportant as long as 4V is maintained across the transducer. Figure 18 shows a circuit which combines the principal demonstrated in Figure 17 with an 8 channel CMOS Multiplexer. The resulting circuit can select one of eighty sensors over only 18 wires with a 7 bit binary word. The inhibit input on the multiplexer turns all sensors off for minimum dissipation while idling.

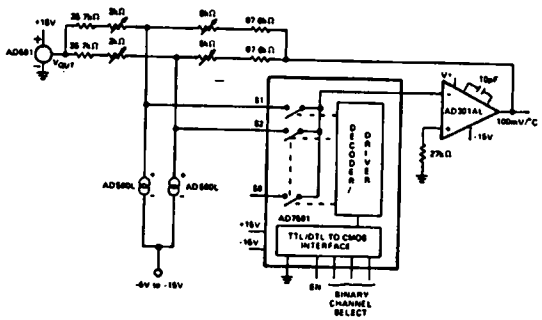


Figure 19. 8-Channel Multiplexer

Figure 19 demonstrates a method of multiplexing the AD590 in the two-trim mode (Figure 7). Additional AD590's and their associated resistors can be added to multiplex up to 8 channels of ±0.5°C absolute accuracy over the temperature range of -55°C to +125°C. The high temperature restriction of +125°C is due to the output range of the op amps; output to +150°C can be achieved by using a +20V supply for the op amp.