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THE DATA SET, MODULE TYPE M1

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1.0 INTRODUCTION

This manual describes the operation of the Data Set (DS), module type M1, and was written to serve as the trouble shooting and maintainance guide for this component of the Monitor and Control System (M&C). This manual is an updated version of an earlier Data Set manual; The Handyman's Guide to the Data Set, Module Type M1, VLA Technical Report No 30. Included is interfacing information which may be useful for those who design command or data channels which interact with the Data Set.

The function of the Data Set is to execute computer control command messages and to gather and format monitor data messages for the control computers. The Data Set is typically installed in a VLA electronics rack and services all the devices in the rack which require computer control or monitoring. The Data Set has a large command/data capacity; none of the VLA Data Sets have been used to capacity.

The Data Set is the prime focus of interest in this manual but functions of the Antenna Buffer and Central Buffer are described where it is necessary to explain aspects of the Data Set operation. For a description of these Buffer units, the reader is referred to "Overview of the Monitor and Control System", VLA Technical Report No 44. The Data Sets and devices serviced by them are depicted in Figure 1, the Monitor and Control System Block Diagram. The Antenna, Central and System Buffer manuals, (VLA Technical Reports Nos 59, 60 and 61 respectively) describe the interactions between these buffers and the Data Set. Figures 2 and 3 depict the Monitor and Control System timing relationships. Figure 4 depicts the message formats.

2.0 DATA SET DESCRIPTION

The Data Set is a digital machine which executes time-serial digital control command messages by controlling the states of controlled devices in accordance with the command message arguments. The Data Set also gathers analog and digital monitor data from these devices and formats the data into time-serial digital monitor data messages which are routed to the control computers for diagnostic purposes.

The Data Set is passive; it performs a command or data function only when stimulated by an Antenna, Central or System Buffer. The Buffer emits a stream of command, monitor data and data request messages and depending upon the character of the messages, the Data Set executes the command and monitor data operation.

The command messages originate in the central control computers and are routed to the Data Set via the Serial Line Controller, Central (or System) Buffer, Local Oscillator/Waveguide System

(LO/WG), and Antenna Buffer. The monitor data messages are polled from the Data Sets by the Buffers, temporarily stored and then transmitted to the control computers via the Antenna Buffer, LO/WG transmission system, the Central (or System) Buffer and SLC.

The Data Set is packaged in a 1-wide standard VLA module and contains wire-wrapped logic connector boards for the digital logic chips and a removeable (for alignment and test) analog multiplexer and A/D converter PC board. A front panel numeric LED indicates the Data Set address and flashing green and red LEDs indicate monitor data message output activity and malfunctioning signal conditions. Front panel test points permit direct observation of important logic signals for diagnostic purposes. The Data Set physique is depicted in the Data Set Top Assembly Drawing, D13720P73 and the Illustrated Parts Breakdown (Fig 10) in the rear of this manual.

2.1 MESSAGE FORMAT DESCRIPTION

Figure 4 depicts the format of the M&C Command and Monitor Data messages and the "Q" character format. The Data Set accepts and outputs the NRZ form of these messages. All M&C messages are prefixed by an "S" (for start) character which signals that a message immediately follows. The bit rate of the S character is 5 usec/bit and the message bit rate is 10 usec/bit; thus the S character is unique and always distinguishable from message data patterns. The message consists of five 8-bit data bytes; the first byte contains a 5 bit DCS ddress (which can range from 0 to 31, 0 to 37, octal) and a 3 bit Data Set Address (DSA) which can range from 0 to 7. The second byte is the Multiplex Address which designates a particular command or data channel. The third, fourth and fifth bytes are components of a 24 bit command or monitor data argument. In the case of an analog data message, the 24 bit argument consists of two 12 bit values resulting from the conversion of two analog signals by the Data Set analog-to-digital converter. In all address and argument values, the first bit (in time) is the most significant bit.

The "Q" (for query) character is used by the CB, SB and AB to poll data from a Data Set and is sequentially directed to Data Sets via the Buffer's Data Set Command Ports. The bit rate of the Q character is 5 usec/bit.

2.2 DATA SET I/O SIGNALS

- Data Set Input Port, - an optically isolated (in the DS), TTL level input port which receives low-true command and monitor data messages and the data request (Q) character.

- Data Set Monitor Data Port, - a TTL level, low-true monitor data message output to the Buffer.

- Data Tap Port, - a TTL level, low-true output to the Data Tap which may be connected to the Data Set Input Port.

- 5 Mhz, - a 5 Mhz, 1 volt (nominal) clock which drives the Data Set logic. The clock may be either a 1 volt peak, (nominal) sine wave signal from the L8 distribution system or a TTL level clock from the Antenna Buffer.

- Analog Inputs, ALGI-0 .. ALGI-7, - eight differential, +/- 10 volt level analog signal inputs to the A/D converter analog multiplexer from controlled devices.

- Digital Command Output Ports, - three TTL level, low-true command output ports consisting of clock, strobe and data lines and returns.

- Digital Monitor Input Ports, - four TTL level, low-true digital monitor input ports consisting of clock, strobe and data lines and returns.

- SMA-0 .. SMA-3, - four TTL level, low-true lines and returns which are used by devices to decode device select addresses. After the completion of a command or monitor operation, these lines are defaulted to the high (false) state.

- DSA address lines, - three low-true, TTL lines which define the Data Set address. These lines are hard-wired to logic common on the back of the bin to define the Data Set address.

- DCS address lines, - five low-true, TTL level lines to the monitor data output register which define the DCS address of the monitor data message output by the Data Set. These lines have no relevance in Data Sets connected to the Antenna Buffer because the AB dubs the DCS address into the monitor data messages in the process of polling antenna Data Sets. These lines must be hard-wired to ground when Data Sets are used with the System or Central Buffers.

In performing a command operation, the Data Set detects, loads and tests the command message for parity errors. If the message contents satisfy the error detection logic, the Data Set address (DSA) components of the message are compared with the hard-wired (in the bin) Data Set address to determine if the command is directed to it. If so, then the command information and multiplex address are stored for execution of the command. In executing the command the multiplex address is decoded to activate output data, clock and strobe lines causing the command to be serially loaded into the multiplex address-designated device. The DCS address component of the command message is not decoded by the Data Set; the Buffers store only the commands which pertain to their associated antenna so that the Data Sets

need not test for DCS address relevance.

The Data Set is caused to perform a monitor data operation when it detects a Data Request character (Q) emitted by the associated Buffer. The Data Set then gathers digital and analog data which is formatted into a monitor data message along with multiplex address, Data Set address, DCS address, and message parity components. In the case of analog monitor data messages, there are two analog values and only one multiplex address. The multiplex address for the second analog value is implied and is the multiplex address + 1. The monitor data message is then serially output to the Buffer. The monitor data control logic has a 200 microsecond delay for analog data settling and A/D conversion.

The Data Set monitor data sampling operations are time and multiplex address ordered. The Buffer evokes two monitor data messages (MW-1-MW-2) from each Data Set in one VLA machine cycle. The multiplex addresses for the first monitor data (MW-1) message are derived from an address program stored in a programmable read-only-memory (EPROM) which may be programmed to produce any sequence of multiplex addresses within a 192 message period. The EPROM may be programmed to sample channels at rates between 1 sample/10 seconds to 1 sample/VLA machine cycle. The multiplex addresses for the second monitor data (MW-2) message are derived in either of two ways:

1) Sequential mode in which 128 analog signals are sampled twice and 64 digital channels are sampled once over a ten second period.

2) Selected mode in which the multiplex address is set to a fixed channel specified by the control computers. This mode permits intensive (1 sample/VLA cycle) sampling of the designated channel for diagnostic purposes.

The reason that there are two different address-peculiar monitor data messages per VLA cycle is that the control computer operating system uses the EPROM address-designated (MW-1) data for diagnostic and control purposes which are fixed and constant. The second monitor word is provided for investigative and high sampling rate (in the Select mode) monitoring of device functions independent of the control computer programs. Figure 7 depicts typical MW1, MW2 and System overlay relationships.

Commands directed to the Data Set designate the selected address and control Select/Sequential modes. In addition, the EPROM address counter may be initialized to a base value by a Data Set Reset command so that all Data Sets with identical EPROMs sample the same data in any given machine cycle.

The monitor data messages emitted by the Data Set are

rebroadcast by the Antenna Buffer as they are stored in the AB monitor data memory. The rebroadcast data is sometimes called "gossip data". This rebroadcasting enables a Data Tap (see the Data Tap manual for details) to be connected to any Data Set in the antenna for visual display of command or monitor data messages. The Data Set is inhibited from responding to it's own monitor data messages to prevent positive feedback perturbations to the logic.

When the Data Set detects an error-tainted (ie. parity error), command or monitor data message, parity error detection logic inhibits the execution of the message (if it is a command); the multiplex and Data Set address of the error-tainted message are stored for future monitor data readout by multiplex address 200 (octal). A flag bit is set if the error is detected in the multiplex address component of the message. A binary counter in the error data logic counts the parity errors that occurred in the intervals between address 200 data readout messages. The counter is reset to zero as part of the readout process. Because the Data Set is unable to respond to it's own monitor data messages, it cannot test or report it's own malfunctioning output.

Analog data is multiplexed in the Data Set by an 8 channel differential input multiplexer-buffer amplifier. Each of these inputs is (typically) driven by an 8 or 16 channel single-ended or differential multiplexer located in the modules serviced by the Data Set. The lower four bits of the multiplex address drive the remote multiplexer and the next three bits drive the eight input Data Set multiplexer. The multiplex address is incremented after the first analog to digital conversion so that the second analog data channel can be selected and converted.

The output of the Data Set multiplexer/amplifier drives a sample and hold unit which "holds" the analog level constant for the analog to digital converter. The Data Set conversion control logic provides a 30 microsecond settling delay for the analog signal before it is held; the A/D converter causes the data to be loaded into a storage register for subsequent readout when the monitor data is output.

The major specifications of the analog multiplexer - A/D converter are:

Analog input range - +10.235 to - 10.240
Multiplexer "on" input impedance - 100 megohms
Analog settling delay - 30 microseconds
Multiplexer "on" resistance - 2 Kohms/line
A/D conversion period - 50 microsaconds
Common moderejection - > 60 db with a 1 Kohm source unbalance
Conversion code - 12 bit 2's complement binary, 5 mv/bit
Settling time - < 4 microseconds to .01% of full scale

Cross talk - < 1mv, P-P @ 10 Khz
Input over voltage tolerance - 35 V, max

2.3 MODULE CONTROL/DATA INTERFACE

Each module serviced by a Data Set contains a small control/data interface driven by the Data Set which decodes addresses and accepts and stores command information. Under control of the Data Set, the control/data interface samples the device binary states and serially unloads it to the Data Set. Analog data is routed to the Data Set A/D converter by either single-ended or differential analog multiplexers in the control/data interface. Many different implementations of control/data interfaces are possible to service command, analog or binary data channels. The most general implementation incorporates all three functions and consists of about 13 chips which can decode and store a 24 bit command, load and output 24 bits of binary data and multiplex 8 channels of differential analog data. Figure 9 shows the logic diagram of a typical control/data interface. In effect these control/data interfaces are an extension of the Data Set logic. The use of these interfaces located in the various VLA functional modules enables the Data Set to service a great many command and data channels.
Figure 9 depicts the analog and digital circuitry of a typical Control/Data Interface

2.4 DATA SET CAPACITY

The full command/data capacity of the Data Set is:

1) 128 analog channels, converted to 12 bit 2's complement digital values.
2) 64 channels of 24 bit binary data (1536 bits).
3) 48 channels of 24 bit binary command (1172 bits).

The following table shows the Address/Function assignments:

MULTIPLEX ADDRESS*			FUNCTION	CAPACITY
0	to	17	Analog data input, ALGI-0	16 channels
20	to	37	Analog data input, ALGI-1	|
40	to	57	Analog data input, ALGI-2	|
60	to	77	Analog data input, ALGI-3	|
100	to	117	Analog data input, ALGI-4	|
120	to	137	Analog data input, ALGI-5	|
140	to	157	Analog data input, ALGI-6	|
160	to	177	Analog data input, ALGI-7	16 channels
200			Parity data readout	
201	to	217	Binary monitor data, DIGI-0	15 channels
220	to	237	Binary monitor data, DIGI-1	16 channels

240	to	257	Binary monitor data, DIGI-2	|
260	to	277	Binary monitor data, DIGI-3	|
300			Set MW 2 to select mode	
301			Set MW 2 to sequential mode	
302			Reset EPROM address counter	
303	to	317	Reserved for future Data Set use	
320	to	337	Binary command, DIGO-0	16 channels
340	to	357	Binary command, DIGO-1	|
360	to	377	Binary command, DIGO-2	|

* addresses in octal notation

3.0 DETAILED FUNCTIONAL DESCRIPTION

This section contains a description of the theory of operation and is broken into sections which are keyed to the Data Set Block Diagram, (Figure 4). The Data Set logic is straightforward and easily grasped by those with digital backgrounds, therefore the logic descriptions in the sections are brief and emphasize the most important aspects of the logic rather than exhaustive discussions of the function performed by each logic element. The logic is discussed in the order of increasing functional dependency.

Figure 8 depicts the waveforms which may be observed on the front panel test point connector.

The reader should study the timing diagrams referenced by the description as they graphically illustrate logic operations; they are a replica of the timing waveforms which may be observed with an oscilloscope. The timing diagrams are keyed to the signal source points by the location designator and pin number. Important causitive relationships are indicated by arrows from one waveform to others. Clocking relationships are implied by an up or down arrow which indicates the portion of the waveform which causes driven devices to be triggered. Where it is important to the discussion, logic states, timing durations, delays or frequencies are marked on the diagrams. A linear time base is employed in all diagrams but delays may be exxagerated for emphasis of race or delay considerations. Waveform sampling is indicated by arrows, tick marks and the letter S to denote sampling.

The discussions refer to the Model D and E versions of the Data Set which differ in the type of EPROM which stores the data sampling program. The Model D units use an Intel 1702A, (8 bit x 256 byte) word EPROM which must be changed when relocating Data Sets between racks. The Model E units use an Intel 2716 (8 bit x 2 k byte) EPROM which contains all data sampling programs. The three DSA lines (hardwired on the rear panel) select the program

appropriate for the rack location, (e.g racks A,B,C,D); this simplifies the logistics of swapping Data Sets. Earlier models of the Data Set were upgraded to levels D and no longer exist. Model E Data Set construction started in the spring of 1986. Logic diagrams for both models are found in the rear of this manual.

3.1 5 Mhz CLOCK DETECTION AND DOUBLING LOGIC

An externally provided 5 Mhz, 1.0 volt peak (nominal) sine wave signal is the clock source for the Data Set. A 72710 analog comparator (A30B) and 7404 inverter square the 5 Mhz signal to drive the harmonic doubler A14 which doubles the 5Mhz clock. The A14 tank circuit rings at 10 Mhz and is "kicked" by the positive-going edge of the drive from inverter A1002. A10 is a 74S04 because of it's high switching speed which produces sharp edged pulses for the harmonic generator. The drive edges are differentiated by the 10 pf/1 Kohm circuit in the MPS 918 base circuit and the positive-going edge provides a narrow current pulse to the transistor base. Inverter A1004 is caused to operate in a quasi-linear region by the 2 Kohm resistor in A14. The output of A1006 is the highest frequency clock source in the Data Set and all clock rates are derived from it. **A10 must be a 74S04; the high switching speed of the Schottky logic is important for the doubler circuit's operation.**

3.2 INPUT SIGNAL SYNCHRONIZATION LOGIC

Optically-coupled isolator A30A detects the Data Set command/Q signals from the Antenna or Central Buffers and provides ground isolation between the Data Set and the Buffers. The data is clocked into shift register A25 by the 10 Mhz clock. 1/0 or 0/1 data edges are detected by exclusive or gate A2403 which presets counters A12 and A13 to a count state of 41. This counter is incremented by the 10 Mhz clock to a count of 90 which then causes the counter to be reset to the 41 state via the 7402 D3004. Timing Diagram 1 depicts the timing relationships. Output A1313 is a 200 Khz waveform whose positive-going edge is delayed 2 usec from the 1/0 or 0/1 signal edges. The 200 Khz signal is the clock for counters A16 and A11 and also the sample clock for shift register A18. The purpose of this delay is to sample the input signal at the approximate center of the S character bits. A 1 Mhz clock is tapped off counter A1211. The use of this clock is discussed later.

3.3 MESSAGE DETECTION/LOADING LOGIC

Shift register A18 is serially loaded with the input data stream by the phase adjusted 200 Khz clock from A1313 described above. Gates A2610 and A2710 detect a data request message (Q) or a start of a command or monitor data message (S) in shift

register A18. When the last 8 bits of the Q character are loaded into A18, gate A2610 goes true for 5 usec. This Q detection initiates the monitor data gathering sequence described later.

Similarly gate A2710 goes true for 5 usec when the last 8 bits of the start (S) character are loaded into A18. This S detection activates the message load counter consisting of flip-flops B2106 and synchronous counters A16 and A11. The counter generates 45 shift clocks to serially load the message into the message input registers B30, B25, B15, and B10. See timing diagram 2 for details. Counter A16 operates with a radix of 9 to program a parity test of the message data on a byte by byte basis. The parallel contents of register B30 are presented to B26, a parallel parity generator/checker, and at the count of 9 the output of B26 will enable the J input of flip-flop B2110. If there is a parity error, B2110 will be clocked true. At the completion of the loading sequence, the counter is shut off by the fall of A1111 which also triggers one-shot C1810. The strobe output of C1810 causes parity error data to be stored in the error data register (discussed later) if a parity error occurred in the message.

If the message passes the parity test, the C1810 strobe is enabled onto comparator B8 which compares the message Data Set address with the hard-wired (in the bin) DSA. If the addresses agree, B8 A=B output passes the B2110 strobe to gate B2914 which further tests the message to determine if it a command by anding mux address bits 128 and 64 which are both true for command messages. This test is necessary because the message could be a rebroadcast monitor data message which is of no consequence to the Data Set other than the parity test.

If the message is a command message addressed to the Data Set in discussion, then the 24 command argument bits are parallel loaded into registers B24, B19 and B14. The Cmd busy flip-flop B1111 is also set by B2914. The command multiplex address is caused to be stored in the multiplex address register A15 and A2 via multiplexers D21, D22, D26 and D27. The multiplexers are pointed to the portions of the message loading registers which contain the command multiplex address by gates D0506/10, D2406/10 and the Cmd Busy flip-flop B1111. The mux address is strobed into registers A15 and A2 by the trailing edge of one shot C3009. C3009 is triggered by the trailing edge of one shot C1810 and provides 100 ns of delay to enable the mux address to propagate through the multiplexers and stabilize at A15 and A2 before being clocked by C3009. If a parity error should occur, one shot C1807 is triggered on to provide a stretched illumination of the front panel red parity error LED.

Note that the parity test logic operates on <u>both</u> command and monitor data messages and causes error data to be stored for both types of messages. Thus a parity error in a monitor data message

is heard by all Data Sets in the antenna and is multiply reported. Also note that the DCS address is not tested or used in the loading process other than in the parity error tests.

3.4 COMMAND OUTPUT LOGIC

In the previous section we saw how the command messages were loaded, error tested and parallel stored. The storage process is completed by about 200 ns after the last load shift clock. The 24 command argument bits are immediately unloaded to the command destination which leaves the the message loading circuitry free to accept the next message which may immediately follow. The unload operation is initiated by gate B22914 (mentioned above) which sets control flip flops B1105 and C1511. B1105 enables counters B17 and B22 to count out 24 100 Khz shift clocks and one clock time later a strobe pulse. The 24 command argument bits, shift clocks and strobe are enabled to one of three sets of digital outputs by address decoder B12 which is driven by the four high order bits of the multiplex address. The four lower order bits of the multiplex address are decoded by the commanded devices and enable the information output on the three sets of outputs to be loaded and stored. For details on the usage of these signals in a controlled device see Section 6 for an example of a typical command channel logic diagram.

The trailing edge of the strobe pulse resets the Cmd Busy flip flop B1111. B1111 forces the multiplex address registers A2 and A15 to be cleared via the DS busy gate B0613. Thus the multiplex address storage registers are cleared to address 0 between command operations. Timing Diagram 3 shows the time relationships of the command output logic.

3.5 MW-1/MW-2 AND MUX LOAD SEQUENCE

When a data request character (Q) is detected (see Section 3.3), it toggles D2305 which controls the MW-1/MW-2 steering of the multiplex address multiplexers D21, D22, D26 and D27.. D2305 also increments the EPROM address counters D17 and D18. The reader will remember that MW-1 (ie. the first monitor data message evoked by the Buffer in a VLA machine cycle) contains data selected by the program residing in the EPROM. MW-2 is associated with either a computer-specified (ie. selected address) or a sequentially scanned address. The MW-1/MW-2 ordering is accomplished by the two one-shots D0405 and D0409, which are triggered by the Q detection gate A2610. The Q characters occur in pairs, (1 pair/VLA machine cycle) and are separated by either 1000 usec or 4.5 milliseconds depending upon which Buffer drives the Data Set. One-shot D0406 is retriggerable with a period of of 5 milliseconds; this is greater than the interval between the Buffer's Q character outputs. This delay causes flip-flop D2305 to be left in the proper state to steer the EPROM address to the address register when the

Buffer requests the first monitor word in the VLA cycle. Shift register D9 is a clock phase generator which generates a time delayed clock to allow the multiplex address enough time to propagate through the address multiplexer to the address storage register. Other functions of the clock phase generator are initialization of the 200 Khz divider A0705, triggering of the output data sequencing logic, loading of the multiplex address, Data Set address and DCS addresses in C22 and C27, and the "S" character bits in registers C24 and C26. Timing diagram 4 shows the clock terms generated by the clock phase generator D9.

Because of it's 24 pin package, the EPROM is physically located on the analog multiplexer - A/D board for packaging convenience.

3.6 MONITOR DATA ADDRESS FORMULATION

Counters D17 and D18 are incremented by the leading edge of the Q detection gate A2610 and have a radix of 192; thus the EPROM address recycle rate is 192 addresses in 10 seconds. Since counters D17 and D18 are incremented by the leading edge of the Q detection gate, the address program contents of the EPROM have about 5 microseconds to settle through the multiplexer before they are loaded into the multiplex address registers A2 and A15 by the logic descsribed above. This same settling time also applies to the Select and Sequential address data.

The Select address data is stored in shift register C21 which is loaded by a command addressed to multiplex address 300 (octal). When this command is detected, the lower 8 bits of the command are shifted into C21 and the Select/Sequential flip-flop is set to the select state. This flip-flop then causes the multiplex address multiplexer to route the selected address stored in C21 to the address registers A2 and A15.

The sequential address is formed by 2-to-1 multiplexers D19 and D20 and full adder D13 under control of gates D2903, D2906, D1203, C1213,C0514 and C0506. The sequential addresses scan all 128 analog addresses twice in ten seconds and the 64 digital addresses once in ten seconds. The digital address scan is broken into two scans of 32 addresses each between analog address scan. The base for the sequential address counter is the EPROM address counter which sequences from 0 to 191 and is incremented once each VLA cycle by the Q detector logic.

The Sequential address algorithm is very simple and involves using the EPROM address counter directly, doubling the counter value and/or adding 64 to the count. The algorithm is depicted on the next page, (Np = Prom address, Ns = Sequential Address):

EPROM address counter range	Sequential address counter range	Rule
0 <= Np <= 63	0 <= Ns <= 126	Ns = 2Np
64 <= Np <= 95	128 <= Ns <= 159	Ns = Np + 64
96 <= Np <= 159	0 <= Ns <= 191	Ns = 2Np
160 <= Np <=191	160<= Ns <= 191	Ns = Np

The control gates enable or inhibit the add 64 and left or no shift logic operations in the adder and multiplexers on the basis on the Prom address counter states. The contents of the multiplex address register are used extensively in the Data Set to control the distribution of monitor data and command output clocks, strobes and data. The lower four bits of the address register are buffered out of the Data Set as low-true lines by buffer A8. After the completion of a command or monitor data message output, the D5 busy logic A17 and B6 force the multiplex address register to the zero state. This makes the sub-mux address assume the zero state; • all control/data interfaces will sense this state. The external analog multiplexers will all select the zero address channel and route it to the Data Set ALGI-0 analog input. The Data Set is not perturbed by the presence of this signal since the multiplexer and A/D are inactive.

3.7 ANALOG DATA GATHERING SEQUENCE

Counter C17 and C1605 are enabled by control flip-flop C1611 which is set by the clock pulse generator discussed in Section 3.5. The multiplex address had been loaded 1 usec earlier in multiplex address registers A2 and A15. The counter is incremented by 100 Khz clocks from A0705 to generate sequential control terms for the Sample and Hold unit and A/D Converter. At 30 usec, the Sample and Hold is set to the hold mode; at 40 usec, the A/D start conversion input is triggered by one-shot D1006. After the 50 usec duration conversion, the A/D end of conversion line drops and triggers one-shot D1010 which resets flip-flop A0710 to reset the Sample and Hold unit to the sample mode. Gate C1913 steers the 500 ns one-shot to load the A/D data into shift registers C1 and C2. At 100 usec, counter C17 increments the multiplex address registers (if the mux address is in the analog data address range) which then causes the next sequential analog channel to be selected by the external analog multiplexer. With the new analog signal, the Sample and Hold unit, start conversion, end of conversion and data storage operations occur at 130, 140, and 190 usec respectively. At 200 usec, flip-flop C1610 is reset and the output data shift operation is initiated by setting flip-flop C1505. Gate C1913 generates a binary data strobe which is used to cause binary data sources to paralell load output shift registers for an impending unload shift.

3.8 OUTPUT DATA SEQUENCING LOGIC

The data output operation consists of serially shifting out the DCS, DSA & MUX addresses, A/D data, parity bits and the "S" message prefix. When the message emerges at the output port it will be in the M&C message format. Counters C14 and D16 are incremented by 100 Khz clock pulses from A0705 and generate sequencing and control terms which program the output of the monitor data message. Counter C14 operates with a radix of 9 to cause parity data to be output at the appropriate points in the output message. Shift register B27 is a Johnson counter with a radix of 10 and is incremented by 1 Mhz clock pulses from A1211. The counter is initialized to an all zero state by flip-flop C1505. When C1505 goes high at the start of the output sequencing operation, a wave of five "1"s followed by a wave of five "0"s circulate around the register. The gates driven by B27 generate time-phased clocking terms to clock all the monitor data registers. Timing Diagram 5 shows these waveforms and the basic logic. The logic driven by these terms are: parity counter C8, output register C29 and C26, data register C1, C2 C6 and C11, parity error registers B5 and C9 and the binary data channels from the external device controllers. These sample clocks are time-phased to avoid race conditions in clocking the long string of concatenated shift registers; this makes the Data Set very tolerant of logic delays in external binary data channels. Timing Diagram 6 and 7 show the generation and usage of these clock terms. Under multiplex address control, multiplexer C7 selects either the A/D converted data or binary data from a binary data channel in some module serviced by the Data Set. And-or-invert gate D0210 selects either the C7 data mentioned above or the parity eror data from parity data registers C9 and B5. Every ninth count state of counter C14, the parity readout control logic (consisting of gates B1310, inverters C2514 and C2502 and flip-flop A1705) causes and-or-invert gate D0206 to steer the parity data from flip-flop C8 into the output data stream.

Gate B0110 causes the clock inhibit flip-flop D1412 to be set at a count of 24 so that the three data registers (ie. converted analog data, parity error data and external binary data register) see only 24 unload clock pulses which is enough to unload them completely. An additional 16 clock pulses are required to bring these bits to the output register C24. This 24 clock pulse count is chosen to permit command channels to operate in a circular shift mode so that the contents of command channels may be read out non-destructively as binary data. Module L7 uses this feature. Counter D16 is preset to a count of 3 which provides sufficient time for all data to propagate through registers C24 and C26 with an additional 45 usec of shift time after the last data has shifted through C24 and C26.

The DS busy flip-flop A1710 is reset at the completion of the

output data shift operation.

An output of flip-flop C1506 is used to inhibit the ability of the Data Set to "hear" it's own output when used with an Antenna Buffer. This inhibit disables the phase adjust term from exclusive or gate A2403 and clears shift register A18 so that the 200 Khz clocks are not phase perturbed by the Data Set's own output (a positive feedback). In addition it inhibits the detection of the S in it's output message.

Buffers A0411 and A0409 drive the data to the Buffer and the Data Out LED respectively.

3.9 PARITY ERROR DATA READOUT LOGIC

In the event that a distorted command or monitor data message is detected by the Data Set, gate B1606 causes the message multiplex and Data Set address components and the error count to be stored in registers B5 and C9. In addition, if the error occurred in byte 2 of the message, gate B0106 sets flip-flop D2311 which is also stored with the data above. In the event that the parity error rate is high, counter B4 counts the number of errors (up to 16) between the error data readouts on multiplex address 200 (octal). Gate D0610 goes true when multiplex address 200 occurs and enables the parity data in registers C9 and B5 to be routed to the output logic via and-or-invert gate C0210. The data is clocked and sampled in the same manner as A/D or digital data from a device interface.

4.0 ANALOG SUBSYSTEM ALIGNMENT AND TESTS

The analog multiplexer - A/D converter board is removeable from the Data Set for alignment and test in a controllable analog and logic environment. This environment is provided by an A/D-mux test fixture, (dwg D13720L45) a high precision adjustable DC source (Fluke 343A), a digital multimeter and an oscilloscope.

The A/D-mux test fixture has a dual bus switching structure and several analog signal sources. Control and conversion logic sequences the multiplex address, triggers the sample/hold unit and A/D converter and displays the converted digital value and mux channel. The timing of these terms is identical to those in the Data Set. Control switches permit the multiplex address to sequence or be set at any channel. These switches also permit the selection of continuous or manually triggered conversions and the use of the various alignment and perturbation sources.

4.1 ALIGNMENT PROCEDURE FOR A/D BOARD

1. Set the front panel switches of the test fixture as follows:

CMP/LC	- LC
SCAN/SEL	- SEL
MANUAL ON/OFF	- OFF
BUS A 0-J0	- 0
BUS A DIFF/COMM	- DIFF
BUS A +/-	- +
BUS B 0-50	- 0
BUS B DIFF/CM	- DIFF
CHANNEL SELECT	- CH 0
BUS A SOURCE	- GND
BUS B SOURCE	- GND

Set all channel switches to BUS A.
Plug an A/D board (component side up) into the top socket and set the power switch to on.

2. Connect a 4 digit Data Precision DVM between the S/H out and the analog ground test points and adjust the S/H offset pot for a reading of 0.0000 volts.

3. Move the DVM to the analog out test point and adjust the zero adjust pot for 0.000 volts.

4. Remove the DVM and adjust the ADC offset pot for a tester display of 0.000 volts.

4.2 DC Common Mode

1. Set the BUS A DIFF/COM switch to CM. Set the BUS A source to 100 Hz square wave. Switch the desired channel to BUS A and all others to BUS B (GND). With a scope of at least 5 MV/cm sensitivity connected between the analog out and analog gnd terminals, adjust the DC CMR pot for the minimum signal.

4.3 AC Common Mode

1. Using the procedure outlined above, set the BUS A source to a 1 Khz sime wave and adjust the AC CMR pot.

2. Repeat the DC CMR adjustment of 6.2 to insure proper AC and DC CMR alignment.

4.4 A/D Adjustment and Test

1. Set the BUS A DIFF/CM switch to DIFF and the BUS A source to external. Apply a precision DC reference between the BUS A Hi and Low terminals.

2. Set the reference to +10.000 volts and adjust the ADC gain

pot for a panel reading of 10.000 volts.

3. Set the reference to 0.000 volts and adjust the ADC offset pot for a panel reading of 0.000 volts. Return to step 2 and repeat the 2/3 sequence until no further adjustment is necessary.

4. Using the test data sheet, Figure 10, vary the external reference from +10.000 to -10.000 in 1.0 volt increments and record the displayed values.

4.5 CMR Test

1. Install a 1 Kohm resistor between the BUS A Hi and Low terminals. Connect the selected channel to BUS B.

2. Set BUS A source to external. Set RSA and RSB switches to 0 resistance. Set A and B +/- switches to +. Set A and B CM/DIFF switches to CM.

3. Set BUS B source to 1 k, and note the converted value.

4. Set BUS B source to 1 volt and record the value.

5. Set BUS B source to 10 volts and note value.

6. Calculate and record the followint values:

$$\text{CMMR(db)} = 20 \log \frac{|\ (\text{step 3} - \text{step 4})\ |}{1 \text{ volt}}$$

$$\text{CMMR(db)} = 20 \log \frac{|\ (\text{step 3} - \text{step 4})\ |}{10 \text{ volts}}$$

In handling the A/D board, it is very important to avoid touching the PC board contact fingers as human skin oil and salts may contaminate and corrode the edge connector contacts on the board and in the Data Set. Board contact plating often is porous and skin oils and salts can form corrosion products which will cause unreliable electrical contact in a few months. If the contact fingers are touched, the contact area should be thourougly cleaned before installing the A/D-mux board in the Data Set.

DATA SET MUX-A/D BOARD TEST DATA

Board Type _____ Serial # _____
Date _____ Test by _____

A/D Ser # _____ Installed in Data Set Ser # ____ Date _____

Input Volts	Converted Value	Error, MV
+10.000		
+9.000		
+8.000		
+7.000		
+6.000		
+6.000		
+5.000		
+4.000		
+3.000		
+2.000		
+1.000		
0.000		
-1.000		
-2.000		
-3.000		
-4.000		
-5.000		
-6.000		
-7.000		
-8.000		
-9.000		
-10.000		

CMR, db _____

5.0 Major Data Set Drawings

Top Assembly Drawings
D13720P73 Data Set, Model D Top Assembly Drawing
A13720Z99 Data Set, Model D Top BOM

Functional Drawings
D13720L75 Data Set, Model E Logic Diagram
D13720L44 Data Set, Model D Logic Diagram
A13720P57 IC Panel Chip Location Map, Model D & E

Wiring Drawings
A13720W61 Data Set, Model D Master Wire List
A13720W62 Data Set, Model D Hand Wire List
A13720W63 Data Set, Model D Machine Wire List
A13720W64 Data Set, Model D Connector Pin/Signal Wire List
C13720P03 DCS Module Logic Wire-Wrap Field Dim & Notation
D13720M97 Data Set Wiring Jig Configuration
A13720W44 Data Set J1 I/O Signal Wire List
A13720W45 Data Set J3 I/O Signal Wire List
A13720W46 Data Set J4 I/O Signal Wire List

Mechanical Components Drawings
C13720M16 Data Set Front Panel Machining Drawing
C13720M15-1, 2 Modification, Rail
B13720M18-1 Front Panel Filter, Polarizing
B13720M18-2 Front Panel Filter, Clear
C13720M17 Insulated Spacer, Rail
C13720P68 Insulated Side Panel Ass'y
B13720M49 Side Panel Insulation
C13720M50 Side Panel, Modified
C13720M07 Perf Cover Ass'y
B13050M17 Perf Cover Fastener
B13050M32 1-Wide 42/34 Rear Panel
B13720M46 A/D PCB Connector Support
C13720AA51 Data Set Front Panel Silk Screen Artwork

Front Panel LED Display Drawings
C13720P38 Front Panel LED Display Ass'y
A13720Z23 Front Panel LED Display Ass'y BOM
D13720M33 Front Panel LED Display Detail
B13720AB06 Front Panel LED Display PCB Artwork

Burr-Brown Type Mux-A/D Converter Drawings, (Model D DS only)
(uses Burr-Brown SDM 853 and Intel 1702 EPROM)
D13720P92 A/D Converter Ass'y Drawing
A13721Z19 A/D Converter Ass'y, BOM
D13720AD20 PCB Artwork
D13720AD22 PCB Silkscreen Artwork
D13720M55 PCB Drill Drawing
D13720AD23 PCB Solder Mask Artwork
C13720P93 Prom Carrier PC Board Ass'y

B13720M57 Prom Socket Protector

Analog Devices Type Mux-A/D Converter Drawings, (Model D DS only)
(uses Analog Devices AD 363 Analog Input System & Intel 1702 EPROM)
C13721P41 A/D Converter Ass'y
A13720Z61 A/D Converter Ass'y BOM
D13720M91 PCB Drill Drawing
C13720AB35 PCB Solder Mask Artwork
C13720AB36 PCB Silkscreen Artwork
A13720P93 Prom Carrier PC Board Ass'y
B13720M57 Prom Socket Protector

(note, the PCB artwork for this board was modified to the Model E Data Set version)

Analog Devices Type Mux-A/D Converter Drawings, (Model E DS only)
(uses Analog Devices AD 363 Analog Input System & Intel 2716 EPROM)
D13720S23 Logic Schematic
C13720AB48 PCB Artwork
D13721M13 PCB Drill Drawing
C13720AB49 PCB Silk Screen Artwork
A13720P93 Prom Carrier PC Board Ass'y
B13720M67 Prom Socket Protector

6.0 Input/Output Signal Pin Assignments

J1 - 37 pin Front Panel test D connector
J2 - 86 pin Mux - A/D board internal connector
J3 - 34 pin Amp Rear Panel connector
J4 - 42 pin Amp Rear Panel connector

Power Inputs:

+ 5 Volt logic power	-	J4 - 10
Logic Common	-	J4 - 34
+ 15 Volt power	-	J4 - 16
- 15 Volt power	-	J4 - 17
Analog Gnd	-	J4 - 42

Address Inputs:

Anta-4 ("16")	-	J4 - 18
Anta-3 ("8")	-	J4 - 24
Anta-2 ("4")	-	J4 - 20
Anta-1 ("2")	-	J4 - 13
Anta-0 ("1")	-	J4 - 2
DSA-2 ("4")	-	J4 - 29
DSA-1 ("2")	-	J4 - 28
DSA-0 ("1")	-	J4 - 11

Command Message/Q Inputs:

Cmd/Q Hi	-	J4 - 25
Cmd/Q Lo	-	J4 - 26

Monitor Data Message Outputs:

Data to Buffer Hi	-	J4 - 15
Data to Buffer Lo	-	J4 - 27

Data Tap Output:

Cmd/Data Messages Hi	-	J4 - 8
Cmd/Data Messages Lo	-	J4 - 9

Submultiplexer Address Outputs:

Signal	Pin
SMA-0 ("1")	J3 - EE
SMA-0 Ret	J3 - CC
SMA-1 ("2")	J3 - KK
SMA-1 Ret	J3 - HH
SMA-2 ("4")	J3 - DD
SMA-2 Ret	J3 - FF
SMA-3 ("8")	J3 - JJ
SMA-3 Ret	J3 - LL

Command/Data Channel I/O Pin Assignments

Digital Command Outputs

DIGI/O	#0	#1	#2	#3
Addr *	200 - 217	220 -237	240 - 257	260 - 277
Signal				
DIGI-X	J3 - B	J3 - R	J4 - 1	J4 - 19
DIGI-X Ret	J3 - D	J3 - T	J4 - 4	J4 - 22
CLKI-X	J3 - F	J3 - V	J4 - 3	J4 - 21
CLKI-X Ret	J3 - J	J3 - X	---	---
STRI-X	J3 - L	J3 - Z	J4 - 12	J4 - 23
STRI-X Ret	J3 - N	J3 - BB	---	---

* Address in octal notation

Digital Monitor Data Inputs

Addr *	320 - 337	340 -357	360 - 377
Signal			
DIGO-X	J3 - C	J3 - S	J4 - 35
DIGO-X Ret	J3 - A	J3 - P	J4 - 36
CLKO-X	J3 - H	J3 - W	J4 - 37
CLKO-X Ret	J3 - E	J3 - U	---
STRO-X	J3 - M	J3 - AA	J4 - 30
STRO-X Ret	J3 - K	J3 - Y	---

Analog Monitor Data Inputs:

Signal			Address *
ALGI-0+	J4	- 14	00
ALGI-0-	J4	- 32	
ALGI-1+	J4	- 33	20
ALGI-1-	J4	- 41	
ALGI-2	J4	- 7	40
ALGI-3	J4	- 40	60
ALGI-4	J4	- 6	100
ALGI-5	J4	- 39	120
ALGI-6	J4	- 5	140
ALGI-7	J4	- 38	160

* address is in octal notation

7.0 SPECIAL MODULE DATA SHEETS

Three different versions of analog multiplexer - A/D Converter PC board sub-assemblies are used:

1) Burr-Brown - SDM853, used in Model D Data Sets only
2) Analog Devices - AD363KD AIS, with Intel 1702A EPROM; used in Model D Data Sets only.
2) Analog Devices - AD363KD AIS with Intel 2716 EPROM; used in Model E Data Sets only.

Two EPROMs are used for MW1 address programs: the Intel 1702 and 2716 (data acces speed is not a problem, just about any 1702 or 2716 will work). The EPROMs are located on the A/D board because of the chip 24 pin package. When Model D Data Sets are installed in a rack, be sure that the EPROM program is appropriate for the rack location. This consideration does not apply to the Model E Data Sets because the 2716 EPROM contains programs for all racks.

Data Sheets for these devices follow.

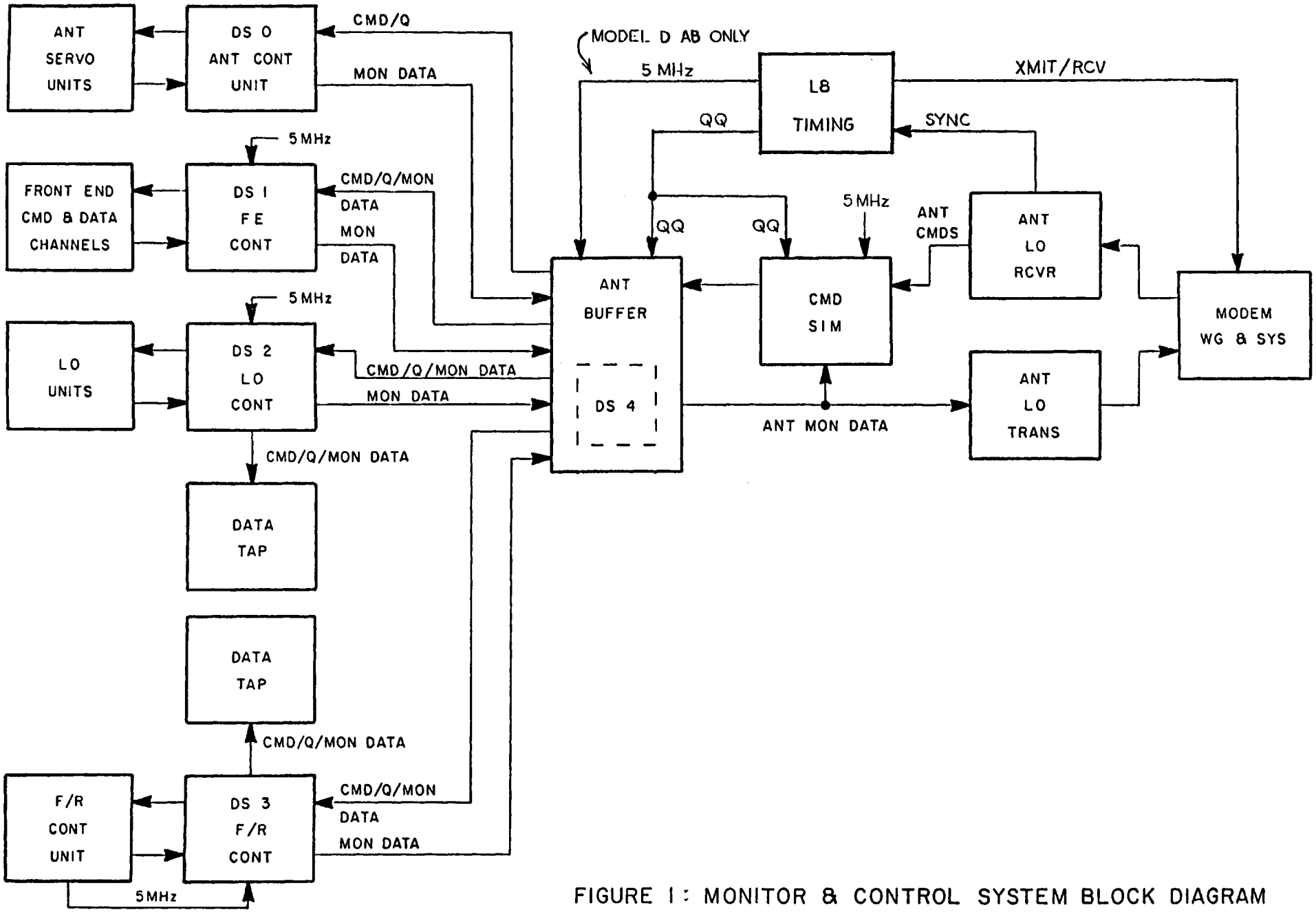


FIGURE 1 : MONITOR & CONTROL SYSTEM BLOCK DIAGRAM

REV. 7-86

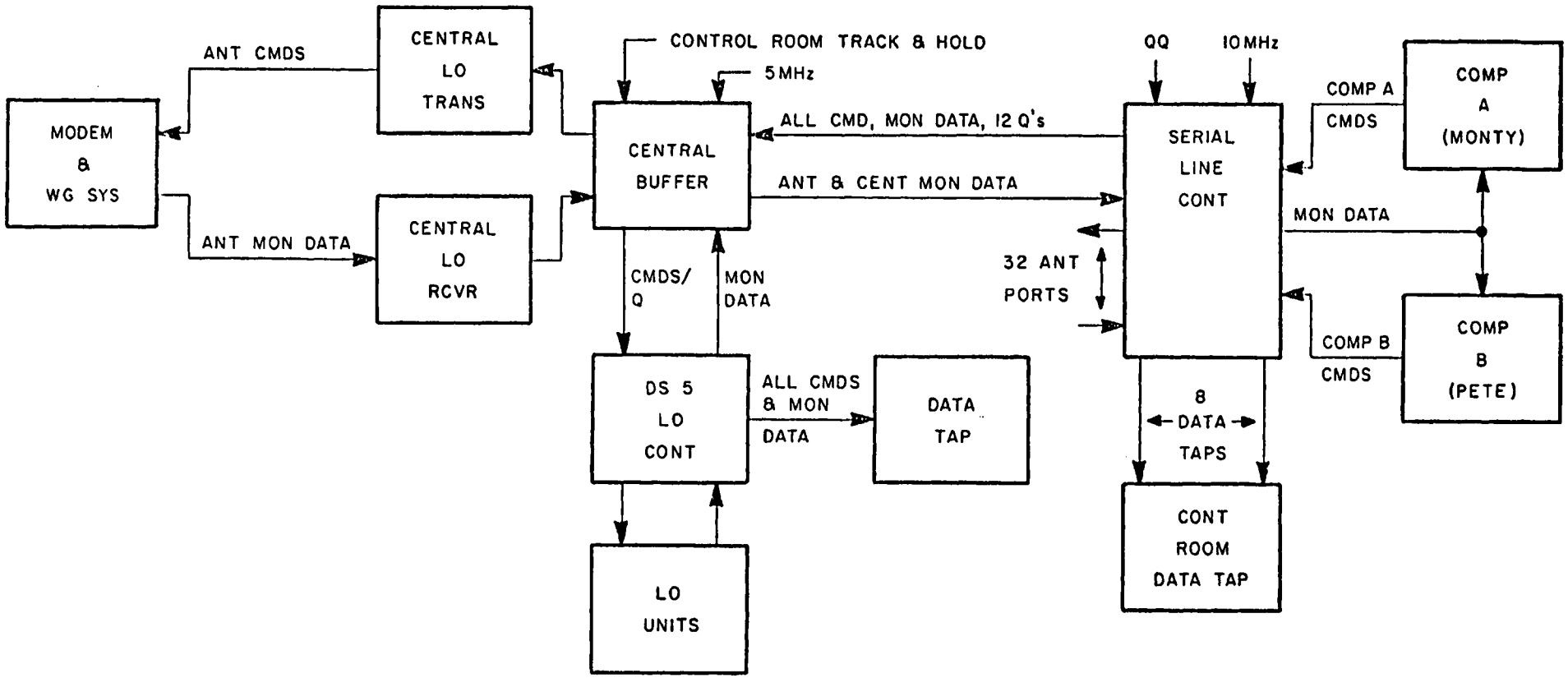


FIGURE 1: CONTINUED

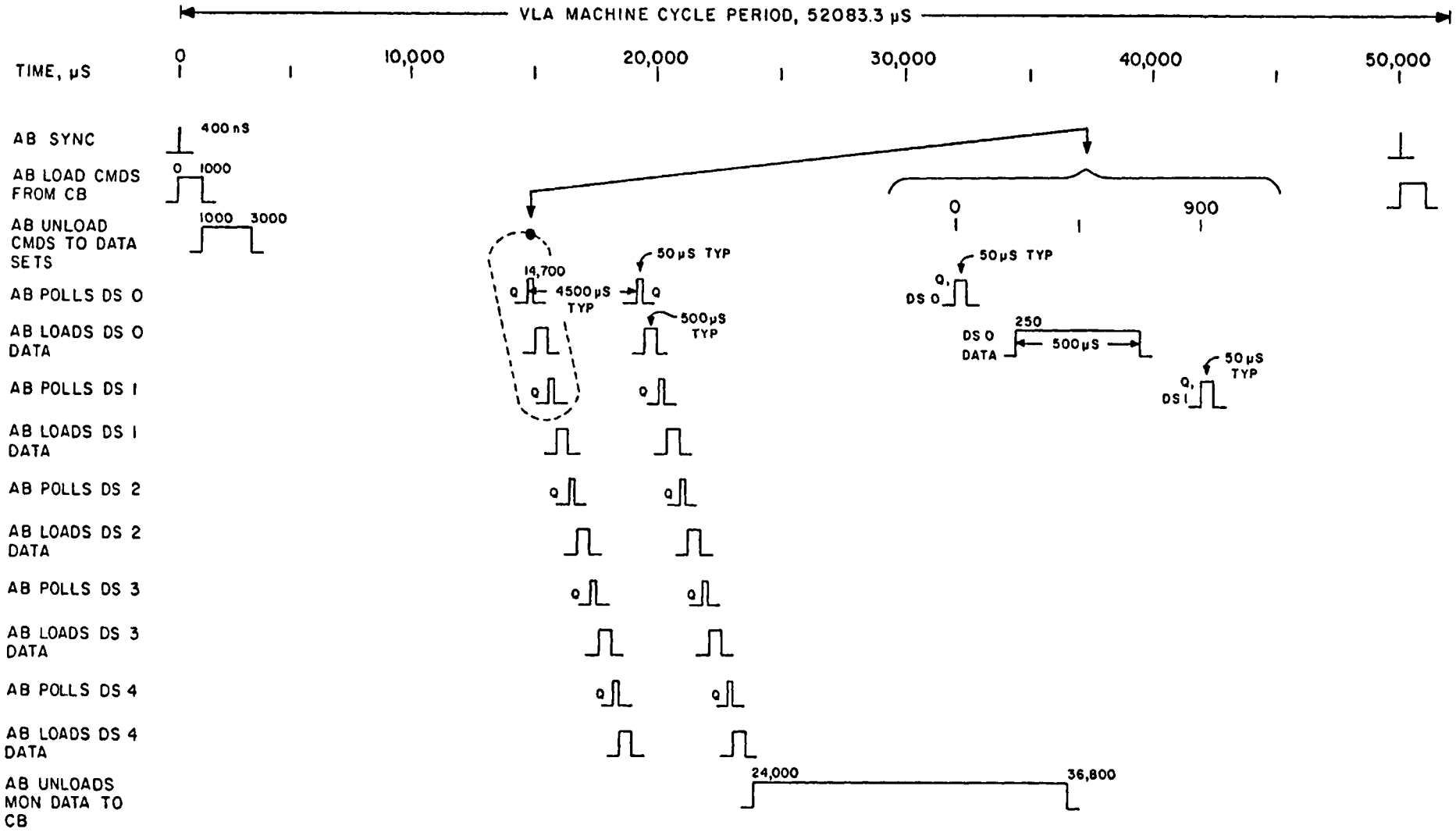


FIG. 2
ANTENNA TIMING OPERATIONS

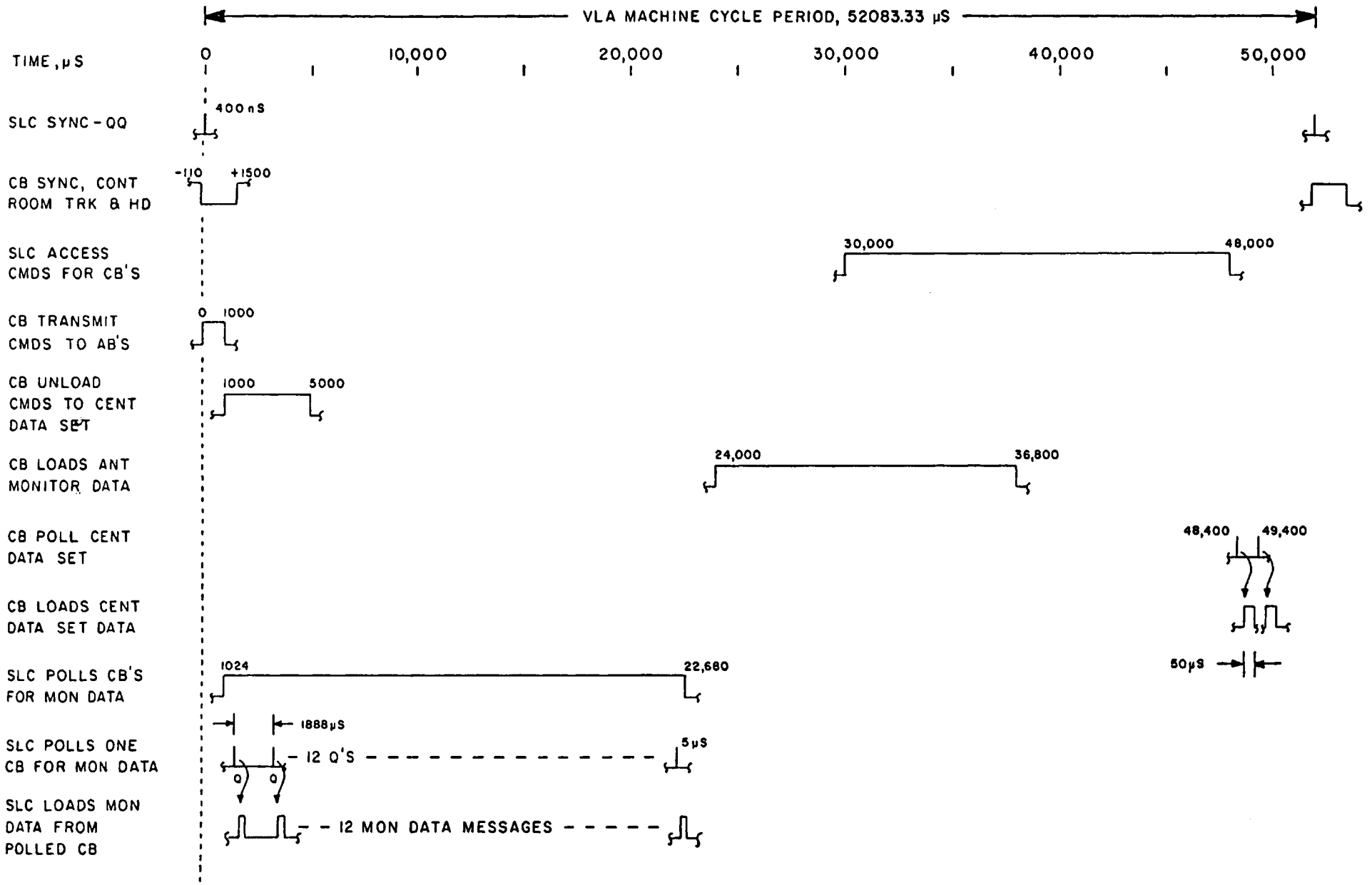


FIG. 3
CENTRAL TIMING OPERATIONS

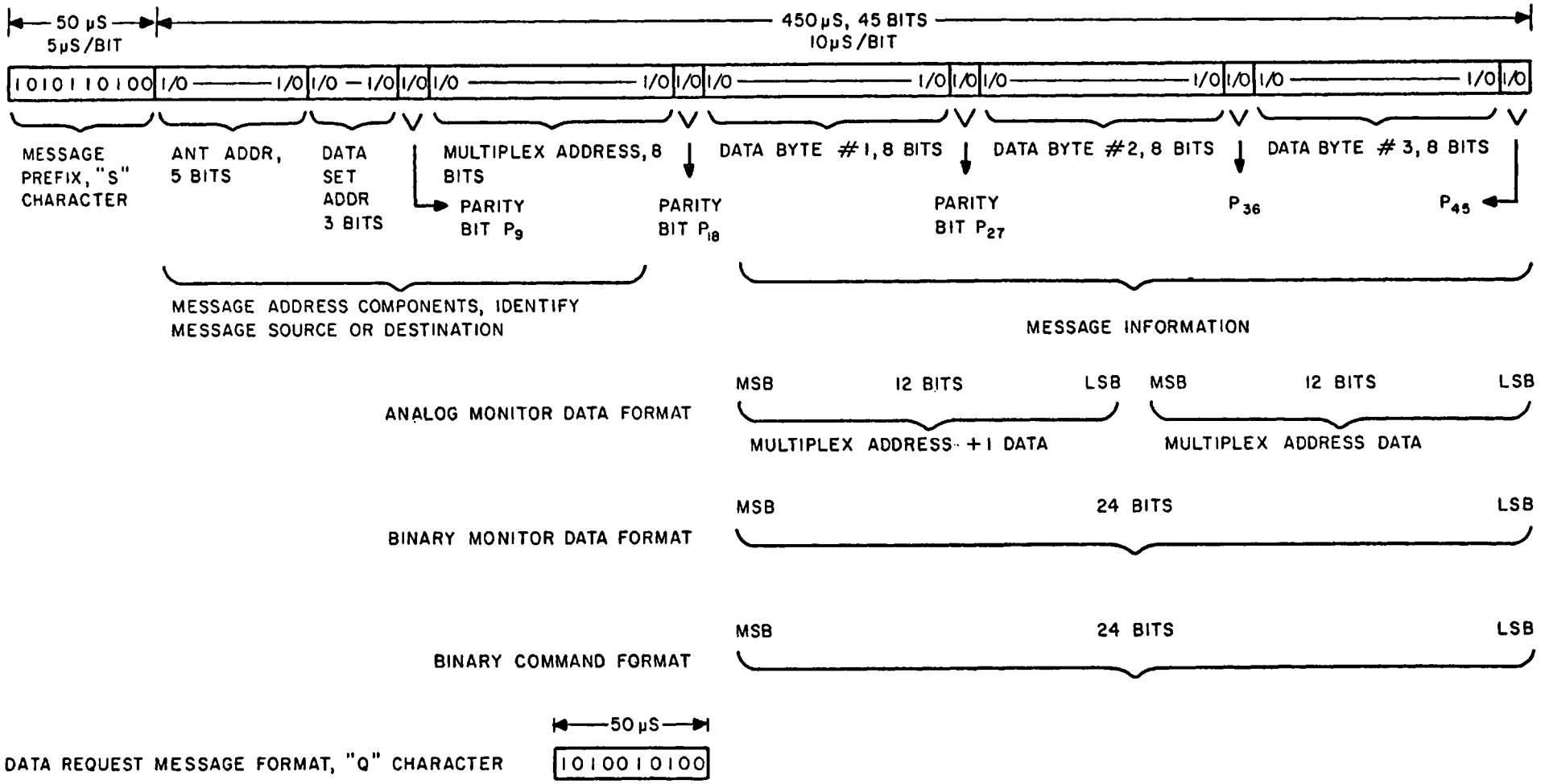


FIGURE 4: DATA SET COMMAND AND MONITOR DATA AND DATA REQUEST MESSAGE FORMATS

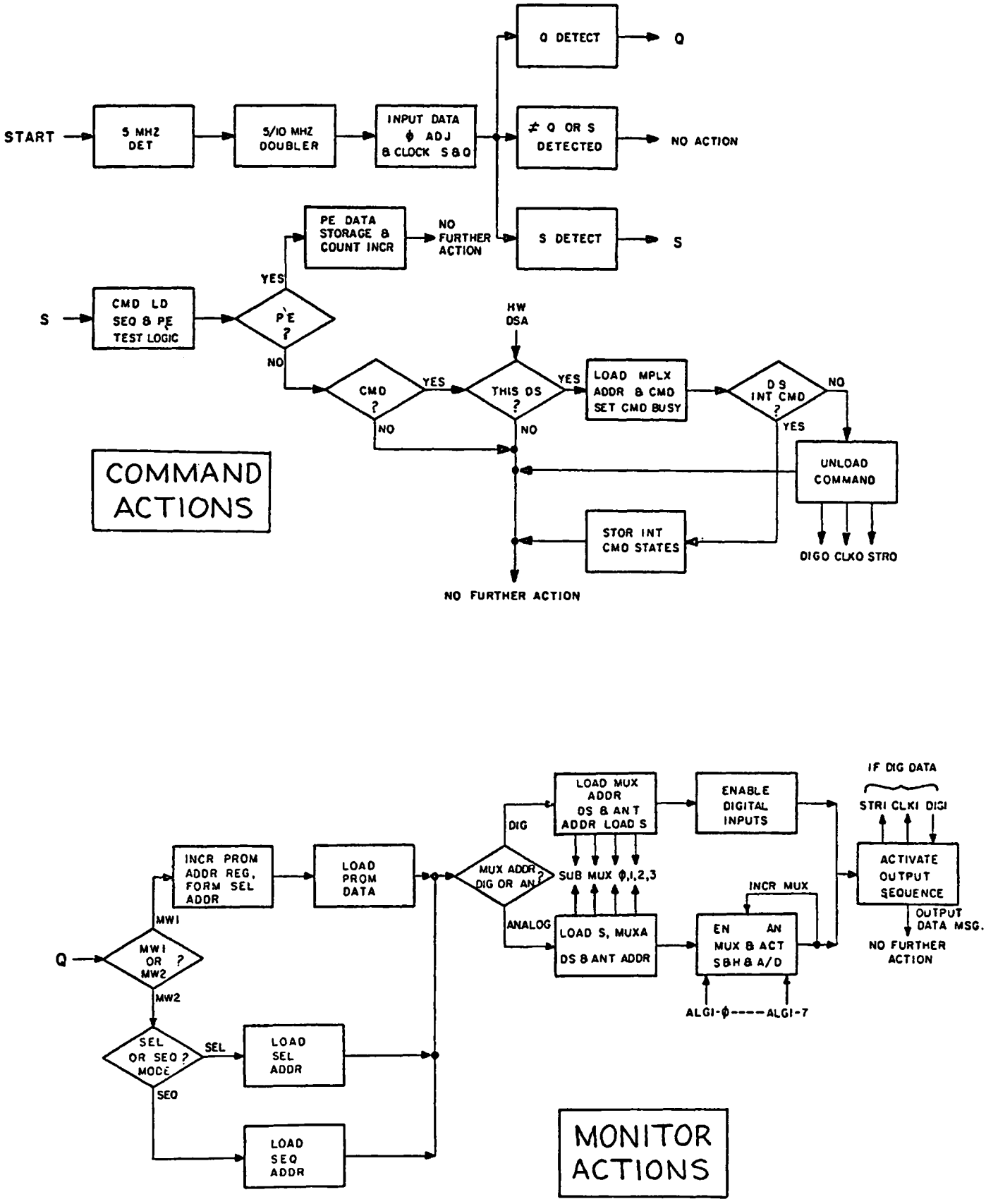


FIG. 5 DATA SET LOGIC FLOW DIAGRAM

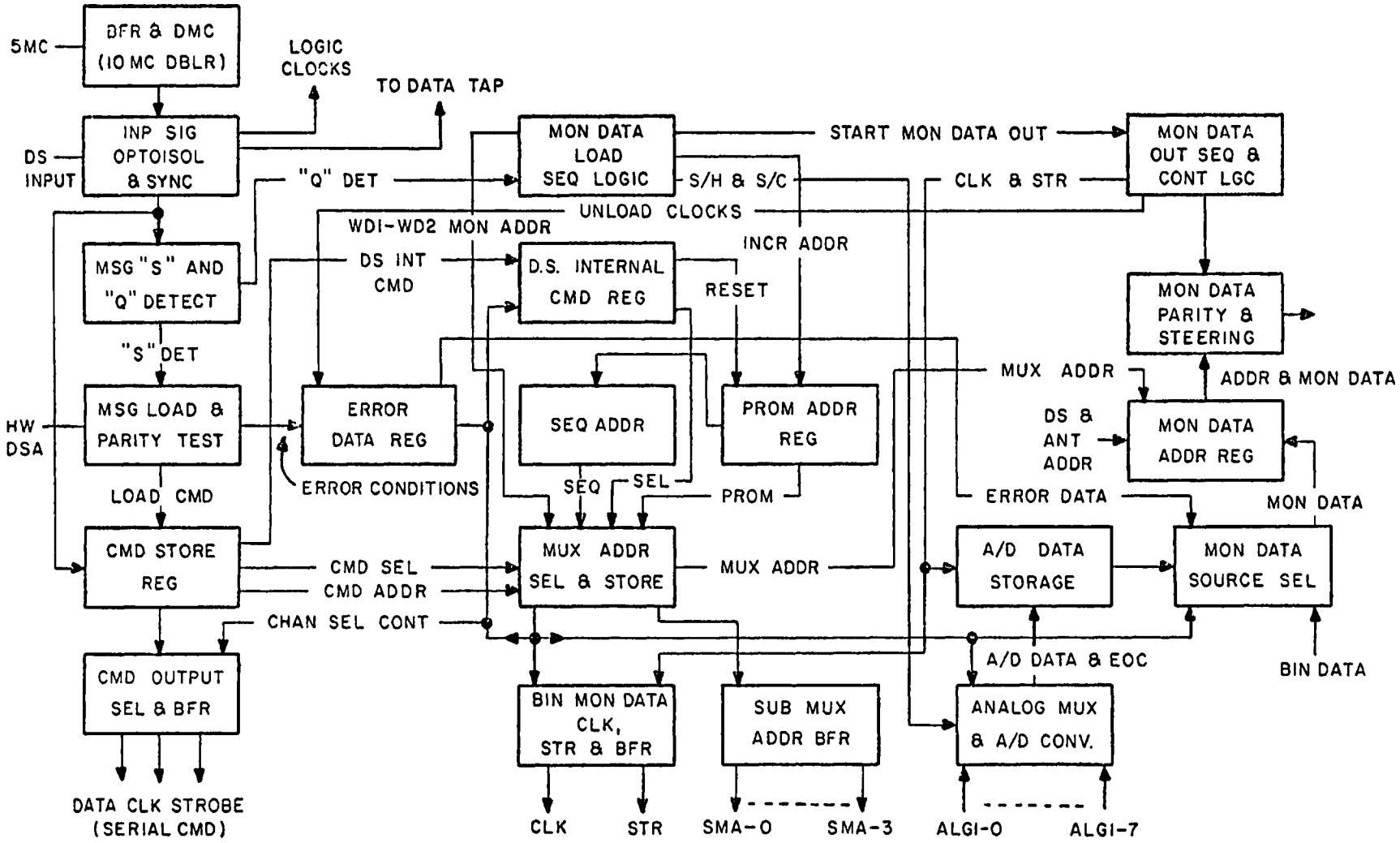


FIGURE 6: DETAILED FUNCTIONAL BLOCK DIAGRAM

MONITOR WORD 1 DCS=12 DS=5

(A000)	0.890	1.095	0.000	3.485			-0.985	-0.895
(A010)			0.005	0.000	3.505	-7.520	0.005	7.465
(A020)								
(A030)								
(A040)	0.000	-0.455			0.000	0.990	4.640	1.065
(A050)	-0.885	4.490	1.545	0.000	0.040	0.095	0.100	4.130
(A060)								
(A070)								
(A100)	-4.630	-4.275			5.975	6.295	5.815	6.150
(A110)	5.145	0.000	7.470	-7.510			0.005	0.000
(A120)	3.615	3.450	3.535	4.240				
(A130)								
(A140)								
(A150)								
(A160)								
(A170)								
(D200)	FFFFFF							
(D210)								
(D220)	2EA000	FFF000						
(D230)								
(D240)	000000	0F0000						
(D250)								
(D260)								
(D270)								

MW-1

MONITOR WORD 2 DCS=12 DS=5

(A000)	
(A010)	
(A020)	0.105 0.140
(A030)	
(A040)	
(A050)	
(A060)	
(A070)	
(A100)	
(A110)	
(A120)	
(A130)	
(A140)	
(A150)	
(A160)	
(A170)	
(D200)	
(D210)	
(D220)	
(D230)	
(D240)	
(D250)	
(D260)	
(D270)	

MW-2

SELECT MODE

(MUX 022/023 SHOWN SELECTED)

MONITOR WORD 2 DCS=12 DS=5

(A000)	0.890	1.095	0.060	3.460	0.045	0.920	-0.990	-0.895
(A010)	0.510	0.460	0.000	0.000	3.505	-7.520	0.000	7.465
(A020)	0.300	0.295	0.070	0.105	0.170	0.190	0.015	-0.010
(A030)	1.045	1.075	1.355	1.335	1.145	1.020	0.500	0.600
(A040)	0.000	-0.455	-0.275	-0.015	0.000	0.990		
(A050)	-0.885	4.490	1.545	0.005	0.040	0.095	0.100	4.135
(A060)	0.005	0.005	0.005	0.000	0.000	0.000	0.005	0.000
(A070)	0.000	0.000	0.000	0.000	0.000	0.000	0.005	0.000
(A100)	-4.625	-4.275	-4.650	-4.710	5.975	6.275	5.820	6.150
(A110)	5.145	0.000	7.475	7.505	6.965	-6.950	0.000	0.000
(A120)	3.615	3.495	3.595	4.320	0.005	0.000	0.000	0.000
(A130)	3.260	3.200	4.470	4.255	1.670	1.485	0.355	0.370
(A140)	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000
(A150)	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000
(A160)	0.005	0.000	0.000	0.000	0.005	0.000	0.000	0.000
(A170)	0.005	0.000	0.000	0.000	0.000	0.000	0.000	0.000

(D200)	FFFFFF	000000		000000	000000	000000	000000	
(D210)		000000	000000	000000	000000	000000		000000
(D220)	2EB000	7FE000	000000	000000	000000	000000		000000
(D230)		000000	000000	000000	000000	000000	000000	000000
(D240)	000000	0F0000	000000	000000	000000	000000	000000	000000
(D250)	000000	000000	000000	000000	000000	000000	000000	000000
(D260)	000000	000000	000000	000000	000000	000000	000000	000000
(D270)	000000	000000	000000	000000	000000	000000	000000	000000

MW-2

SEQUENCE MODE

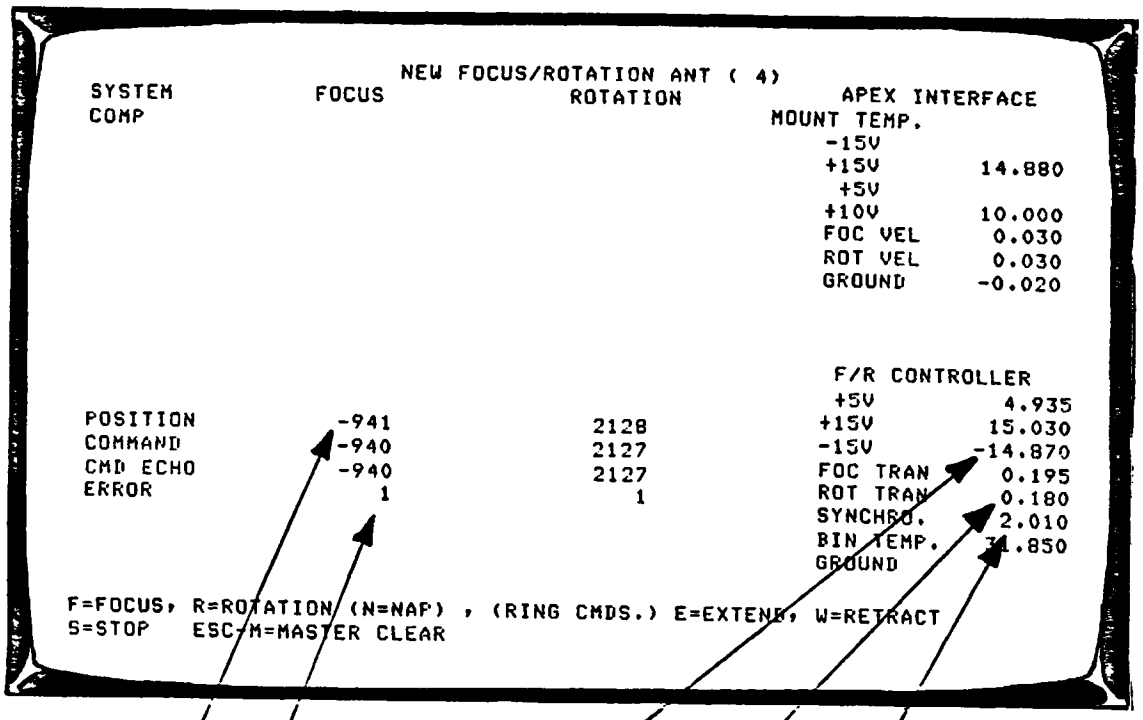
DMP TERMINAL CMD's:

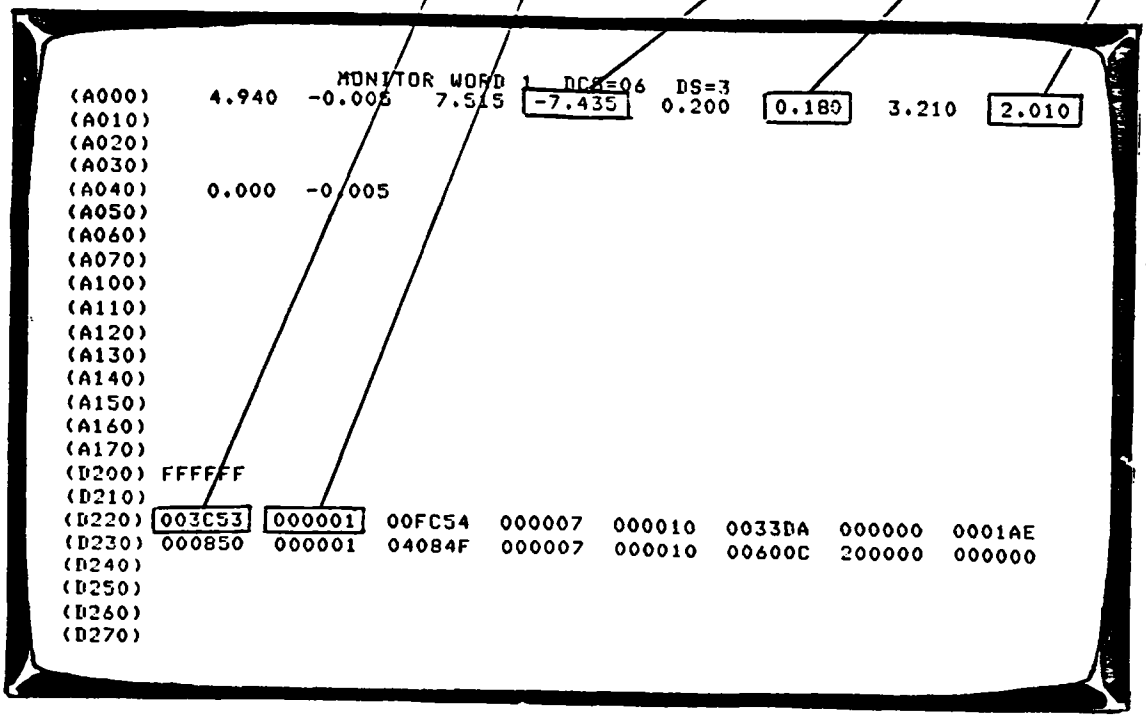
Select MW1 Overlay:
MW 1 'DCS DS
Select MW2 Overlay:
MW 2 'DCS DS
FREE(Seq. Mode) DS:
F DS DCS
Select Mode Address:
S 'MUX DS 'DCS

Figure 7 (a)
TYPICAL MONITOR WORD OVERLAYS

TYPICAL FR OVERLAY

NOTE: ALL SYSTEM OVERLAYS ARE BASED ON MONITOR WORD-1 DATA ONLY.





TYPICAL MW-1 OVERLAY (DS-3)

EXAMPLE SHOWING HOW "RAW" DATA SET MONITOR WORD DATA IS EXTRACTED INTO "FORMATTED" OVERLAY DATA.

FIG. 7b
TYPICAL MONITOR WORD OVERLAYS

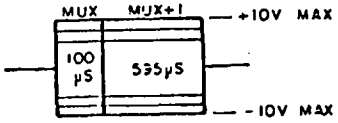
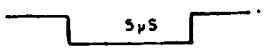
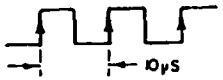
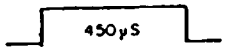
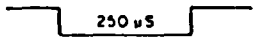
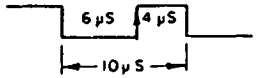
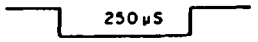
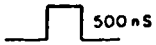
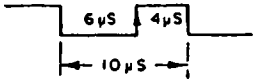
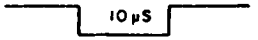
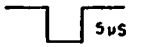
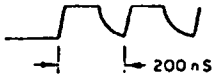
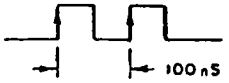
J1 Pin	Signal	Comment	Waveform (+3.5 = HI, Gnd = LO)
1	+5SYNC	+5 VDC	DC, +5
2	GNDSYNC	Logic Conn	DC, Gnd
3	ANMON	Multiplexed Analog Data	
4	PARERR	Parity Error Detected	
5	DTAOUT	Monitor Data to Buffer	Monitor Data Message, Hi-True
6	DSINP	Data Set	Cmd/Monitor Messages, Lo-True
7	CLKDIN	Clocked Input Message	Cmd/Monitor Messages, Hi-True
8	SHFTCLK	Input Message Load Clock	
9	SHFTEN	Input Message Shift Enable	
10	SDET	Cmd/Mon Message Detected	
11	QDET	Data Request Message Detected	
12	SERCMD	Output Cmd Information	10 µs/Bit, Lo-True
13	ADEOC	A/D Conv End of Conversion	
14	192EN	DS Int Cmd En	
15	DSSEL	Message Directed to Data Set	
16	SER/SEL	Sequential/Select Mode Control	Hi = Sequential Mode Control
17	CMDCLK	Command Output Shift Clock, 24 Pulses	
18	RSPPOM	Reset Prom Address Register	
19	A/DSC	A/D Converted Start Conversion	
20	DSCLK	Binary Monitor Data Shift Clock	
21	BINSTR	Binary Monitor Data Load Store	
22	DINDTA	Binary Monitor Data Input to Data Set	Low True Serial Waveform
23	CMDSTR	Cmd Chan Load Strobe	
24	5MHZ	5 MHz detector Output	
25	10MHZ	Doubled 5 MHz	
26	SMA-4	Mux Address - 4, "16", Hi True	 250µS CMDS 700µS MON DATA

FIG. 8 DATA SET TESTPOINTS (J1) WAVEFORMS

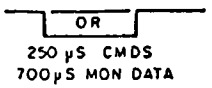
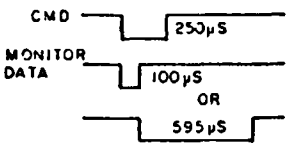
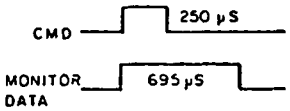
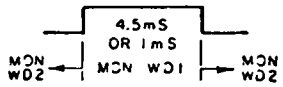
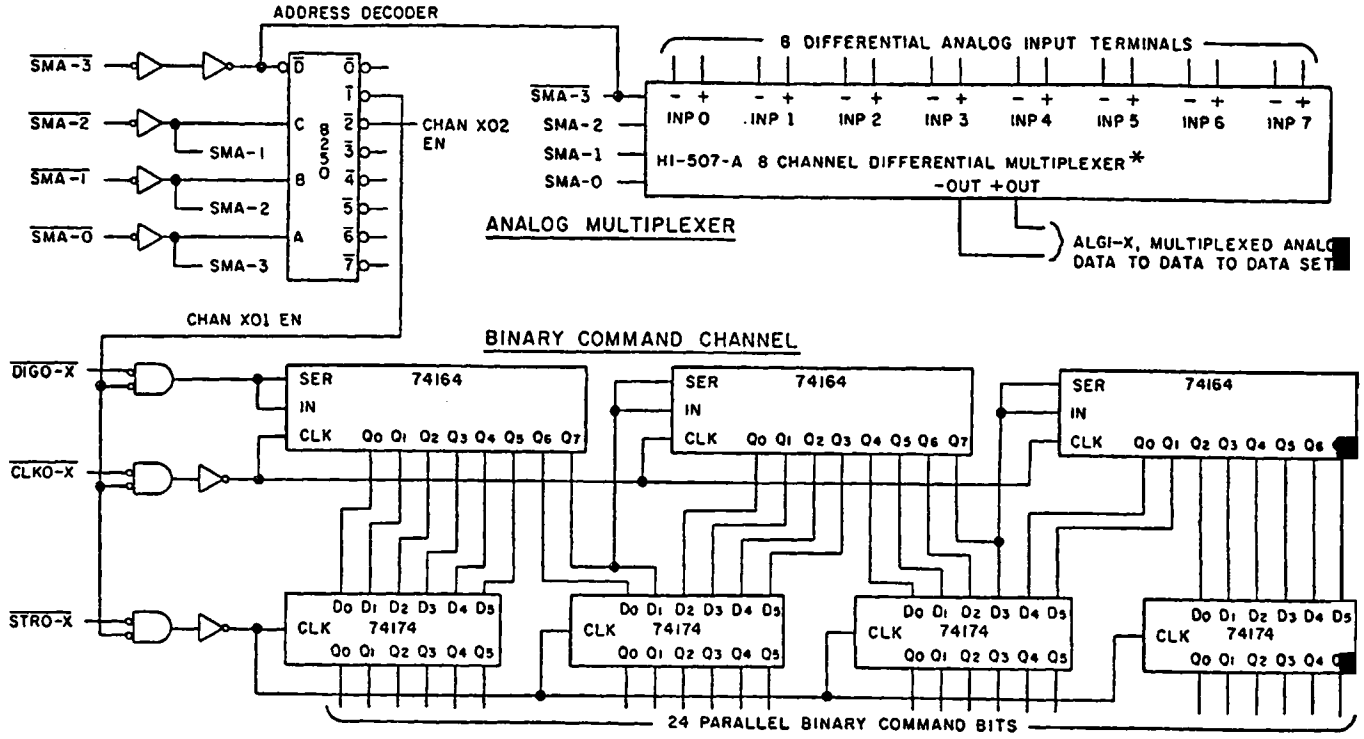
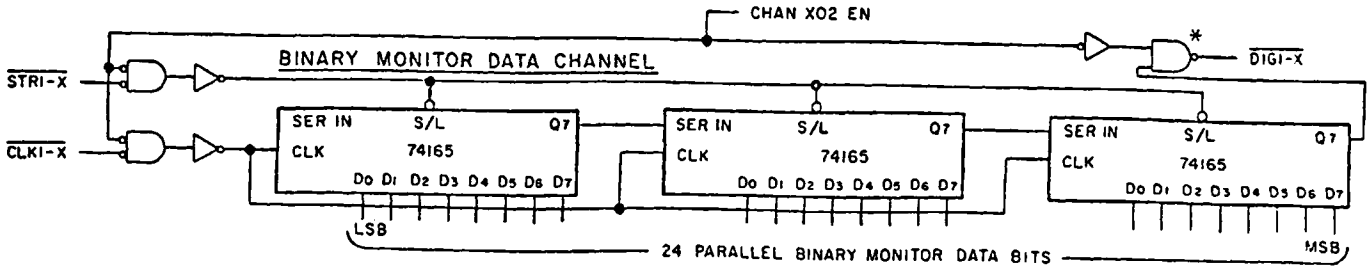
27	SMA-5	Mux Address - 5 "32", Hi True	
28	SMA-6	Mux Address - 6 "64", Hi True	SAME AS ABOVE
29	SMA-7	Mux Address - 7 "128", Hi True	SAME AS ABOVE
30	SMA-0	Sub-Mux Address - 0 "1", Low-True	
31	SMA-1	Sub-Mux Address - 1 "2", Low-True	SAME AS ABOVE
32	SMA-2	Sub-Mux Address - 2 "4", Low-True	SAME AS ABOVE
33	SMA-3	Sub-Mux Address - 3 "8", Low-True	SAME AS ABOVE
34	A/DDATA	Converter Analog Data Storage Reg	24 Bits, Low True
35	DSBUSY	Data Set Busy, Executing CMD or Gathering New Data	
36	WD1/WD2	Monitor Word 1/2 Control Flip-Flop	
37	PEDATA	Parity Error Data Storage Reg Output	PE Message Data, Hi-True

FIG. 8 - Continued



* ANOTHER 8 CHANNEL DIFFERENTIAL MULTIPLEXER MAY BE ADDED OR 16 CHANNEL SINGLED MULTIPLEXERS SUBSTITUTED IF COMMON MODE VOLTAGES ARE LOW.



* - THIS GATE MUST HAVE AN OPEN COLLECTOR AS THE DIGI-X LINE IS A PARTY LINE WITH THE PULL-UP RESISTOR IN THE DATA SET.

FIG. 9 - TYPICAL CONTROL / DATA INTERFACE LOGIC

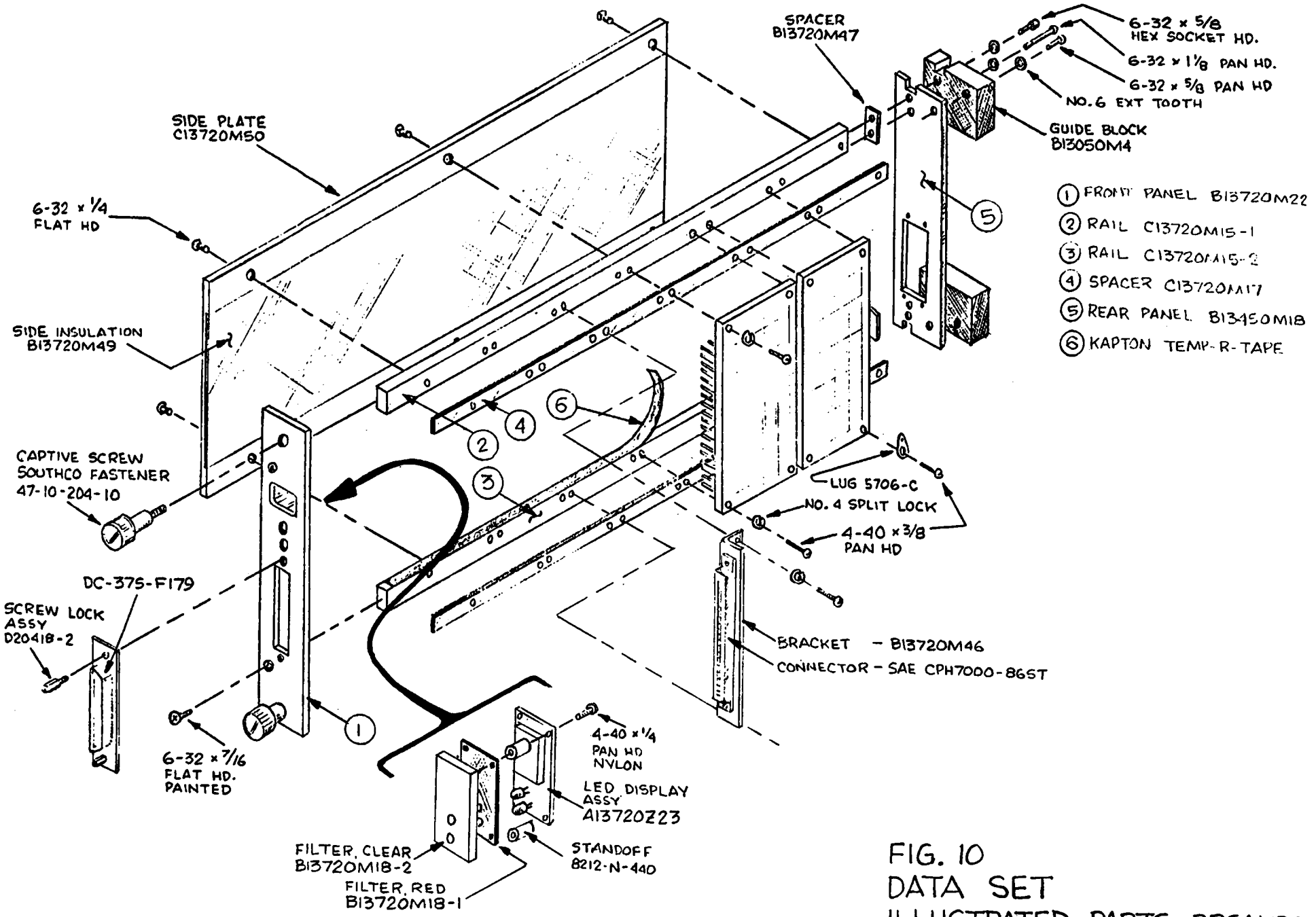
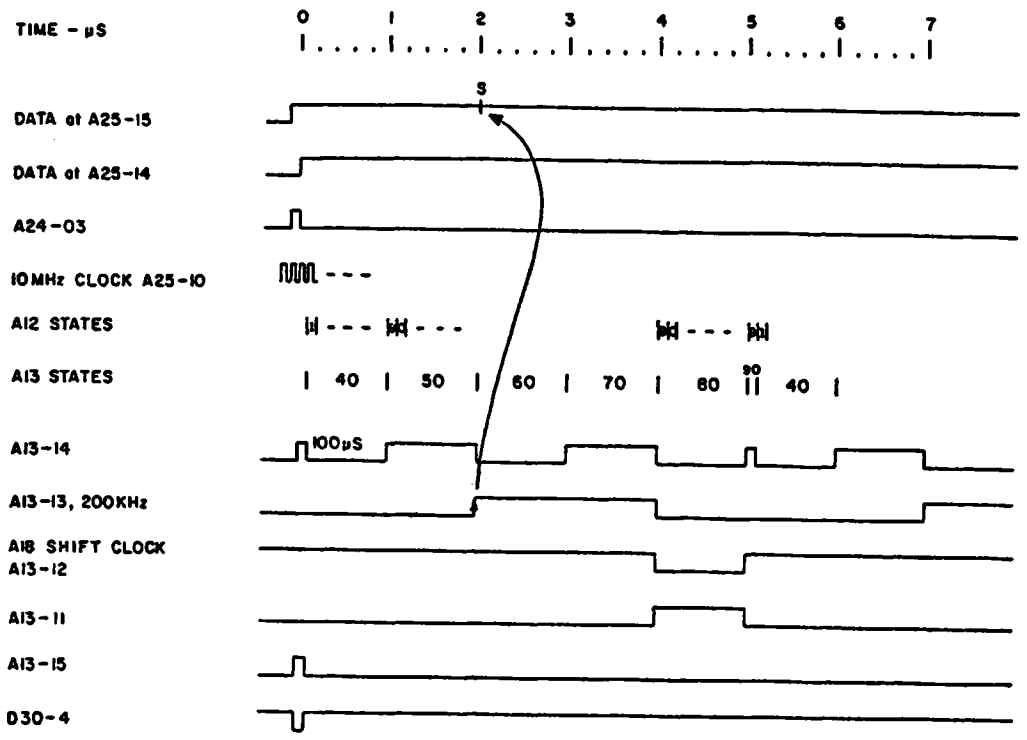
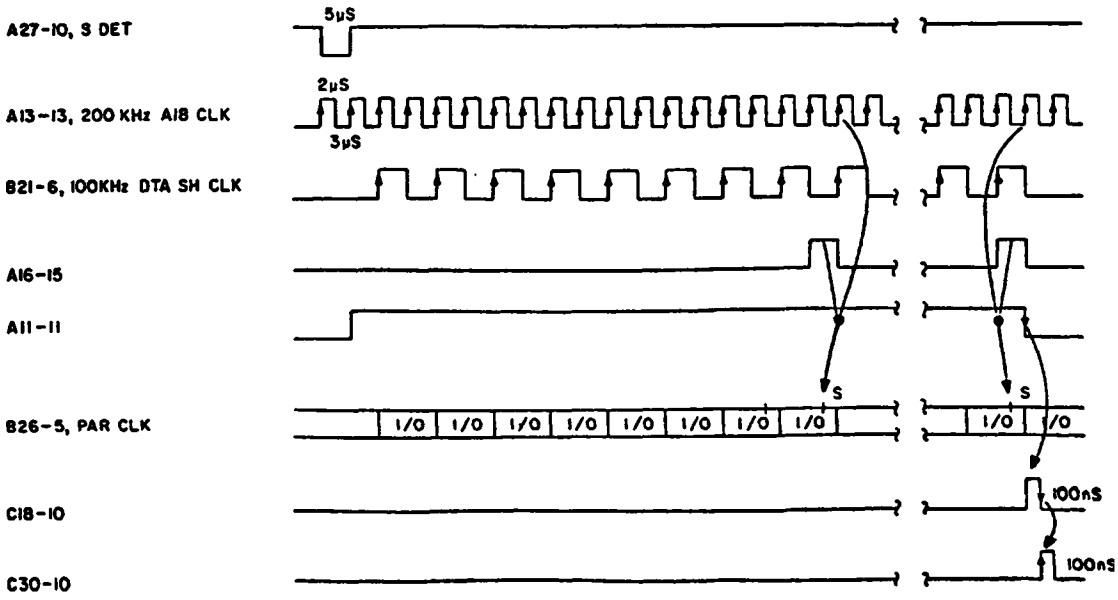


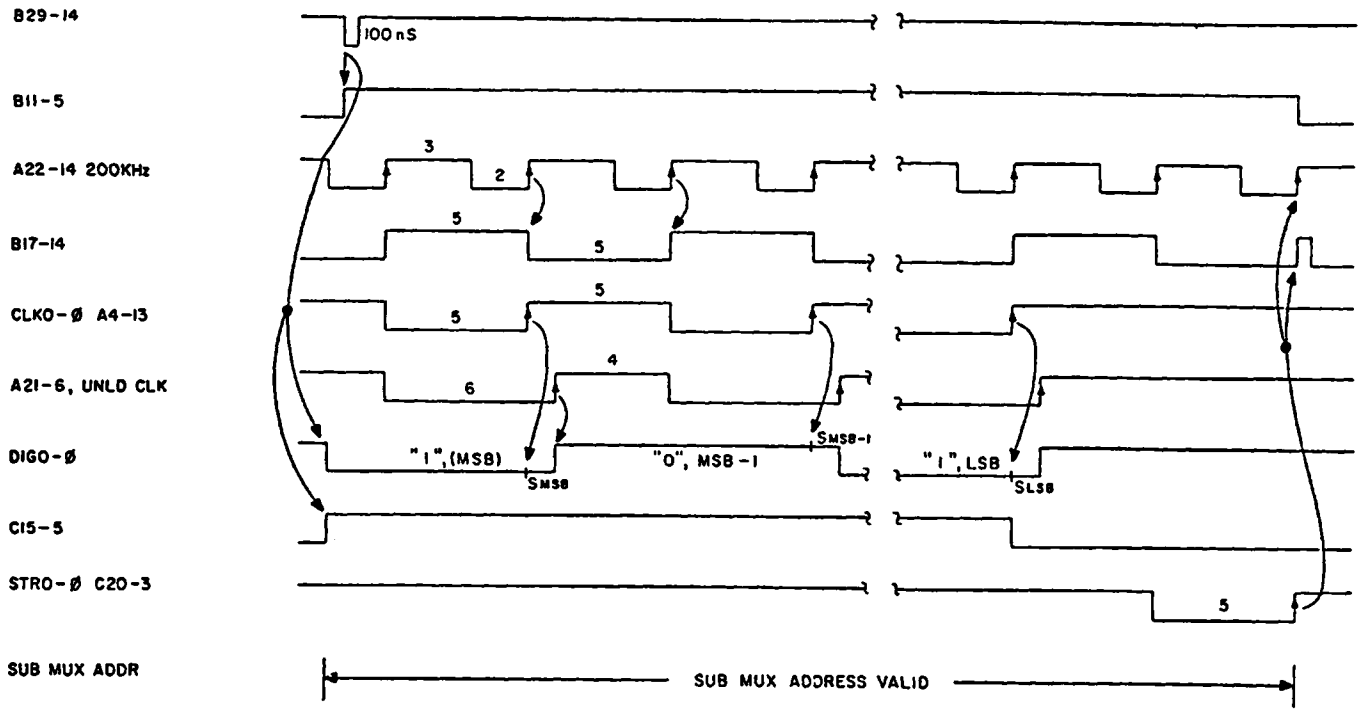
FIG. 10
DATA SET
ILLUSTRATED PARTS BREAKDOWN



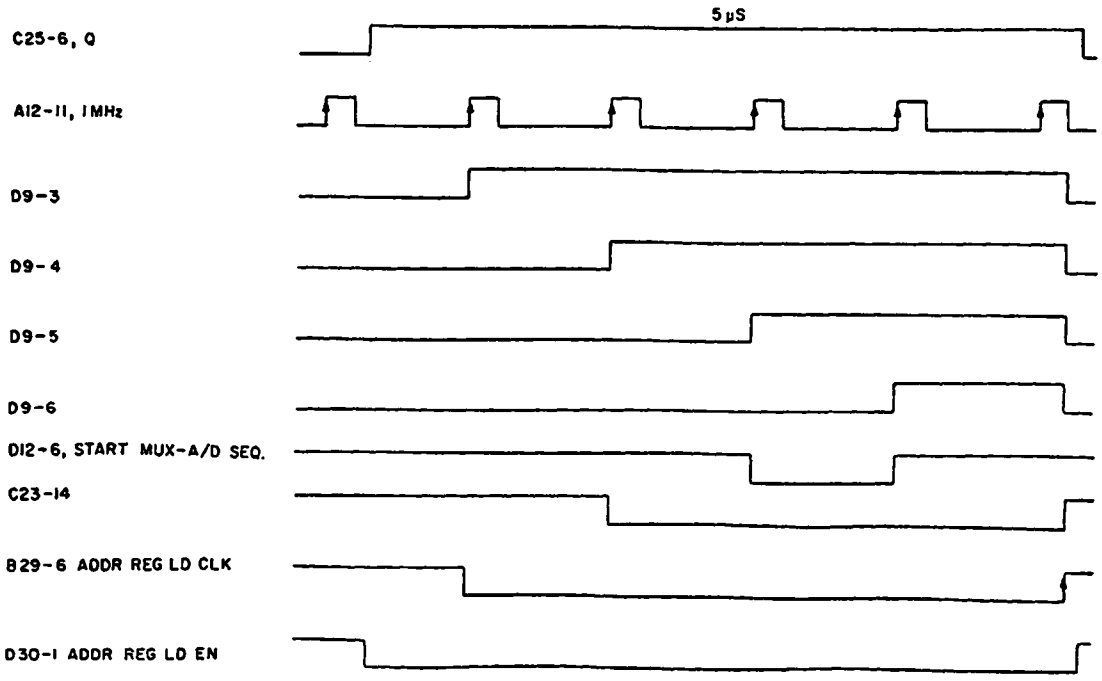
TIMING DIAGRAM 1: INPUT SIGNAL SYNCHRONIZATION TIMING



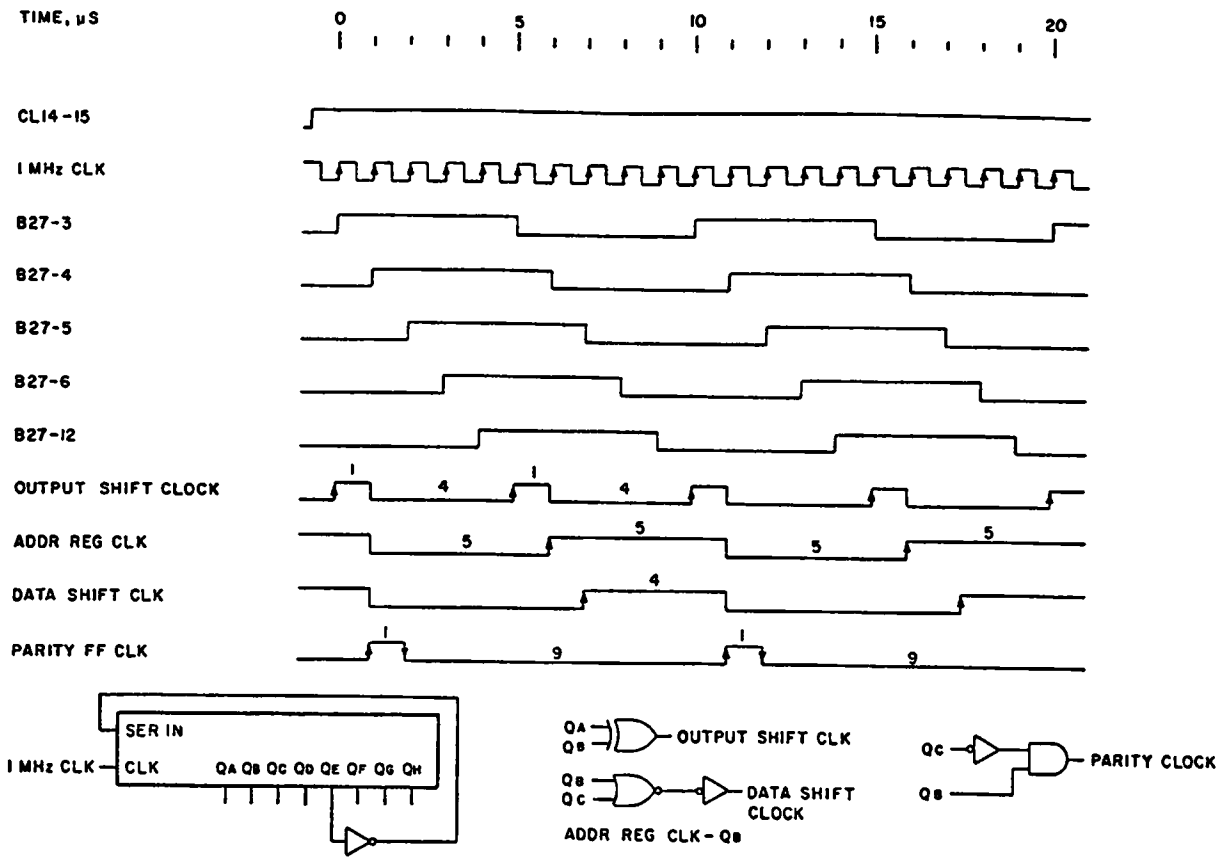
TIMING DIAGRAM 2: MESSAGE DETECTION - LOADING TIMING



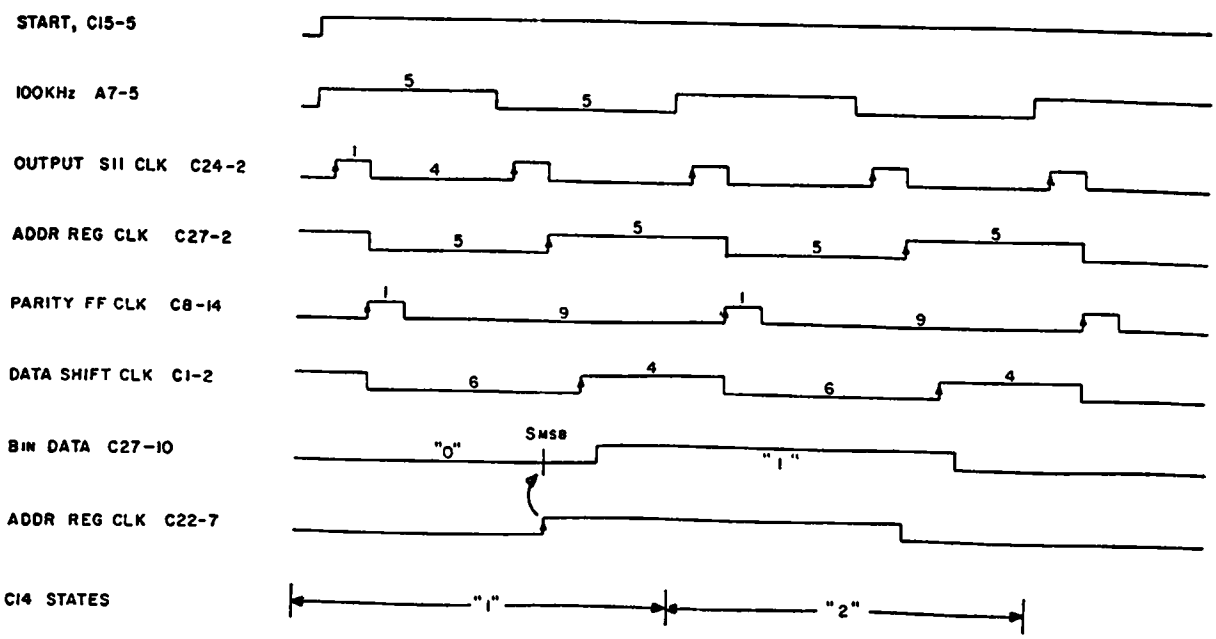
TIMING DIAGRAM 3: COMMAND OUTPUT TIMING



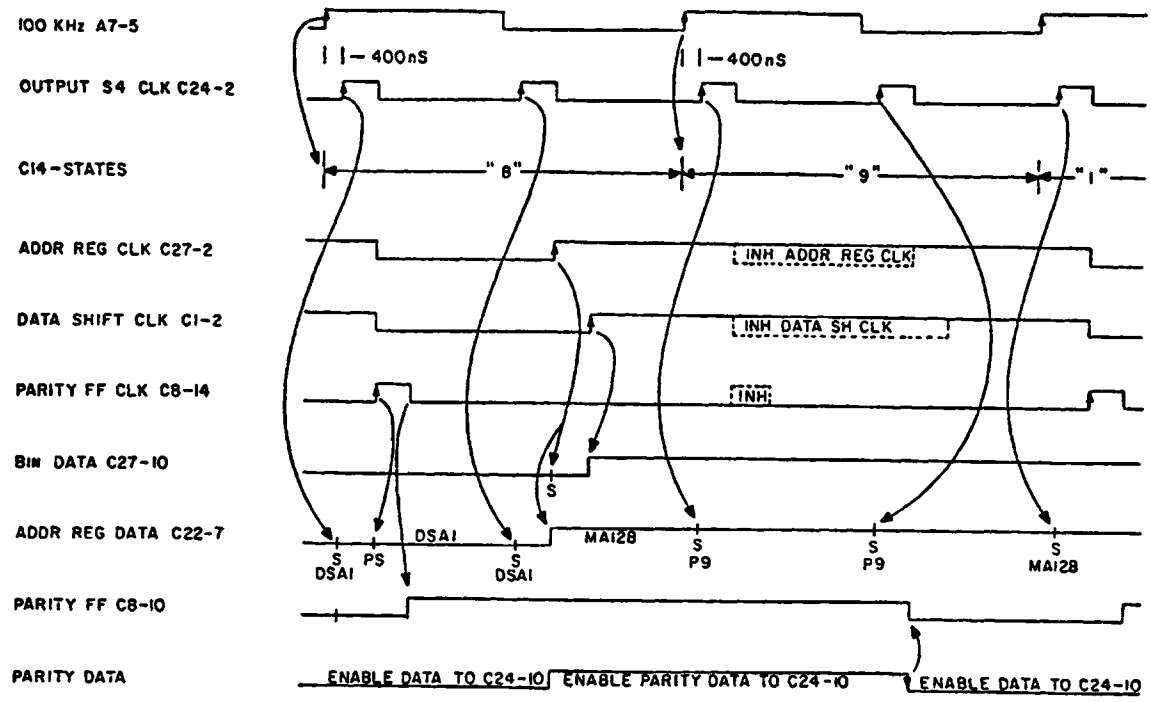
TIMING DIAGRAM 4: MONITOR DATA MULTIPLEX ADDRESS CLOCK PHASE GENERATOR



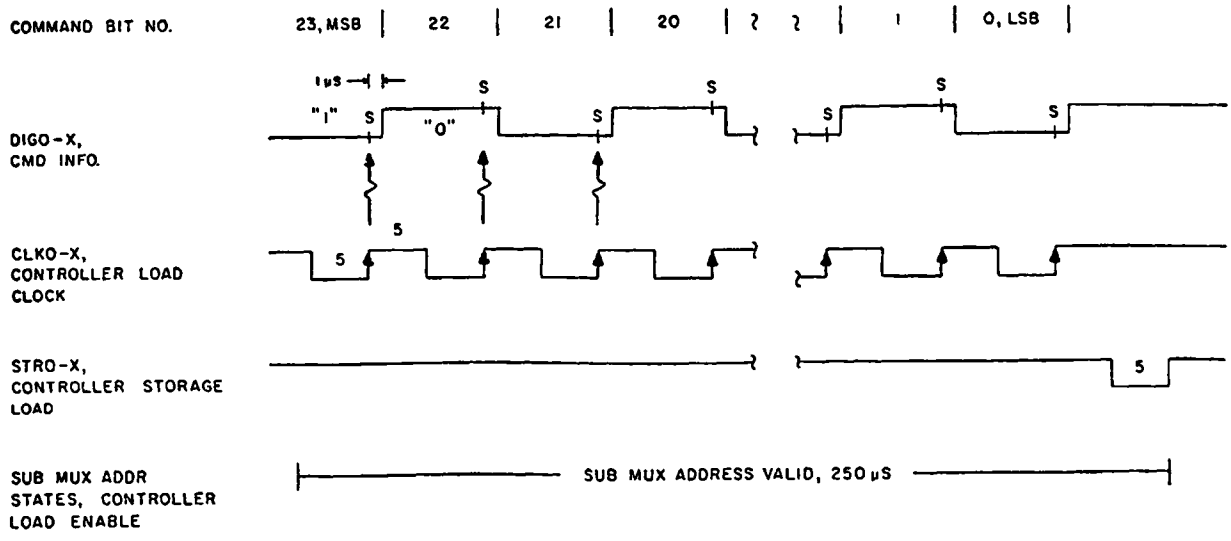
TIMING DIAGRAM 5: MONITOR DATA OUTPUT CLOCK GENERATOR



TIMING DIAGRAM 6: MONITOR DATA OUTPUT CLOCKING, START OF DATA OUTPUT

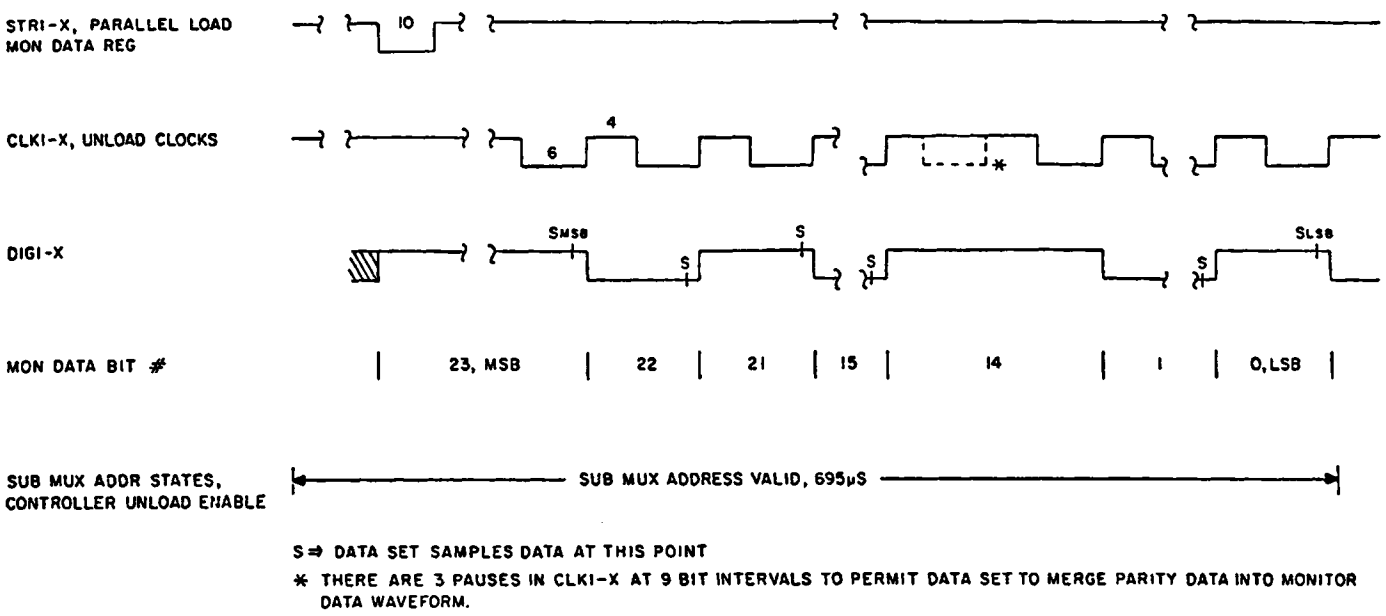


TIMING DIAGRAM 7: MONITOR DATA OUTPUT TIMING, PARITY DATA OUTPUT



S = CONTROLLER SAMPLES (ie. LOADS SHIFT REG.) CMD INFO. AT THIS POINT

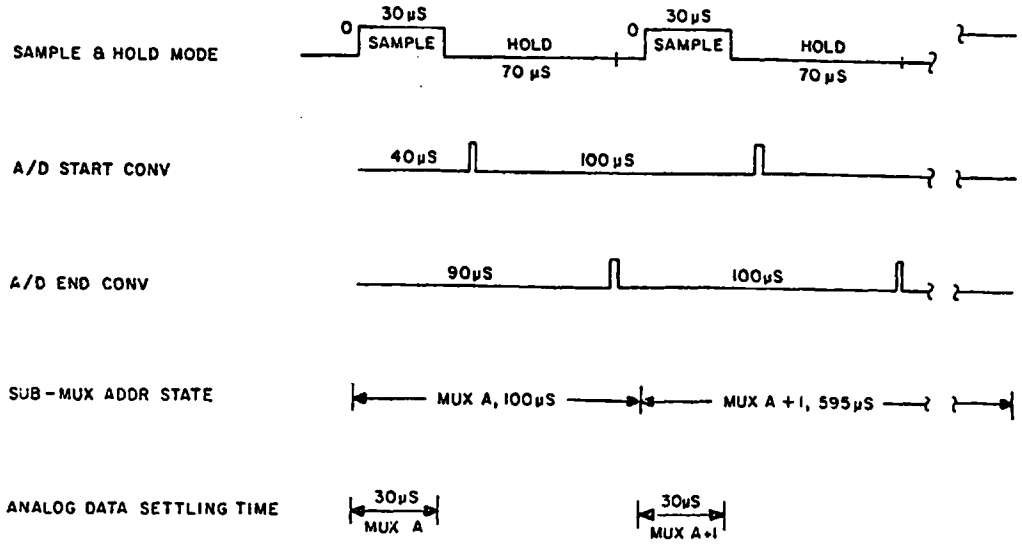
TIMING DIAGRAM 8 — CONTROLLER COMMAND LOAD TIMING



S ⇒ DATA SET SAMPLES DATA AT THIS POINT

* THERE ARE 3 PAUSES IN CLKI-X AT 9 BIT INTERVALS TO PERMIT DATA SET TO MERGE PARITY DATA INTO MONITOR DATA WAVEFORM.

TIMING DIAGRAM 9: CONTROLLER BINARY MONITOR DATA UNLOAD TIMING



TIMING DIAGRAM 10 – CONTROLLER ANALOG DATA TIMING

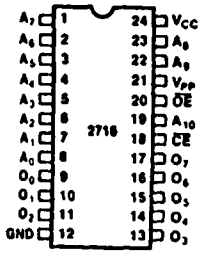
2716
16K (2K x 8) UV ERASABLE PROM

- **Fast Access Time**
  - — 2716-1: 350 ns Max.
  - — 2716-2: 390 ns Max.
  - — 2716: 450 ns Max.
  - — 2716-5: 490 ns Max.
  - — 2716-6: 650 ns Max.
- **Single +5V Power Supply**
- **Low Power Dissipation**
  - — Active Power: 525 mW Max.
  - — Standby Power: 132 mW Max.
- **Pin Compatible to Intel 2732A EPROM**
- **Simple Programming Requirements**
  - — Single Location Programming
  - — Programs with One 50 ms Pulse
- **Inputs and Outputs TTL Compatible During Read and Program**
- **Completely Static**

The Intel 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static standby mode, and features fast single-address programming. It makes designing with EPROMs fast, easy and economical.

The 2716, with its single 5-volt supply and with an access time up to 350 ns, is ideal for use with high-performance +5V microprocessors such as Intel's 8085 and 8086. Selected 2716-5s and 2716-6s are also available for slower speed applications. The 2716 also has a static standby mode which reduces power consumption without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 uses a simple and fast method for programming—a single TTL-level pulse. There is no need for high voltage pulsing because all programming controls are handled by TTL signals. Programming of any location at any time—either individually, sequentially or at random is possible with the 2716's single-address programming. Total programming time for all 16,384 bits is only 100 seconds.



PIN NAMES

A_0-A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS

Figure 1. Pin Configuration

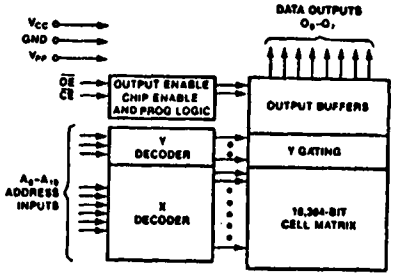


Figure 2. Block Diagram

PROGRAMMING CHARACTERSITICS

D.C. PROGRAMMING CHARACTERISTICS: T_A = 25°C ±5°C, V_{CC}[1] = 5V ±5%, V_{PP}[1,2] = 25V ±1V

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{LI}	Input Current (for Any Input)			10	μA	V_{IN} = 5.25V/0.45
I_{PP1}	V_{PP} Supply Current			5	mA	$\overline{CE}$ = V_{IL}
I_{PP2}	V_{PP} Supply Current During Programming Pulse			30	mA	$\overline{CE}$ = V_{IH}
I_{CC}	V_{CC} Supply Current			100	mA	
V_{IL}	Input Low Level	−0.1		0.8	V	
V_{IH}	Input High Level	2.0		V_{CC}+1	V	

A.C. PROGRAMMING CHARACTERISTICS: T_A = 25°C ±5°C, V_{CC}[1] = 5V ±5%, V_{PP}[1,2] = 25V ±1V

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions*
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	2			μs	
t_{OEH}	$\overline{OE}$ Hold Time	2			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	Output Enable to Output Float Delay	0		200	ns	$\overline{CE}$ = V_{IL}
t_{OE}	Output Enable to Output Delay			200	ns	$\overline{CE}$ = V_{IL}
t_{PW}	Program Pulse Width	45	50	55	ms	
t_{PRT}	Program Pulse Rise Time	5			ns	
t_{PFT}	Program Pulse Fall Time	5			ns	

***A.C. CONDITIONS OF TEST**

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.8 to 2.2V
Input Timing Reference Level ..... 0.8V and 2V
Output Timing Reference Level ..... 0.8V and 2V

NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The 2716 must not be inserted into or removed from a board with V_{PP} at 25 ±1V to prevent damage to the device.
2. The maximum allowable voltage which may be applied to the V_{PP} pin during programming is +26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 26V maximum specification.

Programming of multiple 2716s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2716s may be connected together when they are programmed with the same data. A high-level TTL pulse applied to the $\overline{CE}$ input programs the paralleled 2716s.

Program Inhibit

Programming of multiple 2716s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel 2716s may be common. A TTL-level program pulse applied to a 2716's $\overline{CE}$ input with V_{PP} at 25V will program that 2716. A low-level $\overline{CE}$ input inhibits the other 2716 from being programmed.

Verify

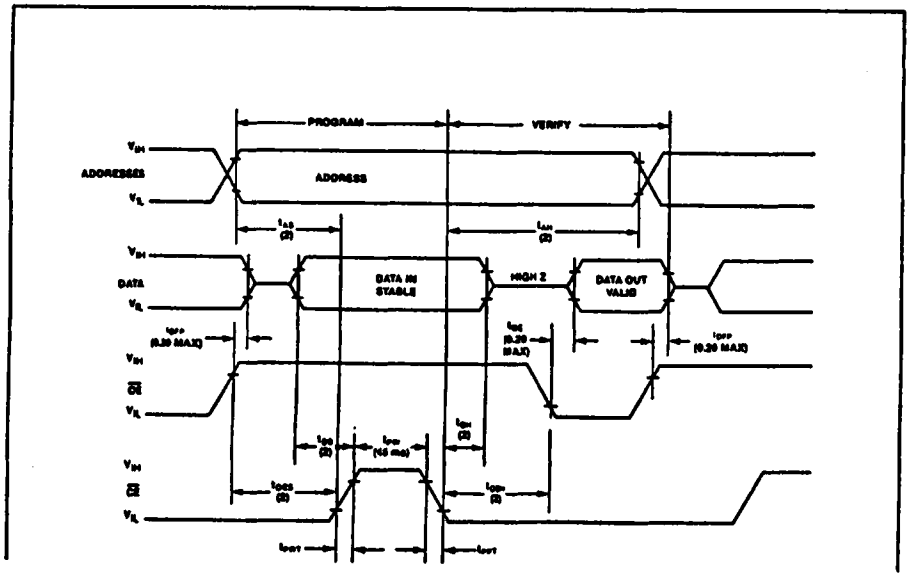
A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at 5V.

ERASURE CHARACTERISTICS

The erasure characteristics of the 2716 are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 Å range. Data show that constant exposure to room-level fluorescent lighting could erase the typical 2716 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 2716 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the 2716 window to prevent unintentional erasure.

The recommended erasure procedure for the 2716 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μ W/cm^2 power rating. The 2716 should be placed within 1 inch of the lamp tubes during erasure.

PROGRAMMING WAVEFORMS



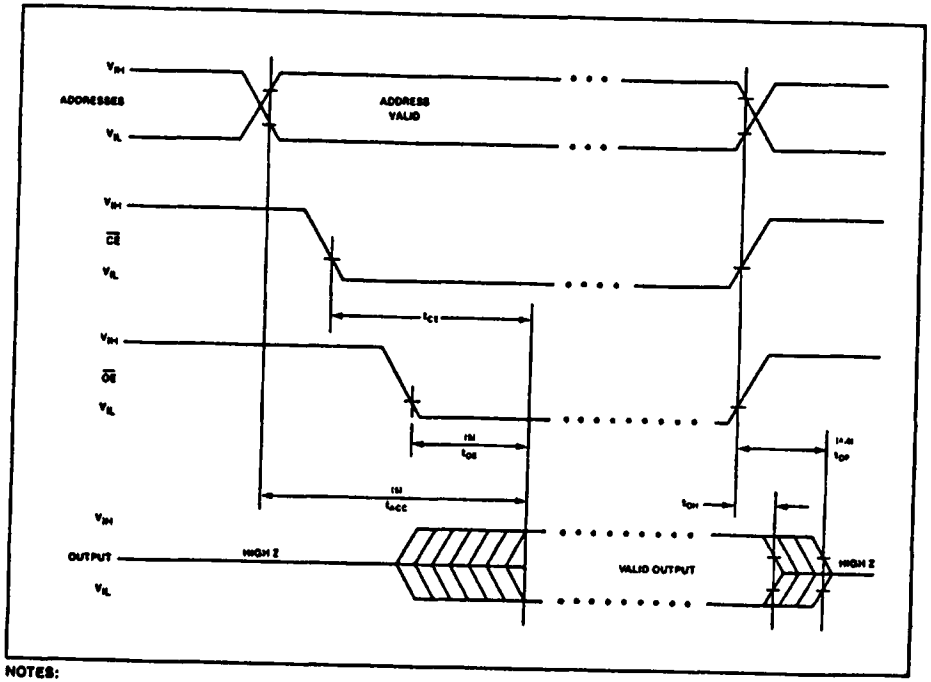
CAPACITANCE[4] (T_A = 25°C, f = 1 MHz)

Symbol	Parameter	Typ.[3]	Max.	Units	Test Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

†A.C. TEST CONDITIONS

Output Load ..... 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times ..... ≤20 ns
Input Pulse Levels ..... 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs ..... 0.8V and 2V
Outputs ..... 0.8V and 2V

A.C. WAVEFORMS[1]



NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for T_A = 25°C and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested.
5. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
6. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

DEVICE OPERATION

The six modes of operation of the 2716 are listed in Table 1. It should be noted that inputs for all modes are TTL levels. The power supplies required are a +5V V_{CC} and a V_{PP}. The V_{PP} power supply must be at 25V during the three programming modes, and must be at 5V in the other three modes.

Read Mode

The 2716 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The 2716 has a standby mode which reduces the maximum active power dissipation by 75%, from 525 mW to 132 mW. The 2716 is placed in the standby mode by applying a TTL-high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

Because 2716s are usually used in larger memory arrays, Intel has provided a 2-line control function that accomodates this use of multiple memory connections. The two-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ (pin 18) should be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low-power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

Initially, and after each erasure, all bits of the 2716 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2716 is in the programming mode when the V_{PP} power supply is at 25V and $\overline{OE}$ is at V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 msec, active-high, TTL program pulse is applied to the $\overline{CE}$ input. A pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec. The 2716 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Table 1. Mode Selection

Mode \ Pins	$\overline{CE}$ (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	Outputs (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Output Disable	V_{IL}	V_{IH}	+5	+5	High Z
Standby	V_{IH}	X	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +125°C
All Input or Output Voltages with Respect to Ground ..... +6V to −0.3V
V_{PP} Supply Voltage with Respect to Ground During Program ..... +26.5V to −0.3V

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND A.C. OPERATING CONDITIONS DURING READ

	2716	2716-1	2716-2	2716-5	2716-6
Temperature Range	0°C-70°C	0°C-70°C	0°C-70°C	0°C-70°C	0°C-70°C
V_{CC} Power Supply[1,2]	5V ±5%	5V ±10%	5V ±5%	5V ±5%	5V ±5%
V_{PP} Power Supply[2]	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}

READ OPERATION

D.C. CHARACTERISTICS

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.[3]	Max.		
I_{LI}	Input Load Current			10	μA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.25V
I_{PP1}[2]	V_{PP} Current			5	mA	V_{PP} = 5.25V
I_{CC1}[2]	V_{CC} Current (Standby)		10	25	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}
I_{CC2}[2]	V_{CC} Current (Active)		57	100	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
V_{IL}	Input Low Voltage	−0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 μA

A.C. CHARACTERISTICS

Symbol	Parameter	Limits (ns)										Test Conditions†
		2716		2716-1		2716-2		2716-5		2716-6		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address to Output Delay		450		350		390		450		450	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
t_{CE}	$\overline{CE}$ to Output Delay		450		350		390		490		650	$\overline{OE}$ = V_{IL}
t_{OE}[4]	Output Enable to Output Delay		120		120		120		160		200	$\overline{CE}$ = V_{IL}
t_{DF}[4,6]	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	100	0	100	0	100	0	100	0	100	$\overline{CE}$ = V_{IL}
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		0		0		$\overline{CE}$ = $\overline{OE}$ = V_{IL}

ANALOG DEVICES

Complete 16-Channel 12-Bit Integrated Circuit Data Acquisition System

AD363

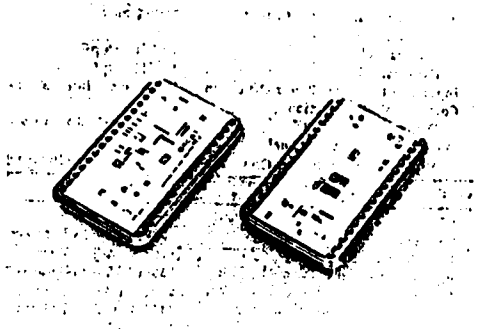
FEATURES

- Versatility
  - Complete System in Reliable IC Form
  - Small Size
  - 16 Single-Ended or 8 Differential Channels with Switchable Mode Control
  - Military/Aerospace Temperature Range: -55°C to +125°C (AD363S) MIL-STD-883B Processing Available
  - Versatile Input/Output/Control Format
  - Short-Cycle Capability
- Performance
  - True 12-Bit Operation: Nonlinearity ≤ ±0.012%
  - Guaranteed No Missing Codes Over Temperature Range
  - High Throughput Rate: 30kHz
  - Low Power: 1.7W
- Value
  - Complete: No Additional Parts Required
  - Reliable: Hybrid IC Construction, Hermetically Sealed, All Inputs Fully Protected
  - Precision +10.0 ±0.005 Volt Reference for External Application
  - Fast Precision Buffer Amplifier for External Application
  - Low Cost

PRODUCT DESCRIPTION

The AD363 is a complete 16 channel, 12-bit data acquisition system in integrated circuit form. By applying large-scale linear and digital integrated circuitry, thick and thin film hybrid technology and active laser trimming, the AD363 equals or exceeds the performance and versatility of previous modular designs.

The AD363 consists of two separate functional blocks. Each in hermetically-sealed 32 pin dual-in-line packages. The analog input section contains two eight-channel multiplexers, a differential amplifier, a sample-and-hold, a channel address register and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD363 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hard-wire programming and permits a mixture of single-ended and differential sources to be interfaced to an AD363 by dynamically switching the input mode control.



The Analog-to-Digital Converter Section contains a complete 12-bit successive approximation analog-to-digital converter, including internal clock, precision 10 volt reference, comparator, buffer amplifier and a proprietary-design 12-bit D/A converter. Active laser trimming of the reference and D/A converter results in maximum linearity errors of ±0.012% while performing a 12-bit conversion in 25 microseconds.

Analog input voltage ranges of ±2.5, ±5.0, ±10, 0 to +5 and 0 to +10 volts are user-selectable. Adding flexibility and value are the precision 10 volt reference (active-trimmed to a tolerance of ±5mV) and the internal buffer amplifier, both of which may be used for external applications. All digital signals are TTL/DTL compatible and output data is positive-true in parallel and serial form.

System throughput rate is as high as 30kHz at full rated accuracy. The AD363K is specified for operation over a 0 to +70°C temperature range while the AD363S operates to specification from -55°C to +125°C. Processing to MIL-STD-883B is available for the AD363S. Both device grades are guaranteed to have no missing codes over their specified temperature ranges.

This four-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional infor

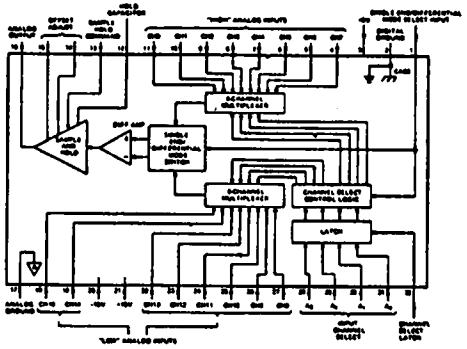
SPECIFICATIONS (typical @ +25°C, ±15V and +5V with 2000pF hold capacitor as provided unless otherwise noted)

MODEL	AD363K	AD363S
ANALOG INPUTS		
Number of Inputs	16 Single-Ended or 8 Differential (Electronically Selectable)	•
Input Voltage Ranges		
Bipolar	±2.5V, ±5.0V, ±10.0V	•
Unipolar	0 to +5V, 0 to +10V	•
Input (Bias) Current, Per Channel	±50nA max	•
Input Impedance		
On Channel	$10^{10}\Omega$, 100pF	•
Off Channel	$10^{10}\Omega$, 10pF	•
Input Fault Current (Power Off or On)	20mA, max, Internally Limited	•
Common Mode Rejection		
Differential Mode	70dB min (80dB typ) @ 1kHz, 20V p-p	•
Mux Crosstalk (Interchannel, Any Off Channel to Any On Channel)	-80dB max (-90dB typ) @ 1kHz, 20V p-p	•
RESOLUTION	12 BITS	•
ACCURACY		
Gain Error[1]	±0.05% FSR (Adj. to Zero)	•
Unipolar Offset Error	±10mV (Adj to Zero)	•
Bipolar Offset Error	±20mV (Adj to Zero)	•
Linearity Error	±½LSB max	•
Differential Linearity Error	±1LSB max (±½LSB typ)	•
Relative Accuracy	±0.025% FSR	•
Noise Error	1mV p-p, 0 to 1MHz	•
TEMPERATURE COEFFICIENTS		
Gain	±30ppm/°C max (±10ppm/°C typ)	±25ppm/°C max (±15ppm/°C typ)
Offset, ±10V Range	±10ppm/°C max (±5ppm/°C typ)	±8ppm/°C max (±5ppm/°C typ)
Differential Linearity	No Missing Codes Over Temperature Range	•
SIGNAL DYNAMICS		
Conversion Time[2]	25µs max (22µs typ)	•
Throughput Rate, Full Rated Accuracy	25kHz min (30kHz typ)	•
Sample and Hold		
Aperture Delay	100ns max (50ns typ)	•
Aperture Uncertainty	500ps max (100ps typ)	•
Acquisition Time To ±0.01% of Final Value for Full Scale Step	18µs max (10µs, typ)	•
Feedthrough	-70dB max (-80dB typ) @ 1kHz	•
Droop Rate	2mV/ms max (1mV/ms typ)	•
DIGITAL INPUT SIGNALS[3]		
Convert Command (to ADC Section, Pin 21)	Positive Pulse, 200ns min Width. Leading Edge ("0" to "1") Resets Register, Trailing Edge ("1" to "0") Starts Conversion.	•
	1TTL Load	•
Input Channel Select (To Analog Input Section, Pins 28-31)	4 Bit Binary, Channel Address.	•
	1LS TTL Load	•
Channel Select Latch (To Analog Input Section, Pin 32)	"1" Latch Transparent	•
	"0" Latched	•
	4LS TTL Loads	•
Sample-Hold Command (To Analog Input Section Pin 13 Normally Connected To ADC "Status", Pin 20)	"0" Sample Mode	•
	"1" Hold Mode	•
	2LS TTL Loads	•
Short Cycle (To ADC Section Pin 14)	Connect to +5V for 12 Bits Resolution.	•
	Connect to Output Bit n + 1 For n Bits Resolution.	•
	1TTL Load	•
Single Ended/Differential Mode Select (To Analog Input Section, Pin 1)	"0": Single-Ended Mode	•
	"1": Differential Mode	•
	1TTL Loads	•

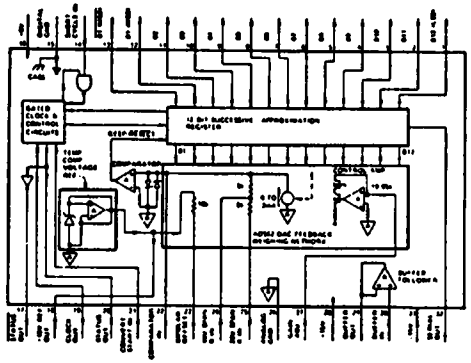
MODEL	AD363K	AD363S
DIGITAL OUTPUT SIGNALS[3]		
(All Codes Positive True)		
Parallel Data		
Unipolar Code	Binary	•
Bipolar Code	Offset Binary/Two's Complement	•
Output Drive	2TTL Loads	•
Serial Data (NRZ Format)		
Unipolar Code	Binary	•
Bipolar Code	Offset Binary	•
Output Drive	2TTL Loads	•
Status ($\overline{\text{Status}}$)	Logic "1" ("0") During Conversion	•
Output Drive	2TTL Loads	•
Internal Clock		
Output Drive	2TTL Loads	•
Frequency	500kHz	•
INTERNAL REFERENCE VOLTAGE	+10.00V, ±10mV	•
Max External Current	±1mA	•
Voltage Temp. Coefficient	±20ppm/°C, max	•
POWER REQUIREMENTS		
Supply Voltages/Currents	+15V, ±5% @ +45mA max (+38mA typ)	•
	-15V, ±5% @ -45mA max (-38mA typ)	•
	+5V, ±5% @ +136mA max (+113mA typ)	•
Total Power Dissipation	2 watts max (1.7 watts typ)	•
TEMPERATURE RANGE		
Specification	0 to +70°C	-55°C to +125°C
Storage	-55°C to +85°C[4]	-55°C to +150°C

NOTES.
[1] With 500Ω, 1% fixed resistor in place of Gain Adjust pot.
[2] Conversion time of ADC Section.
[3] One TTL Load is defined as I_{IL} = -1.6mA max @ V_{IL} = 0.4V, I_{IH} = 40μA max @ V_{IH} = 2.4V.
One LS TTL Load is defined as I_{IL} = -0.36mA max @ V_{IL} = 0.4V, I_{IH} = 20μA max @ V_{IH} = 2.7V.
[4] AD363K External Hold Capacitor is limited to +85°C. Analog Input Section and ADC Section may be stored at up to +150°C.

*Specifications same as AD363K.
Specifications subject to change without notice.

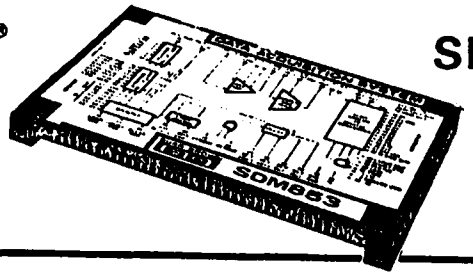


AD363 Analog Input Section Functional Block Diagram and Pinout



AD363 ADC Section (AD572) Functional Diagram and Pinout

BURR-BROWN®



SDM853

DATA ACQUISITION SYSTEM

FEATURES

- SAVES DESIGN TIME
- RELIABLE - 168-hour bake
- LOW LEVEL OR HIGH LEVEL INPUTS
- SAVES SPACE
- FLEXIBLE - Up to four modes of operation
- LOW COST

DESCRIPTION

The SDM853 is a complete 8- or 16-channel data acquisition system in a compact 4.6" x 3.0" x 0.375" metal case. This system differs from most in that it can acquire and digitize low level or high level analog signals. A built-in high quality instrumentation amplifier allows input signal ranges of ±10mV to ±10V. This means that the SDM853 can be connected to low level sensors such as thermocouples and strain gauges without external signal conditioning.

This expandable module accepts either 16 single-ended or 8 differential inputs and converts the multiplexed data signals into 12-bit digial words with an accuracy of ±0.025% at throughput rates of up to 33,000 samples per second.

International Airport Industrial Park • P.O. Box [redacted] • Tel. [redacted] • Twx: [redacted] • Cable: [redacted] • Telex: [redacted]

DISCUSSION OF PERFORMANCE

The SDM853 is a complete modular "off the shelf" data acquisition system. With this system it is possible to configure complete data acquisition systems in one-fourth the space for a fraction of the cost previously possible.

These systems contain all the components necessary to multiplex and convert ±10mV to ±10V analog data into equivalent digital outputs yielding resolutions of 2.4μV to 2.4mV. The minimum throughput sampling rates are up to 30 kHz for 12 bit and up to 43 kHz for 8 bit resolution. The model SDM853 contains an analog multiplexer which can be connected in a 16 channel single ended or 8 channel differential mode, instrumentation amplifier, sample/hold, 12 bit successive approximation A/D converter and programming logic. The amplifier and sample/hold are not internally interconnected. This allows maximum application flexibility. These systems can be expanded without limit using Burr-Brown's MPC-16S and MPC-8D monolithic multiplexers. Figure 1 shows the components of the SDM853. The system is designed to be mounted on a printed circuit card. The only requirement for system operation are input signals, power and the interconnection of the system components into the desired operating configuration.

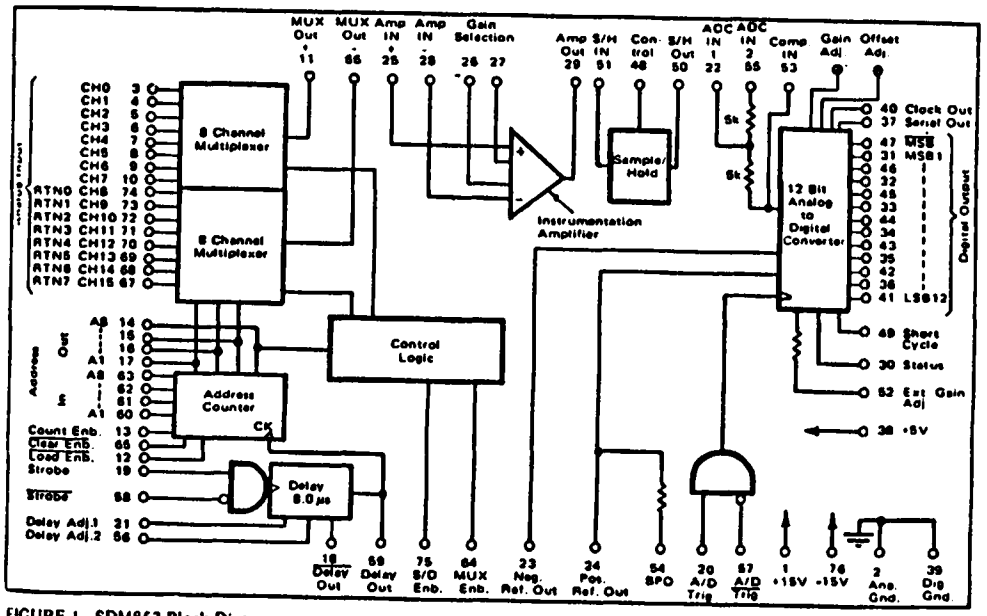


FIGURE 1. SDM853 Block Diagram.

ANALOG MULTIPLEXER

Two one of eight CMOS analog multiplexers are used to allow user selection by external jumpers of 16 single ended channel or 8 double ended channel operation. In 16 channel operation the multiplexer may be used in a pseudo differential mode by connecting the amplifier inverting input to a common, remote, signal ground. Channel selection is by [redacted] bit binary word stored [redacted] settable address counter. Channel capacity is

INSTRUMENTATION AMPLIFIER

The instrumentation amplifier is a low drift, differential amplifier featuring high speed at gains above unity, and external gain programming with an external resistor. With the gain programming pins open, the gain is unity. Gain may be selected from unity to 60 dB.

Coding	One standard TTL load, positive true
Load Enable	4-bit binary
Clear Enable	One standard TTL load, negative true, address loaded with strobe inputs
Strobe A, Strobe	One standard TTL load, negative true, address loaded with strobe inputs
Count Enable	One standard TTL load. STROBE and STROBE edge trigger the delay timer and clock the address counter. STROBE must be high to enable STROBE and STROBE must be low to enable STROBE. Two standard TTL loads, positive true, logic "0" allows the Strobe inputs to trigger the delay timer, but prevents the MUX address counter from being clocked
ADC trigger	One standard TTL load, a positive going edge at TRIG initiates conversion, a negative going edge at TRIG initiates conversion. TRIG must be "0" to enable TRIG, TRIG must be "1" to enable TRIG
Short cycle	One standard TTL load, logical 1 for 12-bit resolution, connected to the N + 1 bit output for N bit resolution
Multiplexer Enable	Two standard TTL loads, logical 1 enable multiplexer output and logical 0 turns off all channels
Multiplexer Enable	Two standard TTL loads, logical 1 enables 16-channel single-ended operation and logical 0 enable 8-channel differential operation
S/D select	

DIGITAL OUTPUT SPECIFICATIONS

Data outputs	
Parallel B1, B1 ... B12	2 Standard TTL loads, negative true
Serial out	2 Standard TTL loads, negative true, time serial data output beginning with B1, (see timing diagram)
Address outputs	5 Standard TTL loads, positive true, 4-bit binary code, internal 2kΩ pull-up resistors
Delay out (Delay Out)	5 Standard TTL loads high (low) during the delay period, triggered by Strobe and Strobe inputs
Clock	5 Standard TTL loads for synchronizing serial out data (see timing diagram).
Status	5 Standard TTL loads, high during the A/D conversion

SYSTEM TIMING DIAGRAMS

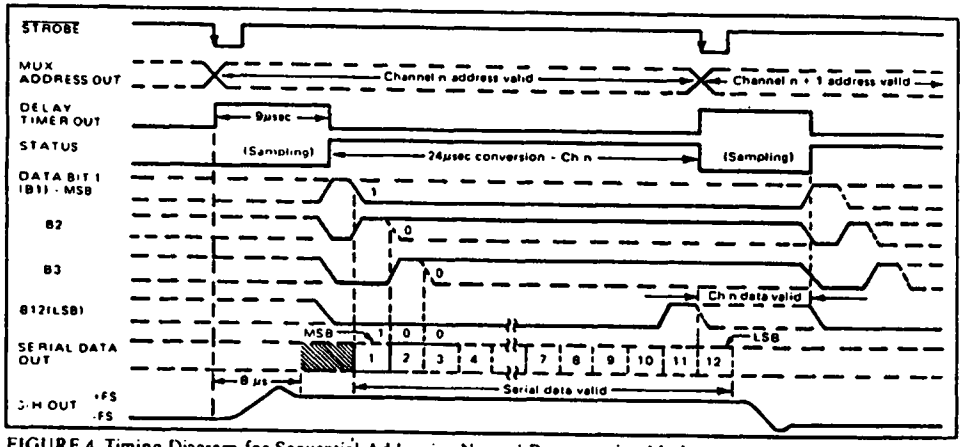


FIGURE 4. Timing Diagram for Sequential Addressing Normal Programming Mode.

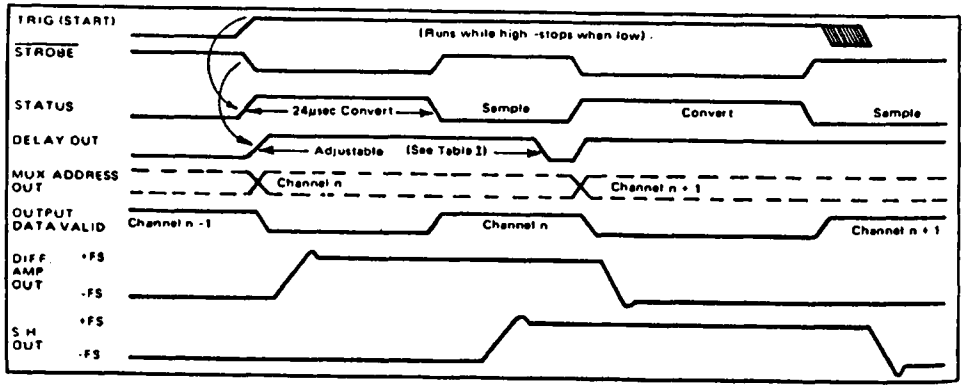
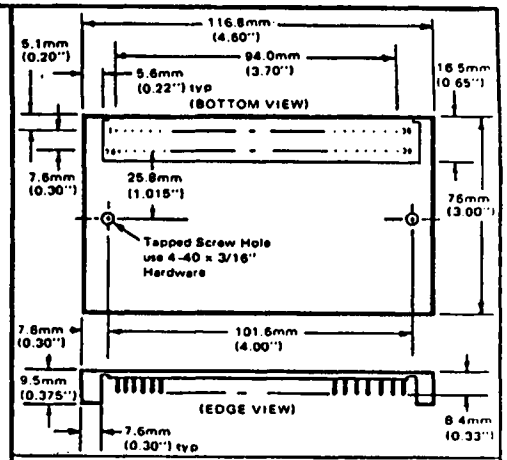


FIGURE 5. Timing Diagram for Sequential Overlap Programming Mode. (Delay must be adjusted to status pulse.)

PACKAGE AND PIN CONFIGURATION

SDM853 CONNECTOR PIN DIAGRAM

+15V	1	76	-15V
ANA. GND.	2	75	S/D ENB
CH 0 IN	3	74	CH 8 IN (0 RTN)
CH 1 IN	4	73	CH 9 IN (1 RTN)
CH 2 IN	5	72	CH 10 IN (2 RTN)
CH 3 IN	6	71	CH 11 IN (3 RTN)
CH 4 IN	7	70	CH 12 IN (4 RTN)
CH 5 IN	8	69	CH 13 IN (5 RTN)
CH 6 IN	9	68	CH 14 IN (6 RTN)
CH 7 IN	10	67	CH 15 IN (7 RTN)
MUX OUT HI	11	66	MUX OUT LO
LOAD ENB	12	65	CLR ENB
COUNT ENB	13	64	MUX ENB
A8 OUT	14	63	A8 IN
A4 OUT	15	62	A4 IN
A2 OUT	16	61	A2 IN
A1 OUT	17	60	A1 IN
DLY.	18	59	DLY.
STROBE	19	58	STROBE
ADC TRIG	20	57	ADC TRIG
DLY. ADJ. 1	21	56	DLY. ADJ. 2
R1	22	55	R2
NEG REF OUT	23	54	BPO
POS. REF OUT	24	53	COMP IN
AMP IN HI	25	52	GAIN ADJ.
G2	26	51	S/H IN
G1	27	50	S/H OUT
AMP IN LO	28	49	SHT. CYC.
AMP OUT	29	48	S/H CONTROL
STATUS	30	47	B1
B1 MSB	31	46	B2
B3	32	45	B4
B5	33	44	B6
B7	34	43	B8
B9	35	42	B10
B11	36	41	B12 LSB
SER OUT	37	40	CLK. OUT
+5	38	39	DIG RTN



CASE MATERIAL: Insulated Steel
CONNECTOR PINS: Gold Flashed
WEIGHT: 145 grams (5 oz.)

MOUNTING INSTRUCTIONS:

MOUNTING FLUSH ON PC CARD

1. Use strip connectors or two 14 pin and three 16 pin low profile IC sockets (shipped with each unit).
2. Use 4-40 x 3/16" (4.8mm) LG Pan HD Hardware to secure the SDM853 to PC Card.

SAMPLE AND HOLD AMPLIFIERS

The sample and hold amplifier is a complete, stand alone, sample and hold circuit featuring buffered output, 7μsec acquisition time, and 30nsec aperture time. Input, output and mode control functions are brought to separate connector pins. This allows maximum system flexability for performing such functions as automatic gain ranging with no loss of aperture time.

ANALOG-TO-DIGITAL CONVERTER

The ADC is a ceramic packaged, 12-bit converter featuring 24μsec conversion time and 0.01% accuracy. Thin-film networks and current switching are used to assure linearity over wide temperature ranges.

ADDRESS COUNTER

A 4-bit binary address counter is connected to the multiplexer. This counter may be externally loaded, cleared, clocked or enabled. The address outputs are brought to connector pins for convenient system control.

DELAY TIMER

The delay timer is provided to allow for the settling time of the multiplexer, amplifier, and sample and hold circuits. The delay time is adjustable over a wide range by an external potentiometer and/or external capacitor. This allows for the longer settling time of the instrument amplifier at high gains.

CONTROL LOGIC

Delay and ADC trigger functions are edge-triggered and gated. Counter control functions are synchronous with the counter clock which is internally connected to the delay timer output.

CHANNEL EXPANSION

The number of analog input channels of these systems can easily be increased using Burr-Brown's MPC8D and MPC16S CMOS multiplexers. The MPC8D is an 8-channel differential model and the MPC16S is a 16-channel single-ended model. These are latch-free devices which contain internal binary decoding, TTL or MOS logic levels, and may be integrated into a system with minimum external logic.

SYSTEM PERFORMANCE

The SDM853 can be configured to continuously sequence through all analog channels, to accept random addresses or to sequence through all analog channels on command from an external trigger.

The status signal, pin 30, is connected to the strobe input of the delay timer, pin 58, for normal programmed sequencing with a minimum throughput sampling rate of 30kHz for 12-bit resolution.

By using "overlap" programming, the settling time effects of the analog multiplexer and instrumentation amplifier can be reduced, extending throughput sampling rates up to 32kHz for 12-bit and 43kHz for 8-bit resolution. This mode of operation is most useful when converting low level inputs to accommodate the increased settling time of the instrumentation amplifier. Overlap programming is accomplished by connecting the status signal, pin 30, to the strobe input of the delay timer, pin 19, and extending the delay time. The internal logic will then select analog channel (n + 1) while channel n is being converted.

SYSTEM PERFORMANCE

(Typical at 25°C and rated supplies)

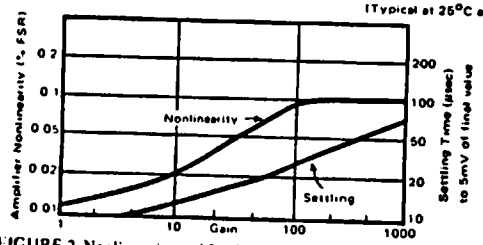


FIGURE 2. Nonlinearity and Settling Time vs. Amplifier Gain.

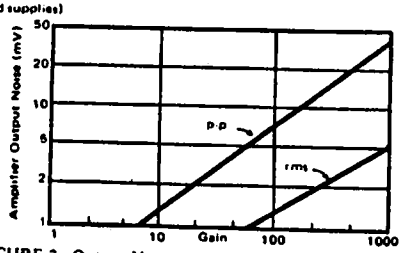


FIGURE 3. Output Noise vs. Amplifier Gain.

System Gain	System Accuracy	Throughput Rate (Channels/sec)		Delay Time (μsec)	
V/V		Normal	Overlap	Normal	Overlap
1	±0.025% FSR	30k	32k	9	31
10	±0.035% FSR	25k	32k	18	
100	±0.08% FSR	20k	32k	25	31
1000	±0.1% FSR	10k	14k	70	70

TABLE I. Throughput Rate vs. Gain for Normal and Overlap Modes.

FSR	ADC Range	Amplifier Gain	Resolution	Delay for Settling to ±0.2% (μsec)	Delay for Settling to ±0.05% (μsec)	Delay for Settling to 0.01% (μsec)
20V	±10V	1	4.88mV	7	8	9
1V	0 to 10V	10	244μV	10	15	18
0.1V	0 to 10V	100	24.4μV	20	28	30
10mV	0 to 10V	1000	2.44μV*	60	70	-

TABLE II. This table shows the delay timer setting required to allow for the settling time of the instrumentation amplifier to the accuracies specified. Add the 24μsec conversion time of the A/D converter to the above delay times to obtain channel conversion times. * Depends on desired S/N ratio.

ELECTRICAL SPECIFICATIONS

Typical at 25°C and rated power supplies unless otherwise noted.

MODEL	SDM853
TRANSFER CHARACTERISTICS	
Throughput Rate, min	30kHz, 33μsec/channel
Resolution	12 Bits
Number of Channels	16 single-ended/8 differential
ANALOG INPUTS	
ADC gain ranges	0-5V, 0-10V, ±2.5V, ±5V, ±10V
Amplifier gain range	1 to 1000
Amplifier gain equation	$G = 1 + 20k\Omega/R_{ext}$[1]
Max. input voltage without damage	±16V
Max. input voltage for multiplexer operation[2]	±10.24V
Input impedance	100MΩ, 10pF OFF channel 100MΩ, 100pF ON channel
Bias current	
25°C	20nA
0°C to 70°C	50nA
Differential Bias Current (25°C)	10nA
Differential Bias Current Drift	0.1nA/°C
Amplifier output noise (Gain = 100, R_s = 500Ω)	1.2mV, rms; 7mV, p-p
Amplifier input offset voltage, max	400μV
Amplifier voltage offset drift	$2 + 20/G\ \mu V/°C$
ACCURACY[3]	
System RSS accuracy at 25°C (Gain = 1)	±0.025% FSR[4] at 30kHz throughput
Linearity (Gain = 1)	±1/2LSB, at 30kHz throughput
Differential linearity (Gain = 1)	±1/2LSB, at 30kHz throughput
Quantizing error	±1/2LSB
Gain error	Adjustable to zero
Offset error	Adjustable to zero
Power supply sensitivity	±0.005% FSR/% change of supply voltage
STABILITY OVER TEMPERATURE	
System accuracy drift, max	±30ppm/°C of reading
Linearity drift	±3ppm of FSR/°C
DYNAMIC ACCURACY	
Sample & Hold aperture time	30nsec
Aperture time uncertainty	±5nsec
Error for full scale transition between successively addressed channels	1LSB at 30kHz
Differential amplifier CMRR (Gain = 1)	74dB at 1kHz, 65dB at 3kHz (100dB at 60Hz Gain = 1000)
Channel cross talk	80dB down at 2kHz, for OFF channel to ON channel
Sample & Hold feedthrough	80dB down at 5kHz
Sample & Hold decay rate	10μV/μsec
OUTPUT	
Output Coding (Complementary)	Unipolar Straight Binary, Bipolar Offset, Binary Two's Complement
Gain trim[4][5]	Adjustable to zero error
Offset trim[4][5]	Adjustable to zero error
A/D Conversion-Time	24μsec
Delay	9μsec nominal, externally adjustable from 5.5μsec to 14μsec[5][6]
POWER REQUIREMENTS	±15VDC ±3% at +50mA, 5mV, rms, ripple -15VDC ±3% at -75mA, 5mV, rms, ripple +5VDC ±5% at +300mA, 25mV, rms, ripple
ENVIRONMENTAL	
Operating temperature	0°C to 70°C
Storage temperature	-25°C to +85°C
Relative humidity	95% noncondensing

1. With R_{ext} between pins 26 and 27.
2. No missing codes guaranteed.
3. FSR means Full Scale Range.
4. Gain and Offset controls are located in the module. The adjustment ranges are ±0.1% FSR for Gain and ±0.1% FSR for Offset.
5. Adjustable to 10 seconds with external capacitor.
6. For differential operation with gain > 1, the common-mode input voltage range is ±5V.

REVISIONS

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
F	1-31-79			REDRAWN WAS C13720P57

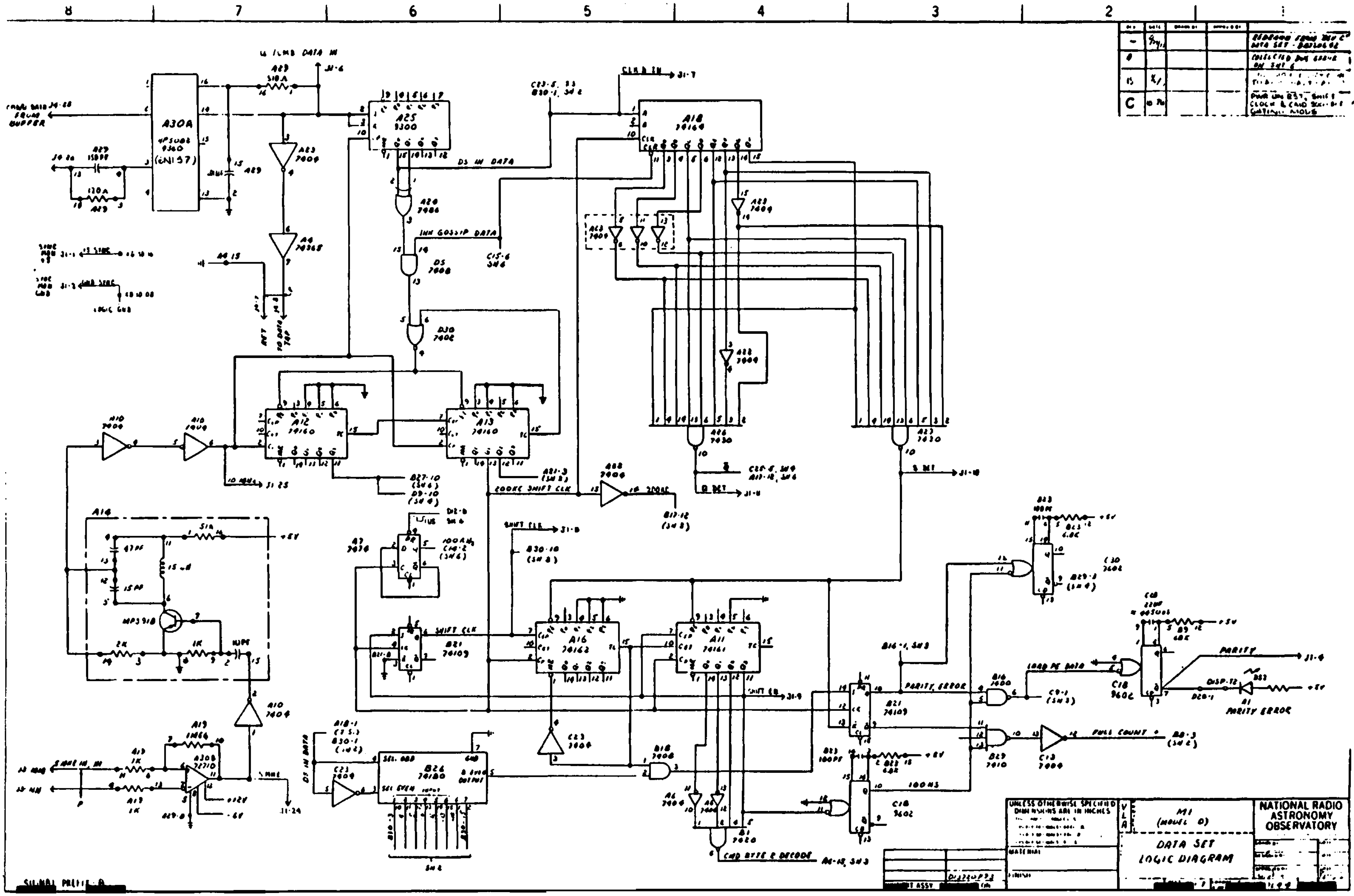
DRAWN BY	DATE			M1
DESIGNED BY	DATE			D13720P56
APPROVED BY	DATE			D13720P73
			NEXT ASSY	USED ON

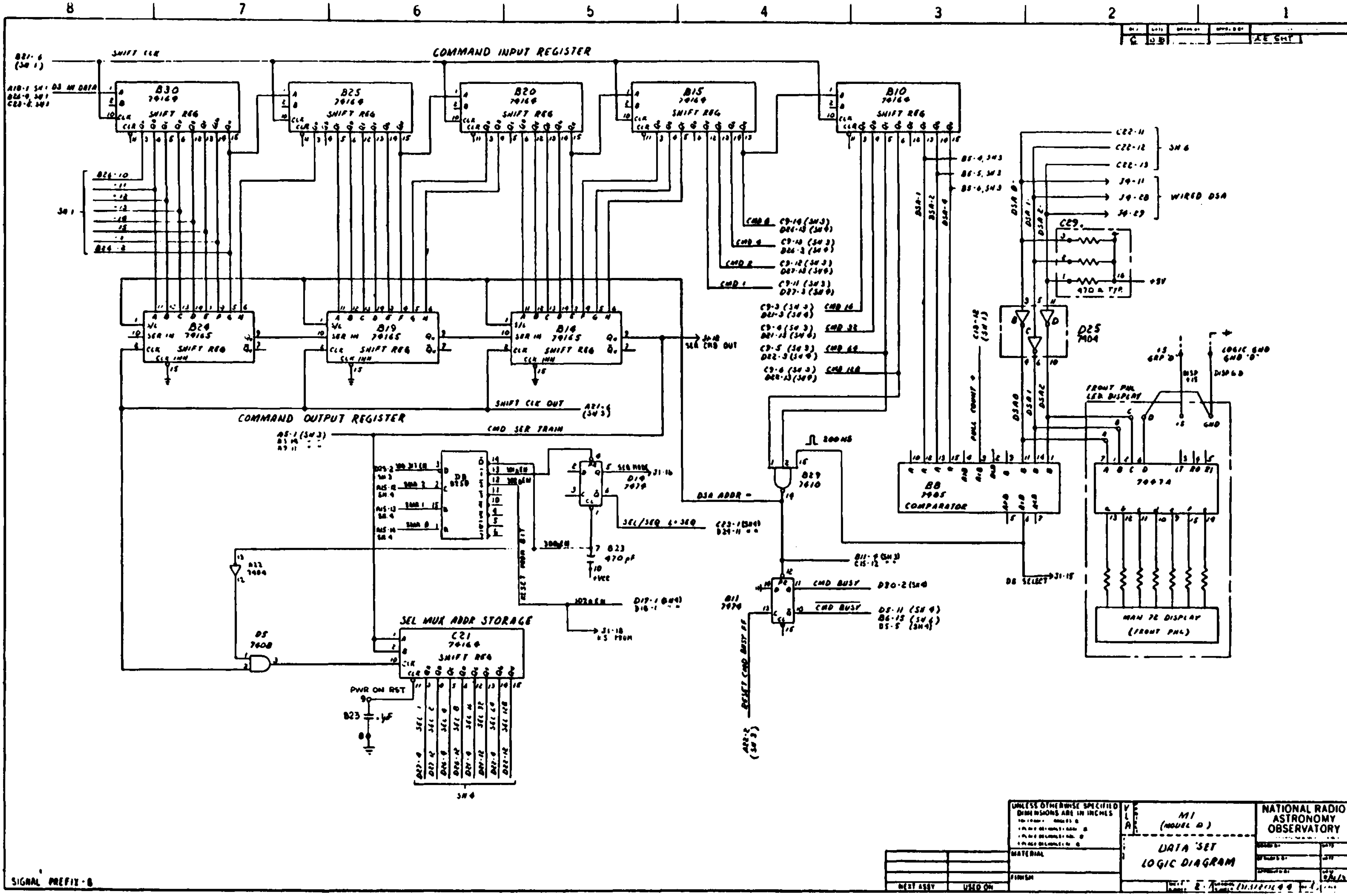
BILL OF MATERIALS: MODEL C : A13720E84
MODEL D : A13720E99

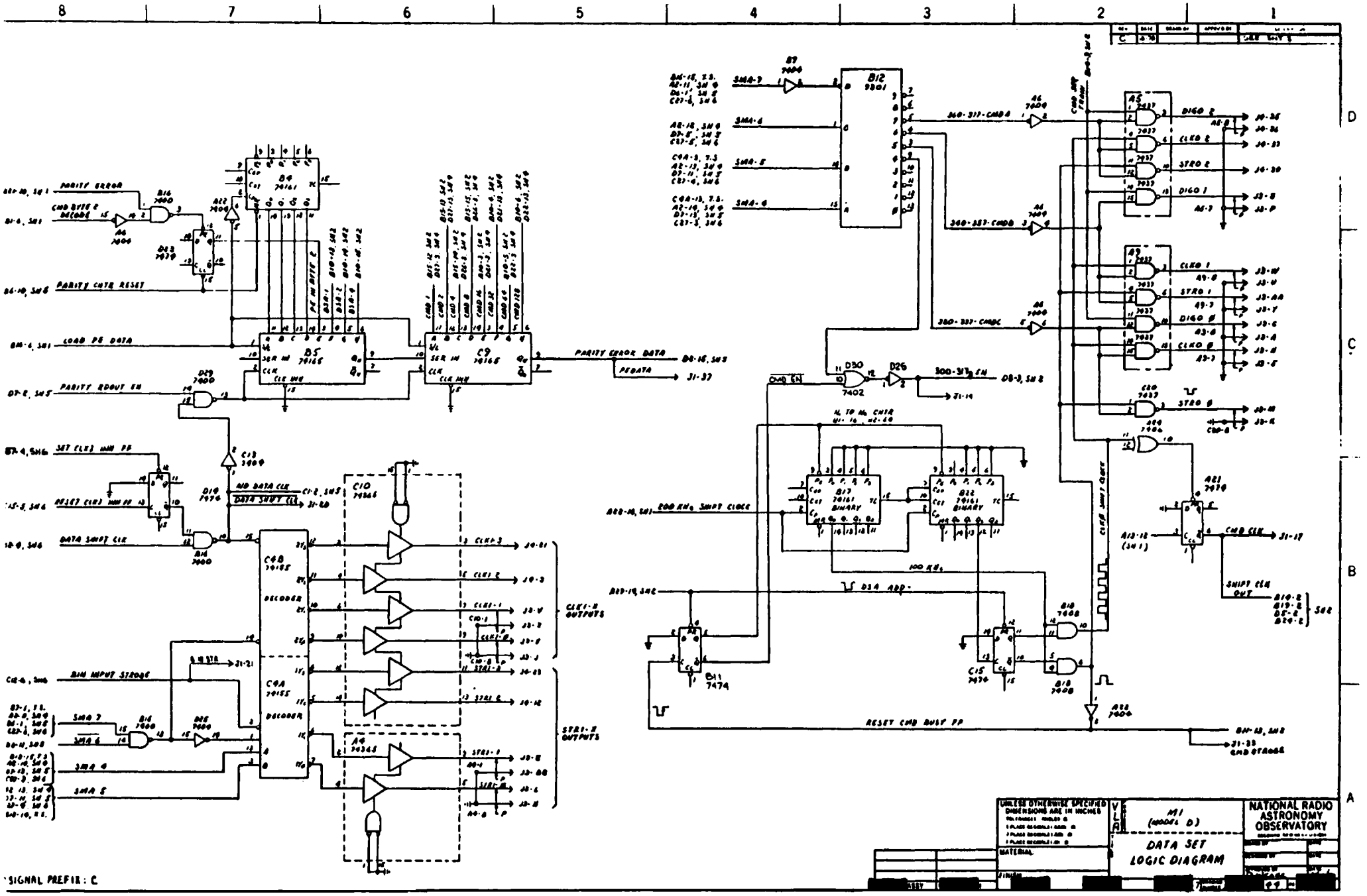
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

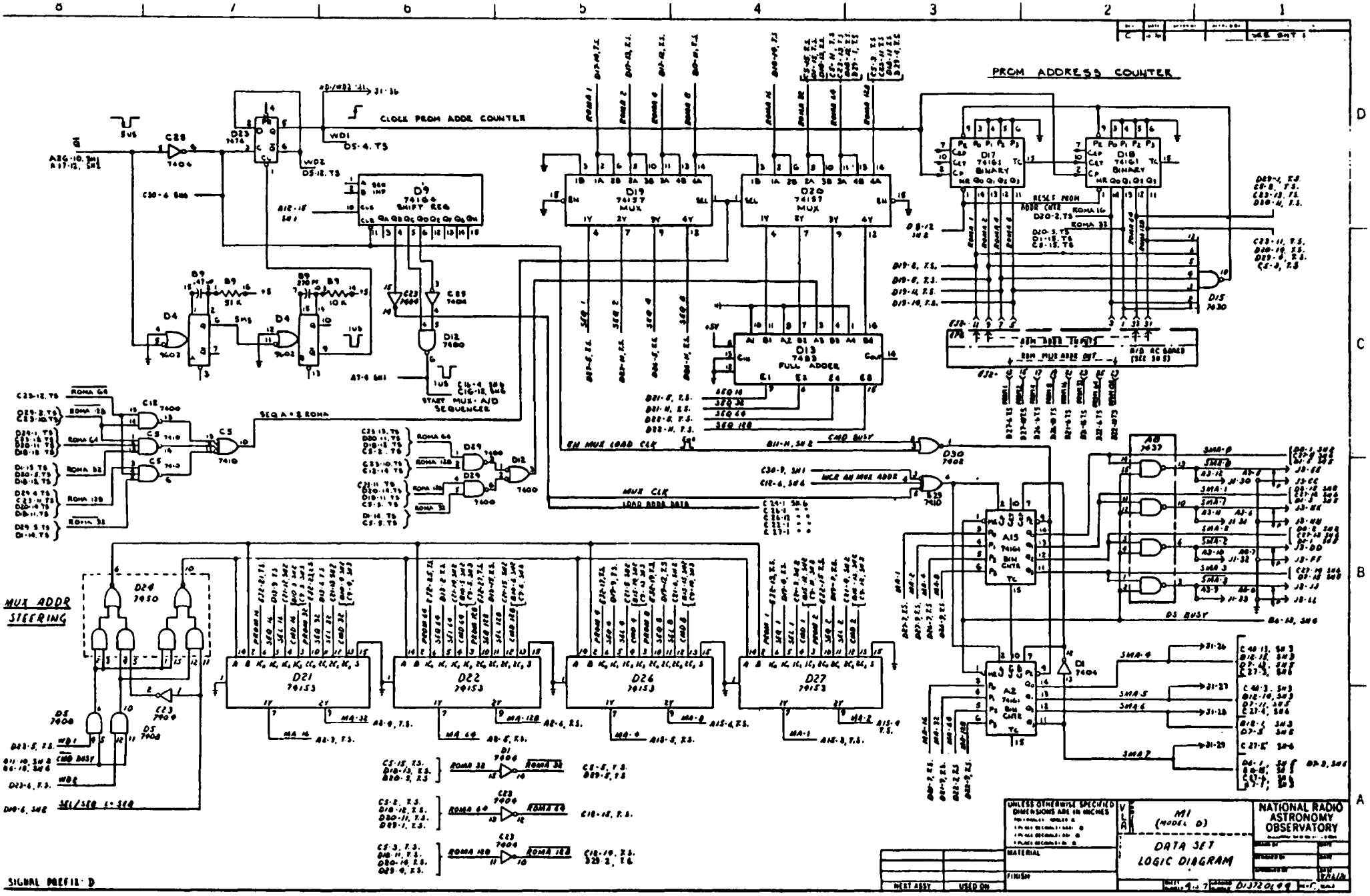
VLA

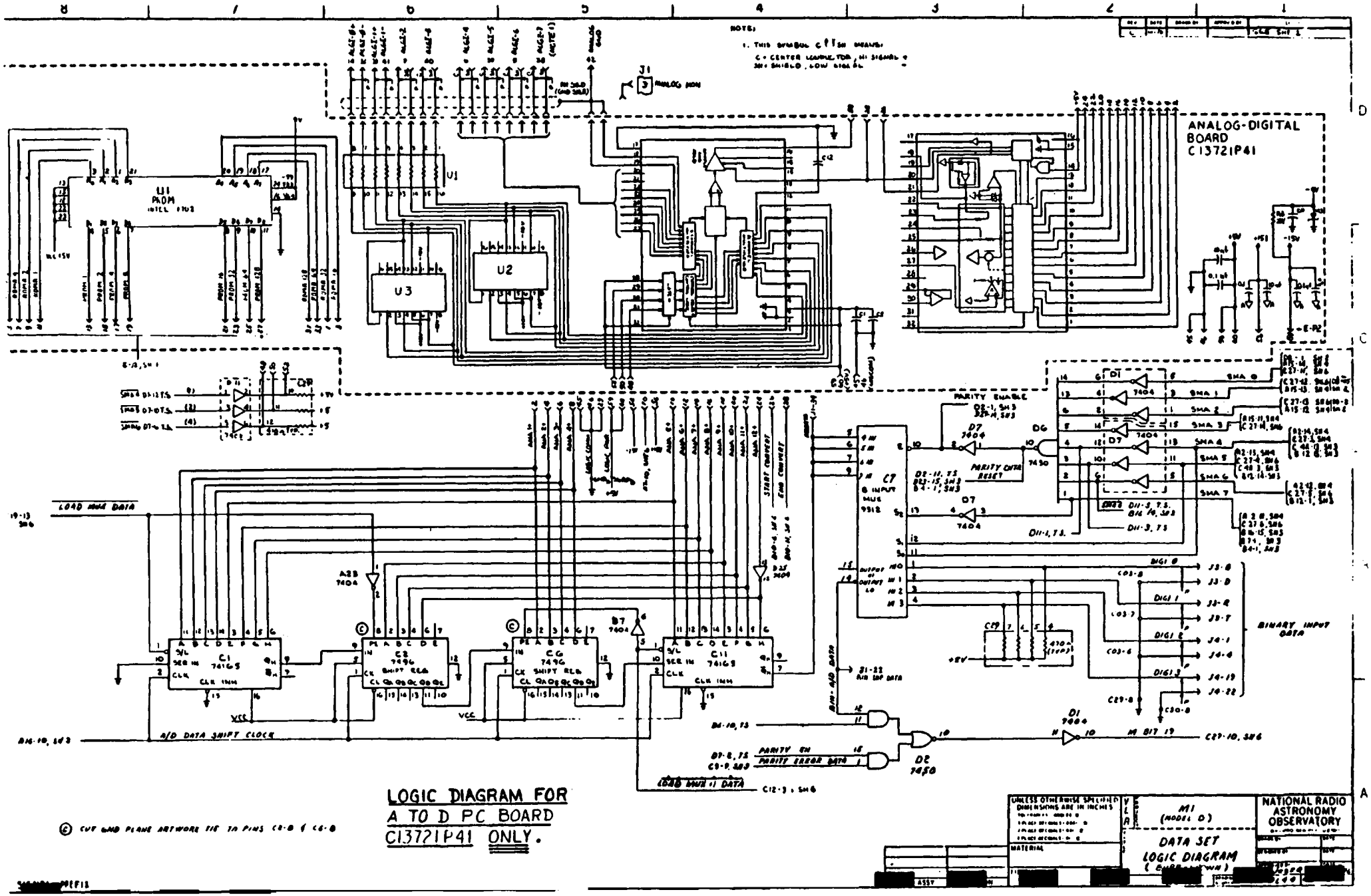
PROJECT M1
TITLE I.C. MODULE PANEL
DATA SET MODEL C+D
DWG NO. A13720P57 SHEET OF


NATIONAL RADIO ASTRONOMY OBSERVATORY
M1 (MODEL D)
DATA SET LOGIC DIAGRAM
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
A30A
A25 9300
A18 74164
A12 74160
A13 74160
A16 74162
A11 74161
B26 74180
DS IN DATA
INH GOSSIP DATA
SHIFT CLK
PARITY
PARITY ERROR
PARITY ERROR
FULL COUNT
CMD BYTE 2 DECODE
MP3918


COMMAND INPUT REGISTER
SHIFT CLK
B30 74164 SHIFT REG
B25 74164 SHIFT REG
B20 74164 SHIFT REG
B15 74164 SHIFT REG
B10 74164 SHIFT REG
B24 74165 SHIFT REG
B19 74165 SHIFT REG
B14 74165 SHIFT REG
SER CMD OUT
SHIFT CLK OUT
COMMAND OUTPUT REGISTER
CMD SER TRAIN
SEL MUX ADDR STORAGE
C21 74164 SHIFT REG
PWR ON RST
SH 4
SH 6
WIRED DSA
D25 7404
B8 7485 COMPARATOR
DSA ADDR
CMD BUSY
FRONT PNL LED DISPLAY
MAN 72 DISPLAY (FRONT PNL)
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL
FINISH
NEXT ASSY
USED ON
M1 (MODEL D)
DATA SET LOGIC DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY
SIGNAL PREFIX-B


8
7
6
5
4
3
2
1
D
C
B
A
PARITY ERROR
CMD BYTE 0 DECODE
PARITY CNTR RESET
LOAD PS DATA
PARITY RDOUT EN
SET CLK1 MM PP
RESET CLK1 MM PP
DATA SHIFT CLK
AND DATA CLK
DATA SHIFT CLK
BIN INPUT STROBE
PARITY ERROR DATA
PDATA
SMA 7
SMA 6
SMA 4
SMA 5
CLK1-A OUTPUTS
STR1-A OUTPUTS
200 KHz SHIFT CLOCK
100 KHz
RESET CMD BUSY PP
CMD BYTE 0
CMD EN
CMD CLK
SHIFT CLK OUT
CLK1 SHIFT CLK
DSA ARP
DIGO E
CLKO E
STRO E
DIGO I
CLKO I
STRO I
DIGO B
CLKO B
STRO B
SIGNAL PREFIX : C
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL
M1 (MODEL D)
DATA SET LOGIC DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY


PROM ADDRESS COUNTER
CLOCK PROM ADDR COUNTER
MUX ADDR STEERING
SEQ A + B ROMA
EN MUX LOAD CLK
MUX CLK
LOAD ADDR DATA
START MUX-A/D SEQUENCER
DATA SET LOGIC DIAGRAM
MI (MODEL D)
NATIONAL RADIO ASTRONOMY OBSERVATORY
SIGNAL PREFIX: D



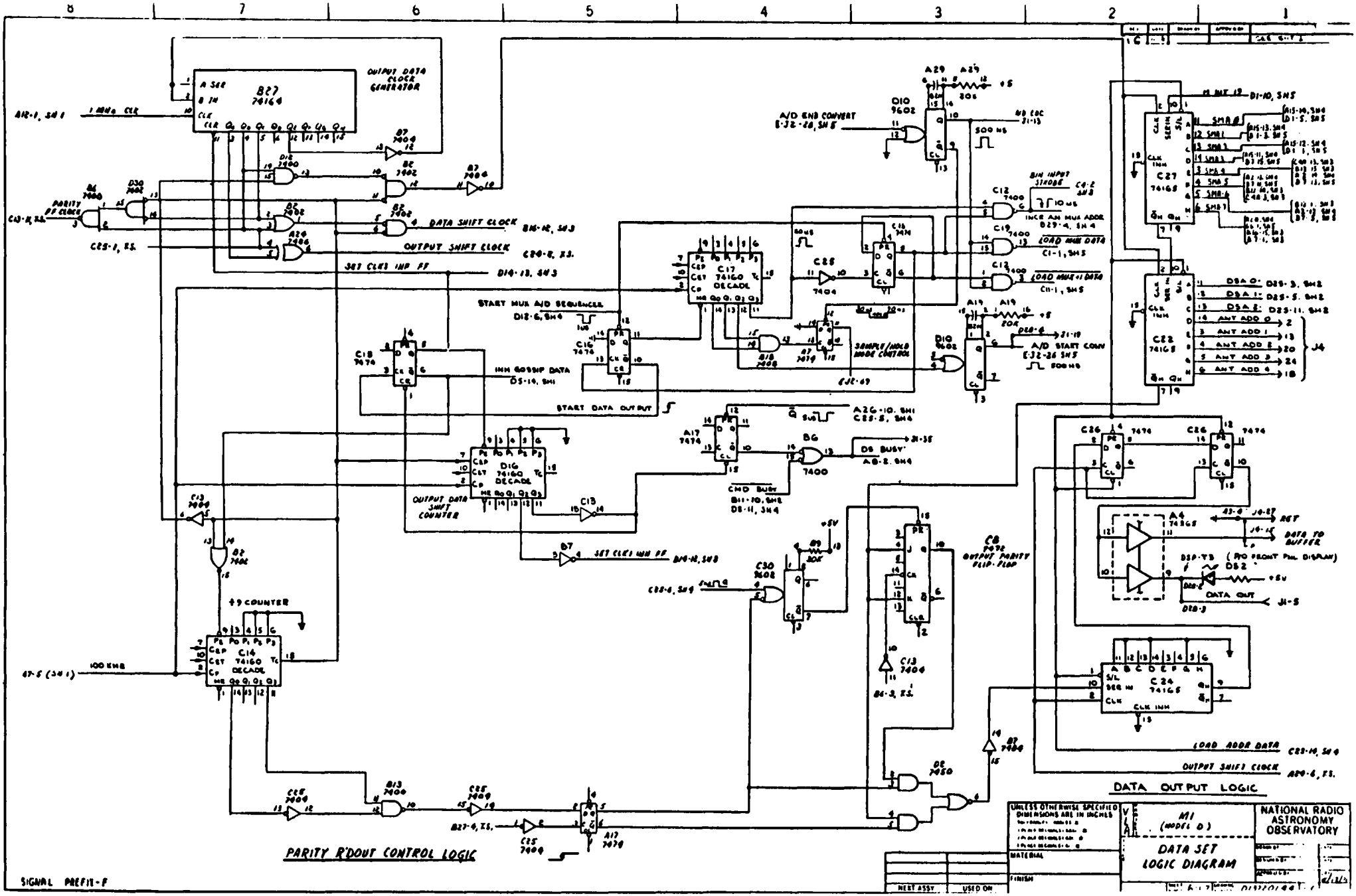
LOGIC DIAGRAM FOR
A TO D PC BOARD
C13721P41 ONLY.

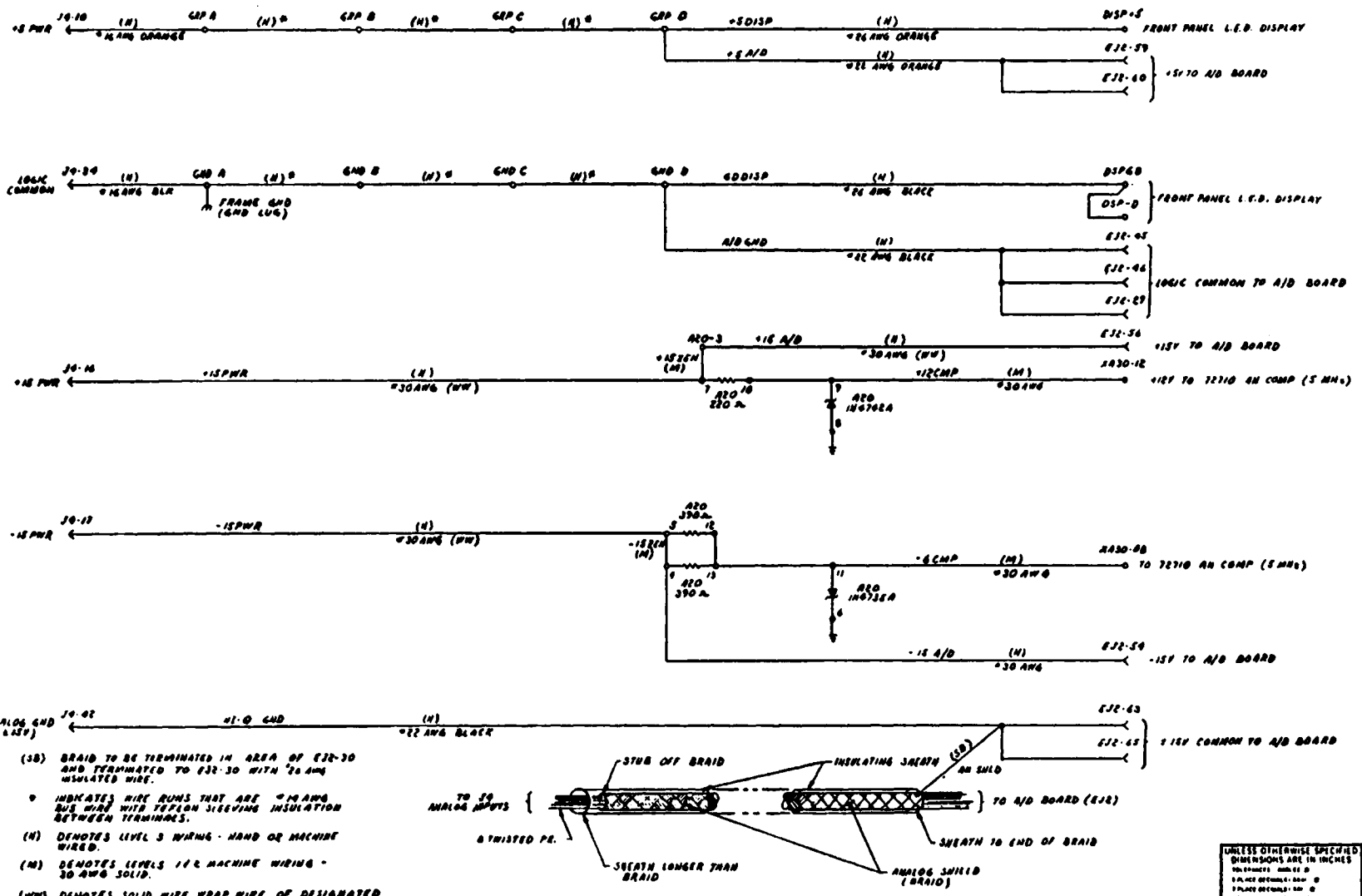
© CUT GND PLANE ARTWORK FOR 7A PINS C8-8 & C6-8

M1
(MODEL 0)

DATA SET
LOGIC DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY


OUTPUT DATA CLOCK GENERATOR
B27 74164
1 MHz CLK
DATA SHIFT CLOCK
OUTPUT SHIFT CLOCK
SET CLK1 INH FF
START MUX A/D SEQUENCER
START DATA OUTPUT
INH GOSSIP DATA
OUTPUT DATA SHIFT COUNTER
÷9 COUNTER
100 KHz
PARITY R'DOUT CONTROL LOGIC
A/D END CONVERT
500 NS
SAMPLE/HOLD MODE CONTROL
A/D START CONV
DS BUSY
CMD BUSY
OUTPUT PARITY FLIP-FLOP
DATA OUT
LOAD ADDR DATA
OUTPUT SHIFT CLOCK
DATA OUTPUT LOGIC
M1 (MODEL D)
DATA SET LOGIC DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY
SIGNAL PREFIX - F



(SB) BRAID TO BE TERMINATED IN AREA OF EJ2-30 AND TERMINATED TO EJ2-30 WITH #26 AWG INSULATED WIRE.

* INDICATES WIRE RUNS THAT ARE #16 AWG BUS WIRE WITH TEFLON SLEEVING INSULATION BETWEEN TERMINALS.

(H) DENOTES LEVEL 3 WIRING - HAND OR MACHINE WIRED.

(M) DENOTES LEVELS 1 & 2 MACHINE WIRING - 30 AWG SOLID.

(WW) DENOTES SOLID WIRE WRAP WIRE OF DESIGNATED SIZE.

ANALOG INPUT HARNESS

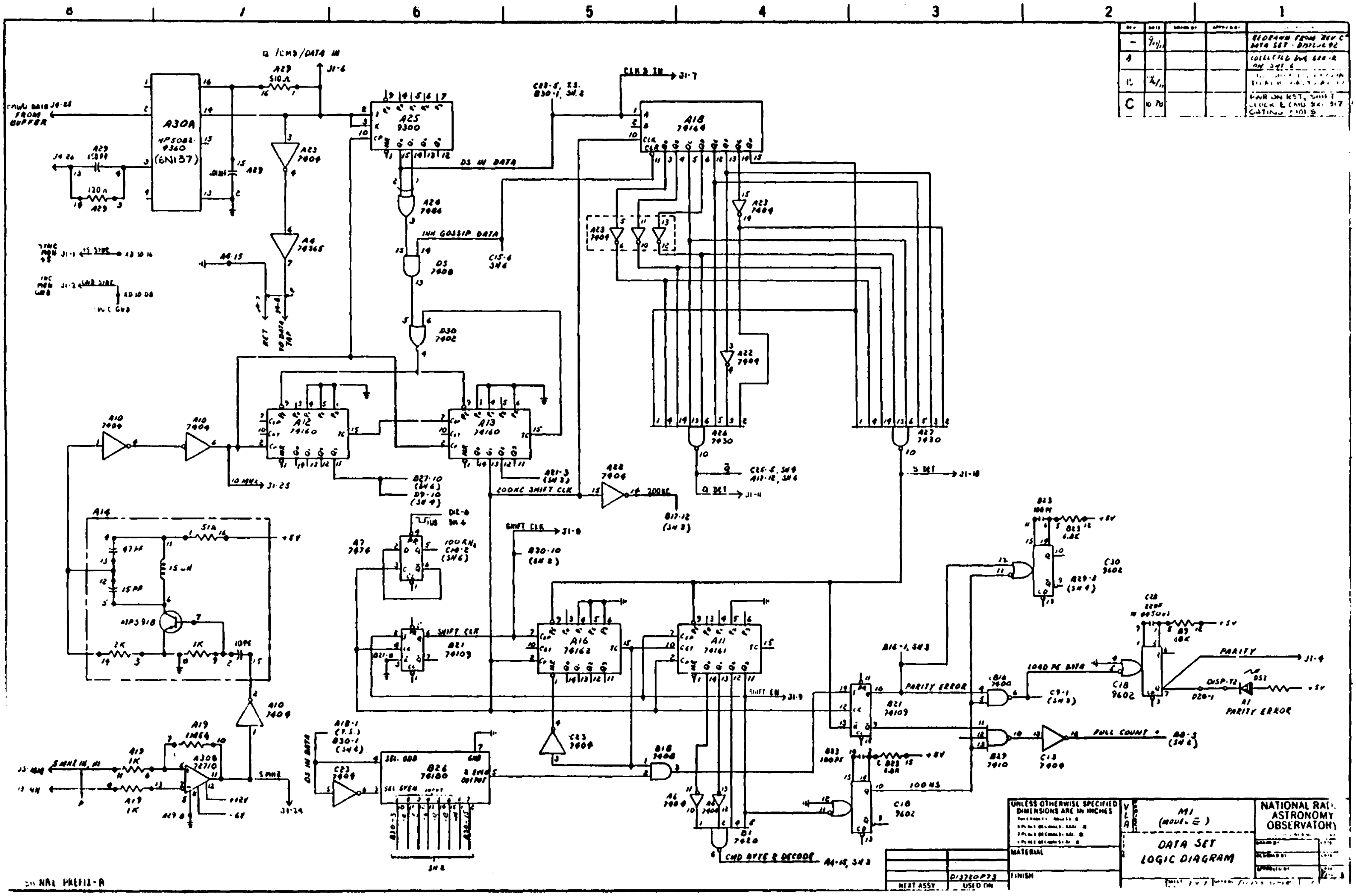
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL

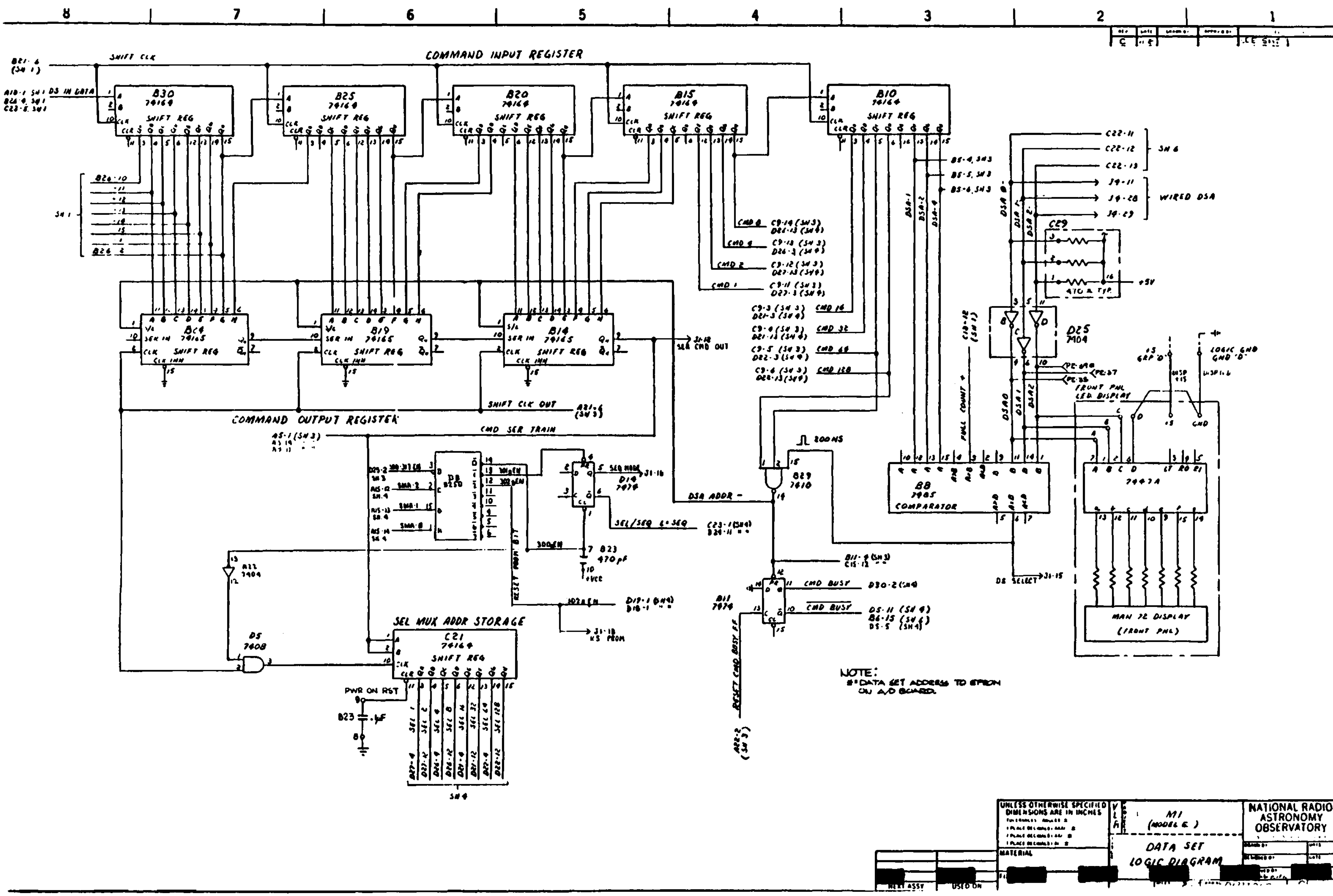
M1 (MODEL B)

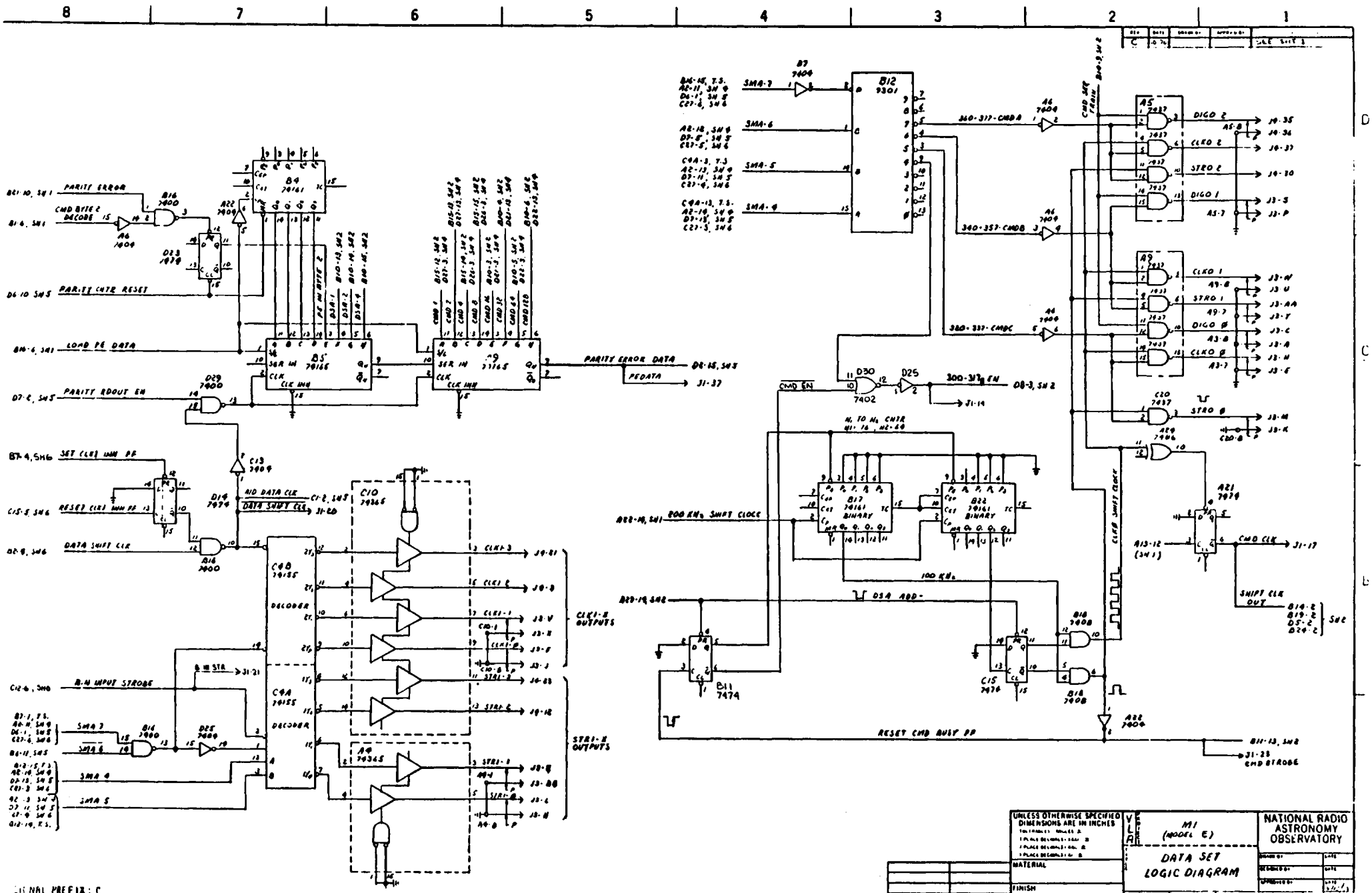
DATA SET LOGIC DIAGRAM

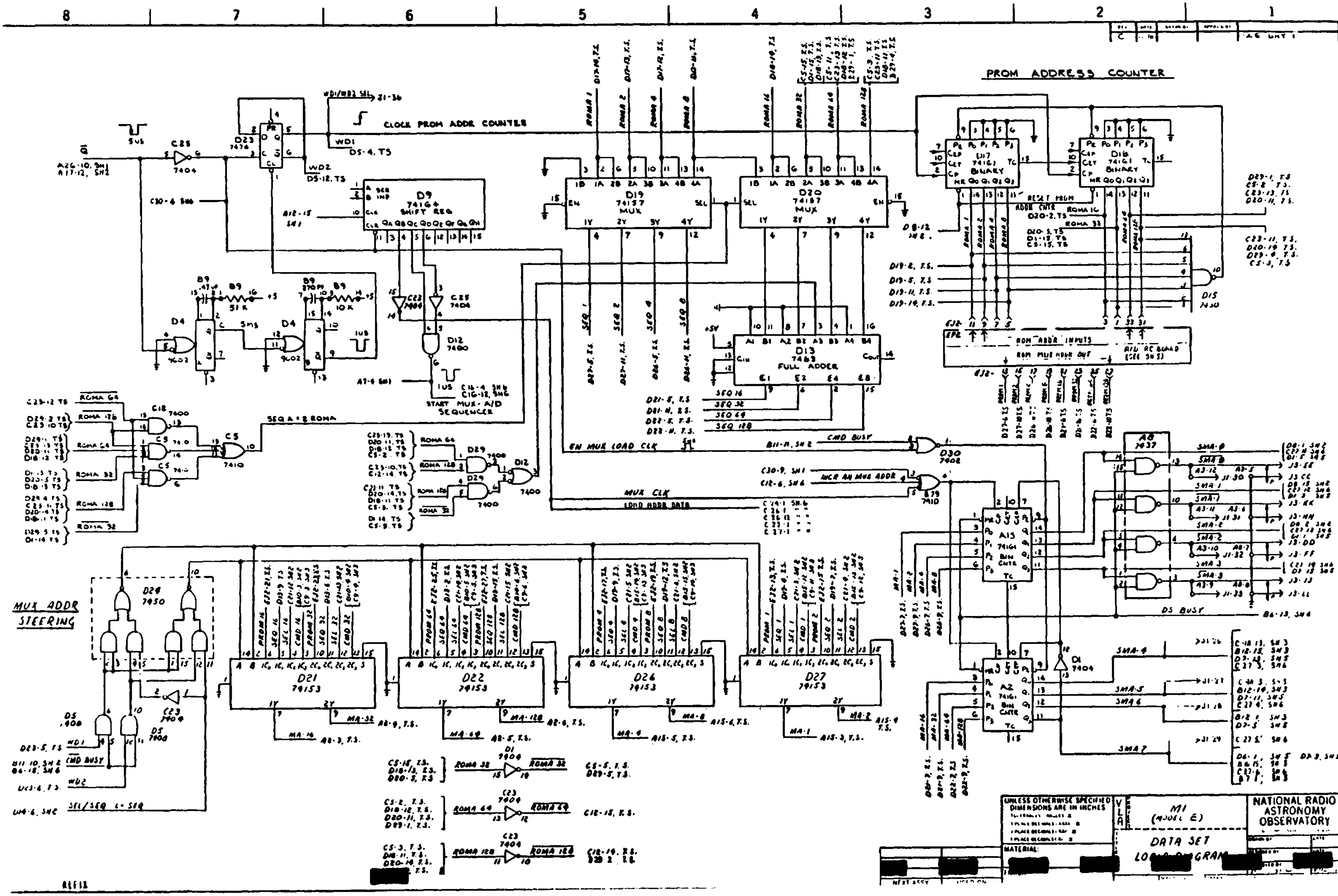
NATIONAL RADIO ASTRONOMY OBSERVATORY

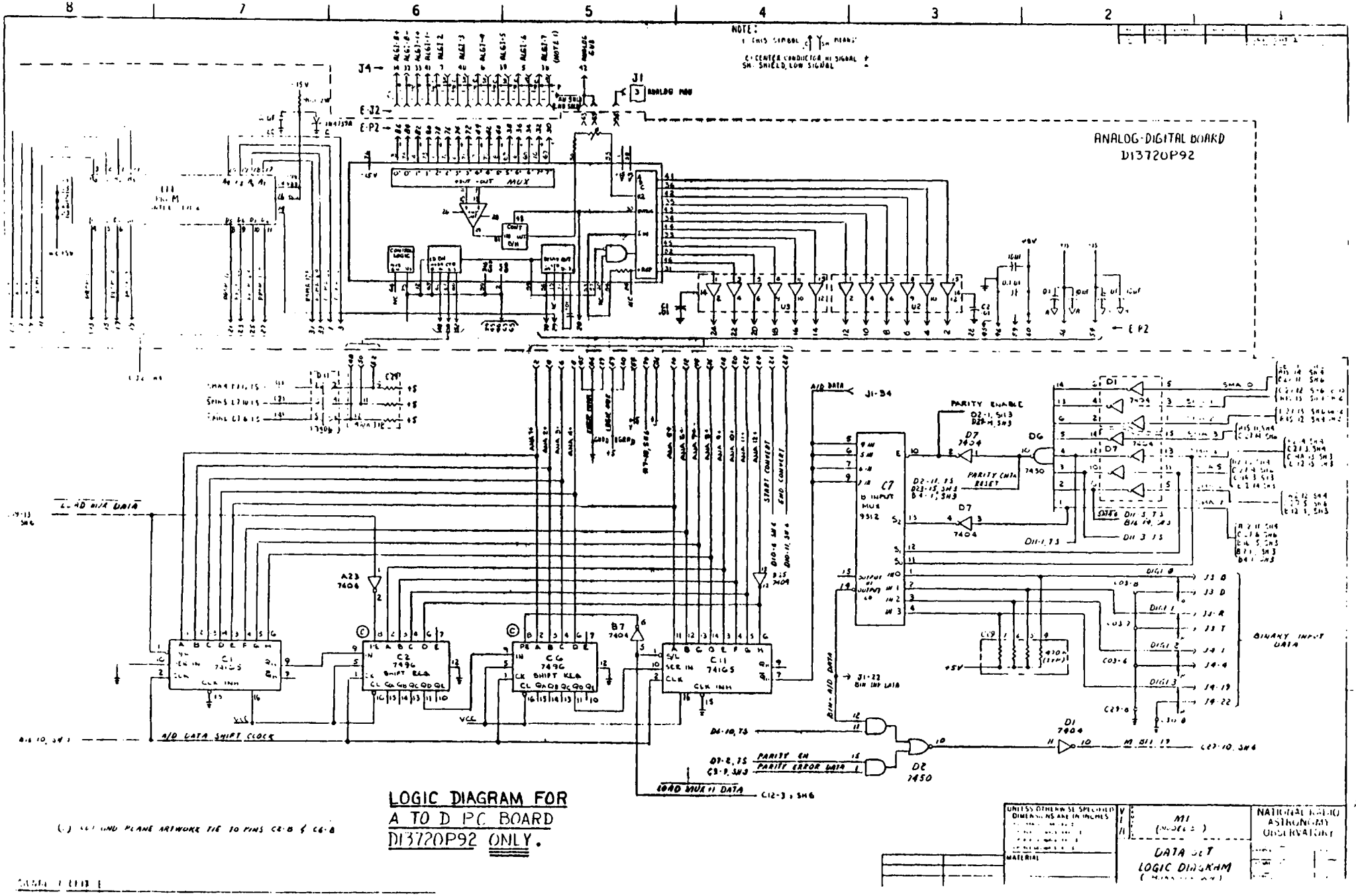


A30A
HP5082-4360
(6N137)
A25
9300
A18
74164
A24
7486
D5
7408
D30
7402
A12
74160
A13
74160
A16
74163
A11
74161
B26
74150
A26
7430
A27
7430
B21
74109
C18
9602
C30
9602
A14
MPS918
A19
72710
DS IN DATA
INH GOSSIP DATA
CLK B IN
200KC SHIFT CLK
SHIFT CLK
10 MHZ
Q DET
S DET
5 MHZ
PARITY ERROR
PARITY
FULL COUNT
LOAD PE DATA
CMD BYTE & DECODE
A1
PARITY ERROR
SIGNAL PREFIX-A
DATA SET
LOGIC DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY
NEXT ASSY
USED ON
MATERIAL
FINISH


COMMAND INPUT REGISTER
SHIFT CLK
DS IN DATA
B30
74164
SHIFT REG
B25
74164
SHIFT REG
B20
74164
SHIFT REG
B15
74164
SHIFT REG
B10
74164
SHIFT REG
SH 1
BC4
74165
SHIFT REG
B19
74165
SHIFT REG
B14
74165
SHIFT REG
SER CMD OUT
COMMAND OUTPUT REGISTER
SHIFT CLK OUT
CMD SER TRAIN
CMD 8
CMD 4
CMD 2
CMD 1
CMD 16
CMD 32
CMD 64
CMD 128
SH 6
WIRED DSA
C29
+5V
D25
7404
FRONT PNL
LED DISPLAY
LOGIC GND
DSA ADDR
200NS
B29
7410
B8
7485
COMPARATOR
7447A
MAN 72 DISPLAY
(FRONT PNL)
DS SELECT
B11
7474
CMD BUSY
RESET CMD BUSY F.F.
D14
7474
SEQ MODE
SEL/SEQ L=SEQ
B23
470 pF
D8
8250
RESET PROM BIT
KS PROM
A22
7404
D5
7408
SEL MUX ADDR STORAGE
C21
74164
SHIFT REG
PWR ON RST
B23
SH 4
NOTE:
*DATA SET ADDRESS TO EPROM ON A/D BOARD.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL
NEXT ASSY
USED ON
M1
(MODEL C)
DATA SET
LOGIC DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY


8
7
6
5
4
3
2
1
PARITY ERROR
CMD BYTE 2 DECODE IS
PARITY CNTR RESET
LOAD PE DATA
PARITY READOUT EN
PARITY ERROR DATA
PEDATA
SET CLK1 INH FF
RESET CLK1 INH FF
A/D DATA CLK
DATA SHIFT CLK
DATA SHIFT CLK
R-N INPUT STROBE
SMA 4
SMA 5
CLK1-8 OUTPUTS
STR1-8 OUTPUTS
DECODER
SMA-7
SMA-6
SMA-5
SMA-4
CMD SET TRAIN
CMD EN
N1 TO N4 CNTR
200 KH2 SHIFT CLOCK
100 KH2
RESET CMD BUSY FF
CMD CLK
SHIFT CLK OUT
CMD STROBE
DIGO 2
CLKO 2
STRO 2
DIGO 1
CLKO 1
STRO 1
DIGO B
CLKO B
STRO B
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL
FINISH
M1 (MODEL E)
DATA SET LOGIC DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY

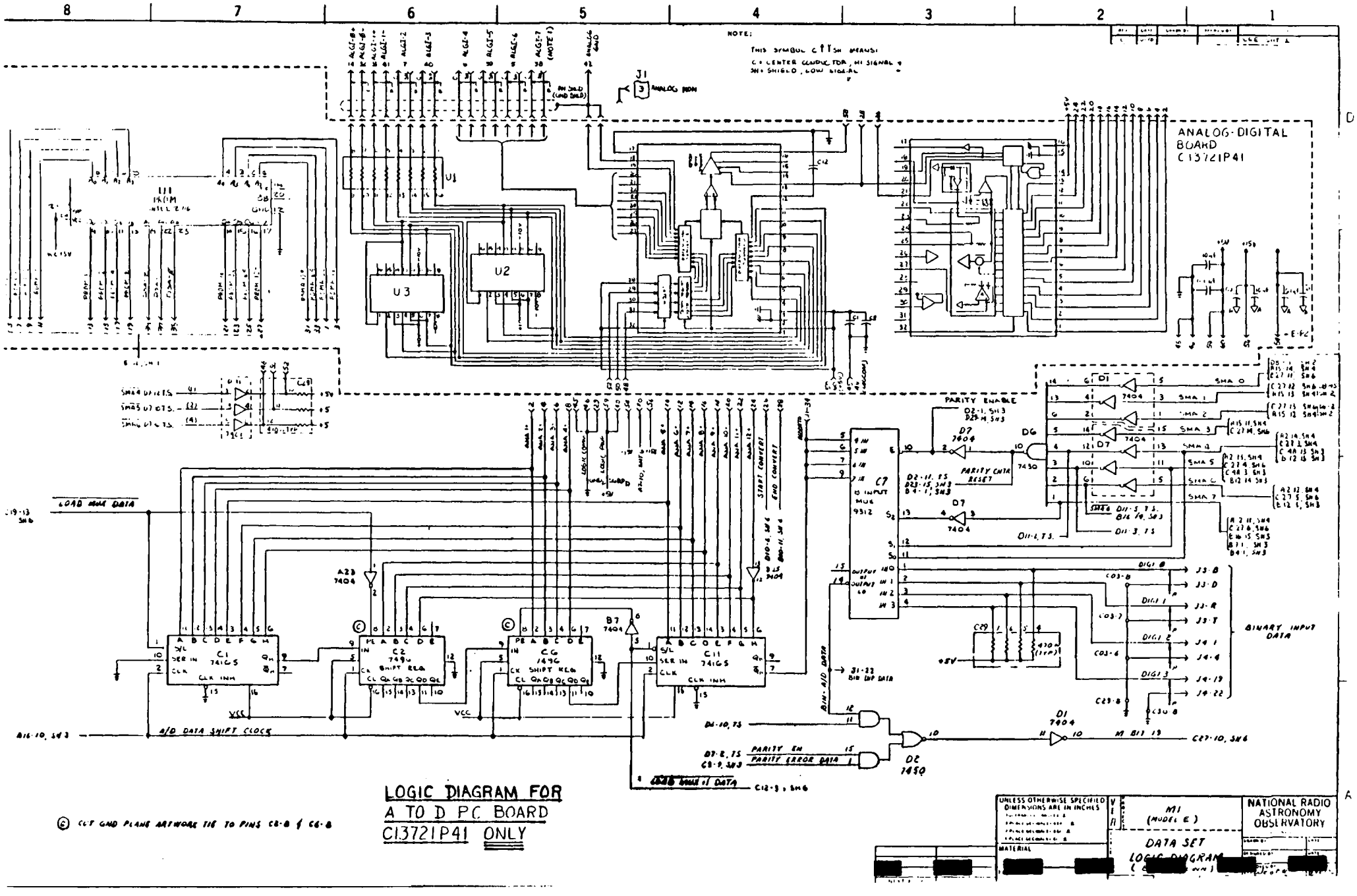

PROM ADDRESS COUNTER
CLOCK PROM ADDR COUNTER
START MUX-A/D SEQUENCER
FULL ADDER
SHIFT REG
MUX ADDR STEERING
EN MUX LOAD CLK
MUX CLK
LOAD ADDR DATA
CMD BUSY
INCR AN MUX ADDR
DS BUSY
SEQ A + B ROMA
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL:
VLA
M1 (MODEL E)
DATA SET
NATIONAL RADIO ASTRONOMY OBSERVATORY
[redacted]

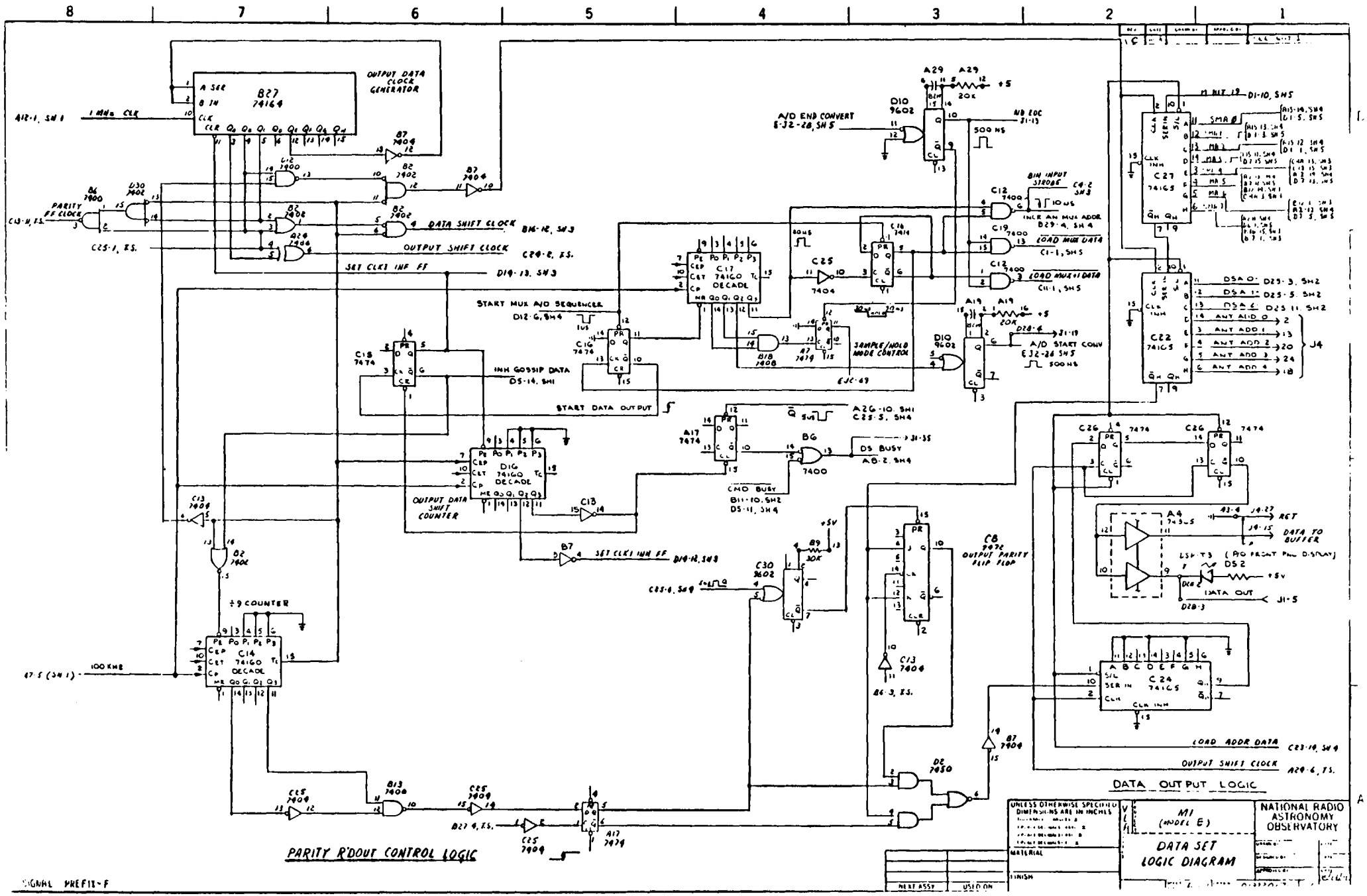


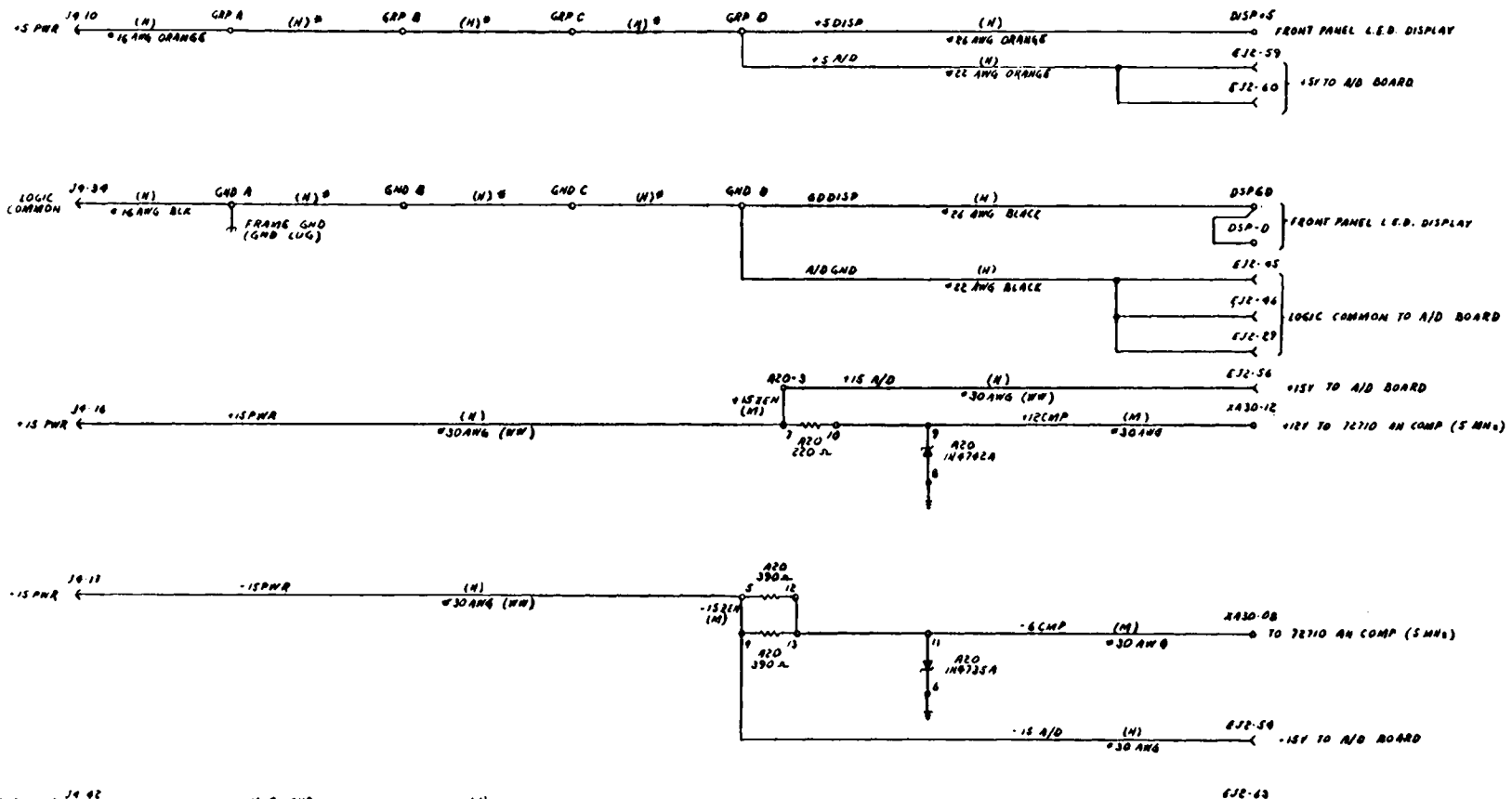
LOGIC DIAGRAM FOR
A TO D PC BOARD
D13720P92 ONLY.

(*) GROUND PLANE ARTWORK TIE TO PINS C6-8 & C6-8

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	M1 (MODEL)	NATIONAL RADIO ASTRONOMY OBSERVATORY
MATERIAL	DATA SET LOGIC DIAGRAM	


8
7
6
5
4
3
2
1
NOTE:
THIS SYMBOL ⊂ ⊤ ⊤ SH MEANS:
C = CENTER CONDUCTOR, HI SIGNAL
SH = SHIELD, LOW SIGNAL
J1
ANALOG IN
ANALOG-DIGITAL
BOARD
C13721P41
U1
U2
U3
PARITY ENABLE
D2-1, SH3
D23-M, SH3
PARITY CNTR RESET
LOAD MUX DATA
A/D DATA SHIFT CLOCK
START CONVERT
END CONVERT
BIN A/D DATA
31-22 BIN INP DATA
BINARY INPUT DATA
PARITY EN
PARITY ERROR DATA
M BIT 19
LOGIC DIAGRAM FOR
A TO D P.C. BOARD
C13721P41 ONLY
© CUT GND PLANE ARTWORK TIE TO PINS C8-8 & C6-8
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL
M1
(MODEL E)
DATA SET
LOGIC DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY


OUTPUT DATA CLOCK GENERATOR
1 MHz CLK
DATA SHIFT CLOCK
OUTPUT SHIFT CLOCK
SET CLK1 INH FF
START MUX A/D SEQUENCER
INH GOSSIP DATA
START DATA OUTPUT
SAMPLE/HOLD MODE CONTROL
A/D END CONVERT
A/D START CONV
DS BUSY
CMD BUSY
OUTPUT DATA SHIFT COUNTER
÷9 COUNTER
100 KHz
PARITY R'DOUT CONTROL LOGIC
OUTPUT PARITY FLIP FLOP
DATA TO BUFFER
LOAD ADDR DATA
OUTPUT SHIFT CLOCK
DATA OUT
DATA OUTPUT LOGIC
M1 (MODEL E)
DATA SET LOGIC DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY



(SB) BRAID TO BE TERMINATED IN AREA OF EJ2-30 AND TERMINATED TO EJ2-30 WITH #26 AWG INSULATED WIRE.

9 INDICATES WIRE RUNS THAT ARE #19 AWG BUS WIRE WITH TEFLON SLEEVING INSULATION BETWEEN TERMINALS.

(H) DENOTES LEVEL 3 WIRING - HAND OR MACHINE WIRED.

(M) DENOTES LEVEL 3 OR 4 MACHINE WIRING - 30 AWG SOLID.

(WW) DENOTES SOLID WIRE WRAP WIRE OF DESIGNATED SIZE.

ANALOG INPUT HARNESS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL [redacted]

FINISH

VLA

M1 (MODEL E)

DATA SET LOG[redacted]GRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY

NOTES:

1. MARKING SHALL BE 1/8" HIGH, LEGIBLE AND PERMANENT. LOCATE APPROX. AS SHOWN.
2. A WIRING SERVICE LOOP OF SUFFICIENT LENGTH TO ALLOW THE FAINT (REAR) PANELS TO BE FOLDED FLAT MUST BE PROVIDED (SEE MIB-SK-66)
3. THE ANALOG INPUT HARNESS (USE ITEMS 54, 55 PER WE 40 DWG DISPLACED SHT 2) IS TO BE ROUTED ALONG THE LOWER RAIL (ITEM 15) AND ALL OTHER I.D. WIRING IS TO BE ROUTED ALONG THE UPPER RAIL (ITEM 14).
4. WHERE TWO WASHERS (ITEM 68) ARE REQ'D, PLACE ONE UNDER THE SCREW HEAD AND THE OTHER BETWEEN THE GUIDE (ITEM 13) AND THE REAR PANEL (ITEM 15)
5. THE TERMINALS ON THE REAR OF THE I.C.D. DISPLAY SUB-ASSY (ITEM 10) ARE TO BE SHORTENED AS REQ'D IN ORDER TO PREVENT INTERFERANCE WITH THE A-D CONVERTER PC B ASSY (ITEM 8)
6. THE "DISP" DESIGNATIONS ARE GIVEN FOR WIRING ORIENTATION ONLY AND ARE NOT TO BE MARKED.
7. LEADS TERMINATING AT POS. 10, 39 & 92 USE ITEM NO. 37
   LEADS TERMINATING AT POS. 16 & 17 USE ITEM NO. 38
   LEADS TERMINATING AT POS. 5, 6, 7, 38, 39 & 90 USE ITEM NOS 38, 90 & 91.
8. SOLDER "SOLDER LUG" (ITEM NO. 50) TO GND PLANE AND PLACE UNDER SCREW HEAD APROX AS SHOWN.

NOTES: (CONT'D)

9. SOLDER GND TERMINAL (ITEM 98) TO GROUND PLANE (COMPONENT SIDE OF I.C. MODULE PANEL - ITEM 9).
10. SOLDER PWR TERMINAL (ITEM 97) TO PWR PLANE (WIRE WRAP TERM. SIDE OF I.C. MODULE PANEL - ITEM 9).
11. THE PWR / GND BUS WIRING SHALL BE ON THE WIRE-WRAP TERM. SIDE OF I.C. MODULE PANEL - ITEM 9.
12. THE "KAPTON TAPE" (ITEM 56) SHALL RUN THE FULL LENGTH OF THE RAILS (ITEMS 14 & 15)
13. CEMENT ITEM 23 TO ITEM 18 USING A CONTACT TYPE OF CEMENT AND INSTALL AS SHOWN IN SECT B-B.
14. BEVEL CORNER OF NYLON SPACER ENOUGH TO CLEAR WIRE WRAP TERMINAL OF CIRCUIT BOARD. (ITEM 10).

-				REDRAWN FROM ECO A DATA SET D1372 JP5A
A	4/4/			ADDED NOTE #13 TO FIG E. ACCOMPANIED VARIOUS MINOR CHANGES.

FIG E

FIG A
PICTORIAL VIEW OF PWR-GRD BUS (UNDERSIDE OF I.C. MOD SUB-ASSY - ITEM 9)

SECT B-B

VIEW C-C

SECT D-D

BILL OF MATERIALS A13720299

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL

FINISH

NEXT ASSY | USED ON

VLA

MI (MODEL 0)

DATA SET MODULE

NATIONAL RADIO ASTRONOMY OBSERVATORY

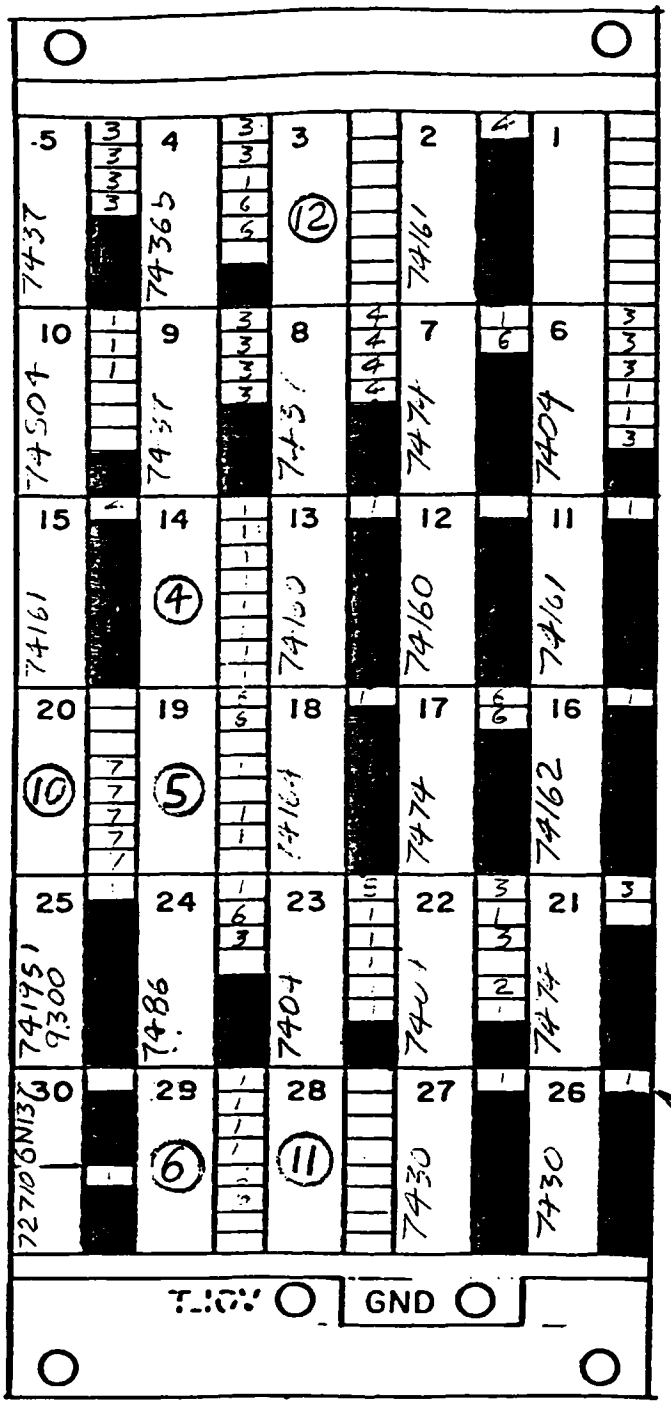
DRAWN 9/3/74

CHECKED

APPROVED 9/3/74

D13720021 A

LOC A



NUMBER IN THIS LOCATION REPRESENTS SHEET NUMBER OF LOGIC DIAGRAM, TYP.

SPECIAL SUB ASSY'S

ITEM	BOM #	DWG #
4	A13720Z39	B13720P6
5	A13720Z86	A13720P59
10	A13720Z90	A13720P63
6	A13720Z8	B13720P17
12	A13720Z10	B13720P14
11	A13720Z9	B13720P16

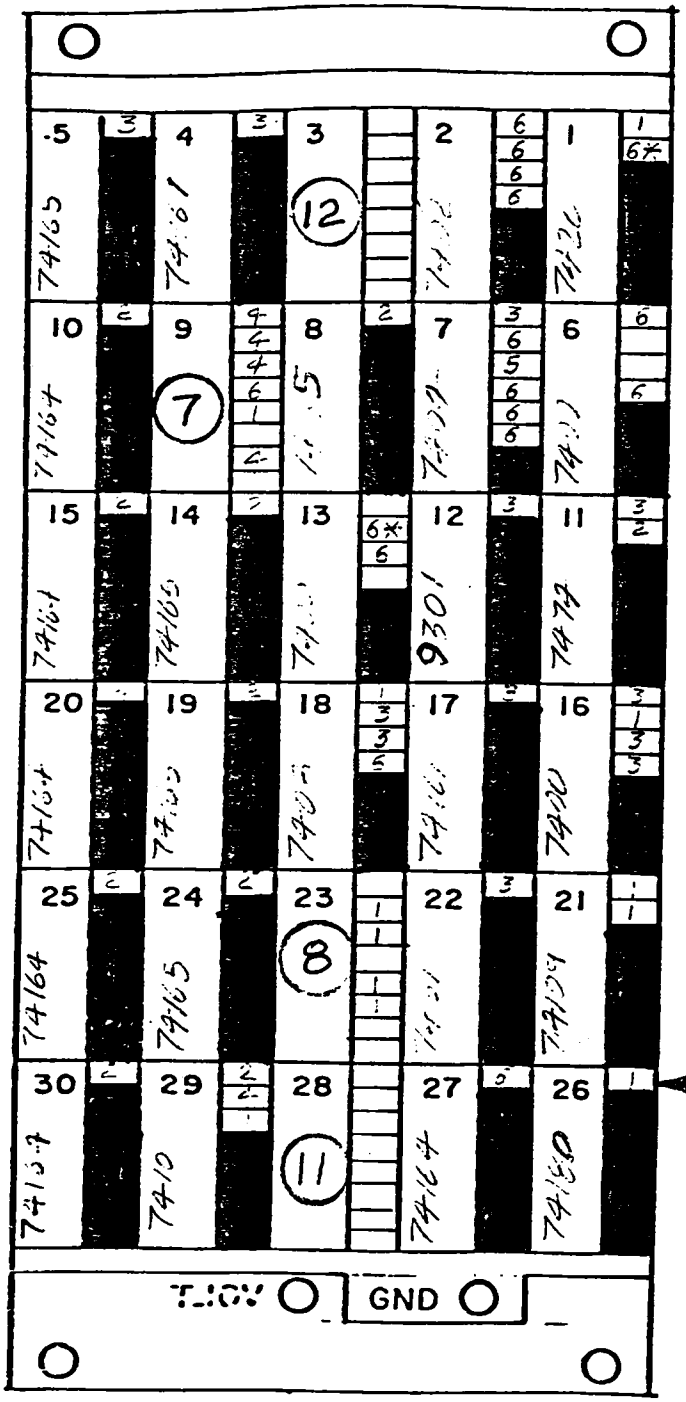
BILL OF MATERIALS: MODEL C : A13720Z84
MODEL D : A13720Z99

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLA

PROJECT M1
TITLE I.C. MODULE PANEL
DATA SET MODEL C+D
DWG NO. A13720P57 SHEET 2 OF 5

LOC B



SPECIAL SUB ASSY'S

ITEM	BOM #	DWG #
12	A13720Z10	B13720P14
7	A13720Z87	B13720P60
8	A13720Z88	B13720P61
11	A13720Z9	B13720P16

* MAY OR MAY NOT BE USED, DEPENDING UPON MODIFICATION LEVEL

NUMBER IN THIS LOCATION REPRESENTS SHEET NUMBER OF LOGIC DIAGRAM, TYP.

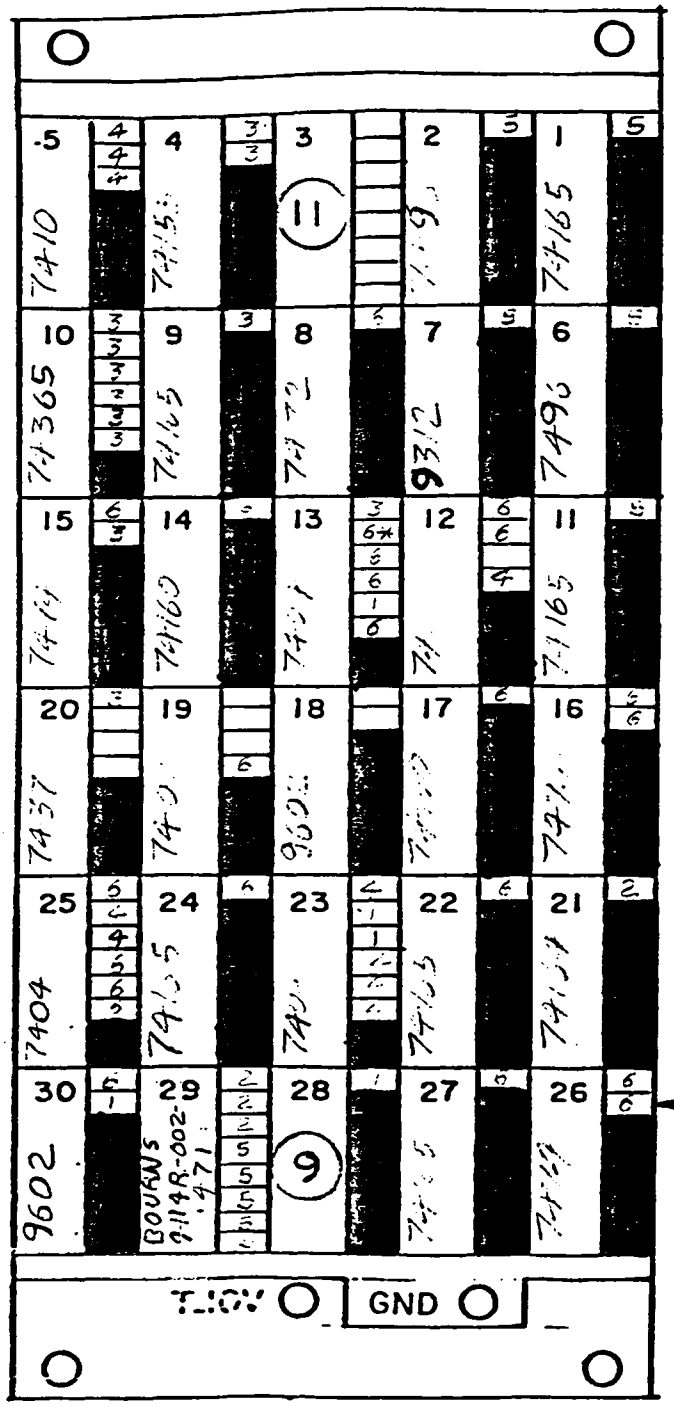
BILL OF MATERIALS: MODEL C : A13720E84
MODEL D : A13720Z99

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLA

PROJECT M1
TITLE I.C. MODULE PANEL
DATA SET MODEL C+D
DWG NO. A13720P57 SHEET 3 OF 5

LOC C



SPECIAL SUB ASSY'S

ITEM	BOM #	DWG #
11	A1372039	B1372CP16
9	A1372059	A1372CP62

*MAY OR MAY NOT BE USED, DEPENDING UPON MODIFICATION LEVEL.

NUMBER IN THIS LOCATION REPRESENTS SHEET NUMBER OF LOGIC DIAGRAM

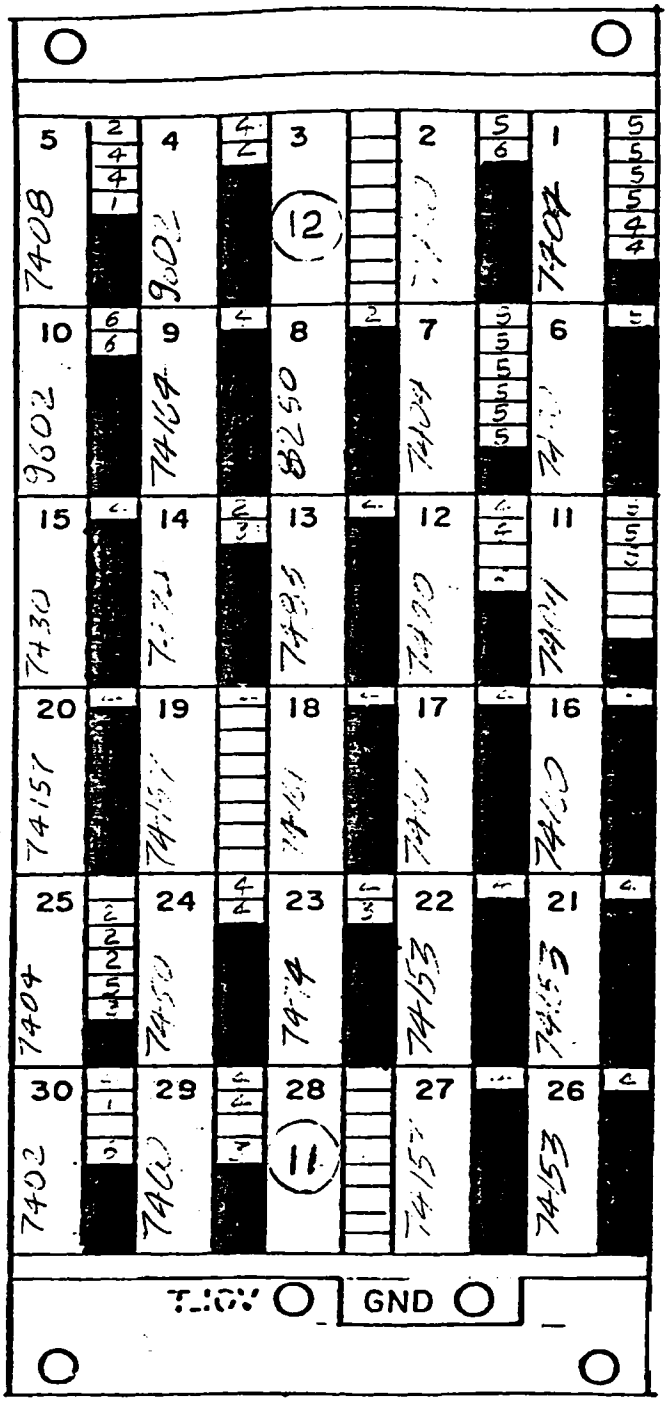
BILL OF MATERIALS: MODEL C : A1372084
MODEL D : A1372099

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLA

PROJECT M1
TITLE I.C. MODULE PANEL
DATA SET MODEL C+D
DWG NO. A1372CP57 SHEET 4 OF 5

LOC D



SPECIAL SUB ASSY'S

ITEM	BOM #	DWG #
12	A13720Z10	B13720P14
11	A13720Z9	B13720P16

BILL OF MATERIALS: MODEL C : A13720E84
MODEL D : A13720Z99

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLA

PROJECT M1
TITLE I.C. MODULE PANEL
DATA SET MODEL C+D
DWG NO. A13720P57 SHEET 5 OF 5