VLA Technical Report No 59

The Antenna Buffer, Module type M4

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List of Illustrations and Major Drawings

1.0 INTRODUCTION

This manual describes the operation of the Antenna Buffer (AB), module type M4, and was written to serve as a trouble-shooting and maintainance guide for this component of the VLA Monitor and Control (M&C) System. The manual describes both the D and E Models of the Antenna Buffer; the D models will be modified to E Models to minimize the RFI effects of coherent harmonics of the digital clocks.

This manual does not address the signal transmission properties of the LO/WG Transmission systems which are in effect the "wire" used by the M&C system for antenna - central message communications; the subject of the transmission characteristics is too extensive to be addressed in this manual but important aspects of these characteristics are discussed where it seems appropriate to do so. Timing discretes inputs from L8 and L8 timing "jitter" are discussed.

To put the operation of the AB into the system context, the reader is referred to the manual: "An Overview of the Monitor and Control System", Electronics Memorandum No 44. "The Handyman's Guide to the Data Set", Electronics Memorandum No 30 provides a detailed description of the AB/Data Set interactions. Figure 1 depicts the Monitor and Control System and the relationships of the Antenna Buffer to the balance of the system. Figures 2 and 3 depict the M&C timing relationships which are discussed below.

The emphasis is upon the detailed functional operation; the writer's intent is to provide a thorough description of the Antenna Buffer's theory of operation. Straight-forward portions of the logic are treated briefly; more complex areas (and there are several) are fully explained and the explanations are augmented by timing diagrams. Using this manual as a reference, a digital maintainance technician should be able to quickly identify and repair malfunctions.

The logic descriptions are based upon two contrasting perspectives: 1) operations as a function of time (which is the driving parameter in the VLA Electronics); 2) command and monitor data message transmission operations, - the primary functions performed by this module.

2.0 ANTENNA BUFFER DESCRIPTION

The primary function of the Antenna Buffer is command/data message distribution; the AB detects bit-serial digital command messages from the Central Buffer (CB) for distribution to the antenna Data Sets and polls the antenna Data Sets for Monitor Data messages which are transmitted to the Central Buffer. All M&C messages exchanged between the Antenna Buffer and the Central Buffer are routed through the LO/WG Transmission systems.
The Antenna and Central Buffers form a complementary pair of M&C message handlers on either end of the LO/WG Transmission systems.

The AB must be able to distribute up to 4 antenna command messages

and gather 10 monitor data messages/VLA machine cycle.

For the Antenna/Central Buffer combination, command messages extracted from the control computers in one VLA machine cycle are delivered to the controlled devices in the next cycle. The response of the controlled device to the command may be monitored in the cycle in which the device received the command but it is input to the control computers in the next cycle; therefore the earliest possible monitored response to a command is input to the computers two VLA machine cycles after the computer output the command to the M&C System.

Figures 5 and 6 depict the Antenna Buffer logic flow and logic block diagram.

The Antenna Buffer is packaged in a standard VLA module and contains wire-wrapped logic connector boards for the digital logic. A front panel numeric LED display indicates the DCS address and flashing discrete LEDs indicate command and monitor data message flow. A front panel test point connector permits observation of important logic signals for diagnostic purposes. DC power regulators on the rear panel provide special voltages required by certain logic chips. The Top Assembly, BOM and IC location drawings are included in this manual for reference.

2.1 MESSAGE FORMAT DESCRIPTION

Figure 4 depicts the format of the Command and Monitor Data messages and the "Q" character format. All M&C messages are prefixed by an "S" (for start) character which signals that a message immediately follows. The bit rate of the S character is twice the bit rate of the data bits to make this character unique. The message consists of five 8-bit data bytes; the first byte contains a 5 bit DCS Address (which can range from 0 to 31) and a 3-Bit Data Set Address (DSA) which can range from 0 to 7. The second byte is the Multiplex Address which designates a particular command or data channel. The third, fourth and fifth bytes are components of a 24 bit command or monitor data argument. In the case of an analog data message, the 24 bit argument consists of two 12 bit values resulting from the conversion of two analog signals by the Data Set analog-to-digital converter. In all address and argument values, the first bit (in time) is the most significant bit.

The M&C messages transmitted through the LO/WG Transmission system have a different format than the simple NRZ described above; the bit sense is conveyed by the phase of a 500 Khz phase-modulated carrier. The form of modulation is called BI-Ø-1 (L for level, also called Manchester encoding); a modulator in the output circuitry of the Antenna and Central Buffers inverts the phase of the 500 Khz carrier for each NRZ data one bit; a zero bit does not change the phase. This encoding scheme provides a signal edge in every bit space, a very desireable property for situations in which receiving logic must derive a clock from the structure of time-serial digital messages. This BI-Ø modulation requires some additional circuitry in the receiving buffer

to reconstitute the NRZ format. The BI-Ø antenna command messages from the CB to AB have a higher data bit rate than the BI-Ø antenna monitor data messages from the AB to the CB. The details of these formats are discussed below.

BI-Ø modulation of the NRZ data stream eliminates the DC term and all frequency components below 500 Khz from the message signal spectrums; a necessary measure since the outputs of the LO Receivers are AC-coupled. A second, very important reason for the use of BI-Ø modulation is that the LO System 1800 Mhz carrier spectrum must not have any low frequency modulation components since they can perturb the operation of the stable frequency references in the LO System.

The "Q" (for Query) character is used by the CB and AB to poll data from a Data Set and is directed to one Data Set at a time via the buffer's Data Set Command Ports. The SLC uses the "Q" character to poll data from the Central Buffers via the CB Command Ports. The bit rate of the Q character is 5 usec/bit, the same as the bit rate of the S character in the Data Set command/monitor data messages.

2.2 ANTENNA BUFFER I/O SIGNALS

- QQ pulse, - a 400 ns differential TTL level signal from L8 which signals the start of the 1000 usec period in which command messages are transmitted from the Central Buffer via the Central LO/WG Transmission systems.

- 5 Mhz clock output- a digital TTL level clock generated by the AB to clock the AB and Data Set logic.

- Antenna Command Signal Input - a 750 millivolt peak (nominal), bipolar analog BI-Ø format signal from the Antenna LO Receiver, L4. The S character and data bit rates are 2 usec/bit (1 BI-Ø cycle) and 4 usec/bit (2 BI-Ø cycles), respectively.

- Antenna Monitor Data Output, - a TTL level, BI-O format signal to the Antenna LO Transmitter, L3. The S character and data bit rates are 20 usec/bit (10 BI-Ø cycles) and 40 usec/bit (20 BI-Ø cycles) respectively.

- Data Set Command Ports, - five TTL level, NRZ format, low-true line driver outputs which drive the Command Inputs of the associated Data Sets. The S character and data bit rates are 5 usec/bit and 10 usec/bit respectively.

- Data Set Monitor Data Ports, - five TTL level optical isolator/multiplexer input ports which receive low-true, NRZ format monitor data inputs from the Data Sets. The S character and data bit rates are 5 usec and 10 usec respectively.

2.3 TIME-DRIVEN ANTENNA BUFFER OPERATIONS

The operations performed by the Antenna Buffer are time-directed in that functions are enabled, initiated and terminated by control discretes derived from the internal time base; these discretes regulate the message flow between the antenna and the central electronics to insure that the AB is properly synchronized with the (CB) and the modes of the LO/WG Transmission system. Figure 2 depicts the time-ordered operations performed by the Antenna Buffer. Figure 5 depicts these operations in flow diagram form. Figure 6 depicts the Antenna Buffer Block Diagram.

The AB time base is referenced to the QQ pulse from L8 and timing terms are stated in terms of microseconds of elapsed time from the QQ pulse. The AB time base is triggered into operation by the QQ pulse and is clocked by a 10 Mhz crystal clock in the Model E AB; the Model D uses a 5 Mhz clock provided by L8. If the QQ pulse is missing the AB will remain in the quiescent state.

A 0 to 1000 usec enable permits the AB BI-Ø to NRZ demodulator and command detection circuits to operate during the time that commands are transmitted from the Central Buffer via the Central LO/WG Transmission systems. When a command message is detected, a loading sequence is initiated which causes the command message to be temporarily stored in the serial command message memory. The DCS/DS address byte of the incoming message is analyzed on the fly for parity errors; if found untainted by errors, the DCS address is stored for subsequent use in storing Data Set monitor data messages. If the DCS/DSA address byte is tainted by a parity error, the address is not stored but the message is stored, (Data Sets do not execute an error-tainted message and will report the occurrance). The antenna command messages are separated by 8 BI-Ø spacing bits, but the command memory is loaded with the command message and only 4 of the spacing bits. The command transmission bit rate from the Central Buffer is 4 usec/bit for the message bits and 2 usec/bit for the "S" bits. The BI-Ø clock rate is 500 Khz so that the BI-Ø "S" bit durations are one BI-Ø cycle and the message bit durations are two BI-Ø cycles. The BI-Ø modulator in the Central Buffer is coherent with the message unload clock so that the transmitted BI-Ø command waveform duty cycle is 50%.

During the 1000 - 5000 usec period, the stored NRZ antenna command messages are serially unloaded from the command memory to all the antenna Data Sets via the Data Set Command Ports. Each Data Set analyzes the message stream to determine if it is the target of a command message; if it is, it executes the command. See the Data Set manual for a description of this process.

The Antenna command message stream consists of an 80 usec preamble of BI-Ø zeros and up to four command messages separated by 8 BI-Ø spacing bits. The total period for this message stream is 944 usec (80 usec preamble + 4 x (100 bit messages + 8 spacing bits)) x 2 usec/bit. The stream is emitted by the Central Buffer at t = 0 and approximatly 1016

usec is available for transmission.

At t = 14,700 usec the AB begins to poll the antenna Data Sets for Monitor Data by sequentially emitting "Q" characters on the Data Set Command Ports at 900 usec intervals. The Data Set polling sequence is DS-0 ... DS-4, DS-0 ... DS-4; the first pass through the sequence evokes the MW-1 data and the second pass evokes the MW-2 data. See the Data Set description for the usage of these data values. The AB polling sequence is terminated at t = 23,700 usec. As each Data Set is polled, "Q" detection circuitry in the Data Set initiates a monitor data acquisition sequence so that at t = 250 usec (in the 900 usec polling period) the Data Set begins to emit a monitor data message. The 200 usec delay between the start of the "Q" and the begining of the monitor data message is used by the Data Set for sampling and A/D conversion. The duration of a monitor data message is 500 usec so there is a 150 usec margin in the 900 usec period. Figure 2 depicts the Data Set polling timing.

As each Data Set emits a monitor data message, it is input to the AB via the Data Set Monitor Data ports which consists of an optical isolator and digital multiplexer. The monitor data loading sequence loads an additional 8 spacing bits between monitor data messages. When the monitor data "S" character preamble is detected, a message loading sequence is initiated and the previously stored DCS address is merged into the DCS/DSA byte in the message as it is stored in the serial monitor data memory. Parity is re-formulated over the whole DCS/DS address byte in the process. When the monitor data message stream is detected, it is immediately rebroadcast to all Data Sets via the AB's Data Set Command Ports during the monitor data memory loading sequence. This rebroadcast data is tapped upstream of the DCS address injection logic so that all rebroadcast monitor data has the DCS address of 00. This rebroadcast Monitor Data is sometimes referred to as "gossip data". A Data Tap connected to any Data Set input is able to hear all antenna command and monitor data messages.

At t = 24,000 usec, the AB begins to transmit the 10 monitor data messages stored in the serial monitor data memory to the Central Buffer via the Antenna LO/WG Transmission systems. The messages are serially clocked out at a 40 usec/data bit rate and a 20 usec/"S" bit rate. The data bits control a 500 Khz modulator so that there are 20 and 10 BI-0 cycles for each message and "S" bit respectively. The transmission duration is 12,800 usec for the ten messages, 8 spacing bits/message and an 80 usec preamble so that the data memory has been completely unloaded at t = 36,000. Transmission of dummy bits continues until t = 48,000 at which time the output driver is inhibited. The BI-Ø Monitor Data stream from the AB amplitude modulates an 1800 Mhz carrier in the Antenna LO Transmitter (L3).

One portion of the AB logic labelled "Substitute Data Generator", performs two functions: in the event that a Data Set does not respond to a polling request within 300 usec, the data generator is triggered into a readout cycle to load substitute data into the Monitor Data

memory. The DSA of the non-responsive Data Set, a multiplex address of 205 (octal), and a count of the number of commands detected during the command input phase are injected into the message format. The command count provides a Monitor Data readback of the cycle by cycle count of command messages detected by the Antenna Buffer and may be used to verify command message transmission between the Central and Antenna portions of the M&C system. In the Model D AB this data generator was always connected to the Data Set #4 multiplexer input and the physical Data Set #4 port was disconnected; in the Model E AB, the physical DS #4 port has been reconnected to the multiplexer DS #4 input port. The data generator logic still continues to function as a default psuedo Data Set if one or more of the five Data Sets is non-responsive.

Finally, at t = 51,000 usec the time base is shut down and the AB remains in this quiescent state until stimulated back into operation by the next QQ pulse. There are no provisions for flywheeling of the time base in the Antenna Buffer; the flywheeling function is performed by L8.

The command message handling and monitor data message handling operations are not concurrent; there is plenty of time available for all operations.

ANTENNA ID READOUT -- An independant section of logic is a digital monitor channel (mux 202, octal) which provides a readout of the antenna serial number and command count to Data Set #2. The antenna serial number is hard-wired on the AB I/O connector. The antenna serial number readout is cross-checked for consistency with the DCS address by the control computers

3.0 DETAILED CIRCUIT DESCRIPTION

The logic diagrams of both the Models D and E Antenna Buffers are included for reference in the following discussion.

3.1 TIME BASE

The time base logic provides a series of time-based control discrete terms which regulate all functions of the Antenna Buffer. The time base is quiescent until triggered into operation by the "QQ" pulse from L8 which sets a control flip flop that releases the preset enable on the time base counters to enable the counter operation. A discrete term turns off the control flip flop near the end of the 52,083.3 usec period. The L8 "QQ" pulse is a 400 ns differential signal detected by D2, a 75182 differential receiver which outputs a 400 ns (nominal) low-true pulse on D0206. This pulse sets flip-flop B1311 which lifts the preset enable on the time base dividers B4, B5, B9, B8, C4 and C5 to enable the time base to start counting from a preset count of 0.

In the Model D AB, the time base clock is a 2 Volt P-P, 5 Mhz sine wave clock from L8. In the Model E AB, the clock is derived from a 10

Mhz crystal oscillator which also functions as a clock source for the Vertex Room Data Sets. For this purpose, the 10 Mhz clock is divided by two by B0605 to produce a 5 Mhz clock for the 74128 line driver A2401 which outputs the 5 Mhz to the Data Sets.

In the Model D AB, the 5 Mhz sine wave clock is detected by analog comparator A2411 (on Sheet 4) which senses the 5 Mhz axis crossing (with a little hysteresis). The TTL-compatible output of A2411 drives a Schottky 74S04 (B1702) which "squares" the 5 Mhz clock to drive the B11 harmonic doubler circuit which rings at 10 Mhz. The 5 Mhz drive to the doubler is differentiated by the 10 pf, 1K ohm, (B11) RC circuit so that the MPS 918 transistor has a narrow collector current pulse. The tank is tuned to 10 Mhz and the AC coupled output drives the Schottky 74S04 B1704 which is caused to operate in a linear region by the 2K ohm resistor on the doubler's output. Inverter B1704 and B1706 square the 10 Mhz clock signal which drives the time base and clocks the message edge detection shift registers. **Inverter B1704 must be a 74S04; the high switching speed of the Schottky logic is important to the doubler circuit's operation.**

The reason that 10 Mhz is used as a clock in the Antenna Buffer is that it provides a 100 ns resolution for synchronization to the incoming command 500 Khz BI-Ø format message stream from the CB. The use of a 5 Mhz clock for this purpose would be too granular for this function.

At t = 51,000 usec, gates C1010 and D2210 triggers the 500 ns one-shot B0704 which resets control flip flop B1311. B1311's low true output drives the time base counter pre-set enables so that the counters continue to load a count of zero with the result that the time base (and hence the AB) is quiescent. The time base remains quiescent until stimulated on again by the next QQ pulse. The time base counters B5, B10, B9, B8, C5, and C4 are a string of synchronous counters driven by the 5 Mhz clock A0403.

A series of time discretes are derived from the time base to control the AB operations. These are:

0 to 1000 -- Enable terms 0 to 1000 are generated by two flip-flops C0605 and D1705 (Sheet 2). D1705 controls shift register E26, A1 and A23 (Sheet 1) while C0605 controls gates B1603 and E0714 (Sheet 1) These flip-flops are set by the QQ pulse and edge reset by the rising edge of the first 1-Khz term from counter C0514. Enable 0 to 1000 (CMD aperature) is used in high-true form at shift register E26, A1 and A23 (sheet 1) to enable the Antenna Buffer to "hear" antenna commands from the Central Buffer. This high-true term is also used at gate B1603 (sheet 1) to permit the detected commands to be loaded into the command memory B19. During the time the commands are being unloaded to the Data Sets, the false state of this term causes zero's to be loaded into the command memory. The 0 to 1000 term is also used as an inhibit on the monitor data multiplexer A1515; so that the monitor data circuitry is disabled during command output time. The 0 - 1000 term is also used

as an enable on gate E0714, the DCS address storage logic.

1000 to 5000 -- Enable term 1000 - 5000 is generated by C0611 (sheet 2). Flip flop C0611 is triggered on by the falling edge of the 0 to 1000 enable and turned off by by gate C2503 (sheet 3) which goes true at t = 5000 usec (and periodically thereafter). Enable 1000 - 5000 is used as an enable for the command unload clocks at gate B14 (Sheet 1).

14,700 to 23,700 -- Enable 14,700 - 23,700 is generated by flip flop C1405 which is direct set by gate E0110. Flip-flop C1405 is reset at the completion of the 10'th (last) Data Set polling period. Gate C2510 trailing edge triggers the clock input of flip flop C14. Gate C0910 which goes true at t = 24,000 to direct reset C14 is a functionally redundant vestige of an earlier AB model reset circuit. Enable 14,700 - 23,700 is applied to counters A2 and A8 master resets (sheet 2). When this enable is low, the counters are held in the reset state; when the enable goes high the counters are permitted to operate. The action of this enable is to inhibit the Data Set polling logic and initialize counter A8 (the Data Set port address counter), to port 0 (ie Data Set #0).

Enable 24,000 - 48,000 is generated by flip flop A2211 which is direct set by gate C0910 which goes true at 24,000 usec. Gate C0810 goes true at t = 48,000 usec to direct reset A2211. This 24,000 - 48,000 term is applied to gate D2406 to enable the monitor data unload clocks to push the Monitor Data out of the serial memory into the BI-0 modulator. The low-true form of 24,000 - 48,000 is used to enable the monitor data on gate D2406 (Sheet 5) to enable the monitor data load clocks during the Data Sets polling period. Gate D2506 and inverter C2006 (Sheet 3) combine the time enable and the data load enable which drives the and-or load clock gate D2406 on Sheet 5.

In the antenna, when synchronizing an oscilloscope to the AB logic to the time base or the QQ pulse, you will observe a puzzling 10 usec jitter in the time of arrival of the command messages from the Central buffer; this is an artifact of the L8 Timing Generator which goes through a 3-state periodic variation of the 19.2 Hz period. The L8 logic implementation causes the 3 periods to vary in a sequence which is base, base + 200 ns, base +10 usec. In observing the Antenna Buffer command input logic waveforms in the antenna, the command S detector output is a convenient scope sync point.

3.2 COMMAND SIGNAL DETECTION, STORAGE AND OUTPUT

This is one of the two major functions performed by the Antenna Buffer; most of the VLA command messages are handled by this unit.

COMMAND SIGNAL DETECTION AND NOISE FILTERING -- The command signal from the Antenna LO Receiver (L4) is threshold detected by analog comparator A2911 (sheet 4) which switches high and low at input signals above and below + and - 200 millivolts. Resistor A21-5/12 provides a positive feedback to the comparator + input so that the comparator is caused to

have about a 200 millivolt hysteresis. The typical command signal from L14 is about 1.5 volts P-P. The baseline noise is typically about 100 millivolts (peak); the 200 millivolt threshold was chosen to insure that the comparator does not switch on baseline noise. Baseline noise is not relevant to the process of detecting the command signal; it is undesireable to have the signal detection logic switching on this noise. The 200 millivolt switching point permits detection of command signals which have dropped several db below the nominal 1.5 volt P-P level. The 200 millivolt switching points are determined by the amount of signal current fed to the comparator + input; this is controlled by potentiometer A21-1/2/5. Resistor A21-7/10 (510 ohms) is a terminating resistor for the driving circuit in L4.

A careful observation of the L14 LO Receiver output on an oscilloscope shows a pronounced baseline wobble of the signal (typically about 50 millivolts) as a function of the BI-Ø bit changes; this effect is an artifact of the AC coupling of the signal in L4, the LO Receiver. The signal level bounces up and down because BI-Ø bit changes alter the apparent duty cycle of the signal in a small region of time after a bit change. This baseline wobble phase-modulates the command signal input to the A2911 comparator; as a result the logic signal output by the comparator also has this phase modulation of about 50 nanoseconds. It should be noted that this effect is not seen on the Monitor and Control System test bench because the Test Bench analog command and monitor data signals are DC coupled.

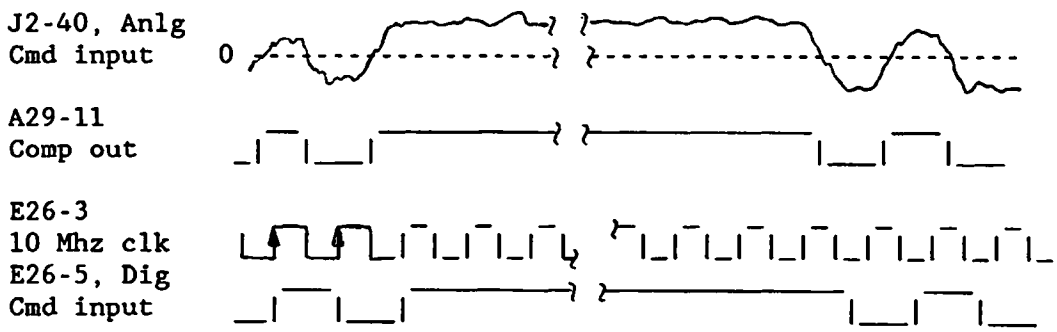
The 0 - 1000 usec command aperature on the reset inputs of shift registers A26, A1 and A23 enables this logic during the time that command messages are transmitted from the CB; this enable inhibits the command detection logic outside this aperature.

Shift register E26 provide a very important augmentation of the analog-to-digital conversion operation by comparator A2911. These flip-flops are Schottky 74S74's which have a 5 ns set up and 0 ns hold time. Comparator A2911 is a fairly fast comparator but is slow compared with TTL logic speed; the Schottky flip flops are used as a narrow aperature (5 ns) sampler to perform the 1/0 decisions. It is very important that **only 74S74 flip flops be used in E26; the 5 ns set-up and 0 ns hold times of the Schottky logic are vital in this A/D conversion process.**

Edge noise filter A23 has a very important function: filtering of command signal bit edge noise from the BI-Ø command stream. The logic decision performed by the comparator and E26 is influenced by noise, (eg power supply noise or RF noise added to the data signal in the transmission link); this noise can obscure the analog command signal and cause erroneous logic decisions. As the analog signal traverses through the comparator switching region at the edge of a data bit, this noise can cause spurious noise bits to be added to the detected data stream, causing them to have "fuzzy" edges so that the process of detecting and sampling the data bits in the center of the bit period could be erroneous if the appearance of a 1/0 or 0/1 change were

interpreted as the arrival of a new data bit. This phenomena is depicted in the Timing Diagram below. What is needed is a time-based digital filter that integrates over these noisy edges to indicate a true 1 or 0 data bit. The comparator waveforms are depicted below.

COMMAND SIGNAL A/D CONVERSION

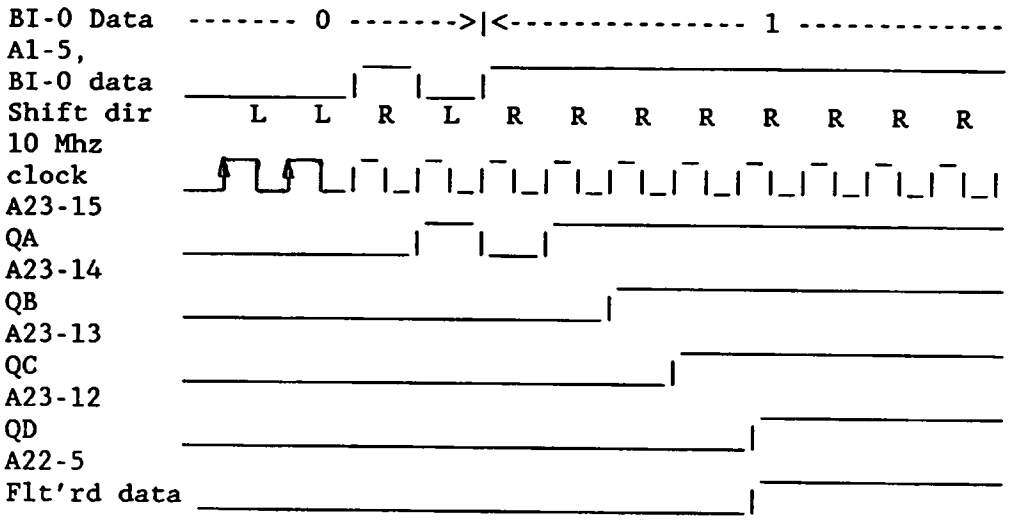


Register A23 performs the fuzz filtering function. A23 is a four-mode shift register: parallel load, clear, shift left and shift right as a function of the state of the control inputs S0 and S1 which are driven by shift register E26/A1. The 00 and 11 states of S0 and S1 clear and parallel load A23; these states never exist in this logic because A23 is driven by flip-flop A1 so that A23 sees only 10 and 01 states on the S0 and S1 inputs. These two states force left and right shifts of the data presented at the two data inputs: SR (shift right) and SL (shift left). The shift left input is tied to logic ground so that in shifting left, 0's are shifted into QD and move leftward through the register and the shift right input is floating (high) so that 1's are shifted into QA and move to the right through the register in the right shift mode. Note that the data is not shifted through the register. The contents of A23 may be all 1's, all 0's and either a 1/0 (eg. 1100, 1110 etc.) or 0/1 (eg. 0111, 0011, etc.) transition; multiple 1/0 or 0/1 transitions are impossible. Thus the 1's, 0's, and 1/0 or 0/1 transitions are pushed left or right in the register in accordance with the sequence of data states applied to the S0 and S1 inputs. Flip-flop A2205 is a noise-filtered replica of the BI-Ø data stream and is set to the 1 state when the first 1 (shifting right) in the 1100 (etc) transition reaches QD. A2205 is reset when the first 0 (shifting left) in the 0011 (etc) transition sequence reaches QA. Therefore, to set A2205 to the 1 state there must be an unbroken sequence of four 1's (or five 1's if there is a 0, six 1's if there are two 0's etc). The converse is the case for the reset of A2205. The simplified timing diagram on the next page illustrates how the "fuzz" on the edges of the data bits are integrated by this circuit.

At this point you may ask: "Under what conditions does this filter fail?". The filter fails when the signal is so badly obscured by noise that there are four consecutive false 1's or 0's; this will cause erroneous outputs. The period of such an event is 400 ns. The amplitude of a noise signal perturbation large enouth to cause this sort of damage would be in excess of .8 volts; the comparator must be

driven in the opposite direction, past the switching threshold. A signal this badly contaminated by noise is completely unuseable because the parity error rate would be immense. This noise level would obscure the BI-0 signal so badly that it would be difficult to recognize it by an oscilloscope observation of the L14 LO Receiver output. The timing diagram below illustrates the operation of this logic.

BI-Ø COMMAND SIGNAL EDGE NOISE FILTER TIMING



BI-Ø TO NRZ DEMODULATOR -- This not very obvious circuitry performs the function of reconstituting the NRZ data stream from the BI-Ø modulated signal. The demodulation process involves sensing BI-Ø bit edges, sampling each half of the 500 Khz BI-Ø signal, performing a comparison of successive portions of the signal to sense phase reversals and finally developing an NRZ data shift clock.

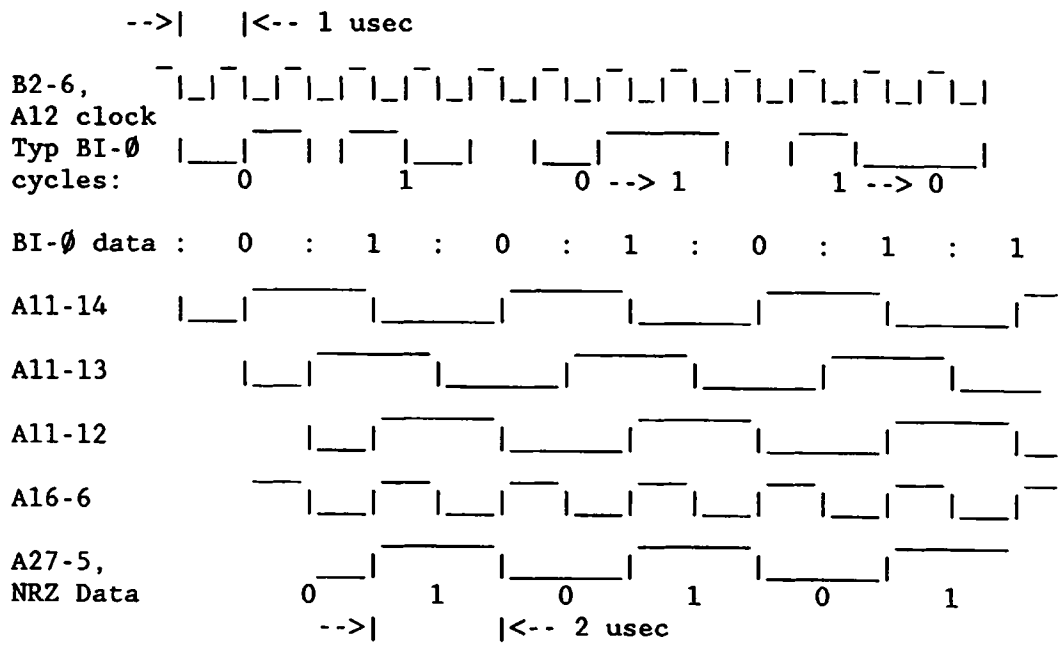
The essence of the BI-Ø demodulation process is depicted below. BI-Ø data is shifted through register A11 at a 1 Mhz rate to test each half of the BI-Ø structure; exclusive or A1606 output goes high when the inputs differ. The rise of A1606 clocks A2705 (with about 45 ns of delay to allow A2705 to set up) to sample the state of A11-12 which is 1 usec earlier in time. If there is a phase change in the BI-Ø data stream, A2705 will be set to the state which preceded the change, thus the resultant sequence of states of A2705 is the reconstituted NRZ data stream. The simplified timing diagram below (next page) illustrates the process. Note that the BI-Ø to NRZ demodulation process does not require any logic initialization; the message structure conveys the 1/0 message transitions. The AB and CB message streams are however prefaced by a preamble of BI-Ø zeros; this has been done to provide a time delay for the LO Receiver switching transient to settle.

Register A17, counter A12 and associated circuitry develop edge-synchronized sampling and shift clocks which sample the BI-Ø data, clock the BI-Ø to NRZ converter and load the NRZ data into the command

input registers B1 and B24.

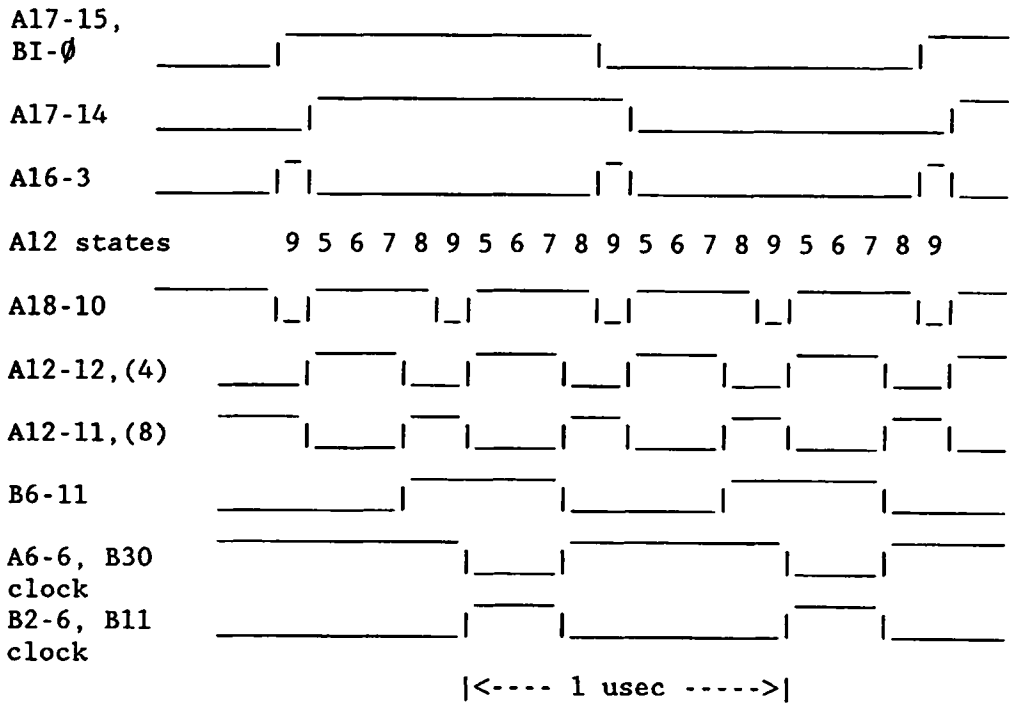
Counter A12 is the Bi-Ø demodulation control counter which is synchronized to the BI-Ø data bit edges; terms developed from the counter states regulate all demodulation and data loading functions. These timing operations are depicted on the simplified timing diagram below.

BI-Ø TO NRZ CONVERSION OF THE START OF A COMMAND MESSAGE



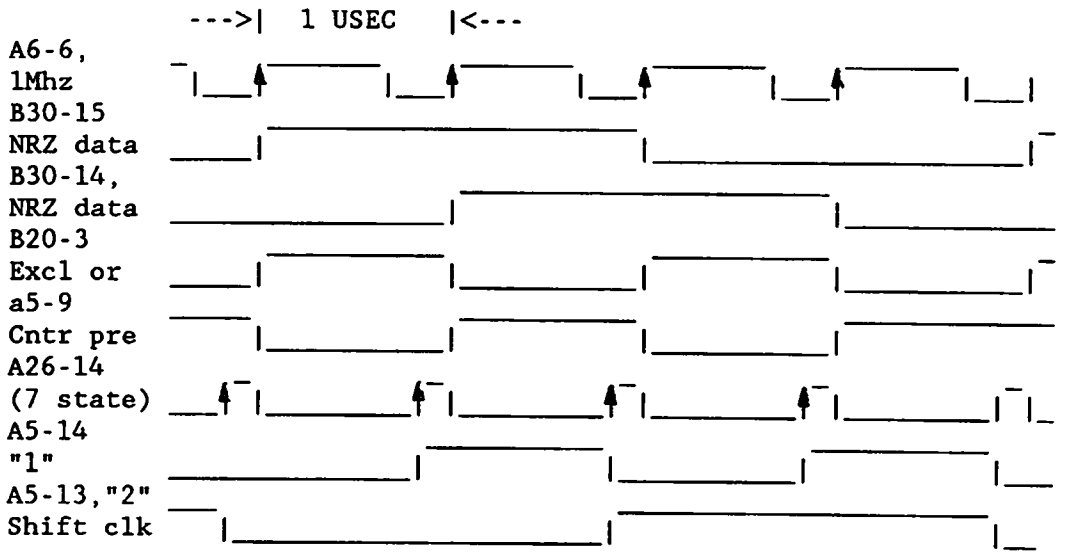
The noise filtered BI-Ø bit stream is shifted through shift register A17 at a 10 Mhz rate; 1/0 or 0/1 state differences in A17-15, 14 cause exclusive or gate A1603 to go high. This high output causes counter A12 to be set to the 5 state and it proceeds to count through the states 5,6,7,8,9,5,6 ... ; the terminal count on pin 15 is fed back to preset the counter to the 5 state when there is not an edge sensed by A1606. The 500 Khz BI-Ø signal has a period of 2 usec and there may (or may not be) a phase reversal. A12 generates a 1 Mhz sample clock delayed by 500 ns from the bit edges to sample each half of the BI-Ø cycle in the center of the pulse. When A12 is preset to 5, flip flop B0611 is cleared and then is toggled to the 1 state at the start of the 8 state in A12. Gate A606 goes low during states 5,6,7 in A17 and goes high at the start of the 8 state, the leading edge (fall) of A606 clocks the BI-Ø data into shift register A11 and the trailing edge (rise) clocks the demodulated NRZ data into B30. Thus the A606 clock is a 1 Mhz clock, phased to the BI-Ø data edges and controls both the BI-Ø demodulation and NRZ data loading. Inverter A10 is tied to the clear input of flip-flop B0611 to insure the correct phasing of B0611. The major timing generation terms are depicted on next page.

BI-Ø TO NRZ CONVERTER CLOCK GENERATION



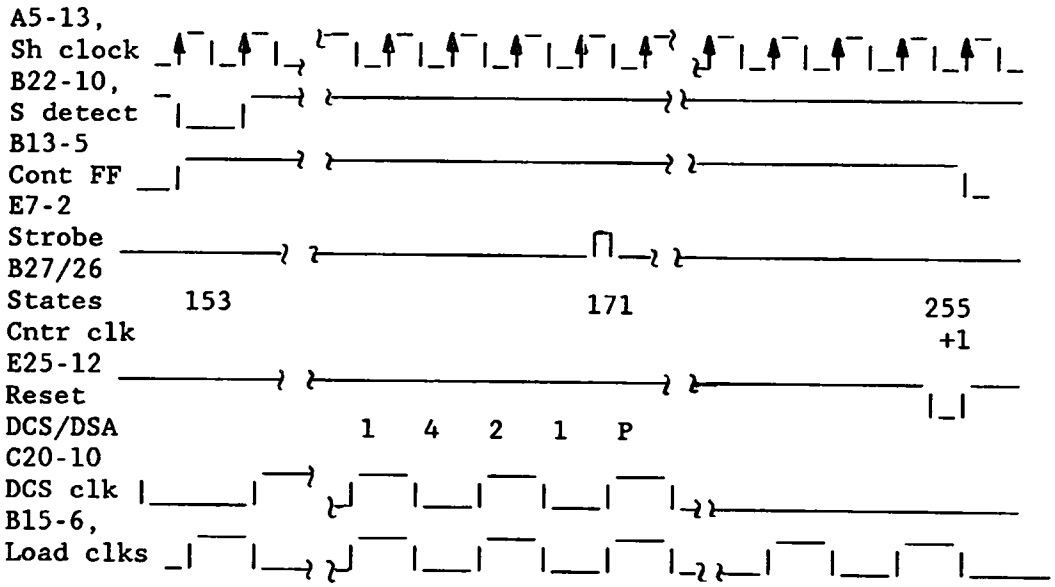
NRZ DATA CLOCK SYNCHRONIZATION -- Having managed to demodulate the Bi-Ø signal to the NRZ format, it is now necessary to synchronize to and store the incoming message in the serial command memory. A 500 Khz clock, edge-phased to the NRZ data is required to shift the reconstituted NRZ data from B3014 into the Command Message Detector registers B24 and B1 so that the message stream can be tested for the occurance of the "S" (Start) prefix to the command messages. Counter A12 (used in the BI-Ø to NRZ demodulator) is used as a coherent clock source. Counter A5 performs this synchronizing function and is phased to the NRZ data edges in B30 by exclusive or B2003. Counter A5 is preset to a count of 12 by B2003 and sequences through the states 12,13,14,15,12,13.... to divide the 2 Mhz clocks (A12 state 7) 4 to produce the phased 500 Khz clocks which shift the NRZ data into B24. The simplified timing diagram (next page) illustrates the operation of this logic.

NRZ DATA CLOCK SYNCHRONIZATION



COMMAND MESSAGE DETECTION AND LOADING LOGIC -- Having managed to develop a load clock synchronized to the edges of the NRZ data, it is now necessary to detect and load the command messages. The NRZ data stream is shifted into the Command Message Detector shift registers B24 and B1 by the load clock developed in A0513. Gate B2210 tests the B24 pattern for the presence of the "S" character, - when detected, the low true output sets load contol flip-flop B13 which enables the command message to be loaded into the command message memory B19. The command message stream is tapped off shift register B0105 and the loading is enabled by the 0 - 1000 term on gate E1603. The memory load clocks are controlled by the command load counter B27 and B26 which are preset to a count of 151 and clocked by B2312 which is inverted from the sense of the A513 (which loads the shift registers B24 and B1) clock. The loading sequence is terminated when the 128 bit falls low at a count of 256 (1 count after 255, ie, all bits set in B27 and B26). The 128 bit is (low-true) and-ed with the counter clock in gate E25 and the rising edge of the gate output clocks control flip-flop B13 off to inhibit the memory load clocks via and-or gate B14 pin 3. The load control counter thus provides 104 clock pulses to load the 100 bit message and 4 spacing bits into the command memory. The simplified timing diagram on the next page illustrates the operation of this logic.

MESSAGE LOAD CONTROL TIMING



The command message stream is shifted through the shift registers B18 and A19 which drive the 74180 Parity checker/generator to test the DCS/DS address byte and associated parity bit for parity errors. A timing strobe term is applied to gate E0714 to clock the DCS address into register E11 if not inhibited by the parity checker and exclusive-or B20.

The stored DCS address is displayed on the front panel.

The timing strobe term is generated by gate C1006 which goes true at count 202 in counter B24/B1. Flip-flop E0205 is initialized true by the "S" detect which enables gate C10; the strobe is short (about 60 ns); the duration is determined by the propagation time of E0205, C10 and inveter C2004. Flip-flop D1711 generates a 100 Khz shift clock for the DCS address parity checking circuitry and is initialized by the "S" detect gate B2210. The shift clock is turned of by flip-flop C1505 which is reset by the timing strobe that tests the DCS address parity.

The reason for testing the parity on the DCS byte is that the stored DCS address is dubbed into the monitor data as it is loaded into the monitor data memory. As an aside; the reason why the DCS address is trapped from the command message stream rather read from a rack-mounted thumbwheel switch is to eliminate the need for remembering to set this switch correctly when moving antennas. This switch setting would almost invariably be wrong after an antenna move.

Pull-up resistors B2101 and B2102 are required because the AM2855PC command memory registers require a signal swing slightly greater (ie. > 4 volts) than that normally available from a TTL gate. These memory chips shift on the fall of the clock rather than the rise like the other shift registers in the AB. And-or gate B1406 is a clock selector

used to select either the 500 Khz Command Load or 200 Khz command unload clock rates as a function of the control discretes 0 -1000 or 1000 - 5000 usec.

Command Memory B19 is a quad, 128 bit bit MOS shift register with TTL compatible clock, inputs and outputs. When quiescent, the clock must be held in the low state. See the Data Sheet section for the specifics on the AM 2855PC chip.

COMMAND UNLOAD LOGIC -- The command unload logic is quite simple; Counter B29 develops a 200 Khz unload clock which is applied to the B14 and-or gate to push the command messages out of B19. The unload is enabled by the 1000 - 5000 enable. The message unload period is 500 microseconds/message so that all messages are completely flushed out in the 4 ms unload time. The messages are broadcast to all Data Sets via the 4-input low-true or gates (Sheet 1) which drive the Data Set Command Ports.

You will note that the signal polarity of the Data Set 0 port is high-true; this is necessary because the ACU requires a high-true input. This polarity reversal is also the case with the Data Set 0 Monitor Data Port.

3.3 MONITOR DATA POLLING, DETECTION, STORAGE AND OUTPUT

This is the second major function of the Antenna Buffer; most of the VLA monitor data is gathered by this module.

DATA SET POLLING LOGIC -- Enable 14,700 - 23,700 permits the monitor data control counters, (Sheet 2) A2 and A8 to poll the Data Sets for monitor data messages. Counter A2 generates the 900 usec polling period and has a 10 Khz Cet input from counter B9 so that it counts at a 10 Khz rate. Gate A0603 goes true at the count of 9 and immediately presets the counter to 0 so that the period is 900 usec. The A0603 trailing edge clocks counter A8 which generates a 3 bit Port Address to select Data Set Ports for output of the "Q" polling character and to listen for the monitor data message evoked from the Data Set in response to the Q. A8 has a radix of 5; it is initialized to 0 by the 14,700 - 23,700 enable and is reset to 0 at the leading edge of state 4.

The Q character is immediatley emitted by shift registers A7 and D23 when the 14,700 - 23,700 enable rises and at the beginning of each 900 usec polling period; gate C3010 or's the enable and counter A2 resets to load the Q character into the shift registers. Flip-flop D2306 generates a one clock pulse duration hold-off inhibit on gate C3010 so that the leading edge of the Q is a distinct rise to a 1 state. The Q's are distributed to the Data Set Command Port or gates by A9, a data selector (decoder) under control of the port address terms from counter A8.

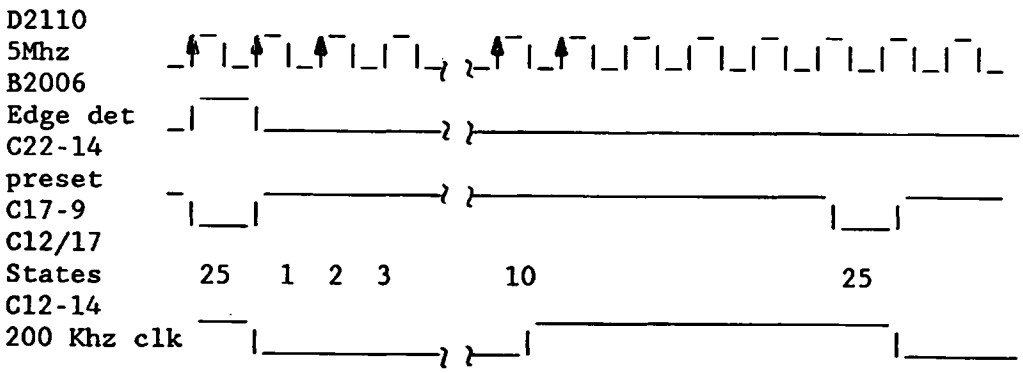
The Q character shift clocks are generated by gates C0906 and D2203

using terms from counter B10 which is the 1 Mhz to 100 Khz, divider in the time base.

DATA SET MONITOR DATA INPUT LOGIC --- The Data Set Monitor Data Ports consist of 5 optical isolators (to eliminate common-mode noise effects) and a digital multiplexer D1515 driven by the port address terms from counter A8. This simple logic is shown on Sheet 5. The multiplexer output is inhibited until enabled by the 14,700 -23,700 enable. Note that Data Set 0 has a high-true input; the ACU output polarity is opposite to the Data Set signal polarity.

The output of the multiplexer D1515 is the monitor data message stream evoked from the selected Data Set by the Q character. The receiving logic on Sheet 4 must detect and synchronize to the message stream. The monitor data stream is sampled at a 5 Mhz rate (the message bit rate is 200 Khz) in register C13. Exclusive or B2006 on shift register C13 senses the data edges of the incoming message stream and phase adjusts the time base counter C17 and C12. The counter divides by 25 to produce the 200 Khz shift clock which is phased 10 counts from the edge of the input data bits. The operation of this phase adjusted time base is similar to the phase-adjusted clocks described above; the simplified timing is depicted below.

MONITOR DATA PHASE ADJUSTED TIME BASE TIMING



The rise of B2006 also sets flip-flop A2711 (Sheet 1), the Data Set Heard From enable (DSHF) which permits the Data Set data to be clocked out to the Data Set Command Port or gates as Gossip Data.

As the monitor data message propagates through the SAA Inject & Parity Logic on Sheet 4, the stored DCS address (from register E11 on Sheet 1), the Data Set Address and the parity bit for the byte must be injected into the message stream. This operation is performed by the tricky setup of the shift registers C18, D29, D30 and C23. We will defer the description of this logic till later in the discussion.

This SAA Inject & Parity Logic shift register is clocked at 200 Khz by the phase adjusted clock counter C17 and C12. As edges are detected by B2006, the counter is preset to a count of 1; at the count

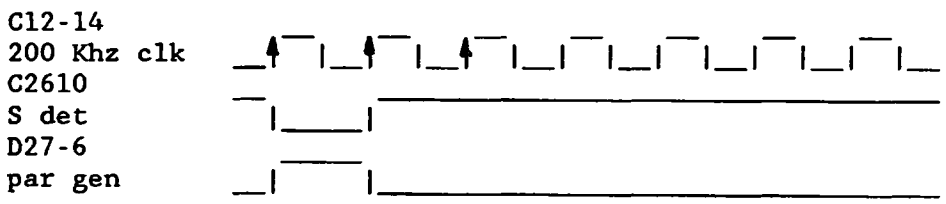
of 25 the counter is again preset to 1; in the event that the exclusive or B2006 senses another edge before the 37 count reset, the counter will again be reset to 1 count. The rise of C1213 (at a count of 10) is the phase adjusted 200 Khz shift clock which shifts the monitor data through the SAA etc register. The 10 count phasing (in C17 & C12) is the approximate mid-point of the monitor data message data bits.

When the S character message prefix reaches the C23 and C27 shift register, it is detected by and-gate C2610 which goes low-true for 5 usec; this does two things: 1) the SAA Inject & Parity shift registers are caused to parallel load the DCS, DSA (ie the Data Set port address from A8) and the parity bit states appearing at the register's parallel inputs. 2) the Monitor Data Load Counter is set into operation to load the Monitor Data Register with the incoming message.

Let's first consider the SAA inject logic: Parity generator D2706 forms odd parity over these 8 address bits and the odd parity output is applied to register C18 pins 4,5. The next two 200 Khz clocks cause the parity bit and the two addresses to be loaded into C18, D29, D30 and C23. The odd-looking feed-forward of the Q's of C18, D29 and C23 into the next stage preset inputs deserves some attention. The parallel load of the DCS/DSA and parity bit into these registers results from the clock rising edge when the preset enable is low. Since this parallel load is performed on the fly as the message is shifting through the register, the pause for loading causes the registers to "miss" one shift clock; to compensate for this loss the register contents are "jumped" one stage to make up the one shift clock deficit. The D30 register is asnychronously set by the Shift/load line and is independant of the clock; the address bits are wired to two inputs on this register. The timing of this logic is depicted on the next page.

The incoming message stream is inverted by A1814 and reclocked by flip flop D2511 (sheet 2) to form the low-true Gossip data which is output to the Data Set Command Ports or-gates which cause it to be broadcast to all Data Sets (with the exception of Data Set 0, the ACU which gets confused by the Gossip data). Note that this pickoff point us upstream from the DCS injection logic so that the Antenna monitor data always has a DCS address of 0 irrespective of the actual antenna DCS address. This feature can be very convenient at an antenna Data Tap as it permits observation of the monitor data message flow from a Data Set distinct from the command message flow (set the Mux sel switch to any). See next page.

DCS/DSA ADDRESS & PARITY BIT INJECTION LOGIC TIMING

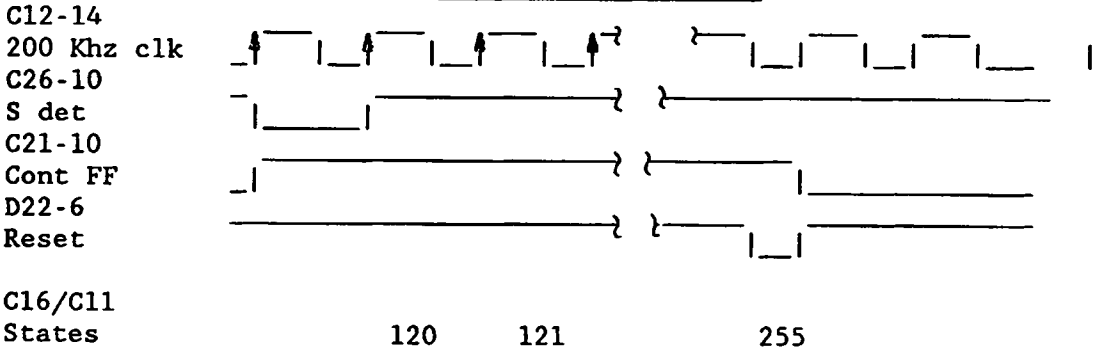


(Assumes that sum of DCS/DSA data bits in the byte is even)

The Monitor Data Load Counter, C16 and C11 generates a load enable to permit the monitor data messages to be loaded into the Monitor Data Memory, D20, D19, and D14. The memory is loaded by the shift clocks generated by C1214 which are used to shift in the monitor data message as described above. Counter C16, C11 are preset to a count of 135 by the S detect gate C2610 which sets counter control flip-flop C2105 and presets the counter to a count of 135. The terminal count of C11 is and'ed with the clock in gate D22 to reset C2105 which terminates the load enable. The load enable, C2105 is fed to the and-or gate D2403 (Sheet 5) which causes the monitor data message to be shifted into the serial monitor data memory. The monitor data message to be loaded is tapped off shift register C2714 on Sheet 4. The timing of this logic is depicted below.

Pull-up resistors B21-3,4 provide a 5 volt swing for the memory data input and clock lines.

MONITOR DATA MEMORY LOAD TIMING

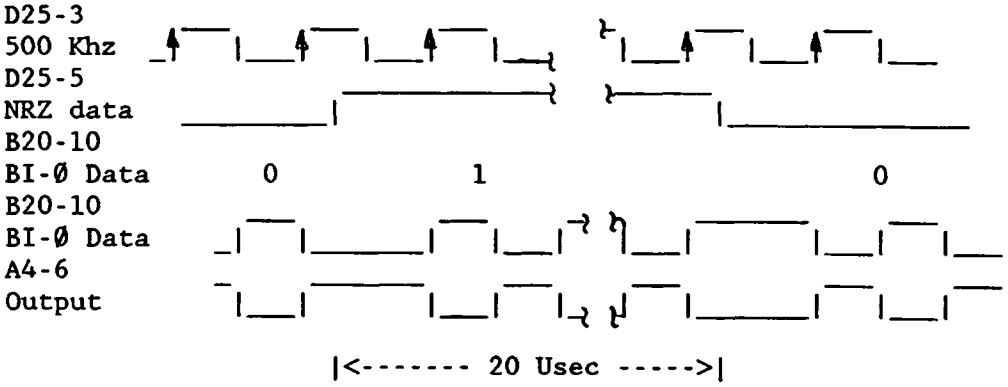


MONITOR DATA UNLOAD TO CENTRAL BUFFER -- The last thing to be done in the Monitor Data operations is to unload the messages accumulated in the Monitor Data Memory to the Central Buffer via the Antenna LO Transmitter, L3. The 24,000 - 48,000 enable term is input to and-or gate D2405 and permits the 50 Khz clocks to shift out the data. The memory output is clocked into flip-flop D2505 and the flip-flop output is BI-Ø modulated by exclusive or B2010. The data memory is clocked into D2510 so that the BI-0 signal has a 50% duty cycle. Finally, the BI-Ø output is gated by and buffer and gate A0406 which enables the

BI-Ø data output to the LO Transmitter only during the actual period of the monitor data transmission. If this BI-Ø signal was ungated, the BI-Ø would continuously modulate the L3 and it would be more difficult to observe the data structure on the Central LO Receiver (L9) output. The buffer gate output to L3 pulls a 5 volt tap point on a 15 volt resistive divider to ground in L3. The BI-Ø modulation process is depicted in the timing diagram below.

It should be noted that the Command message path, Central LO Transmitter (L10) to Antenna LO Receiver (L4) transmission link has a signal inversion in the Receiver but the Monitor Data path, Antenna LO Transmitter (L3) to Central LO Receiver (L9) does not have a corresponding inversion. The reason for this inversion is that in the two LO receivers, the diode detectors which detect the signals have opposite polarities on the input to the receiver data amplifiers. The L3 diode detects the positive RF swings while the L9 diode detects the negative RF swings.

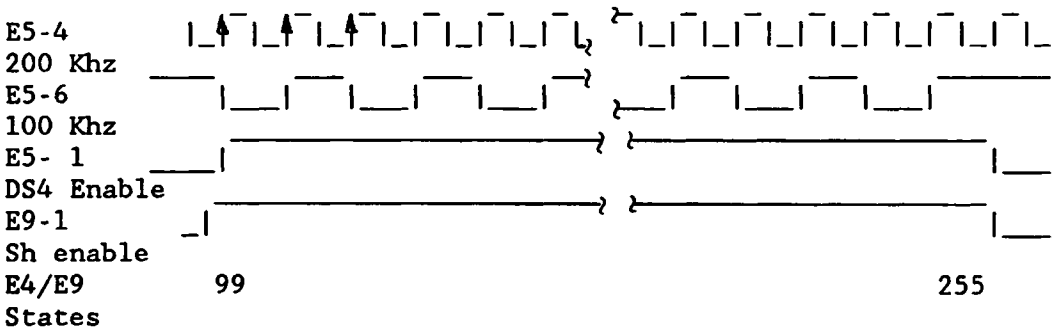
ANTENNA BUFFER BI-Ø MODULATOR TIMING



DATA GENERATOR LOGIC -- The data generator logic on Sheet 6 generates a monitor data message in response to a DS4 Enable from C1410 (Sheet 2). Referring to this sheet we see that C1410 is set at 300 usec if DSHF (low true) is low; that is if the selected Data Set has not respoded within 300 usec, (it should respond in 250 usec) the DS4 Enable term goes true and the Data Generator is triggered into operation. Load control counter E4/E9 is enabled by the DS4 Enable. Flip-flop E0506 divides the 200 Khz clock to produce the 100 Khz clock pulses which unload the E8 .. E12 portion of the register. The 200 Khz clock unloads the E17/E18 portion of the register. The delay line B17 provides about 80 nanoseconds of delay to the 100 Khz shift clocks so that E17 can properly sample the output of E12. The DS4 Enable permits the Data Generator output to be routed through the 2:1 multiplexer E2204 (Sheet 5) on the output of the data selector multiplexer in the Data Set Monitor Data Ports. Thus the DS4 Enable selects the output of the Data Generator rather than the Data Set multiplexer, D1515. The commands detected by the command detectaion circuitry are counted by E19 and are caused to be loaded with the mux address 205 (octal) DS4 enable. Counter E19 is cleared by the QQ pulse from the L8 at the

start of the 1000 usec period. The operation of this logic is depicted in the simplified timing diagram below.

DATA GENERATOR OUTPUT TIMING



In the Model D AB the output of optical isolator D134 was disconnected from the D1515 multiplexer and the Data Generator output was hard-wired to the E2204 multiplexer. In the Model E AB, the optical isolator has been re-connected to multiplexer D1515 and the hard-wired connection to the Data Generator has been removed so that a real Data Set can be connected to the Data Set #4 port. This change was incorporated to add the Data Set that controls the X-band receiver.

3.5 ANTENNA ID READOUT -- The Antenna ID number is read out by Data Set 2 as a conventional Binary Monitor Data channel, mux address 202 (octal). This logic has no functional relationship to the AB functions and resides in the Antenna Buffer simply because there was no other place to put it. The Data Set provides a load strobe to parallel load registers E20 and E24 and shift clocks to push the contents of the registers out to the Data Set. Note that the register E20 QH output is tied to the it's Serial input, this makes the contents recirculate in E20 so that the Antenna ID is read out in both the middle and least significant byte. By averaging these two readouts the computer is able to obtain a more accurate value for the ID#. The most significant byte contains the command count described in the Data Generator logic. The Antenna ID # is hard-wired on the back of the bin; grounding any of the 5 I/O pins will cause a zero to be read out in the corresponding data bits. See the Data Set manual for a description of the way that the Data Set reads binary monitor data.

3.6 POWER CIRCUITS -- The analog comparators and the MOS memories require non-standard -12 volt, +12 volt and -5 volt power; Motorola MC7905 and MC79812 regulators provide the negative voltages and a Motorola MC7812 provides the +12 volt power. These regulators require isolation of the case from module ground; if these chips fail, don't forget to replace the mica washers and Silicone grease when replacing them. If non-Motorola replacements are substituted, be sure of the wiring because other manufacturers regulators have similar part numbers but a different pin-out.

4.0 LIST OF MAJOR ANTENNA BUFFER DRAWINGS

D13720P78 Antenna Buffer Top Assembly Drawing
A13720Z04 Antenna Buffer Top Assembly BOM
D13720L47 Antenna Buffer Logic Schematic, Model D
D13720L76 Antenna Buffer Logic Schematic, Model E
A13720W16 Master Wire List
A13720W17 Machine Wire List
A13720W18 Hand Wire List
A13720W19 Connector Wire List
A13720W49 J2 Wire List
B13720AB05 LED Display PCB Artwork
C13720M36 LED Display PCB Drill Dwg
C13720M16 Front Panel
B13720AA50 Front Panel Silkscreen Artwork
A13720P79 IC Module Ass'y
A13720Z34 IC Module Ass'y BOM
A13720P39 LED Display Ass'y
B13050M17 Perf Cover Fastener
C13050M07 1W Perf Cover
C13720M15-1,-2 Rail Modification
C13720M17 Insulated Spacer
C13720M23 Rear Panel
C13720M32 DCS Module WW Field Dim Def
C13720M50 Side Plate, Modified
C13720P68 Insulated Side Plate Ass'y
X13720M49 Side Plate Insulatiion
B13720M47-1 Module Bar Spacer
D13720M96 Buffer Wiring Jig Configuration

See the Drafting Drawing Listing for Dip Header drawings

5.0 Special Module Data Sheets

The Data Sheet for the AM2855PC MOS serial memory chip follows.

Am2855 • Am2856 • Am2857

Quad 128-Bit, Dual 256-Bit and Single 512-Bit Static Shift Registers

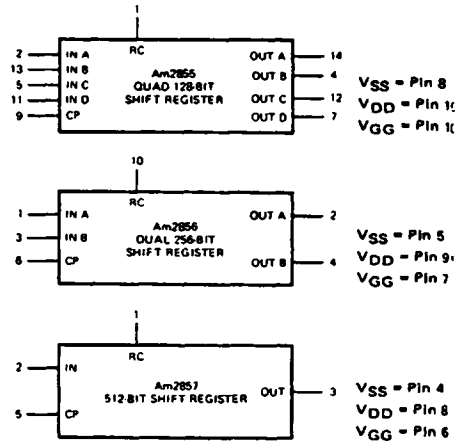
Distinctive Characteristics

- High-speed replacement for National 5055/6/7
- Internal recirculate
- Single TTL compatible clock
- Operation quaranteed from DC to 2.5MHz
- 100% reliability assurance testing in compliance wi MIL-STD-883

FUNCTIONAL DESCRIPTION

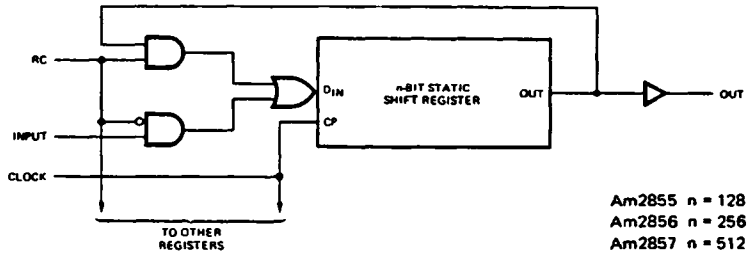
These devices are a family of static P-channel MOS shift registers in three configurations. The Am2855 is a quad 128-bit register; the Am2856 is a dual 256-bit register; and the Am2857 is a single 512-bit register. All three devices include on chip recirculate. The registers are all clocked by a single low-level clock input. Because the registers are static, the clock may be stopped indefinitely in the LOW state without loss of data. Each of the registers has a single data input; data on the input is written into the register on the HIGH-to-LOW clock edge. A single recirculate control (RC) on each chip determines whether the registers on that chip are to write data in from the data inputs or recirculate the data appearing on the output. If RC is LOW, new data is written in; if RC is HIGH then the data on the output will be written back into the register input on the next clock pulse.

LOGIC SYMBOLS



MOS-440

LOGIC BLOCK DIAGRAM
(One Register Shown)



Am2855 n = 128
Am2856 n = 256
Am2857 n = 512

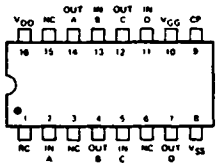
MOS-441

ORDERING INFORMATION

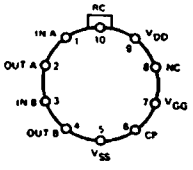
Package Type	Temperature Range	Order Number
16-Pin Molded DIP	0°C to +70°C	AM2855PC
16-Pin Hermetic DIP	0°C to +70°C	AM2855DC
16-Pin Hermetic DIP	−55°C to +125°C	AM2855DM
10-Pin Plastic DIP	0°C to +70°C	AM2856PC
TO-100 Can	0°C to +70°C	AM2856HC
TO-100 Can	−55°C to +125°C	AM2856HM
8-Pin Molded DIP	0°C to +70°C	AM2857PC
8-Pin Hermetic DIP	0°C to +70°C	AM2857DC
8-Pin Hermetic DIP	−55°C to +125°C	AM2857DM

CONNECTION DIAGRAMS

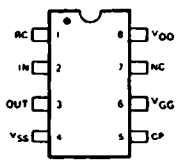
Am2855



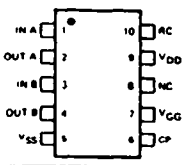
Am2856



Am2857



Am2856



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +160°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{DD} Supply Voltage	V_{SS} −10V to V_{SS} +0.3V
V_{GG} Supply Voltage	V_{SS} −20V to V_{SS} +0.3V
DC Input Voltage	V_{SS} −20V to V_{SS} +0.3V

OPERATING RANGE

Part Number	Ambient Temperature	V_{SS}	V_{DD}	V_{GG}
Am2855DM Am2856HM Am2857DM	−55°C to +125°C	5.0V ±5%	0V	−12V ±5%
Am2855PC, DC Am2856HC Am2857PC, DC	0°C to +70°C	5.0V ±5%	0V	−12V ±5%

5

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −0.5mA	2.4			Volts
V_{OL}	Output LOW Voltage	I_{OL} = 1.6mA			0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	V_{SS} −1.0		V_{SS} +0.3	Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	V_{SS} −18.5		V_{SS} −4.2	Volts
I_{IL}	Input Leakage Current	V_{IN} = −10.0V, all other pins GND, T_A = 25°C		0.01	0.5	µA
I_{DD}	V_{DD} Power Supply Current	T_A = 25°C, $t_{\phi pw}H$ = 160 ns, Data = 1010. . . output open, f = 2.5 MHz		20.0	28.0	mA
I_{GG}	V_{GG} Power Supply Current			12.0	16.0	mA

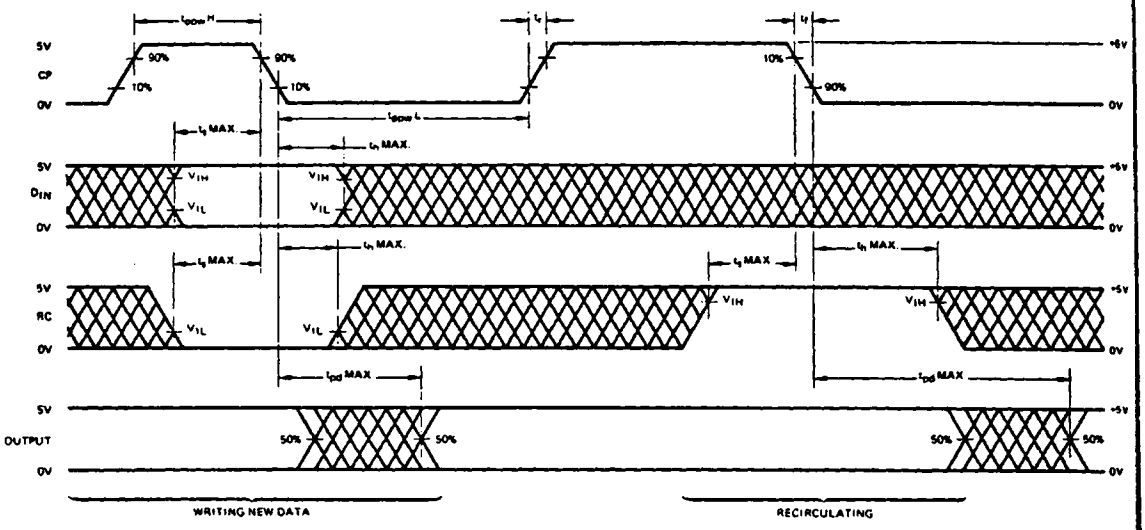
Note: 1. Typical Limits are at V_{SS} = 5.0V, V_{GG} = −12V, 25°C ambient and maximum loading.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
f	Clock Frequency		0		2.5	MHz
$t_{\phi pw}H$	Clock HIGH Time		0.16		10.0	µs
$t_{\phi pw}L$	Clock LOW Time		0.200		∞	µs
t_r, t_f	Clock Rise and Fall Times		10		200	ns
t_s	Set-up Time, D or RC Inputs (see definitions)	t_r = t_f = 50ns	100			ns
t_h	Hold Time, D or RC Inputs (see definitions)	t_r = t_f = 50ns	40			ns
t_{pd}	Delay, Clock to Output LOW or HIGH	R_L = 4k, C_L = 10pF	(Note 3)	160	280	ns
C_{in}	Capacitance, Data In and RC Inputs (Note 2)	f = 1MHz, V_{IN} = V_{SS}		3	7	pF
C_ϕ	Capacitance, Clock Input (Note 2)	f = 1MHz, V_{IN} = V_{SS}		3	7	pF

Notes: 2. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.
3. At any temperature, t_{pd} min. is always much greater than t_h(D) max.

TIMING DIAGRAM



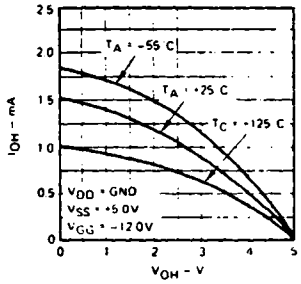
MOS-4

KEY TO TIMING DIAGRAM

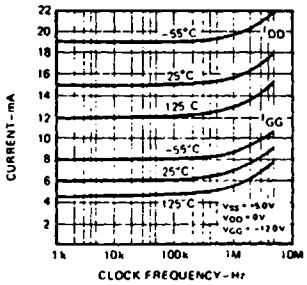
WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
▨	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN

PERFORMANCE CURVES

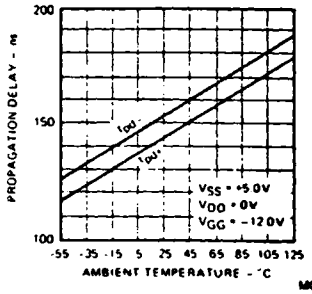
Typical Data Output HIGH Current Versus Data Output Voltage



Typical Power-Supply Currents Versus Frequency



Typical Propagation Delay Versus Ambient Temperature



MOS-4

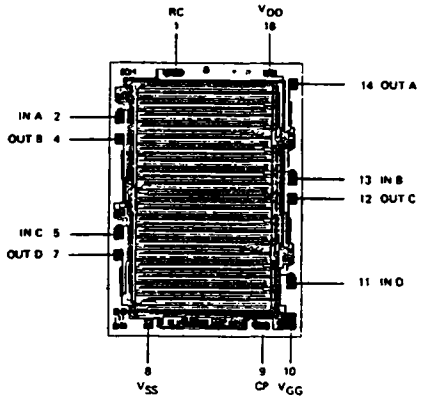
DEFINITION OF TERMS

STATIC SHIFT REGISTER A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is HIGH and is transferred to the static slaves while the clock is LOW. The clock may be stopped indefinitely in the LOW state, but there are limitations on the time it may reside in the HIGH state.

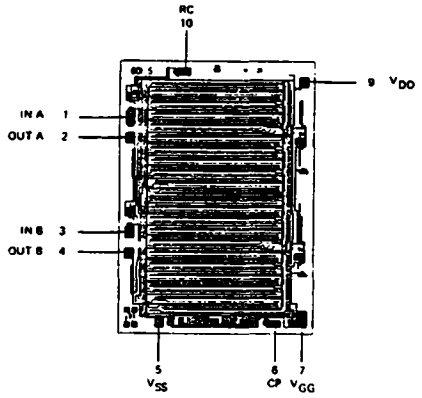
SET-UP and HOLD TIMES The shift register will accept the d that is present on its input around the time the clock goes f HIGH-to-LOW. Because of variations in individual devices, t is some uncertainty as to exactly when, relative to this c transition, the data will be stored. The set-up and hold ti define the limits on this uncertainty. To guarantee storing correct data, the data inputs should not be changed betw the maximum set-up time before the clock transition and maximum hold time after the clock transition. Data cha within this interval may or may not be detected.

Metallization and Pad Layouts

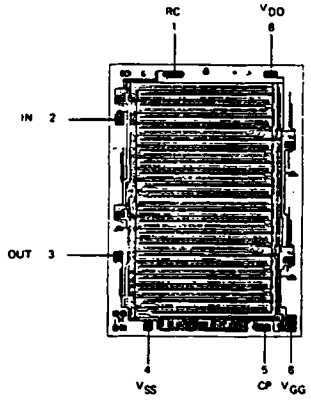
Am2855



Am2856



Am2857



DIE SIZES: 0.101" X 0.142"

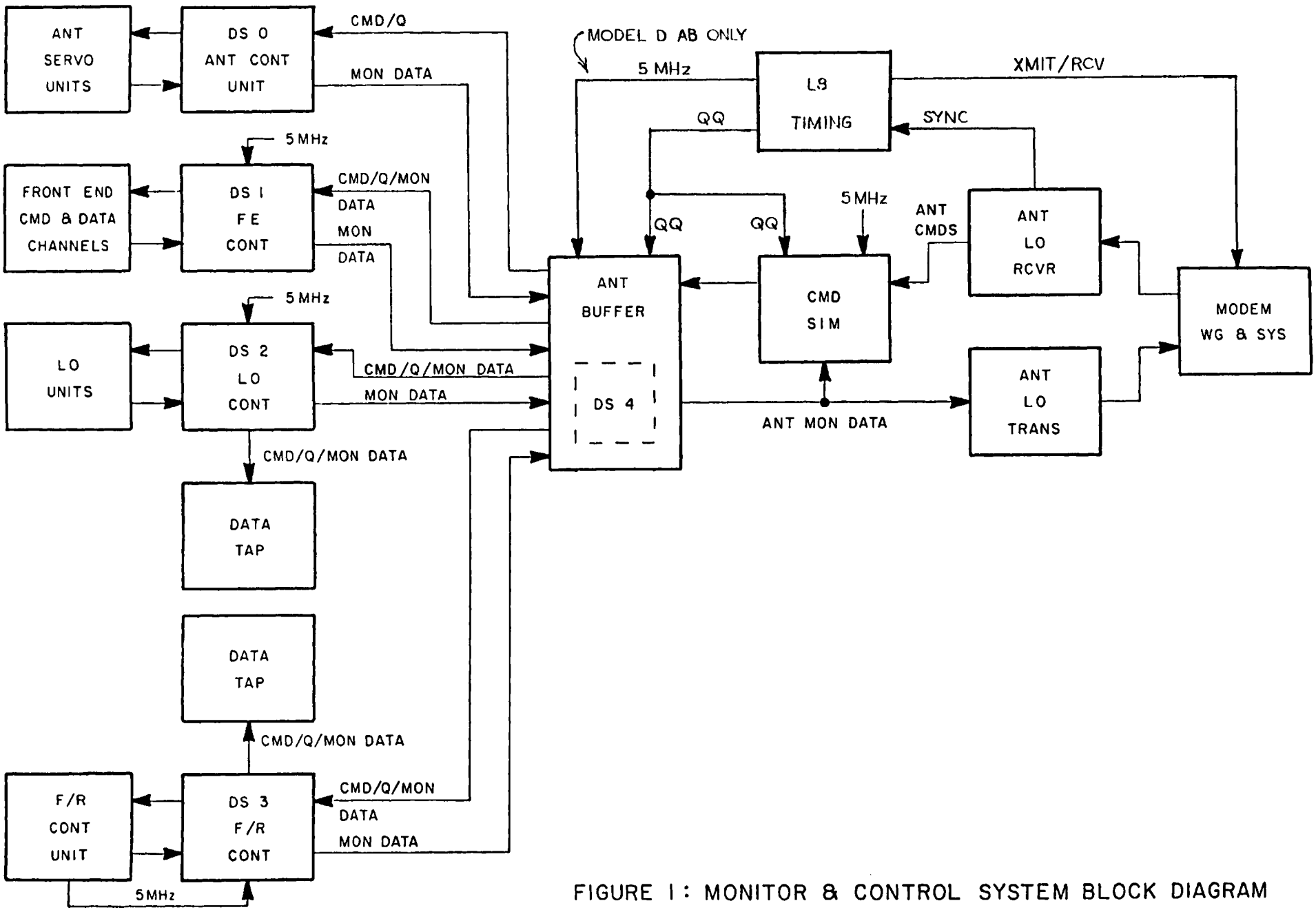


FIGURE 1: MONITOR & CONTROL SYSTEM BLOCK DIAGRAM

REV. 7-86

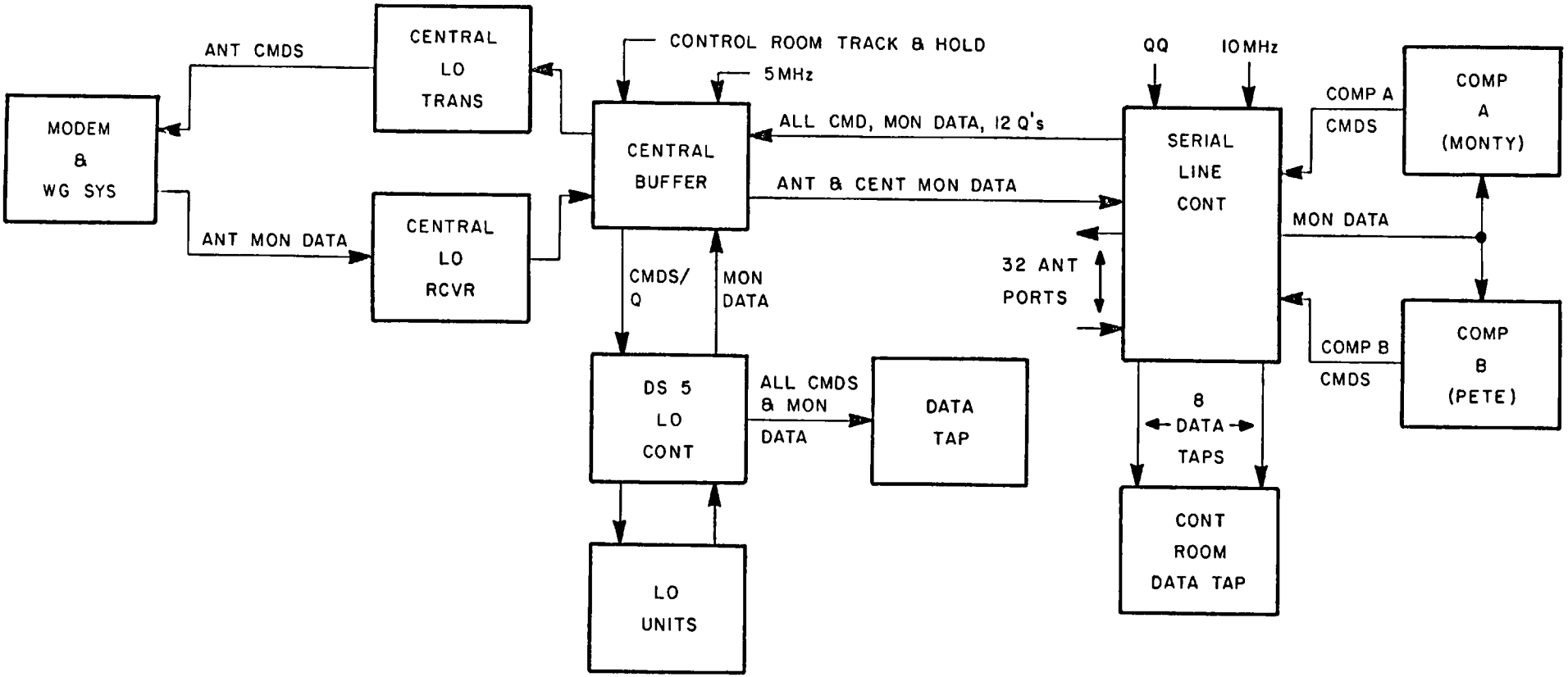


FIGURE 1: CONTINUED

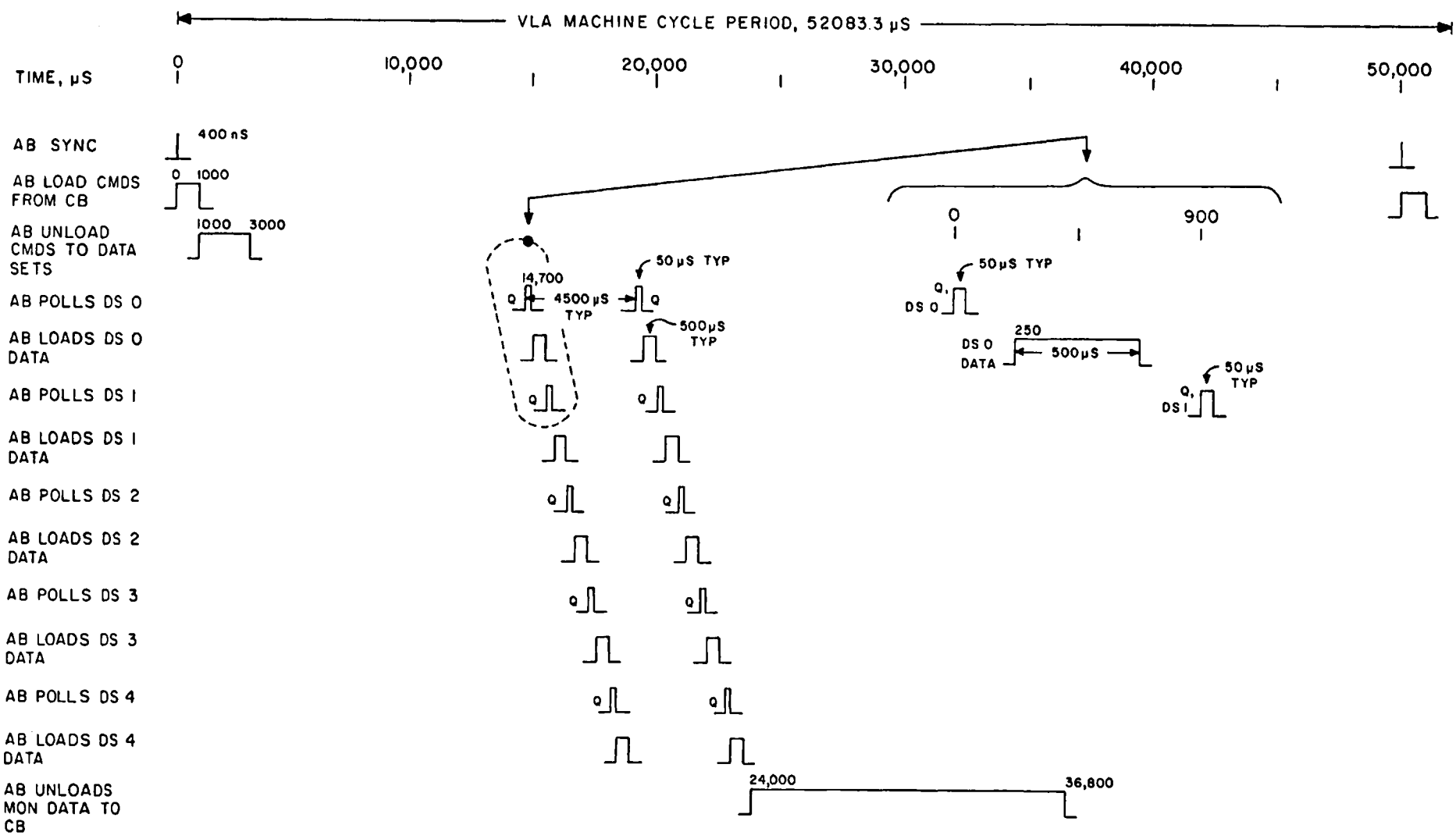


FIG. 2

ANTENNA TIMING OPERATIONS

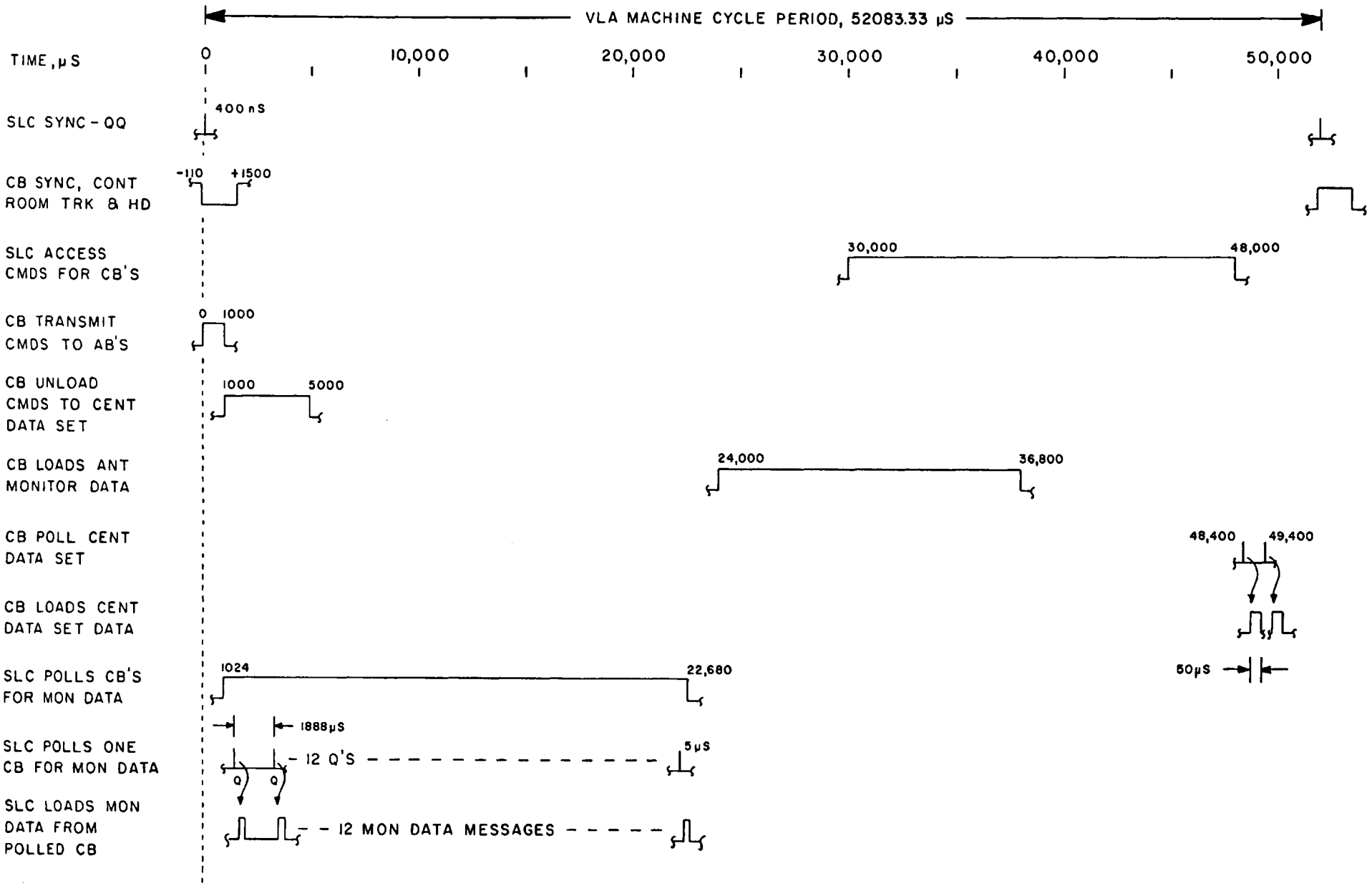


FIG. 3
CENTRAL TIMING OPERATIONS

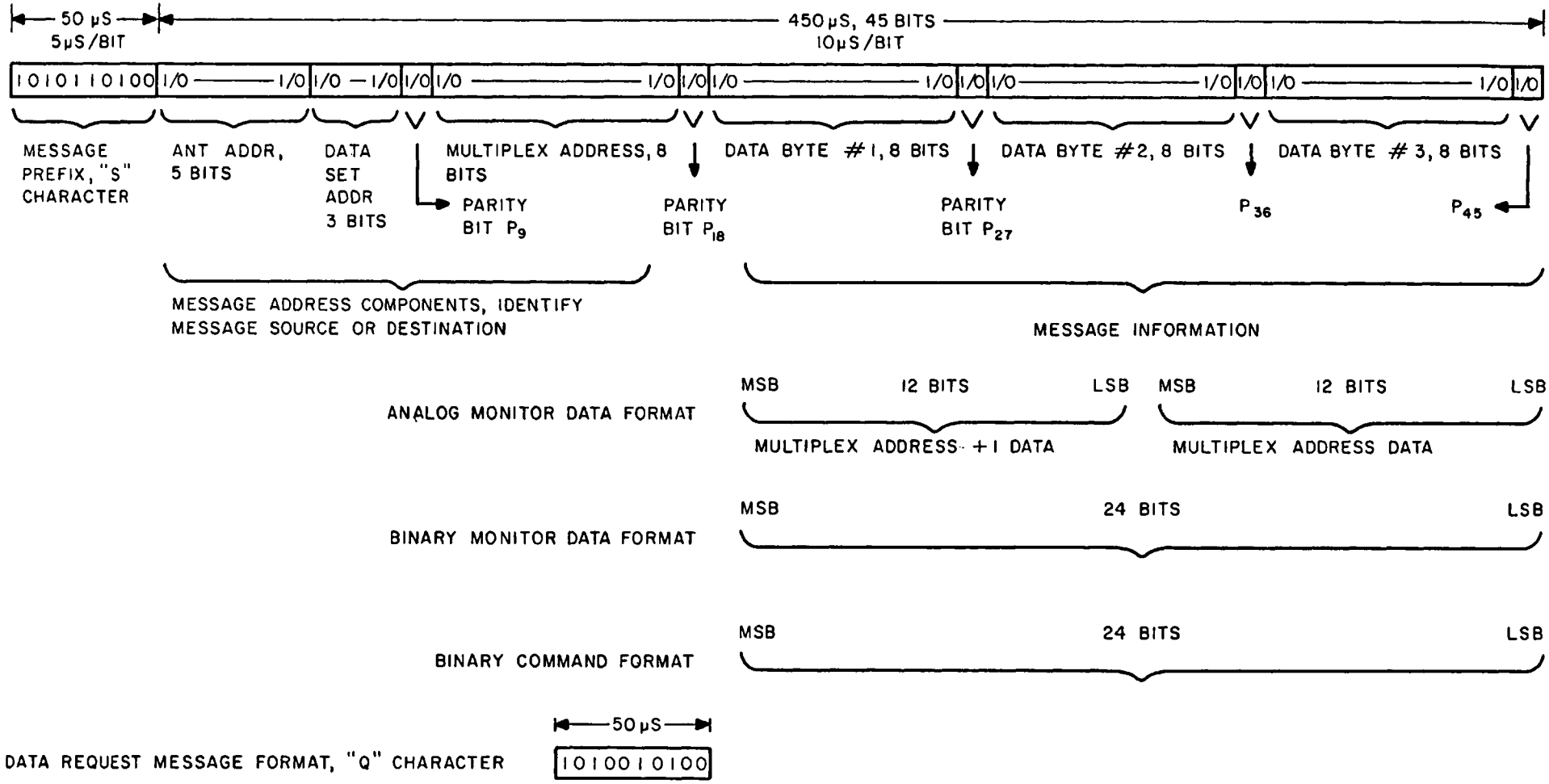


FIGURE 4: DATA SET COMMAND AND MONITOR DATA AND DATA REQUEST MESSAGE FORMATS

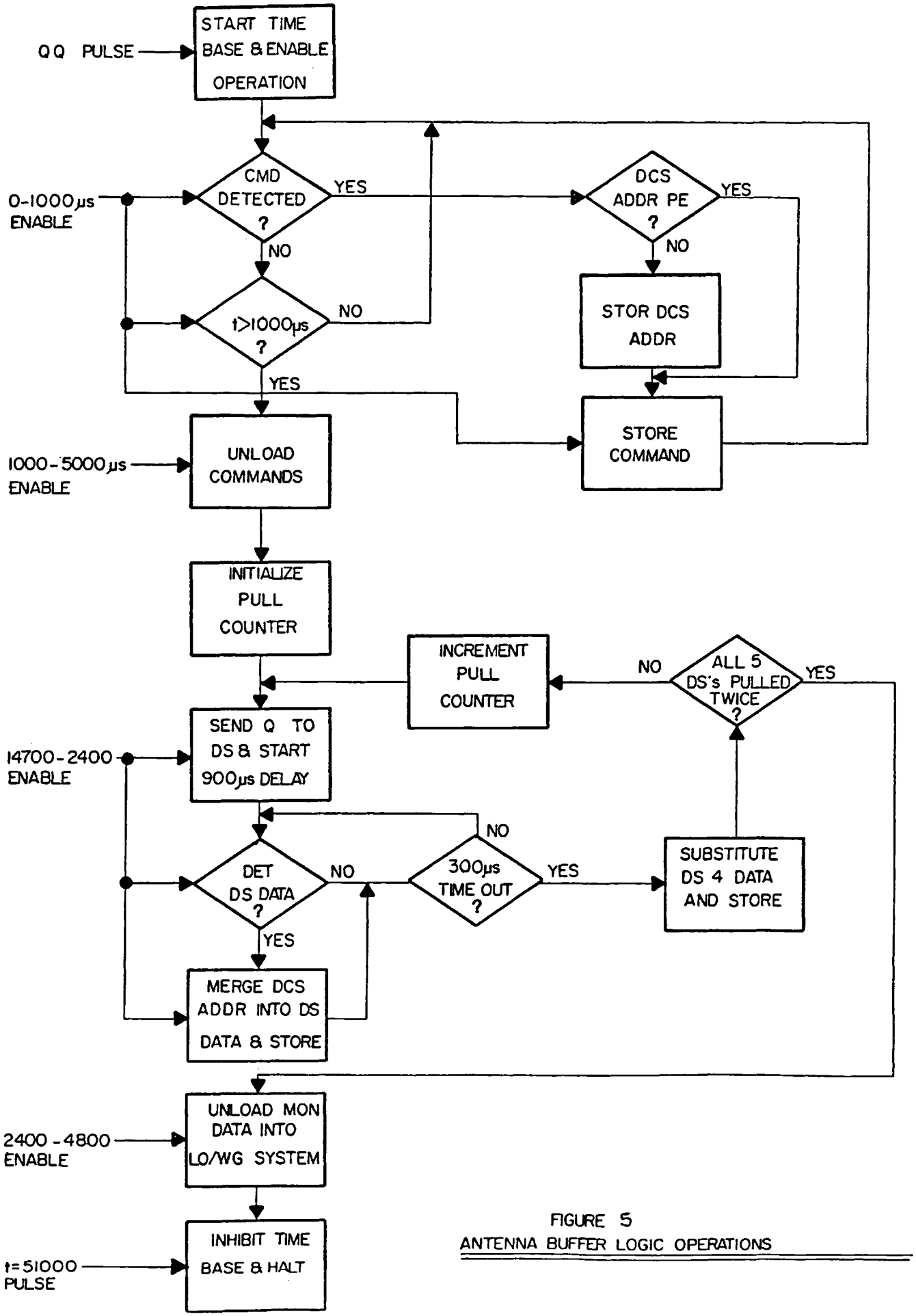


FIGURE 5
ANTENNA BUFFER LOGIC OPERATIONS

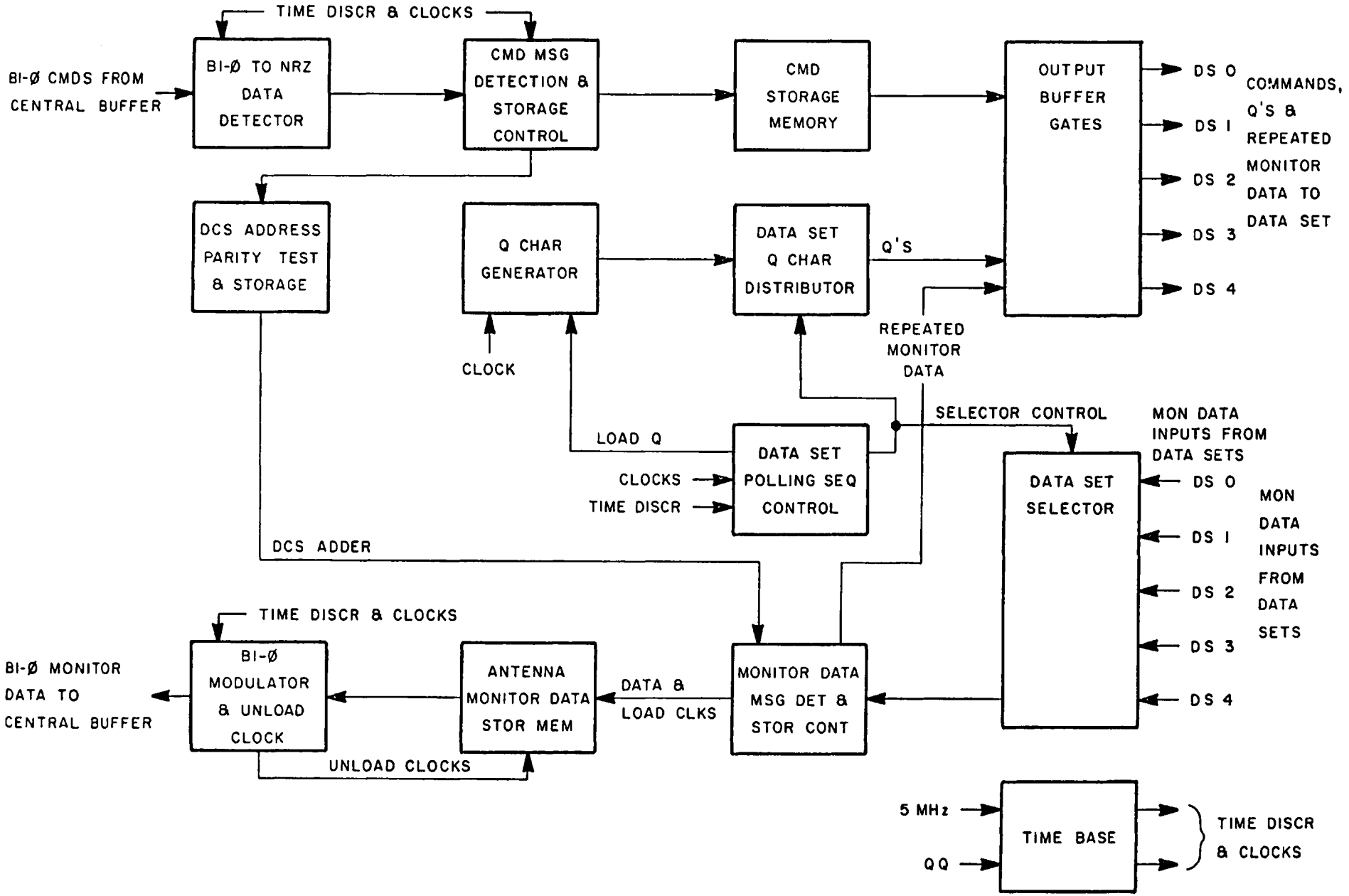
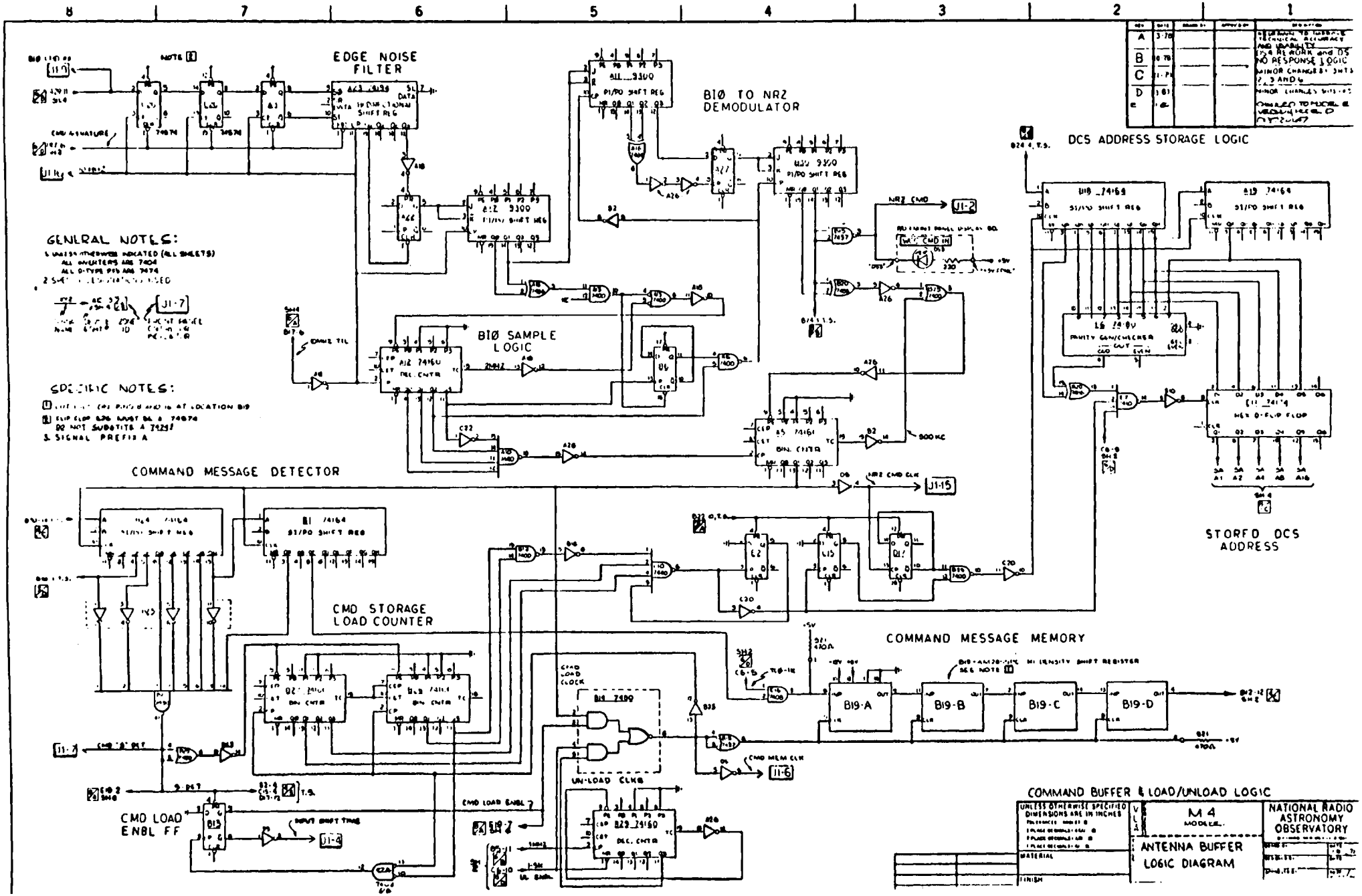
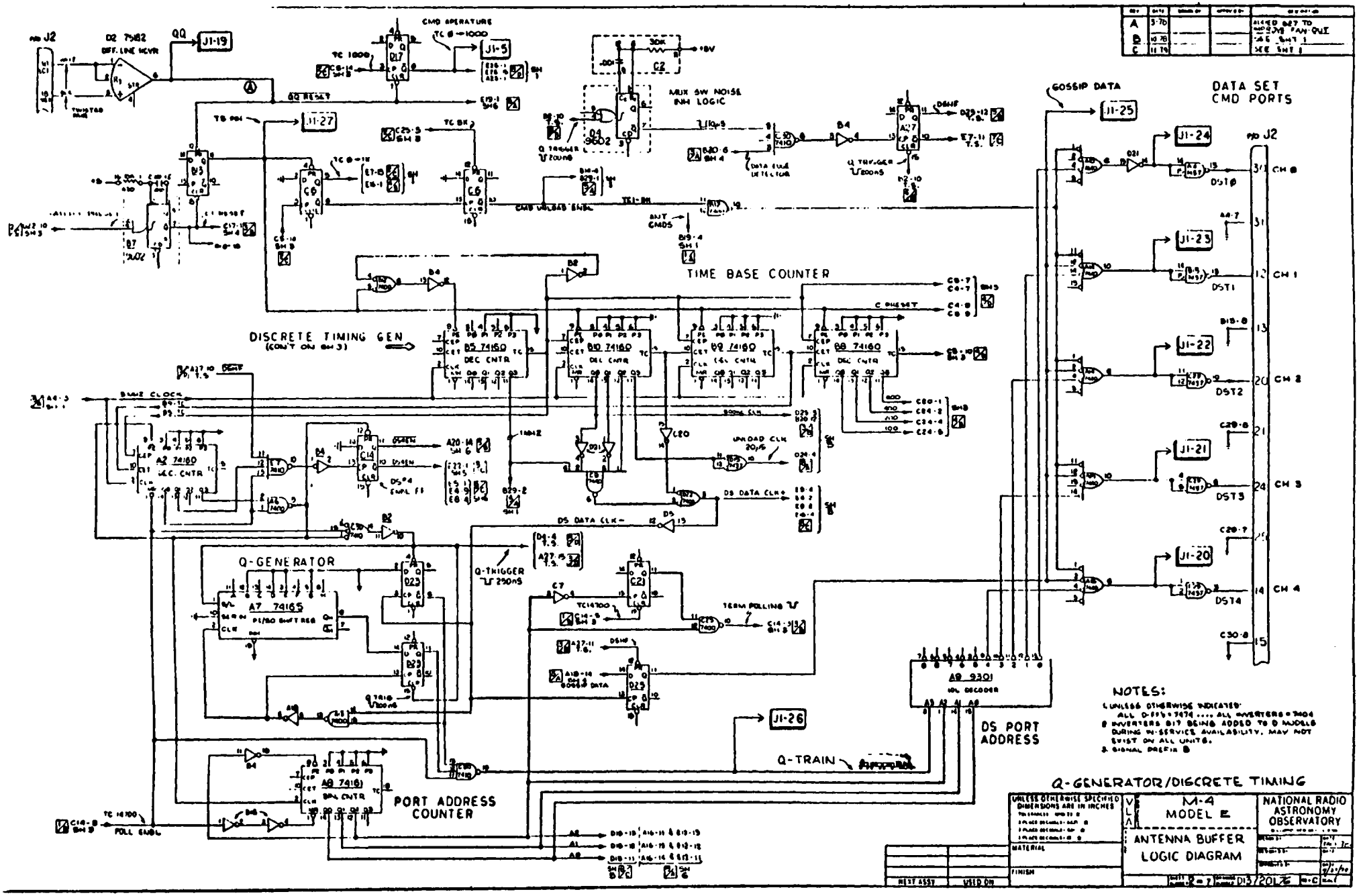
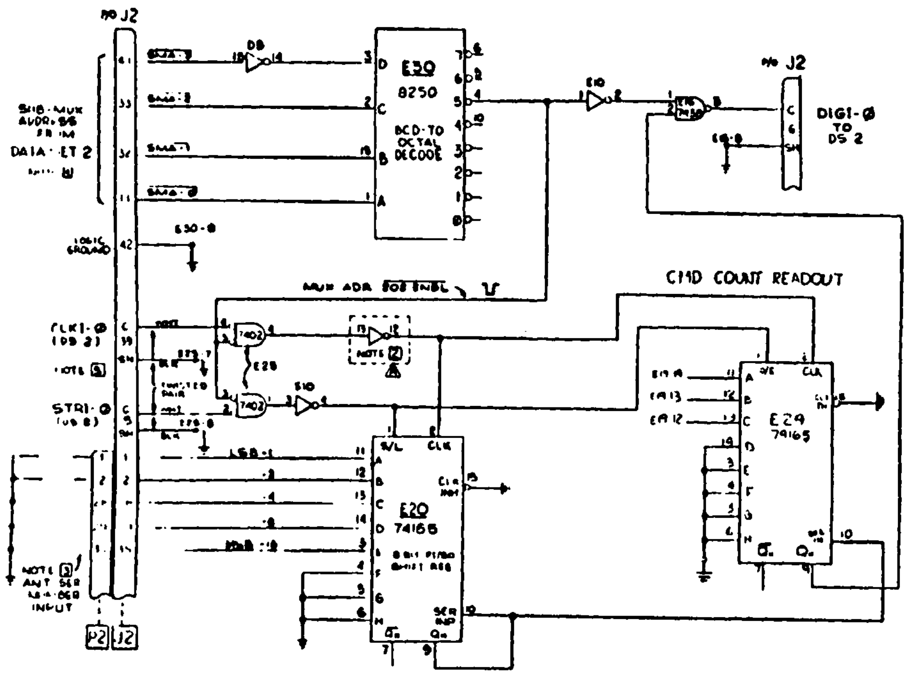


FIGURE 6: ANTENNA BUFFER BLOCK DIAGRAM

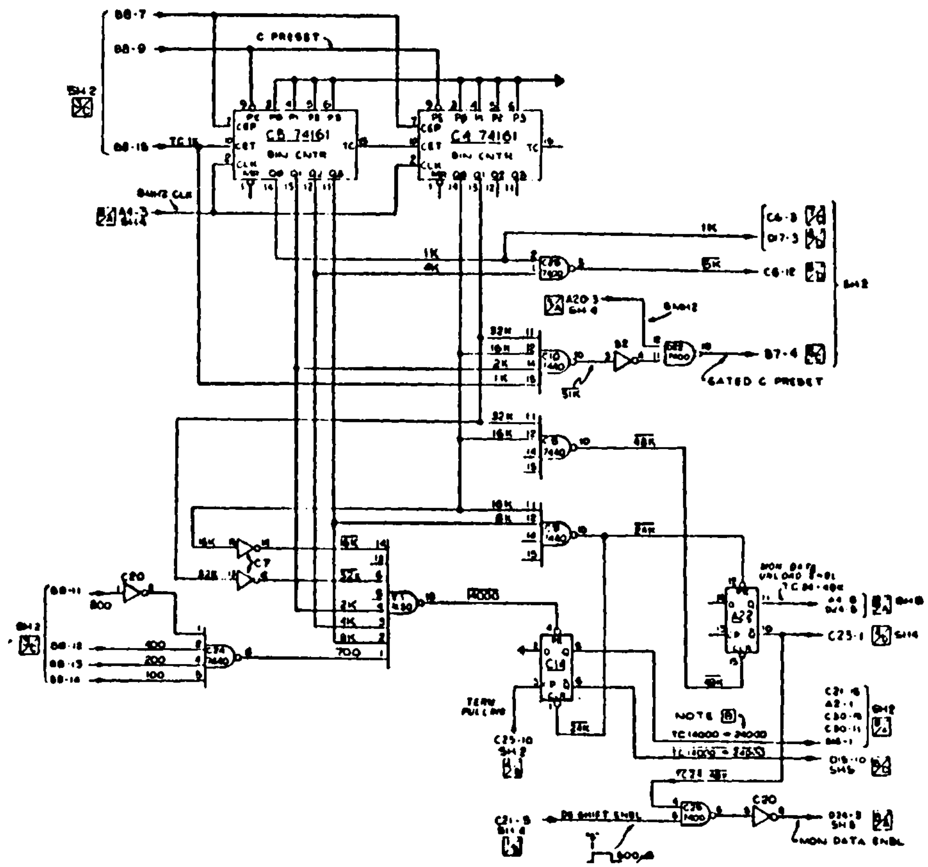

EDGE NOISE FILTER
BIØ TO NRZ DEMODULATOR
DCS ADDRESS STORAGE LOGIC
GENERAL NOTES:
SPECIFIC NOTES:
BIØ SAMPLE LOGIC
COMMAND MESSAGE DETECTOR
CMD STORAGE LOAD COUNTER
COMMAND MESSAGE MEMORY
STORED DCS ADDRESS
CMD LOAD ENBL FF
UNLOAD CLKB
B19-A
B19-B
B19-C
B19-D
COMMAND BUFFER & LOAD/UNLOAD LOGIC
M4
ANTENNA BUFFER LOGIC DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY


TIME BASE COUNTER
DISCRETE TIMING GEN
Q-GENERATOR
PORT ADDRESS COUNTER
DS PORT ADDRESS
Q-TRAIN
GOSSIP DATA
DATA SET CMD PORTS
NOTES:
Q-GENERATOR/DISCRETE TIMING
M-4 MODEL E
ANTENNA BUFFER LOGIC DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY

ANTENNA SER. NO. READOUT LOGIC (DS-2, MUX-202)



DISCRETE TIMING GENERATOR (CONT FM SH 2)



NOTES:

1. UNLESS OTHERWISE INDICATED:
   ALL INVERTERS = 7404
   ALL D-FF'S = 7474

A 2. ~~[struck-through text]~~ 8-2 REV D MODELS

3. ANT. SERIAL NUMBER IS "PROGRAMMED" ON THE 8' MCR CONNECTOR BY GROUNDING PINS WHERE A LOGICAL 'Ø' IS DESIRED (ACTIVE HIGH)

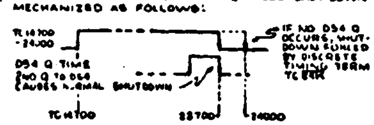
4. DATA SET SIGNALS D-A1-Ø, CLK-Ø, STR1-Ø AND SMA LINES ARE DATA SET 2 ONLY.

5. J2 OMQ LOAN PINS ARE IDENTIFIED BY:
   C ← CENTER PIN
   39 ← A M P PIN-BLOCK DESIG
   SH ← SHIELD (OUTER CONDUCTOR)

6. ANT NO. READBACK ON MUX 202 IN FOLLOWING FORMAT:
   MSB (UOLUCBAODUEDCBAODUEDCBA LSB
   → BITS LOGIC "O" CORRESPONDING TO E20 INPUTS A,B,C,D,E THAT ARE GROUNDED THROUGH P2/J2
   → REDUNDANT (UN-USED BITS)
   SEQUENCE REPEATED 3 TIMES TO ACCOMODATE ALL 24 MON BITS

7. SIGNAL PREFIX - C

6. TERM "TC14700 - 24000" IS A NOMINAL VALUE SHUT-DOWN MECHANIZED AS FOLLOWS:



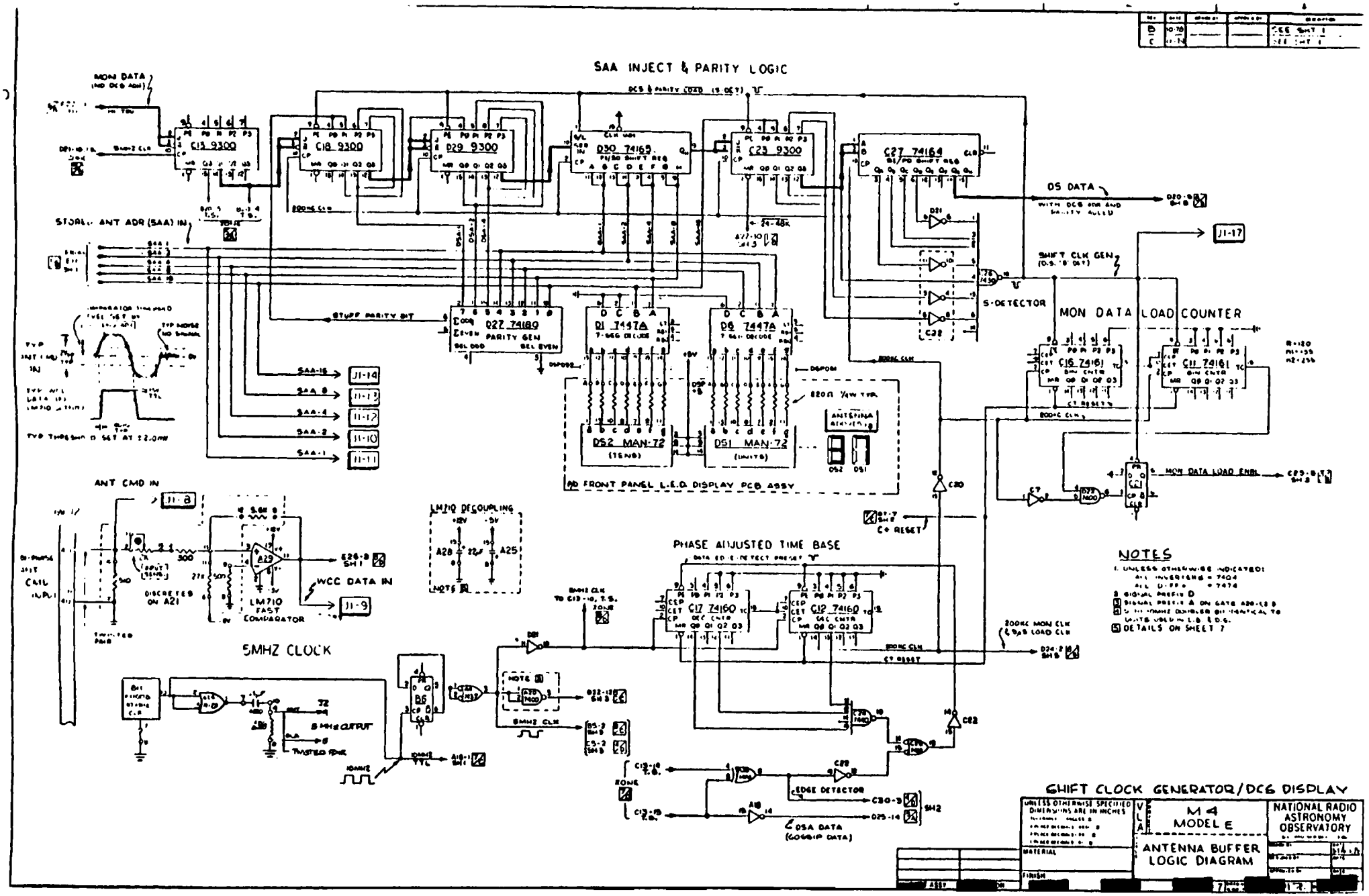
TIMING DISCRETE GEN & ANT S/N LOGIC

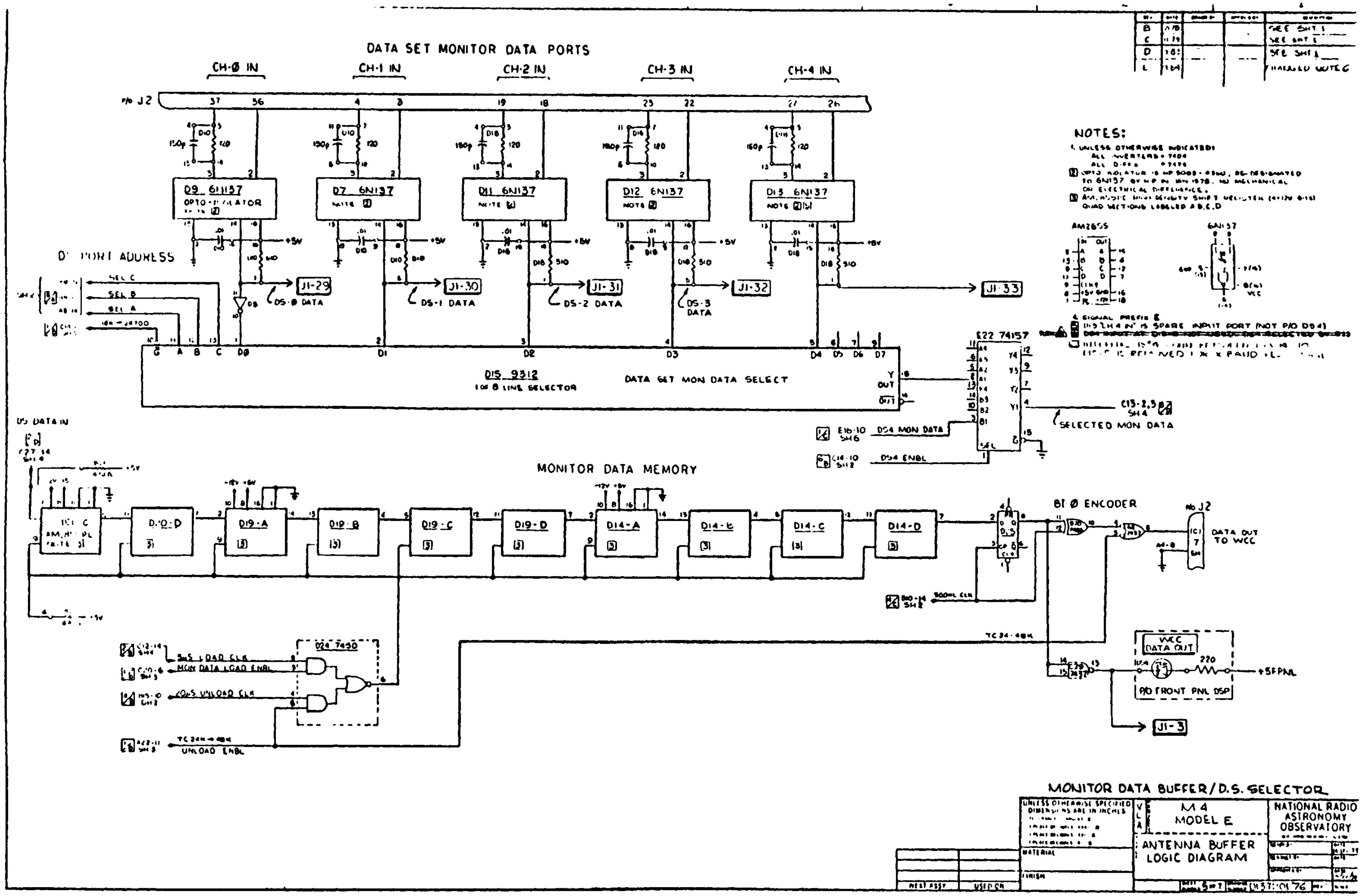
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	VLA
MATERIAL	M 4 MODEL E
FINISH	ANTENNA BUFFER LOGIC DIAGRAM
NEXT ASSY	USED ON

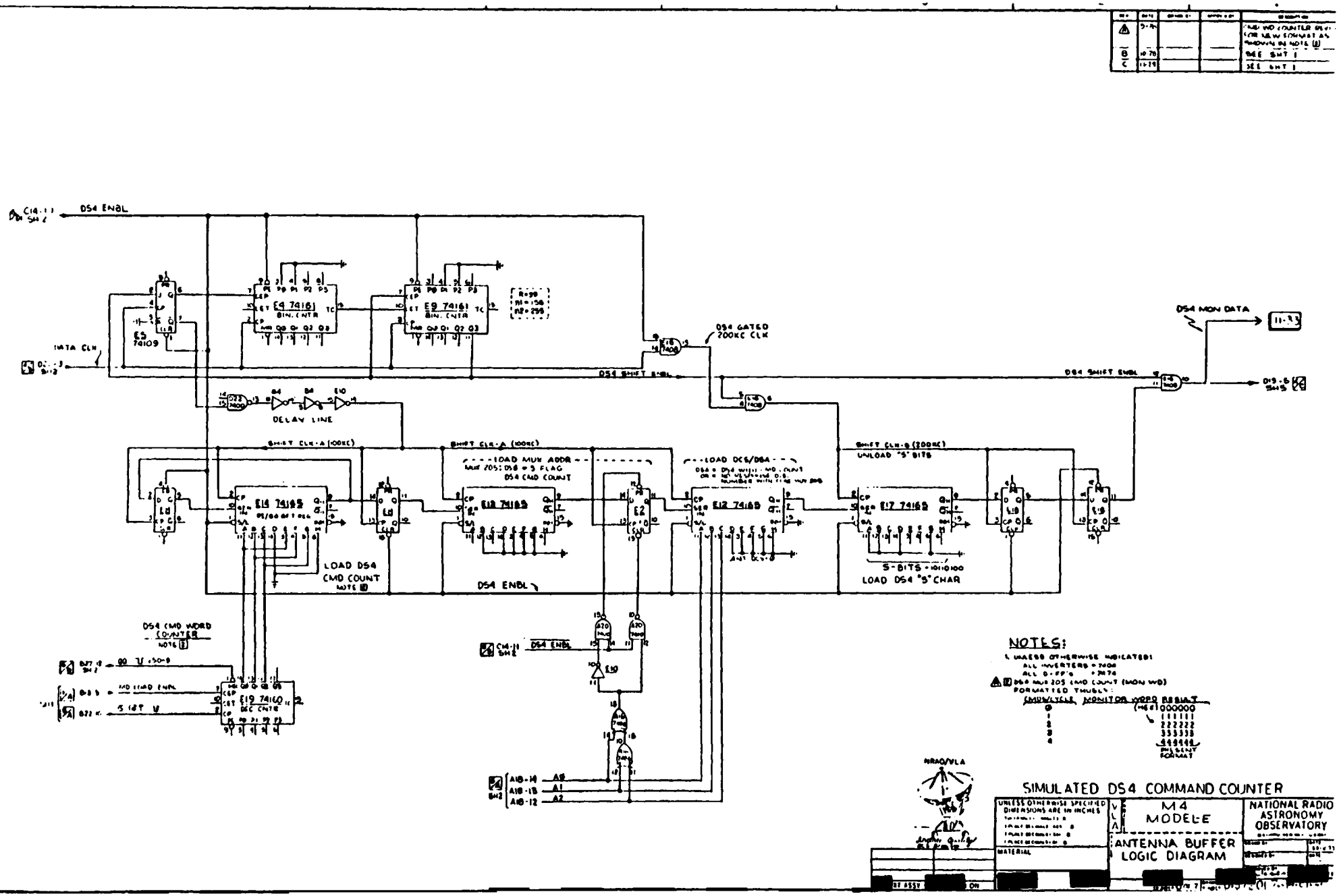
NATIONAL RADIO ASTRONOMY OBSERVATORY

SHEET 3 OF 7 — D13720176 — C

REV D — ADDED E24


SAA INJECT & PARITY LOGIC
MON DATA
C13 9300
C18 9300
D29 9300
D30 74165
C23 9300
C27 74164
DS DATA
STORE ANT ADR (SAA) IN
STUFF PARITY BIT
Q27 74180
PARITY GEN
D1 7447A
D6 7447A
DS2 MAN-72
(TENS)
DS1 MAN-72
(UNITS)
FRONT PANEL L.E.D. DISPLAY PCB ASSY
S-DETECTOR
SHIFT CLK GEN
MON DATA LOAD COUNTER
C16 74161
C11 74161
MON DATA LOAD ENBL
ANT CMD IN
LM710 FAST COMPARATOR
WCC DATA IN
LM710 DECOUPLING
PHASE ADJUSTED TIME BASE
C17 74160
C12 74160
200KC MON CLK & DA LOAD CLK
5MHZ CLOCK
5 MHz OUTPUT
TWISTED PAIR
EDGE DETECTOR
OSA DATA
(GOSSIP DATA)
NOTES
DETAILS ON SHEET 7
SHIFT CLOCK GENERATOR/DCB DISPLAY
M4
MODEL E
ANTENNA BUFFER
LOGIC DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY


DATA SET MONITOR DATA PORTS
CH-Ø IN
CH-1 IN
CH-2 IN
CH-3 IN
CH-4 IN
P/O J2
D9 6N137
OPTO-ISOLATOR
D7 6N137
D11 6N137
D12 6N137
D13 6N137
J1-29
J1-30
J1-31
J1-32
J1-33
DS-Ø DATA
DS-1 DATA
DS-2 DATA
DS-3 DATA
DS PORT ADDRESS
SEL C
SEL B
SEL A
D15 9312
1 OF 8 LINE SELECTOR
DATA SET MON DATA SELECT
E22 74157
SELECTED MON DATA
DS4 MON DATA
DS4 ENBL
DS DATA IN
MONITOR DATA MEMORY
D19-A
D19-B
D19-C
D19-D
D14-A
D14-B
D14-C
D14-D
BI Ø ENCODER
DATA OUT TO WCC
WCC DATA OUT
P/O FRONT PNL DSP
+5FPNL
J1-3
D24 7450
MON DATA LOAD ENBL
UNLOAD ENBL
NOTES:
MONITOR DATA BUFFER/D.S. SELECTOR
M 4
MODEL E
ANTENNA BUFFER
LOGIC DIAGRAM
NATIONAL RADIO
ASTRONOMY
OBSERVATORY



NOTES:

1. UNLESS OTHERWISE INDICATED:
   ALL INVERTERS = 7406
   ALL D-FF'S = 7474
2. DS4 MON DS CMD COUNT (MON WD) FORMATTED THUSLY:

CMD/CYCLE	MONITOR WORD RESULT (HEX)
0	000000
1	111111
2	222222
3	333333
4	444444

RIGHT JUSTIFIED FORMAT

NRAO/VLA

SIMULATED DS4 COMMAND COUNTER

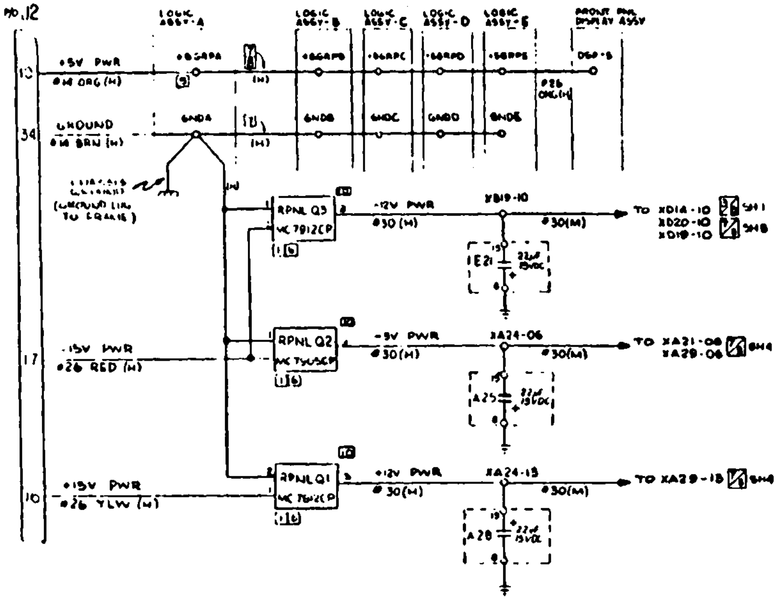
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL

M4 MODELE

ANTENNA BUFFER LOGIC DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY



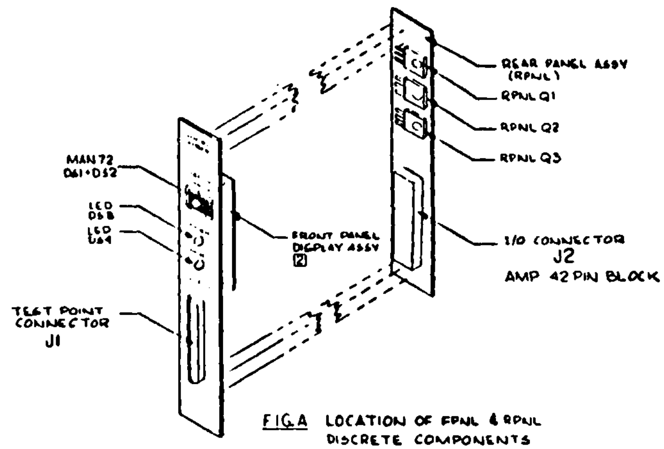


FIG. A LOCATION OF FPNL & RPNL DISCRETE COMPONENTS

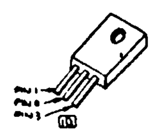
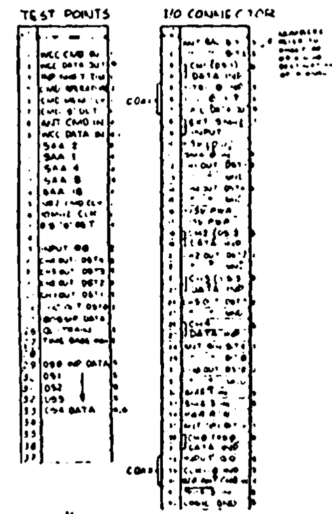
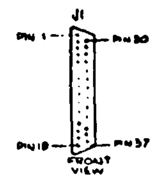


FIG. B IDENTIFICATION OF RPNL Q1 Q2 Q3 PIN TERMINALS



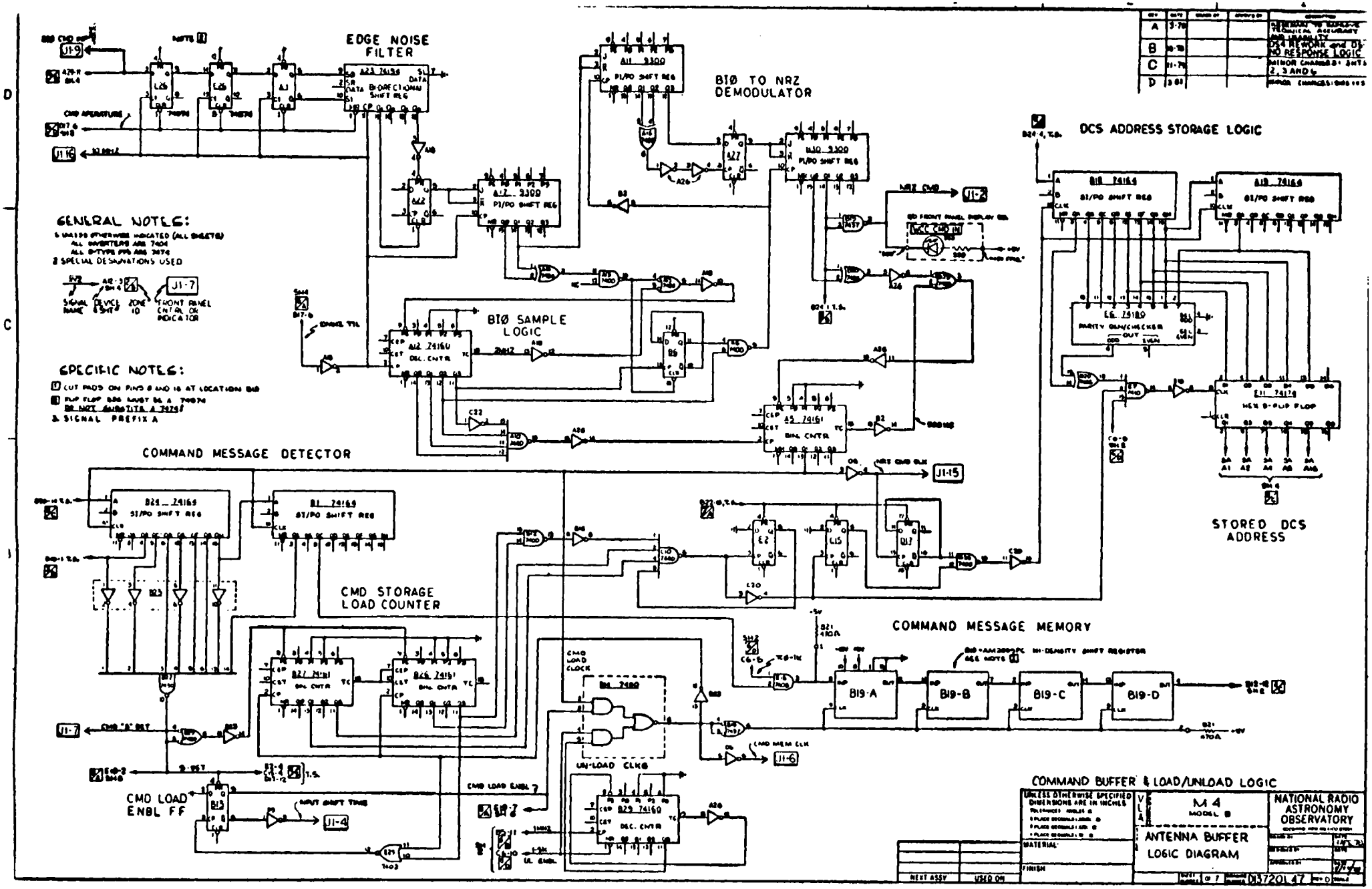


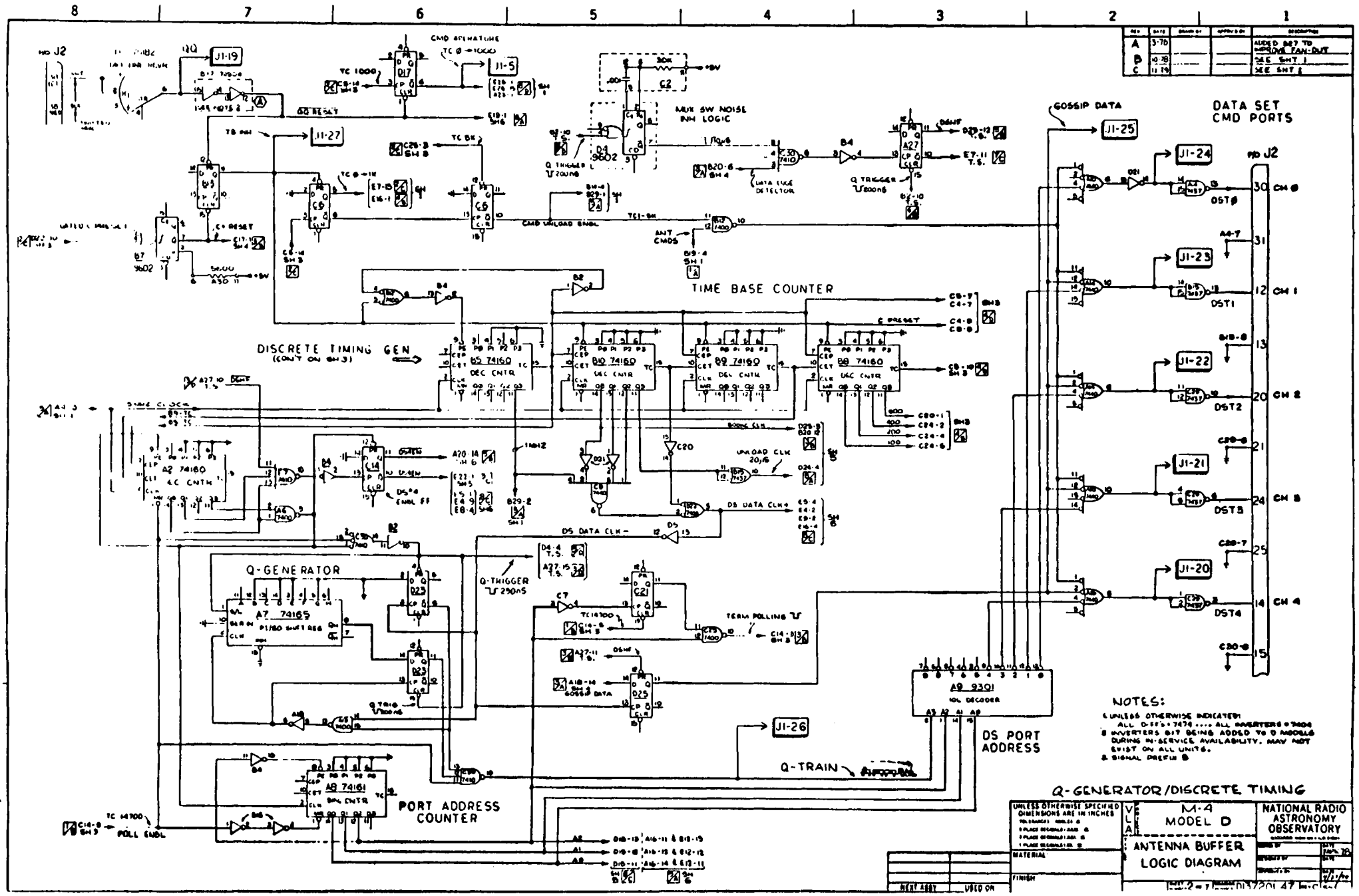
NOTES:

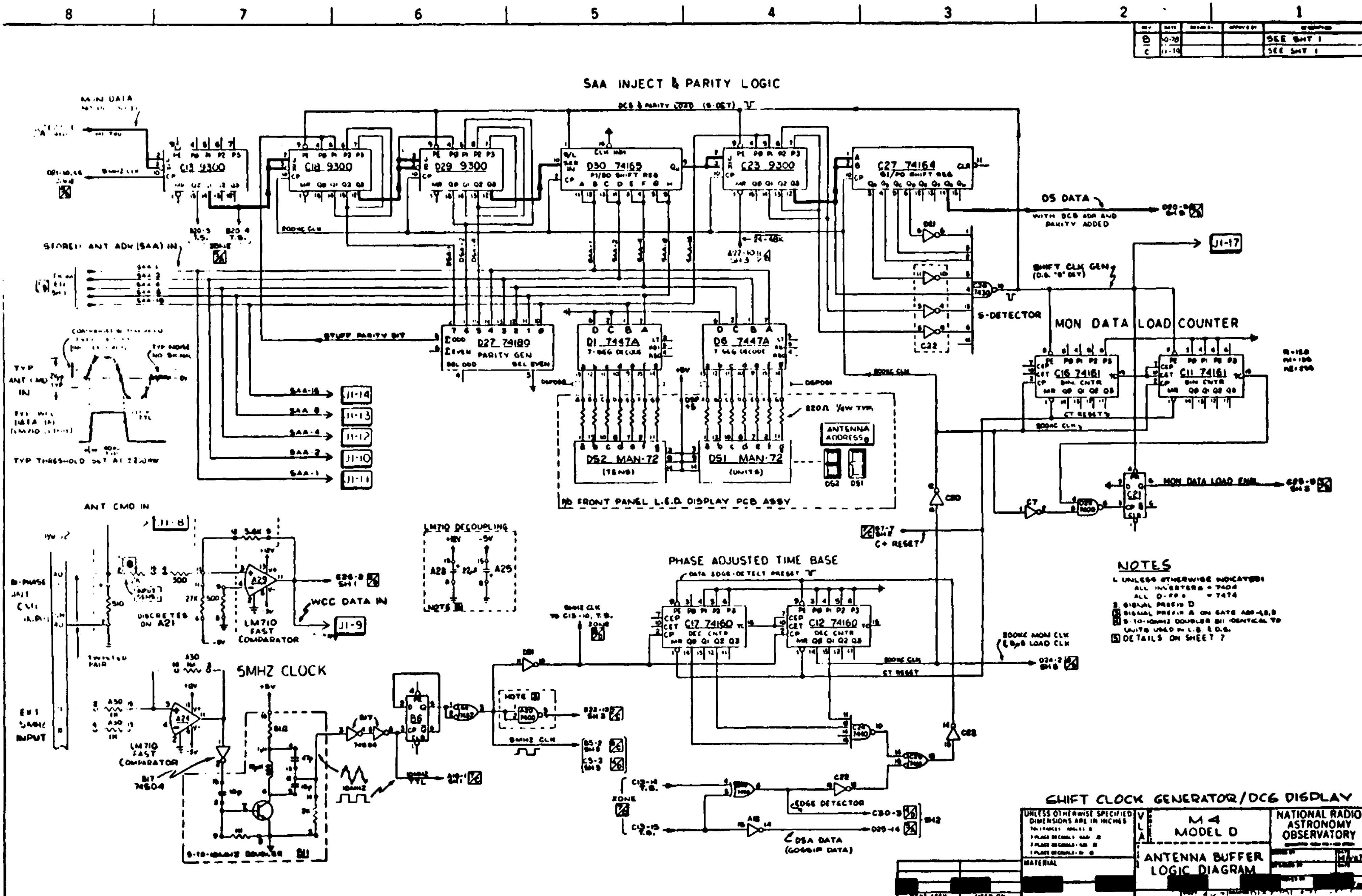
1. VOLT REGULATORS RPNL Q1, RPNL Q2 AND RPNL Q3 ARE MOUNTED ON REAR PANEL. REFER TO FIG A
2. [illegible] INDICATOR ASSY [illegible] C5720 [illegible]
3. THE NOTATION (H) INDICATES HAND WIRING.
4. ANTENNA BUFFER WIRE LIST REFER TO A5720WI
5. NOTATIONS "+5GAPA", "GNDB", ETC. REFER TO LOGIC CONNECTOR BOARD TERMINALS
6. RPNL Q1 THRU RPNL Q3 TERMINALS IDENTIFIED IN FIG B.
7. THE "+5V PWR" BUSS AND "GROUND" BUSS LEADS ARE TO BE ROUTED AND SLEEVED AS PER NRAO DWG [illegible]. THE BUSS LEADS SHALL EACH BE A CONTINUOUS PIECE OF BUSS WIRE THRU THEIR (6) RESPECTIVE TERMINALS.
8. THE [illegible] IS FILTERED AT THE FOLLOWING LOCATIONS WITH THE DIP HEADER INDICATED:
   [illegible]
9. THIS DWG FORMERLY C-5720 [illegible] FOR ANTENNA BUFFERS MODELS A.B.C. MERGED WITH LOGIC DIAGRAM DWGS ON MODEL D.
10. [illegible] FOR THE MOTOROLA [illegible] WHEN NON MOTOROLA [illegible] ARE USED [illegible] THESE OTHER DEVICES.

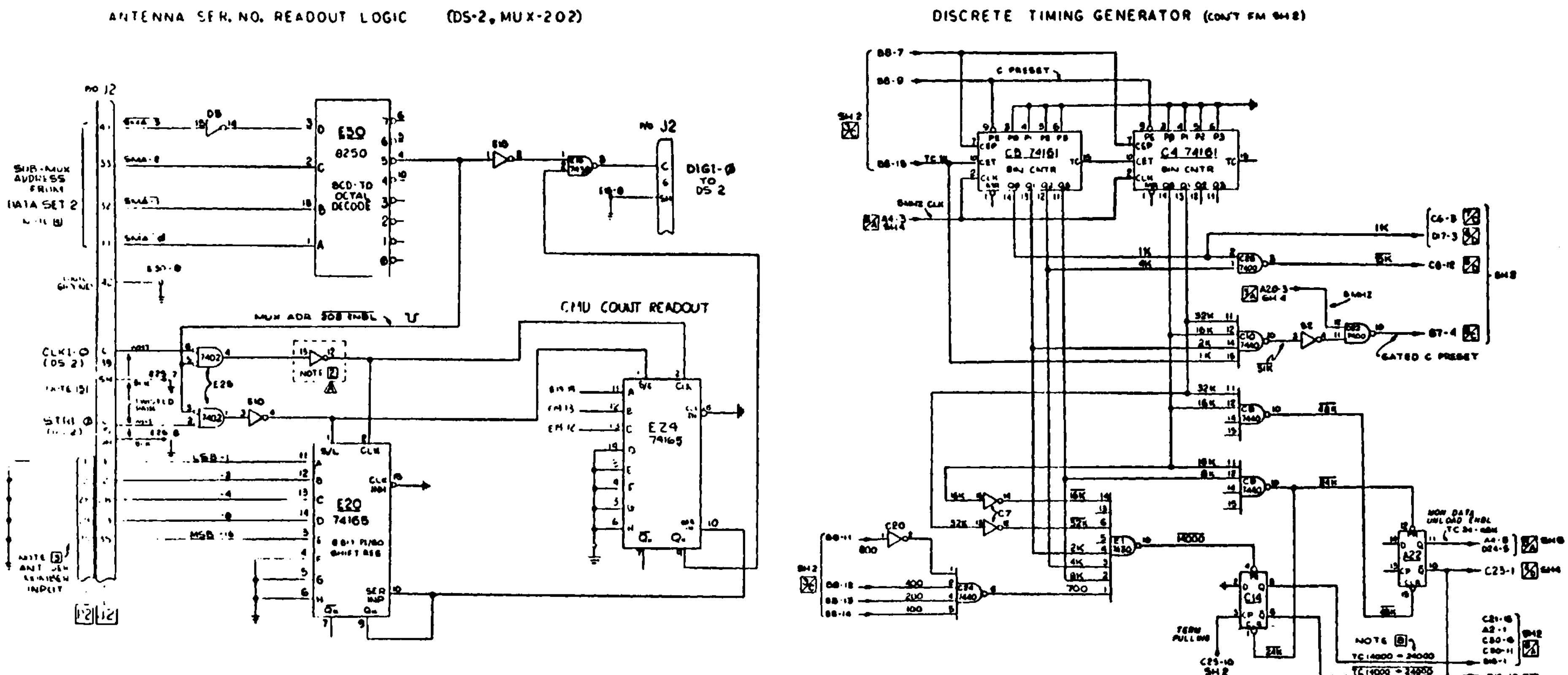
POWER WIRING/J1 & J2 CONNECTOR DETAILS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	VLA M4 MODEL-E	NATIONAL RADIO ASTRONOMY OBSERVATORY
MATERIAL	ANTENNA BUFFER LOGIC DIAGRAM	
FINISH		


EDGE NOISE FILTER
BIØ TO NRZ DEMODULATOR
DCS ADDRESS STORAGE LOGIC
GENERAL NOTES:
SPECIFIC NOTES:
BIØ SAMPLE LOGIC
COMMAND MESSAGE DETECTOR
CMD STORAGE LOAD COUNTER
COMMAND MESSAGE MEMORY
STORED DCS ADDRESS
CMD LOAD ENBL FF
UN-LOAD CLKØ
COMMAND BUFFER & LOAD/UNLOAD LOGIC
ANTENNA BUFFER LOGIC DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY
M4
MODEL B
D37201 47

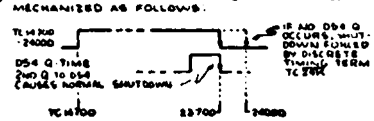

TIME BASE COUNTER
DISCRETE TIMING GEN
Q-GENERATOR
PORT ADDRESS COUNTER
DS PORT ADDRESS
Q-TRAIN
GOSSIP DATA
DATA SET CMD PORTS
NOTES:
Q-GENERATOR/DISCRETE TIMING
M-4 MODEL D
ANTENNA BUFFER LOGIC DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY


SAA INJECT & PARITY LOGIC
C13 9300
C18 9300
D29 9300
D30 74165
C23 9300
C27 74164
DS DATA
WITH DCS ADR AND PARITY ADDED
STORED ANT ADR (SAA) IN
SHIFT CLK GEN
S-DETECTOR
MON DATA LOAD COUNTER
C16 74161
C11 74161
D27 74180
PARITY GEN
STUFF PARITY BIT
D1 7447A
D6 7447A
7-SEG DECODE
220Ω 1/4W TYP.
ANTENNA ADDRESS
DS2 MAN-72
(TENS)
DS1 MAN-72
(UNITS)
DS2
DS1
FRONT PANEL L.E.D. DISPLAY PCB ASSY
J1-14
J1-13
J1-12
J1-10
J1-11
J1-17
SAA-16
SAA-8
SAA-4
SAA-2
SAA-1
TYP THRESHOLD SET AT ±200mV
ANT CMD IN
J1-8
LM710 FAST COMPARATOR
WCC DATA IN
J1-9
DISCRETES ON A21
LM710 DECOUPLING
MON DATA LOAD ENBL
C+ RESET
PHASE ADJUSTED TIME BASE
DATA EDGE-DETECT PRESET
C17 74160
C12 74160
DEC CNTR
200KC MON CLK & P/S LOAD CLK
CT RESET
5MHZ CLOCK
EXT 5MHZ INPUT
5MHZ CLK
10MHZ TTL
5-10-10MHZ DOUBLER
EDGE DETECTOR
DSA DATA (GOSSIP DATA)
NOTES
1. UNLESS OTHERWISE INDICATED: ALL INVERTERS = 7404, ALL D-FF'S = 7474
2. SIGNAL PREFIX D
3. SIGNAL PREFIX A ON GATE A20-A25
4. 5-10-10MHZ DOUBLER BU IDENTICAL TO UNITS USED IN L.E.D.
5. DETAILS ON SHEET 7
SHIFT CLOCK GENERATOR/DCS DISPLAY
M4 MODEL D
NATIONAL RADIO ASTRONOMY OBSERVATORY
ANTENNA BUFFER LOGIC DIAGRAM
SEE SHT 1
SEE SHT 1



NOTES:

1. UNLESS OTHERWISE INDICATED: ALL INVERTERS = 7404, ALL D-FF's = 7474
2. B-3 REV D MODELS
3. ANT. SERIAL NUMBER IS "PROGRAMMED" ON THE B RACK CONNECTOR BY GROUNDING PINS WHERE A LOGICAL 'Ø' IS DESIRED (ACTIVE HIGH)
4. DATA SET SIGNALS DIGI-Ø, CLK-Ø, STR-Ø AND SMA LINES ARE DATA SET 2 ONLY.
5. J2 DMQ LOAK PINS ARE IDENTIFIED BY:
   - C — CENTER PIN
   - 5S — AMP MINI-BLOCK DESIG
   - SH — SHIELD (OUTER CONDUCTOR)
6. ANT NO. READBACK IN MUX 202 IN FOLLOWING FORMAT: MSB [illegible] LSB
   - BITS LOGIC 'O' CORRESPONDING TO E20 INPUTS A,B,C,D,E THAT ARE GROUNDED THROUGH P2/J2
   - REDUNDANT (UN-USED BITS)
   - SEQUENCE REPEATED 3 TIMES TO ACCOMODATE ALL 24 MON BITS
7. SIGNAL [illegible] - C
8. TERM "TC14700-24000" IS A NOMINAL VALUE SHUT-DOWN MECHANIZED AS FOLLOWS:



TIMING DISCRETE GEN & ANT S/N LOGIC

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL

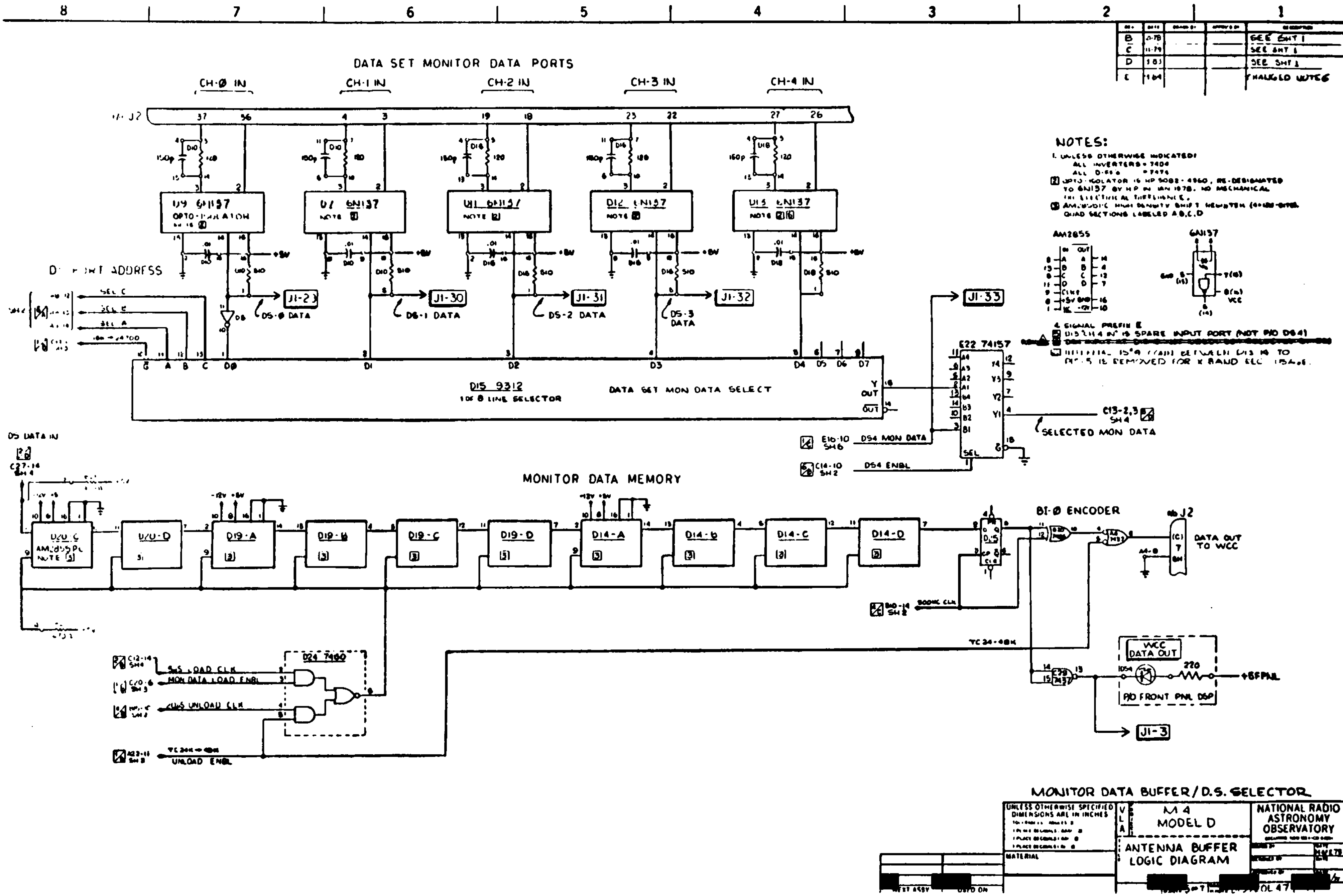
FINISH

VLA

M4 MODEL D

ANTENNA BUFFER LOGIC DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY



MONITOR DATA BUFFER/D.S. SELECTOR

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

V L A

M 4 MODEL D

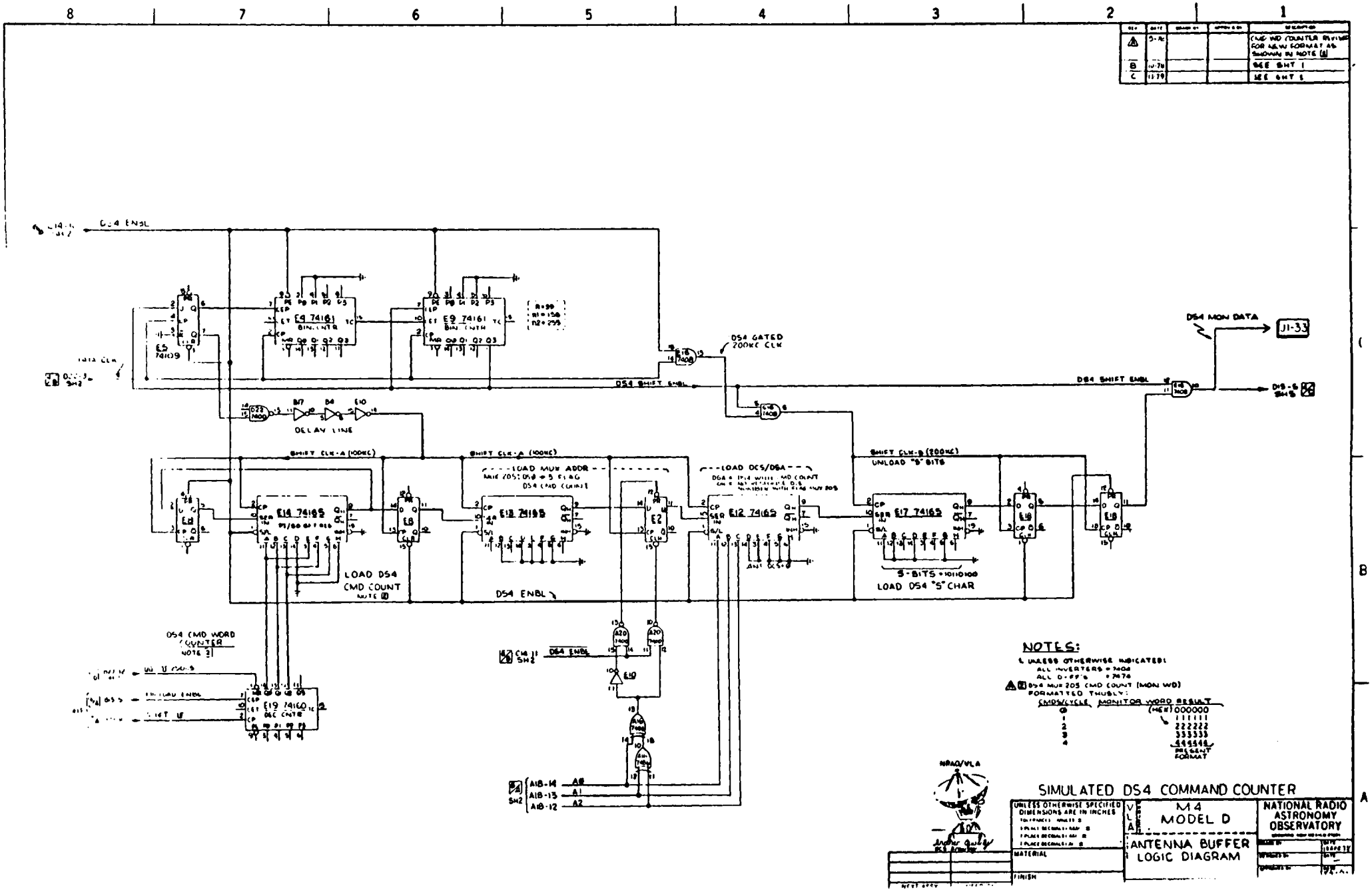
NATIONAL RADIO ASTRONOMY OBSERVATORY

MATERIAL

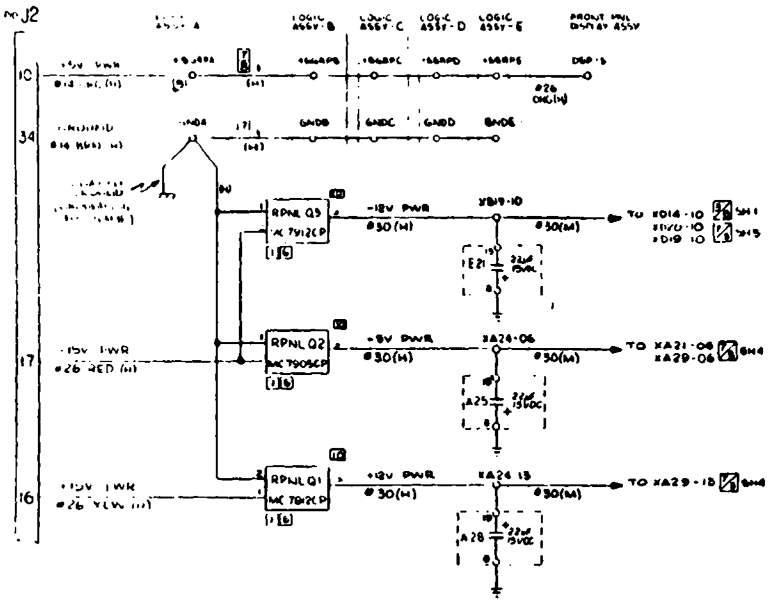
ANTENNA BUFFER LOGIC DIAGRAM

[redacted] NEXT ASSY [redacted] USED ON

[redacted] 5 of 7 [redacted] OL 47 [redacted]


DS4 ENBL
DS4 GATED 200KC CLK
DS4 SHIFT ENBL
DS4 MON DATA
J1-33
DELAY LINE
SHIFT CLK-A (100KC)
SHIFT CLK-B (200KC)
UNLOAD "B" BITS
LOAD MUX ADDR
DS4 CMD COUNT
LOAD DCS/DSA
LOAD DS4 CMD COUNT
LOAD DS4 "S" CHAR
S-BITS = 10110100
DS4 CMD WORD COUNTER
NOTES:
UNLESS OTHERWISE INDICATED:
ALL INVERTERS = 7404
DS4 MUX ADS CMD COUNT (MON WD) FORMATTED THUSLY:
CMDS/CYCLE
MONITOR WORD RESULT
(HEX)
0 000000
1 111111
2 222222
3 333333
4 444444
PRESENT FORMAT
NRAO/VLA
SIMULATED DS4 COMMAND COUNTER
M4
MODEL D
ANTENNA BUFFER
LOGIC DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY
MATERIAL
FINISH

REV	DATE			DESCRIPTION
A	[illegible]			SEE NOTE 9 AND ADDED ADDITIONAL INFORMATION [illegible] SHT 1
B	[illegible]			
C	11-79			SEE SHT 1



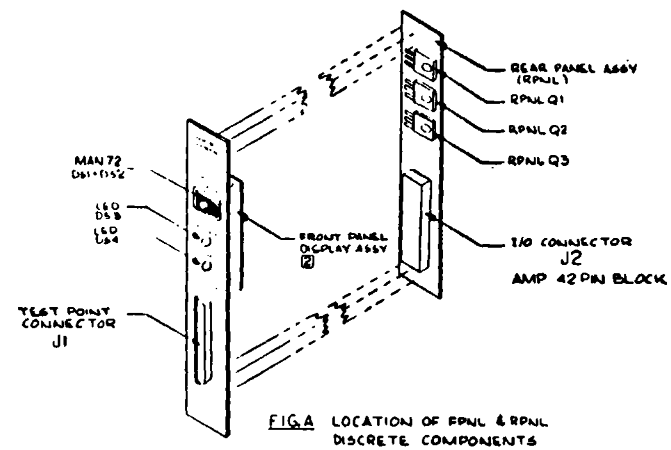


FIG. A LOCATION OF RPNL & RPNL DISCRETE COMPONENTS

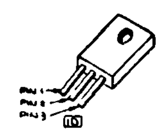
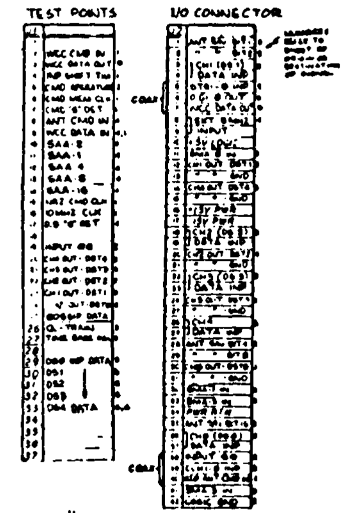
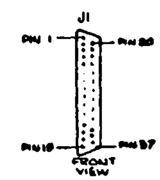


FIG. B IDENTIFICATION OF RPNL Q1 - Q3 PIN TERMINALS





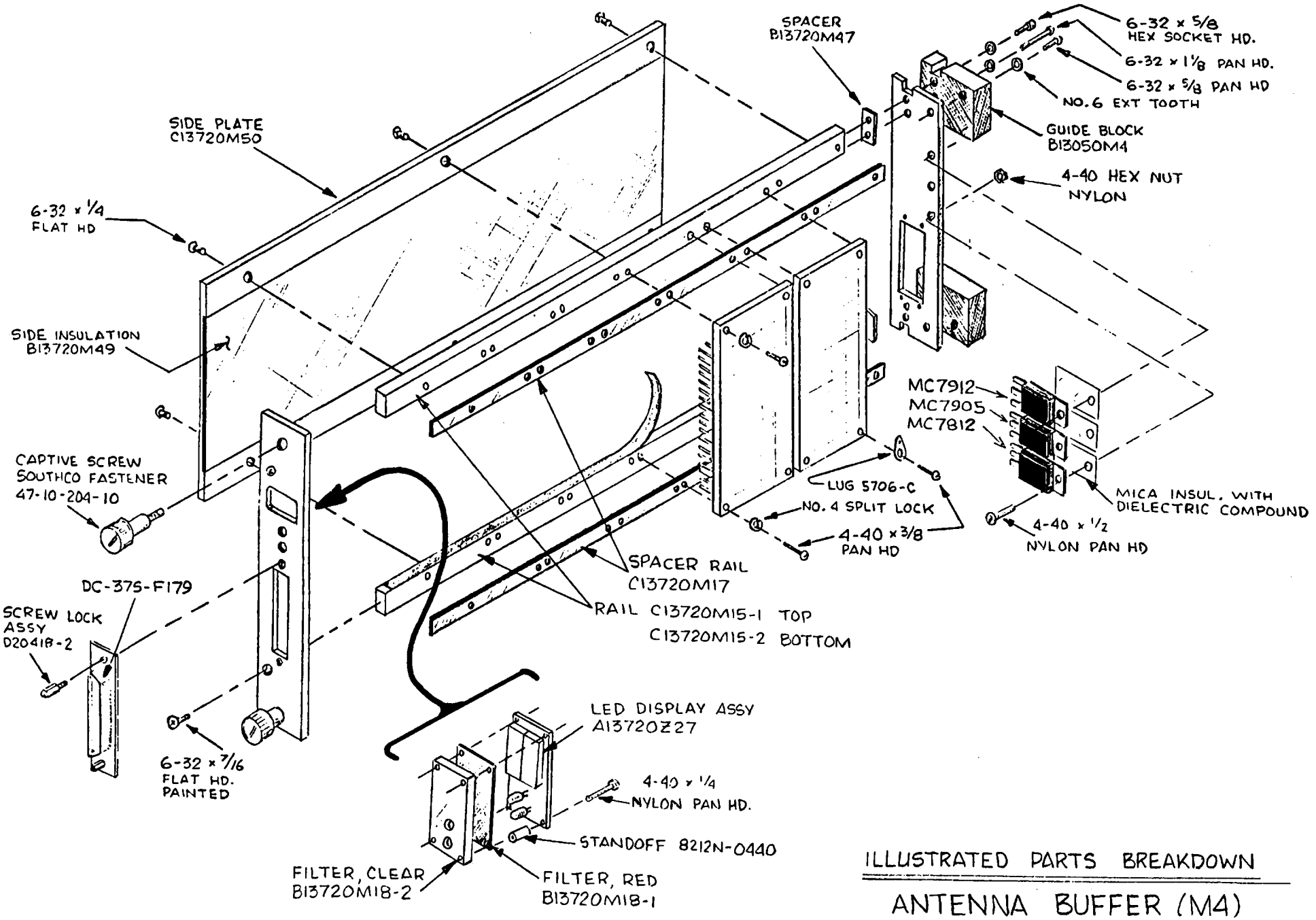
NOTES:

1. VOLT REGULATORS RPNL Q1, RPNL Q2 AND RPNL Q3 ARE MOUNTED ON REAR PANEL. REFER TO FIG A
2. FRONT PANEL NUMERIC INDICATOR ASSY (NRAO DWG C13720S3) REF DESIG IS A1
3. THE NOTATION (H) INDICATES HAND WIRING.
4. ANTENNA BUFFER WIRE LIST REFER TO A13720W19
5. NOTATIONS [illegible] GNDB, ETC, REFER TO LOGIC CONNECTOR BOARD TERMINALS
6. [illegible] TERMINALS IDENTIFIED IN FIG B
7. THE [illegible] PWR BUSS AND GROUND [illegible] LEADS ARE TO BE ROUTED AND SLEEVED AS PER NRAO DWG D13720P1. THE BUSS LEADS SHALL EACH BE A CONTINUOUS PIECE OF [illegible] WIRE THRU THEIR [illegible] RESPECTIVE TERMINALS.
8. THE [illegible] ARE FILTERED AT THE FOLLOWING LOCATIONS WITH THE DIP HEADER INDICATED:
   B13720P14 - B8, C38, D8, E8
   B13720P16 - A8, B8 C8, D28, E28
   B13720P20 - A28
9. THIS DWG FORMERLY C13720W42 FOR ANTENNA BUFFERS MODELS A B.C. MERGED WITH LOGIC DIAGRAM DWGS ON MODEL D.
10. [illegible] FOR THE MOTOROLA [illegible] NON MOTOROLA [illegible] TO [illegible] OTHER DEVICES.

POWER WIRING/J1 & J2 CONNECTOR DETAILS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	VLA	M4 MODEL D	NATIONAL RADIO ASTRONOMY OBSERVATORY
MATERIAL		ANTENNA BUFFER LOGIC DIAGRAM	

[redacted]



ILLUSTRATED PARTS BREAKDOWN

ANTENNA BUFFER (M4)

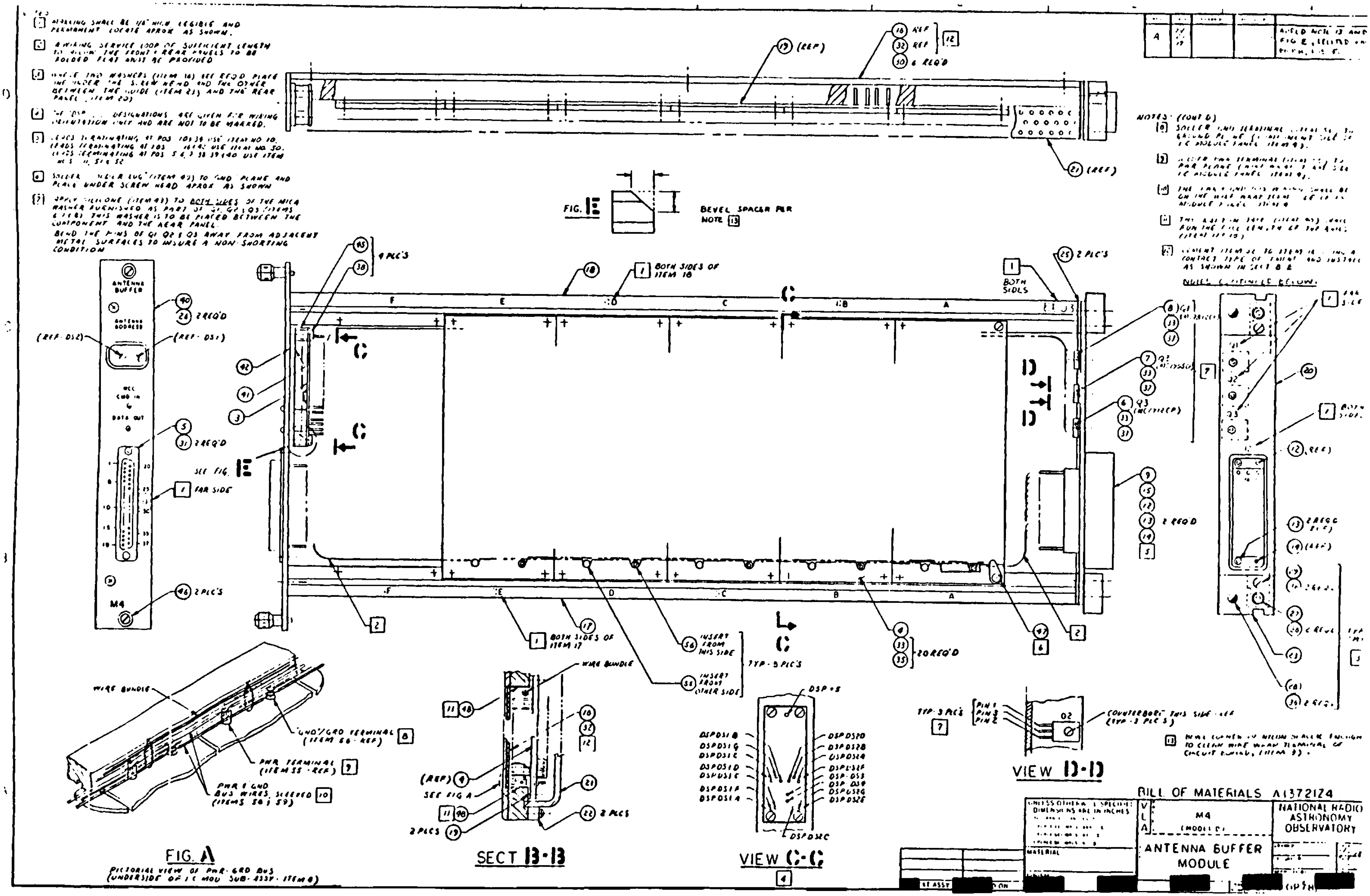


FIG. E
BEVEL SPACER PER NOTE 13
ANTENNA BUFFER
M4
SEE FIG. E
FAR SIDE
BOTH SIDES OF ITEM 18
BOTH SIDES OF ITEM 17
BOTH SIDES
INSERT FROM THIS SIDE
INSERT FROM OTHER SIDE
TYP 5 PLC'S
20 REQ'D
2 REQ'D
2 PLC'S
4 PLC'S
VIEW D-D
FIG. A
PICTORIAL VIEW OF PWR-GRD BUS (UNDERSIDE OF I C MOD SUB-ASSY ITEM 8)
WIRE BUNDLE
GND/GRD TERMINAL (ITEM 56 - REF)
PWR TERMINAL (ITEM 55 - REF)
PWR & GND BUS WIRES, SLEEVED (ITEMS 58 & 59)
SECT B-B
SEE FIG A
VIEW C-C
NOTES (CONT'D)
NOTES CONTINUED BELOW
BILL OF MATERIALS A1372124
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL
M4
ANTENNA BUFFER MODULE
NATIONAL RADIO ASTRONOMY OBSERVATORY

REVISIONS				
REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

DRAWN BY	DATE			
DESIGNED BY	DATE			
APPROVED BY	DATE		NEXT ASSY	USED ON

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLA

PROJECT M4

TITLE ANTENNA BUFFER MODULE

DWG NO. A1372124 SHEET OF

BILL OF RIAL

NATIONAL RADIO ASTR...OMY OBSERVATORY

[XX] ELECTRICAL [ ] MECHANICAL BOM # A1372124 REV _____ DATE _____ PAGE 1 OF 4

MODULE # M4 NAME ANTENNA BUFFER MODULE DWG # D13720P78 SUB ASMB _____ DWG # _____

SCHEMATIC DWG # D13720L47 LOCATION _____ QUA/SYSTEM _____ PREPARED BY R. Runyon APPROVED _____

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
1		N.R.A.O.	A1372124	ANTENNA BUFFER ASS'Y.	-	
2						
3		N.R.A.O.	A13720Z27	L.E.D. DISPLAY SUB-ASS'Y.	1	
4		N.R.A.O.	A1372125	I.C. MODULE PANEL SUB-ASS'Y.	1	
5	J1	CINCH	DC-37S-F179	CONNECTOR, TEST JACK	1	
6	Q3	MOTOROLA	MC7912CP	VOLTAGE REG., - 12V	1	
7	Q2	MOTOROLA	MC7905CP	VOLTAGE REG., -5V	1	
8	Q1	MOTOROLA	MC7812CP	VOLTAGE REG., +12V	1	
9	J2	AMP SPECIAL INDUST.	601488-4	42 PIN MOD. CONN. (PRE-ASM)	1	
10		AMP SPECIAL INDUST.	201570-1 /	CRIMP PIN	2	
11		AMP SPECIAL INDUST.	201143-5	COAX CONN.	6	
12		AMP SPECIAL INDUST.	200833-4	GUIDE PIN	1	
13		AMP. SPECIAL INDUST.	203964-6	GUIDE SOCKET	2	
14		AMP SPECIAL INDUST.	202514-1	GROUND GUIDE PIN	1	
15		AMP SPECIAL INDUST.	202394-2	CONN. SHIELD	2	

BILL OF MA \L

NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☒ MECHANICAL BOM # A1372124 REV _____ DATE _____ PAGE 2 OF 4

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
16		N.R.A.O.	C13720M50	SIDE PLATE	1	
17		N.R.A.O.	C13720M15-1	RAIL, MODIFIED	1	
18		N.R.A.O.	C13720M15-2	RAIL, MODIFIED	1	
19		N.R.A.O.	C13720M17	RAIL, SPACER	2	
20		N.R.A.O.	C13720M23	REAR PANEL	1	
21		N.R.A.O.	C13050M7	PERFORATED COVER	1	
22		N.R.A.O.	B13050M17	COVER MT'G. HDWRE.	2	
23		N.R.A.O.	B13050M4	GUIDE	2	
24			~~.003 THK. MYLAR~~	~~INSUL. SHIELD, 5 1/2 in x 19 in~~	~~1~~	
25		N.R.A.O.	B13720M47	SPACER	2	
26			#6-32x1/4 in	ST. ST'L., CR. REC., FL'T. HD. MACH. SCR.	2	
27			#6-32x3/8 in	ST. ST'L., HEX SOC. HD. CAP SCR.	2	
28			#6-32x 1 in	ST. ST'L., PAN HD., SLOTTED, MACH.SCR.	2	
29			#6-32x3/4 in	ST. ST'L., PAN HD., SLOTTED, MACH.SCR.	2	
30			#6-32x1/4 in	ST. ST'L., FL'T. HD., SLOTTED, MACH.SCR.	6	
31		CINCH	D20418-2	SCREW LOCK ASS'Y (FEMALE)	2	
32		N.R.A.O.	B13720M49	PANEL, SIDE, INSULATION	1	

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

[ ] ELECTRICAL [XX] MECHANICAL BOM # A13721Z4 REV _____ DATE _____ PAGE 3 4

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
33			#4-40x3/8in	ST.ST'L., PAN HD.,SLOTTED,MACH.SCR	27	
34						
35			#4 NOM.	ST.ST'L. INT. TOOTH LK. WASHER	24	
36			#6	WASHER, EXT. TOOTH, ST. ST'L	12	
37			#4-40	SELF LOCKING, NYLON HEX NUT	3	
38			#4-40x1/4in	NYLON, PAN HD. SLOTTED SCR.	4	
39		N.R.A.O.	C13720M16	FRONT PANEL (MACHINED)	REF	
40		N.R.A.O.	B13720M19	FRONT PANEL (ENGRAVED)	1	
41		N.R.A.O.	B13720M18-1	FRONT PANEL FILTER (RED)	1	
42		N.R.A.O.	B13720M18-2	FRONT PANEL FILTER (CLR.)	1	
43						
44		PEM FASTENERS	FHS-440-6	THREADED STUD	4	
45		AMATOM	8212-N-0440	Threaded Standoff (NYLON-4-40x5/16)	4	
46		SOUTHCO	47-10-204-10	CAPTIVE SCREW	2	
47		G.C. ELECTRONICS	5706-C	GROUND LUG	1	
48		CONN. HARD RUBBER CO.	TYPE K350	KAPTON TEMP. -R-TAPE(32/64"WIDE)	38"	
49		G.E.	INSULGREASE G641	SILICONE DIELECTRIC COMPOUND	A/R.	

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☒ MECHANICAL BOM # A13721Z4 REV _____ DATE _____ PAGE 4 OF 4

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA
50		AMP SPECIAL INDUST.	201578-1	CRIMP PIN	3
51		AMP SPECIAL INDUST.	328666	FERRULE	6
52		AMP SPECIAL INDUST.	201142-2	RETENTION SPRING	6
53					
54					
55		H. H. SMITH	2010	TERMINAL (SPLIT LUG)	6
56		H. H. SMITH	2025	TERMINAL (MIN. THROUGH)	6
57					
58		ALPHA	286	BUS BAR	A/R
59		ALPHA	TFT-200/13(NAT)	TEFLON EXTRUDED TUBING	A/R
60					
61					
62		N.R.A.O.	A13720W16	WIRE LIST - MASTER	-
63		N.R.A.O.	A13720W18	WIRE LIST - HAND	-
64		N.R.A.O.	A13720W17	WIRE LIST - MACHINE	-
65		N.R.A.O.	A13720W49	WIRE LIST - CONNECTOR	-
66		N.R.A.O.	A13720W42	WIRE LIST - POWER	-

REVISIONS

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
B	2-9-79			REDRAWN WAS C13720PT9

DRAWN BY	DATE			M4
DESIGNED BY	DATE			
APPROVED BY	DATE			D13720P78
			NEXT ASSY	USED ON

BILL OF MATERIALS: A13720Z5

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

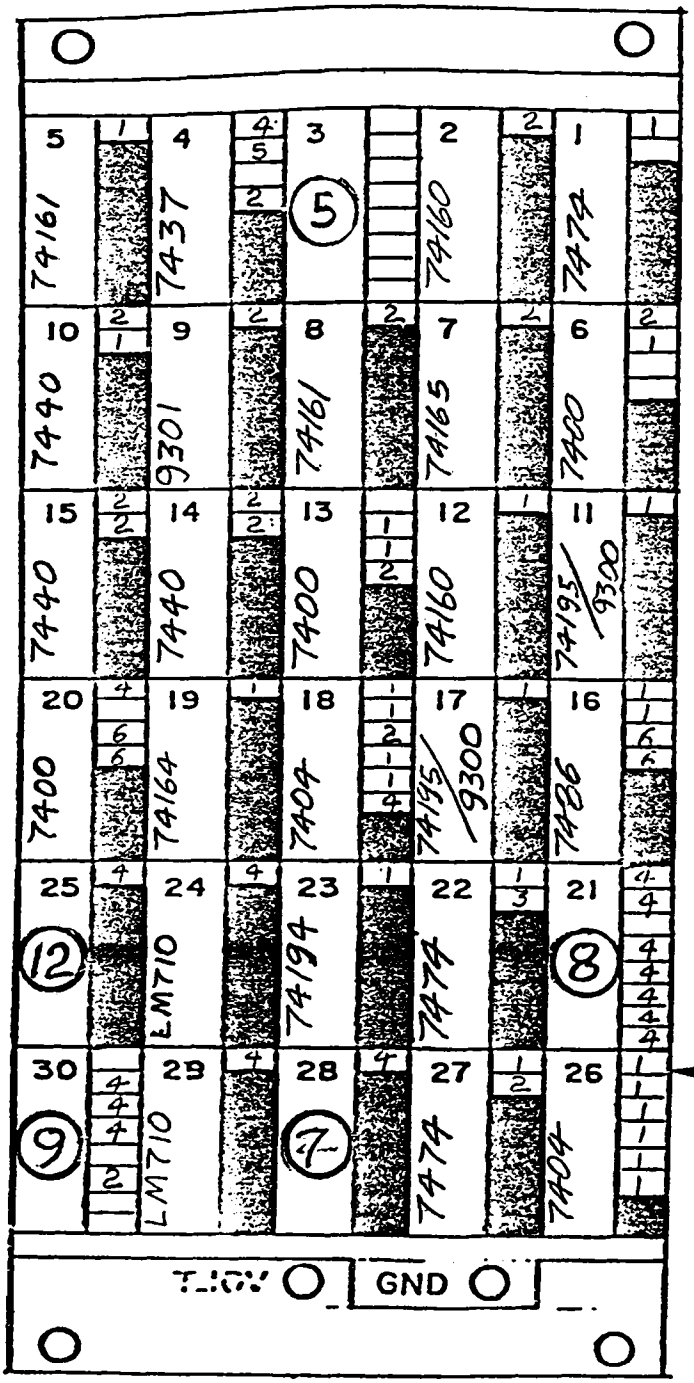
V L A

PROJECT M4

TITLE I.C. MODULE PANEL ANTENNA BUFFER MODEL D

DWG NO. A13720P79 SHEET 1 OF 6

LOC A



SPECIAL SUB ASSY'S

ITEM	BOM #	DWG #
5	A13720Z9	B13720P16
8	A13720Z36	B13720P24
12	A13720Z95	A13720P71
7	A13720Z28	B13720P20
9	A13720Z38	B13720P26

NUMBER IN THIS LOCATION REPRESENTS SHEET NUMBER OF LOGIC DIAGRAM, TYP.

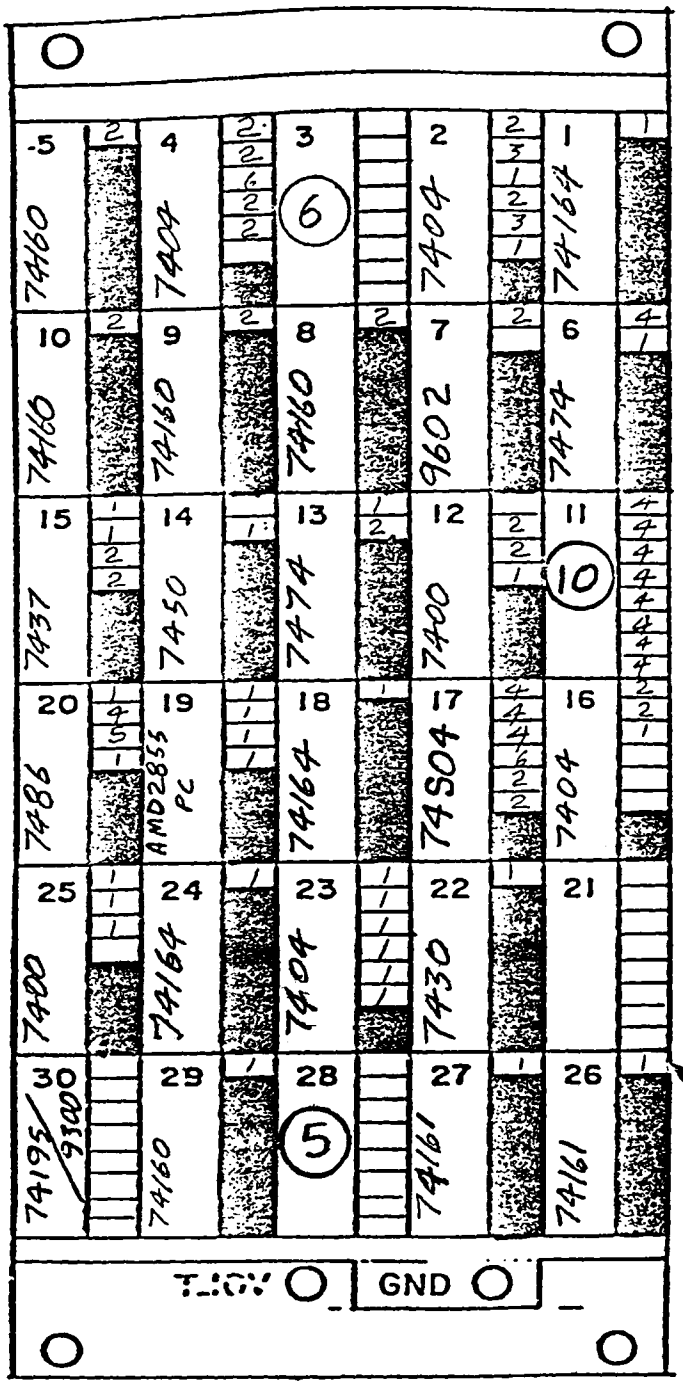
BILL OF MATERIALS: A13720Z5

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLA

PROJECT M4
TITLE I.C. MODULE PANEL
ANTENNA BUFFER MODEL D
DWG NO. A13720P79 SHEET 2 OF 6

LOC B



SPECIAL SUB ASSY'S

ITEM	BOM #	DWG #
6	A13720Z10	B13720P14
10	A13720Z39	B13720P6
5	A13720Z9	B13720P16

NUMBER IN THIS LOCATION REPRESENTS SHEET NUMBER OF LOGIC DIAGRAM, TYP.

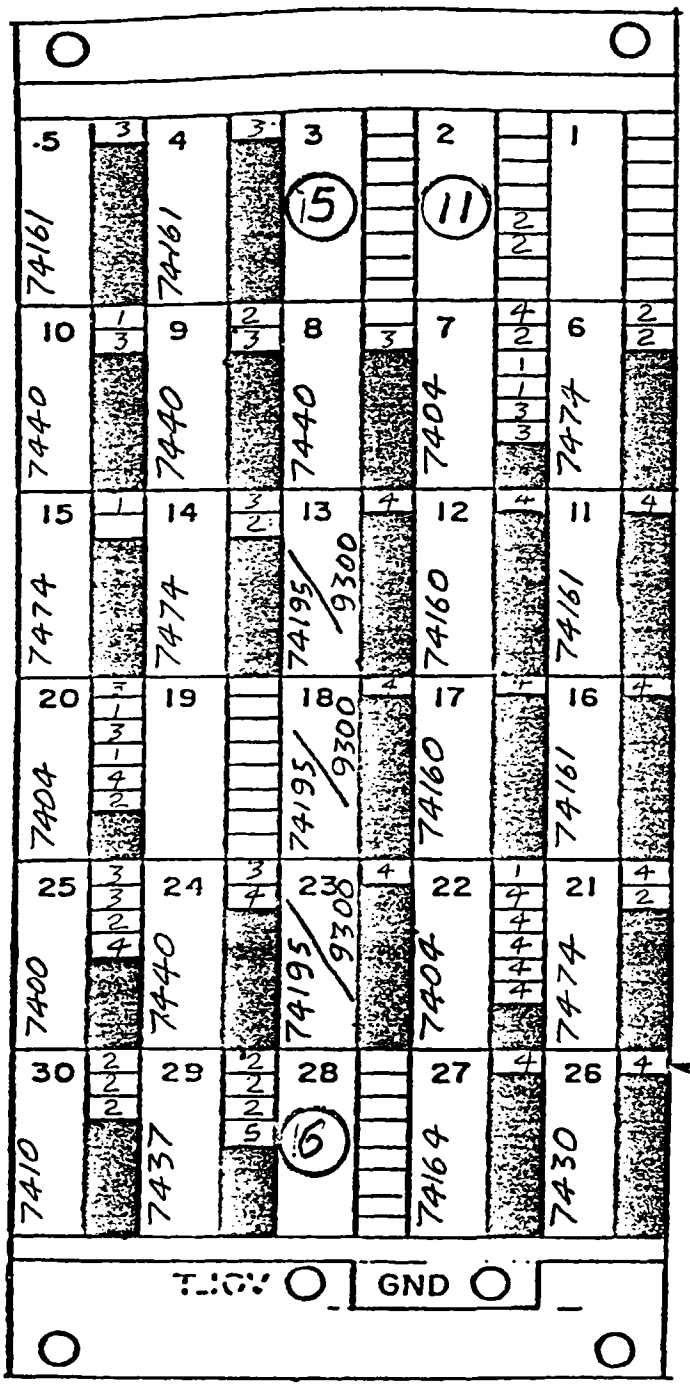
BILL OF MATERIALS: A13720Z5

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLA

PROJECT M4
TITLE I.C. MODULE PANEL
ANTENNA BUFFER MODEL D
DWG NO. A13720P79 SHEET 3 OF 6

LOC C



NUMBER IN THIS LOCATION REPRESENTS SHEET NUMBER OF LOGIC DIAGRAM, TYP.

SPECIAL SUB ASSY'S

ITEM	BOM #	DWG #
11	A13720Z9	B13720P16
5	A13720Z52	A13720P46
6	A13720Z10	B13720P14

BILL OF MATERIALS: A13720Z5

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

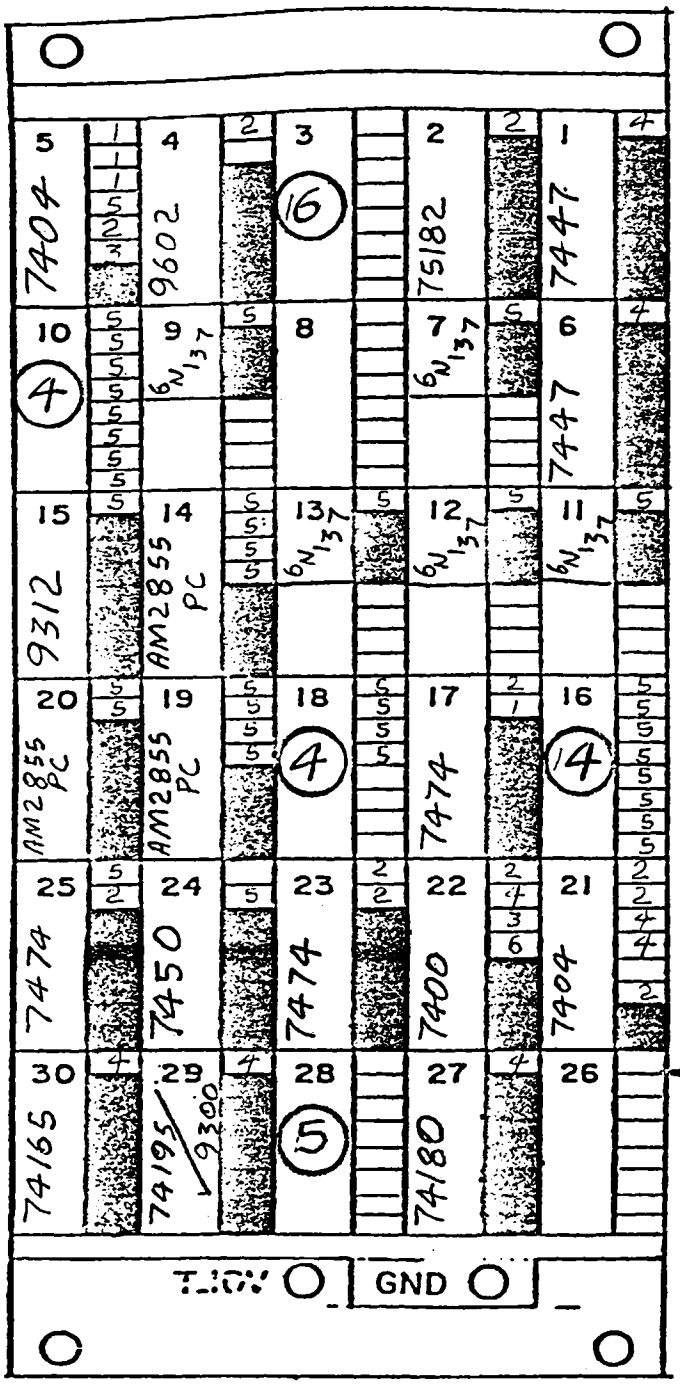
VLA

PROJECT M4

TITLE I.C. MODULE PANEL
ANTENNA BUFFER MODEL D

DWG NO. A13720P79 SHEET 4 OF 6

LOC D



SPECIAL SUB ASSY'S

ITEM	BOM #	DWG #
6	A13720Z10	B13720P14
4	A13720Z8	B13720P17
5	A13720Z9	B13720P16

← NUMBER IN THIS LOCATION REPRESENTS SHEET NUMBER OF LOGIC DIAGRAM, TYP.

BILL OF MATERIALS: A13720Z5

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

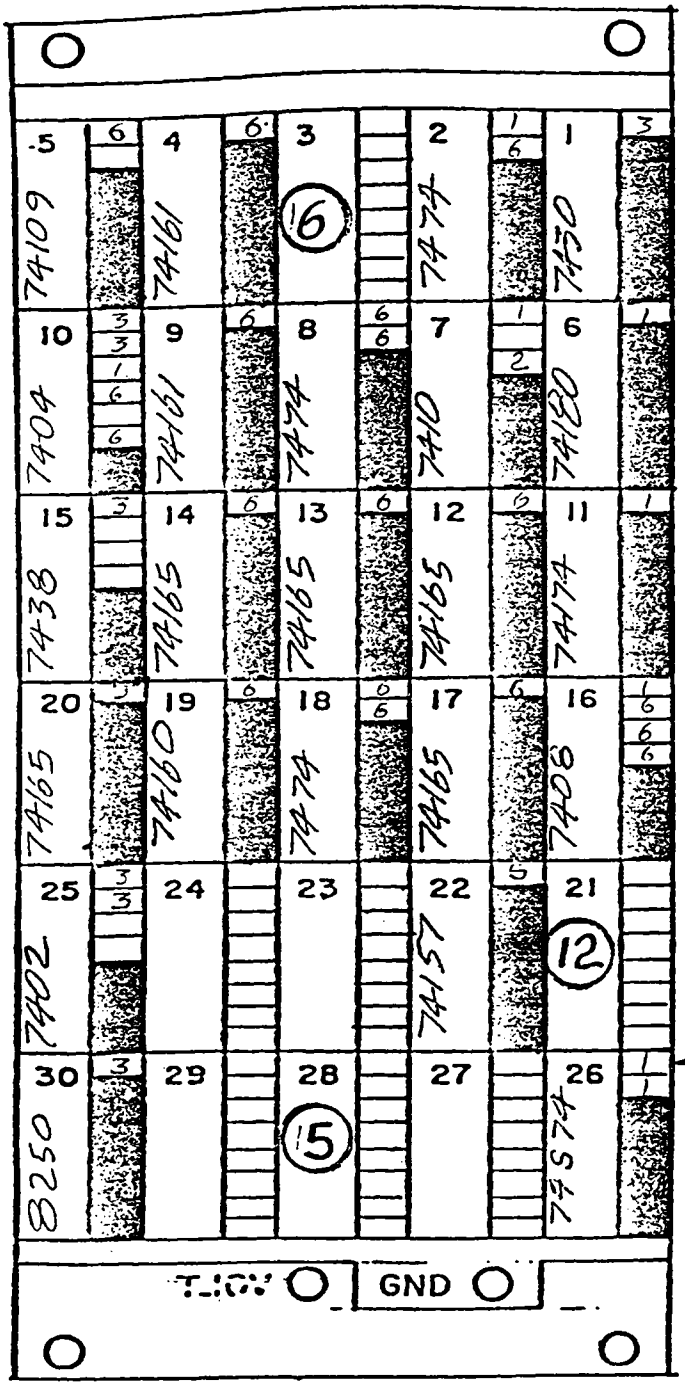
VLA

PROJECT M4

TITLE I.C. MODULE PANEL
ANTENNA BUFFER MODEL 2

DWG NO. A13720P12 SHEET 5 OF 6

LOC E



SPECIAL SUB ASSY'S

ITEM	BOM #	DWG #
16	A13720Z10	B13720P14
12	A13720Z96	A13720P71
5	A13720Z9	B13720P16

NUMBER IN THIS LOCATION REPRESENTS SHEET NUMBER OF LOGIC DIAGRAM, TYP.

BILL OF MATERIALS: A13720Z5

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLA

PROJECT M4

TITLE I.C. MODULE PANEL
ANTENNA BUFFER MODEL D

DWG NO. A13720P79 SHEET 6 OF 6