VLA Technical Report No 60
The Central Buffer, Module type M3

David Weber
8/14/86

Table of Contents

1.0 Introduction

2.0 Central Buffer Functional Description

- 2.1 Message Format Description
- 2.2 Central Buffer I/O Signals
- 2.3 Time-Driven Central Buffer Operations

3.0 Detailed Circuit Description

- 3.1 Time Base
- 3.2 Command Signal Detection, Storage and Output
- 3.3 Antenna Monitor Data Detection and Storage
- 3.4 Central Monitor Data Polling and Storage
- 3.5 SLC Polling and Monitor Data Output
- 3.6 Power Circuits

4.0 List of Central Buffer Drawings

5.0 Data Sheets

AM2855PC

List of Illustrations and Major Drawings

Figure 1, Block Diagram of the Monitor and Control System

Figure 2, Antenn Timing Operations

Figure 3, Central Timing Operations

Figure 4, Message Format

Figure 5, Central Buffer Logic Flow Diagram

Figure 6, Central Buffer Block Diagram

Figure 7, Central Buffer Exploded View

D13720L48, Model D Central Buffer Logic Schematic

D13720P80 Model D Centrl Buffer Assembly Drawing

A13720P81 Model D Central Buffer IC Location Map

A13720Z24 Model D Central Buffer BOM

1.0 INTRODUCTION

This manual describes the operation of the Model D Central Buffer (CB), module type M3 and was written to serve as a trouble-shooting and maintainance guide for this component of the VLA Monitor and Control (M&C) System.

To put the operation of the CB into the system context, the reader is referred to the manual: "An Overview of the Monitor and Control System", VLA Technical Report No 44. "The Handyman's Guide to the Data Set", VLA Technical Report No 30 provides a detailed description of the CB/Data Set interactions. Figure 1 depicts the relationship of the CB to the balance of the M&C system. Figures 2 and 3 depict the Monitoar and Control System timing, Figure 4 depicts the message format.

The emphasis is on the detailed functional operation; the writer's intent is to provide a thorough description of the Central Buffer's theory of operation. Straight-forward portions of the logic are treated briefly; more complex areas (and there are several) are fully explained and the explanations are augmented by timing diagrams. Using this manual as a reference, a digital maintainance technician should be able to quickly identify and repair malfunctions.

The logic descriptions are based upon two contrasting perspectives: 1) operations as a function of time (which is the driving parameter in the VLA Electronics); 2) command and monitor data message transmission operations, - the primary functions performed by this module.

This manual does not address the signal transmission properties of the LO/WG Transmission systems which are in effect the "wire" used by the M&C system for antenna - central message communication; the subject of the transmission characteristics is too extensive to be addressed in this manual but important aspects of these characteristics are discussed where it seems appropriate to do so. The timing discretes inputs from L8 and L8 timing "jitter" are discussed.

2.0 CENTRAL BUFFER DESCRIPTION

The primary function of the Central Buffer is command/data message distribution; the CB detects bit-serial digital command messages from the Serial Line Controller (SLC) for distribution to the Antenna Buffer (AB) and central Data Set, detects and stores BI-Ø antenna monitor data messages, polls the central Data Set for monitor data messages and then transmits these monitor data messages to the SLC in response to polling requests from the SLC. All M&C messages exchanged between the Antenna Buffer and the Central Buffer are routed through the LO/WG

Transmission systems; the Antenna and Central Buffers form a complementary pair of M&C message handlers on either end of the LO/WG Transmission systems. Figures 5 and 6 depict the CB logic flow and logic block diagram.

In contrast to the Antenna Buffer which has five Data Sets to deal with at low speed, has a lot of time available and has no concurrent command/data handling functions, the Central Buffer interacts with only one Data Set but must perform concurrent command/monitor data operations and must deal with many high speed message flow interactions with the Serial Line Controller. There is virtually no time that the CB logic is inactive.

The CB must be able to detect, store and output up to four antenna and up to eight central command messages and detect and store ten antenna monitor data messages. The CB must also poll the central Data Set for two monitor data messages which are stored with the antenna monitor data messages for output to the SLC when polled by the SLC.

For the Antenna/Central Buffer combination, command messages extracted from the control computers in one VLA machine cycle are delivered to the controlled device in the next cycle. The response of the controlled device to the command may be monitored in the cycle in which the device received the command but it is input to the control computers in the next cycle; therefore the earliest possible monitored response to a command is input to the computers two VLA machine cycles after the computer output the command to the M&C System.

The CB is packaged in a standard VLA 1-wide module and contains wire-wrap logic connector boards for the digital logic. A front panel numeric LED shows the DCS address and flashing descrete LEDs indicate command and monitor data message flow. A front panel test point connector permits observation of logic signals for diagnostic purposes. DC power regulators on the rear panel provide special voltages required by some of the logic chips.

2.1 MESSAGE FORMAT DESCRIPTION

Figure 4 depicts the format of the Command and Monitor Data messages and the "Q" (for Query) character format. The messages are prefixed by an "S" (for start) character which signals that a message immediately follows. The bit rate of the S character is twice the bit rate of the data bits to make this character unique. The message consists of five 8-bit data bytes; the first byte contains a 5 bit DCS Address (which can range from 0 to 31) and a 3-Bit Data Set Address which can range from 0 to 7. The second byte is the Multiplex Address which designates a particular command or data channel. The third, fourth and fifth bytes are components of a 24 bit command or monitor data argument. In the case of an analog data message, the 24 bit

argument consists of two 12 bit values resulting from the conversion of two analog signals by the Data Set analog-to-digital converter. In all address and argument values, the first bit (in time) is the most significant bit.

The M&C messages transmitted through the LO/WG Transmission system have a different format than the simple NRZ described above; the bit sense is conveyed by the phase of a 500 Khz phase-modulated carrier. The form of modulation is called BI-Ø-L (L for level, also called Manchester encoding); a modulator in the output circuitry of the Antenna and Central Buffers inverts the phase of the 500 Khz carrier for each NRZ data one bit; a zero bit does not change the phase. This encoding scheme provides a signal edge in every bit space, a very desireable property for situations in which receiving logic must derive a clock from the structure of time-serial digital messages. This BI-Ø modulation requires some additional circuitry in the receiving buffer to reconstitute the NRZ format. The BI-Ø antenna command messages from the CB to the AB have a higher bit rate than the antenna monitor data messages from the AB to the CB. The details of these formats are discussed below.

BI-Ø modulation of the NRZ data stream eliminates the DC term and all frequency components below 500 Khz from the message signal spectrums; a necessary measure since the outputs of the LO Receivers are AC-coupled. A second, very important reason for the use of BI-Ø modulation is that the 1800 Mhz LO carrier spectrum must not have any low frequency modulation components since they can perturb the operation of the stable frequency references in the LO System.

The "Q" character is used by the CB to poll data from Data Set #5 via the buffer's Data Set Command Port. The SLC uses the "Q" character to poll data from the Central Buffers via the SLC's Command/Q Ports. The bit rate of the Q character is the same as the bit rate of the S characters.

2.2 CENTRAL BUFFER I/O SIGNALS

- T/H pulse, - a 1.6 millisecond, low-true, single-ended TTL level signal from the L8 Distribution System which goes true (falls) 105 (average) usec before the start of the VLA timing cycle.

- 5 Mhz clock, - a 2 volt P-P (nominal) sine wave clock generated by the L8 Distribution System to clock the CB and Data Set #5 logic.

- SLC Command Signal Input - an optically isolated (in the CB), low-true, TTL logic level, NRZ format command message input from the SLC. Bit rates are 500 ns/bit and 1 usec/bit for the S character and message bits respectively.

- SLC Monitor Data Output - a TTL level, low-true, NRZ monitor data message output to the SLC. Bit rates are 500 ns/bit and 1 usec/bit for the S character and message bits respectively.

- Antenna Monitor Data Input - a bipolar, 2 volt P-P, analog BI-Ø format signal input from the Central LO Receiver, L9. Bit rates are 20 usec/bit (10 BI-Ø cycles) and 40 usec/bit (20 BI-Ø cycles) for the S character and message bits respectively.

- Antenna Command Message Output, - a TTL level, BI-Ø format signal output to the Central LO Transmitter, L10. Bit rates are 2 usec/bit (1 BI-Ø cycle) and 4 usec/bit (2 BI-Ø cycles) for the S character and message bits respectively.

- Data Set Command Port - a TTL level, NRZ format output to the Command Input of Data Set #5. Bit rates are 5 usec/bit and 10 usec/bit for the S character and message bits respectively.

- Data Set Monitor Data Port - an optically isolated (in the CB), input port which receives a low-true, TTL level, NRZ format, monitor data input from Data Set #5. Bit rates are 5 usec/bit and 10 usec/bit for the S character and message bits respectively.

- Data Tap Port - a TTL level, low-true output to the Data Tap. The outputs to the Data Tap are both command and monitor data messages at the SLC/CB bit rates.

- DCS Address Lines - five high true TTL level lines which are grounded on the back of the bin to define the DCS address of the CB.

2.3 TIME-DRIVEN CENTRAL BUFFER OPERATIONS

The operations performed by the Central Buffer are time-directed in that functions are enabled, initiated and terminated by control discretes derived from the internal time base; these discretes regulate the message flow between the antenna and the central electronics to insure that the CB is properly synchronized with the AB, the modes of the LO/WG Transmission system and the SLC. Figure 2 depicts the time-ordered operations performed by the Central Buffer. Figure 5 depicts these operations in flow diagram form. Figure 6 depicts the Central Buffer Block Diagram.

The CB time base is referenced to the T/H pulse from the L8 Distribution System and timing terms are stated in terms of microseconds of elapsed time from t = 0 which is 105 usec (average, see the discussion of L8 jitter) after the start (fall) of the T/H pulse. The CB time base is triggered into operation by the T/H pulse and is clocked by 10 Mhz which is generated by

doubling the 5 Mhz clock from the L8 Distribution System. If the T/H pulse is missing the CB will remain in the quiescent state.

A 0 - 1000 usec enable causes the CB to transmit the stored antenna commands to the Antenna Buffer via the LO/WG Transmission systems. The command message stream amplitude modulates an 1800 Mhz carrier in the Central LO Transmitter, L10. The antenna command bit rate is 2 usec/bit (1 Bi-Ø cycle) and 4 usec/bit (2 Bi-Ø cycles) for the message and S character bits respectively.

The antenna command message stream consists of an 80 usec preamble of BI-Ø zeros and up to four BI-Ø format command messages separated by 8 Bi-Ø spacing bits. The durationn of the preamble, four messages and spacing bits is 944 usec. In the event that there are no command messages, (e.g. the computer message stream is stopped), the command message stream will consist of an unbroken sequence of BI-Ø zeros and will last approximatly 1000 usec.

An 8 - 8000 enable causes the CB to unload the stored NRZ format central commands to Data Set #5 via the Data Set #5 Command Port. Data Set #5 analyzes the message stream to determine if it is the target of a command message; if it is, it executes the command. See the Data Set manual for a description of this process.

A 24,000 - 48,000 enable permits the CB to listen for Bi-Ø format monitor data messages from the AB via the LO/WG Transmission System. When an antenna monitor message is detected, a loading sequence is initiated which causes the data message to be stored in the serial monitor data memory. The monitor data message transmission bit rate from the Antenna Buffer is 40 usec/bit for the message bits and 20 usec for the "S" bits. The BI-Ø clock rate is 500 Khz so that the BI-Ø "S" bit durations are 10 BI-Ø cycles and the message bit durations are 20 BI-Ø cycles. The BI-Ø modulator in the Antenna Buffer is coherent with the message unload clock so that the transmitted BI-Ø command waveform duty cycle is 50%.

The antenna monitor data message stream consists of an 80 usec preamble of BI-Ø zeros and ten BI-Ø format monitor data messages separated by 8 BI-Ø spacing bits. The total period for this message stream is 12,800 usec (80 usec preamble + 10 x (100 bit messages + 8 spacing bits)) x 20 usec/bit. The stream is emitted by the Antenna Buffer at t = 24,000 and approximatly 24,000 usec is available for transmission.

At 48400 and 49400 the CB polls data from Data Set #5 by emitting Q characters on the Data Set #5 Command Port. After a 50 usec delay to detect the Q, the Data Set detects the Q character and begins a data acquisition sequence. 250 usec after the output of the Q, the Data Set begins to emit an NRZ format

monitor data message to the CB's Data Set #5 Monitor Data Port. This port is optically isolated (in the CB) to eliminate ground noise effects. The monitor data loading sequence loads an additional 8 spacing bits between monitor data messages. The 200 usec delay between the start of the "Q" and the begining of the monitor data message is used by the Data Set for sampling and A/D conversion. The Data Set monitor data message duration is 500 usec so there is a 250 usec margin in the 1000 usec period. The Data Set #5 monitor data is gathered after the antenna monitor data messages have been stored so that the memory contents are in the order: MW1 - DS0 ... DS4; MW2 - DS0 ... DS4; MW1 - DS5; MW2 - DS5. This is the order that they are read out to the control computers by the SLC. Figure 3 depicts the Data Set #5 polling timing.

A 24,000 - 51,000 usec enable permits the Central Buffer to listen for NRZ format command messages from the Serial Line Contoller. The command messages may be in any order and may be directed to either the antenna Data Sets (0 - 4) or to the central Data Set (5). The command memories in the Central Buffer can handle up to 8 central and up to 4 antenna command messages in any VLA cycle. The SLC can extract, format and output up to 128 commands from either (or any combination of) two computers during this period. There are no requirements for dummy command messages (ie. messages to non-existent devices) to fill the command memories.

A 1000 - 24000 usec enable permits the Central Buffer to be polled by the Serial Line Controller for the NRZ format monitor data messages stored in the CB's serial monitor data memory. The Serial Line Controller directs a Q character to each CB in the sequence of DCS-#0, DCS-#1.... DCS-#37 (octal, for a total of 32 CB's). This sequence is repeated 11 times.

When the polled monitor data message is detected by the SLC, it is immediately rebroadcast to all CB's via the SLC's Central Buffer Command Ports during the monitor data memory loading sequence. This rebroadcast data is tapped off the CB's Command Input Port and fed to the Data Tap in the bin so that the Data Tap is able to hear all rebroadcast monitor data and command messages. This rebroadcast Monitor Data is sometimes referred to as "gossip data". There are 384 monitor data words (32 buffers x 12 words/ant) polled from the CB's during this period. The polling period is tight: 60 usec which is about 1 usec longer than required for the CB to detect the Q, output the monitor data message to the SLC, and enable the SLC to detect and temporarily store the message.

At t = 51,000, the CB time base is shut down and remains in this quiescent state until stimulated back into operation by the T/H signal. By design there are no provisions for flywheeling of the time base in the Central Buffer; the flywheeling function is

performed by L8.

3.0 DETAILED CIRCUIT DESCRIPTION

3.1 TIME BASE

The time base logic (Sheet 4) generates a series of time-based control discrete terms which regulate all functions of the Central Buffer. The time base is quiescent until triggered into operation by the T/H pulse from the L8 distribution system.

The leading edge (fall) of T/H triggers E1007, an AM26S02 high stablilty one-shot which times out a 105 usec delay. The trailing edge of the one shot output clocks the E1205 flip-flop which permits flip-flop D2305 to capture the next 10 Mhz clock. This sets control flip-flop D2311 which removes the low-true inhibit on the Master Reset of the time base counters E6 .. D29. The inhibit forces the counters to count from the cleared state of zero.

Flip-flop D2305 also generates a psuedo QQ pulse; gate D2203 senses D2305 and D2310 (D2310 Q- output), these states are true for 100 nanoseconds during the sequence of shifts which set the time base control flip-flop D2311. Gate's D2203's low true output (QQ) clears a number of discrete-generating flip-flops.

The time base counters E6, D21,D16, D11, D6 D1 and D29 are a string of synchronous counters driven by the 10 Mhz clock E0106.

At t = 51,000 usec, gate E0710 triggers the 1 usec one-shot E1109 which resets the control flip flops D2305,11. D2311's low true output drives the time base counter E6 .. D29 Master Resets through gate B3006 so that the counters are held reset to the zero count state. Thus the time base (and hence the CB) is quiescent and remains in this state until stimulated on again by the next T/H pulse.

The time base clock is a 2 Volt P-P, 5 Mhz sine wave clock from the L8 Distribution System. The 5 Mhz clock is detected by analog comparator A2111 (on Sheet 3) which senses the 5 Mhz axis crossing (with a little hysteresis). The TTL-compatible output of A2111 drives a Schottky 74S04 (E0102) which "squares" the 5 Mhz clock to drive the E2 harmonic doubler circuit which rings at 10 Mhz. The 5 Mhz drive to the doubler is differentiated by the 10 pf, 1K ohm, (E2) RC circuit so that the MPS 918 transistor has a narrow collector current pulse. The tank is tuned to 10 Mhz and the AC coupled output drives the Schottky 74S04 E0104 which is caused to operate in a linear region by the 2K ohm resistor on the doubler's output. Inverter E0104 and E0106 square the 10 Mhz clock signal which drives the time base and clocks the message edge detection shift registers. Inverter E01 must be a 74S04; the high switching speed of the Schottky logic is important to

the doubler circuit's operation.

The reason that a 10 Mhz clock is used as a clock in the Central Buffer is that it provides a 100 ns resolution for synchronization to the 2 Mhz and 500 Khz bit rate incoming message streams from the SLC and AB. The sampling clock must be an integral multiple of the bit rate of the incoming message stream.

A series of time discretes are derived from the time base to control the CB operations. These are:

0 to 1000 -- Enable term 0 to 1000 is generated by flip flop D2605 (sheet 4) which is set by the time base reset pulse (the psuedo QQ) from D2203. D2606 is reset by the rising edge of the first 1-Khz term from counter D0614.

Enable 0 to 1000 is used in gate A3003 (Sheet 1) to permit the antenna commands stored in the Antenna Command Memory (Sheet 5) to be pushed out to the Central LO Transmitter, L9. The 0 - 1000 enable is also used in gate E1105 (Sheet 5) to permit the BI-0 Antenna Command Output to be active only during the time that the LO/WG Transmission system is transmitting command messages to the antenna.

0 - 8000 -- Enable term 0 - 8000 is generated by flip-flop D1311 (Sheet 4). D1311 is clocked on by the psuedo QQ pulse described above. D1311 is direct reset by the first 8000 term from time base counter D0611. Flip-flop C0910 is a superflous vestige of an earlier version of this logic which is clocked reset by the first 8 usec edge (in the cycle) from time base counter D2111. The rising edge clock from C0910 has no effect on Flip-flop D1311 since it is already set. Enable 0-8000 is used in gate A3006 (Sheet 1) to enable 200 Khz clocks to unload the Central Command Memory F0606 (Sheet 5) to the Data Set Command Port, (Sheet 5). This enable is also used in the port gating in gate A2503 to disconnect the command memory from the Data Set port.

Enable 24,000 - 48,000 is generated by flip flop D0211 which is direct set by gate E0406 which goes true at 24,000 usec. Gate E0706 goes true at t = 48,000 usec to direct reset D0211. This 24,000 - 48,000 term enables the CB to listen for antenna monitor data messages from the AB.

When synchronizing an osciloscope to the CB time base or QQ pulse, you will observe a puzzling 10 usec jitter in the time of arrival of the antenna monitor data messages from the AB; this is an artifact of the L8 Timing Generator which goes through a 3-state periodic variation of the 19.2 Hz period. The L8 logic implementation causes the 3 periods to vary in a sequence which is base, base + 200 ns, base +10 usec.

3.2 COMMAND SIGNAL DETECTION, STORAGE AND OUTPUT

This is the first major function performed by the Central Buffer; all of the antenna and antenna-associated commands are handled by the CB.

ANTENNA AND CENTRAL COMMAND DETECTION, STORAGE AND OUTPUT -- All command messages originate in the SLC which extracts them from either of two control computers, formats them into serial messages and broadcasts them to the Central and System Buffers at a 2 Mhz S character and a 1 Mhz message bit rate. If the commands are all derived from one computer the command message intervals are 160 usec; if two computers are involved the interval between messages is either 80 or 160 usec depending upon the settings of the various selector switches on the front of the SLC, see the Overview of the Monitor and Control System manual for details.

It is the task of Central Buffer to listen to all the incoming command messages, decode the DCS address to determine whether the address matches it's assigned hard-wired (in the bin) matches the message address; having determined that it is the target of a command message, the CB then decodes the Data Set address to determine whether the command message should be stored in a local buffer memory or stored in an antenna command memory for output to Central LO Transmitter (L9). Having stored the command messages in the serial command memories, the CB then outputs them at appropriate time in the nest VLA machine cycle.

In a hardware sense, there is no ordering of command messages to the CBs as there is in the monitor data polling; any CB could receive a continuous stream of command messages at 80 usec intervals and must be able to store them in the command memories. Obviously the command memories would quickly fill up and overflow if the command stream in a given cycle exceeded the memory capacity of 4 antenna and 8 central command messages. In practice the control programs in the ModComp computers formulate commands in an orderly schedule so that there are never more than 4 commands (4 is a very rare occurance, the average is about 1.5) per VLA machine cycle.

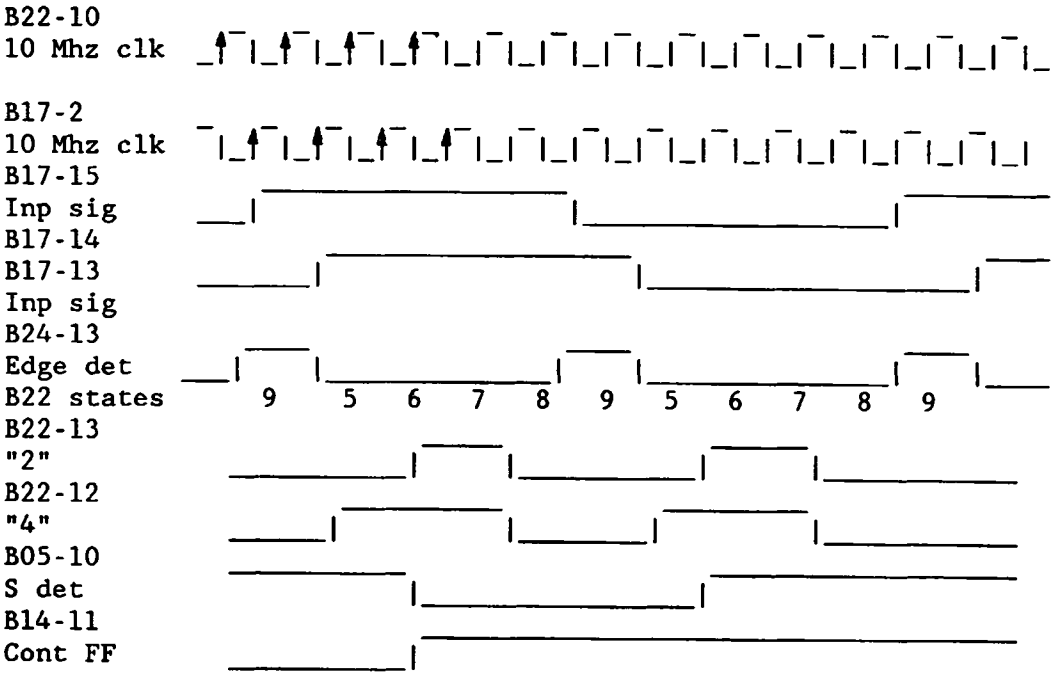
SLC commands are input in low-true form at the SLC Command Signal Input port, J2-39 where they drive an optical isolator to eliminate ground noise effects. The output of the isolator drives a power buffer, A0210 which drives the Data Tap Port, J2-14/15.

The high-true command message is sampled by shift register B17 which is clocked by 10 Mhz. Exclusive or A2410 generates a 100 ns output when signal edges shift through the register. These edges preset counter B22 to a count of 5 throuh or gate B2706.

B22 sequences through the states 5,6,8,9,5,6 etc because of the TC feedback to B2706. The "4" stage of B22 clocks the data stream from B1713 into flip-flop B0111 and shift registers B12, B7 and B2 which have decode logic to test for Q, and S characters and to compare the DCS and DSA addresses. The Q detect gate B0910 activates the monitor data output logic (discussed below); the S detect gate B0510 strobes the magnitude comparator B20 to test the message DCS address against the address hardwired on the bin. Exclusive or A2413 provides the fifth bit of comparison for the four bit magnitude comparator. Both S and Q detect gate outputs are 500 ns wide.

The operation of this logic is depicted in the simplified timing diagram below.

COMMAND MESSAGE INPUT PHASING



The "Inhibit Gossip Data" term on shift register B17 holds this register reset when the CB is outputting a monitor data message to the SLC. The monitor data 2 Mhz output shift clock is taken off counter B22; the inhibit holds the phase of the 2 Mhz clock generated by counter B22 constant during the period of output of a message output to the SLC. The reasons for the inhibit are discussed in the monitor data section of this manual.

If the comparison agree, the message is addressed to the CB that we are discussing and a message loading sequence is initiated. The comparator strobe sets load control flip-flop B1411 and strobes flip-flop B1405. B1405's D input is driven by magnitude comparator B13 which tests the message DSA against

the hardwired address 5. If the DSA is 4 or less the command is to be stored in the antenna command memory and if 5 or greater it is to be stored in the central command memory. B1405's outputs steer the memory load clocks via gates B0614 and B0606. Load control counter C21 and C16 generates a load enable to permit the 2 Mhz clocks from B2213 to load the command message into the serial command memories. The counter is preset to a count of 151 and at the count of 256 (1 count after 255, the all 1's state), the 128 counter term is anded with the 2 Mhz clock in gate D2213. The trailing edge (rise) of D2213 clocks control flip-flop B1411 reset. B1411's output is the load enable on the memory clock gates B0614 and B0606. The message stream is tapped of of flip-flop D1905 which is an extension of the B12,B7,B2 shift register. Shift register B2 and D19 are enabled by a 24,000 - 51,000 enable which holds them in the clear state except during the period that the CB should receive commands. The inhibit prevents the S detector from responding to the rebroadcast monitor data messages from the same CB which would cause them to be loaded into the command memories. The large width of the message decode register is a vestige of the original design in which the buffer's time base was set to zero when two concatenated Q characters were detected; there were two Q detectors on the register. In practice this scheme was found to too easily perturbed because of the data recirculation; buffers would tend to get out of sync. The use of the discrete T/H term was adopted when antenna #3 was put in service and the second Q detector gate was removed from the logic. The register could have been shortened to two stages instead of three but this was not done.

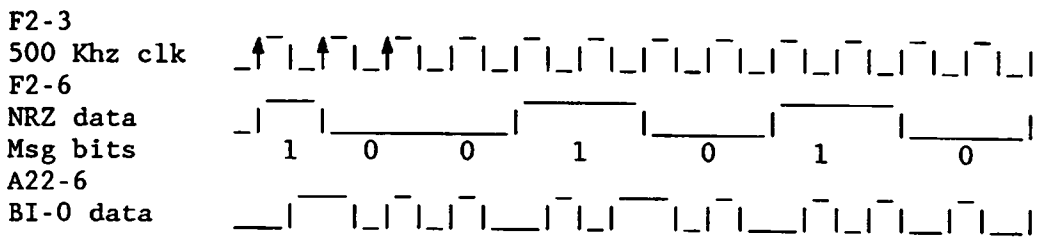
COMMAND UNLOAD TO ANTENNA BUFFER AND CENTRAL DATA SET -- Having loaded the command memories we now consider the unload logic. The unload process for both classes of commands is a simple enable of unload clocks to the command memories.

The antenna commands are pushed forward in the command memory by the counter F17,F18 (Sheet 4). This is done because the command memory is a quad 128 bit memory and the (100 bit) commands need to brought forward in the memory for the impending output. This counter is activated by the trailing edge of the 24,000 - 48,000 enable and generates a train of 48 500 Khz clocks starting at 49,000 usec.

The antenna commands are unloaded by a 500 Khz clock enabled by a 0 -1000 usec enable on gate A3003 which drives the antenna coommand memory through or gate F1906. The output of antenna command memory F1 is sampled by flip-flop F0206 which in combination with the 500 Khz clock drives the BI-Ø modulator, A2206. The BI-Ø command message stream is enabled by the 0 -1000 enable so that the LO Transmitter (L9) sees signal activity only during the period that commands are transmitted to the antenna.

The operation of the BI-Ø modultor is depicted in the simplified timing diagram below.

ANTENNA COMMAND BI-Ø MODULATOR TIMING



The central electronics commands are 200 Khz clocks enabled by the 0 - 8,000 usce enable on gate B3013 (Sheet 1) via or gate A0806 to the Data Set Command Port, J2 -24,25.

3.3 ANTENNA AND CENTRAL MONITOR DATA GATHERING, STORAGE AND OUTPUT

This is the second major function performed by the Central Buffer; all of the VLA antenna and antenna-associated central monitor data messages are handled by the CB.

ANTENNA MONITOR DATA DETECTION AND NOISE FILTERING --- The antenna monitor data signal from the Central LO Receiver (L9) is threshold detected by analog comparator A1611 (sheet 3) which switches high and low at input signals above and below + and - 200 millivolts. Resistor A25-5/12 provides a positive feedback to the comparator + input so that the comparator is caused to have about a 200 millivolt hysteresis. The typical monitor data signal from L9 is about 2 volts P-P. The baseline noise is typically about 100 millivolts (peak); the 200 millivolt threshold was chosen to insure that the comparator does not switch on baseline noise. Baseline noise is not relevant to the process of detecting the monitor data signal; it is undesireable to have the signal detection logic switching on this noise. The 200 millivolt switching point permits detection of monitor data signals which have dropped several db below the nominal 2 volt P-P level. The 200 millivolt switching points are determined by the amount of signal current fed to the comparator + input; this is controlled by potentiometer A25-1/2/15. Resistor A23-7/10 (510 ohms) is a terminating resistor for the driving circuit in L9.

A careful observation of the L9 LO Receiver output on an oscilloscope shows a pronounced baseline wobble of the signal (typically about 50 millivolts) as a function of the BI-Ø bit changes; this effect is an artifact of the AC coupling of the signal in L9, the LO Receiver. The signal level bounces up and down because BI-Ø bit changes alter the apparent duty cycle of the signal in a small region of time after a bit change. This

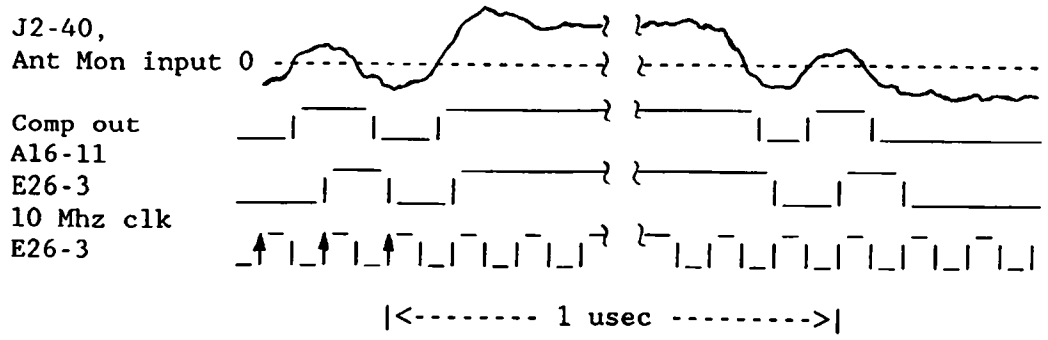
baseline wobble phase-modulates the command signal input to the A2911 comparator; as a result the logic signal output by the comparator also has this phase modulation of about 50 nanoseconds. It should be noted that this effect is not seen on the Monitor and Control System test bench because the Test Bench analog command and monitor data signals are DC coupled.

The 24,000 - 48,000 enable on registers E26 and A7 inhibits the antenna monitor data detection logic outside the permitted period of transmission from the Antenna Buffer.

Shift register E26 provide a very important augmentation of the analog-to-digital conversion operation by comparator A1611. These flip-flops are Schottky 74S74's which have a 5 ns set up and 0 ns hold time. Comparator A1611 is a fairly fast comparator but is slow compared with TTL logic speed; the Schottky flip flops are used as a narrow aperature (5 ns) sampler to perform the 1/0 decisions. It is very important that only 74S74 flip flops be used in E26; the 5 ns set-up and 0 ns hold times of the Schottky logic are vital in this A/D conversion process.

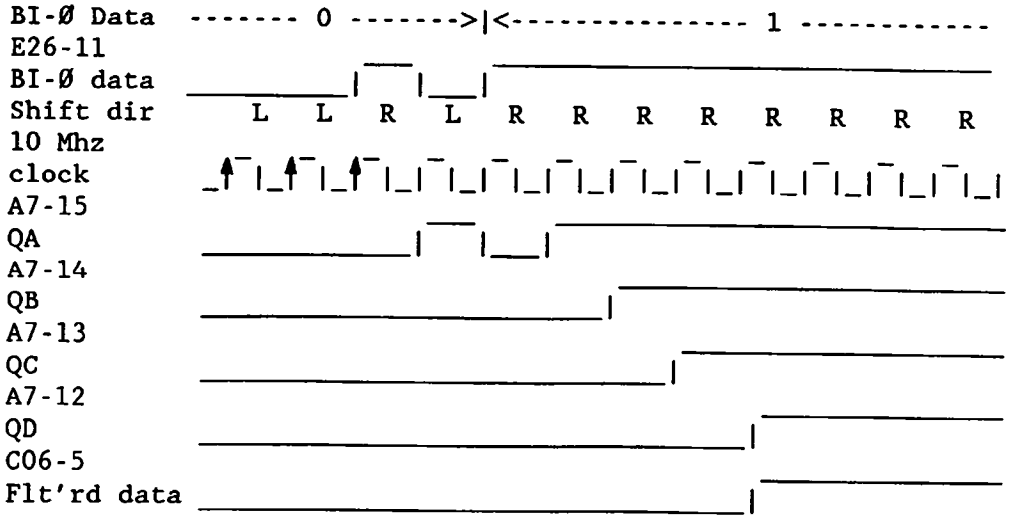
Edge noise filter A7 has a very important function: filtering of command signal bit edge noise from the BI-0 command stream. The logic decision performed by the comparator and E26 is influenced by noise, (eg power supply noise or RF noise added to the data signal in the transmission link); this noise can obscure the analog monitor data signal and cause erroneous logic decisions. As the analog signal traverses through the comparator switching region at the edge of a data bit, this noise can cause spurious noise bits to be added to the detected data stream, causing them to have "fuzzy" edges so that the process of detecting and sampling the data bits in the center of the bit period could be erroneous if the appearance of a 1/0 or 0/1 change were interpreted as the arrival of a new data bit. This phenomena is depicted in the Timing Diagram below. What is needed is a time-based digital filter that integrates over these noisy edges to indicate a true 1 or 0 data bit. The comparator waveforms are depicted below.

ANTENNA MONITOR DATA SIGNAL A/D CONVERSION



Register A7 performs the fuzz filtering function. A7 is a four-mode shift register: parallel load, clear, shift left and shift right as a function of the state of the control inputs S0 and S1 which are driven by shift register E26. The 00 and 11 states of S0 and S1 clear and parallel load A7; these states never exist in this logic because A7 is driven by flip-flop E26 so that A7 sees only 10 and 01 states on the S0 and S1 inputs. These two states force left and right shifts of the data presented at the two data inputs: SR (shift right) and SL (shift left). The shift left input is tied to logic ground so that in shifting left, 0's are shifted into QD and move leftward through the register and the shift right input is floating (high) so that 1's are shifted into QA and move to the right through the register in the right shift mode. Note that the data is not **shifted through the register.** The contents of A7 may be all 1's, all 0's and either a 1/0 (eg. 1100, 1110 etc.) or 0/1 (eg. 0111, 0011, etc.) transition; multiple 1/0 or 0/1 transitions are impossible. Thus the 1's, 0's, and 1/0 or 0/1 transitions are pushed left or right in the register in accordance with the sequence of data states applied to the S0 and S1 inputs. Flip-flop C0605 is a noise-filtered replica of the BI-0 data stream and is set to the 1 state when the first 1 (shifting right) in the 1100 (etc) transition reaches QD. C0605 is reset when the first 0 (shifting left) in the 0011 (etc) transition sequence reaches QA. Therefore, to set C0605 to the 1 state there must be an unbroken sequence of four 1's (or five 1's if there is a 0, six 1's if there are two 0's etc). The converse is the case for the reset of C0605. The simplified timing diagram below illustrates how the "fuzz" on the edges of the data bits are integrated by this circuit.

BI-Ø MONITOR DATA SIGNAL EDGE NOISE FILTER TIMING

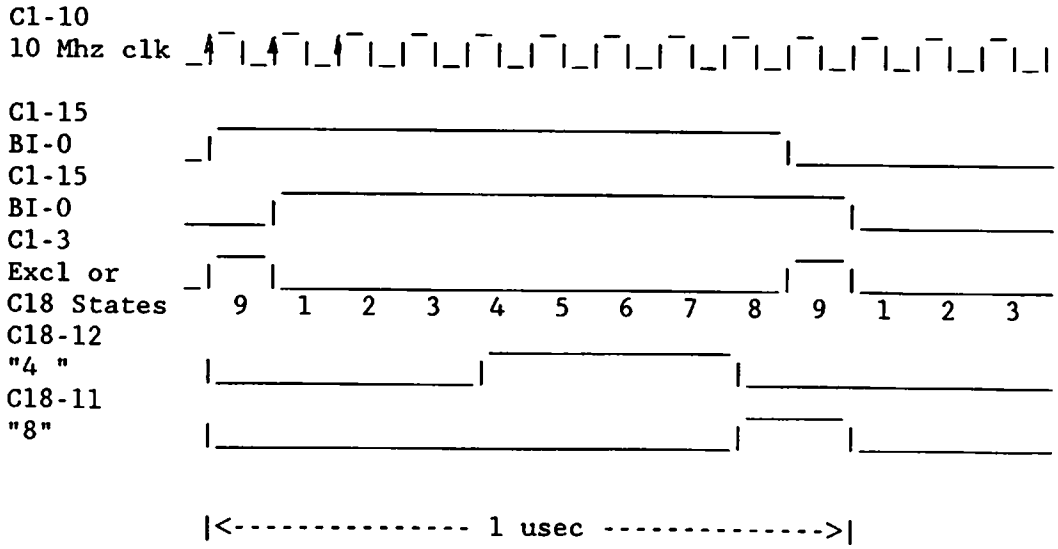


At this point you may ask: "Under what conditions does this filter fail?". The filter fails when the signal is so badly

obscured by noise that there are four consecutive false 1's or 0's; this will cause erroneous outputs. The period of such an event is 400 ns. The amplitude of a noise signal perturbation large to cause this sort of damage would be in excess of 1 volt; the comparator must be driven in the opposite direction, past the switching threshold. A signal this badly contaminated by noise is completely unuseable because the parity error rate would be immense. A noise level this high would obscure the signal so badly that it would be difficult to recognize it by an oscilloscope observation of the L9 LO Receiver output.

BI-Ø SIGNAL EDGE SYNCRONIZATION -- Shift register C1, exclusive or C0203 and counter C18 develop clocking terms which are phased to the BI-Ø data edges; these terms clock the BI-Ø signal into 1/0 & 0/1 BI-Ø transition detection logic (C8, C13 E25 etc.) and clock the BI-Ø to NRZ integrator logic. Exclusive or C0203 senses the edges of the BI-0 signal and presets counter C18 to zero; terminal count (count = 9) feedback causes the counter to be preset to the count of zero so that C18's 4 and 8 outputs are 1 Mhz clocks which have diffferent phases; that is the rising edges occur at different count states. A 1st NRZ feedback from the BI-Ø to NRZ integrator inhibits the edge-phasing during the period of demodulation of the BI-Ø signal; as a result counter C18 fly-wheels through the message period after it has been initialized to the BI-Ø signal at the start of a message. The operation of this logic is depicted in the simplified timing diagram below.

BI-Ø SIGNAL EDGE SYNCHRONIZATION



BI-Ø TO NRZ DEMODULATOR -- This not very obvious circuitry performs the function of reconstituting the NRZ data stream from the BI-Ø modulated signal. The demodulation process involves sensing BI-Ø bit edges, sampling each half of the 500 Khz BI-Ø

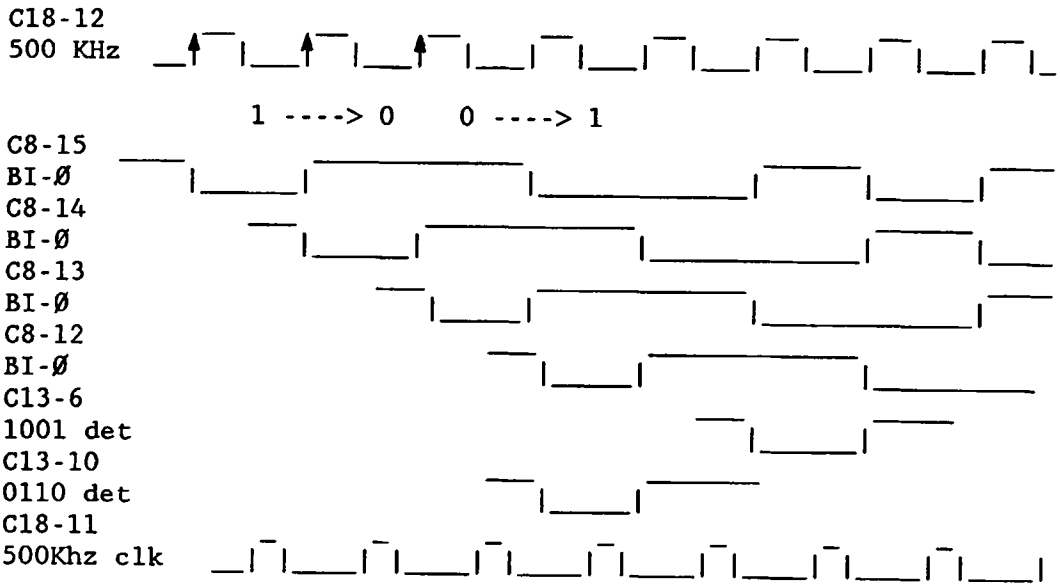
signal, performing a comparison of successive portions of the signal to sense phase reversals, integrating the BI-Ø to NRZ conversions over a period of 10 Bi-Ø cycles and finally developing an NRZ data shift clock.

Remember that the AB monitor data message bit rate is 50 Khz; there are 10 Bi-Ø cycles in each S bit and 20 Bi-Ø cycles in each message bit. Over an S or message bit the sense of the BI-0 carrier phase is constant, (if not altered by noise). It would be possible to sense the 1/0 and 0/1 phase reversals at the beginning of each NRZ bit and use only these transitions in reconstituting the NRZ data but this approach throws away most of the power in the signal because the logic decision would be based upon only one cycle of the available ten cycles in the bit period; the signal power in the balance would be ignored. A better approach is to test the phase of the Bi-Ø signal over the whole bit period and make the NRZ bit decision on the basis of the number of phase comparisons. With this approach the NRZ bit decision is based upon an integration of the phase structure of the BI-Ø signal over the period of the whole NRZ data bit. This integration approach is the essence of the CB BI-Ø to NRZ demodulation logic.

BI-Ø data is shifted through register C8 at a 1 Mhz rate to test each half cycle of the BI-Ø structure; two cycles (four register bits) of the BI-Ø signal stream are tested by gates C1306,10. These detect 1001 and 0110 patterns in C8, - the patterns for 1/0 and 0/1 BI-Ø phase bit transitions. These gate outputs are the steering inputs for J/K-bar flip-flop E2506 so that E2506 is set by the 1 Mhz clock whenever there is a 0/1 BI-Ø bit transition in the bit stream and is reset by a 1/0 transition. Since E2506 is a J/K-bar flip-flop, the state is not altered by the clock if the J input is high and the K-bar is low; these are the conditions when there is <u>not</u> a 1/0 or 0/1 transition, (look at the truth table in a data book). Therefore, having been initially set (or reset) by the 1/0 or 0/1 transition at the start of a data bit, if no phase transitions occur, E2506 will remain in this state until the next Bi-Ø bit phase transition.

The BI-Ø 1/0 and 0/1 phase transition detector timing is depicted on the next page.

BI-Ø 1/0 AND 0/1 TRANSITION TIMING



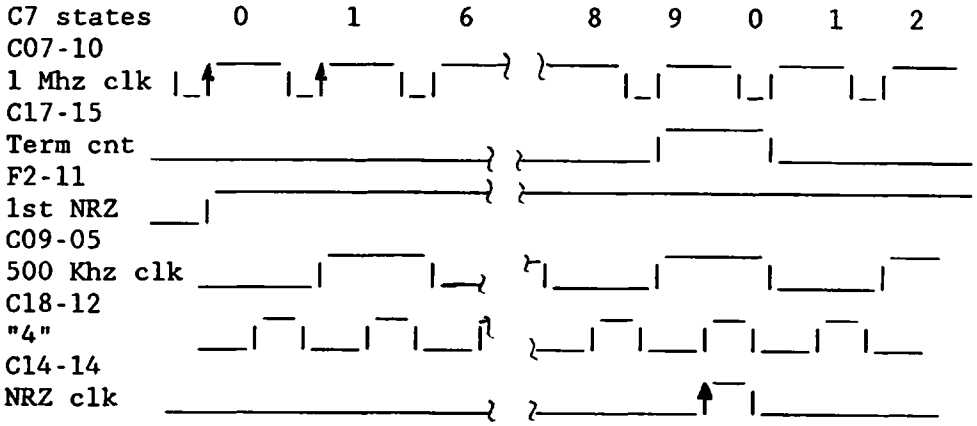
We have shown how the the phase transition detector logic works; we will now consider how the signal is integrated. The most probable effect of noise perturbation to the signal (say in the LO Receiver) is false 1/0 or 0/1 transitions; we want to integrate out these perturbations over the period of an NRZ data bit period. Flip-flop E2506 is an up/down steering input to binary up/down counter E21 which is clocked by a 500 Khz clock from C0905. At the beginning of an NRZ data bit period, counter E21 is preset to a count of 8; this count will be incremented by a 500 Khz clock if the U/D input is low and decremented if the U/D input is high. If there are 1/0 or 0/1 phase transitions during a data bit period, the count state of E21 at the end of the bit period will depend upon the relative number of 0/1 and 1/0 transitions during this period. The count state of E21 is compared with a count of 8 by the magnitude comparator E22; if the state of E21 is 8 or more (up to a maximum of 15) gate C2915 provides a high (ie. NRZ 1) to the serial input of the S detect shift register C19. The NRZ data 1/0 bit decision is performed when C19 is clocked to load the NRZ data into C19. The increment/decrement sequence of E21 states is thus an integration of the BI-0 signal phase states over an NRZ data bit period. The initialization of counter E21 to a count of 8 base is equivelent to an NRZ 1; if the NRZ data bit is a 0, this count will be decremented.

Having shown the essence of the BI-Ø to NRZ conversion and integration, it is clear that this logic must be initialized and the bit periods must be timed to perform the NRZ decision. Counter C17 and associated logic perform this function. Initially, flip-flop E2506 is set to the 1 state (equivelent to a NRZ 0 bit); the first 1001 pattern at the start of a message, (a

BI-Ø 0/1 transition) at the K-bar input clocks flip-flop F0211 to a 1 state; this 1st NRZ word term freezes the edge-phasing of counter C18 (discussed above) and lifts the pre-load on the U/D counter E21 so that it is free to count. The 1st NRZ word term also lifts the pre-load from counter C17 so that it can generate an end-of-bit strobe to the magnitude comparator, E22 to enable the NRZ bit decision. Counter C17's TC is fed back to it's pre-load to cause it to continue to generate end-of-bit strobes for the balance of the message. Flip-flop C0905 is phase-initialized by the 1st NRZ word term and toggles to produce a 500 Khz clock to the U/D counter. Counter C17's TC also reloads a count of 8 into the U/D counter E21 to integrate the BI-0 over the next NRZ bit.

The NRZ data is clocked into the S detect shift register, C19 by gate F2610 which combines the C17 TC end-of-bit term, the 500 Khz clock from C0905 and 1 Mhz clock from C1812. The operation of this logic is depicted in the simplified timing diagram below.

BI-Ø TO NRZ INTEGRATOR TIMING



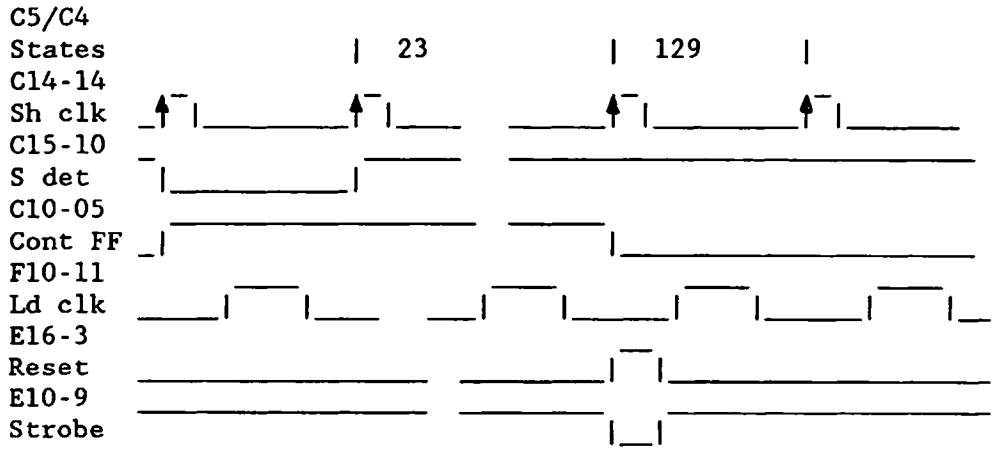
The NRZ data serial memory (Sheet 5) load clock is generated by flip-flop F1011. Counter C1712 ("4") clocks flip-flop F1011 high and C1711 direct resets it; the result is a 50 Khz clock which goes high at state 4 of C17 and low at state 8.

As the NRZ data shifts through register C19, the message start character prefix S is detected by gate C1610 which starts the message load counter C05 and C04. Control flip-flop C1005 is set and C5/C4 are loaded with a count of 23. C1005 permits the counter to count by enabling the Cep input and provides a load enable to permit the NRZ data to be clocked into the serial monitor data memory by gate A1810. The counter is clocked by the C19 shift clock; at the count of 129, gate E1403 triggers E1009 which resets the control flip-flop and also resets the 1st NRZ word flip-flop F0211 to initialize the integrator for the next message.

Counter control flip-flop C1005 output is used as an enable to load the antenna monitor data message into the serial monitor data memory (Sheet 5). Gates A1810 and B2614 are enabled by this load control term; the serial data is loaded into the memory on a message by message basis. 106 shift clocks are generated by this load control counter; 6 spacing bits are loaded between messages.

The operation of this logic is depicted by the simplified timing diagram below.

ANTENNA MONITOR DATA MEMORY LOAD TIMING



470 ohm pull-up resistors are used on the memory data and clock inputs; the AMD 2855PC requires a high input greater than 4 volts, a marginal level for TTL logic; the pull-up resistor provides a 5 volt level. These serial memory chips shift on the fall of the clock rather than the rise like the other shift registers in the CB. The data sheet for this chip is included in this manual.

3.4 CENTRAL DATA SET MONITOR DATA POLLING, LOADING AND STORAGE

Having loaded the antenna monitor data into the serial monitor data memory, we will now consider the operations of polling the central Data Set (#5) for central electronics monitor data.

Flip-flop C1011 (Sheet 4) is clocked low at t = 48400 and 49400 by gate D0710 and direct set high by the 20 usec term from counter D16. This 20 usec low-true term loads a Q into shift register C11 and A1 (Sheet 1); when the load term rises the 200 Khz shift clocks push out the Q through or gate A0806 and the low-true Data Set Command Port J2-25/25. Register stage A0110 provides an initial 0 to the Q character so that the first 1 is the proper 5 usec.

The Data Set should respond to the Q within 50 usec and begin to output the monitor data message within 250 usec after the

start of the Q. The low-tru monitor data message evoked by th Q is input on the Data Set Monitor Data Port, J2-22/23. Optical isolator A2614 detects and inverts the signal. Shift register A29 and exclusive or A2403 detect signal edges to synchronize counter A9/A10 which samples the signal in the center of the pulse. Counter A9/A10 is preset to a count of 1 by the exclusive or A2403 and is clocked by 5 Mhz. At the count of 37 gate A1506 goes true and feeds back to the pre-set input through A1502,- thus the radix is 37. At the count of 32, the 16 term in A10 falls which generates a shift clock (via inverter F1614). The 200 Khz 32 term in A10 clocks the serial data stream into S detect register A20. When the S is detected by gate A1410, a message loading sequence is initiated in which load control flip-flop B0105 and counter A4/A5 generate a load enable to permit the monitor data message to be loaded into the serial monitor data memory. The counter is preset to a count of 151; at the count of 256 (i.e. when all bits fall), control flip-flop B0105 is reset which inhibits the monitor data load clocks and data at gates B2614 and B21610 respectively. Flip-flop D1910 is an enable flip-flop which is clocked permissive at the trailing edge (rise) of the 24,000 - 48,000 antenna monitor data enable. This term permits the input of monitor data from the central Data Set only when it is being polled. Flip-flop D1910 is direct cleared by the term 50.8 from D1806, (Sheet 4).

It is worthwhile to consider the order of the monitor data messages in the monitor data memory. The monitor data memory (F15, F14, F13) is a set of quad 128 bit MOS shift registers (identical to those used in the Antenna Buffer). The order of data in the memory (looking into the memory from the output) is the antenna monitor data: MW-1, DS-0...DS-4; MW-2, DS-0...DS4; MW-1, DS-5; MW-2, DS-5. At the end of the central Data Set load, this data and some spacing bits are pushed deeply into the memory but are not at the output; message positioning logic at the bottom of Sheet 5 performs this function. Because the SLC monitor data polling period is very short; 59 usec, there is not enough time to wait for the first (or subsequent) monitor data messages to shift to the memory output. In operation, this logic positions the monitor data messages at the output of the memory so that it is immediately available when polled by the SLC. The message positioning logic detects the S character and halts the shift process in anticipation of the next Q character.

The first monitor data message is positioned at the memory output so that it is ready for immediate output at the beginning of the next cycle. At t = 0, the low-true 100 ns psuedo QQ pulse from gate D2203 (Sheet 4) direct sets flip-flop F1005 through low-true or gate F2203 (gate F2203 should be drawn as an or with bubble inputs). This control flip-flop permits 2 Mhz push clocks to shift the memory contents via gate B0610 until stopped by the S detect gate F0810 which resets flip-flop F1005. This 2 Mhz clock is phased to the Q detection logic (Sheet 1, discussed below) so

that the data unload clock is coherent with the SLC Q edges.

3.5 SLC MONITOR DATA POLLING

Having loaded the serial monitor data memory and positioned the first message at the memory output let us now consider the SLC polling and monitor data output to the SLC. The SLC polls each CB in the sequence: DCS-0...DCS-32; DCS...DCS32; etc for a total of 12 cycles. The time intervals of the SLC Q at a given buffer is therefore 32 x 59 usec or 1888 usec. When an SLC Q is detected, the low-true Q detection gate, B0910 (Sheet 1, SLC Q detection is discussed above in the SLC command detection logic) sets flip-flop F1005 through low true or gate F2203 which permits unload clocks to shift the message out to the SLC via the SLC Monitor Data Port, J2-6. The unload operation is terminated when the S character of the next message is detected via gate F0810.

Note that the action of this unload logic is just the reverse of all the S detect/load control counters in the Monitor and Control System; in all other cases the S detection causes a message load sequence; in this logic it terminates a message unload sequence, (except for the first message initialization case).

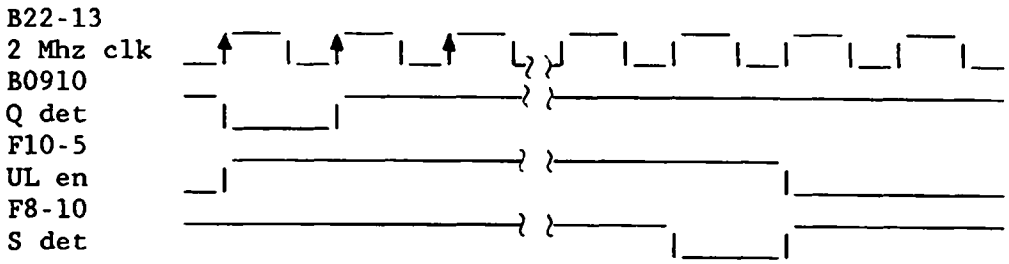
The control flip-flop F1005 is is permitted to operate only during the period of 0 - 24,000 by the enable 0 - 24,000 from flip-flop F2005, sheet 4 which direct resets the unload clock control flip-flop F1005 at all times except during this aperature. Enable 1k - 24k at gate F0503 enables the monitor data output to the SLC during the SLC polling period.

One shot F2710 provides up to 250 ns of delay of the memory shift clocks for shift register F4; this delay is to accomodate the worst case propagation delay of the AM 2855PC monitor data memory. The delay should be set up by checking the eye pattern of the data and clock on an oscilloscope.

An important use of flip-flop F1005 is the "inhibit gossip data" feedback to the SLC Command Signal Input logic. When the CB outputs a monitor data message to the SLC, it is immediately rebraodcast on the SLC command output lines to the CB's Command Signal Input which will edge phase a sampling clock to the incoming message stream. Since the monitor data unload clock is this edge-phased clock this would be a positive feedback situation were it not for this gossip data inhibit term.

The timing of the SLC polling/monitor data unload logic is shown on the simplified timing diagram on the next page.

MONITOR DATA UNLOAD TO SLC



MASTER LO INTERFACE -- The LM318 operational amplifier circuitry shown on the upper right corner of Sheet 5 is no longer used. This circuitry was used to enable the AB to communicate directly with the CB for use in the Master LO System but this scheme proved to be unsatisfactory; the System Buffer (M14) was developed for control/monitoring situations in which the LO/WG System timing, message signal format (i.e. no BI-Ø) and Data Set location constraints were not a factor.

3.6 POWER CIRCUITS

The analog comparators and the MOS memories require non-standard -12 volt, +12 volt and -5 volt power; Motorola MC7905 and MC79812 regulators provide the negative voltages and a Motorola MC7812 provides the +12 volt power. These regulators require isolation of the case from module ground; if these chips fail, don't forget to replace the mica washers and Silicone grease when replacing them. If non-Motorola replacements are substituted, be sure of the wiring because other manufacturers regulators have similar part numbers but a different pin-out.

4.0 List of Additional Central Buffer Drawings

D13720P80	Central Buffer Top Assembly Drawing
A13720Z24	Central Buffer Top BOM
D13720L48	Central Buffer Logic Schematic
A13720W12	Central Buffer Master Wire List
A13720W13	Machine Wire List
A13720W14	Hand Wire List
A13720W15	Connector Wire List
A13720W48	I/O Connecator (J2) Wire List
B13720AB05	LED Display PCB Artwork
C13720M36	LED Display PCB Drill Drawing
C13720P39	LED Display Assembly
C13720M16	Front Panel Fabrication Drawing
A13720P81	IC Module Assy (IC Map)
B13050M17	Perf Cover Fastener
C13050M07	1W Perf Cover
C13720M15-1,2	Rail Modification
C13720M17	Insulated Spacer
C13720M23	Rear Panel
C13720M32	DCS Module WW Field Dim Def
C13720M50	Side Plate, Modified
C13720P68	Insulated Side Plate Assy
B13720M49	Side Plate Insulation
B13720M47-1	Module Bar Spacer
D13720M96	Buffer Wiring Jig Configuration

See the Drafting Drawing Listing for Dip Header drawings

6.0 Special Module Data Sheets

The Data Sheet for the AM2855PC MOS serial memory chip follows.

Am2855 • Am2856 • Am2857

Quad 128-Bit, Dual 256-Bit and Single 512-Bit Static Shift Registers

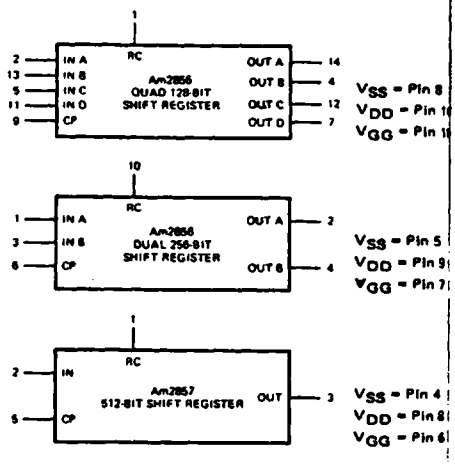
Distinctive Characteristics

- High-speed replacement for National 5055/6/7
- Internal recirculate
- Single TTL compatible clock
- Operation quaranteed from DC to 2.5MHz
- 100% reliability assurance testing in compliance wi MIL-STD-883

FUNCTIONAL DESCRIPTION

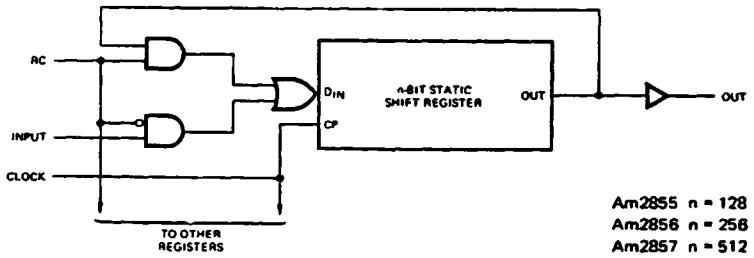
These devices are a family of static P-channel MOS shift registers in three configurations. The Am2855 is a quad 128-bit register; the Am2856 is a dual 256-bit register; and the Am2857 is a single 512-bit register. All three devices include on chip recirculate. The registers are all clocked by a single low-level clock input. Because the registers are static, the clock may be stopped indefinitely in the LOW state without loss of data. Each of the registers has a single data input; data on the input is written into the register on the HIGH-to-LOW clock edge. A single recirculate control (RC) on each chip determines whether the registers on that chip are to write data in from the data inputs or recirculate the data appearing on the output. If RC is LOW, new data is written in; if RC is HIGH then the data on the output will be written back into the register input on the next clock pulse.

LOGIC SYMBOLS



MOS-440

LOGIC BLOCK DIAGRAM
(One Register Shown)



Am2855 n = 128
Am2856 n = 256
Am2857 n = 512

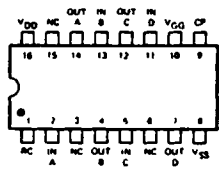
MOS-44

ORDERING INFORMATION

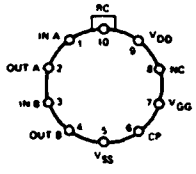
Package Type	Temperature Range	Order Number
16-Pin Molded DIP	0°C to +70°C	AM2855PC
16-Pin Hermetic DIP	0°C to +70°C	AM2855DC
16-Pin Hermetic DIP	−55°C to +125°C	AM2855DM
10-Pin Plastic DIP	0°C to +70°C	AM2856PC
TO-100 Can	0°C to +70°C	AM2856HC
TO-100 Can	−55°C to +125°C	AM2856HM
8-Pin Molded DIP	0°C to +70°C	AM2857PC
8-Pin Hermetic DIP	0°C to +70°C	AM2857DC
8-Pin Hermetic DIP	−55°C to +125°C	AM2857DM

CONNECTION DIAGRAMS

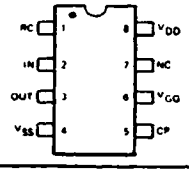
Am2855



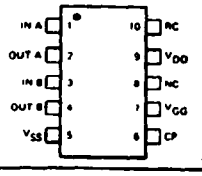
Am2856



Am2857



Am2856



MOS-

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +160°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{DD} Supply Voltage	V_{SS} −10V to V_{SS} +0.3V
V_{GG} Supply Voltage	V_{SS} −20V to V_{SS} +0.3V
DC Input Voltage	V_{SS} −20V to V_{SS} +0.3V

OPERATING RANGE

Part Number	Ambient Temperature	V_{SS}	V_{DD}	V_{GG}
Am2855DM Am2856HM Am2857DM	−55°C to +125°C	5.0V ±5%	0V	−12V ±5%
Am2855PC, DC Am2856HC Am2857PC, DC	0°C to +70°C	5.0V ±5%	0V	−12V ±5%

5

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −0.5mA	2.4			Volts
V_{OL}	Output LOW Voltage	I_{OL} = 1.6mA			0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	V_{SS} −1.0		V_{SS} +0.3	Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	V_{SS} −18.5		V_{SS} −4.2	Volts
I_{IL}	Input Leakage Current	V_{IN} = −10.0V, all other pins GND, T_A = 25°C		0.01	0.5	µA
I_{DD}	V_{DD} Power Supply Current	T_A = 25°C, $t_{\phi pw}H$ = 160 ns, Data = 1010. . . output open, f = 2.5 MHz		20.0	28.0	mA
I_{GG}	V_{GG} Power Supply Current			12.0	16.0	mA

Note: 1. Typical Limits are at V_{SS} = 5.0V, V_{GG} = −12V, 25°C ambient and maximum loading.

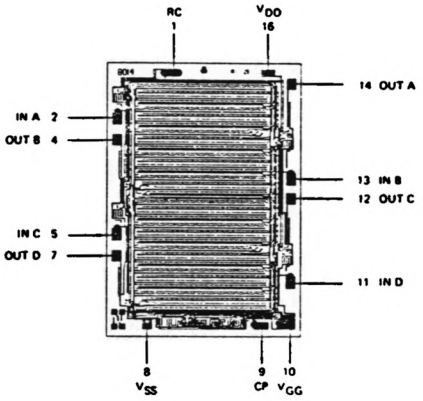
SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
f	Clock Frequency		0		2.5	MHz
$t_{opw}H$	Clock HIGH Time		0.16		10.0	µs
$t_{opw}L$	Clock LOW Time		0.200		∞	µs
t_r, t_f	Clock Rise and Fall Times		10		200	ns
t_s	Set-up Time, D or RC Inputs (see definitions)	t_r = t_f = 50ns	100			ns
t_h	Hold Time, D or RC Inputs (see definitions)	t_r = t_f = 50ns	40			ns
t_{pd}	Delay, Clock to Output LOW or HIGH	R_L = 4k, C_L = 10pF	(Note 3)	160	280	ns
C_{in}	Capacitance, Data In and RC Inputs (Note 2)	f = 1MHz, V_{IN} = V_{SS}		3	7	pF
C_o	Capacitance, Clock Input (Note 2)	f = 1MHz, V_{IN} = V_{SS}		3	7	pF

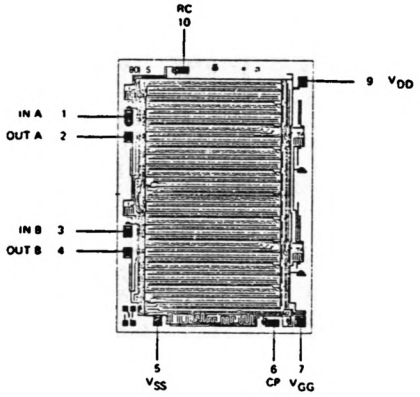
Notes: 2. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.
3. At any temperature, t_{pd} min. is always much greater than t_h(0) max.

Metallization and Pad Layouts

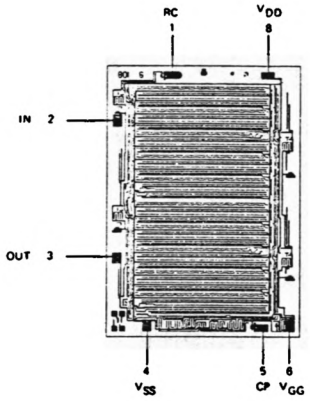
Am2855



Am2856



Am2857



DIE SIZES: 0.101" X 0.142"

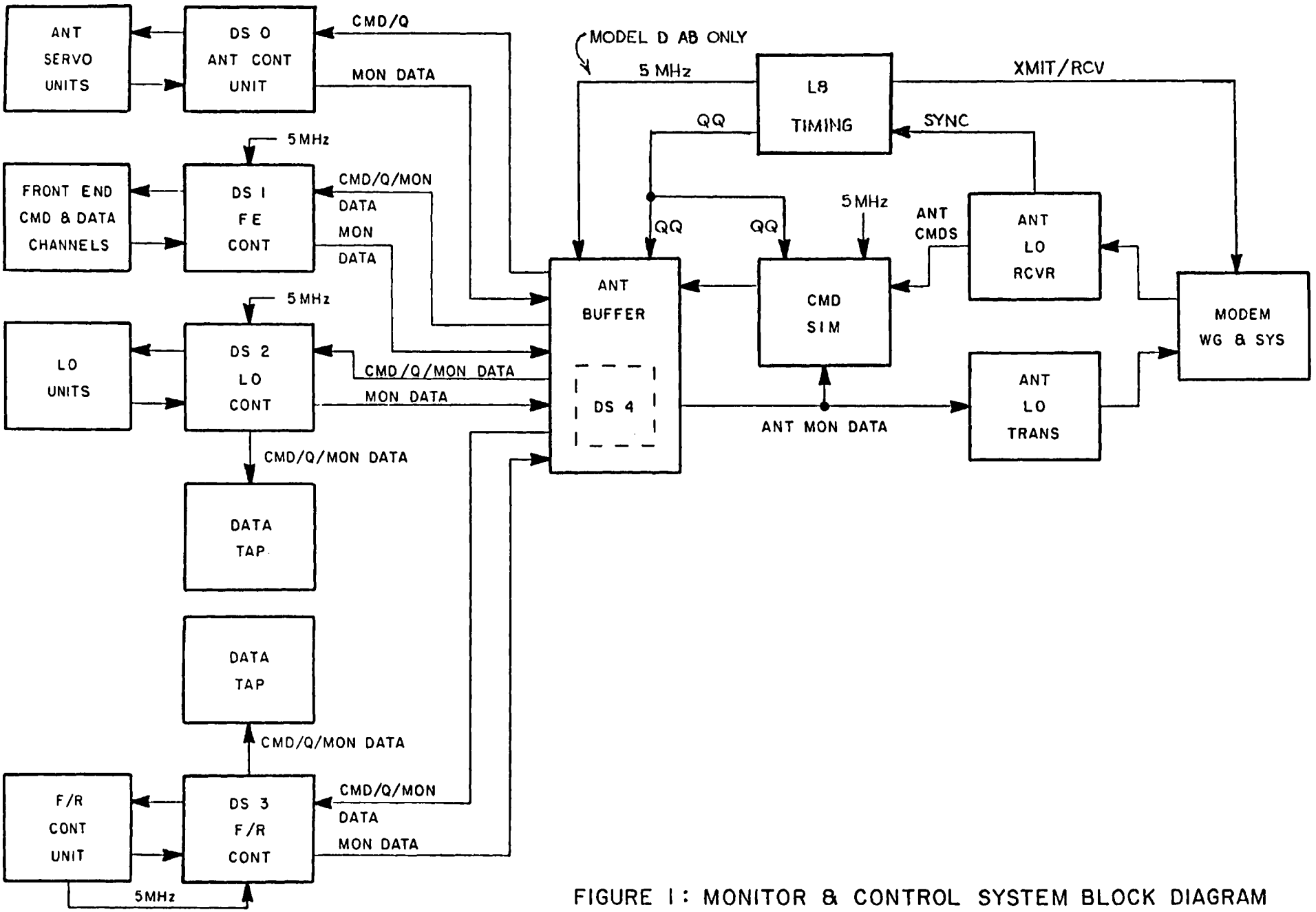


FIGURE 1: MONITOR & CONTROL SYSTEM BLOCK DIAGRAM

REV. 7-86

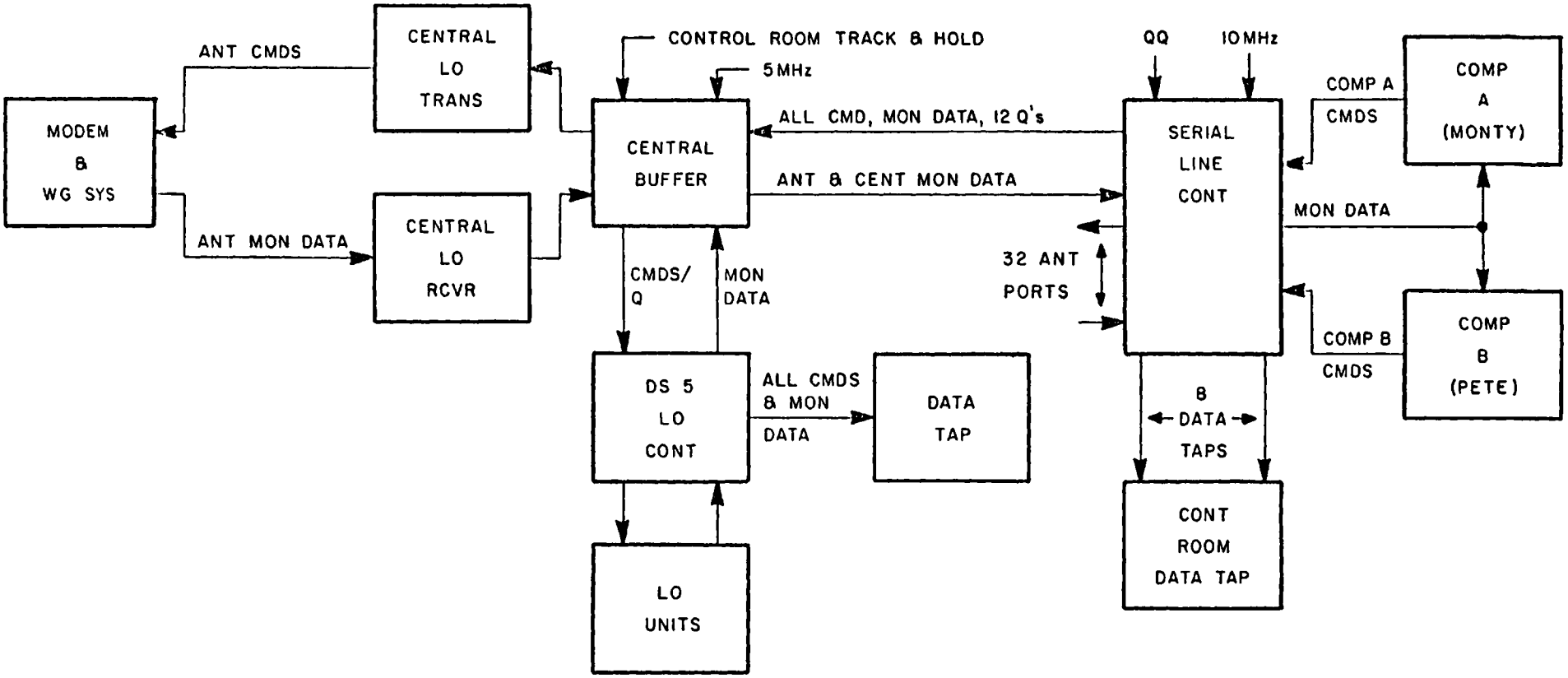


FIGURE 1: CONTINUED

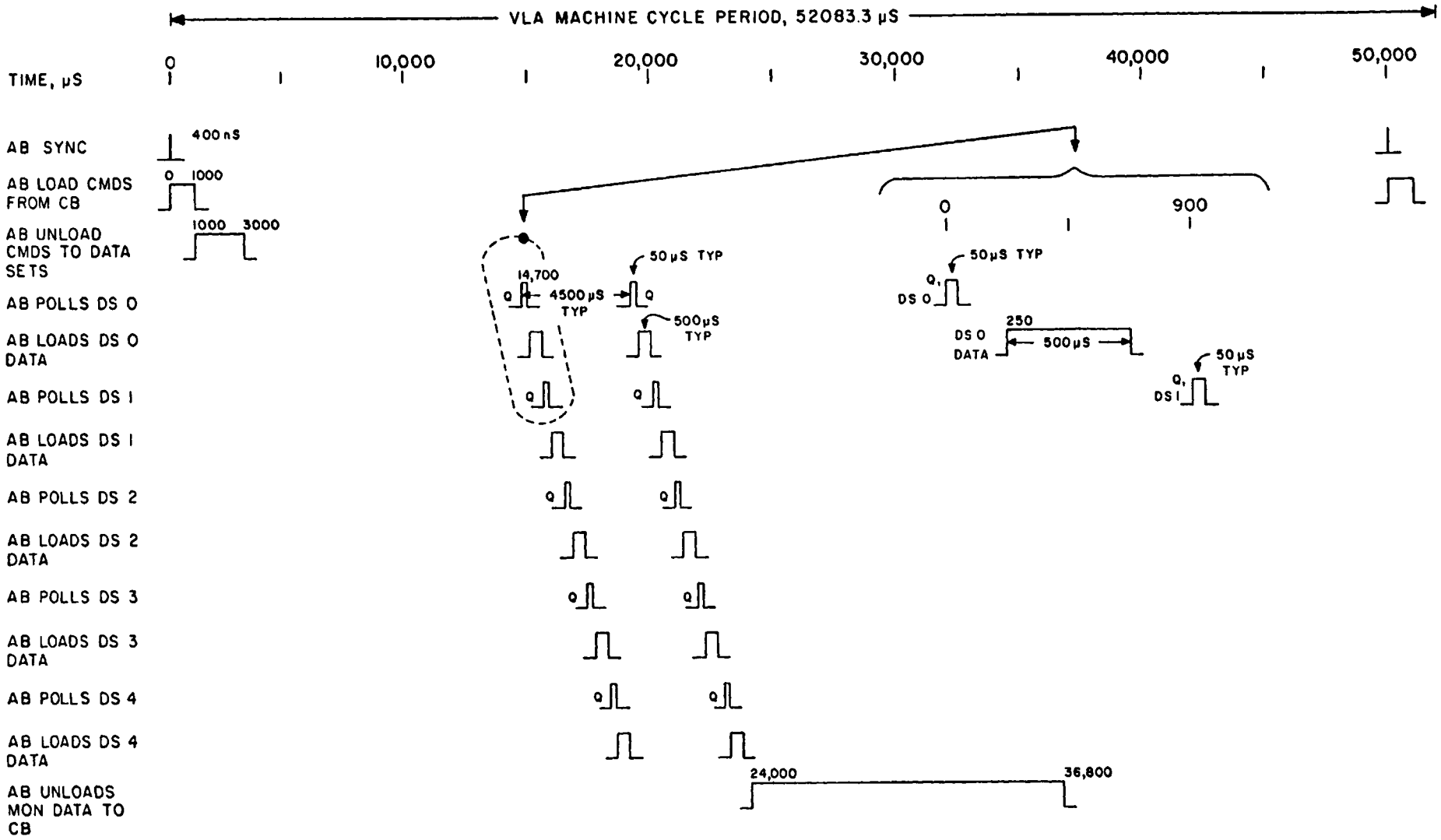


FIG. 2
ANTENNA TIMING OPERATIONS

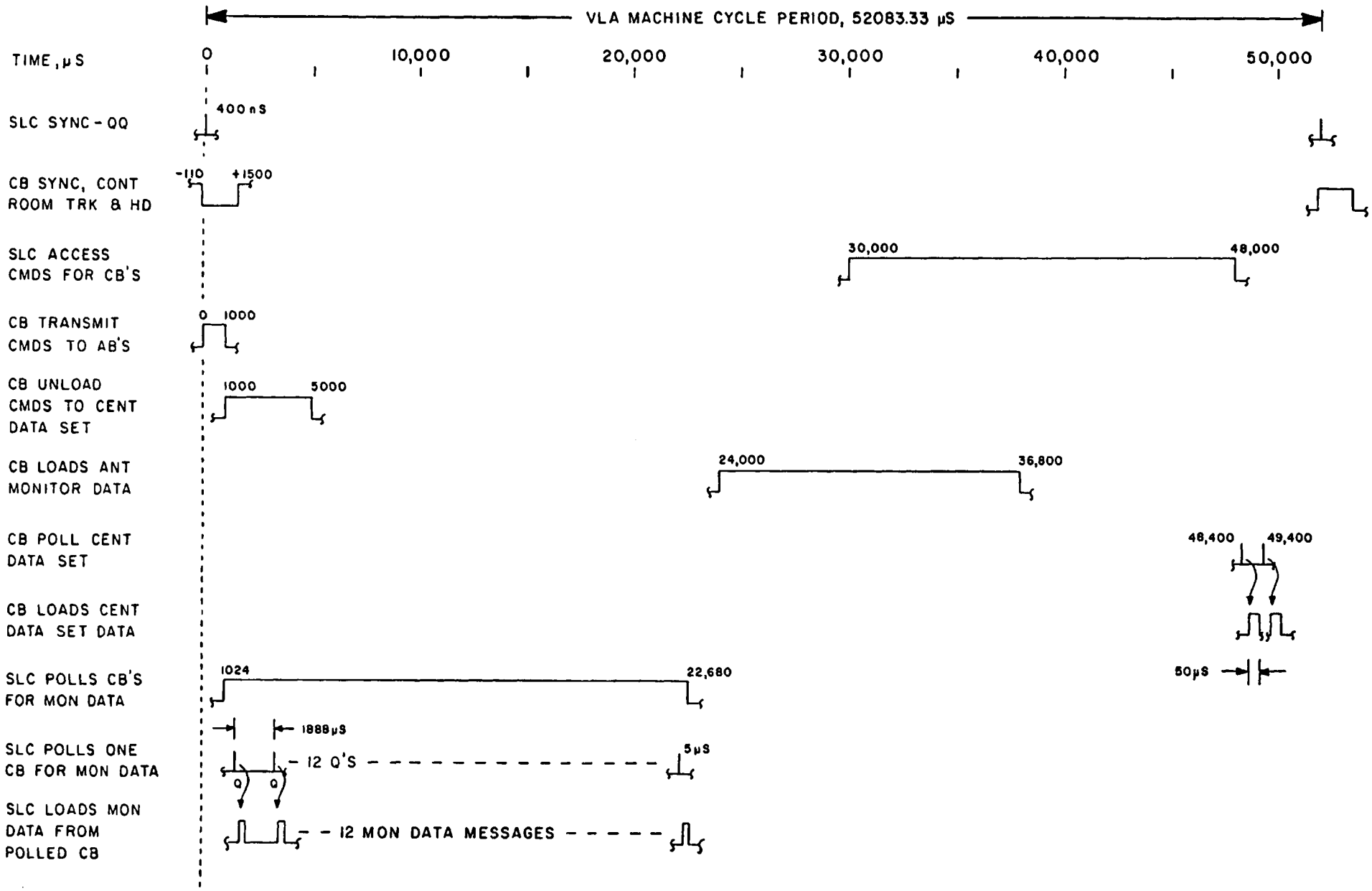


FIG. 3
CENTRAL TIMING OPERATIONS

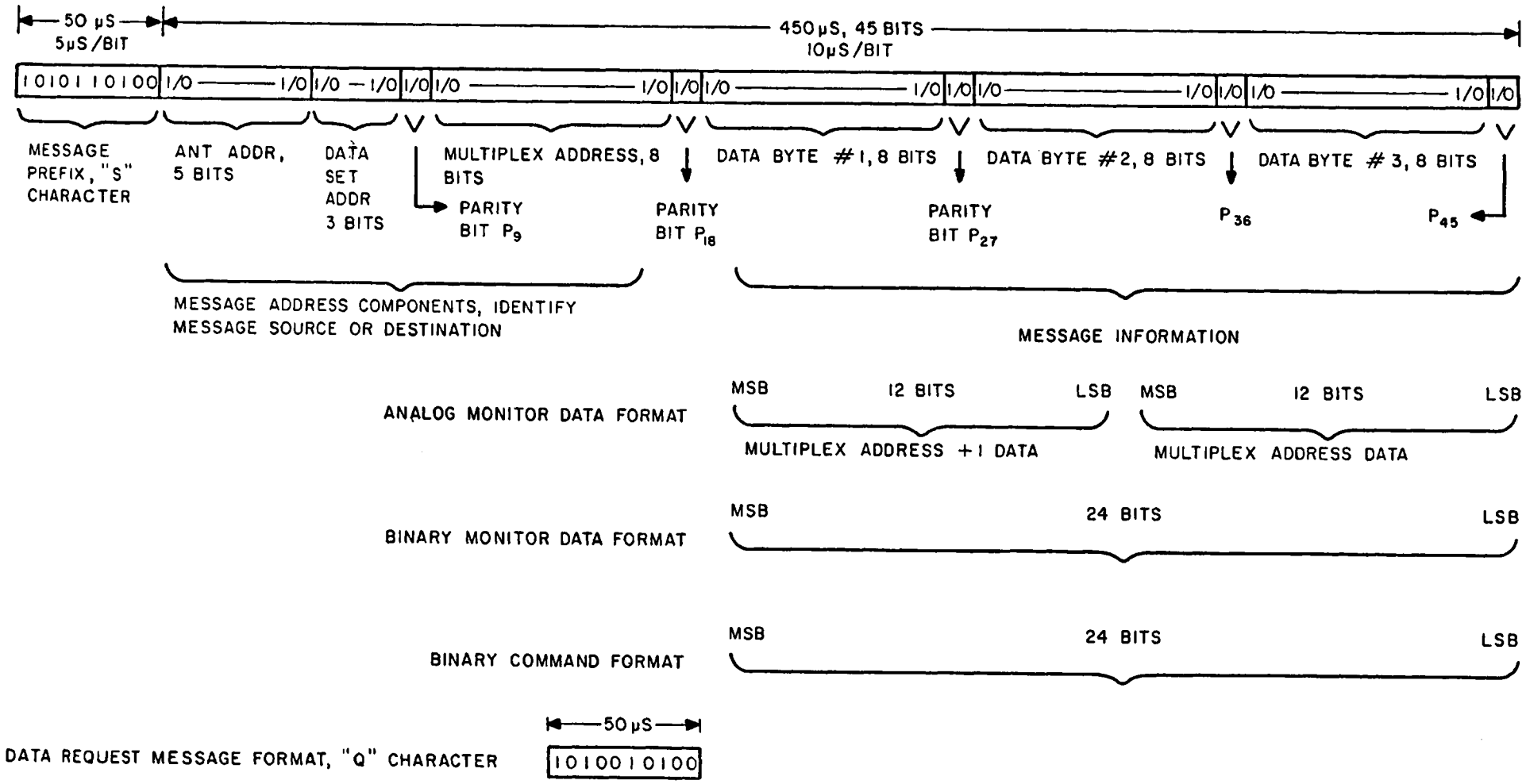


FIGURE 4: DATA SET COMMAND AND MONITOR DATA AND DATA REQUEST MESSAGE FORMATS

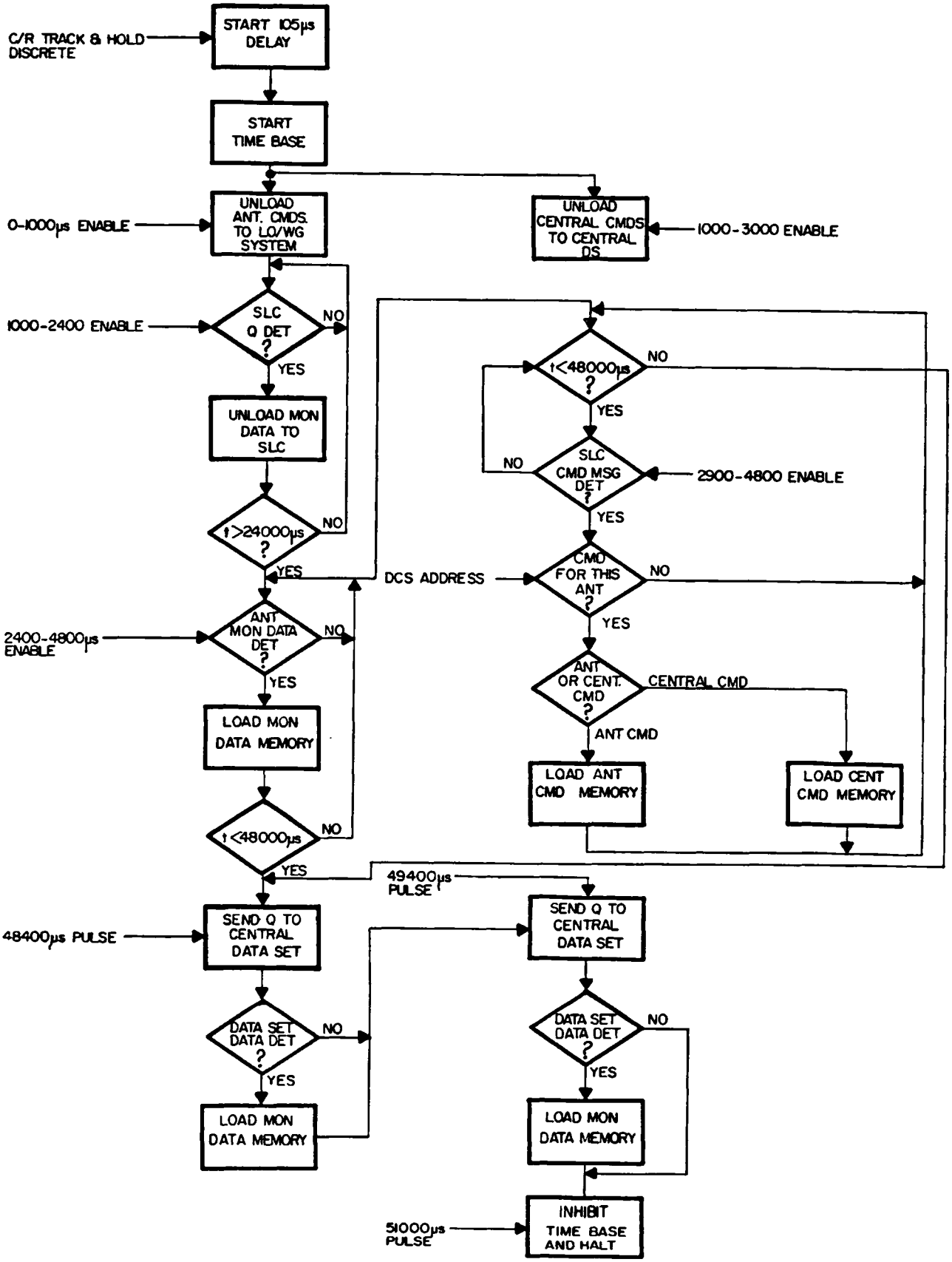


FIGURE : 5

CENTRAL BUFFER LOGIC OPERATIONS

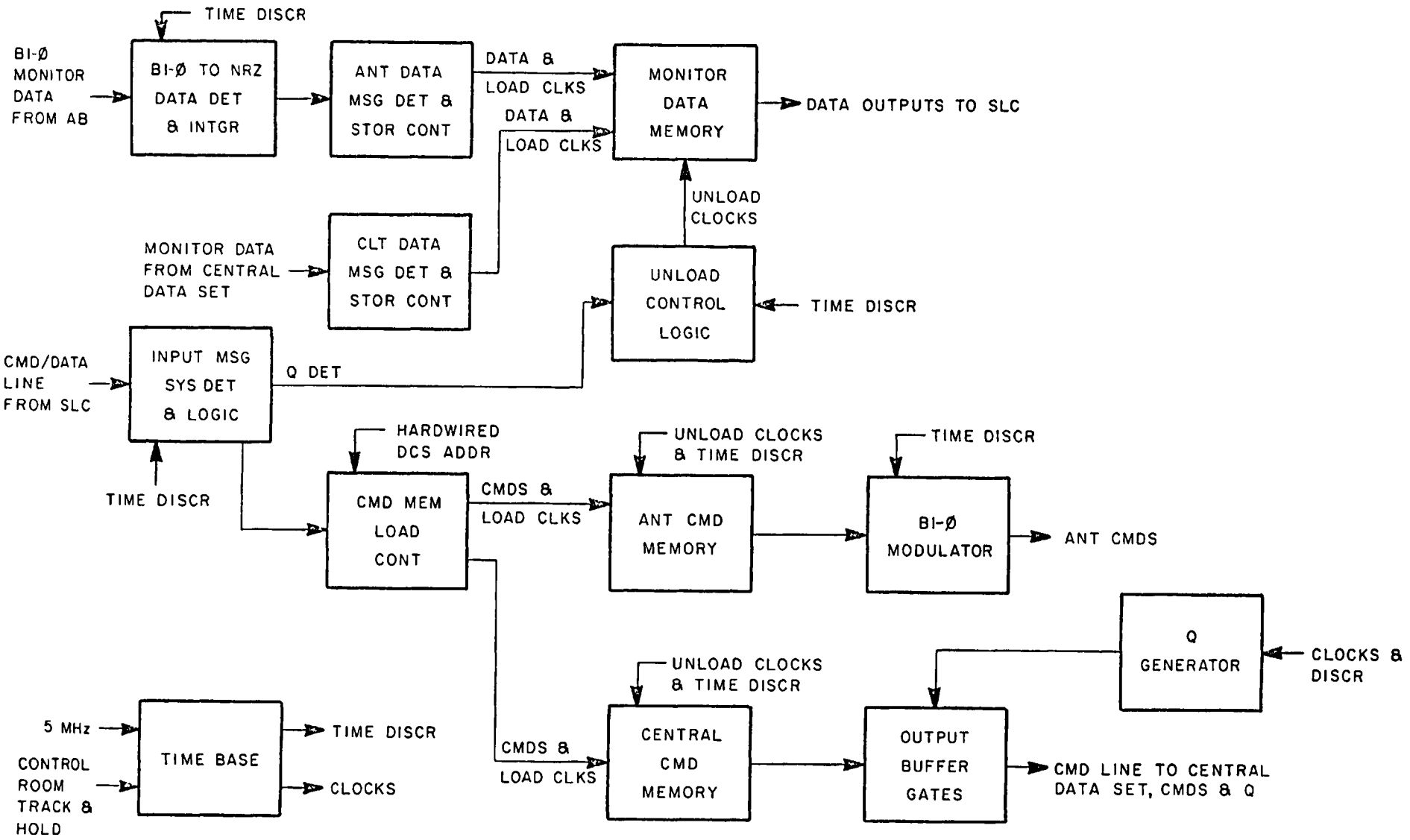


FIGURE 6: CENTRAL BUFFER BLOCK DIAGRAM

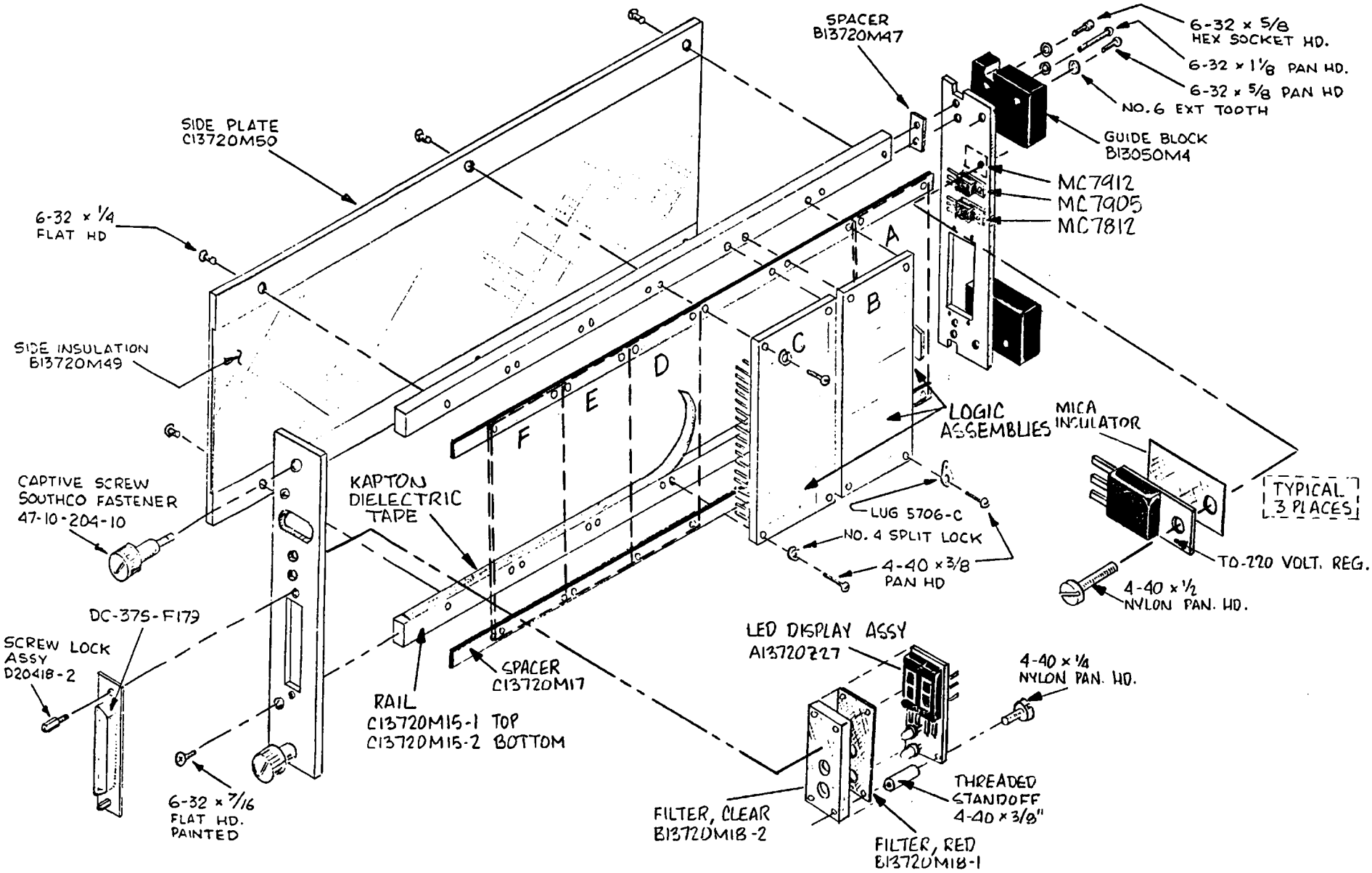
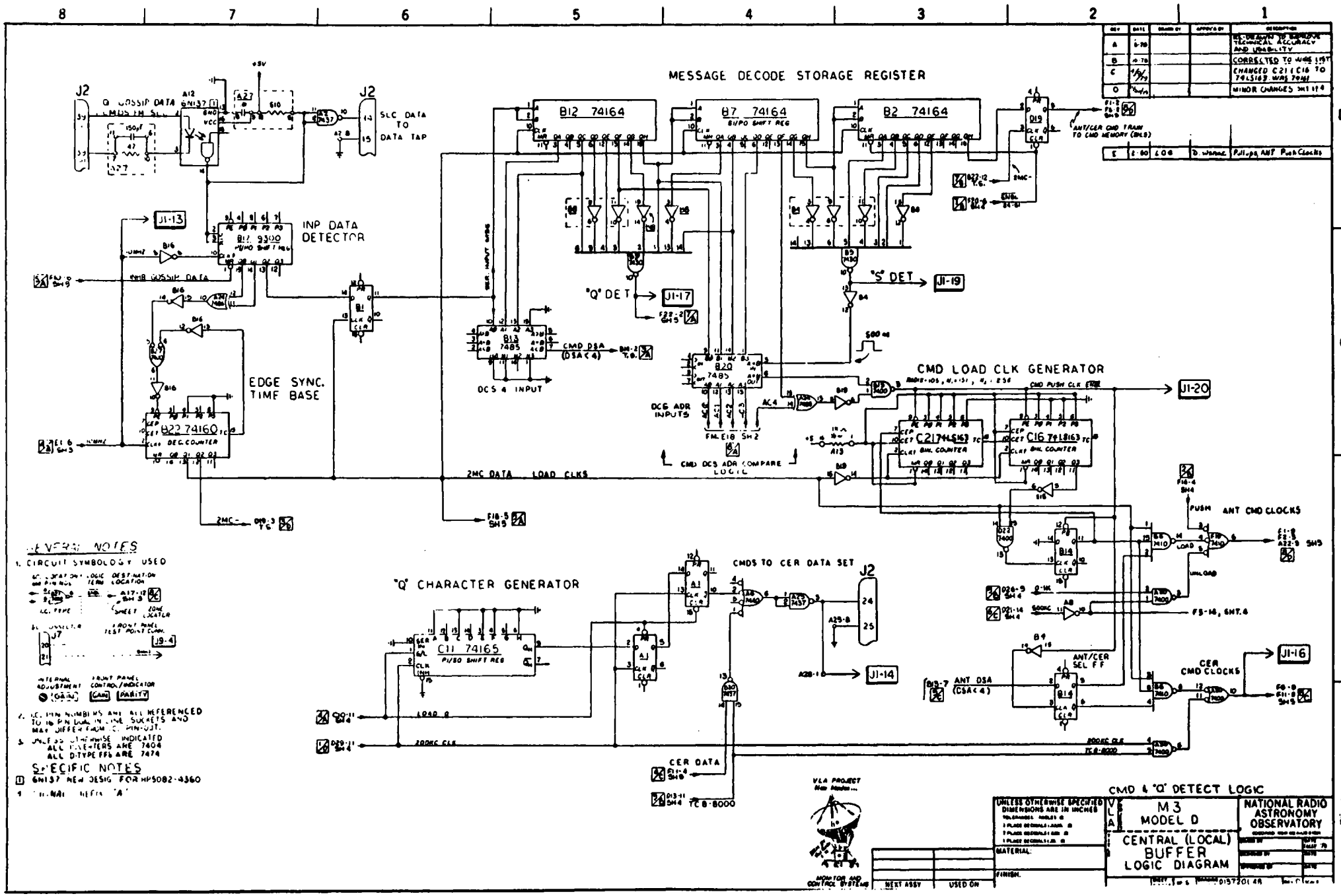
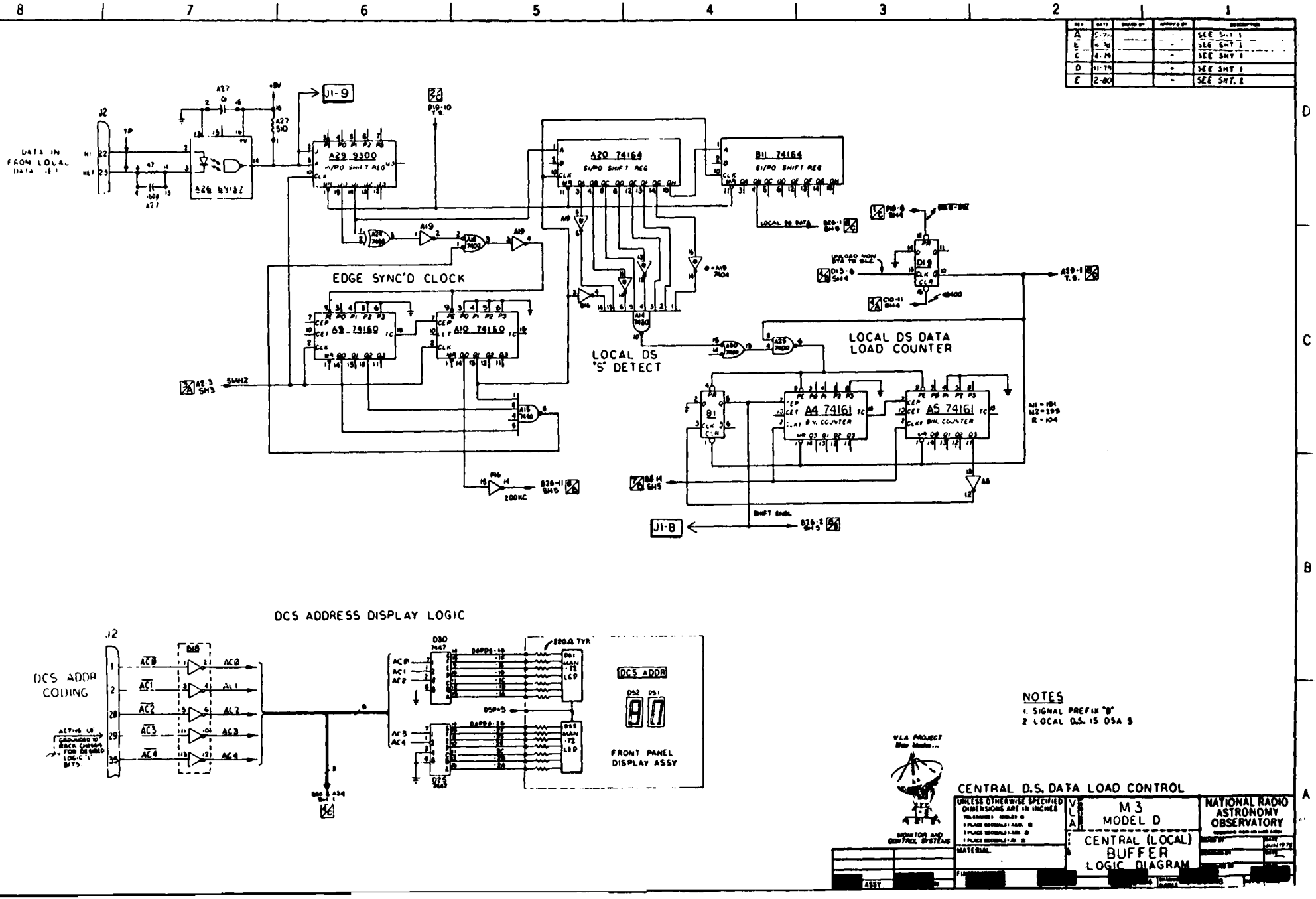


FIG.7
ILLUSTRATED PARTS BREAKDOWN
M3 LOCAL BUFFER


MESSAGE DECODE STORAGE REGISTER
B12 74164
B7 74164
B2 74164
INP DATA DETECTOR
EDGE SYNC. TIME BASE
"Q" DET
"S" DET
CMD LOAD CLK GENERATOR
CMD DCS ADR COMPARE LOGIC
"Q" CHARACTER GENERATOR
CMDS TO CER DATA SET
ANT CMD CLOCKS
CER CMD CLOCKS
ANT/CER SEL FF
CER DATA
2MC DATA LOAD CLKS
SLC DATA TO DATA TAP
J1-13
J1-14
J1-16
J1-17
J1-19
J1-20
CMD & "Q" DETECT LOGIC
M3 MODEL D
CENTRAL (LOCAL) BUFFER LOGIC DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY



NOTES

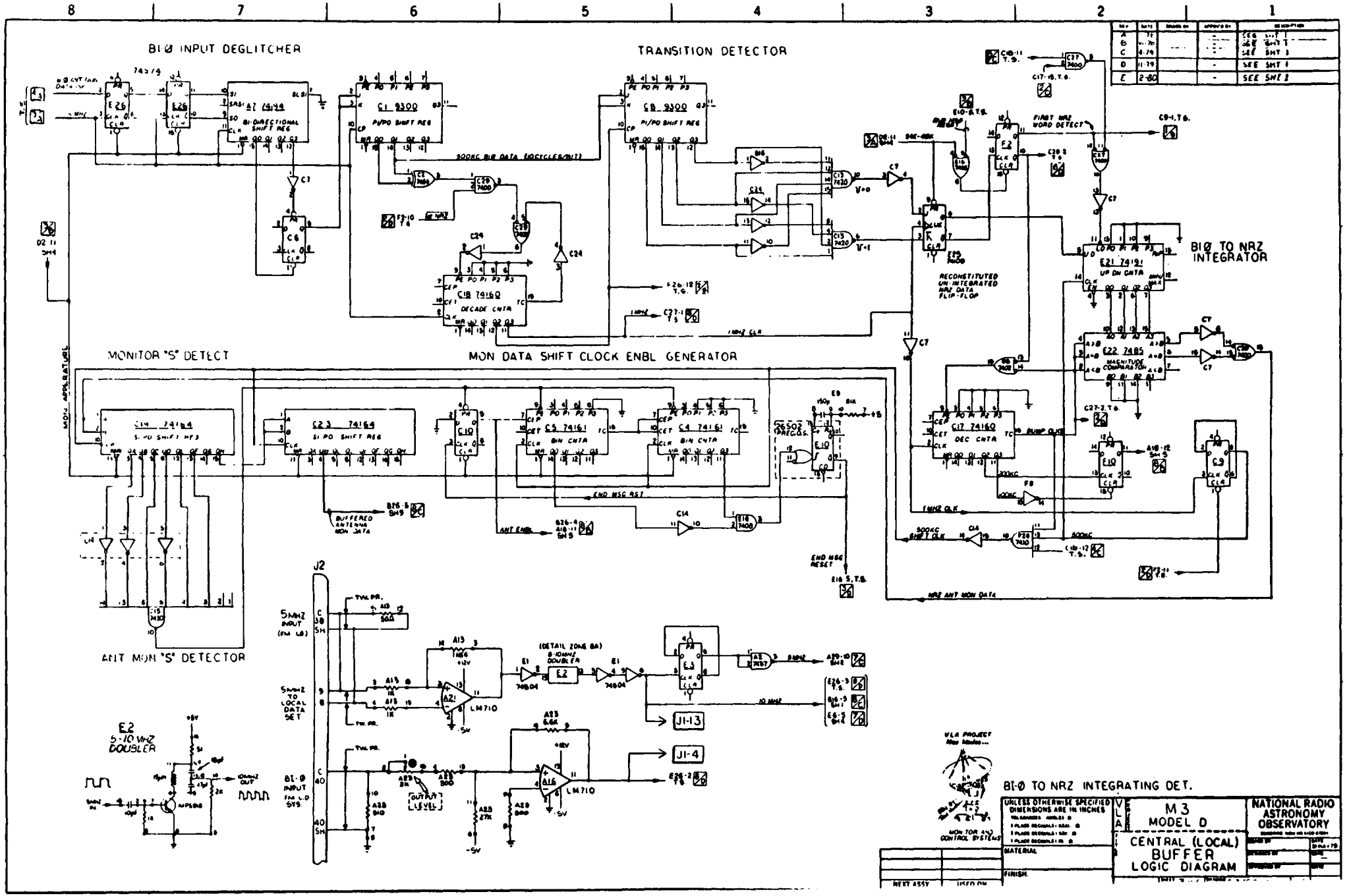
1. SIGNAL PREFIX "B"
2. LOCAL D.S. IS DSA 5

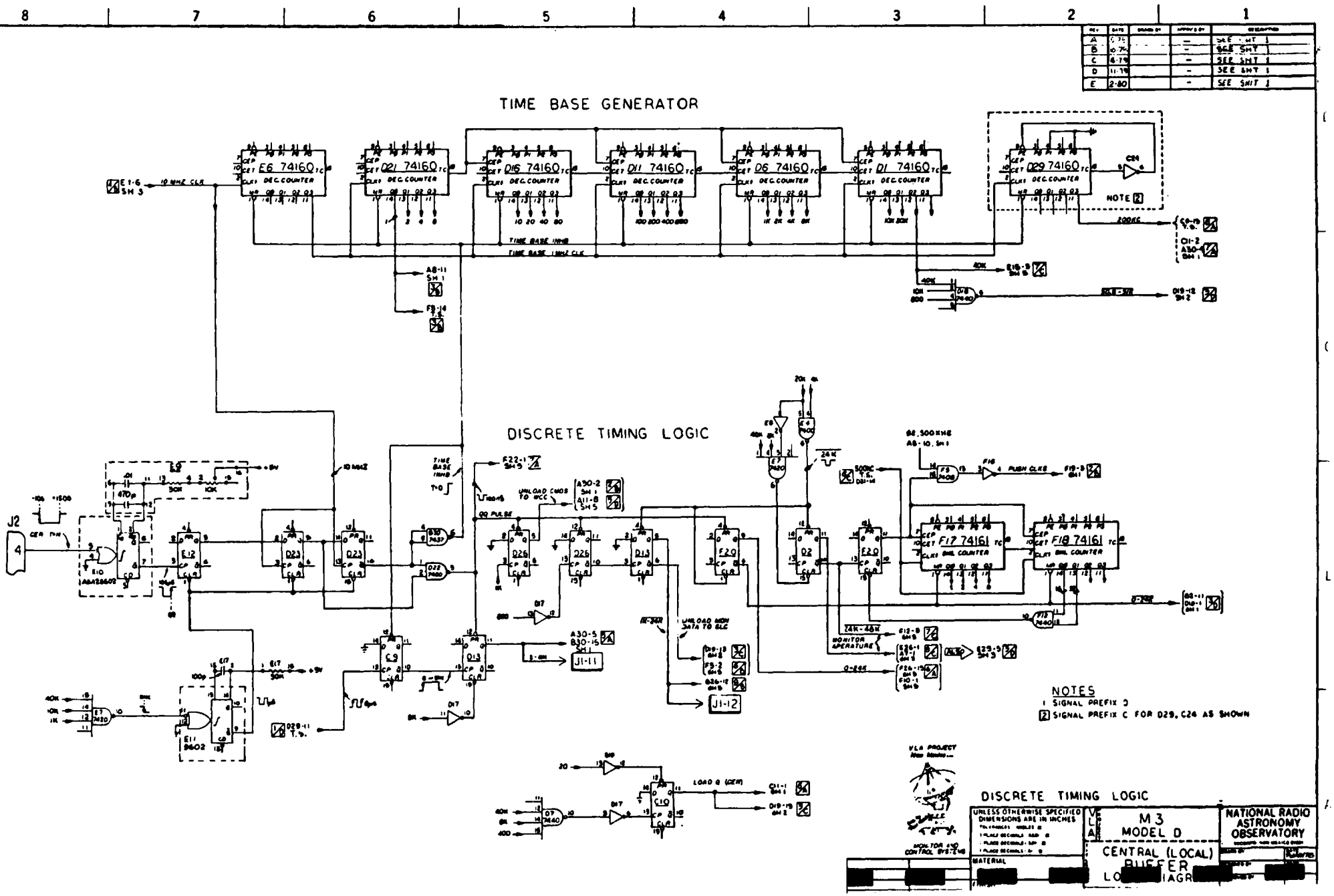
CENTRAL D.S. DATA LOAD CONTROL

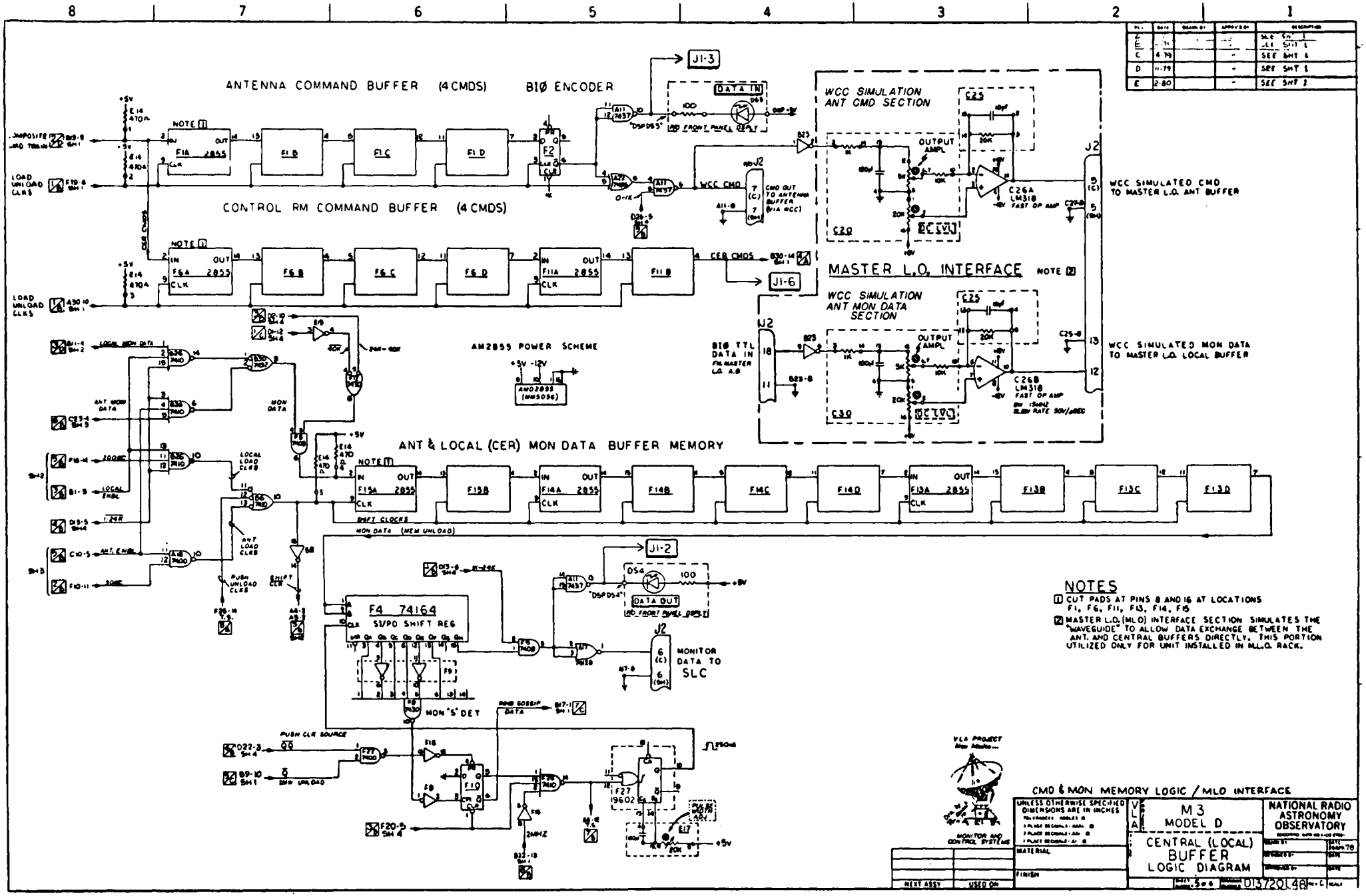
M3 MODEL D

CENTRAL (LOCAL) BUFFER LOGIC DIAGRAM

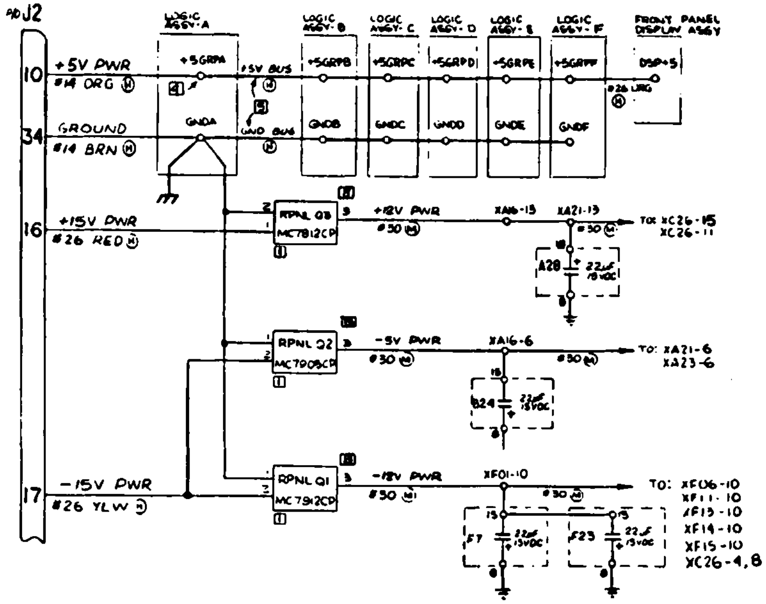
NATIONAL RADIO ASTRONOMY OBSERVATORY


BI-Ø INPUT DEGLITCHER
TRANSITION DETECTOR
BI-Ø TO NRZ INTEGRATOR
MONITOR "S" DETECT
MON DATA SHIFT CLOCK ENBL GENERATOR
ANT MON "S" DETECTOR
E2 5-10 MHZ DOUBLER
BI-Ø TO NRZ INTEGRATING DET.
M3 MODEL D
CENTRAL (LOCAL) BUFFER LOGIC DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY


TIME BASE GENERATOR
DISCRETE TIMING LOGIC
NOTES
1 SIGNAL PREFIX D
2 SIGNAL PREFIX C FOR D29, C24 AS SHOWN
DISCRETE TIMING LOGIC
M3
MODEL D
CENTRAL (LOCAL) BUFFER
NATIONAL RADIO ASTRONOMY OBSERVATORY


ANTENNA COMMAND BUFFER (4 CMDS)
BIØ ENCODER
CONTROL RM COMMAND BUFFER (4 CMDS)
WCC SIMULATION ANT CMD SECTION
WCC SIMULATED CMD TO MASTER L.O. ANT BUFFER
MASTER L.O. INTERFACE
NOTE 2
WCC SIMULATION ANT MON DATA SECTION
WCC SIMULATED MON DATA TO MASTER L.O. LOCAL BUFFER
AM2855 POWER SCHEME
ANT & LOCAL (CER) MON DATA BUFFER MEMORY
F4 74164
SI/PO SHIFT REG
MONITOR DATA TO SLC
MON 'S' DET
NOTES
1 CUT PADS AT PINS 8 AND 16 AT LOCATIONS F1, F6, F11, F13, F14, F15
2 MASTER L.O. (MLO) INTERFACE SECTION SIMULATES THE "WAVEGUIDE" TO ALLOW DATA EXCHANGE BETWEEN THE ANT. AND CENTRAL BUFFERS DIRECTLY. THIS PORTION UTILIZED ONLY FOR UNIT INSTALLED IN M.L.O. RACK.
CMD & MON MEMORY LOGIC / MLO INTERFACE
M 3
MODEL D
CENTRAL (LOCAL) BUFFER LOGIC DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY
VLA PROJECT
MONITOR AND CONTROL SYSTEMS
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL
FINISH
NEXT ASSY
USED ON
D1372048

REV	DATE	DRAWN BY	APPROVED	DESCRIPTION
A	5-??		-	SEE SHT 1
B	10-??		-	SEE SHT 1
C	4-79		-	SEE SHT 1
D	4-79		-	SEE SHT 1
E	?-80		-	SEE SHT 1



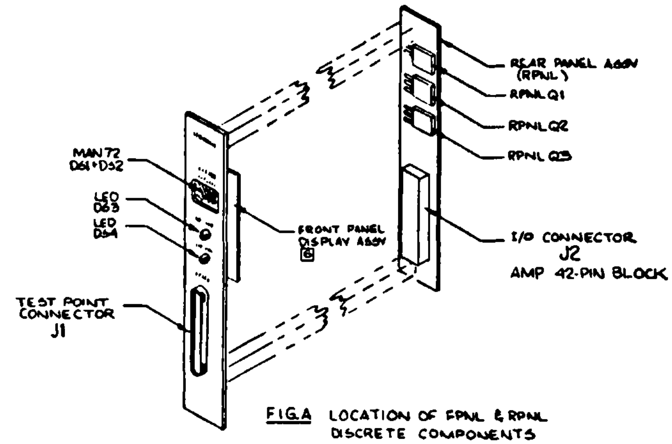


FIG.A LOCATION OF FPNL & RPNL DISCRETE COMPONENTS

J1	TEST POINT CONN	
1		
2	MON DATA NRZ OUT	5
3	ANT CMDS NRZ OUT	5
4	INPUT [illegible] (TTL)	3
5		
6	DSS CMDS NRZ OUT	5
7		
8	DSS MON SHFT ENBL	2
9	DSS MON DTA INP	2
10		
11	Ø TO BK	4
12	[illegible] TO [illegible]	4
13	[illegible] TTL CLK	1,3
14	DSS NRZ CMDS OUT	1
15		
16	DSS CMD PUSH CLK	1
17	Q-DET. V	1
18		
19	S-DET. V	1
20	CMD PUSH CLK ENBL	1
21		
22		
23		
24		
25		
26		
27		
28		
29		
30		
31		
32		
33		
34		
35		
36		
37		

J2	I/O CONN	
1	AC0	2
2	AC1	2
3		
4	TRACK/HOLD	4
5	MLO AB CMD	5
6	DTA TO SLC	5
7	BY-Ø OUT	5
8	[illegible] TO-RT	3
9	DSS -HI	3
10	+5V PWR	
11	SET PWR-B	3
12	MLO BCD MON	3
13	SET PWR-2	3
14	DATA TAP-HI	1
15	[illegible] -LO	1
16	+15V PWR	
17	-15V PWR	
18	MLO BCD IN	3
19		
20		
21		
22	DSS UP-HI	2
23	-RET	2
24	CMDS TO DSS	1
25	SET PWR 2V	1
26		
27		
28	AC2	2
29	AC3	2
30		
31		
32		
33		
34	PWR GND	
35	AC4	2
36		
37		
38	SMPZ INP	3
39	[illegible] SIG	1
40	BY-Ø INPUT	3
41		
42		
43		
44		
45		
46		
47		
48		
49		
50		

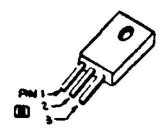


FIG. B IDENTIFICATION OF RPNL Q1..Q2..Q3 PIN TERMINALS

NOTES:

1. VOLT. REGULATORS RPNLQ1, RPNLQ2 AND RPNLQ3 ARE MOUNTED ON REAR PANEL. REFER FIG A.
2. (H) INDICATES HAND WIRING
   (M) INDICATES MACHINE WIRING.
3. CENTRAL BUFFER WIRE LIST REFER TO A13720W14
4. NOTATIONS "+5GRPA", "GNDA", ETC., REFER TO LOGIC BOARD ASSY TERMINALS
5. THE "+PWR" AND "GROUND" BUS LEADS ARE TO BE ROUTED AND SLEEVED PER NRAO DWG D13720P10
6. FRONT PANEL DISPLAY ASSY (A1) NRAO DWG C13720P39
7. +5V PWR IS FILTERED AT THE FOLLOWING LOCATIONS WITH THE INDICATED DIP HEADER ASSY:
   - B13720P14 - B3, C28, D3, E28, F3
   - B13720P16 - A3, B28, C3, D28 E5, F24
   - B13720P20 - A28
   - A13720P71 - B24, F28
8. THE REGULATOR PIN OUT SHOWN IS FOR MOTOROLA 7800 & 7900 SERIES REGULATORS. WHEN NON-MOTOROLA REGULATORS ARE USED ADJUST WIRING TO CONFORM TO THE PIN OUT OF THESE OTHER DEVICES

POWER WIRING/J1 & J2 DETAILS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL

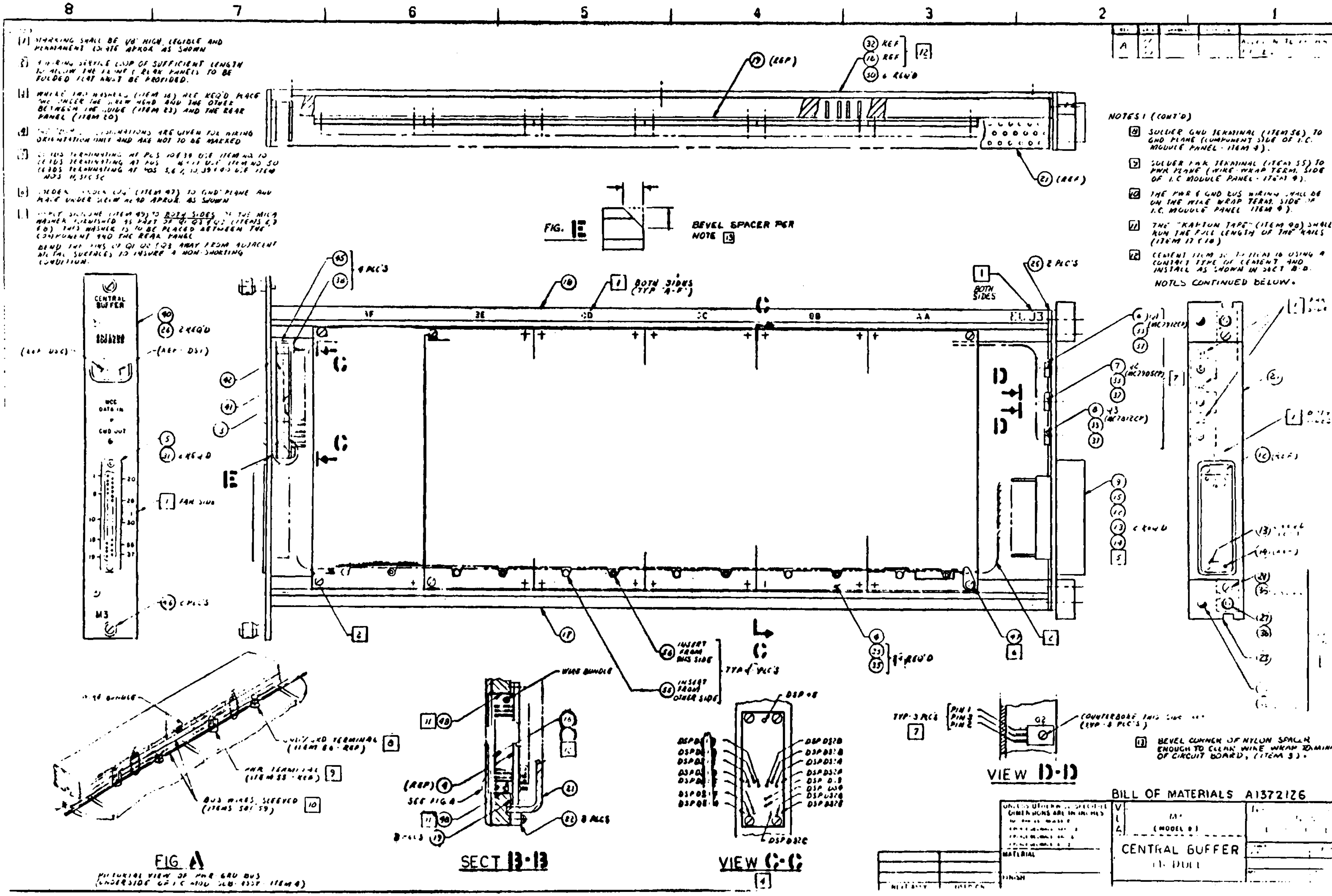
VLA M 3 MODEL D

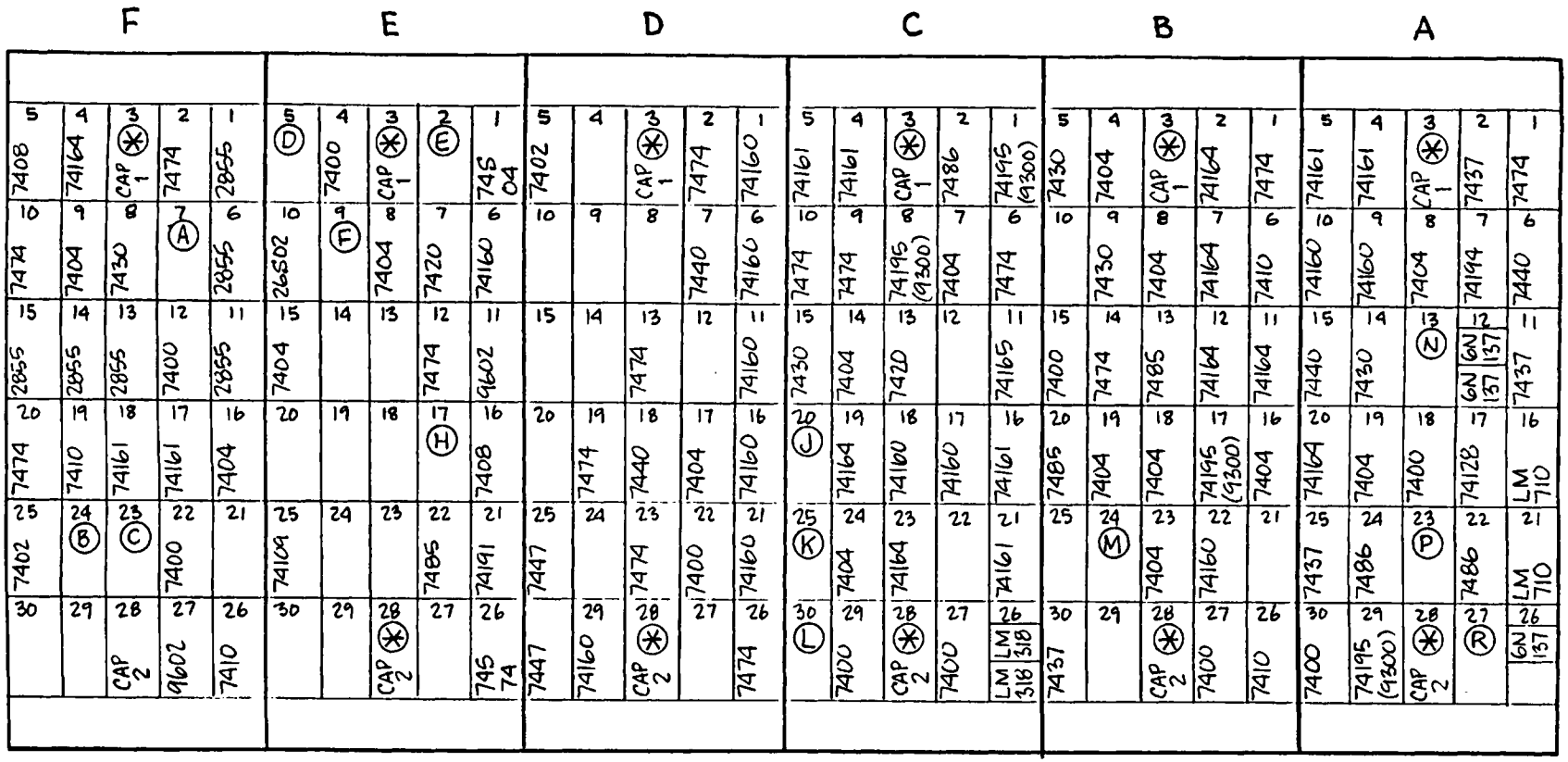
CENTRAL (LOCAL) BUFFER LOG[redacted]AGR[redacted]

NATIONAL RADIO ASTRONOMY OBSERVATORY

[redacted] NEXT ASSY [redacted] ON [redacted]

B13720148

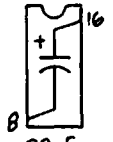

NOTES: (CONT'D)
NOTES CONTINUED BELOW.
FIG. E
BEVEL SPACER PER NOTE 13
BOTH SIDES
CENTRAL BUFFER
M3
WIRE BUNDLE
INSERT FROM BUS SIDE
INSERT FROM OTHER SIDE
BEVEL CORNER OF NYLON SPACER ENOUGH TO CLEAR WIRE WRAP TERMINAL OF CIRCUIT BOARD, (ITEM 3).
FIG A
SECT B-B
VIEW C-C
VIEW D-D
BILL OF MATERIALS A1372126
CENTRAL BUFFER
MATERIAL
FINISH



DIP HEADER ASSY's:

REF. SYM.	B.O.M.	ASSY DWG.	REF.	BOM
Ⓐ	A13721Z14	C13720P81	Ⓚ	A13721Z12
Ⓑ	A13720Z29	C13720P81	Ⓛ	A13721Z13
Ⓒ	↓ Z96	↓	Ⓜ	A13720Z96
Ⓓ	Z9		Ⓩ	Z43
Ⓔ	Z39		Ⓟ	↓ Z36
Ⓕ	Z91		Ⓡ	Z98
Ⓗ	↓ Z92		◯	
Ⓙ	A13721Z13	↓	◯	

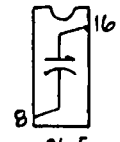
CAP-1



22μF

BOM:
A13720Z9

CAP-2



.01μF

BOM:
A13720Z28

A13720P81 - CENTRAL BUFFER
I.C. MODULE PANEL

CENTRAL BUFFER
I.C. LOGIC ASSY & DETAILS