VLA Technical Report No. 61
The System Buffer, Module type M14
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List of Illustrations and Major Drawings

1.0 INTRODUCTION

This manual describes the operation of the Model A System Buffer (SB), module type M14, and was written to serve as a trouble-shooting and maintainance guide for this component of the VLA Monitor and Control (M&C) System.

The System Buffer is used in central control/monitor applications in which the Local Oscillator (LO) and Modem/Waveguide (WG) transmission systems are not used for message transmission. This situation is the case for the Master LO System, the Weather Station, the Waveguide pressure monitors, the Fluke Synthesizer Control units (L16) and The Hydrogen Maser monitor. Similar applications will no doubt continue to arise from time to time and will be controlled by System Buffers.

To put the operation of the SB into the system context, the reader is referred to the manual: "An Overview of the Monitor and Control System", VLA Technical Report No 44. "The Handyman's Guide to the Data Set", VLA Technical Report No 30 provides a detailed description of the SB/Data Set interactions. Figure 1 depicts the relationship of the SB to the balance of the M&C System. Figures 2 and 3 depict the Monitor and Control system timing relatioships. Figure 4 depicts the message formats.

Like the Antenna Buffer (AB) and Central Buffer (CB), the function of the System Buffer is command-monitor data message handling but message interchanges only occur between the System Buffer, Data Sets and the Serial Line Controller (SLC). To the SLC the System Buffer appears to be another Central Buffer; to the Data Sets the System Buffer appears to be another Antenna Buffer. Because the System Buffer operations are identical to many of the AB and CB functions, much of the System Buffer logic is a hybrid combination of logic abstracted from these corresponding functions in the AB and CB.

The use of the LO/WG Transmission system for message transmission between the central electronics and the antennas imposes signal spectrum constraints on the Central and Antenna Buffer message signal outputs. To meet these constraints, BI-0 modulation of the command and monitor data message signals are used to eliminate spectrum components below 500 Khz. The BI-0 modulators and demodulators add to the complexity of these buffers. In contrast, the System Buffer does not require BI-0 modulators and demodulators; the messages inter-changed between the System Buffer, the SLC and Data Sets all use the NRZ message format; there are no analog elements in the signal paths and the paths are not perturbed by IF noise as is the case in the Central-Antenna Buffer paths. These simplifying factors considerably reduce the amount of logic circuitry in the Buffer.

The emphasis of this manual is on detailed functional operations; the writer's intent is to provide a thorough description of the System Buffer's theory of operation. Straight-forward portions of the logic are treated briefly; more complex areas (and there are several) are fully explained and the explanations are augmented by timing diagrams. Using this manual as a reference, a digital maintainance technician should be able to quickly identify and repair malfunctions.

The logic descriptions are based upon two contrasting perspectives: 1) operations as a function of time (which is the driving parameter in the VLA Electronics); 2) command and monitor data message transmission operations, - the primary functions performed by this module.

2.0 SYSTEM BUFFER DESCRIPTION

The function performed by the System Buffer is command/data message distribution; the SB detects bit-serial digital command messages from the Serial Line Controller (SLC) for storage and subsequent distribution to 6 Data Sets, polls the Data Sets for monitor data messages and then transmits these monitor data messages to the SLC in response to polling requests from the SLC. Figures 5 and 6 depict the SB logic flow and logic block diagram.

Like the Antenna Buffer, the System Buffer deals with several (6) Data Sets, and like the Central Buffer it must perform concurrent command/monitor data operations and must deal with many high speed message flow interactions with the Serial Line Controller. The sixth Data Set (DS #5) is polled separately for monitor data so that the data presented to the control computer is ordered in a manner identical to the Antenna - Central Buffer combination. Because there are no LO/WG transmission system interactions, the mid-portion of the 52,083 period has some slack time.

Like the Central-Antenna Buffer combination, command messages extracted from the control computers in VLA machine cycle n are delivered to the controlled devices in cycle n+1. The response of the controlled device to the command may be monitored in cycle in n+1 but it is input to the control computers in cycle n+2; therefore the earliest possible monitored response to a command is input to the computers two VLA machine cycles after the computer output the command to the M&C System.

The SB must be able to detect, store and output up to eight command messages to it's associated Data Sets and poll, detect and store twelve monitor data messages from Data Sets 0 - 5 and must output these messages when polled by the SLC.

The SB is packaged in a standard VLA 1-W module and contains wire-wrap logic connector boards for the digital logic. A front

panel numeric LED shows the DCS address and flashing descrete LEDs indicate command and monitor data message flow. A front panel test point connector permits observation of logic signals for diagnostic purposes. DC power regulators on the rear panel provide special voltages required by some of the logic chips. The System Buffer package is depicted on the Top Assembly Drawing and Exploded View (Fig 7) in the back of this manual.

2.1 MESSAGE FORMAT DESCRIPTION

Figure 4 depicts the format of the Command and Monitor Data messages and the "Q" (for Query) character format. The NRZ format messages are prefixed by an "S" (for start) character which signals that a message immediately follows. The bit rate of the S character is twice the bit rate of the data bits to make this character unique. The message consists of five 8-bit data bytes; the first byte contains a 5 bit DCS Address (which can range from 0 to 31) and a 3-Bit Data Set Address which can range from 0 to 7. The second byte is the Multiplex Address which designates a particular command or data channel. The third, fourth and fifth bytes are components of a 24 bit command or monitor data argument. In the case of an analog data message, the 24 bit argument consists of two 12 bit values resulting from the conversion of two analog signals by the Data Set analog-to-digital converter. In all address and argument values, the first bit (in time) is the most significant bit.

The "Q" character is used by the SB to poll data from Data Sets via the buffer's Data Set Command Ports. The SLC uses the "Q" character to poll data from the System Buffers via the SLC's Command/Q Ports. The bit rate of the Q character is the same as the bit rate of the S characters in the same message environment.

The bit rates of the messages and Q characters are discussed below.

2.2 SYSTEM BUFFER I/O SIGNALS

- QQ pulse, - a 400 nano second differential TTL level signal from the L8 Distribution System which signals the start of the VLA timing cycle.

- 5 Mhz clock input, - a 2 volt P-P (nominal) sine wave clock generated by the L8 Distribution System to clock the SB and Data Set logic.

- 5 Mhz clock output, - a TTL level, AC-coupled digital clock which drives the Data Set's clock inputs.

- SLC Command Signal Input - an optically isolated (in the SB), low-true, TTL level, command message input from the SLC. Bit rates are 500 ns/bit and 1 usec/bit for the S and Q characters

and message bits respectively.

- SLC Monitor Data Output - a TTL level, low-true, monitor data message output to the SLC. Bit rates are 500 ns/bit and 1 usec/bit for the S character and message bits respectively.
- Data Set Command Ports - six, TTL level, low-true line driver outputs which drive the command inputs of the associated Data Sets. The S and Q characters and message bit rates are 5 and 10 usec/bit respectively.

- Data Set Monitor Data Ports - six optically isolated (in the SB), input ports which receive low-true, TTL level, monitor data inputs from Data Set 0 - 5. Bit rates are 5 and 10 usec/bit for the S character and message bits respectively.

- Data Tap Port - a TTL level, low-true output to the Data Tap. The outputs to the Data Tap are both command and monitor data messages at the SLC/SB message bit rates.

- DCS Address Lines - five high true TTL level lines which are grounded on the back of the bin to define the DCS address of the SB.

2.3 TIME-DRIVEN SYSTEM BUFFER OPERATIONS

The operations performed by the System Buffer are time-directed in that functions are enabled, initiated and terminated by control discretes derived from the internal time base; these discretes regulate the message flow between the SB, the Data Sets and SLC. Figures 2 and 3 depicts the time-ordered operations performed by the Antenna and Central Buffers. The System Buffer emulates the message transmission operations of the Central and Antenna Buffers but there are small time differences between the System and Antenna Buffer Data Set Polling; these differences are unimportant, the timing diagrams illustrate the essence of the SB operation. Figure 5 depicts the System Buffer operations in flow diagram form. Figure 6 depicts the System Buffer Block Diagram.

The SB time base is referenced to the QQ pulse from the L8 Distribution System and timing terms are stated in terms of microseconds of elapsed time from the QQ pulse. The SB time base is triggered into operation by the QQ pulse and is clocked by the 5 Mhz clock from the L8 Distribution System. If the QQ pulse is missing the SB will remain in the quiescent state. A 10 Mhz clock is generated by doubling the 5 Mhz clock.

A 1000 - 16,000 usec enable causes the serial command memory contents to be unloaded to the Data Set Command Ports. The command bit rate is 5 usec/bit and 10 usec/bit for the message and S character bits respectively. Each Data Sets analyzes the message stream to determine if it is the target of a command

message; if it is, it executes the command. See the Data Set manual for a description of this process.

A 1000 - 24,000 usec enable permits the System Buffer to be polled by the Serial Line Controller for the monitor data messages stored in the SB's serial monitor data memory. The Serial Line Controller directs a Q character to each SB (or CB) in the sequence DCS-#0, DCS-#1.... DCS-#37 (octal, for a total of 32 CB/SB's). This sequence is repeated 11 times.

When the polled monitor data message is detected by the SLC, it is immediately rebroadcast to all CB's and SB's via the SLC's Central Buffer Command Ports during the monitor data memory loading sequence. This rebroadcast data is tapped off the SB's Command Input Port and fed to the Data Tap in the bin so that the Data Tap is able to hear all rebroadcast monitor data and command messages. This rebroadcast Monitor Data is sometimes referred to as "gossip data". There are 384 monitor data words (32 buffers x 12 words/ant) polled from the CB's and SB's during this period. The polling period is tight: 59 usec which is about 1 usec longer than required for the CB and SBs to detect the Q, output the monitor data message to the SLC, and enable the SLC to detect and temporarily store the message.

A 24,000 - 33,000 enable causes the SB to poll Data Sets 0 - 4 for monitor data messages. When a monitor data message from a Data Set is detected a loading sequence is initiated which causes the data message to be stored in the serial monitor data memory. After a 50 usec delay to detect the Q character, the Data Set begins a data acquisition sequence. 250 usec after the output of the Q, the Data Set begins to emit a monitor data message to the SB's Data Set Monitor Data Port. This port is optically isolated (in the SB) to eliminate ground noise effects. The monitor data loading sequence loads an additional 8 spacing bits between monitor data messages. The 200 usec delay between the start of the "Q" and the begining of the monitor data message is used by the Data Set for sampling and A/D conversion. The Data Set monitor data message duration is 500 usec so there is a 150 usec margin in the 900 usec period.

A 24,000 - 48,000 usec enable permits the System Buffer to listen for command messages from the Serial Line Contoller. The command messages may be in any order and may be directed to any of the six Data Sets controlled by the System Buffer. The command memories in the system Buffer can store up to 8 command messages in any VLA cycle. The SLC can extract, format and output up to 128 commands from either (or any combination of) two computers during this period. There are no requirements for dummy command messages (ie. messages to non-existent devices) to fill the command memories.

At 48,400 and 49,400 the SB polls data from Data Set #5 by emitting Q characters on the Data Set #5 Command Port. The Data Set #5 monitor data is gathered after the Data Set 0 - 4 monitor data messages have been stored so that the memory contents are in the order: MW1 - DS0 ... DS4; MW2 - DS0 ... DS4; MW1 - DS5; MW2 - DS5. This is the order that they are read out to the control computers by the SLC. Figure 3 depicts the Data Set #5 polling timing.

At t = 51,000; the SB time base is shut down and remains in this quiescent state until stimulated back into operation by the QQ signal. By design there are no provisions for flywheeling of the time base in the System Buffer; the flywheeling function is performed by L8.

3.0 DETAILED CIRCUIT DESCRIPTION

3.1 TIME BASE

The time base logic (Sheets 1 and 2) generates a series of time-based control discrete terms which regulate all functions of the System Buffer. The time base is quiescent until triggered into operation by the QQ pulse from the L8 distribution system.

The fall of differential receiver B2506 output sets the time base control flip-flop B2005; this lifts the preset enables on the time base synchronous counters B26, B21, B16, B11, B6 and B1 so that they are able to count from the preset count of 0. All time discrete terms are derived from decodes of these counters.

Gates B0206 and B0713 combine a decode of 51,000 usec and the 5 Mhz clock to generate a gated C reset which triggers one-shot B3007 to reset the time base control flip-flop B2005. This re-applies the low-true time base counter preset enable to the time base counter which causes it to continuously load zeros. Thus the time base (and hence the SB) is quiescent and remains in this state until stimulated on again by the next QQ pulse.

The time base clock is a 2 Volt P-P, 5 Mhz sine wave clock from the L8 Distribution System. The 5 Mhz clock is detected by analog comparator A0413 (on Sheet 3) which senses the 5 Mhz axis crossing. The TTL-compatible output of A0413 drives the A5 harmonic doubler circuit which rings at 10 Mhz. The 5 Mhz drive to the doubler is differentiated by the 10 pf, 1K ohm, (A5) RC circuit so that the MPS 918 transistor has a narrow collector current pulse. The tank is tuned to 10 Mhz and the AC coupled output drives the Schottky 74S04 B2302 which is caused to operate in a linear region by the 2K ohm resistor on the doubler's output. Inverter B2302 and B2304 square the 10 Mhz clock signal which drives the time base and clocks the message edge detection shift registers. Inverter B23 must be a 74S04; the high

switching speed of the Schottky logic is important to the doubler circuit's operation.

The System Buffer provides a 5 Mhz clock output for the Data Sets; flip-flop C17 toggles to produce a 5 Mhz clock which is output via buffer A2606. The 5 Mhz Data Set clock is AC coupled via B29 7/10.

The reason that 10 Mhz is used as a clock in the System Buffer is that it provides a 100 ns resolution for synchronization to the 2 Mhz bit rate incoming message streams from the SLC. The sampling clock must be an integer multiple of the bit rate of the incoming message stream.

A series of time discretes are derived from the time base to control the CB operations. These are:

Enable 0 - 24,000 is generated by flip-flop A2511 which is direct set by the QQ pulse and direct reset by gate B0710 which goes true at t = 24,000 usec. This enable initializes the monitor data output logic for polling by the SLC.

Enable 1000 - 24,000 is generated by flip-flop B0405 which is clocked true by the 1k term of counter B6. B0405 is direct reset by gate B0710 which goes true at t = 24,000. This enable permits the SLC to poll the SB.

Enable 1000 - 16,000 is generated by flip-flop B1505 (Sheet 1) which is set by flip-flop B2010 which is clocked true by the 1k term from the time base counter. Flip-flop B1505 is direct reset by the 16k term from the time base counter. This enable causes the command messages to be pushed out of the serial command memory.

Enable 24,000 - 48,000 is generated by flip flop B1311 which is direct set by gate B0710 which goes true at 24,000 usec. Gate B0706 goes true at t = 48,000 usec to direct reset B1311. This 24,000 - 48,000 term enables the SB to listen for command messages from the SLC.

Enable 48,000 - 51,000 is generated by flip-flop B1305 which is direct set by gate B0706 which goes true at t = 48,000. B1305 is direct reset at t = 51,000 by the counter reset term described above. This enable permits Data Set #5 to be polled for monitor data.

Enables 48,400 and 49,400 are generated by flip-flop B0811 which is clocked low by gate B1203 which combines the 48,000 decode and the 400 term from time base counter B11. The duration of the enable is 20 usec and is determined by the 20 term from counter B16 which direct sets B0811 to raise the low-true enable. The flip-flop is held direct set during the

50,000 period by gate B1206 which is an or input to gate B0512. B1206 includes the counter 2000 term; this holds the output of B0811 high so that it cannot be clocked by the 400 term rising edge during the 50,000 period. These two enables generate Q characters for Data Set #5.

When synchronizing an osciloscope to the SB time base or QQ pulse, you may observe a puzzling 10 usec jitter in the period. This is an artifact of the L8 Timing Generator which goes through a 3-state periodic variation of the 19.2 Hz period. The L8 logic implementation causes the 3 periods to vary in a sequence which is base, base + 200 ns, base +10 usec.

3.2 COMMAND SIGNAL DETECTION, STORAGE AND OUTPUT

This is the first major function performed by the System Buffer; all of the non-antenna associated commands are handled by the SB.

COMMAND DETECTION, STORAGE AND OUTPUT -- All command messages originate in the SLC which extracts them from either of two control computers, formats them into serial messages and broadcasts them to the Central and System Buffers at a 2 Mhz S character and a 1 Mhz message bit rate. If the commands are all derived from one computer, the command message intervals are 160 usec; if two computers are involved the interval between messages is either 80 or 160 usec depending upon the settings of the various selector switches on the front of the SLC, see the Overview of the Monitor and Control System manual for details.

It is the task of System Buffer to listen to all the incoming command messages and to compare the DCS address with the hard-wired (in the bin) address. If the compared addresses agree, the SB is the target of a command message and the SB must then store these command messages in the serial command memory and outputs them during the 1000 - 16,000 period of the next VLA machine cycle.

There is no ordering of command messages to the CBs and SBs as there is in the monitor data polling; any SB/CB could receive a continuous stream of command messages at 80 usec intervals and must be able to store them in the command memories. Obviously the command memories would quickly fill up and overflow if the command stream in a given cycle exceeded the memory capacity of 8 command messages. In practice the control programs in the ModComp computers formulate commands in an orderly schedule so that there are never more than 4 commands (4 is a very rare occurance, the average is about 1.5) per VLA machine cycle.

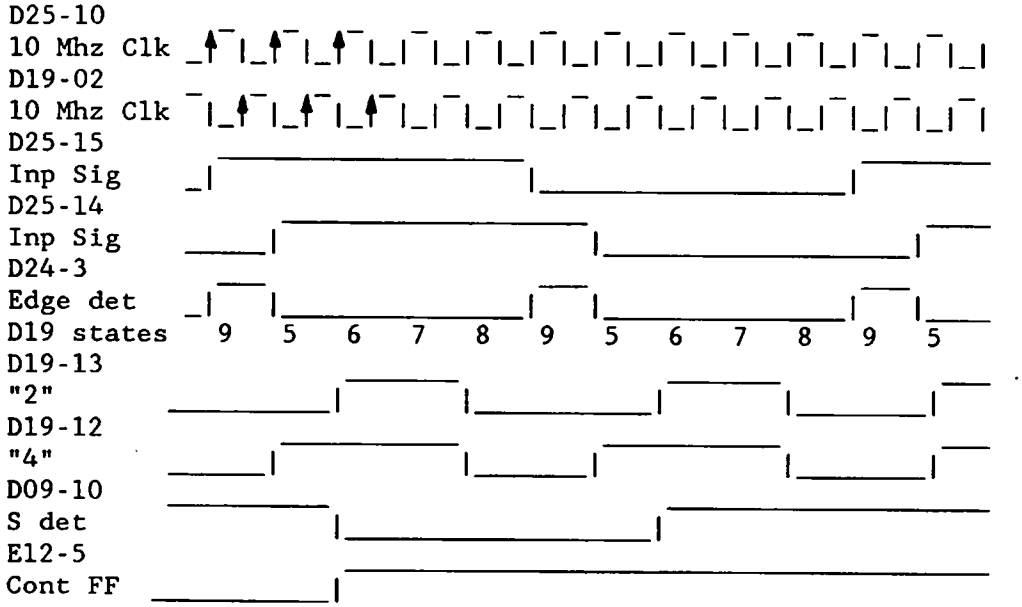
SLC commands are input in low-true form at the SLC Command Signal Input port, J2-39 (Sheet 1) where they drive an optical

isolator to eliminate ground noise effects. The output of the isolator drives a power buffer, A2610 which drives the Data Tap Port, J2-8/9.

The high-true command message is sampled by shift register D25 which is clocked by 10 Mhz. Exclusive or D2403 generates a 100 ns output when signal edges shift through the register. These edges preset counter D19 to a count of 5 through or gate D2001. D19 sequences through the states 5,6,8,9,5,6 etc because of the TC feedback to D2003. The "4" stage of D19 clocks the data stream from D25 into flip-flop D1111 and shift registers D15, D10 and D5 which have decode logic to test for Q and S characters and to compare the DCS addresses. The Q detect gate D1810 activates the monitor data output logic (discussed below); the S detect gate D0910 strobes the magnitude comparator E0606 to test the message DCS address against the address hardwired on the bin. Exclusive or D2406 provides the fifth bit of comparison for the four bit magnitude comparator. Both S and Q detect gate outputs are 500 ns wide.

The operation of this logic is depicted in the simplified timing diagram below.

COMMAND MESSAGE INPUT PHASING



The "Inhibit Gossip Data" term on shift register B17 holds this register reset when the SB is outputting a monitor data message to the SLC. The monitor data 2 Mhz output shift clock is taken off counter D1913; the inhibit holds the phase of the 2 Mhz clock generated by counter D19 constant during the period of output of a monitor data message to the SLC. The reasons for the inhibit are discussed in the monitor data section of this manual.

If the command message DCS address-bin comparison is true, the message is addressed to the SB that we are discussing and a message loading sequence is initiated. The comparator strobe sets load control flip-flop E1205. flip-flop E1205 generates a load enable to permit the 2 Mhz clocks from gate E1603 to load the command message into the serial command memories on Sheet 8. The counter is preset to a count of 151 and at the count of 256 (1 count after 255, the all 1's state), the 128 counter term is anded with the 2 Mhz clock in gate E1106. The trailing edge (rise) of E0711 clocks control flip-flop E1205 reset. E1205's output is the load enable on the memory clock gate E1110. The message stream is tapped off flip-flop E1211 which is an extension of the D15, D10, D5 shift register. Shift register D5 and E1211 are enabled by a 24,000 - 48,000 enable which holds them in the clear state except during the period that the SB should receive commands. The inhibit prevents the S detector from responding to the rebroadcast monitor data messages from the SB's and CB's which would cause them to be loaded into the command memories. The large width of the message decode register is a vestige of the CB logic design and does not have to be this wide but it was decided to retain this feature of the CB for commonality of the circuitry See the CB manual for a discussion of this register length.

COMMAND UNLOAD TO DATA SETS -- Having loaded the command memory we shall now consider the unload logic. The unload process is a simple enable of unload clocks to the command memory.

Pull up resistors E21-1,2,3,4 are required because the AM2855PC command memory registers require a signal swing slightly greater (ie. > 4 volts) than that normally available from a TTL gate. These memory chips shift on the fall of the clock rather than the rise like the other shift registers in the AB.

Command Memory E17 and E22 are quad, 128 bit bit MOS shift registers with TTL-compatible clock, inputs and outputs. . When quiescent, the clock must be held in the low state. See the Data Sheet section for the specifics on the AM 2855PC chip.

The commands are unloaded by 200 Khz clocks which are enabled by the 1000 - 16,000 usec enable on gate E1113 (Sheet 6) via or gate E1603 to the Data Set Command Ports: J2 - 30, 12, 20, 24, 14 (Sheet 1), and 32 (Sheet 6).

The operation of this unload logic is so simple that it is not pictured by a timing diagram.

3.3 MONITOR DATA GATHERING, STORAGE AND OUTPUT

This is the second major function performed by the System Buffer; all of the VLA non-antenna-associated central monitor

data messages are handled by SB's.

DATA SET 0 - 4 POLLING LOGIC -- Enable 24,000 - 34,000 permits the monitor data control counters, (Sheet 1) A19 and A9 to poll the Data Sets for monitor data messages. Counter A19 generates the 900 usec polling period and has a 10 Khz Cet input from counter B1615 so that it counts at a 10 Khz rate. Gate A1810 goes true at the count of 9 and immediately presets the counter to 0 so that the period is 900 usec. The A18 trailing edge clocks counter A9 which generates a 3 bit Port Address to select Data Set Ports for output of the "Q" polling character and to listen for the monitor data message evoked from the Data Set in response to the Q. A9 has a radix of 5; it is initialized to 0 by the 24,000 - 33,000 enable and is reset to 0 at the leading edge of state 4.

The Q character is immediately emitted by shift registers A20 and A1505 when the 24,000 - 33,000 enable rises and at the beginning of each 900 usec polling period; gate A1813 or's the enable and counter A19 resets to load the Q character into the shift registers. Flip-flop A1510 generates a one clock pulse duration hold-off inhibit on gate A2910 so that the leading edge of the Q is a distinct rise to a 1 state. The Q's are distributed to the Data Set Command Port or gates by A14, a data selector (decoder) under control of the port address terms from counter A9.

The Q character shift clocks are generated by counter A24 which has a radix of 5 and has Cet and Cep inputs from counter B26 which is the 1 Mhz to 100 Khz divider in the time base.

You will note that DS-0 command and monitor data ports have a high-true signal polarity; this is a vestige of the earlier use of an Antenna Buffer to drive the Central Weather Station Data Set, (DS-0). This was made to be high-true to retain compatibiliy with the circuitry in the Weather Station.

DATA SET 0 - 5 MONITOR DATA INPUT LOGIC --- The Data Set Monitor Data Ports consist of 5 optical isolators (to eliminate common-mode noise effects) and digital multiplexer A1315 driven by the port address terms from counter A9. This simple logic is shown on Sheet 5. The multiplexer output is inhibited until enabled by the 24,000 - 33,000 enable.

The output of the multiplexer A1315 is the monitor data message stream evoked from the selected Data Set by the Q character. The receiving logic on Sheet 3 must detect and synchronize to the message stream. The monitor data stream is sampled at a 5 Mhz rate (the message bit rate is 200 Khz) in register C26. Exclusive or C2403 senses the data edges of the incoming message stream in register C26 and phase adjusts the time base counter C23 and C18 The counter divides by 25 to

produce the 200 Khz shift clock which is phased 10 counts from the edge of the input data bits. The operation of this phase adjusted time base is similar to the phase-adjusted clocks described above; the simplified timing is depicted below.

DS 0 - 4 MONITOR DATA PHASE ADJUSTED TIME BASE TIMING

The rise of C2406 also sets flip-flop B1511 (Sheet 1), the Data Set Heard From enable (DSHF) which permits the Data Set data to be clocked out to the Data Set Command Port or-gates as Gossip Data.

As the monitor data message propagates through the SAA Inject & Parity Logic on Sheet 3, the hard-wired (on the bin) DCS address (from Sheet 1), the Data Set Address and the parity bit for the byte must be injected into the message stream. This operation is performed by the tricky setup of the shift registers C21 C16, C11 and C6. We will defer the description of this logic till later in the discussion.

This SAA Inject & Parity Logic shift register is clocked at 200 Khz by the phase adjusted clock counter C23 and C18. As edges are detected by C2403 the counter is preset to a count of 1; at the count of 25 the counter is again preset to 1; in the event that the exclusive or C2403 senses another edge before the 37 count reset, the counter will again be reset to 1 count. The rise of C1214 (at a count of 10) is the phase adjusted 200 Khz shift clock which shifts the monitor data through the SAA etc register. The 10 count phasing (in C23 & C18) is the approximate mid-point of the monitor data message data bits.

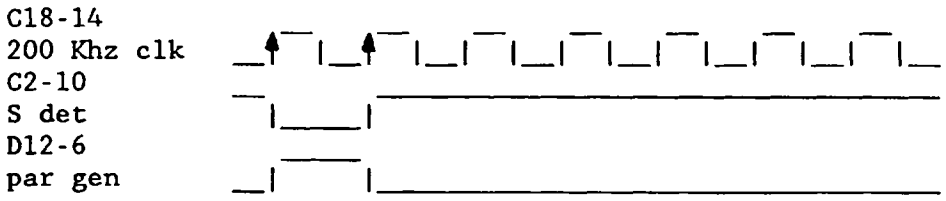
When the S character message prefix reaches the C6 and C1 shift register, it is detected by and-gate C0210 which goes low-true for 5 usec; this does two things: 1) the SAA Inject & Parity shift registers are caused to parallel load the DCS, DSA (ie the Data Set port address from A9) and the parity bit states appearing at the register's parallel inputs. 2) the Monitor Data Load Counter is set into operation to load the Monitor Data Register with the incoming message.

Let's first consider the SAA inject logic: Parity generator

C1206 forms odd parity over these 8 address bits and the odd parity output is applied to register C21 pins 4,5. The next two 200 Khz clocks cause the parity bit and the two addresses to be loaded into C21, C16, C11 and C6. The odd-looking feed-forward of the Q's of C21, C16 and C6 into the next stage preset inputs deserves some attention. The parallel load of the DCS/DSA and parity bit into these registers results from the clock rising edge when the preset enable is low. Since this parallel load is performed on the fly as the message is shifting through the register, the pause for loading causes the registers to "miss" one shift clock; to compensate for this loss the register contents are "jumped" one stage to make up the one shift clock deficit. The C11 register is asnychronously loaded by the Shift/load line and is independant of the clock; the DCS address bits are wired to two inputs on this register. The timing of this logic is depicted below.

The incoming message stream is inverted by C2712 and reclocked by flip flop A1005 (sheet 1) to form the low-true Gossip data which is output to the Data Set 0 - 4 Command Ports or-gates which cause it to be broadcast to all Data Sets. Note that this pickoff point is upstream from the DCS injection logic so that the monitor data **always has a DCS address of 0** irrespective of the actual SB DCS address. This feature can be very convenient at a Data Tap as it permits observation of the monitor data message flow from a Data Set distinct from the command message flow (set the Mux sel switch to any).

DCS/DSA ADDRESS & PARITY BIT INJECTION LOGIC TIMING



(Assumes that sum of DCS/DSA data bits in the byte is even)

The Monitor Data Load Counter, C8 and C13 generates a load enable to permit the monitor data messages to be loaded into the Monitor Data Memory, E14, E19 and E24. The memory is loaded by the shift clocks generated by C1814 which are used to shift in the monitor data message as described above. Counter C8 and C13 are preset to a count of 135 by the S detect gate C0210 which sets counter control flip-flop C1711 and presets the counter to a count of 135. The terminal count of C13 is and'ed with the clock in gate D22 to reset C1711 which terminates the load enable. The load enable, C1711 is fed to the and-or gates E0810 and E1606 (Sheet 8) which causes the monitor data message to be shifted into the serial monitor data memory. The monitor data message to be loaded is tapped off shift register C0114 on Sheet

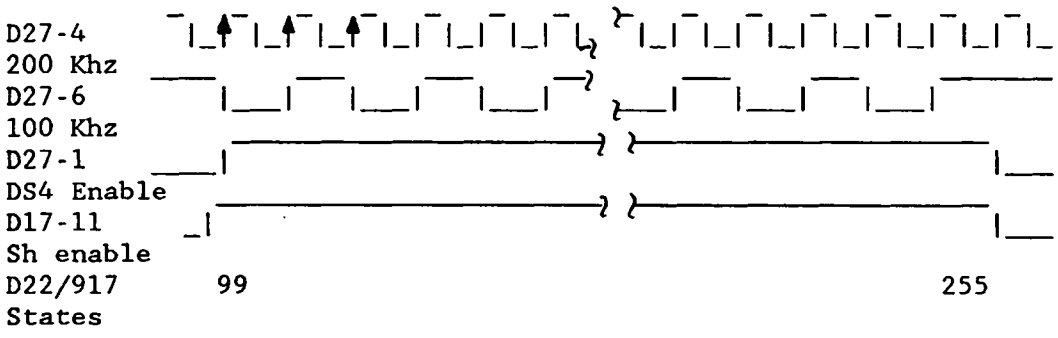
3. The timing of this logic is depicted below.

Pull-up resistors B21-3,4 provide a 5 volt swing for the memory data input and clock lines.

MONITOR DATA MEMORY LOAD TIMING

DATA GENERATOR LOGIC -- The data generator logic on Sheet 4 generates a monitor data message in response to a DS4 Enable from A2505 (Sheet 1). Referring to this sheet we see that A2505 is set at 300 usec if DSHF (low true) is low; that is if the selected Data Set has not respoded within 300 usec, (it should respond in 250 usec) the DS4 Enable term goes true and the Data Generator is triggered into operation. Load control counter D22/D17 is enabled by the DS4 Enable. Flip-flop D2706 divides the 200 Khz clock to produce the 100 Khz clock pulses which unload the D1, D2 portions of the register. The 200 Khz clock unloads the D1/D2 portion of the register. The delay line D12 provides about 80 nanoseconds of delay to the 100 Khz shift clocks so that D1 can properly sample the output of D6. The DS4 Enable permits the Data Generator output to be routed through the 2:1 multiplexer A0804 (Sheet 5) on the output of the data selector multiplexer in the Data Set Monitor Data Ports. Thus the DS4 Enable selects the output of the Data Generator rather than the Data Set multiplexer, A1315. The commands detected by the command detectaion circuitry are counted by D23 and are caused to be loaded with the mux address 205 (octal) DS4 enable. Counter D23 is cleared by the QQ pulse from the L8 at the start of the 1000 usec period. The operation of this logic is depicted in the simplified timing diagram on the next page.

DATA GENERATOR OUTPUT TIMING



470 ohm pull-up resistors are used on the memory data and clock inputs; the AMD 2855PC requires a high input greater than 4 volts, a marginal level for TTL logic; the pull-up resistor provides a 5 volt level. These serial memory chips shift on the fall of the clock rather than the rise like the other shift registers in the SB. The AM2855PC data sheet is included in the back of this manual.

DATA SET #5 MONITOR DATA POLLING, LOADING AND STORAGE - - Having loaded the DS 0 .. DS 4 monitor data into the serial monitor data memory, we will now consider the operations of polling Data Set #5 for monitor data messages.

The 20 usec duration, 48,400 and 49,400 low-true discrete enables from the time base logic loads a Q into shift register F1 and F6 (Sheet 6); when the load term rises the 200 Khz shift clocks push out the Q through or-gate B1213 and the low-true Data Set Command Port J2-32/33. Register stage F0611 provides an initial 0 to the Q character so that the first 1 is the proper 5 usec.

The Data Set should respond to the Q within 50 usec and begin to output the monitor data message within 250 usec after the start of the Q. The low-tru monitor data message evoked by th Q is input on the Data Set Monitor Data Port, J2-28/29. Optical isolator A1110 detects and inverts the signal. Shift register C25 and exclusive or C2413 detect signal edges to synchronize counter C20/C15 which sample the signal in the center of the pulse. Counter C20/C15 is preset to a count of 1 by the exclusive or C2413 and is clocked by 5 Mhz. At the count of 37 gate C3006goes true and feeds back to the pre-set input through B0501;thus the counter radix is 37. At the count of 32, the 16 term in C15 falls which generates a shift clock (via inverter B1714). The 200 Khz 32 term in C15 clocks the serial data stream into S detect register C19 where the S is detected by gate C0910. A message loading sequence is initiated in which load control flip-flop B0411 and counter C5/C10 generate a load enable to permit the monitor data message to be loaded into the serial

monitor data memory. The counter is preset to a count of 151; at the count of 256 (i.e. when all bits fall), control flip-flop B0411 is reset which inhibits the monitor data load clocks and data at gates E0810 and E0814 respectively.

It is worthwhile to consider the order of the monitor data messages in the monitor data memory. The monitor data memory (E14, E19 and E24) is a set of quad 128 bit MOS shift registers (identical to those used in the Central and Antenna Buffers). The order of data in the memory (from the farthest point) is: MW-1, DS-0...DS-4; MW-2, DS-0...DS4; MW-1, DS-5; MW-2, DS-5. At the end of the Data Set 5 load, this data and some spacing bits are pushed deeply into the memory but are not at the output; message positioning logic at the bottom of Sheet 8 performs this function. Because the SLC monitor data polling period is very short; 59 usec, there is not enough time to wait for the first (or subsequent) monitor data messages to shift to the memory output. In operation, this logic positions the monitor data messages at the output of the memory so that it is immediately available when polled by the SLC. The message positioning logic detects the S character and halts the shift process in anticipation of the next Q character.

The first monitor data message is positioned at the memory output so that it is ready for immediate output at the beginning of the cycle. At t = 0, the low-true 400 ns QQ pulse from gate B2404 (Sheet 1) direct sets flip-flop E1511 through low-true or gate E1613. This control flip-flop permits 2 Mhz push clocks to shift the memory contents via gate register E18 until stopped by the S detect gate E2310 which resets flip-flop E1511. This 2 Mhz clock is phased to the Q detection logic (Sheet 1, discussed below) so that the data unload clock is coherent with the SLC Q edges.

3.4 SLC MONITOR DATA POLLING

Having loaded the serial monitor data memory and positioned the first message at the memory output let us now consider the SLC polling and monitor data output to the SLC. The SLC polls each CB in the sequence: DCS-0...DCS-32; DCS-0...DCS32; etc for a total of 12 cycles. The time intervals of the SLC Q at a given buffer is therefore 32 x 59 usec or 1888 usec. When an SLC Q is detected, the low-true Q detection gate, D1810 ,(Sheet 6, see the SLC Q detection discussed in the SLC command detection logic) sets flip-flop E1511 through low true or gate E1613 which permits unload clocks to shift the message out to the SLC via the SLC Monitor Data Port, J2-6. The unload operation is terminated when the S character of the next message is detected via gate E2310.

Note that the action of this unload logic is just the reverse of all the S detect/load control counters in the Monitor and Control System; in all other cases the S detection causes a

message load sequence; in this logic it terminates a message unload sequence, (except for the first message initialization case).

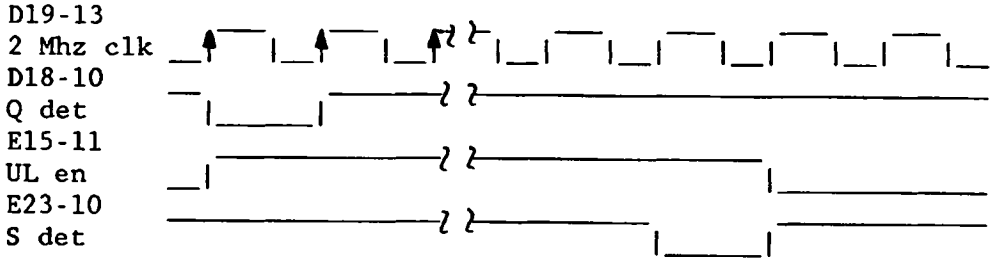
The control flip-flop E1511 is is permitted to operate only during the period of 0 - 24,000 by the 0 - 24,000 enable from the time base logic. This enable holds this flip-flop reset at all times except during this aperature. Enable 1k - 24k at gate E0903 enables the monitor data output to the SLC during the SLC polling period.

One shot E2707 provides up to 250 ns of delay of the memory shift clocks for shift register E18; this delay is to accomodate the worst case propagation delay of the AM 2855PC monitor data memory. The delay should be set up by checking the eye pattern of the data and clock on an oscilloscope.

An important use of flip-flop E1511 is the "inhibit gossip data" feedback to the SLC Command Signal Input logic. When the SB outputs a monitor data message to the SLC, it is immediately rebraodcast on the SLC command output lines to the SB's Command Signal Input which will edge-phase a sampling clock to the incoming message stream. Since the monitor data unload clock is this edge-phased clock this would be a positive feedback situation were it not for this gossip data inhibit term.

The timing of the SLC polling/monitor data unload logic is shown in the simplified timing diagram below.

MONITOR DATA UNLOAD TO SLC



3.4 POWER CIRCUITS -- The MOS memories require non-standard 12 volt and -5 volt power; Motorola MC7905 and MC7912 regulators provide the negative voltages. These regulators require isolation of the case from module ground; if these chips fail, don't forget to replace the mica washers and Silicone grease when replacing them. If non-Motorola replacements are substituted, be sure of the wiring because other manufacturers regulators have similar part numbers but a different pin-out.

4.0 List of System Buffer Drawings

D13721L79	System Buffer Logic Diagram
D13721P63	System Buffer Top Assembly Drawing
A13721Z66	System Buffer Top Bill of Materials
A13721P64	System Buffer IC Location Diagram
B13720AB05	LED Display PCB Artwork
C13720M36	LED Display PCB Drill Drawing
A13720P39	LED Display Assembly
C13720M16	Front Panel Mechanical Drawing
B13050M17	Perf Cover Fastener
C13050M7	Perf Cover
C13720M15-1,2	Rail Modification
C13720M17	Insulated Spacer
C13720M23	Rear Panel
C13720M50	Side Plate, Modified
C13720M49	Side Plate Insulation
C13720P68	Insulated Side Plate Ass'y
C13720M32	DCS Module WW Field Dim Def
D13720M96	Buffer Wiring Jig Configuration

5.0 Special Module Data Sheets

The Data Sheet for the AM2855PC serial MOS memory follows this page.

Am2855 • Am2856 • Am2857

Quad 128-Bit, Dual 256-Bit and Single 512-Bit Static Shift Registers

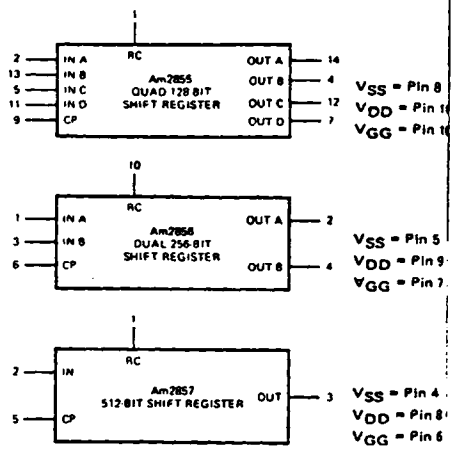
Distinctive Characteristics

- High-speed replacement for National 5055/6/7
- Internal recirculate
- Single TTL compatible clock
- Operation quaranteed from DC to 2.5MHz
- 100% reliability assurance testing in compliance wi MIL-STD-883

FUNCTIONAL DESCRIPTION

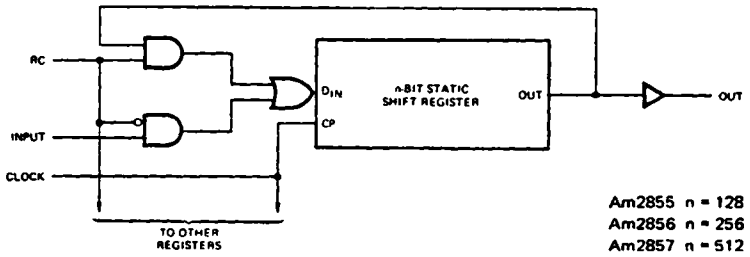
These devices are a family of static P-channel MOS shift registers in three configurations. The Am2855 is a quad 128-bit register; the Am2856 is a dual 256-bit register; and the Am2857 is a single 512-bit register. All three devices include on chip recirculate. The registers are all clocked by a single low-level clock input. Because the registers are static, the clock may be stopped indefinitely in the LOW state without loss of data. Each of the registers has a single data input; data on the input is written into the register on the HIGH-to-LOW clock edge. A single recirculate control (RC) on each chip determines whether the registers on that chip are to write data in from the data inputs or recirculate the data appearing on the output. If RC is LOW, new data is written in; if RC is HIGH then the data on the output will be written back into the register input on the next clock pulse.

LOGIC SYMBOLS



MOS-440

LOGIC BLOCK DIAGRAM
(One Register Shown)



Am2855 n = 128
Am2856 n = 256
Am2857 n = 512

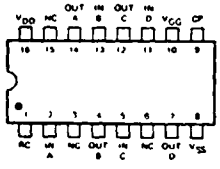
MOS-441

ORDERING INFORMATION

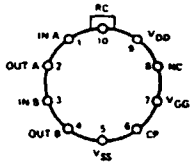
Package Type	Temperature Range	Order Number
16-Pin Molded DIP	0°C to +70°C	AM2855PC
16-Pin Hermetic DIP	0°C to +70°C	AM2855DC
16-Pin Hermetic DIP	–55°C to +125°C	AM2855DM
10-Pin Plastic DIP	0°C to +70°C	AM2856PC
TO-100 Can	0°C to +70°C	AM2856HC
TO-100 Can	–55°C to +125°C	AM2856HM
8-Pin Molded DIP	0°C to +70°C	AM2857PC
8-Pin Hermetic DIP	0°C to +70°C	AM2857DC
8-Pin Hermetic DIP	–55°C to +125°C	AM2857DM

CONNECTION DIAGRAMS

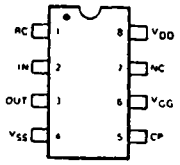
Am2855



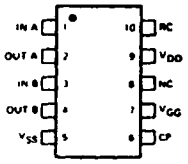
Am2856



Am2857



Am2856



MOS-442

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +160°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{DD} Supply Voltage	V_{SS} −10V to V_{SS} +0.3V
V_{GG} Supply Voltage	V_{SS} −20V to V_{SS} +0.3V
DC Input Voltage	V_{SS} −20V to V_{SS} +0.3V

OPERATING RANGE

Part Number	Ambient Temperature	V_{SS}	V_{DD}	V_{GG}
Am2855DM Am2856HM Am2857DM	−55°C to +125°C	5.0V ±5%	0V	−12V ±5%
Am2855PC, DC Am2856HC Am2857PC, DC	0°C to +70°C	5.0V ±5%	0V	−12V ±5%

5

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −0.5mA	2.4			Volts
V_{OL}	Output LOW Voltage	I_{OL} = 1.6mA			0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	V_{SS} −1.0		V_{SS} +0.3	Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	V_{SS} −18.5		V_{SS} −4.2	Volts
I_{IL}	Input Leakage Current	V_{IN} = −10.0V, all other pins GND, T_A = 25°C		0.01	0.5	µA
I_{DD}	V_{DD} Power Supply Current	T_A = 25°C, $t_{\phi pw}H$ = 160 ns, Data = 1010. . . , output open, f = 2.5 MHz		20.0	28.0	mA
I_{GG}	V_{GG} Power Supply Current			12.0	16.0	mA

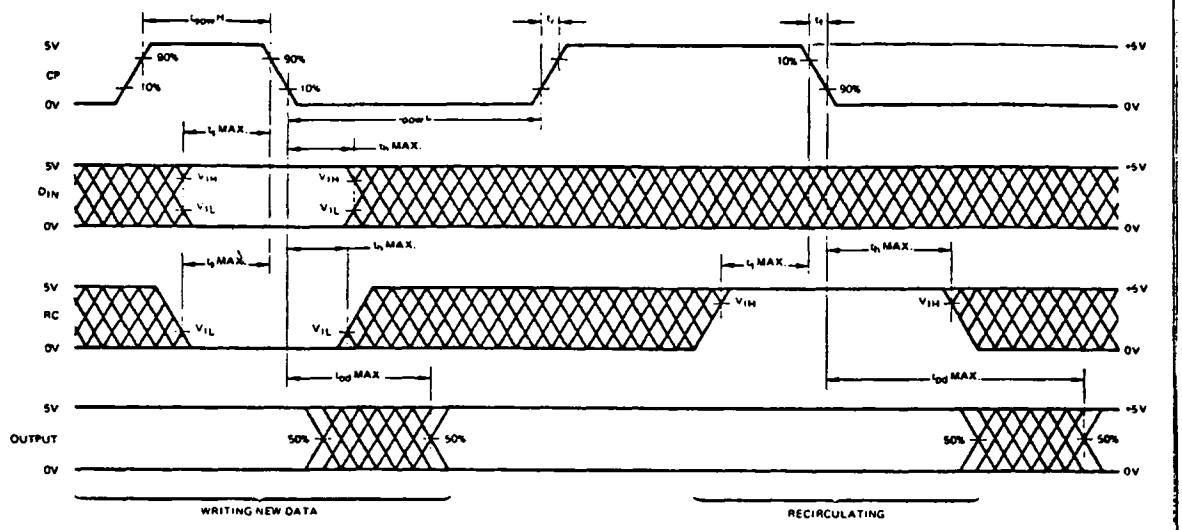
Note: 1. Typical Limits are at V_{SS} = 5.0V, V_{GG} = −12V, 25°C ambient and maximum loading.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

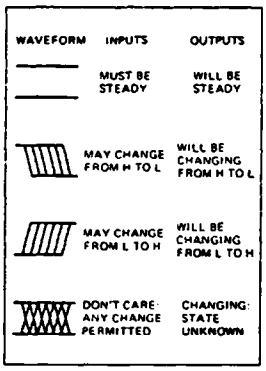
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
f	Clock Frequency		0		2.5	MHz
$t_{\phi pw}H$	Clock HIGH Time		0.16		10.0	µs
$t_{\phi pw}L$	Clock LOW Time		0.200		∞	µs
t_r, t_f	Clock Rise and Fall Times		10		200	ns
t_s	Set-up Time, D or RC Inputs (see definitions)	t_r = t_f = 50ns	100			ns
t_h	Hold Time, D or RC Inputs (see definitions)	t_r = t_f = 50ns	40			ns
t_{pd}	Delay, Clock to Output LOW or HIGH	R_L = 4k, C_L = 10pF	(Note 3)	160	280	ns
C_{in}	Capacitance, Data In and RC Inputs (Note 2)	f = 1MHz, V_{IN} = V_{SS}		3	7	pF
C_o	Capacitance, Clock Input (Note 2)	f = 1MHz, V_{IN} = V_{SS}		3	7	pF

Notes: 2. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.
3. At any temperature, t_{pd} min. is always much greater than t_h(D) max.

TIMING DIAGRAM

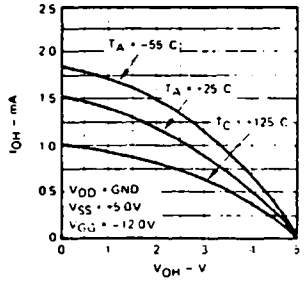


KEY TO TIMING DIAGRAM

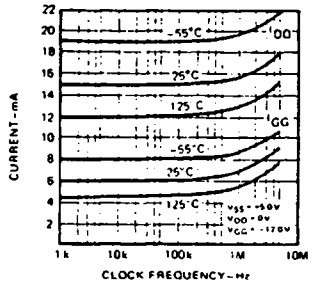


PERFORMANCE CURVES

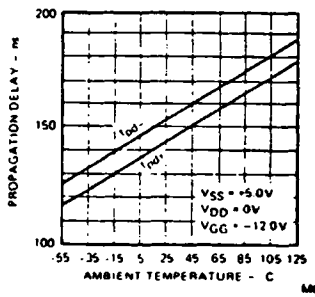
Typical Data Output HIGH Current Versus Data Output Voltage



Typical Power-Supply Currents Versus Frequency



Typical Propagation Delay Versus Ambient Temperature



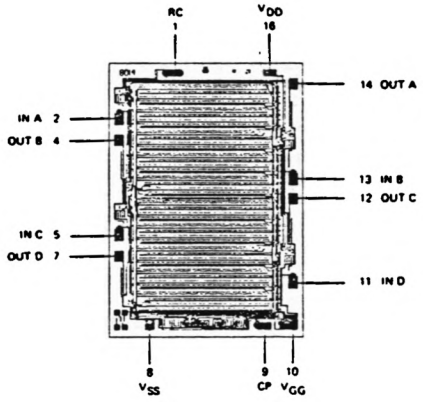
DEFINITION OF TERMS

STATIC SHIFT REGISTER A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is HIGH and is transferred to the static slaves while the clock is LOW. The clock may be stopped indefinitely in the LOW state, but there are limitations on the time it may reside in the HIGH state.

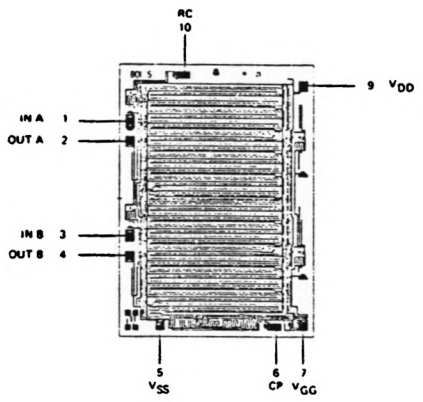
SET-UP and HOLD TIMES The shift register will accept the data that is present on its input around the time the clock goes from HIGH-to-LOW. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

Metallization and Pad Layouts

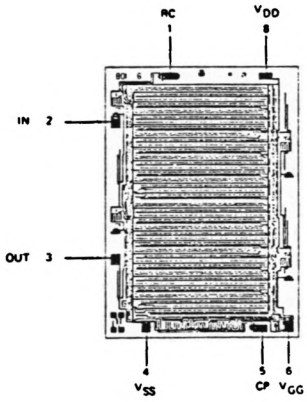
Am2855



Am2856



Am2857



DIE SIZES: 0.101" X 0.142"

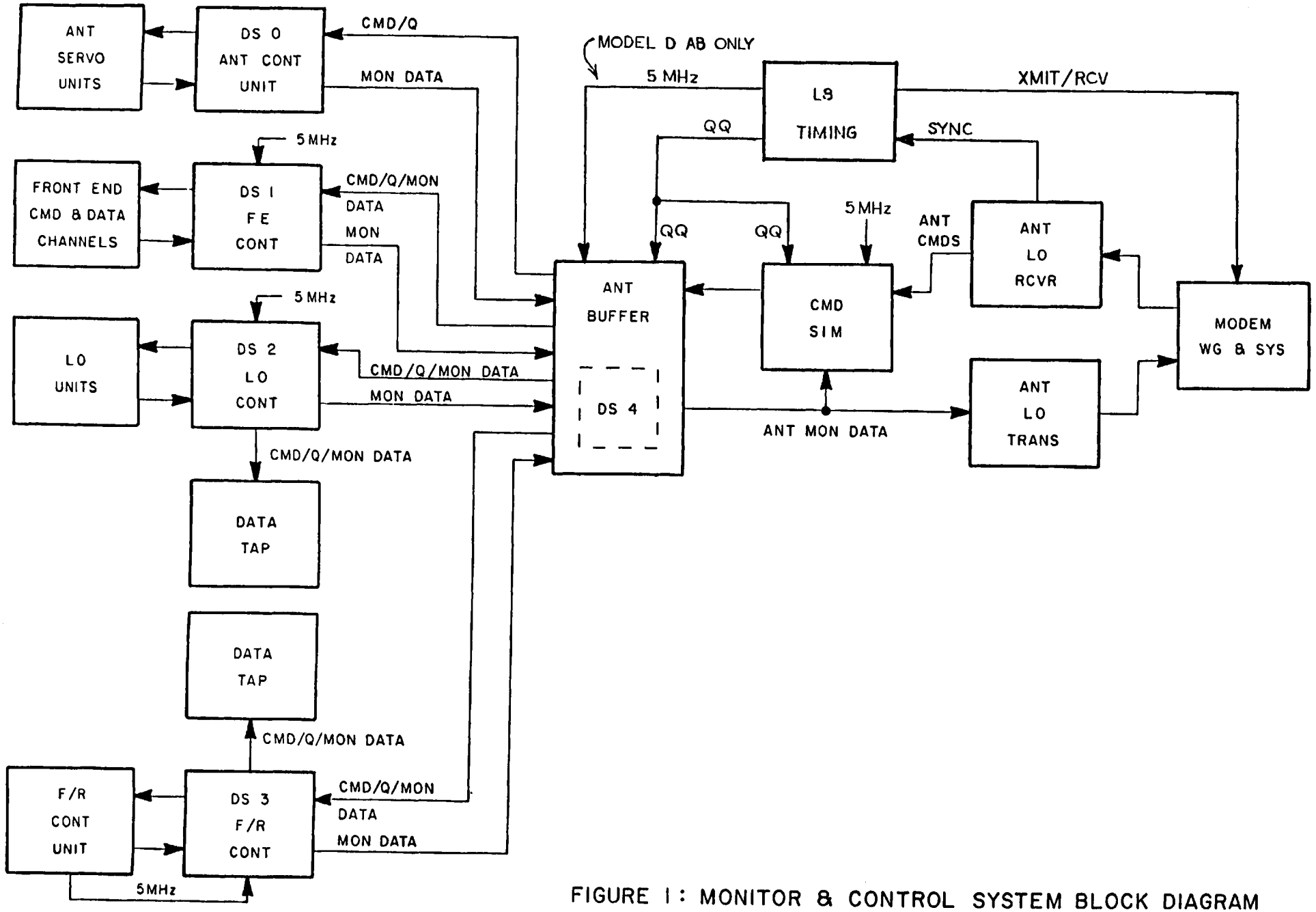


FIGURE 1: MONITOR & CONTROL SYSTEM BLOCK DIAGRAM

REV. 7-86

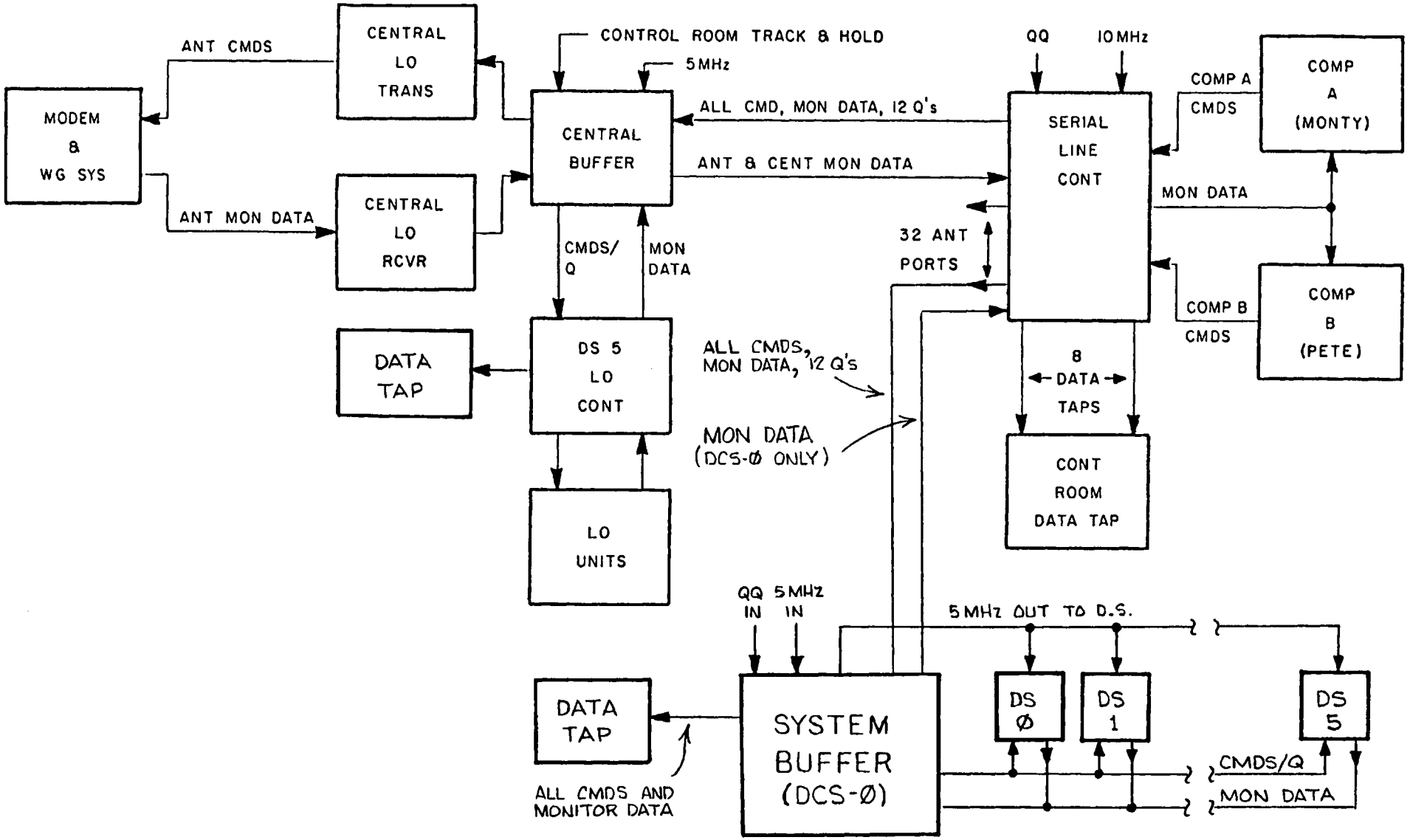


FIGURE 1: CONTINUED

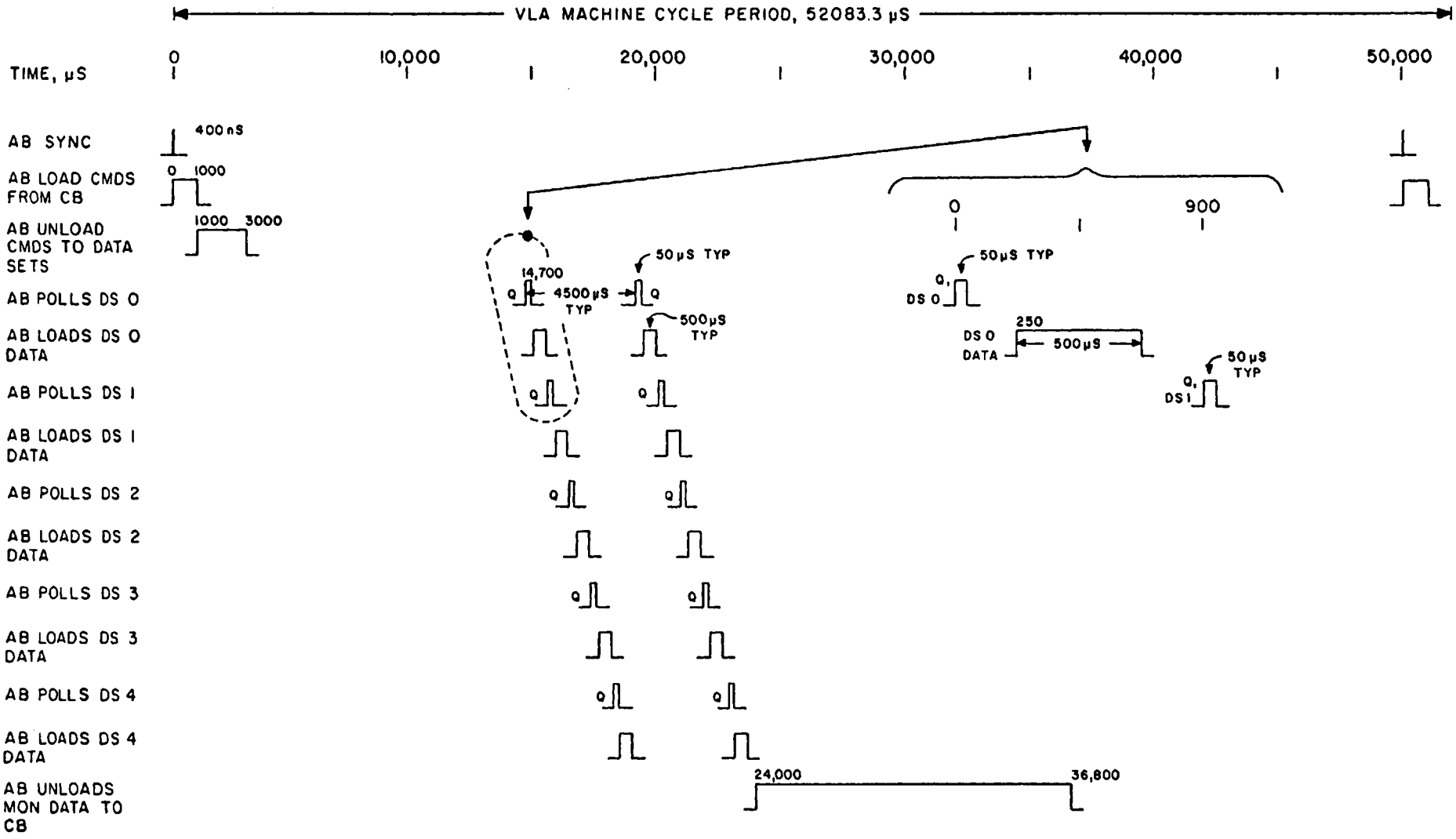


FIG. 2
ANTENNA TIMING OPERATIONS

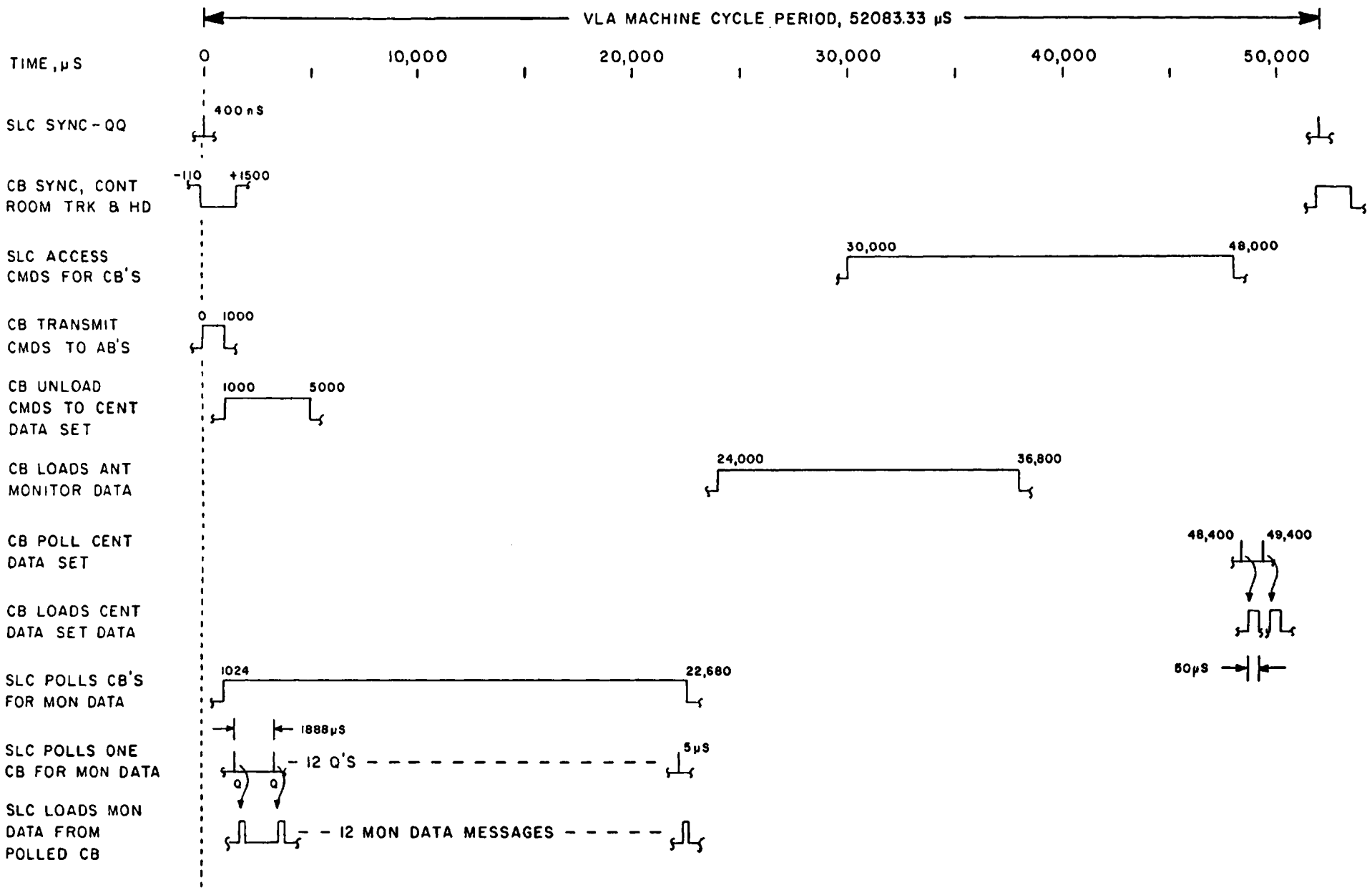


FIG. 3
CENTRAL TIMING OPERATIONS

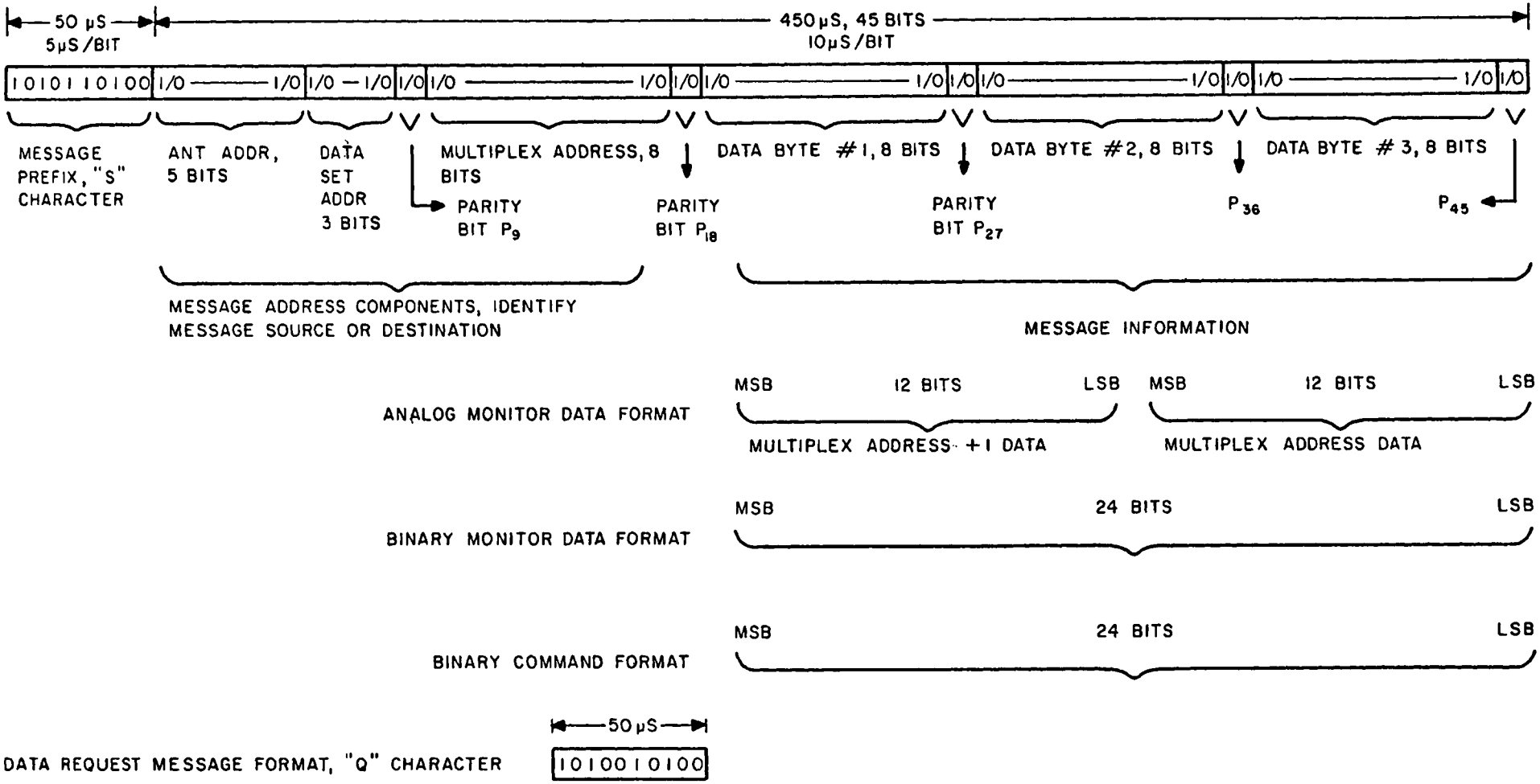


FIGURE 4: DATA SET COMMAND AND MONITOR DATA AND DATA REQUEST MESSAGE FORMATS

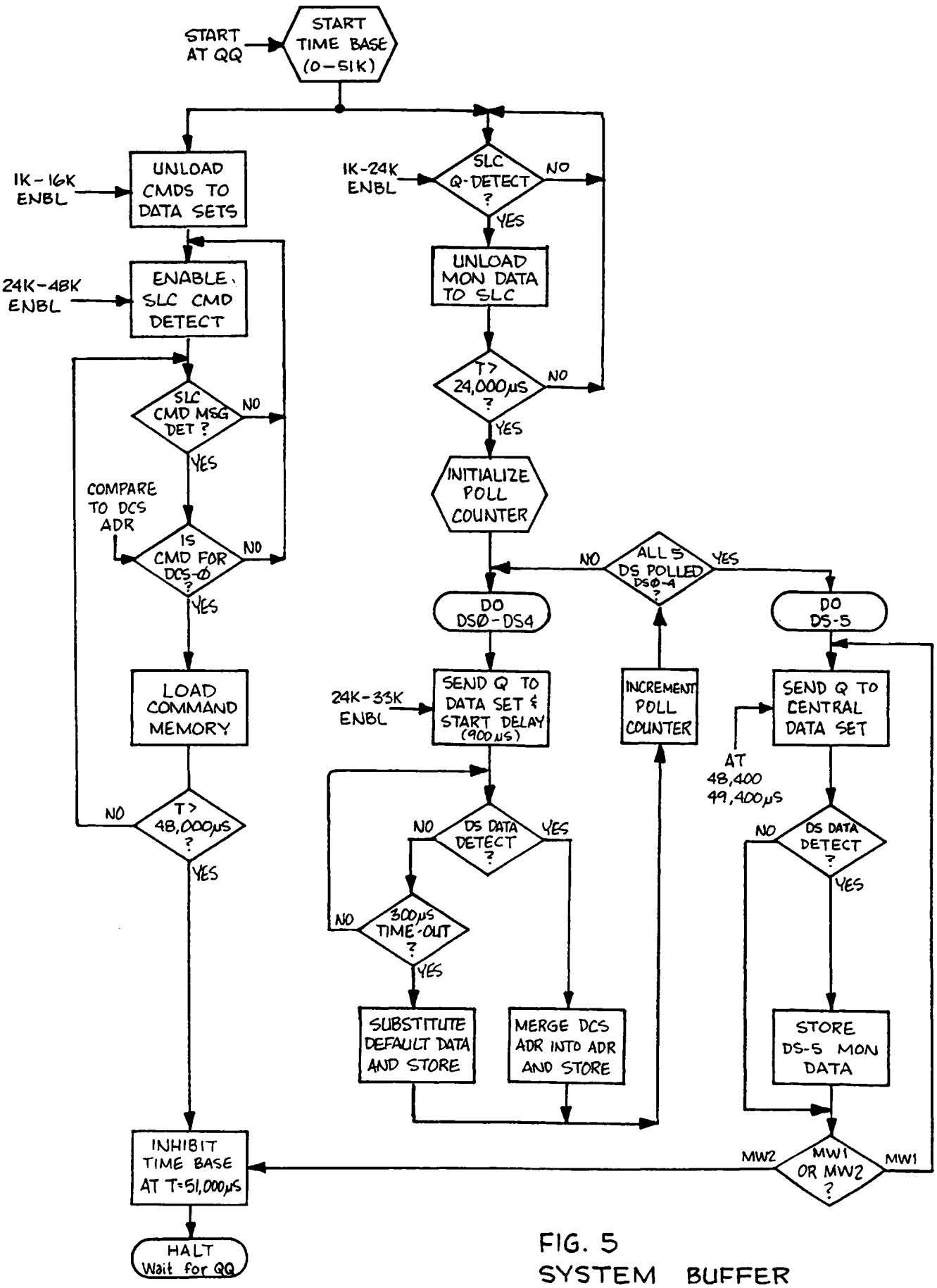


FIG. 5
SYSTEM BUFFER
LOGIC FLOW DIAGRAM

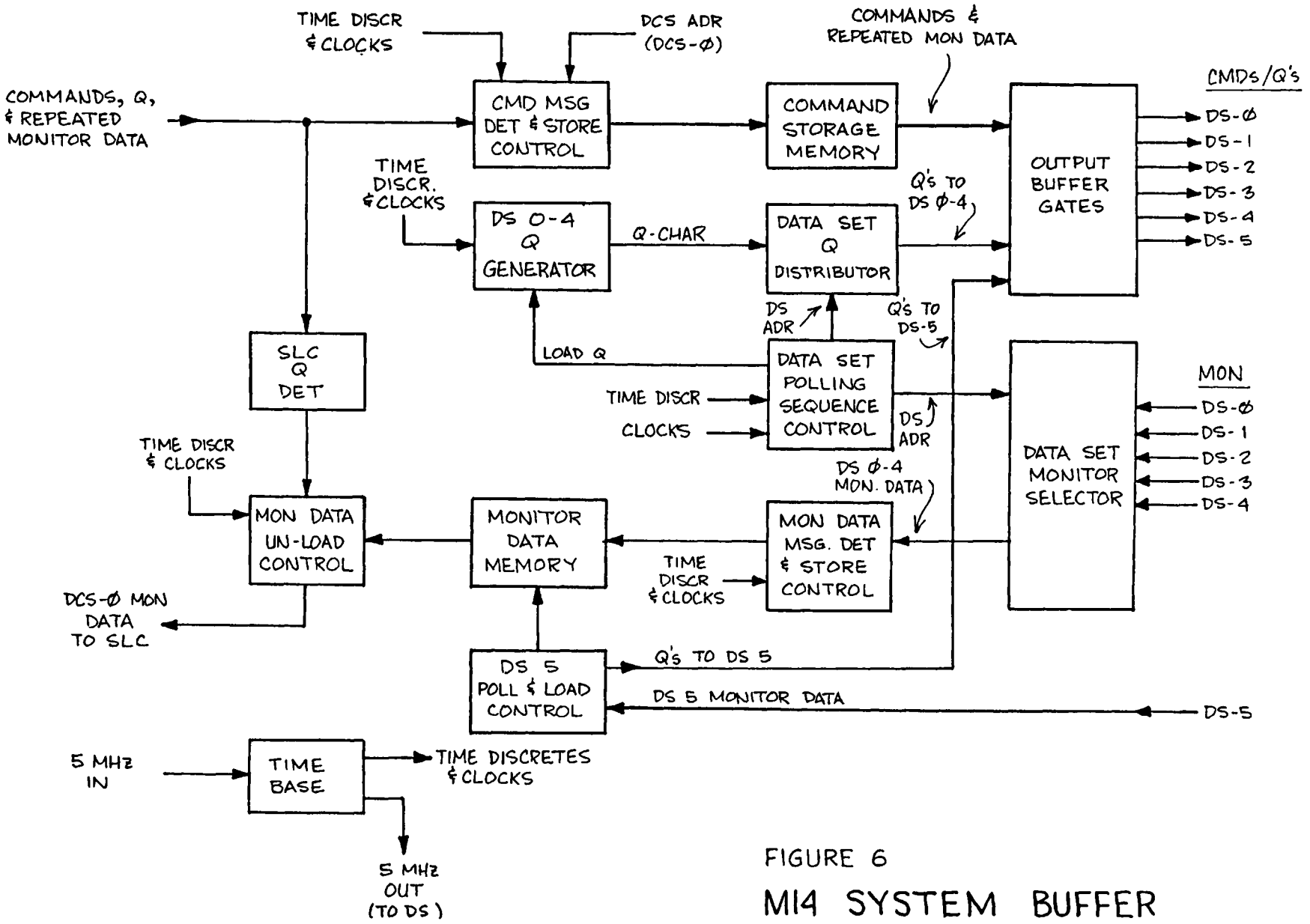


FIGURE 6

MI4 SYSTEM BUFFER BLOCK DIAGRAM

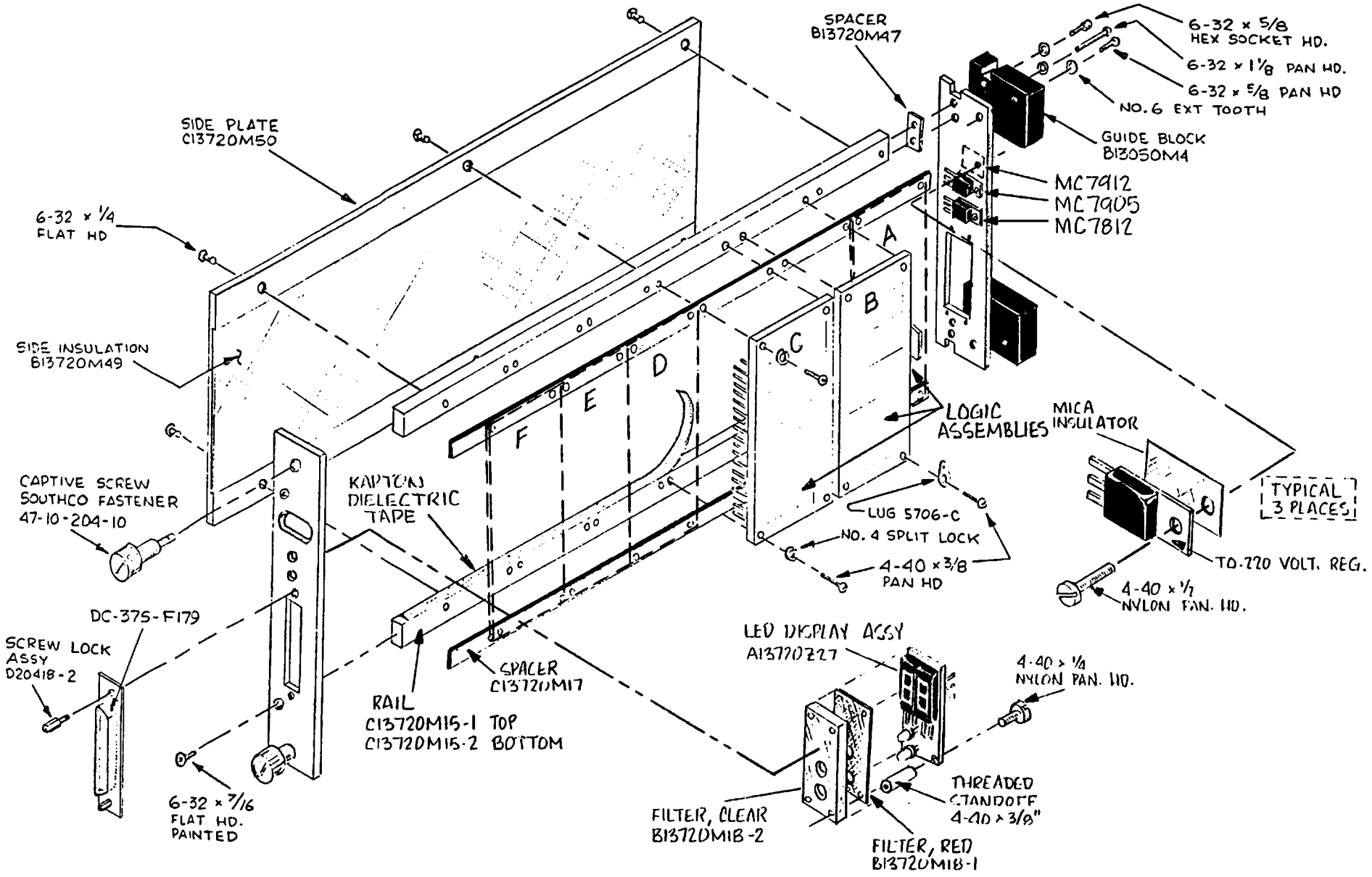
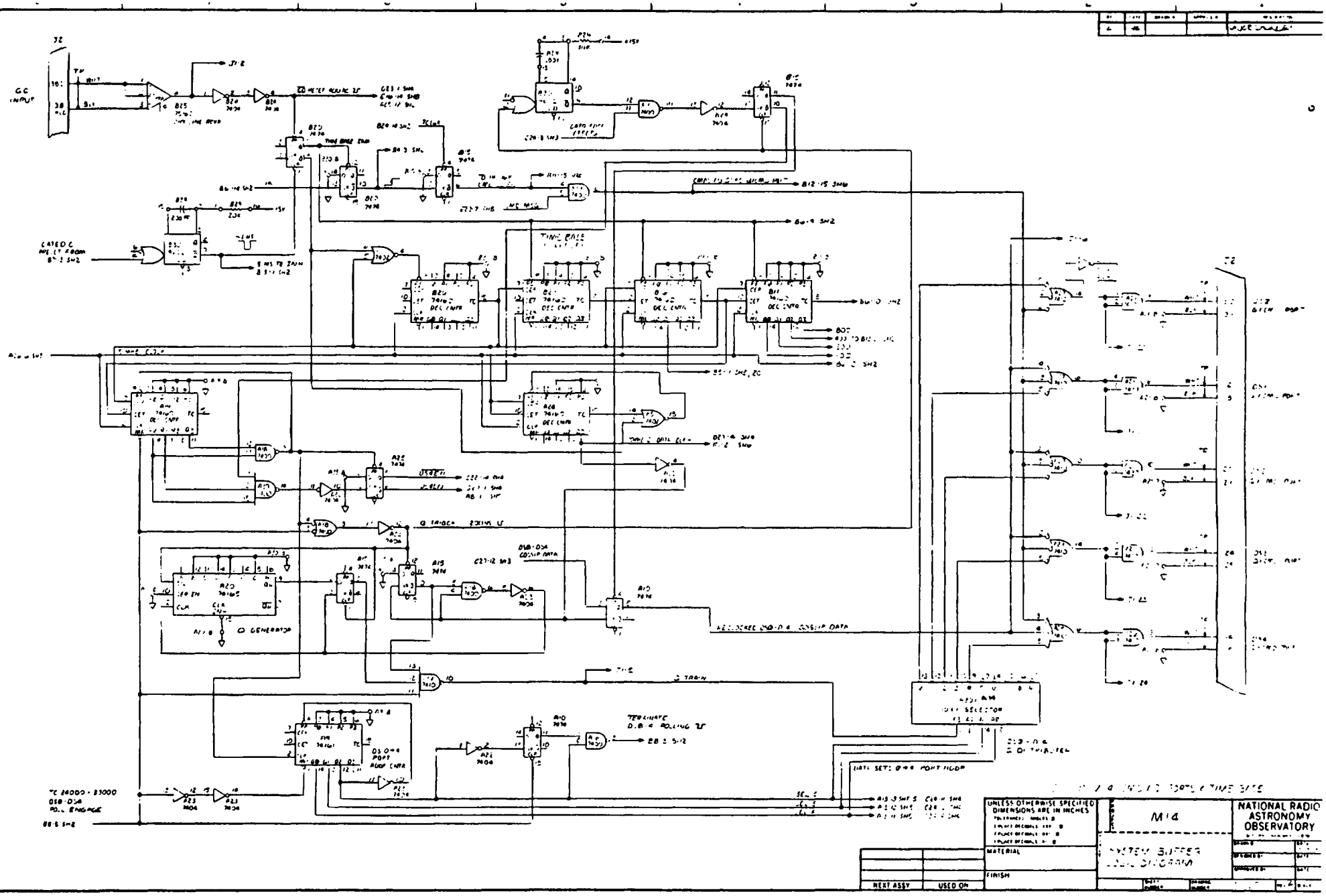
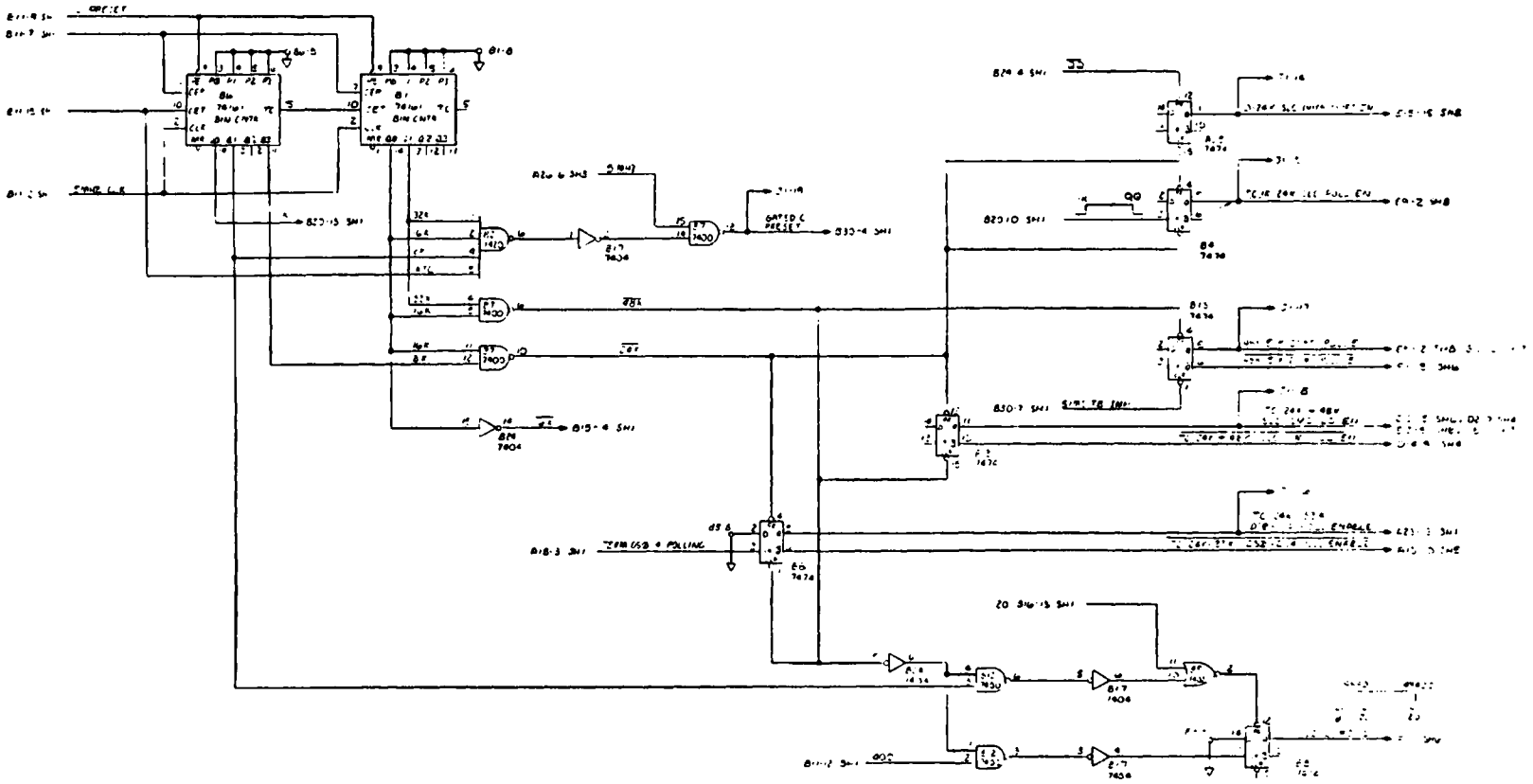


FIG. 7

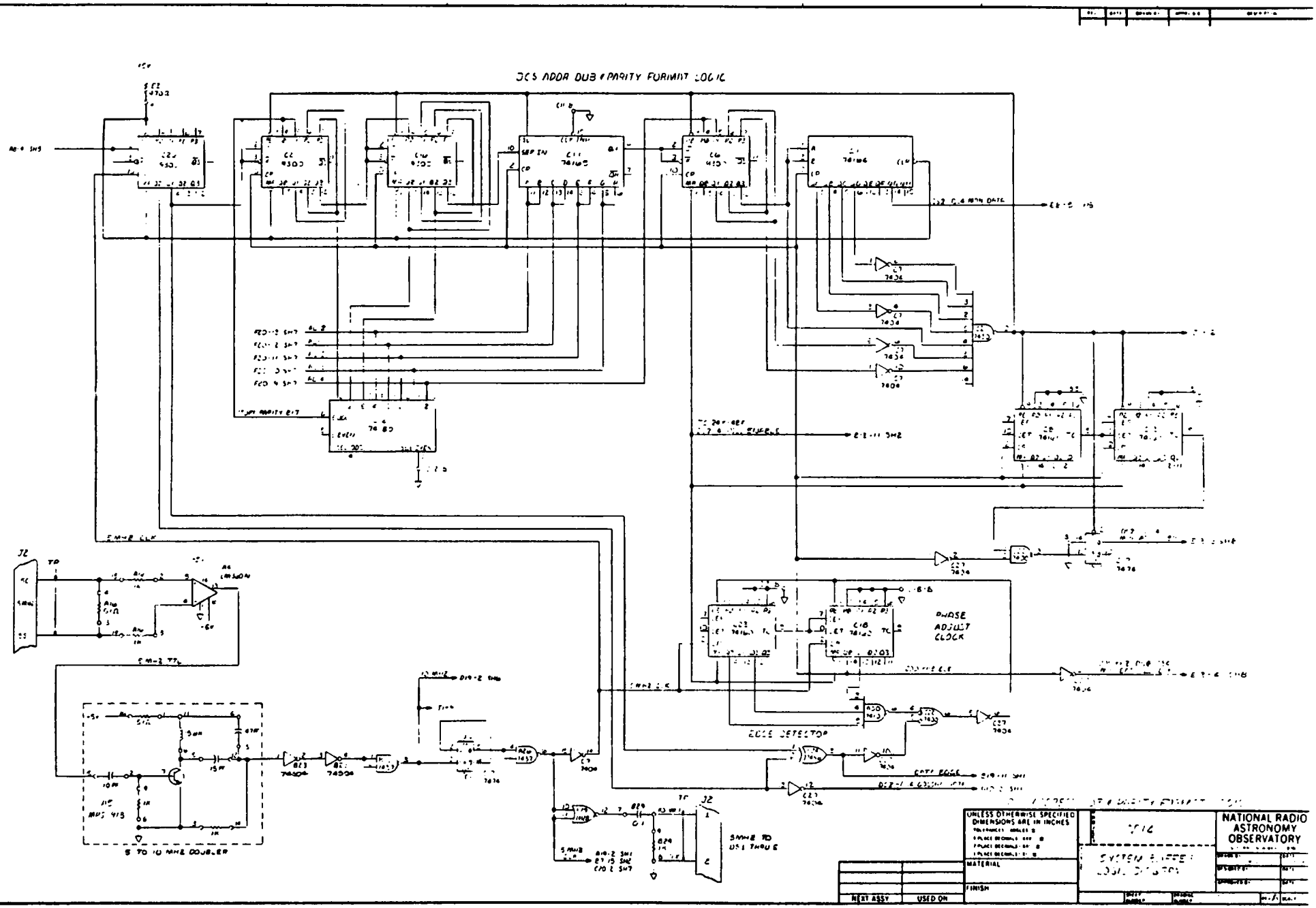
ILLUSTRATED PARTS BREAKDOWN

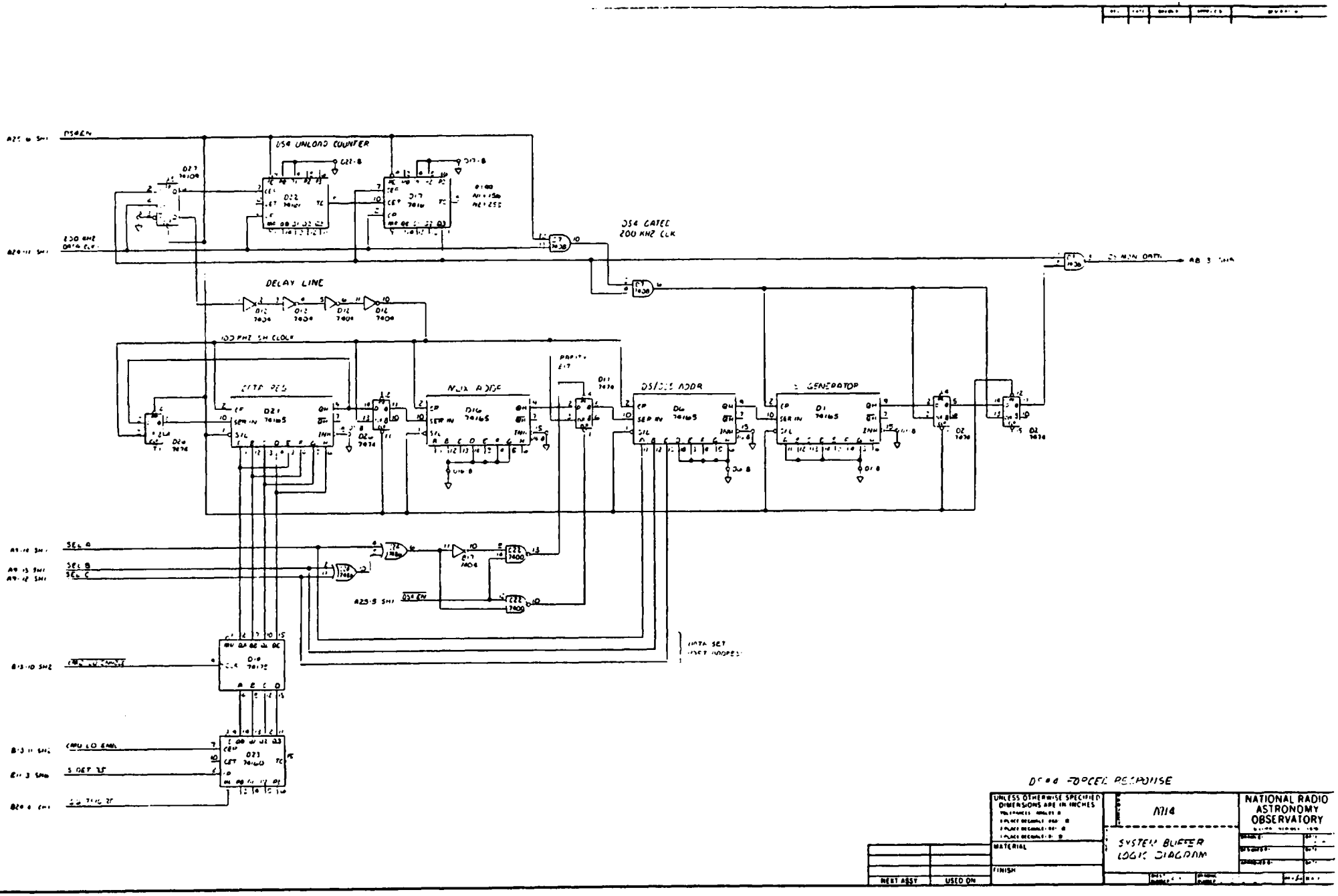
M14 SYSTEM BUFFER

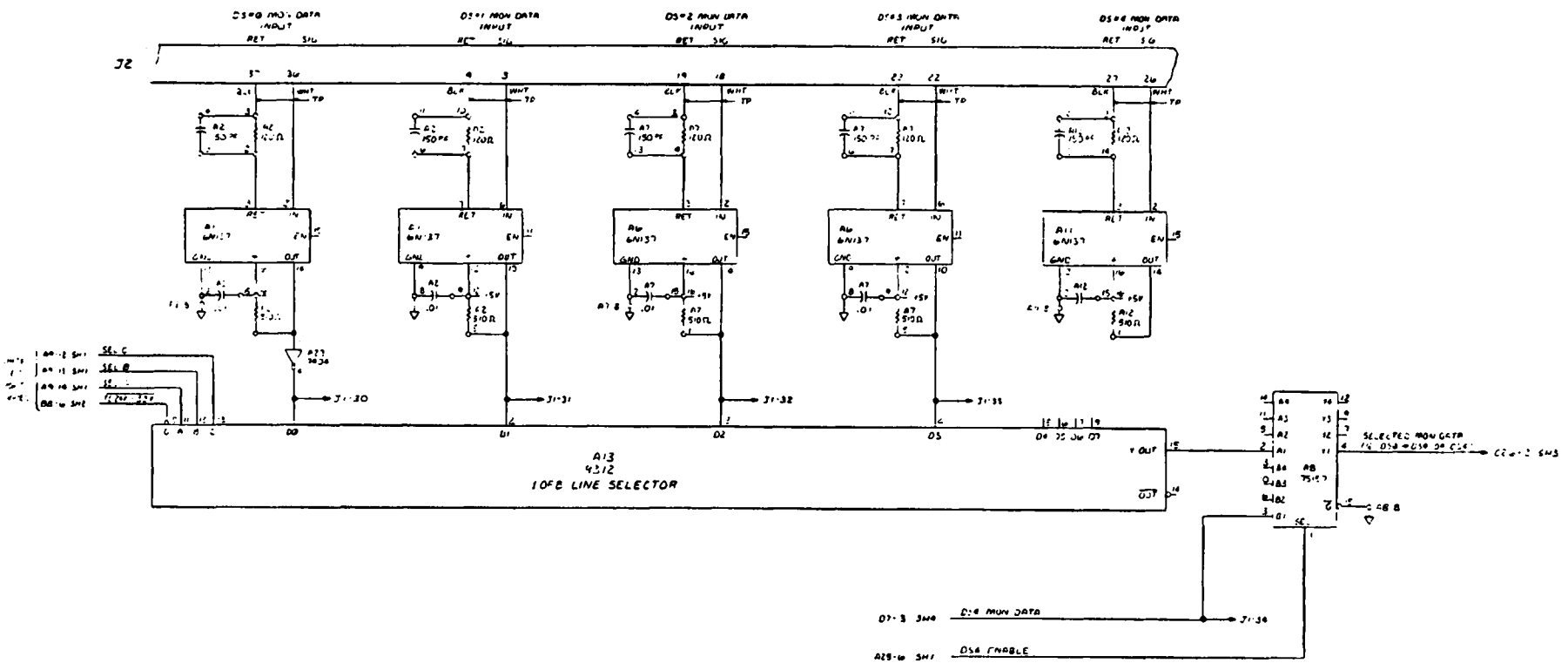

M14
SYSTEM BUFFER
LOGIC DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL
FINISH
NEXT ASSY
USED ON



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		NATIONAL RADIO ASTRONOMY OBSERVATORY
MATERIAL		
FINISH		
NEXT ASSY	USED ON	

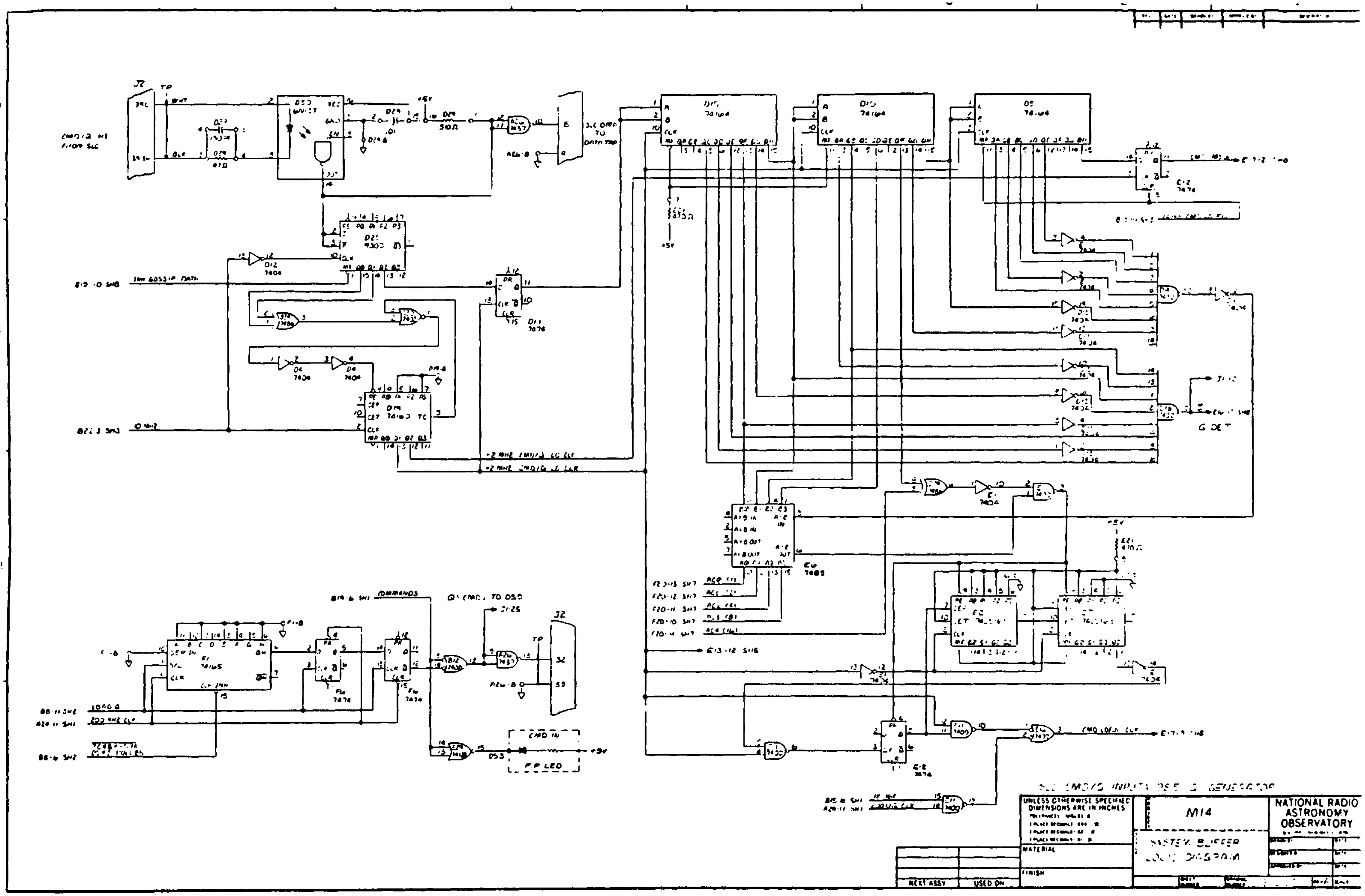

DCS ADDR DUB & PARITY FORMAT LOGIC
PHASE ADJUST CLOCK
EDGE DETECTOR
5 TO 10 MHz DOUBLER
NATIONAL RADIO ASTRONOMY OBSERVATORY
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL
FINISH
NEXT ASSY
USED ON


DS4 UNLOAD COUNTER
DELAY LINE
DS4 GATED 200 KHZ CLK
100 KHZ SH CLOCK
DS4 FORCED RESPONSE
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL
FINISH
NEXT ASSY
USED ON
NRAO
NATIONAL RADIO ASTRONOMY OBSERVATORY
SYSTEM BUFFER LOGIC DIAGRAM

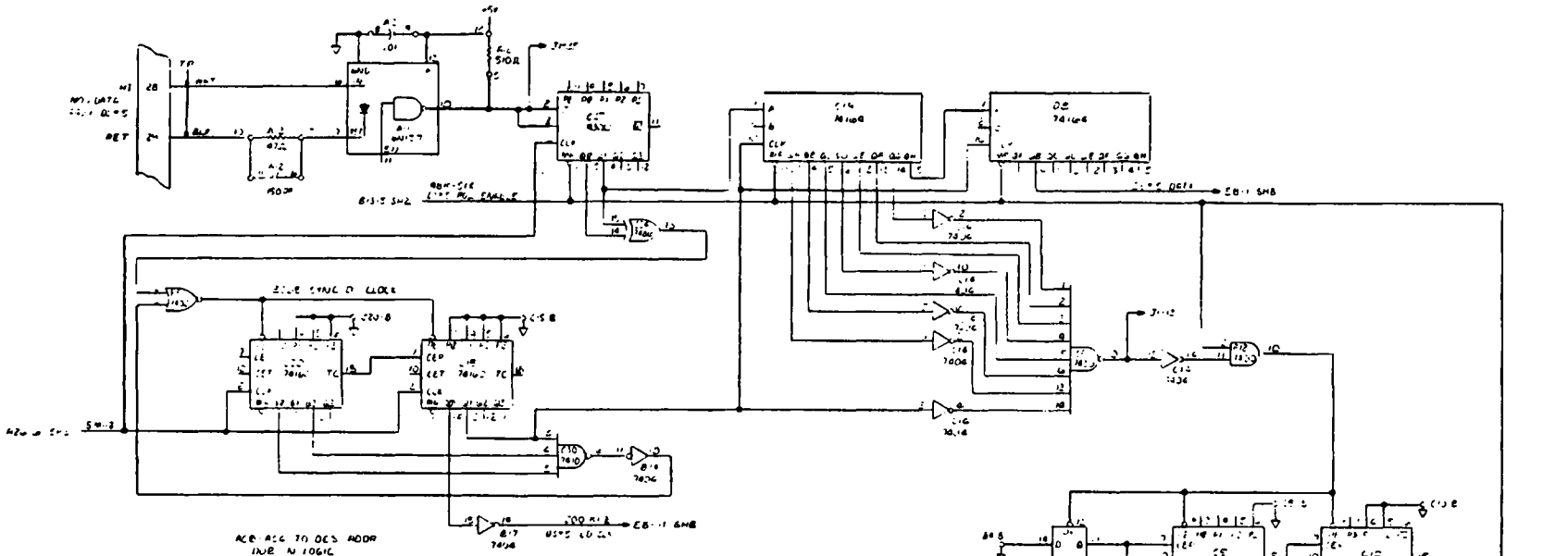


DS#0-4 MON DATA INPUT PORTS

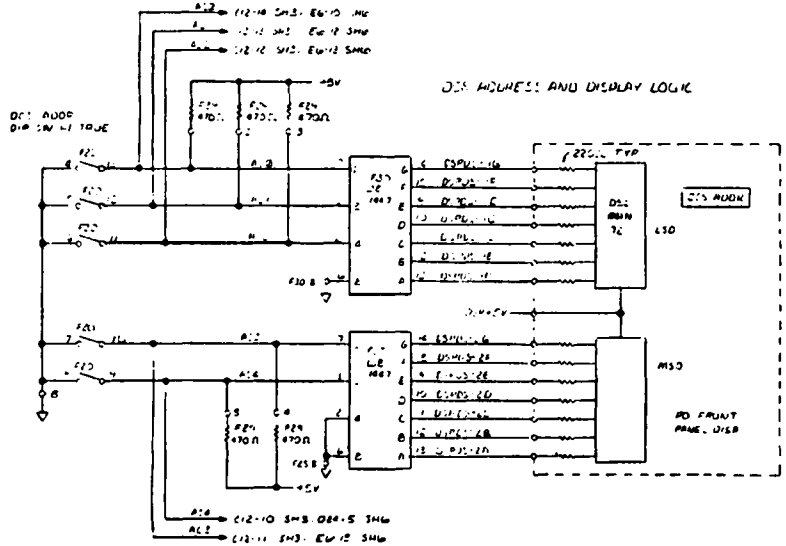
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	A114	NATIONAL RADIO ASTRONOMY OBSERVATORY	
MATERIAL	SYSTEM BUFFER LOGIC DIAGRAM		
FINISH			
NEXT ASSY / USED ON			A

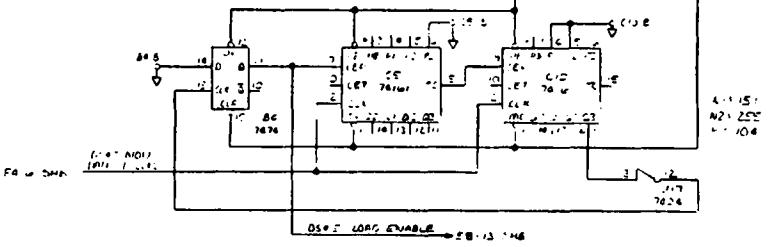

J2
TP
CMD/12 MHZ FROM SLC
D53
6N137
+5V
510Ω
S.C DATA TO DATA TAP
D15
74164
D10
74164
D5
74164
D21
9300
D11
7474
D16
74161
E13 -10 SHB
E13 -12 SHB
G DET
E16
7485
E2
74161
E8
7474
COMMANDS
F1
74165
CMD IN
F.P. LED
+5V
CMD LOAD CLK

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL
FINISH
NEXT ASSY
USED ON
M14
SYSTEM BUFFER LOGIC DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY

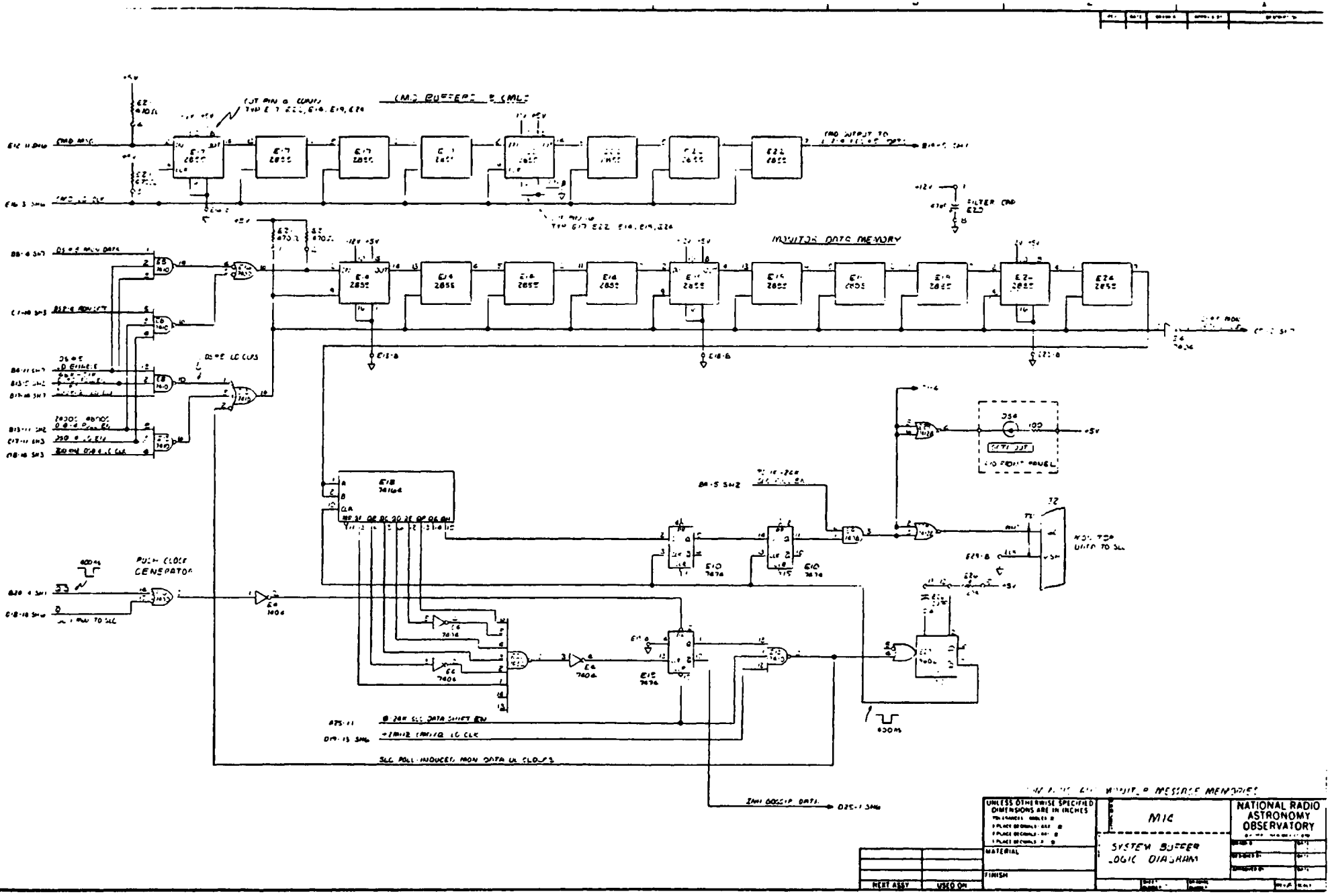


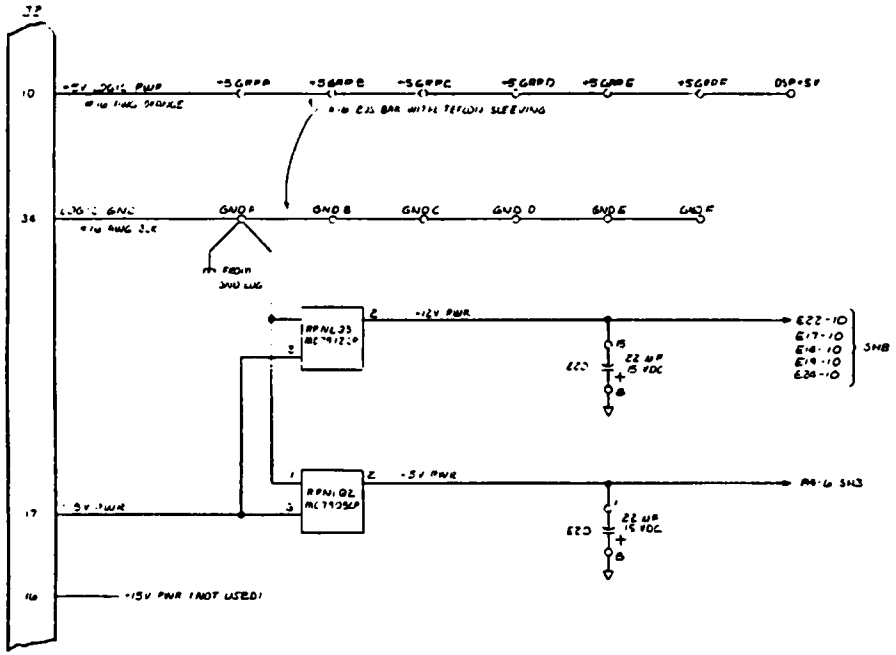
ACB ASG TO DES ADDR
DVR N LOGIC

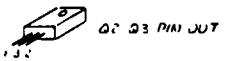




UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	M16	NATIONAL RADIO ASTRONOMY OBSERVATORY
MATERIAL	SYSTEM BUFFER LOGIC DIAGRAM	
FINISH		
NEXT ASSY / USED ON		


(M.) BUFFER & SMU
INPUT DATA MEMORY
PUSH CLOCK GENERATOR
NATIONAL RADIO ASTRONOMY OBSERVATORY
MIC
SYSTEM BUFFER LOGIC DIAGRAM





J1	TEST POINTS
1	N C
2	OGIN
3	N C
4	MONITOR DATA TO SLC
5	Q TRAIN
6	GOSSIP DATA TRAIN
7	N C
8	N C
9	10 MHZ
10	DET
11	DET CMDS
12	DET MON DS0-6
13	DET MON DS9
14	8P-30K SLC SHIFT EN
15	1P-24K SLC POLL EN
16	2P-33K DS0-6 POLL EN
17	4P-51K DS9 POLL EN
18	7P-68K CARD LOAD EN
19	L RESET
20	DS 2 OUT
21	DS 1 OUT
22	DS 2 OUT
23	DS 3 OUT
24	DS 4 OUT
25	DS 5 OUT
26	N C
27	N C
28	N C
29	N C
30	DS 0 IN
31	DS 1 IN
32	DS 2 IN
33	DS 3 IN
34	DS 4 IN
35	DS 5 IN
36	N C
37	N C

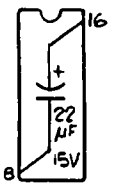
J2	
1	SMHZ OUT
2	
3	DS1 DATA
4	
5	
6	DATA TO SLC
7	
8	DATA FROM POST
9	
10	+5V LOGIC PWR
11	
12	DS1 CMD
13	
14	[illegible] CMD
15	
16	+5V PWR
17	+5V PWR
18	DS2 DATA
19	
20	DS2 CMD
21	
22	DS3 DATA
23	
24	DS3 CMD
25	
26	DS4 DATA
27	
28	DS5 DATA
29	
30	DS0 CMD
31	
32	[illegible] CMD
33	
34	+5V PWR
35	
36	DS0 DATA
37	
38	GO NO-GO
39	DATA FROM SLC
40	
41	
42	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		M14	NATIONAL RADIO ASTRONOMY OBSERVATORY
MATERIAL		SYSTEM BLOCK & LOGIC DIAGRAM	
FINISH			
NEXT ASSY	USED ON		

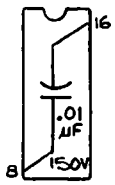
F					E					D					C					B					A				
5	4	3 CAP 1 ⊛	2	74165 –	5	4 7404	3 CAP 1 ⊛	2 74LS 163	1 7404	5 74164	4 7404	3 CAP 1 ⊛	2 7474	1 74165 –	5 74161	4	3 CAP 1 ⊛	2 7430	1 74164 –	5 7402	4 7474	3 CAP 1 ⊛	2	1	5 DH-3 ⊛	4 LM 360	3 CAP 1 ⊛	2 DH-1 ⊛	GN 137
10	9	8	7	6 7474	10 7445 74	9 7408	8 7410	7 74LS 163	6 7485	10 74164	9 7430	8 74164	7 7405	6 74165	10 74161	9 7430	8 74161	7 7404	6 74195	10 RES-1 4700Ω ⊛	9 75183 (8830)	8 7474	7 7400	6 74161	10 7474	9 74161	8 74157	7 DH-1 ⊛	GN 137
15	14	13	12	11	15 7474	14 2855	13 7410	12 7474	11 7400	15 74164	14 74175	13 7404	12 7404	11 7474	15 74160	14 7404	13 74161	12 74186	11 74165	15 7474	14 75183 (8830)	13 7474	12 7400	11 74160	15 7474	14 93L01	13 93L12	12 DH-1 ⊛	GN 137
20 DIP SWITCH	19	18	17	16	20 CAP 3 ⊛	19 2855	18 74164	17 2855	16 7400	20 7402	19 74160	18 7430	17 74161	16 74165	20 74160	19 74164	18 74160	17 7474	16 74195	20 7474	19 7400	18	17 7404	16 74160	20 74165	19 74160	18 7400	17	DH-2 ⊛
25 7447	24	23	22	21	25	24 2855	23 7430	22 2855	21 RES-1 470Ω ⊛	25 74195	24 7486	23 74160	22 74161	21 74165	25 74195	24 7486	23 74160	22 7400	21 74195	25 75182 (8812D)	24 7404	23 74S04	22 7437	21 74160	25 7474	24 74160	23 7404	22 7404	21 7437
30 7447	29 RES-1 470Ω ⊛	28 CAP 2 ⊛	27	26	30	29 74128	28 CAP 2 ⊛	27 91602	26 DH-6 ⊛	GN 137	29 DH-5 ⊛	28 CAP 2 ⊛	27 74109	26 7474	30 7410	29	28 CAP 2 ⊛	27 7404	26 74195	30 91602	29 DH-4 ⊛	28 CAP 2 ⊛	27	26 74160	30 7410	29 7410	28 CAP 2 ⊛	27 7410	26 7437

SPECIAL DIP HEADER ASSY DETAILS ⊛

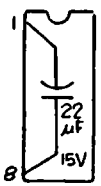
CAP-1



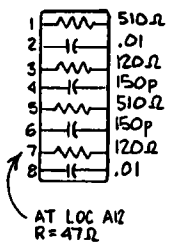
CAP-2



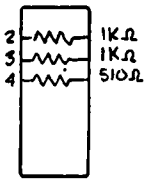
CAP-3



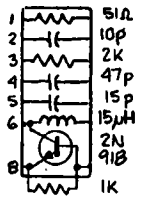
DH-1



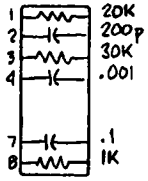
DH-2



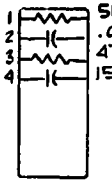
DH-3



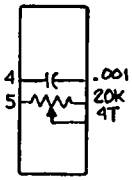
DH-4



DH-5



DH-6



DWG. A13720P

M14 SYSTEM BUFFER

LOGIC I.C. ASSY I[redacted] LOCATIONS [redacted] DETAILS

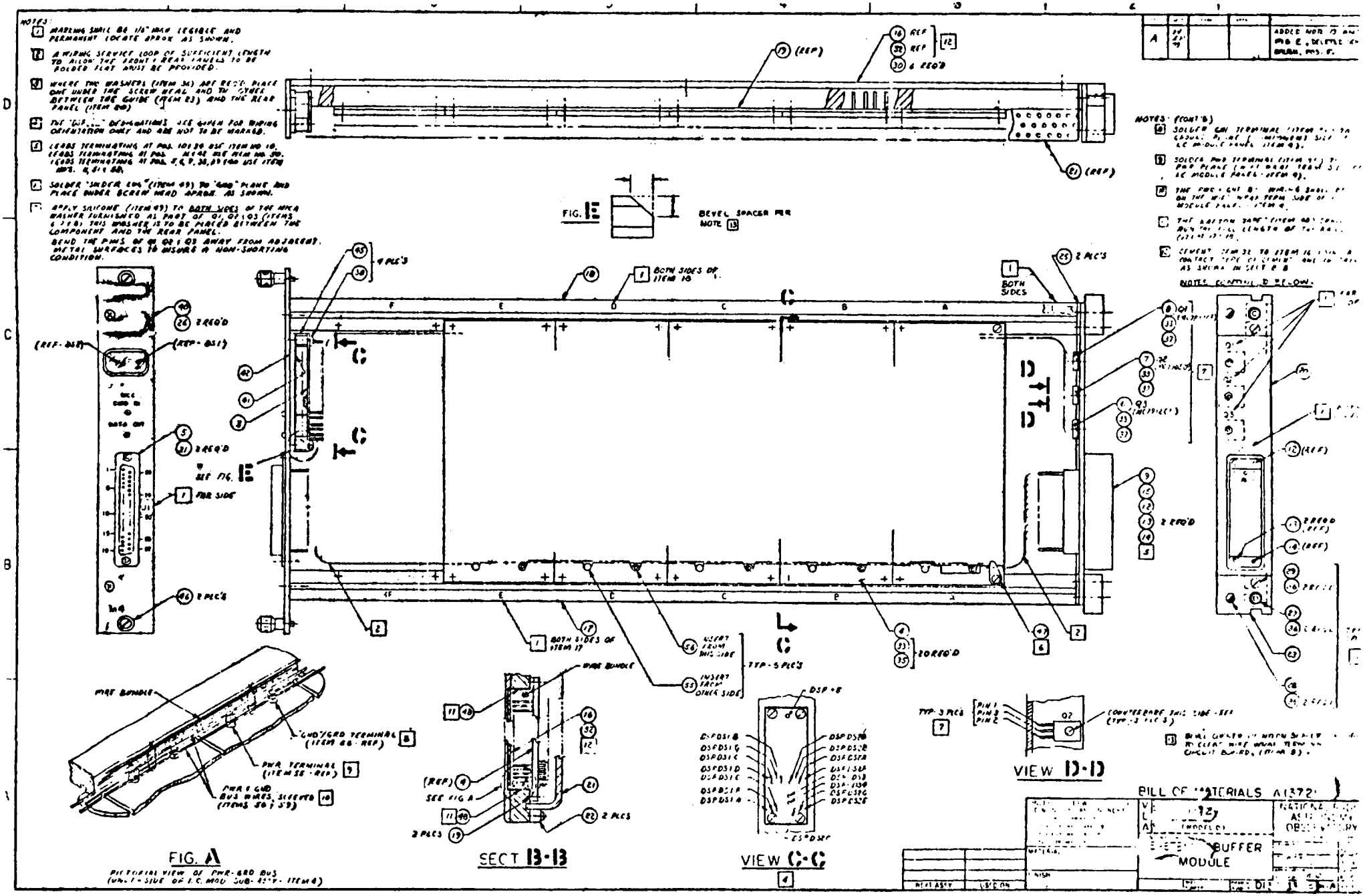


FIG. A
PICTORIAL VIEW OF PWR & GRD BUS
SECT B-B
VIEW C-C
VIEW D-D
FIG. E
BEVEL SPACER PER NOTE 13
BILL OF MATERIALS A1372
BUFFER MODULE

REVISIONS

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
				CORRECTED P/N OF ITEM 10
				CORRECTED LENGTHS OF ITEMS 26-29 AND P/N OF ITEMS 9 & 50

DRAWN BY	DATE			
DESIGNED BY	DATE			
APPROVED BY	DATE		NEXT ASSY	USED ON

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLA

PROJECT M14

TITLE SYSTEM BUFFER

DWG NO. A13721265 SHEET OF

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

[XX] ELECTRICAL [ ] MECHANICAL BOM # A13721Z65 REV B DATE _____ PAGE 1 OF 4

MODULE # M14 NAME SYSTEM BUFFER DWG # _____ SUB ASMB _____ DWG # _____

SCHEMATIC DWG # D13721L79 LOCATION _____ QUA/SYSTEM _____ PREPARED BY _____ APPROVED _____

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
1		N.R.A.O.	A13721	LOCAL BUFFER ASS'Y.		
2		N.R.A.O.	D13721P63	TOP ASSEMBLY DWG.		
3		N.R.A.O.	A13720Z27	L.E.D. DISPLAY SUB-ASS'Y.	1	
4		N.R.A.O.	A13721Z7	I.C. MODULE PANEL SUB-ASS'Y.	1	
5	J1	CINCH	DC-37S-F179	CONNECTOR, TEST JACK	1	
6	Q1	MOTOROLA	MC7912CP	VOLTAGE REG., -12V	1	
7	Q2	MOTOROLA	MC7905CP	VOLTAGE REG., -5V	1	
8	Q3	MOTOROLA	MC7812CP	VOLTAGE REG., +12V	1	
9	J2	AMP SPECIAL INDUST.	601488-4	42 PIN MOD. CONN. (WITH WIRE WRAP PINS)	1	
10		AMP SPECIAL INDUST.	204219-1	CRIMP PIN	2	
11		AMP SPECIAL INDUST.	201143-5	COAX CONN.	6	
12		AMP SPECIAL INDUST.	200833-4	GUIDE PIN	1	
13		AMP SPECIAL INDUST.	203964-6	GUIDE SOCKET	2	
14		AMP SPECIAL INDUST.	202514-1	GROUND GUIDE PIN	1	
15		AMP SPECIAL INDUST.	202394-2	CONN. SHIELD	2	

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

[ ] ELECTRICAL [XX] MECHANICAL BOM # A13721765 REV B DATE _____ PAGE 2 OF 4

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
16		N.R.A.O.	C13720M50	SIDE PLATE	1	
17		N.R.A.O.	C13720M15-1	RAIL, MODIFIED	1	
18		N.R.A.O.	C13720M15-2	RAIL, MODIFIED	1	
19		N.R.A.O.	C13720M17	RAIL, SPACER	2	
20		N.R.A.O.	C13720M23	REAR PANEL	1	
21		N.R.A.O.	C13050M7	PERFORATED COVER	1	
22		N.R.A.O.	B13050M17	COVER MT'G. HDWRE.	a	
23		N.R.A.O.	B13050M4	GUIDE	2	
24						
25		N. R. A. O.	B13720M47	SPACER	2	
26			#6-32 x 7/16"	ST. ST'L., CR. REC., FLT. HD. MACH. SCR	2	
27			#6-32 x 5/8"	ST. ST'L., HEX SOC. HD. CAP SCR.	2	
28			#6-32 x 5/8"	ST. ST'L., PAN HD., SLOTTED, MACH. SCR.	2	
29			#6-32 x 1-1/8"	ST. ST'L., PAN HD., SLOTTED, MACH. SCR.	2	
30			#6-32 x 1/4in	ST. ST'L., FLT. HD., SLOTTED, MACH. SCR.	6	
31		CINCH	D20418-2	SCREW LOCK ASS'Y. (FEMALE)	2	
32		N.R.A.O	B13720M49	PANEL, SIDE, INSULATION	1	

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☒ MECHANICAL BOM # A13721765 REV B DATE _____ PAGE 3 OF 4

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
33			#4-40x3/8 in	ST. ST'L., PAN HD., SLOTTED, MACH. SCR.	24	
34						
35			#4 NOM.	ST. ST'L. INT. TOOTH LK. WASHER	24	
36			# 6	WASHER, EXT. TOOTH, ST. ST'L.	12	
37			#4-40	NUT, HEX, SELF LKG., (NYLON)	3	
38			#4-40x1/4 in	NYLON, PAN HD. SLOTTED SCR.	4	
39		N.R.A.O.	C13720M16	FRONT PANEL (MACHINED)	REF	
40		N.R.A.O.	B13720M20	FRONT PANEL (ENGRAVED)	1	
41		N.R.A.O.	B13720M18-1	FRONT PANEL FILTER (RED)	1	
42		N.R.A.O.	B13720M18-2	FRONT PANEL FILTER (CLR.)	1	
43						
44		PEM FASTENERS	FHS-440-6	THREADED STUD	4	
45		AMATOM	8212-N-0440	THREADED STANDOFF 4-40 NYLON 5/16 lg.	4	
46		SOUTHCO	47-10-204-10	CAPTIVE SCREW	2	
47		G.C. ELECTRONICS	5706-C	GROUND LUG	1	
48		CONN. HARD RUBBER CO.	TYPE K350	KAPTON TEMP-R-TAPE (32/64" WIDE)	18"	
49		G.E.	INSULGREASE G641	SILICONE DIELECTRIC COMPOUND	A/R	

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☒ MECHANICAL BOM # A13721265 REV B DATE _____ PAGE 4 OF 4

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA
50		AMP SPECIAL INDUST.	P76-0001-4142	PIN, WW	2
51		AMP SPECIAL INDUST.	328666	FERRULE	6
52		AMP SPECIAL INDUST.	201142-2	RETENTION SPRING	6
55		H. H. SMITH	2010	TERMINAL (SPLIT LUG)	6
56		H. H. SMITH	2025	TERMINAL (MIN. THROUGH)	6
58		ALPHA	286	BUS BAR, TINNED COPPER (14 AWG)	A/R
59		ALPHA	TFT-200/13 (NAT)	TEFLON EXTRUDED TUBING	A/R
					–
					–
					–
					–
					–