VLA Technical Report No 62

The Command Simulator, Module Type M5

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1.0 INTRODUCTION

This manual describes the theory of operation of the Command Simulator (CS), module type M5, and was written to serve as the trouble-shooting and maintainence guide for this component of the Monitor and Control (M&C) System.

The Command Simulator is a module which permits any command register in the VLA antennas to be manually commanded for test or diagnostic purposes. In operation, the normal command signal connection between the Antenna LO Receiver and the Antenna Buffer is broken and a substitute command message is injected into the Antenna Buffer. The Antenna Buffer then emits the substituted message to the Antenna Data Sets and the addressed Data Set then executes the command in accordance with the message address and argument components. In execution, the Data Set loads the addressed register with the command argument.

Simple single-argument single-shot or recurrent commands may be directed at any Antenna command address (or device) and the response of the commanded device may be monitored on a Data Tap. In most cases these simple commands provide an adequate indication that control logic is operating properly. Since the command argument is the setting of the front panel thumbwheel switches, it is not possible to alter the argument (such as incrementing the value each machine cycle) on a dynamic basis. In the recurent mode the Command Simulator causes the addressed Data Set to repetitively output strobes, clocks and addresses to stimulate control logic; these changing signals can be useful for trouble-shooting.

A secondary objective of this manual is to provide operating instructions for those who wish to use the Command Simulator to exercise command functions at the Antenna.

To put the Command Simulator into the system context, the reader is referred to the manual: "An Overview of the Monitor and Control System", Electronics Memorandum No 44. The manual "The Antenna Buffer, Module Type M4", Electronics Memorandum No 59. provides a detailed description of the command message signal requirenents imposed by the Antenna Buffer. Figure 1 depicts the Monitor and Control System and the relationshiop of the Command Simulator to the the balance of the system. Figures 2 and 3 depict the Monitor and Control System timing relationships. Figure 4 depicts the message format.

The emphasis of this manual is upon the functional details; the writer's intent is to provide a thorough description of the Command Simulator's theory of operation. Straight-forward areas are treated briefly, more complex areas are fully explained and the explanations are augmented by timing diagrams. Using this manual as a reference, a digital maintainence technician should be able to quickly identify and repair malfunctions.

2.0 COMMAND SIMULATOR DESCRIPTION

The primary function of the Command Simulator is described above; a secondary mode is to permit an Antenna Maintainence Computer to be connected to the front panel. This permits the computer to control and monitor Antenna functions for maintainence and alignment purposes.

Another secondary mode of the CS is to use it with a Data Set and Data Tap as a stand-alone Monitor and Control System.

The Command Simulator is a 4-wide module located in Bin Q in the B (Local Oscillator) rack in the Antenna Vertex Room. Wire-wrapped logic connector boards contain the logic elemants.

2.1 COMMAND SIMULATOR CONTROLS AND DISPLAYS

The front panel controls (see Figure 5) are quite simple; octal thumbwheel switches are set to DCS Address, Data Set Address, Multiplex Address and command argument values. A 24 bit, discrete LED display shows hexadecimal groupings of the octal command arguments; some of the VLA command arguments are a composite of octal, hexadecimal and discrete bits; this dual-mode display is helpful in these cases. Obviously the operator must know the address and argument details of the devices that he wishes to test.

Actuating the momentary CMD SIM/COMP switch in the up position sets the CS into operation and causes the red SIM ACTIVE LED to blink at about a 1 Hz rate to indicate that the Command Simulator is the command message source; red LEDs indicate an abnormal mode of the Monitor and Control System. Actuating the switch down causes M&C system command message control to revert to the control computers.

A three position, SINGLE command (momentary down), OFF (center position), RECURRENT (sustained up) switch causes single-shot, quiescent state (ie no commands) or recurrent commands (respectively) to be loaded into the Antenna Buffer when the CMD SIM/COMP switch is in the CMD SIM position.

LED activity indicators indicate the signal activity of the Command Simulator output, LO Receiver command output and the Antenna Buffer output. These provide some assurance that these devices are active and may be useful in diagnosing problems in the Antenna.

Time-out logic causes the CS to revert to the COMP mode after about a 30 minute period of operation; a brief Bronx Cheer from an internal beeper warns the operator that the CS is about to revert to the COMP mode and a second Bronx Cheer signals that it has happened.

2.2 COMMAND SIMULATOR I/O SIGNALS

- QQ Pulse, - a 400 ns differential TTL level signal from L8 which

signals the start of the 1000 usec period in which command messages are transmitted from the Central Buffer via the Central LO/WG Transmission systems. The QQ pulse is jumpered to the front panel connector to permit the Antenna Maintainence Computer to be time-synchronized to L8.

- Command Input from the LO Receiver, - a bipolar 1 volt peak, 500 Khz BI-0 signal from the LO Receiver.

- Command Output to the Antenna Buffer, - a bipolar 1 volt peak, 500 Khz BI-0 signal to the Antenna Buffer input.

- External BI-0 Command Output, - the signal above, wired to the front panel connector to permit the Antenna Maintainence Computer to inject command messages into the Antenna Buffer.

- Antenna Buffer Monitor Data Output - a tap onto the Antenna Buffer monitor data output line. This TTL level signal is also wired to the front panel connector to permit the Antenna Maintainence Computer access to the monitor data stream. This signal is jumpered <u>through</u> the Command Simulator; if the Command Simulator is removed the command path between the LO Receiver and the Antenna Buffer is broken.

- B Rack 5 Mhz Output, - the B Rack 5 Mhz M&C system clock which is jumpered to the front panel connector to clock the Antenna Maintainence Computer.

- Data Set CMD/Q/Mon Output, a high true, TTL level composite signal consisting of the Q character, Command Simulator BI-0 command and Data Set monitor data. The Q permits the Command Simulator to poll data from a Data Set when the pair are used as a stand-alone data system.

- Clock Select, - a ground on this line causes the command message clock rate to be 200 Khz for use with a Data Set. If left floating the clock rate is 500 Khz which is the Antenna Buffer clock rate.

- Data Set Data Input, - an optically isolated (in the CS) monitor data input from a Data Set when used in a stand-alone system.

- 5 Mhz to the Data Set, - a 5 Mhz output to clock a Data Set

- Data Set Data to an External Unit, - a low true, TTL level Data Set Data output to the Antenna Maintainence Computer.

- 10 Mhz To External Unit, a TTL level, differential signal to the Antenna Maintainence Computer.

- Antenna Buffer Signal Format Sense, - a pull-up resistor to +5 to signal to the Antenna Maintainence computer that it is connected to the Command Simulator.

2.3 MESSAGE FORMAT DESCRIPTION

Figure 4 depicts the format of the Command and Monitor Data messages and the "Q" (for Query) character format. The messages are prefixed by an "S" (for Start) character which signals that a message immediately follows. The bit rate of the S character is twice the bit rate of the data bits to make this character unique. The message consists of five 8-bit data bytes; the first byte contains a 5 bit DCS Address (which can range from 0 to 37, octal) and a 3 bit Data Set Address which can range from 0 to 7. The second byte is the Multiplex address which designates a particular command or data channel. The third, fourth and fifth bytes are components of a 24 bit command or monitor data argument. In the case of an analog data message, the 24 bit argument consists of two 12 bit values resulting from the conversion of two analog signals by the Data Set analog to digital converter. In all address and argument values the first bit (in time) is the most significant bit. This format description is general, in the context of the Command Simulator, only command messages are formulated and these have an address range of 300 to 377 (octal).

The M&C messages transmitted through the LO/WG Transmission System have a different format than the simple NRZ described above; the bit sense is conveyed by the phase of a 500 Khz phase-modulated carrier. This form of modulation is called BI-0-L (L for level, also called Manchester encoding); a modulator in the Central and Antenna Buffer's output circuitry inverts the phase of the 500 Khz carrier for each data one bit; a zero bit does not change the phase. This encoding scheme provides a signal edge for every bit space, a very desireable property for situations in which receiving logic must derive a clock from the structure of time-serial digital messages. The Antenna Buffer command messages have a data rate of 1 usec/bit for the S character bits and 2 usec/bit for the message data bits; the Command Simulator has a BI-0 modulator in the output circuitry to generate this signal format.

3.0 DETAILED CIRCUIT DESCRIPTION

The Command Simulator is the simplest on-line component of the Monitor and Control System but there are some details which deserve explanation; the theory of operation follows:

3.1 TIME BASE AND TIMING DISCRETES

The time base is clocked by the internal 10 Mhz crystal oscillator A0510 with a TTL level output (see Sheet 1). The string of synchronous counters A4 through A29 are clocked by this 10 Mhz clock to provide timing terms to control the CS operation. The time base is cleared (ie count set to zero) by the QQ pulse from the L8 module. The QQ pulse signals the start of the VLA machine cycle; the first 1000 usec are dedicated to transmission of commands to the Antenna Buffer from the Central Buffer. This 1000 usec period is the period in which the CS performs it's appointed function; during the balance of the 52,083.3 usec period the CS is quiescent.

The QQ pulse is a differential signal; A0106 is a differential receiver which has a low-true output (if the input polarity is correct) which clears the time base counters through or-gate A1303 and one-shots B11. B1109 stretches the 400 ns QQ to a 1 usec period to permit the parity decision to settle (more about this later). B1109 drives the power buffer A0203 which clears the time base through the asynchronous clears. If the CS is used in a stand alone mode with a Data Set, the time base is reset at 54,200 usec, a period slightly longer than the VLA machine cycle period. This reset is accomplished by gate A0806 which decodes the appropriate terms.

Flip flop A1511 generates a 0 to 1000 usec control discrete which enables the command output logic.

Counter A10 generates a 200 Khz clock used for Data Set applications and the toggling flip flop B04 generates a 500 Khz clock for Antenna Buffer Bi-0 format commands.

3.2 COMMAND REGISTER

The command register (Sheet 2) consists of the address and argument thumbwheel switches; this is the command memory and it is loaded into the output register at the beginning of the VLA cycle by one-shot B11 which is triggered by the QQ pulse. The command register outputs are low-true. The command argument portion of the thumbwheel switches also sink current for the argument LED display.

3.3 OUTPUT REGISTER

The output register consists of the string of shift registers C5 through C20. Parity bit flip flops C8, C13 and C18 are interposed between the register baytes and are set to the appropriate state by parallel parity generators C4, C9, C14, C19 and C24. You will note one unusual feature; the output register serial output is taken off the Qh low-true output of C25, why? The answer is that the register is loaded with low-true bits from the Command Register, the Qh low true output inverts the low-true data stream to high-true form where it is fed into the S generator shift register C30, C18 and C23. The output of C23 is a high true command NRZ message stream that is converted to BI-0 format to drive the Antenna Buffer. The details of the BI-0 modulator are discussed below. The NRZ format output is used to drive the Data Set.

As the Output Register is unloaded, a continuous high is fed into the LSB input of the register; this fills it with zeros so that after the command has been unloaded zero bits continue to be output from the register until the end of the 1000 usec command period.

3.4 OUTPUT REGISTER LOADING

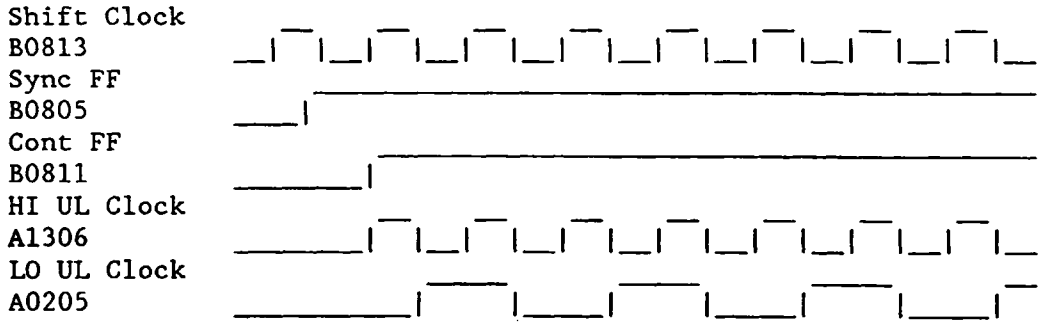
The LOAD CMD term from A0203 strobes the nand gates C0203, C0206,

C0210, C0213 and B1503 to set the parity bit flip flops. The QQ pulse is stretched by one shot B1109 to provide plenty of settling time for the parity generators to settle and set the parity bit flip flops.

3.5 OUTPUT REGISTER UNLOADING

Two different shift clocks are required for the address/argument and S generator portions of the Output Register because the S bit periods are half the data bit periods. These shift clocks are generated by flip flops B0811 and B1305. B0811 and B1305 are initialzed by the RESET from A0203 and held quiescent by the low output of flip flop B0805. When B0805 goes true as a result of the start of a command message output (discussed later), B0811 is clocked on by the next clock. B0811 enables gate A1306 to output the HIGH UL Clock which drives the S generator portion of the Output Register. The falling edge of the HIGH UL CLOCK toggles flip flop B1305 to generate the LO UL CLOCK. The initialization of the flip flops causes the phasing of these two clocks to be such that the higher rate clock causes the S Generator shift register to sample the address/argument register output between the low speed shift clocks; this avoids race conditions which could occur when two clocks are used on a serial shift register. The simplified timing diagram below illustrates the operation of this logic.

UNLOAD CLOCK TIMING



The explanation above describes the unload clocking logic; we will now consider how this action is initiated. Synchronizing manual control switches to active logic requires that the asynchronous switch actuation be properly time-synchronized with the logic operation. There are two cases; 1) recurrent command output (ie once per VLA cycle); 2) single-shot command output (once per switch actuation).

In the recurrent mode switch S1 holds flip flop B10 set. B1011 output through or-gate A1203 enables gate A1310; this permits flip flop B1005 to clock control flip flop B0805 to permit the B0813 unload clock logic to function. B1005 is clocked on by the 200 usec term from the time base; this delays the command output by 200 usec, well into the period in which the Antenna Buffer is permitted to listen for command signals (the LO Receiver has a bad switching transient which lasts for over 50 usec after the start of the 1000 usec period).

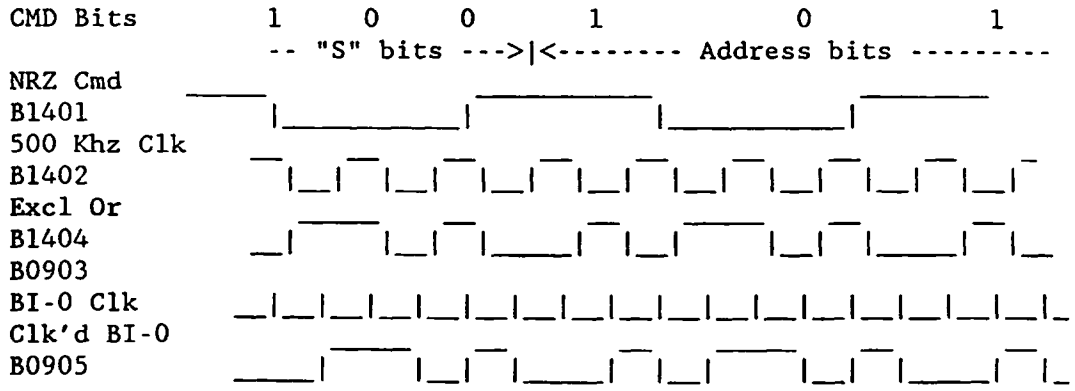
In the single-shot mode, manual (momentary) actuation of switch S1 to the Single position triggers one-shot C2906, (a long period); when the 0 to 1000 term on B0711 goes true, flip flop B0911 is set which then initiates a command output sequence through or-gate A1203 in the same manner as in the recurrent mode described above. Flip flop B0911 and one-shot C2906 are cleared by the RESET term at the start of the next cycle; additional command message outputs must be initiated by additional actuations of switch S1.

The unload clock rate is selected by and-or gate B22, a ground on I/O connector P1-1 selects 200 Khz as a clock rate; this is the selection appropriate for using the CS with a Data Set.

3.6 OUTPUT SIGNAL CONDITIONING

The NRZ command from the Output Register is BI-0 modulated by exclusive or gate B1403 and is clocked into flip flop B0905 by the 1Mhz term .8 usec from counter A14. This term is skewed in time relative to the 500 Khz clock to avoid edge effects in sampling B1403. The reason that the BI-0 signal is clocked into a flip flop is that this insures a 50% duty cycle on the BI-0 output. The simplified timing of the BI-0 modulator is depicted below.

BI-0 MODULATOR TIMING



The BI-0 signal is conditioned by the low pass filter A11 and a portion is picked of by potentiometer A11/1/2/3. The pot output is fed into inverting wide band op amp A6 which outputs a 1 volt peak signal to the output switches A22. Capacitor A1106/11 causes the amplifier high frequency respone to roll off; this amplifier should be set up with an appropriate piece of cable and terminating load; observe the amplifier output on a oscilloscope.

3.7 SIMULATOR/COMPUTER MODE CONTROL

B1311 is the mode control flip flop. Actuating S2 to the SIM position permits the CS to inject command messages into the Antenna Buffer. A power reset on the clear input of B1311 causes it to come up

in the Computer mode when the rack power is switched on.

Two solid state switches A22 and A27 connect the CS output or the LO Receiver BI-0 command message signals to the Antenna Buffer command input. Three modes exist which are controlled by a combination of the mode control flip flop B1311 (Sheet 1) and and external grounding term on the front panel connector J2-35. The mode control flip flop B1311 controls the selection of the CS or the LO Receiver as the command source. The switches A22 and A27 are controlled by a low-true enable, when the CS is inactive the LO Receiver output is routed through A27 to the Antenna Buffer command input; when the CS is active the CS output is routed through switch A22. In both cases the other command source is disconnected because the switches have a high off impedance. When the Antenna Maintainence Computer is connected to the CS, gates B18 and inverter C7 permit the computer to pre-empt control by disconnecting both switches; the computer can inject command signals without interference from either the CS or LO Receiver.

Two switch sections of A22 and A27 are paralleled to provide a lower on impedance since the Antenna Buffer input impedance is a few hundred ohms.

3.8 ACTIVITY SENSORS

The front panel LEDs CS Active, Mon Active and LO Cmd Active LEDs are driven by one-shots B2909, B2907 and C2707. These long period one shots are triggered by actively switching inputs. The CS Active one-shot is triggered by A0810 which switches only when the CS is active. The Mon Active is triggered by the antenna monitor data output of the Antenna buffer, if it is not lit there is probably no monitor data coming out of the Antenna Buffer. The LO Cmd Active indicates that the LO Receiver output is active; if this LED is not lit something is busted in the command signal path.

3.9 TIME-OUT LOGIC

Counter B20 is a 14 stage CMOS counter that is clocked one count per VLA cycle by the 40 K term from the time base. The red Sim Active LED is driven by the Q5 stage of B20 to indicate that the CS is in the active mode. The Q13 output of B20 clocks counter B24, at the count of 7 in B24, one-shot C2709 fires for a few hundred ms which causes the beeper driven by A0207 to emit a Bronx Cheer. This signals that time out is imminent. At the count of 8 in B24 the mode control flip flop B1311 is clocked reset and the rise of B1310 triggers one shot B2507 which causes the beeper to issue another Bronx Cheer to signal that the CS has reverted to the Computer (normal) mode.

3.10 DATA SET MODE

The CS may be used with a Data Set and Data Tap to implement a rudimentary command/monitor system. When the 200 Khz clock rate is selected (discussed above) the Output Register is clocked at a rate

appropriate for the Data Set and the CS emits Q characters that evoke monitor data messages from the Data Set in the same manner as the Antenna, Central and System Buffers.

In this mode, commands are output as described above and a Data Set connected to J1-32/32 will execute the commands. The CS will operate on a periodic cycle rate slightly longer than the standard 19.2 Hz because of the recycle logic described in the time base logic above. Timing terms in the gates connected to flip flops B2 cause Qs to be output by the Q generator B1 and B4 at 16,000 and 20,000 usec. These are output by the or-gate B0614 to the Data Set command/Q/Monitor Data input via J1-32/33. The Data Set Data monitor data output is connected to J1-22/23 which drives optical isolator A0614; the isolator maintains ground isolation between the Data Set and CS.

The CS provides a 5 Mhz AC coupled clock on J1-25/26 for the Data Set logic.

4.0 LIST OF MAJOR DRAWINGS

Major Functional Drawings

D13721P42	Command Simulator Top Assembly Drawing
A13721Z59	Command Simulator Top BOM
D13720L59	Command Simulator Logic Diagram
A13721P43	IC Location Map

Mechanical and Fabrication Drawings

D13720M97	Front Panel Fabrication Dwg
D13720M98	Front Panel Marking
C13720M80	Rear Panel Fabrication Dwg
C13720M17	Insulated Spacer
C13720M15	Module Rails, Modified
B13720M49	Side Plate Insulation
C13720M50	Side Plate, Modified
C13720P68	Side Plate Ass'y
B13050M04	Guide Block
C13720AB34	Front Panel LED Display PCB Artwork
C13721P44	Front Panel LED Display Ass'y
C13720M89	Front Panel LED Display Drill Dwg
A13721Z60	LED Display Ass'y BOM
B13720M96	Plexiglass Cover Detail
C13720AA37	Plexiglass Cover SS Artwork
B13720AA31	Front Panel SS Artwork
B13720M47	Module Bar Spacer

Wiring Drawings

C13720M32	DCS Module WW Field Dim Definitions
D13720M94	Cmd Sim Wiring Jig Configuration and Harness
D13720M95	Wiring Jig
A13720W82	Master Wire List
A13720W83	Machine Wire List
A13720W84	Hand Wire List
A13720W85	Connector Wire List

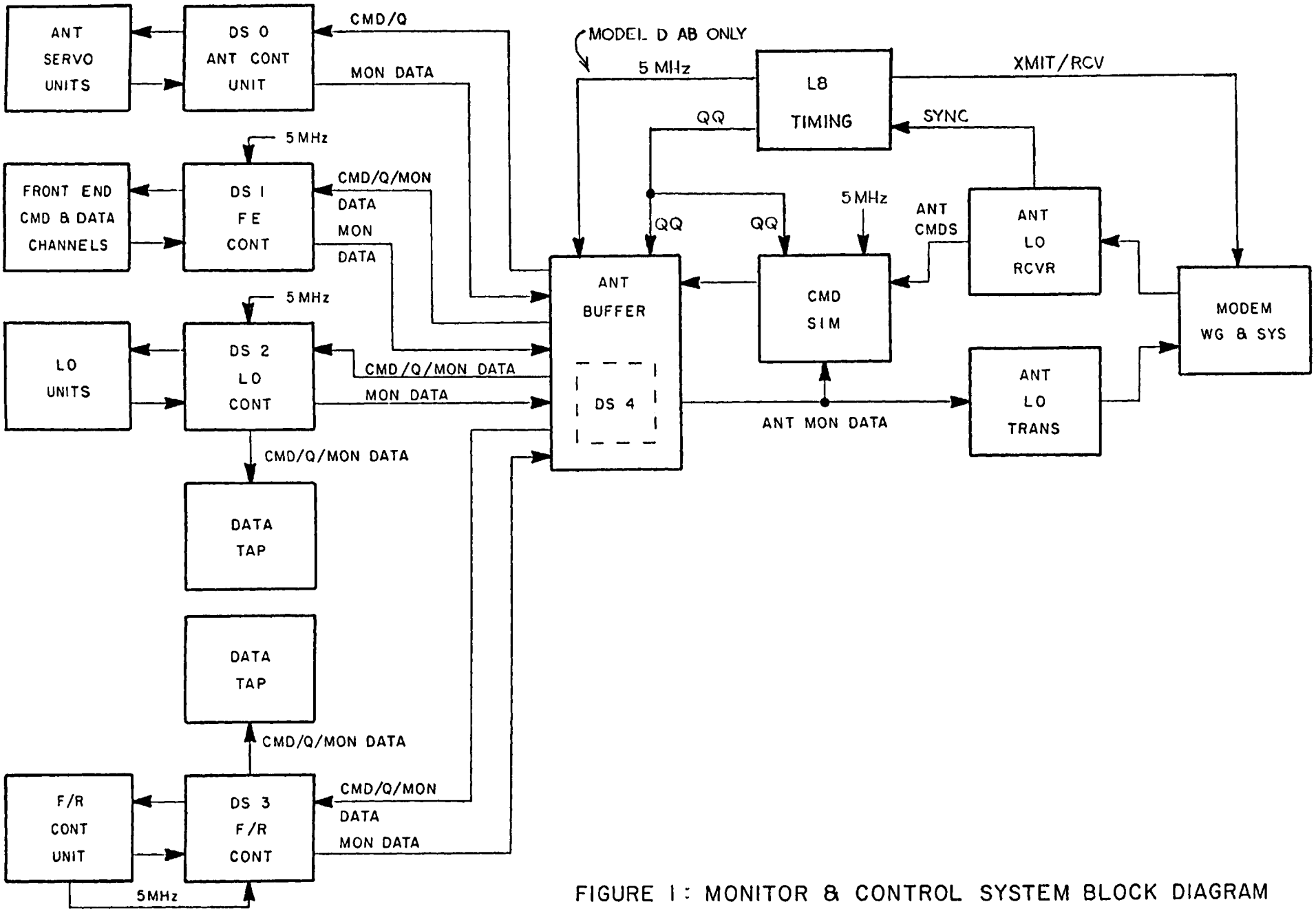


FIGURE 1: MONITOR & CONTROL SYSTEM BLOCK DIAGRAM

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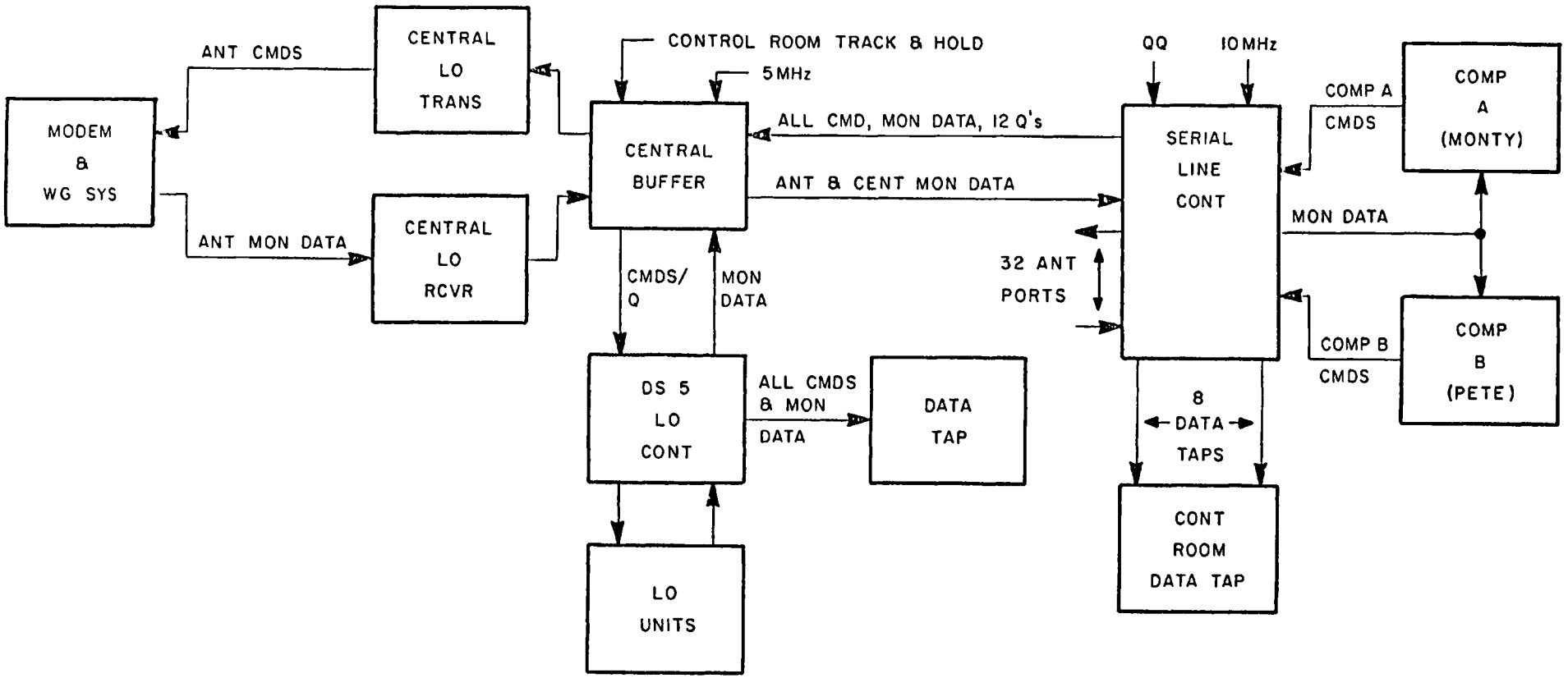


FIGURE 1: CONTINUED

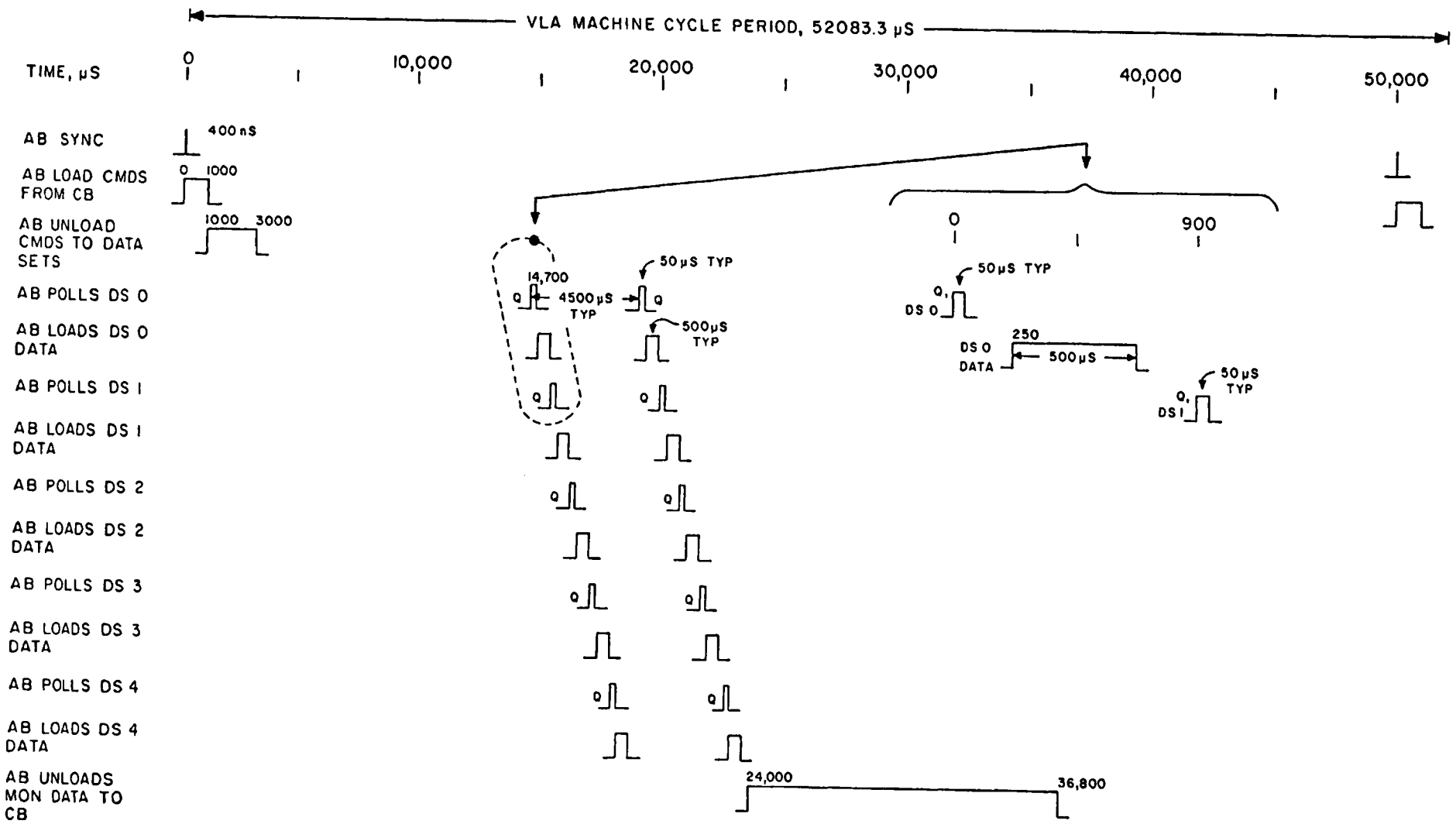


FIG. 2
ANTENNA TIMING OPERATIONS

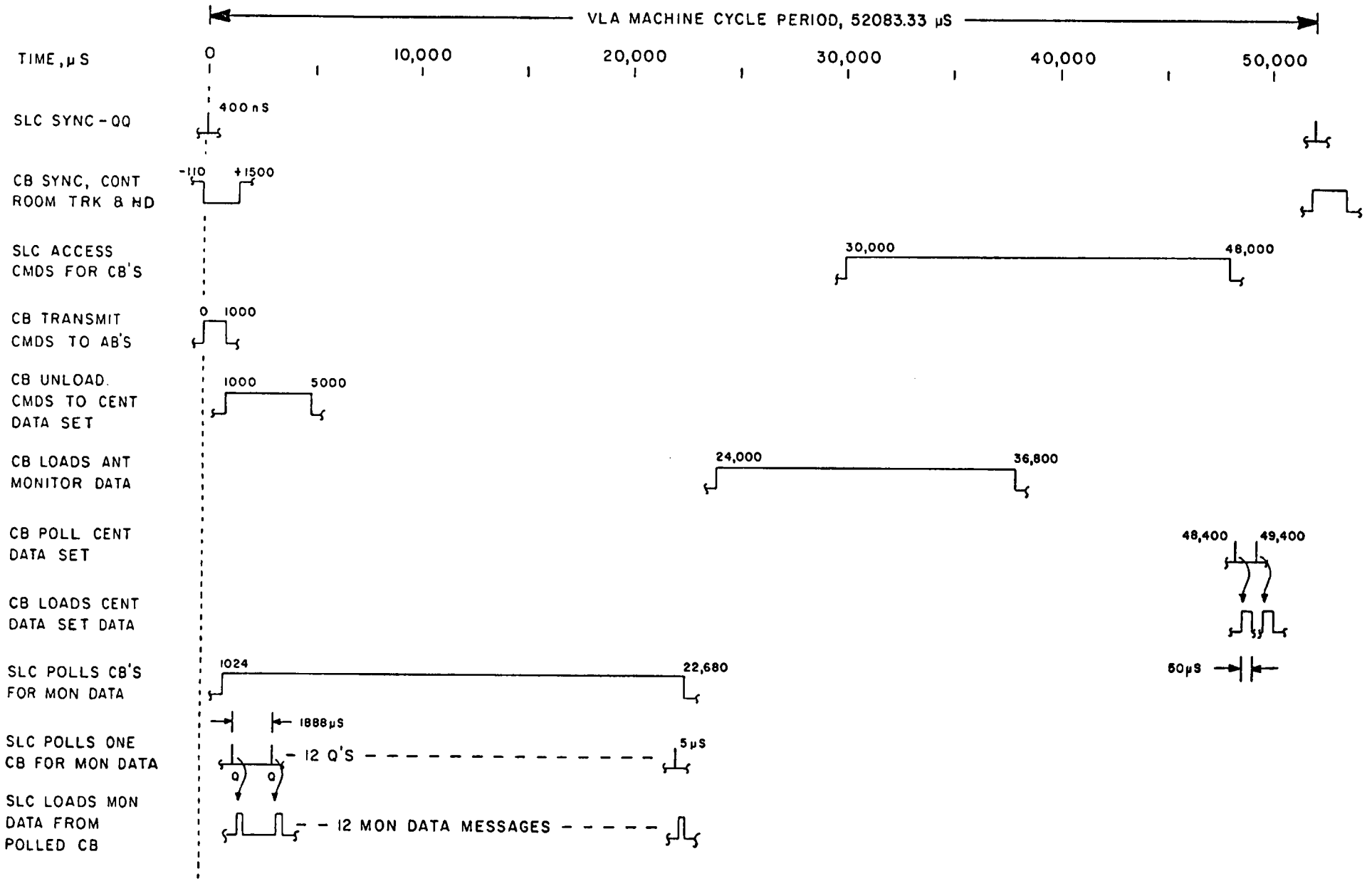


FIG. 3
CENTRAL TIMING OPERATIONS

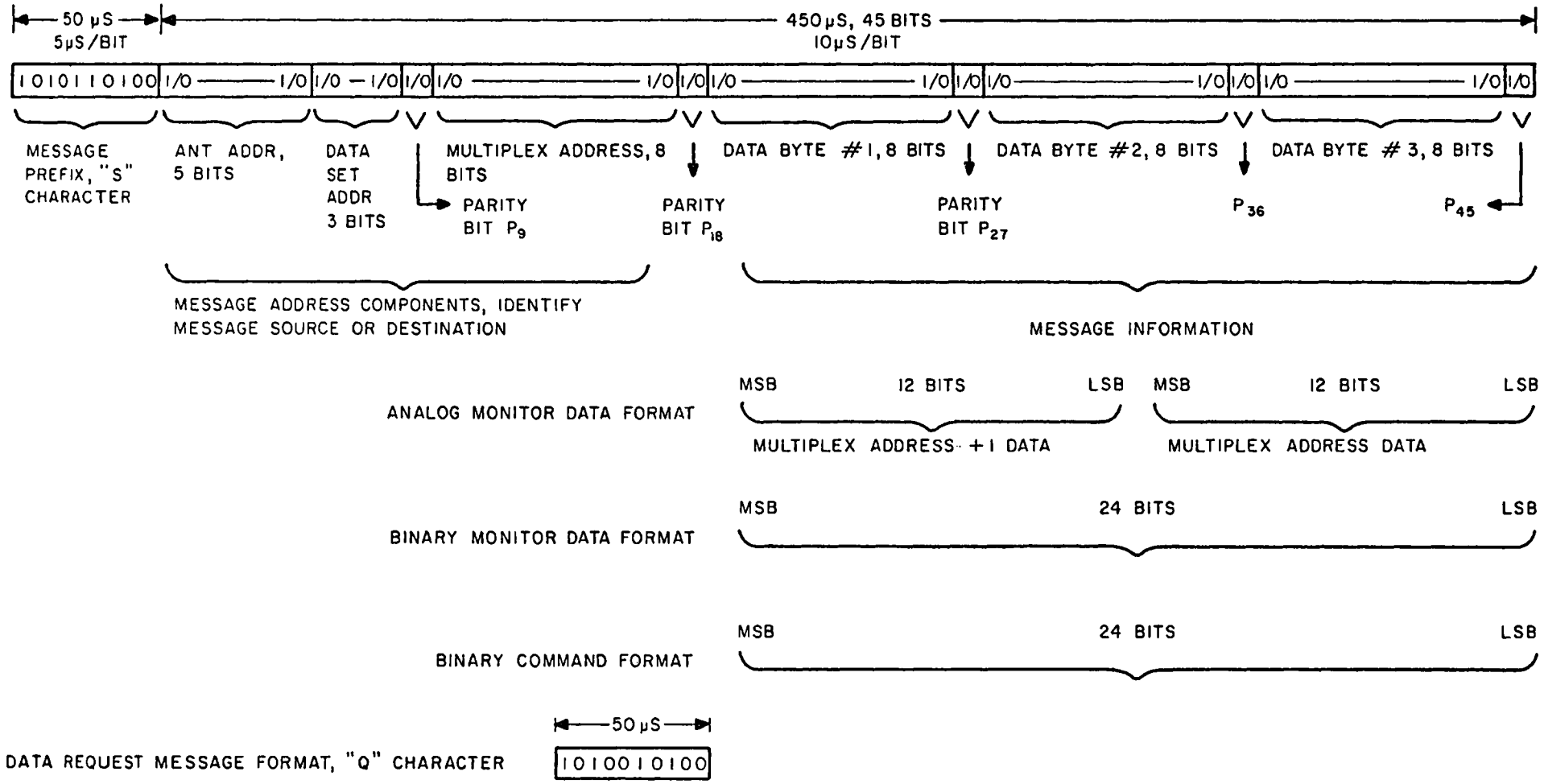


FIGURE 4: DATA SET COMMAND AND MONITOR DATA AND DATA REQUEST MESSAGE FORMATS

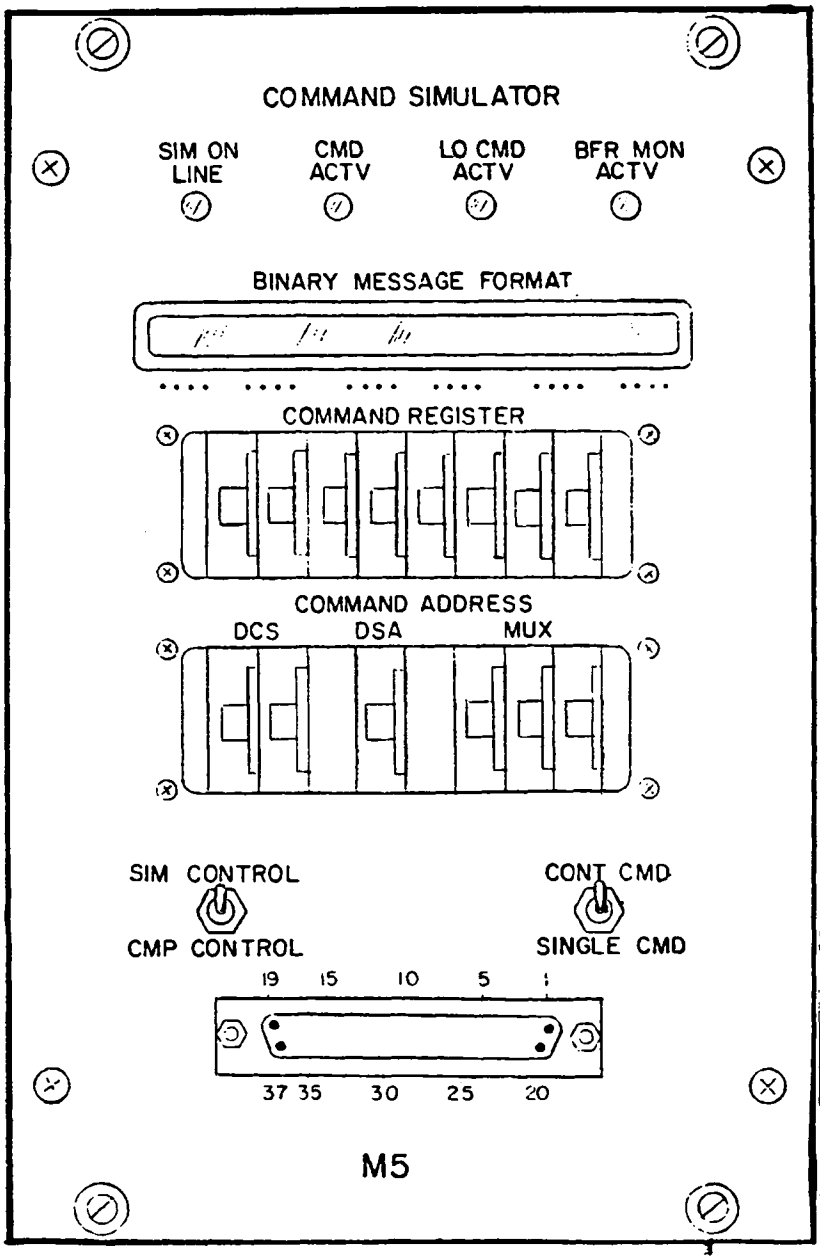


FIG. 5 FRONT PANEL - Controls and Indicators

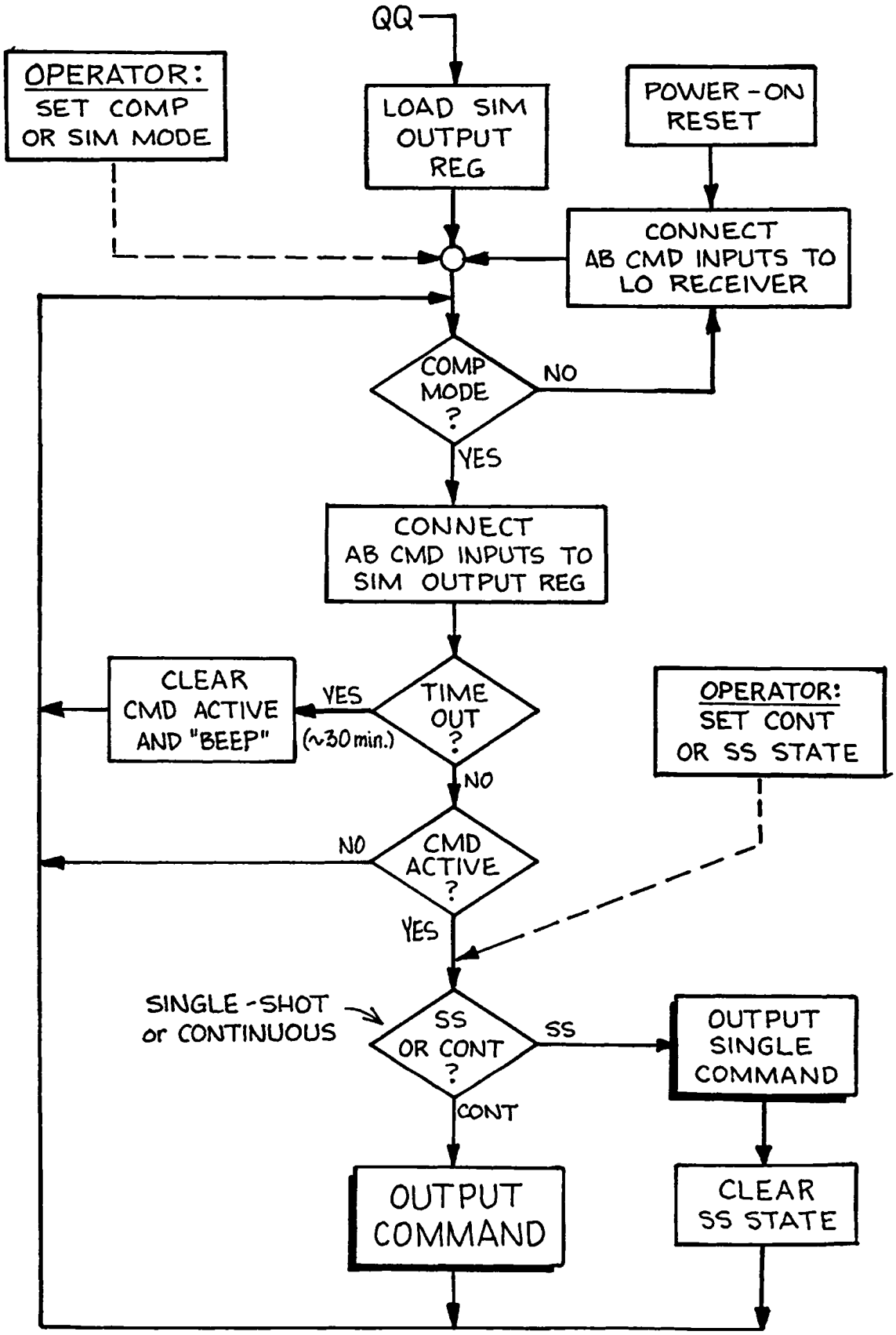


FIG. 6: Command Simulator Logic Flow Diagram

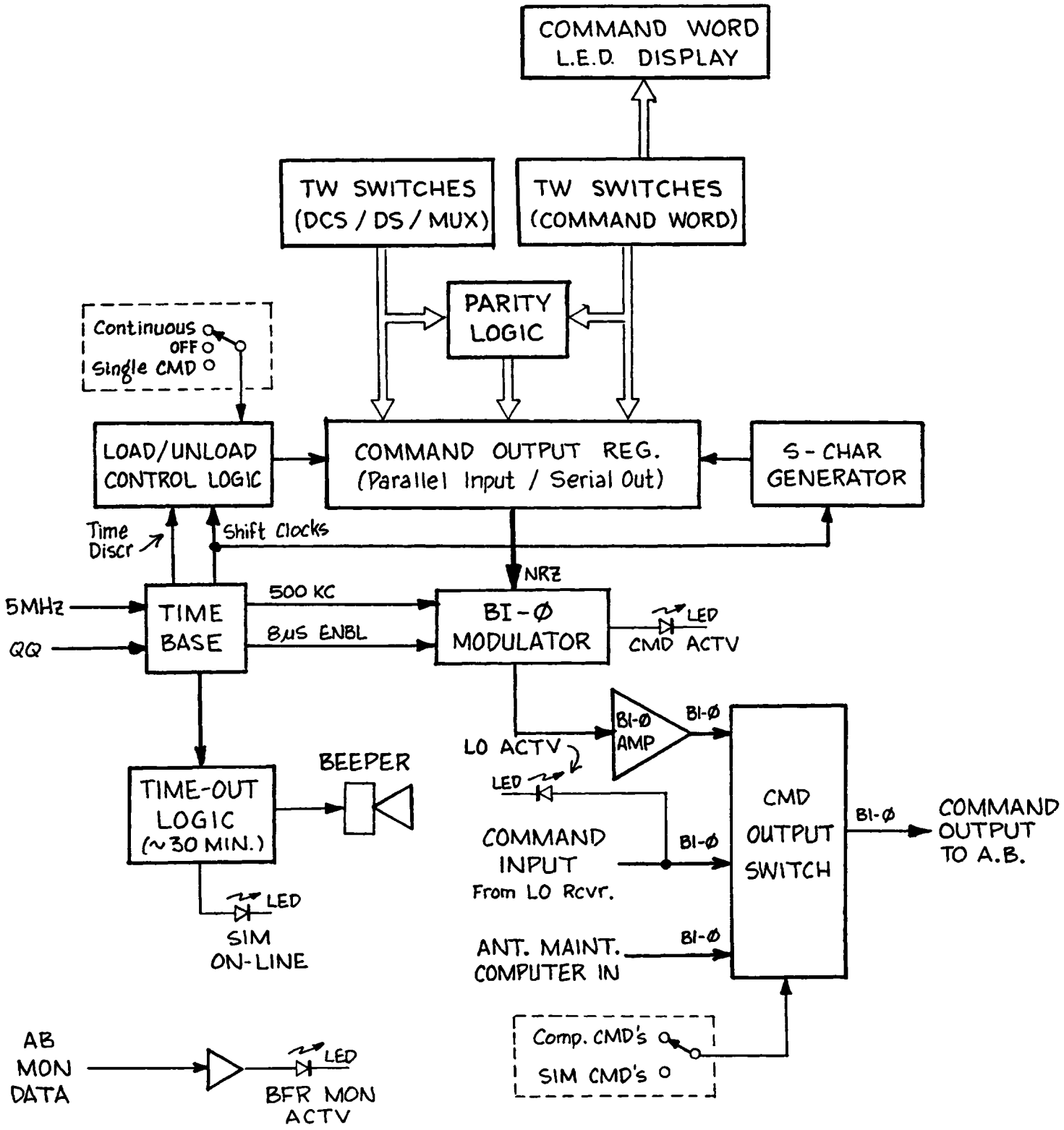
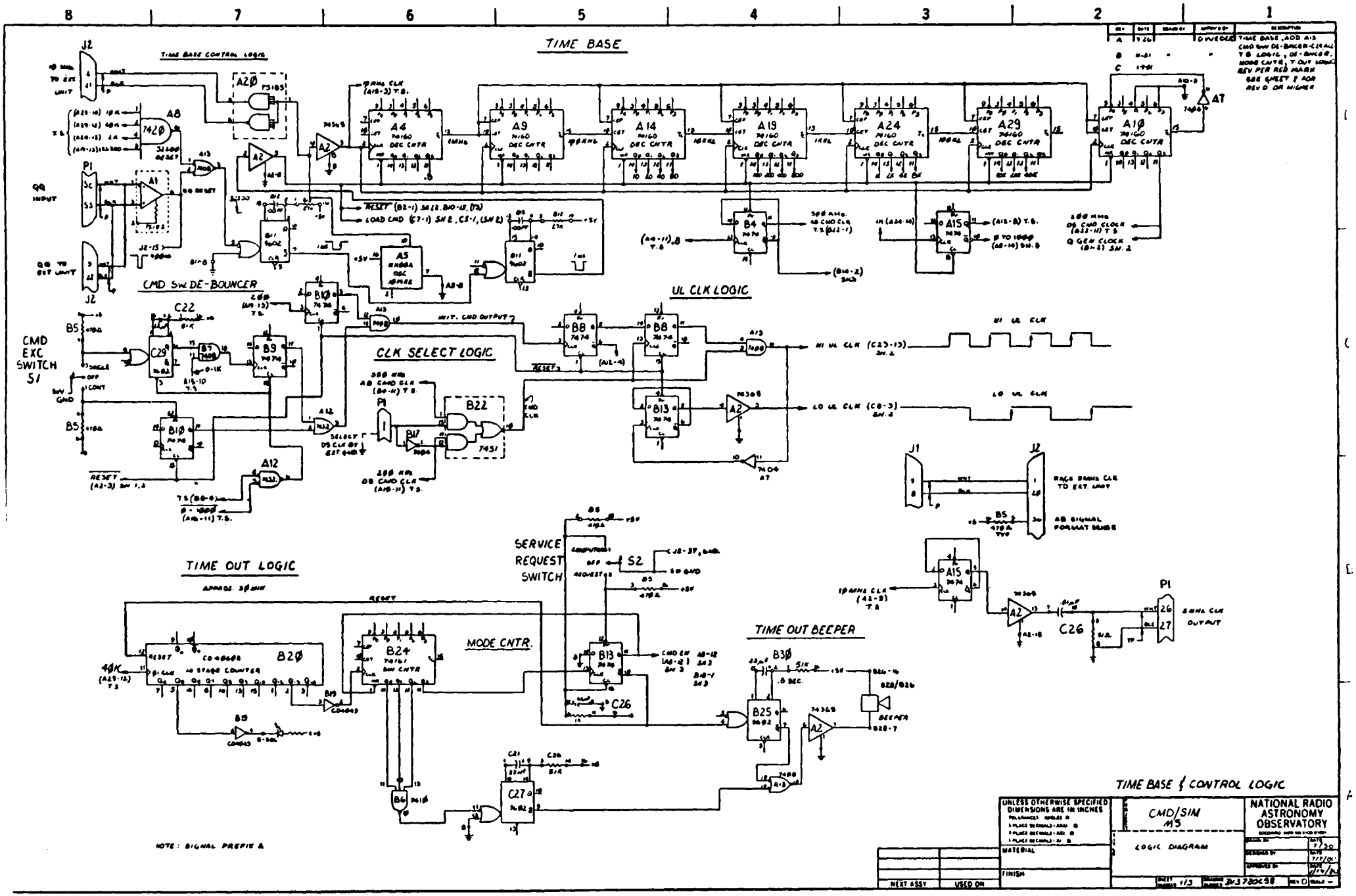
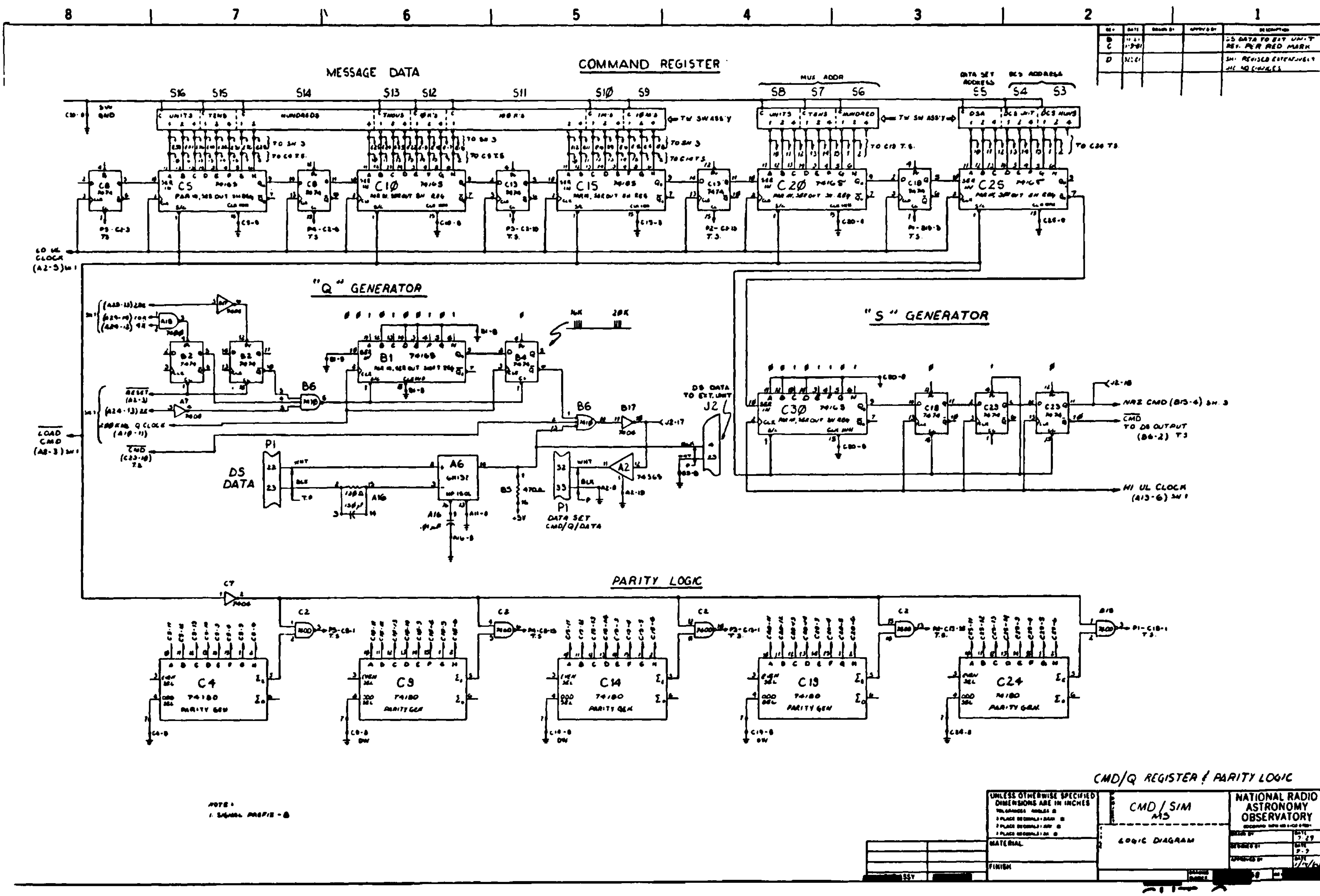
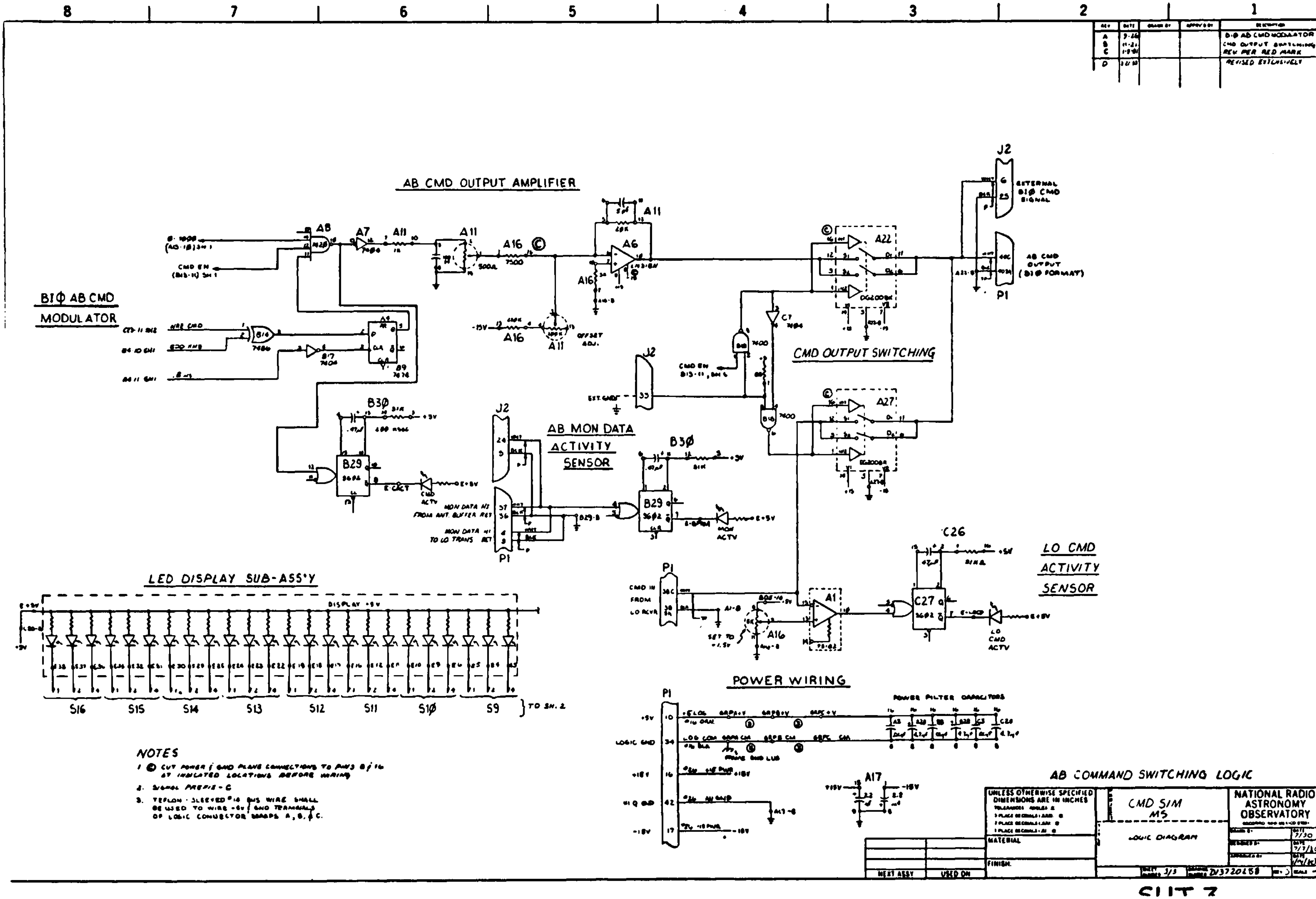


FIG. 7 - Command Simulator Block Diagram


TIME BASE
TIME BASE CONTROL LOGIC
CMD SW DE-BOUNCER
CLK SELECT LOGIC
UL CLK LOGIC
CMD EXC SWITCH S1
SERVICE REQUEST SWITCH
TIME OUT LOGIC
MODE CNTR.
TIME OUT BEEPER
NOTE : SIGNAL PREFIX A
TIME BASE & CONTROL LOGIC
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL
FINISH
NEXT ASSY
USED ON
CMD/SIM M5
LOGIC DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY
DRAWN
CHECKED
APPROVED
DATE
SIZE
DRAWING NUMBER
SCALE
SHEET 1/3
REV

CIIT 1


MESSAGE DATA
COMMAND REGISTER
S16 S15 S14 S13 S12 S11 S10 S9
MUX ADDR
S8 S7 S6
DATA SET ADDRESS
DCS ADDRESS
S5 S4 S3
C5
C10
C15
C20
C25
"Q" GENERATOR
"S" GENERATOR
B1
B6
B17
A6
A2
C30
J2
P1
DS DATA
DS DATA TO EXT. UNIT
DATA SET CMD/Q/DATA
LOAD CMD
NRZ CMD
HI UL CLOCK
PARITY LOGIC
C4
C9
C14
C19
C24
74180
PARITY GEN
CMD/Q REGISTER & PARITY LOGIC
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL
FINISH
CMD/SIM
LOGIC DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY


AB CMD OUTPUT AMPLIFIER
BIΦ AB CMD MODULATOR
CMD OUTPUT SWITCHING
AB MON DATA ACTIVITY SENSOR
LO CMD ACTIVITY SENSOR
LED DISPLAY SUB-ASS'Y
POWER WIRING
POWER FILTER CAPACITORS
EXTERNAL BIΦ CMD SIGNAL
AB CMD OUTPUT (BIΦ FORMAT)
OFFSET ADJ.
CMD IN FROM LO RCVR
MON DATA HI FROM ANT. BUFFER RET
MON DATA HI TO LO TRANS RET
CMD ACTV
MON ACTV
LO CMD ACTV
DISPLAY +5V
S16
S15
S14
S13
S12
S11
S1Φ
S9
TO SH. 2
NOTES
1. © CUT POWER & GND PLANE CONNECTIONS TO PINS 8 & 16 AT INDICATED LOCATIONS BEFORE WIRING
2. SIGNAL PREFIX - C
3. TEFLON - SLEEVED #16 BUS WIRE SHALL BE USED TO WIRE +5V & GND TERMINALS OF LOGIC CONNECTOR SNAPS A, B, & C.
AB COMMAND SWITCHING LOGIC
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL
FINISH
NEXT ASSY
USED ON
CMD SIM M5
LOGIC DIAGRAM
NATIONAL RADIO ASTRONOMY OBSERVATORY
SHEET 3/3
D13720258