VLA Technical Report No 63
The Serial Line Controller

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### 1.0 INTRODUCTION

This manual describes the operation of the Serial Line Controller (SLC) and was written to serve as the trouble-shooting and maintenance guide for this component of the Monitor and Control (M\&C) System. The manual describes both the $B$ and $C$ models of the Serial Line Controller and the interfaces to the Modcomp computers Monty and Bachus. The essential interactions between the the SLC and the Modcomp interface driver program are discussed.

To put the Serial Line Controller into system context the reader is referred to the following manuals: "An Overview of the Monitor and Control System", Electronics Memorandum No 44; "The Central Buffer", VLA Technical Report No 60; "The Antenna Buffer", VLA Technical Report No 59; "The System Buffer", VLA Technical Report No 61 and "The Data Set", VLA Technical Report No 58.

Figure 1 depicts the block diagram of the Monitor and Control System; note the relationship of the Serial Line Controller to the Central and System Buffers and the control computers. Figures 2 and 3 depict the $M \& C$ System Antenna and Central timing operations. Figure 4 depicts the format of the command and monitor data messages.

The emphasis of this manual is on the SLC functional details; the writer's intent is to provide a thorough description of the theory of operation. Straight-forward portions of the logic are treated briefly; more complex areas are fully explained and the explanations are augmented by timing diagrams. SLC hardwarecomputer software interactions are briefly described to show the reasons for certain features in the logic. Using this manual as a reference, a digital maintenance technician should be able to quickly identify and repair malfunctions in the SLC.

### 2.0 SERIAL LINE CONTROLLER DESCRIPTION

The Serial Line Controller (SLC) is the nexus of communication between the control computers and the VLA electronics; all VLA control and monitor operations are performed by the SLC, (clock and correlator excepted). The SLC extracts parallel command words from Monty and Bacchus, formats them into time-serial command messages and outputs them to the Central and System Buffers for distribution to the Central and Antenna Electronics. The SLC polls the Central and System Buffers for time-serial monitor data messages which are broken into parallel words and inserted into Monty and Bacchus. Computer I/O is accomplished via DMP (direct memory path) so that the computer programs are minimally perturbed by interactions with the SLC.

The Serial Line Controller does not have bulk memory; messages
are temporarily stored in 40 bit command and monitor data buffer registers which are immediately unloaded to the Central/System buffers and computers.

It is appropriate to digress $a$ moment and discuss the architecture and some properties of the VLA Electronics. The VLA Electronics are highly integrated and the structure can be considered to consist of two distinct parts: a distributed portion which is not antenna-particular (ie not directly associated with antenna functions) and an antenna-parallel portion which is replicated for each antenna. In the antennaparallel portion there is no coupling between antenna electronics. By design the distributed portion was kept to a minimum so that most of the electronics are antenna-parallel. This emphasis on an antenna-parallel architecture simplifies maintenance in that failures tend to be isolated to a single antenna which may repaired without perturbing the operational antennas; thus observations can continue while a broken antenna is being repaired. Examples of distributed systems are the Master Local Oscillator and LO Distribution systems which generate and distribute reference frequencies for the antennaparallel portions: -- the Local Oscillator-Waveguide Transmission Systems.

The Monitor and Control System conforms to the VLA Electronics architecture in that the SLC is the distributed portion of the system and the Central-Antenna Buffers and associated Data Sets are the replicated antenna-parrallel portion. The SLC is distributed over all the antennas and is a serial-to-parallel and parallel-to-serial interface between the control computers and the buffers.

All communications between the Central Electronics and Antenna Electronics are implemented in the Local Oscillator-Waveguide Transmission System which has a 1 Ghz bandwidth and 1 Mhz guard bands. There is plenty of bandwidth available for transmission of control and monitoring signals and there are no compelling reasons for any other transmission system between the central control system and the antennas.

Time is the driving parameter in the VLA Electronics; all functions are keyed to the 19.2 Hz period and all communications between the Central and Antenna Electronics must adhere to the half-duplex mode of the Local Oscillator-Waveguide Transmission System. The Central Electronics transmit to all the Antennas for 1 millisecond and all Antennas transmit to the Central Electronics for the 51 milliseconds balance of the 52 millisecond cycle.

The M\&C system operates in a half duplex transmission mode in concert with the Local Oscillator-Waveguide Transmission System. The command message memories in the Central Buffers are loaded
serially over a period of 24 milliseconds with command messages in preparation for concurrent transmission down the waveguide during the 1 millisecond period. Conversely, for 24 of the latter portion of the 51 milliseconds period serial monitor data messages are concurrently returned from each antenna and accumulated in the Central Buffer's monitor data memories. The SLC polls the Central Buffers to input this monitor data to the control computers during the first 24 milliseconds of the 51 millisecond period.

Another architectural digression is the question: should the SLC have been a computer? A computerist's design approach to implementing the M\&C system would probably have been to make the SLC a computer which communicates with each antenna on an asychronous basis through a 40 mile, 72 drop, independent full duplex. communication system, (very expensive in itself). With this approach the message memories would be the computer's RAM memories and any failure would bring down the whole system. The cost of such a system with an independent communication system would be very high.

Attempting to adapt a computer-styled Monitor and Control System architecture to the LO-Waveguide transmission system imposes severe constraints on the computer characteristics. The VLA Electronics timing requirements and the LO-Waveguide transmission system modes would probably require an extremely fast processor and antenna-parallel auxiliary memories for the command and monitor data messages. Memory loading/unloading to/from the Local Oscillator-Waveguide Transmission System would be controlled by the Lo System timing. The transmissions would undoubtably be serial; parallel transmission would be horribly expensive and bulky. The message handling functions of serial/parallel conversion, load/unload shifting, synchronizing and storage are inherently simple and do not need the logical power of a computer. In performing these functions, the operating speeds of the hard-wired logic of the Monitor and Control System are quite reasonable but in contrast, a computer would have to be blazing fast to perform the equivelent functions. These message-handling functions could possibly be managed by a set of 32 microprocessors coupled to the computer's DMP channels.

The considerations outlined above determined the character of the Monitor and Control System.

The Serial Line Controller performs an analysis of the incoming monitor data messages to determine whether: 1) the message is tainted with parity errors; 2) the DCS address is not consistent with the port address; 3) the polled buffer has not responded to the polling request within the allotted period. Flags are set in the data input to the computers when these error conditions are detected.

Drawinc C13721B09 depicts the logic flow of the SLC and drawing C13721B08 depicts the SLC logic block diagram. The dotted lines and Sheet Number label reference the associated drawing sheet number.

Unlike the other components of the Monitor and Control System, the SLC is packaged in a conventional chassis with a selfcontained power supply; the digital logic is situated on 12 wirewrapped logic connector boards. 32 rear panel connectors connect the SLC command and monitor data lines to the System and Central Buffers. 8 rear panel connectors may be connected to Data Taps to display command and monitor data messages. A rear panel connnector brings in the $Q Q$ signal from L8 and a 10 Mhz clock from the Master 10 system. Two rear panel connectors carry parallel 16 bit computer $I / O$ and handshake signals to SLC interfaces in the Modcomp computers Monty and Bacchus. Drawing C13721P67 depicts the rear panel connector configuration.

Front panel switches permit an operator to cause either of the two computers to assume total control of command message formulation or permit selective assignment of command control on an antenna-by-antenna basis. The reason for these switches is that at the time the Monitor and Control System specifications were written, it appeared that the way to control a second array (ie subarray) was to use a separate computer; another reason for this dual computer capability is that it would permit the second array to be operated in a test mode without perturbing the observing array. Front panel LED displays show message and parity error status. The details of the switch and display logic are described below.

Drawing Cl3721P67 depicts the Models $B$ and $C$ SLC front panel controls and displays. The differences between the $B$ and $C$ models are the composition of the front panel displays. The Model $C$ unit started life as a backup Model B but the front panel controls and display logic was modified to permit a more detailed display of monitor message message flow and computer interface interactions. These differences are discussed in Section 3.9.

### 2.2 SERIAL LINE CONTROLLER I/O SIGNALS

- QQ Pulse, - a 400 ns differential TTL logic signal from the central L8. $Q Q$ designates the start of a VLA machine cycle and is defined as zero time in the time base.
- LOMhz Clock, - The 10 Mhz clock is a 10 dbm level sinusoidal signal from the Master LO system which is used to clock the SLC logic.
- SLC Command Outputs, - 32 TTL level output ports which convey
command messages to the Central and System Buffers. These outputs also carry repeated monitor data messages so that a Data Tap connected to a Central or System Buffer is able to trap any M\&C System message. The Central and System Buffers are also polled for monitor data by $Q$ characters on these Command Output lines. These lines drive optical isolators in the Central and System Buffers for ground isolation between the buffers and SLC.
- SLC Monitor Data Inputs, - 32 TTL level input ports which convey monitor data messages from the Central and System Buffers. Optical isolators on the monitor data input lines provide ground isolation between the buffers and the SLC.
- SLC Data Tap Outputs, - 8 TTL level output ports which convey the command and monitor data messages to 8 Data Taps for visually monitoring the M\&C System message flow. These lines drive optical isolators in the Data Tap for ground isolation between the SLC and Data Taps.
- Computer $A$ and $B$ Interface Lines, - a set of TTL level parallel 16 bit computer output and 16 bit computer input lines and handshaking terms to the SLC Interfaces in the Monty and Bacchus Modcomp computers. These interface lines also carry mode discretes to tell the interface the SLC mode, (ie command mode and monitor mode). These computer interface lines are terminated in optical isolators to eliminate ground noise effects which could result from the long (150 feet) SLC-computer cable.


### 2.3 MESSAGE FORMAT DESCRIPTION

Figure 4 depicts the format of the command and monitor data messages and the " $Q$ " (for Query) character format. The messages are prefixed by an "S" (for Start) character which signals that a message immediately follows. The bit rate of the $S$ and $Q$ characters is twice the bit rate of the data bits to make these characters unique. The message consists of five 8 bit data bytes; the first byte contains a 5 bit DCS address which can range from 0 to 37 (octal) and a 3 bit Data Set address which can range from 0 to 7 . The second address is an 8 bit Multiplex address which designates a particular command or data channel. The Multiplex address can range from 0 to 377 octal (255 decimal). The third, fourth and fifth bytes are components of a 24 bit command or monitor data argument. In the case of an analog data message, the 24 bit argument consists of two 12 bit values resulting from the conversion of two analog signals by the Data Set's analog to digital converter. In all address and argument values, the first bit (in time) is the most significant bit.

In this manual DCS and multiplex addresses are always expressed as octal numbers.

The "Q" character is used by the SLC to poll data from a Central or System buffer.

The $S$ and $Q$ character bit rate is $2 \mathrm{Mhz} / \mathrm{bit}$ and the message bit rate is 1 usec/bit.

### 2.4 TIME-DRIVEN SERIAL LINE CONTROLLER OPERATIONS

The Serial Line Controller outputs command messages during the period of 28,952 usec to $49,456 \mathrm{usec}$ and polls the Central and System Buffers for monitor data messages during the period of 1024 usec to 23,296 usec. Obviously the Central and System buffer's logic are conditioned to accept command messages and output monitor data messages during these periods. Like the Central and System Buffers the SLC is required to perform concurrent operations. At the end of each of these periods the SLC Interface generates a Service Interrupt to signal the control software that the command or monitor period has ended.

COMMAND MESSAGE ACCESS, FORMATTING AND OUTPUT
At 80 usec intervals during the 28,952 to 49,456 usec period the SLC alternately reads the contents of the two computer's command buffer memories and formats command messages from memory word triplets, ie - three memory words are combined to form the address and argument components of a command message. These messages are then output to the Central and System Buffers. The front panel control switches mentioned above determine whether or not the accessed commands are permitted to be output.

The composition and number of commands output in a given cycle depends upon the contents of the computer's command buffer memory. Prior to the 28,952 time, the computer initializes the command buffer memory with the command words to be output (the balance of the memory is cleared). The most significant byte of the first 16 bit word of the three word triplet contains a sync pattern which is detected by the SLC logic. This sync byte causes the SLC to load the next two 16 bit message components into the SLC output register, formulate parity, append the S character and shift out the assembled command message to all buffers. Because the SLC command message formulation and output logic is dependant upon the presence of the sync pattern, the SLC does not output false command messages (ie messages to nonexistent devices) when the SLC accesses the cleared portion (ie after the last command word triplet) of the command buffer memory. The command transfers between the two computers and the SLC are asynchronous and are as fast as the DMP channels will operate. The observed command word transfer rate is about 5 usec/transfer.

The required command capacity of the SLC/Computers is 128 command messages per VLA cycle; thus any one of the 32 possible
antennas could receive 128 command messages in a given VLA cycle. The command capacity of the Central Buffers is 4 antenna command messages per cycle.

How are the various commands formulated and output by the control computers? The telescope operator IG overlay display shows 4 columns of command words per antenna-DCS address; they are: 1) antenna pointing commands; 2) phase-tracking commands; 3) initialization commands and 4) telescope operator manual commands. The command messages are formulated on a regular schedule in which there are 192 VLA machine cycles per major cycle; the period of this major cycle is 10 seconds. Commands are output by the command formulator program at appointed times in this schedule so that the peak capacity of 4 commands/antenna/VLA machine cycle is never exceeded. Antenna azimuth and elevation pointing commands are alternately output at a 9.6 Hz rate; - thus there is always an antenna pointing command in a VLA machine cycle. 7 phase-tracking commands (ie L7 rate, phase and L8 Walsh function) are output on sucessive cycles every 24 VLA machine cycles. When it is source change time, a set of initialization commands are output on sucessive cycles to set up the L6's, Focus/Rotation system, Front End band and filter selections, Back End filters etc. Finally, the telescope operator may output manually-generated commands at any time in the 192 VLA machine cycle framework.

Now as to command density: the average command message flow is about 1.5 command messages/VLA machine cycle/antenna; most of the time only one command message is output per cycle. Two command messages per cycle occurs about a quarter of the time (pointing + fringing commands); three command messages may be output for a few cycles during source changes (several minute intervals) and four commands may occur when a telescope operator outputs a manual command during a source change burst of pointing, phasetracking and initialization commands. The last case is a rare event. For test purposes it is possible to force one, two, three or four test command message outputs/VLA machine cycle by the use of some special system commands. Most people are not aware of this capability.

## MONITOR DATA POLLING AND INPUT TO THE COMPUTERS

At 58 usec intervals during the 1024 to 23,296 usec period the SLC sequentially polls the 32 Central (or System) Buffers for monitor data messages. The polling sequence is DCSO .... DCS37, DCSO .... DCS37 etc for a total of twelve monitor data messages per Central or System buffer. This produces a sequence of 384 monitor data messages which are input to the computer's monitor data buffer memories per waveguide cycle.

The order of the monitor data message components in the computer monitor data buffer memories is:

| Data Set | DCS-0 | DCS - 1 | DSC-2 | DCS - 3 |  | DCS-37 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 (ACU) | MW1 | MW1 | MW1 | MW1 |  | MW1 |
| 1 (FE) | MW1 | MW1 | MW1 | MW1 |  | MW1 |
| 2 (BRack) | MW1 | MW1 | MW1 | MW1 |  | MW1 |
| 3 (F/R) | MW1 | MW1 | MW1 | MW1 |  | MW1 |
| 4 (XBnd) | MW1 | MW1 | MW1 | MW1 |  | MW1 |
| 0 ( ACU ) | MW2 | MW2 | MW2 | MW2 |  | MW2 |
| 1 (FE) | MW2 | MW2 | MW2 | MW2 |  | MW2 |
| 2 (BRack) | MW2 | MW2 | MW2 | MW2 |  | MW2 |
| 3 ( $\mathrm{F} / \mathrm{R}$ ) | MW2 | MW2 | MW2 | MW2 |  | MW2 |
| 4 (XBnd) | MW2 | MW2 | MW2 | MW2 |  | MW2 |
| 5 (DRack) | MW1 | MW1 | MW1 | MW1 |  | MW1 |
| 5 (DRack) | MW2 | MW2 | MW2 | MW2 |  | MW2 |

You may ask: "what are Monitor Words 1 and 2?". Monitor Word 1 (MW1) is the first monitor word evoked from a Data Set in a VLA machine cycle. The MWI values are used by the control computers in the analysis of the performance of the VLA. MW2 values are used for intensive sampling of data channels for test purposes.
See the Data Set manual (VLA Technical Report No 58) for a discussion of the MW1/MW2 properties.

The monitor data computer 16 bit words are concurrently presented to Monty and Bacchus at 16 usec intervals; the computers must accomplish the word storage in this period. The observed DMP response time is about 5 usec so 16 usec provides plenty of reserve time. Other than this 16 usec constraint the transfers between the SLC and the two computers are asynchronous.

### 3.0 DETAILED CIRCUIT DESCRIPTION

### 3.1 TIME BASE AND CONTROL DISCRETES

The time base logic (Sheet 1) develops clocks and control discretes to regulate the command output and monitor data gathering functions. The clocks are used to clock messages into and out of the SLC. An external, 10 dbm level sine wave clock from the Master LO system is amplified by $A 30$ and the output is squared by 7404 A2402. The output of A2402 and A2404 are two phases of the SLC 10 Mhz clock; one phase drives the time base counters B26 through B11. The time base is cleared (ie set to zero) by the $Q Q$ pulse detected by differential receiver A29 which clocks one-shot A2806 through nor gate A2013. The 5 usec output (much wider than it needs to be) of A2806 clears the time base counters though the asynchronous master resets. For bench test purposes gate $B 0506$ and one-shot $A 2809$ generate a psuedo-QQ pulse at 52,224 usec which is fed back to nor gate A2013.

The 10 Mhz oscillator in location A26 is used for bench test purposes when there is not a 10 dbm 10 Mhz source available. The oscillator should be removed when the SLC is installed in the system.

Gates B 0601 and B 0710 decode timing terms to generate set and reset terms for Command Mode flip-flop B0110. The time base reset is an extra pair of suspenders on B0110. This Command Mode discrete term is the qualifying term for all command message operations in the SLC. When this term is true, counters B16 and B21 generate a strobe term at 80 usec intervals and toggles flip flop Al505 which generates the Computer A Mode+, Computer B Mode+ enables which alternately select interfaces in computers Monty and Bacchus for command word message components. The strobe term E1710 is used to load an $S$ character in the command output register. The 10 Mhz clock is used in gate A2010 to avoid the effects of the 74160 glitch. The $Q Q$ term is applied to or gate E1710 to provide the first load S strobe. Flip Flops A0510 and A0410 are alternately turned on every 80 usec by A1505, the A Mode/BMode toggling flip flop. The outputs of these flip flops through gates A0306 and A0310 signal the start of an attempt to extract a command word triplet from either of the two computers. The details of command message loading and output are discussed in Section 3.2.

The Monitor Mode control flip flop A1911 is set by gate A1810 at 1024 usec and cleared by the fall of counter A0713 at the count of 384 in counter A17, A12, A7. This counter is the Monitor Data Polling Counter which controls the monitor data polling; the DCS address to which a $Q$ will be directed is determined by the DANTA-1 ... DANTA-16 lines from A17 and A12. These address lines also select the appropriate monitor data multiplexer input. This counter permits 384 cycles of counter A22, A27. A22 and A27 have a period of 58 usec which is the Qpolling/Central Buffer response period. The terminal count of A22 and the 1 Mhz clock in gate A1303 causes a $Q$ to be output via gate A1306 and inverter A2404 (Sheet 3). The $Q$ generator E26 is on Sheet 10.

Gates E0810 and A2003 generate a Monitor Data Buffer clear at the count of 55 in counter A27, A22; this clears the monitor data buffer register just before the arrival of monitor data from the addressed Central or System buffer. The register is cleared so that in the event the buffer does not respond the register contents will be zero.

Gates C1114, C1106, C113 and flip flop C1206 generate 2 Mhz clocks with a fixed phase relationship to the time base. The two C1l gates and 10 Mhz clock toggle flip flop Cl206. Or gate C20 drives the command unload clock generator, C1303 @ coordinates B2 on Sheet 12. Inverter E0314 drives the Q generator and blanking generator on Sheet 10 .

### 3.2 COMMAND MESSAGE LOADING, FORMATTING AND OUTPUT

In the time base discussion above (Sheet 1) the low-true terms A Data Req and B Data Req from A0310 and A0306 were identified as command word request terms to the computers Monty and Bacchus. When the selected computer (assume computer A) senses the lowtrue request it places a parallel word on the output lines and makes it's response, A Data Xfer + on K1604 (Sheet 6) go high true. This term is applied to the input of a delay shift register Ell which is clocked at 10 Mhz . E11 thus loads a stream of 1 's. $\quad 300+$ ns after the rise of A Data Xfer + the third stage of Ell, Q2 goes high true which causes A Data Xfer - to go low (D2510). When D2510 goes low it forces A Data Req (A0310) low again and the computer interface in response lowers $A$ Data Trans + so that zeros are now shifted into Ell. When A Data Trans + goes low it forces A Data Req high again which again causes Ell to again load a stream of l's. This cycle would continue indefinetely with the high/low time durations determined by the delay time of shift register Ell, the propagation time of the cable and the delay of the interface logic in Monty. Control logic (described below) limits the sequence to 3 cycles. What we have described is the command word handshaking logic of "Hey computer give me some data", a computer response of "I heard you, data is on line" which generates another "Hey computer give me some data" etc. On each cycle of this handshaking the computer outputs a new word from the command word buffer. The timing for these interactions is depicted on the next page.

SLC - COMPUTER COMMAND INTERFACE HANDSHAKING

A Data Req
A3-10
A Data Xfer + K16-4


E11 Q2
E11-13


Now, how are the three command words loaded? Sheet 9 has the lst word pattern detector B19 and B24 which are parallel comparators. Bits 8 through 16 of the computer's parallel output are tested for a match against the 10101010 sync pattern and if the word matches the pattern the $A=B$ output goes high true. The pattern detector has an enable which we will discuss later. Gate C2606, qualified with A Mode goes true and this is applied to the data input of another shift register E12 on Sheet 12 . E12 is clocked by gate D1913 which senses two 1's in E11 during the time that 1 's are shifting through. When Q2 goes true, shift
register $E 12$ is clocked and the 1 from the pattern detector is loaded into E12. The 0's that are loaded into E11 (the response of the computer when it lowers A Data Xfer + ) causes the El2 clock to go low again but it will rise again on the next cycle of interaction between the $A$ computer and SLC. These interactions are depicted on the timing diagram below.

COMMAND WORD LOAD TIMING
E12 C1k
E7-10
Patt Det
B24-6
E12-Q0
E12-15
E12 Q1
E12-14
E12-Q3
E12-13
Patt Det En D05-5


These sucessive clocks shift the single 1 through E12; this 1 acts as a commutating term to sequentially enable the three word transfers. How is this single 1 generated? When the $l^{\prime \prime} s$ being shifted through reach Q3 (100 ns after the E12 clock), gate E0710 is made true by E11 Q3 and the 1 in E12 at E12 Q1. E0710 direct sets flip flop D0505 which disables the pattern detector enable flip flop D1505, thus sucessive computer words cannot activate the pattern detector. $E 0710$ is the lst WD Load - strobe which direct loads shift register B30 (Sheet 9) with the lower byte of the computer word standing on the computer inputs on Sheet 9. As E11 sucessively cycles waves of $I^{\prime \prime} s$ and $0^{\prime} s$ in interacting with the computer, the 1 loaded into $E 12$ sequentially activates the 2nd Word Load A - and 3rd Word Load A - load strobes which causes these words to be sequentially loaded into the B13-B14 (2nd word) and B8-B9 (3rd word) registers. The trailing edge of E0703, the 3rd Word Load A - strobe clocks flip flop D0505 clear which will permit the pattern detector to become active for the next triplet of command words. The pattern detector is enabled by the Load $S$ term (discussed above) from E1710 on Sheet 1 ; this was described above in Section 3.1. When the leading edge of the 1 that is shifting through El2 reaches Q3 it clocks flip flop A0410 false though inverter E0610. This terminates the transfers until the next cycle, 160 usec later when the $A$ computer is accessed again. The timing for this logic is depicted on the next page.

## 3 WORD TRANSFER CONTROL

load Control
A4-10
A Data Req
A3-10
A Trans +
K16-4
3rd Word +
E12-13


Now let's consider the parity bits for the message that we are formulating. Parallel parity generators B4 and B2 sense the 16 bit computer words; when list Word Load A - goes true (E0710 Sheet 12), it strobes gate $\mathbf{C 2 2 1 0}$ which enables the parity generator B 0206 output to be loaded into the output register parity flip flop B2511. The and and 3rd word loads cause the appropriate parity bits to be loaded into the their appropriate parity flip flops.

Well, we have managed to load the command message output registers B30 through B8 and the parity flip flops; what happens next? When flip flop D0505 was clocked clear by the trailing edge of the 3rd Word Load - A term, flip flop C21 was clocked high. This permits flip flop C1305 to enable 2 Mhz unload shift clocks to unload the $S$ character in register E30 (on Sheet 10). Flip flop Cl311 was held initialized by the output of C1305. When C1305 rises it permits flip flop Cl311 to toggle on the 2 Mhz clock which generates a properly phased 1 Mhz clock for the command message standing in the Command Word Assembly Register, B30-B8. This clock timing is depicted on the timing diagram below.

## COMMAND UNLOAD CLOCK LOGIC

U/L Cont FF C13-5
2 Mhz Clk C13-3 1 Mhz Cl C13-11


Note that the computer inputs off the optical isolators are low true; these low-true terms are loaded into the Command Assembly Register. As they shift out the end of B30, the Uh bar output is fed to the $S$ generator input; thus they are re-inverted to high true form. At the LSB end of the register, 0 's (which are high true) are loaded into the register; when these reach the output end of the $S$ generator the output stays false.

Now let's consider the command input lines from the two computers (Sheets 6 and 7); the lines from the computers are
terminated in optical isolators which eliminates ground noise effects. The optical isolators also function as multiplexers; the isolators enable inputs are driven by the A Mode + and $B$ Mode + terms and the open-collector outputs share a common pull-up resistor on Sheet 9. A high true (ie computer 1) drive into the isolator produces a low-true output; this is why the command register serial output is inverted.

We have described how the command message is formulated and shifted out of the Command and S register; where does it go? The serial command is buffered to or gate-line drivers on Sheet 10 which are driven by the S Char Generator E30 and flip flops E25. Flip flops E16 generate two leading zeros that preface the command message. Gates E2310 and E2303 buffer the command to the or gates and have an enable-inhibit input to either let the command be output to the System and Central Buffers or to stop it. The enable line is driven by flip flop e2405 which is initially cleared (to inhibit the output) by the Load $S$ at the start of a command load cycle. E2405 is set to the permit the command output by the "Mother may I logic" described in the next section, (3.3). The bank of or gates which drive the line drivers permit the $Q$ character and repeated monitor data to be mixed into the command output lines. The reasons for this mixing will be discussed in Section 3.4 .

The 8 Data Tap drivers in the lower right of Sheet 10 buffer the command messages and repeated monitor data. One special case of these drivers exists; driver 00415 has as a command message input the set of command messages which were not permitted to be output by the Mother May I Logic. This requirement was in the original system specifications and was retained when the redesigned SLC's were built in 1978 and 1979.

### 3.3 MOTHER MAY I LOGIC OPERATION

In the previous section we described the process of accessing command words from the control computers, assembling them into command messages and shifting them out to the Central and System Buffers. In this section we will address the logic which permits the command messages to be output in accordance to the settings of the front panel Antenna Select Switches. The action of this logic tests the state of these switches on a message by message basis to determine if the command message that the computer is transferring to the SLC is in fact permitted to be output.

Sheet 8 contains the Mother May I Logic but we will first go to Sheet 9 which has register B18 and B19 which are loaded with the DCS-DSA byte by the lst Word Load + term at the same time the this byte is loaded into the Command Word Assembly Register. The DCS address bits designate the Central or System Buffer (and indirectly the antenna) by the hard-wired $D$ Rack address. On Sheet 8 the three lower address bits are select terms on 8-to-1
multiplexers C29, C30, D26 and D27. These multiplexers read the state of the front panel select switches to see which computer the operator has specified as the command source for the the DCS address of the message being loaded. The output of these multiplexers are enabled by the 2 high order DCS address bits via decoder D21 and the selected multiplexer inverted output is fed into or gate D1610.

How does the Mother May I logic work? There are two permit output flip flops that are initialized non-permissive at the start of a command formulation cycle. The Mother May I logic tests the state of the switches to clock the appropriate flip flop permissive. There are two paths of the decision logic: an exclusive or path associated with the Master Select switch (S33) and the and-or path which is driven by the switch multiplexer described above. S1 through $S 33$ have their wiper contacts tied to ground. Switch S 33 is a three position switch with a center off position in which the two terminals permit the exclusive or gate inputs to be high. In the center off position the individual select switches are operative and in the Select $A$ or Select $B$ position the antenna-by-antenna selection logic is disabled.

At the start of a command message formulation cycle the permit flip flops C1905 and C1911 are set to the inhibit state by the Load S strobe from the command timing logic on Sheet 1.

Let's first consider the exclusive or path. Assume that the Select A switch is actuated which puts a ground on exclusive or D1105 and a high on exclusive or D1102. When A Mode + is true (high) D1106 is high because the inputs differ and D1103 is also high because it's inputs also differ, ie B Mode + is low and the the $B$ Select contact of $S 33$ is high. Thus the two inputs to C1506 are high and the low true output of C1506 provides a high input to the $D$ input of the A output permit flip flop C1905. C1905 is strobed by the trailing edge of the 2nd Word A - from E0706 and set true. This C1905 output anded with A Mode + in nand gate D1803 and or gate C1513 permits the command message output in the logic described in Section 3.2.

Now what happens when the B Mode + term goes true? Assuming the Select switch is in the Select A position, - The B computer gets a shot at outputting a message; will it be permitted to do so? In this condition A Mode + is low and B Mode + is high and both exclusive or gates have identical inputs so the gates outputs are both low so that neither of the permit flip flops is set and command output permission is with-held.

Let us now consider the individually switched case in which S33 is in the center position. The exclusive or gates both have high inputs off the switch contacts and one or the other will have a high output (depending upon the states of $A$ Mode + and $B$

Mode +), but since nand gate $C 1506$ requires that both be high this path is inhibited from setting the permission flip flops. Setting a select switch to the $A$ position feeds a high into the switch multiplexer and a high to gate $C 2710$ (enabled by the $A$ Mode + ) which causes a high on the input of gate D1206. The two other inputs of D1206 are high because of S33's position so the $A$ permit flip flop C1905 is set and permission is granted for computer $A^{\prime} s$ message to be output. If the switch were set to the $B$ position the multiplexer output would have the opposite sense and gate C2703 (enabled by the $B$ Mode + ) would cause the $B$ permit flip flop to be set by the 2nd Word B - strobe edge.

The Ant $A / B$ Select Switch Monitoring logic is operational but not used; it was provided to enable the control computers to read the status of the switch settings via a Data Set. The serial readout has not been wired to a Data Set because of a lack of interest in this data.

The above discussions describe all the operations of accessing command word components from the computers, formatting and outputting them to the System and Central Buffers.

### 3.4 MONITOR DATA POLLING AND MESSAGE LOADING

In this section we will consider the process of polling monitor data from the Central and Antenna Buffers; a more complicated task than the command message operation because the SLC must detect and load the message, evaluate the quality, repeat the monitor data messages on the command lines and load the computer with the message components.

The Monitor Data Sequence counter on Sheet 1 provides port address (ie DCS address) terms DANTA 1 through DANTA 16 which select a Central Buffer data input line via Monitor Data input multiplexers (Sheet 2) and directs a $Q$ character to the selected buffer through selectors (Sheet 10).

Looking at Sheet 2 we see optical isolators (for ground noise isolation between the SLC and Buffers) and a set of four 8-input multiplexers driven by the three low order DANTA bits and enabled by the selector D8 which is driven by the two high order DANTA bits. Gate H2106 combines the multiplexer outputs and the monitor data message stream is fed to the monitor data detection and storage logic on Sheet 3 .

To evoke data from a Central or System Buffer the SLC must poll it by a $Q$ character through the selectors on Sheet 10 . These selectors (L11, L16, K29 and K17) are driven by the three low order bits of Danta and are enabled by the two high order DANTA bits through the decoder $K 27$. The $Q$ character is fed through the addressed selector to the command output drivers via the or gates.

How is the $Q$ generated? In the Monitor Data Sequencing logic of Sheet 1 , counter A27-A22 times out a 58 usec monitor data polling period; at the of this period the 1 Mhz clock and the counter TC (terminal count) are anded in gate A1303 which drives or gate Al306 (Sheet 3). This is the Send Q term that loads a Q into shift register $E 26$ and E2105. The next 2 Mhz shift clock begins to unload the $Q$ through and gate E1703 to the selectors described above. You will note another shift register is loaded by the Send $Q$ term. Register E22 and E27 are a Blanking Generator which generates a $Q$ blanking term required by the monitor data buffer logic (gates K 0603 and K 0606 ) on Sheet 3. The $Q$ blanking inhibits the rebroadcasting of the monitor data input multiplexer (Sheet 2) to the command output buffer gates until the $Q$ is completely unloaded. This period is really a blank period; the buffer will not start to output a monitor data message until it has detected the $Q$. This blanking prevents the multiplexer switching noise or a static 1 bit standing in the selected Central Buffer from perturbing the selected Central Buffer command port. Note that the monitor data input through the multiplexer is distributed to all the Central Buffer command ports via the or gates that drive the drivers. This scheme repeats all monitor data to the Central Buffers so that a Data Tap connected to a Central Buffer can detect and trap any monitor data message from any Central Buffer. This repeated monitor data is sometimes called "Gossip Data".

Having directed a $Q$ at a Central of System Buffer, what happens next? The buffer control logic has a message positioned at the output of it's serial memory so that when the $Q$ is detected the monitor data is immediately available. The Central Buffer output shift rate is 2 Mhz for the S bits and 1 Mhz for the data bits. Consider for the moment the delays and time available: the $Q$ output lasts for 5.2 usec , the round-trip propagation time is about . 2 usec, there is about . 2 usec delay in the Central Buffer, the monitor data message has a duration of 50 usec and there is about . 2 usec delay in the SLC input circuitry; and about . 1 usec is required after the message is loaded in the SLC to wrap things up; the sum of these times is 56.9 usec. The total time available for Central Buffer polling is 58 usec so there is very little spare time in the polling cycle.

The first task is to synchronize the clocking circuitry to the incoming data edges. The monitor data message is input to shift register I 30 by the 10 Mhz clock. Exclusive or 12503 detects the data edges (ie 10 or 01 patterns in 125 QO and Q1) and drives the Preset input of counter J30 through gate J1301. On the next 10 Mhz clock J30 will be set to a state of 5 and will sequence through the states of $56789,56 \ldots$ etc because of the Terminal Count feedback through gate J1301. The states of J30 are thus synchronized to the message data edges and the Q2 output is used as a shift clock on the $Q$ detect shift register J20. The timing
of this message bit synchronization timing is depicted on the simplified timing diagram below.

MONITOR DATA EDGE SYNCHRONIZATION
10 Mhz Clk J30-2
Data @
130-15


Data ©
130-14
Exl or
125-3
J30 states
J30 Q1
J30-13
J30 Q2
J30-12
J30-Q3
J30-11


When the $Q$ in $J 20$ (anded with the 2 Mhz clock) is detected by gate K1110, flip flop $K 2110$ is set and cleared . 5 usec later by the 2 Mhz clock. Thus K2110 blips low for .5 usec and is the S detect strobe that does a number of things to get the message loading process started. The timing of this message load initialization is depicted below.

S DETECTION AND MESSAGE LOAD INITIALIZATION \& TERMINATION
2 Mhz Clk J30-13


The $S$ det strobe sets the load control flip flop Jl011 which permits the load control counter JJS and J15 to count by lifting the parallel count enable. The period of this counter is determined by the pre-load count of 56 and the terminal count of 99 through the fall of J15 Q5 which clock resets the load control flip flop J1011. The $Q$ output of $J 10$ also enables counter J26 to count and the $Q 0$ output is a 1 Mhz clock phased to shift the data stream into the Monitor Data Input Register J1 through J26. This
phasing is depicted on the timing diagram below.
At the terminal count, the rise of J1910 clocks flip flop J1006 true and 200 ns later it is reset by the 2 Mhz clock from J3013. The result is a 200 ns Reg Full strobe which parallel loads the contents of the input register to the Storage Buffer Register, J2 through J27. This Reg Full strobe is or-ed with Send $Q$ (discussed later) to initiate the computer monitor data loading process.

### 3.5 PARITY AND NO RESPONSE LOGIC

A vital function of the monitor data input logic is testing the input data stream for parity errors. This is done on a byte-bybyte basis by the Parity Logic which consists of counter C7, the JKbar flip flop C0806 and the associated gates and inverters. Counter C7 is a radix 9 counter which tests the state of flip flop C0806 every 9th clock pulse. The $S$ Det term from Klllo initializes the logic. Counter C7 and flip flop C0806 are clocked by the 1 Mhz data register load clock. The inverter C0512 provides steering to C0806 so that it toggles when a data bit is a 1 . At the count of 9 through the 5 message bytes the counter reset term at C0310 tests the state of counter C0806 in gate C0606. If the parity count is even C0806 will be high and Parity Register $C 0810$ is set the 1 state. When the message address and data argument is stored in the Storage Register, the state of the Parity Register is stored in J0215.

In the event that a Central Buffer does not respond to the $Q$ or the buffer port is unused, (there are 4 spares) the Send $Q$ term for the next polling cycle is used to simulate the completion of a monitor data message load. The $Q Q$ and Send $Q$ terms applied to flip flops K2105 and J0910 enable gate J0403 to send a simulated register full term thruogh gate Jl406 to the the output sequencing logic on Sheet 12 and No Response logic on Sheet 4.

The No Response logic is on the left side of Sheet 4 and performs the function of testing to see if a Central or System Buffer responded to the $Q$ polling request. In addition it tests to see if an antenna Data Set (Data Set 0 through 4) has not responded. The Danta address bits (ie the address of the buffer port is compared with the DCS address of the message just loaded by comparator J29 and if the comparison is correct (ie they agree) the buffer has responded to the polling request. Now for the other case, - the Data Set no response. In the event that an antenna Data Set does not respond, the Antenna Buffer substitutes a psuedo message with the correct DSA address but a mux address of 205 to signal the event and warn the computer that the monitor data message argument must not be used. Mux address 205 (octal) is low true anded in gate C2312 with not DSA $=4$ (to avoid tripping the No Response logic in antennas which do not have Data Set 4 installed). The Data Set No Response or the

Danta/DSC port address mismatch can set the No Response flip flop J0905 which is clocked by the Register Full term from the monitor data message loading logic of Sheet 3 described in Section 3.4. The No Response flip flop J0905 is cleared by the Monitor Buffer Clear term at count 55 in the monitor data polling cycle timing logic of Sheet 1 .

### 3.6 MONITOR DATA OUTPUT TO COMPUTERS, COMPUTER DATA BUFFERS

Now that we have shown how the monitor data data message has been input and stored in the Monitor Data Storage Register, we shall consider how it is input to the computers.

The Reg Full term signals that the loading process has been completed and it is now time to input the data to the computers. The computers are loaded during the time that another monitor data polling cycle is in process; that is, when the SLC is accepting message $n$, it is sending message $n-1$ to the computers.

The 5 message information bytes in the Monitor Data Storage Register (Sheet 3) are broken into 16 bit computer words by the multiplexers on Sheet 4 and the words are sequentially inserted into the computers by the logic on Sheet 12

The multiplexers on Sheet 4 are dual $4: 1$ units which are controlled by the Sel A and Sel B terms from the control logic on Sheet 12 and select 16 bit portions of the Monitor Data Storage Register for input to the computer via the 74368 line drivers. The drive is low true; a 1 input produces a low signal on the output line.

You will note that the two high order bits in the first word (2CO and 1CO) are the Parity and No Response bits which may be set in the course of evaluating a monitor data message. The next 6 bits form a sync pattern to signal the start of a triplet of monitor data words to the SLC driver program. This pattern is (starting with MSB): Par, No Resp, 1, $0,1,0,1$.

We will consider the use of the 4 th channel of the multiplexers in Section 3.7.

On Sheet 12, the Monitor Data Sequence Control Logic generates the multiplexer select addresses $A$ Sel and $B$ Sel by decoding states in counter D30. Counter D29 and D30 are cleared by the Reg Full strobe from the monitor data message loading logic (discussed in Section 3.4). D29 functions as a 16 usec delay generator to provide 16 usec of delay between the three 16 bit word transfers. As counter D29 sequences, the fall of Q4 clocks counter D30 which increments the A Sel, B Sel bits on the outputs of gates D2406 and D2403 through the states: 00,10 , and 01. The flip flop E 2410 provides a high true enable for the decode; we will discuss the use of this term in Section 3.7.

The first transfer to the computer is initiated by the Reg Full strobe which clocks flip flops D2006 and D2010 true via or gate D1810. The Dump Enable from gate D1813 enables the power nands D1003 and D1006 to generate the low true A Data On Line and B Data On Line signals to the two computers. When $A$ the computer has accepted the data it returns a low true signal A Data Rec'd (from the optical isolator on Sheet 6) which direct clears the Dump Request F1ip Flops D2006 and D2010. When counter D29 Q4 falls the first time after 16 usec and the second time after 32 usec it clocks these flip flops to initiate the second and third word transfers.

When counter D30 reaches the count of 3 , gate D1813 feeds back a low to reset the counter to the state of 15 on the 4 th clock (at 48. usec in the output sequence); this forces the steering to the $D$ input of flip flops D 2006 and D 2010 high and they remain in that state with the result that there are no more Dump Requests to the computers until the next Reg Full strobe. The operation of this logic is depicted on the simplified timing diagram below.

MONITOR DATA INPUT TO THE COMPUTERS
Reg Full
D29-1
A Sel
D24-6
B Sel
D24-3
A Data OL
D10-3
A Data Recd D20-4 Dump en
$\qquad$
A/B Xfer En D30-12

The role of the C16 flip flops will be discussed in Section 3.9 .

One-shot $H 2407$ stretches the monitor period to the computer interface to permit the computer to input the last monitor word.

### 3.7 SLC STATUS OUTPUT TO THE COMPUTERS

In the previous section we alluded to the use of the 4th channel of the multiplexer in the Monitor Data Buffer Output to Computers A/B. This channel is used to provide SLC status to the computers which is permitted during the period of $Q Q$ (ie zero time) to 1024 usec by the flip flop E2410 which forces the A Sel and $B$ Sel addresses to the 11 . This status is not readable at
any other period and cannot be forced to be output by the computer. There are no interactive actions; if the computer wants to obtain the SLC status it reads the data output lines via the computer interface direct input.

What is this SLC status? Register Ll7 is a storage register whose contents are the DCS (ie Central Buffer) address of the most recent monitor message data parity error. This data is output on the lowest five bits of the upper data byte. This feature was implemented to provide an alternate means of indicating parity errors when a Buffer output is so badly errortainted that it cannot be detected by the monitor data message detection circuitry. This feature is of little use except under the very rare conditions of horrible data contamination. When these conditions do occur it is pretty easy to identify the malfunctioning monitor data channel.

### 3.8 FRONT PANEL DISPLAY LOGIC

In this section we will discuss the logic which drives the front panel LED displays. There are two radically different versions of these displays; this is the basis of distinction between the Models B and C SLCs.

MODEL B DISPLAY LOGIC
MONITOR DATA DISPLAY LOGIC -- The Model B Monitor Data Display Logic is very similar to the Model $C$ but two sets of LED display registers are used. Since the action of the storage logic is so similar in the two models the discussion will address the differences; for more detail see the Model C Monitor Data Storage logic discussion below. The adders and decoders perform the same function of decrementing the DANTA address and chip selection. The 4 -input and gate E0806 senses the final state in transferring the monitor data word triplet to the computer and enables the decoder; the $A$ and $B$ Transfer Confirm strobes load the LED display storage registers.

COMMAND DISPLAY LOGIC .- The command display logic (Sheet 6) shows command message activity on an antenna-by-antenna basis.

The logic consists of two sets of 74368 LED drivers which sense command message flow at the Command Line Drivers inputs. The Mode A + , Mode $B+$ terms anded with the CMD Mode term from the timing logic drive the LED drivers tri-state enables. When the enable is low and there is activity on an output port the LED is illuminated.

PARITY ERROR DISPLAY -- The Parity Error Display Logic (Sheet 6) displays monitor data parity error activity on an antenna-byantenna basis. The action of this logic is that as the monitor data is polled from the buffers, the DANTA address bits point
to a parity error memory and when the message is loaded into the Monitor Data Storage Register, the state of the Parity Error bit is strobed into the addressed parity error memory bit. Because the message duration is so short the error occurrance periods are stretched by a factor of 16 to brightly illuminate the Parity Error display LED's. The display register LED's are illuminated for a period of 16 QQ periods and then cleared.

The errors accumulate over a period of 16 QQ's in the loading register E 20 through E 15 ; when counter E 13 Q 3 output falls the contents of the loading register are transferred to the display register Fl6 through F15. The loading register chips are selected by the DANTA bits 8 and 16 via decoder $E 18$ and the bit is selected by the lower order DANTA bits on the 9334 address inputs. The Reg Full strobe from the Monitor Data Load logic (Sheet. 3) strobes the decoder and an error bit is stored depending upon the state of the Parity Error bit in the Monitor Data Storage Register.

## MODEL C DISPLAY LOGIC

The Model $C$ SLC front panel display logic was designed to provide a more detailed picture of the interactions between the SLC, the computers and Central/ System Buffers.

MONITOR DISPLAY -- The Monitor Data Display Logic (Sheet 5) shows the detection of monitor data messages from the Central or System buffers by comparing the Central Buffer port address (DANTA 1 through DANTA 16) with the DCS address of monitor data messages temporarily stored in the Monitor Data Storage Register, (Sheet 3). The 7483 adders subtract one count from the DANTA terms because the DANTA address is always one count higher than the address of the most recent monitor data message temporarily stored in the data storage register. The subtraction is implemented by inverting the DANTA inputs, adding zeros and reinverting the adder outputs. The adder output is then compared in the magnitude comparator and if the addresses agree a zero is stored in a 9334 addressable latch bit addressed by the 3 low order DANTA bits. The appropriate chip is selected by a decoder driven by the two high order DANTA bits. The stored zeros sink current from an LED to indiate the presence or absence of monitor data from a Buffer.

COMMAND DISPLAY -- Sheet 11 contains the command display logic which shows the activity of the computer command outputs. The front panel selector switch permits the display of the command activity of both computers on an individual Data Set basis or an inclusive basis (ie all Data Sets).

The storage memories are 9334 addressable latches which are set on the basis of the DCS address contained in the command message (CANTA 1,..16) and the switch-selected Data Set Address of the
message, (CDSA 1, 2, 4). Because the duration of the command message is short ( 50 usec ) the display LED's are cleared every 16 VLA machine cycles. The setting and clearing are done by two different processes; we will first consider the method by which the displays are illuminated.

Or gate $F 2503$ permits the low-true third word transfer of either Computer $A$ or Computer $B$ to strobe the F18 magnitude comparator which compares the message DSA with the 3 bit code from encoder F21. When the front panel Data Set Select switch is in the 1 through 7 position the associated 3 bit code will be compared in the comparator with the message DSA address. In the Any position of the selector switch, the GS output of the encoder is high true and the Data Set selection basis is disqualified because the high true output always enables the storage logic through gate F2301. The 3 lower order CANTA bits are loaded into 74160 counter $F 20$ by the 1 Mhz clock when the or of 2nd Wd Load $A$ or 2 nd $W d$ Load $B$ is low true. Since flip flop E29 is low the counter is loaded but does not count as the Cep and Cet are low; thus counter $F 20$ acts as a static memory which is loaded with the 3 low order DCS address bits of the message. These bits are used to select one of the 8 latch bits in the 9334's via the address lines of the chip. The high order CANTA bits select the appropriate 9334 chip via the 74155 decoder and the XFER A, XFER $B$ terms from the Mother May I logic of Sheet 8, (Section 3.3) select the Computer $A$ or Computer $B$ memory via the enable of flip flop E29 and the mother-permitted $A$ or $B$ enable. The low-true output of a decoder line is combined with the low true output of flip flop E29; only one of the four 7486 outputs will be low; this will select the appropriate 9334 chip which will have a zero written into the addressed bit because the 9334 data input is a low.

The memory clearing process is radically different from the loading process. Every 16 cycles of $Q Q$, (from Sheet 7) flip flop E29 is cleared which permits counter $F 20$ to count up to 8 because the counter Cep and Cet inputs are high. In counting to 8 all the address states 0 through 7 are traversed. How are the 9334's enabled? Decoder E10 is disabled and all outputs are high; flip flop E2905 is high too so the 7486 outputs are all low so that each 9334 chip is selected. The 9334 data inputs are high because gates F1903 and F1906 are disabled; this causes a 1 to be written into each latch as the addresses sequence through the 0 through 7 states. At the count of 8 in counter F20 gate 525 strobes flip flop E29 to the set state which returns the memory load logic back into the load mode.

PARITY ERROR DISPLAY.$- \quad$ The Mode1 C and B Parity Error Display Logic is identical; see the discussion above.

### 3.9 MONTY AND BACCHUS COMPUTER INTERFACES

The function of this logic is to interface the SLC to the control computers memory via the DMP (Direct Memory Path) channels.

The interface logic has been implemented on wire-wraped Modcomp General Purpose $1 / 0$ interface boards which are installed in a Modcomp Peripheral Interface Chassis in the computer main frame. These interface boards are supplied by Modcomp pre-wired with logic to interface with the computer's $I / O$ bus. The user must add the appropriate logic for the particular interface application. The SLC Interface particularizing consists of I/O device and priority selection, a Command Word buffer register, handshaking logic, strobes etc. There are two versions of this logic which principally differ in the physical layout of the chips on the interface board; in addition, there are minor differences in the composition of chips. The first interface was built in 1975, the second in 1978. In the interval between the designs, Modcomp redesigned the interface board layout and discontinued the older board. The chip locations referenced in this discussion are those of the Bacchus Interface; to correlate the discussion with the Monty interface substitute the equivelent Monty chip locations.

The description in this section is restricted to aspects of interfacing the Modcomp-provided logic terms with the SLC; a general treatment of Modcomp interfacing is beyond the scope of this manual.

The Command word and Monitor Data words interchanged between the computer and SLC are handled by a Modcomp Direct Memory Channel (DMP) channel. A DMP channel is I/O logic which causes blocks of computer words to be input or output directly from memory without direct word-by-word involvement of the CPU. The monitor data block consists of 1152 words ( 384 ea 48 bit monitor data messages) and the command block consists of a variable number of command words up to a total of 384 words (128 ea 48 bit command messages).

There are three functions performed by the Interface logic: .. 1) initialization of the of the Interface and DMP channel by a TRANSFER INITIATE instruction; 2) transferring blocks of 16 bit words into and out of the computer via the DMP channel; 3) enabling SLC and Interface status to be read by the M\&C Driver program via direct $I / O$.

When the M\&C driver performs a TRANSFER INITIATE an Interface select flip-flop is set; this select term is an enable for the word transfers.

The TRANSFER INITIATE instruction causes a word count to be set
into the DMP channel word count register and an initial memory address to be set into the DMP channel memory address register.

As each word is input or output via the DMP channel the word count is decremented and the DMP channel memory address register is incremented; when the word count is zero the DMP channel logic issues a Service Interrupt to signal completion of the block transfer.

The computer M\&C driver operations must be properly synchronized with the SLC logic operations to perform block transfers. To accomplish this synchronization the M\&C driver program reads Interface and SLC status discretes through direct I/O status read logic.

Two .SLC discretes, SLCCMD and SLCMON control the transfer direction and enable block transfers; the Interface generates a Service Interrupt to signal the M\&C driver when these terms go false.

One of the requirements of an $I / O$ bus which is wired to more than one interface is that there must be interface priority arbitration logic to resolve contentions between interfaces in the event that two interfaces concurrently attempt to use the bus. In the Modcomp DMP logic this is done by enabling interfaces to raise a line in the $I / O$ bus data lines which may be tested by other interfaces when they attempt to perform a DMP transfer. The interface priority decode logic is on Sheet 1 ; the signal TUHPRI is derived from or-gates which would be wired to the $1 / 0$ bus data lines to sense the priority of other interfaces. Since the SLC interface is configured for the highest priority none of the or-gate inputs are wired to the $1 / 0$ data lines.

Before we discuss the details of the Interface logic operation the functions performed on each sheet of the logic diagrams are briefly as follows:

The Direct $I / 0$ Device Decode logic is on the right side of Sheet 1 ; the device address is $O F$ (hex) and forms the TUISEL (this unit is selected) signal. The logic on Sheet 1 is all standard Modcomp logic; there are no SLC-peculiar features.

Sheet 2 contains the Source ID code enabled by TUISEL. This logic is standard Modcomp logic; there are no SLC-peculiar features other than the encoded Source ID.

Sheet 3 contains command decode logic; there is no SLC-peculiar logic on this sheet. The terms buffered on this sheet are general control terms associated with inputting, outputting, terminating, selecting etc and are used as required for the interface application. Terms from this sheet are used as inputs on SLC-particular logic on other sheets, (mostly on Sheet 7).

Sheet 4 contains a 16 bit temporary storage buffer for SLC command words. The register is clocked by a BFRSTR1 term from Sheet 7. The direct clear term is not used. Since the I/O bus parallel data is available for only a short period, the data is latched to provide an adequate sampling period for the SLC logic.

Sheet 5 contains a 16 bit optical isolator array to terminate the Monitor Data lines from the SLC. The isolator outputs drive the computer $I / O$ bus via the and-or gates.

The gates enabled by the ENISO1 term are Direct $1 / 0$ status read gates; these permit the computer to direct-read SLC and Interface status. These bits are:

ISLM06 - The SLC/Interface busy (ie Interface is in the CMD or MON word transfer mode)
ISLM15 - The SLC is in the CMD word transfer mode.
ISLM14 - The SLC is in the MON transfer mode. (This term is stretched by the SLC and is about 60 usec longer than the actual period in the SLC.)
ISLM04 - Memory Parity Error (not an SLC function).
ISLM07- The SLC interface has been selected. (ie controller busy)

In the Monty interface all other ISLMXX inputs are grounded to produce logic zeros when the status is read. This is not the case for the Bacchus interface.

Sheet 7 contains the bulk of SLC-particular logic. The functions performed by the logic on this sheet are hand-shaking with the SLC and initiation of DMP channel word transfers, transfer direction control and generation of a Service Interrupt to signal the end of the SLCCMD and SLCMON periods.

The first step in performing a DMP block transfer is to select the SLC Interface by setting the Select FF XVSK05 (Sheet 7) by a TRANSFER INITIATE instruction. Executing this instruction activates the TRANST line, (Sheet 6, XUSA12). This instruction also sets the CMD/MON mode FF XVSK5 to the Mon or Cmd mode which ensures that the M\&C driver program is properly synchronized with the SLC mode. This CMD/MON FF controls the direction (ie input or output) of the word transfers by the direction steering input to XU4B06 on Sheet 6, (see the discussion below). The SLC driver program may check this synchronization by reading the state of the SLCCMD and SLCMON discretes, (ie ISLM14 \& ISLM15). If the SLC driver mode is not properly synchronized to the SLC mode the DMP transfer sequences will not occur because of the disparity between the two mode enables on the command word gate XV5H08 and the monitor word gate XV5H06. The select flip flop is cleared by the EOSEQ term described below.

Flip flop XV5K05 is the CMD/MON mode control flip flop; it's outputs are used to enable command or monitor word transfers via gates XV5H08 and XV5H06 respectively.

The block transfers are terminated by the DMP channel when the word count $=0$; the channel activates the TERMN line.

The term ISLM06 is the logic sum of the SLC command and monitor modes; when this term falls at the end of the SLCMON and SLCCMD periods it generates the EOSEQ term to cause a STSIRQ (Set Service Interrupt Request) to signal the completion of an SLC transfer period. The M\&C driver must know when these periods end in order to properly set up the next block transfer sequence. ISLM06 is also a status bit which may be read by the M\&C driver..

The simplified timing diagram on the next page illustrates the DMP block transfer mode timing.

SLC INTERFACE DMP BLOCK TRANSFER TIMING
Time
SLC Cmd
Mode
SLC Mon
Mode
XV5T6
One-shot
XV5M8
FF
SLCCMD
ISLM14
XV5M6
ISLM15
XV5M5
ISLM06
XV5J6

DONLIN via optical isolator XU4G14 through one-shot (to make a strobe) XU3G10 and gate XV5H06 to activate DATARS (discussed below) through gate XV2R06. The acknowledgement to the SLC is the IGOTIT term from gate XV2NO3 which is driven by the INDCMN (for input data command) from Sheet 3. The DONLIN terms from the SLC go true every 16 usec and the response time of the Interface and DMP channel is about 6 usec ; thus the three word components of a monitor data message are input to the computer in a 54 usec period and the interval between the message bursts is 59 usec . Monitor word transfer timing is discussed in Section 3.4.

The term BFRSTRI is generated by gate XV2P08 which is driven by the OUDCMN term from the command decode logic on Sheet 3. BFRSTRI is the strobe that loads a 16 bit command word into the buffer register on Sheet 4.

Sheet 6 contains the DMP synchronization logic which is mostly standard Modcomp logic with a little SLC particularizing. The encoder on the upper right generates codes used for Source ID during DMP transfers. The low-true ID codes are as follows:

Monitor Data Input (computer Read): 000111 (DMP Channel 7)
Command Word Output (computer Write): 010111
Service Interrupt: 011111
The following description of DMP operations was abstracted from a Modcomp manual:
"A DMP request is generated by signal DATARS (Data Request). This signal sets FF XU4C05. Output of XU4C06 goes to one of the three inputs on or gate XU2A08. If FF XU4A06 is not set and there is presently not a DMP Update Queue on the line, DMP request FF XU4C09 will be set. DMP Request is sent to the CPU, and FFXU4A05 will be set on the first clock following the set of the request FF . This transfers the data request into FF XU4C09 and resets FF XU4C05 through and gate XU5F11 and or gate AXU5B12. When the Update Queue is received, signal DMPRQN is sent to Sheet 1 to put the priority bit on the bus. If this unit has the highest priority, the Source ID bus is enabled. The direction of data flow, whether input or output, is determined by gate XU4B06. Pin 5 of $\mathrm{XU4B}$ B 06 is tied to a signal that indicates output. If XU4B06 is low, this will put Source ID on the bus for output. If $\mathrm{XU4B06}$ is high, this will put Source ID on the bus for input." The input to XU4B06 is CMDMOD; this signals that the output mode is requested. During monitor data transfers CMDMOD is low.
"If this unit is highest priority, and data request FF XU4C06 is set, the $D$ input of $F F$ XU4A09 will be enabled so that on the trailing edge of Update Queue FF XU4A09 will be set providing the signal ENZERO which goes to Gate XU4E08 as an enable. Also, on the trailing edge of Update Queue if this unit is highest

```
priority, DMP request FF will be reset. If this unit is not
highest priority, DMP Request will remain set until this unit is
highest priority. FF XU4C09 will remain set until there is a
request and a Data Request is not made or an initialize DMP
occurs. FF XU4A09 will remain set until a DMP Request occurs
without a Data Request. A terminate will be generated
automatically when the word count reaches zero. A terminate will
be generated with an address of zero. This allows any Data
Request or DMP Request in process to be reset. This is
accomplished through gate XU4E08, which is address zero, and
ENZERO FF is set. This produces signal ADDZEN (Address Zero)
which goes to Sheet 1, (or gate XU1C08) to produce TUISEL.
Output XU4E08 is inverted by XU4F04 which goes to gate XU5F03 to
be and'ed with signal TERM. The output of XU5FO3 goes to or gate
XU5A08. The output of XU5A08 goes to FF XU4C05 as a reset and also goes to DMP Request FF XU4C05 as a reset."
A graphic description of the input/output logic sequence is shown on the next page:
```

Word transfer sequence:

command and monitor discretes have gone false.
"The DMPSRS term is used to generate a DMP Request at the time of the Service Interrupt request. This request is used to store the transfer address. FF XU4D05 is set by DMPSRS, and output XU4D06 goes to or gated XU2A08. If there is no DMP in progress (output of $X U 4 A 05$ ) and there is presently not a DMP Update Queue on line, then DMP Request $F F$ XU4G15 is set. The first clock after request $F F$ is set causes $F F X U 4 A$ to be set. The output of XU4AA05 transfers the store transfer address to FF XU4D09, and also through gate XU5F08 and or gate XU5A06 FF causes XU4D05 to be reset.

When Update Queue is received, signal DMPRQN is generated and sent to Sheet 1 to allow the priority bit to be put on the bus. If this unit is highest priority, the source ID is enabled to be put on the bus by gate XU5B06. The correct ID is provided by output of FF XU4D08. The output goes to two or gates, XU4B08 and XU4Bll. On the trailing edge of Update Queue and this unit is highest priority, DMP Request $F F$ will be reset. If this unit is not the highest priority, DMP Request will stay set until this unit becomes highest priority. The first clock after DMP Request causes FF XU4A05 to be reset. FF XU4D09 (Store Transfer Address) will be reset when the next request is made and $F F$ XU4D05 is not set."

A graphic description of the $S I$ and terminate process is depicted on the next page:

```
Service Interrupt and Terminate logic:
    SLCMON fall or .............-.-.- Set SIREQ to CPU
    TERMN from CPU
        Set FF XU4D05 <-- SIRSTEN from CPU
                                |
    .....> DMP in process ?
    |_........, yes /, \no
                DMP UD Queue <--.
                    active ? |
                    no / \ yes -.....
                    /
            set DMP Req
            FF XU4G15
            I
            set XU4A05
                        |
            XU4A05 causes
            Store Transfer Address
                I
            reset XU4D05
                I
CPU issues -.--> highest priority ? <--.
UD Queue
    yes // \no l
    Enable Source ID
            |
    reset DMP Req FF
        |
    reset XU4A05 FF
        |
    reset Store Transfer
    FF XU4D09
```

```
4.0 List of Major Drawings
SLC Model B Functional Drawings
\begin{tabular}{ll} 
F13720L46 & Model B Logic Diagram \\
A13721P65 & Model B IC Location Map \\
C13720B08 & SLC Block Diagram \\
C13721P67 & Models B and C Front and Rear Panels
\end{tabular}
SLC Mode1 C Functional Drawings
\begin{tabular}{ll} 
D13720L78 & Model C Logic Diagram \\
A13721P66 & Model C IC Location Map \\
C13720B08 & SLC Block Diagram \\
C13721P67 & Models B and C Front and Rear Panels
\end{tabular}
SLC Fabrication Drawings
\begin{tabular}{ll} 
D13721P24 & SLC Assembly \\
A13721Z48 & SLC Model B \& C Bill of Materials \\
D13720W48 & SLC Wiring Jig \\
Al3720N10 & SLC VLA Fabrication Specification \\
A13720W65 & Master Wire List, Model C \\
A13720W67 & Machine Wire List, Model C \\
A13720W66 & Hand Wire List, Model C \\
A13721P15 & SLC Model B Logic Connector Board Ass'y \\
D13720M66 & Top \& Bottom Panel \\
D13720M64 & Front Panel \\
D13720M63 & Left \& Right Side Panels \\
D13720M65 & Rear Panel \\
D13720M67 & Power Supply Mounting Panel \\
C13720M68 & Card Mounting Rail \\
C13720M70 & Wiring Mount \\
C13720M69 & Spacer, Board Mounting \\
D13720AB26 & Front Panel LED Display PCB Artwork \\
D13720M71 & Front Panel Display PCB Drill Drawing \\
D13721P25 & Front Panel Display PCB Assembly Drawing \\
& \\
A13721247 & Front Panel LED Display Assembly Bom \\
C13720AAl3 & Rear Panel Silkscreen Artwork \\
C13720AA12 & Front Panel Model B) Silkscreen Artwork \\
A13720W91 & SLC Modcomp Computer Cable Wire List \\
Monty Interface Drawings
\end{tabular}
D13720L01 Logic Diagram
C13720P01 Interface Assembly Drawing (Monty)
B13720P1 Dip Header Assembly, Optical Isolator
Bacchus Interface Drawings
D13720L60 Logic Diagram
```

B13720P1 Dip Header Assembly, Optical Isolator
5.0 Special Module Data Sheets

The SLC Power Supply manual follows:

# OEM SERIES POWER SUPPLY MODULES 

## INSTRUCTION

 MANUALacde electronics inc. OCEANSIDE, CALIFORNIA

INPUT: $105-125 \mathrm{VAC}, 47-63 \mathrm{~Hz}$ (Useable also at 400 Hz ; consult factory for derating.)

OUTPUT: Voltage is adjustable between limits by externally accessible screwdriver adjustment of a potentiometer. Output is floating; either positive or negative terminal may be grounded. Current: Zero to full load.
Adjustment range: $\quad 4-8$ Volt Models $\pm .25 \mathrm{~V}$
$10-18$ Volt Models $\pm .5 \mathrm{~V}$
20-32 Volt Models $\pm$ IV
Note: Voltage and current are coded by model no. Example: OEM5N5.7 is a 5 volt supply with a maximum current rating of 5.7 amp at $40^{\circ} \mathrm{C}$.

REGULATION: $\quad 0.1 \%+5 \mathrm{mV} \mathrm{NL}-\mathrm{FL}, \pm 0.1 \% \pm 5 \mathrm{mV}$ for $10 \%$ input change.
RIPPLE: 2 mV RMS max., 20 mV P-P max.
STABILITY: Typically 10 mV for eight hour period after initial warmup.
TEMPERATURE: $0.02 \% /{ }^{\circ} \mathrm{C}$ max.
COEFFICIENT
OUTPUT: DC-IKHz: $0.001 \mathrm{R}_{\mathrm{L}}$ or 0.005 ohm max.
I MPEDANCE

TRANSIENT: Output voltage returns to within regulation limits within
RESPONSE 50 usec in response to a $50 \%$ load step.

REMOTE: Terminals are provided to maintain regulation at the load, SENSING compensating for the $D C$ voltage drop in the load cable.

REMOTE: Output voltage may be remotely adjusted over a limited range VOLTAGE by insertion of a variable resistor in the positive sensing line.
ADJUSTMENT
OVERLOAD: Inherently protected against overload and short circuit by a PROTECTION

OVERVOLTAGE: PROTECTION (OPTIONAL)

AMBIENT: Operating; 0 to $71^{\circ} \mathrm{C}$.
TEMPERATURE Storage: -50 to $85^{\circ} \mathrm{C}$

## SPECIFICATIONS - OEM SERIES



GENERAL NOTES
tme overlono ano overvoltage aduustments are consioeped
FACTORY AONUSTMENTS. DO NOT MKEE NYY ADUUSTIENT WITHOUT
CONSULTING FACTORY.
if ove rvoltace protection is included a line fuse shoulo aE installeo ey the user for protection against catastromic fallure.

COMMON APPLICATION PROBLEMS
no output : NO AC input, oeftetive lime fuse, offrut shorteo,
IOU OUTPI INCOMAECT HOON UP.
Low OUTPII: Excessive lond cindent. overvoitace operatimg. OUTPUT VOR TMCE MAUUSTED TOD HIOM, OPEN SENSE
HIOH OUTPUT: LEREN SENSE LEADS.
to rectcle oveavoltace protection, the ac input must ee remoned TOR APPROXIMTELY 2 SECOMOS MO TIEN REAPPLIED.

Case R1 \& R2

se R4 \& R5


## Case R3



Dual Modules R1 \& R2

(1) This mounting pattern is repeated on opposito side for a total of 5 possible mounting faces.
Note: All mounting holes have threads to recoive \#82 scrows.
(1) Provide clearance holes as required for screwheads on this surface.



FIGURE I: CONTINUED


FIG. 2
ANTENNA TIMING OPERATIONS


FIG. 3
CENTRAL TIMING OPERATIONS


DATA REQUEST MESSAGE FORMAT, " 0 " CHARACTER 1010010100
figure a: data set command and monitor data and data request message formats
































$\qquad$ $6 \quad 1 \quad 5$ $\qquad$












| $V$ $S L C$ <br> $A$ MODEL <br> $A$  | NATIONAL RADIO ASTRONOMY OBSERVAIORY |  |
| :---: | :---: | :---: |
| SERIAL line controller I.C. LOGIC ASSY and DETAILS | -एगent | \%ition |
|  | वुदctoo | 045 |
|  | aroon | , |
| spore | ETFG5 an | K4.4 |



loc: A.3

loc:121,22.23



1.C. LOGIC ASSY (Scrub Brushes)

POWER SUPPLY



