VLA Technical Report No. 64

Synthesizer Control Module, Type L16

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"The untold story of the FLUKES in the VLA System."

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1.0 INTRODUCTION

This manual describes the operation of the Model B Synthesizer Control module, type L16. Functional and detailed circuit analysis serve as a troubleshooting guide in performing corrective maintenance actions. Pertinent component data sheets, assembly drawings, Bill of Materials, etc provide further maintenance information and construction data should additional L16's (over the existing ten units) be someday required.

The System Overview (Sect 1.2) presents a brief description of the synthesizer portion of the Master Local Oscillator (MLO) system, the generation of LO's A, B, C, D, and the differences existing between the two synthesizer systems in Racks MT-1 and MT-2. This is presented to place the system in proper context and thus offer the role. purpose and design considerations of the L16's in proper perspective.

1.1 PURPOSE

The Synthesizer Control Module L16 provides the Monitor and Control interfacing required for remote frequency tuning and monitoring of the Model 6160B Fluke Synthesizers by the Central Computers via the DCS System. The four primary functions of the L16 are:

a) Formatting standard DCS serial command data into the 36 bit parallel "latched" tuning commands required by the Fluke Synthesizers for remote operation.

b) Command "echo" readback for command word verification.

c) Real-time 9-digit frequency counter of the Synthesizer RF output for both local display and DCS monitor data.

d) Various status and error monitor reporting.

The Command Echo and Frequency Counter data is used by the MODCOMP Control Computers to confirm proper tuning of the Flukes as a result of the most recent commanded frequency to ensure proper operation of this segment of the MLO System. In Spectral Line and Polarization mode observations., proper setting of the four Flukes, within 2 Hz, is of paramount importance as this establishes the final IF-to-baseband conversion prior to correlation.

There are eight Fluke Synthesizers and associated L16 modules, one for each Fluke, physically located in Racks MT-1 and MT-2 as follows:

Rack MT-1 contains four sets of L16's/Fluke Synthesizers, labeled Channel A, B, C and D. This is the primary local oscillator source for the VLA LO/IF System in the Central Electronics Room. The Fluke RF outputs are routed through their respective L16, sent to power dividers in Rack MS for equal distribution to the MLO electronics in Racks M-1 and M-2, with RF relays in Rack MS selecting either Rack M-1 or M-2 as the "Master" LO System. Rack MT-1 also contains Data Set 3 (DCS-0) serving the L16's in both MT-1 and MT-2 racks.

Rack MT-2 contains four sets of L16's/Fluke Synthesizers, labeled Channels AA, BB, CC, and DD to distinguish these four channels from MT-1. This rack serves the dual-role of providing the local oscillator signals required by the VLBA observing equipment plus as a ready backup for the VLA in the event of a Rack MT-1 failure. Additionally, Rack MT-1 Flukes can be selected by various VLA antenna D-Racks as an alternate source of LO for split-IF operation. The L17 Synthesizer Phase Lock modules and associated electronics are identical to the Rack MT-1, M-1/M-2 arrangement, except these modules are physically located in Rack MT-2 to form a second, self-contained MLO system.

The Fluke Synthesizers in Racks MT-1 and MT-2 are thus both under computer control for remote frequency tuning and monitoring through their respective L16 control modules.

1.2 MLO/SYNTHESIZER SYSTEM OVERVIEW (Fig 1)

The VLA antennas provide four IF channels of astronomical data, called IF's A, B, C, and D, each being 50 Mhz in bandwidth. In Continuum Mode, the distributed power across the 50 Mhz band is of interest. In Spectral Line Mode, a specific frequency of much narrower bandwidth, located within the 50 Mhz IF, is the signal of interest with all other signals to be rejected. In Polarization Mode IF's A and B contain right-hand circularly polarized signals, while IF's C and D contain the left-hand polarized signals. The role of the Central Electronics LO/IF system is to convert these four IF's to 0 - 50 Mhz baseband (video) analog data for the Samplers and Correlator in the Screen Room. This must be accomplished to accomodate the desired mode (Continuum, Spectral Line, Polarization) while preserving the phase characteristics of the signals within nano-second accuracy.

These four IF's emerge from the T1 Modems in the 1.3-1.7 Ghz passband with the same spectral distribution as they left the antenna. Two levels of conversion follow, both being performed by the Baseband Converter module, type T3. Conversion to UHF occurs by mixing IF's AC with 1200 Mhz to produce 200-250 Mhz

while IF's BD are mixed with 1800 to produce 200-250 Mhz. To accomplish the final 0-50 Mhz conversion, the LO signals must mix with these two ranges to produce IF's with a center frequency of 25 Mhz, being half the bandwidth. LO values would thus be 125 Mhz and 225 Mhz, and indeed these values are used for Continuum Mode baseband conversion when the full 50 Mhz bandwidth is desired. However, for Spectral Line Mode, it is desireable to be able to select any portion of each of these four IF passbands as the center frequency and filter out narrower bandwidths for increased selectivity and reject unwanted signals. The resultant narrow bandwidth signal coincides with the precise spectral-line of interest. For this reason, the local oscillator required for the final IF-to-baseband conversion must be variable in frequency. Slewing the center frequency along the four IF passbands to match the various bandwidth filters is the primary function of the four Fluke Synthesizers; a tunable LO in the ranges of 100-150 Mhz (for If's AC) and 200-250 Mhz (for IF's BD) in 2 Hz steps under computer control.

The UHF converters in T3 produce composite IF AC being upper side band (USB) and IF BD being inverted lower sideband (LSB) as a result of the 1200 and 1800 Mhz LO. Considering IF AB, the composite signal is applied to two USB-rejection mixers so that the desired sideband is selected and the unwanted image substantially rejected. Mixer outputs are the 0-50 Mhz baseband desired, with Fluke Synthesizers A and B being the LO source (indirectly). In a similar manner, IF's CD are applied to USB-rejection mixers, producing two baseband outputs, Fluke C and D being the LO source.

The four A, B, C, D basebands are amplified and sent to Baseband Filter modules, type T4, one for each IF, where the final analog filter to establish the desired bandwidth, down to 0.098 Mhz is accomplished. Filter selection is under computer control using pin-diode switches to select one-of-eight octave step filters. Filter select commands are decoded and distributed to the proper filter modules for Baseband Control Module T6C, one for each antenna/D-Rack. The pin-diode arrays and filters are in the T4 Baseband Filter Modules, whose output are further amplified by Baseband Drivers, type T5C, and sent to the Samplers in the Correlator Room. The T5'C, one for each IF, also generates the ALC used by the Samplers for level control. Thus through the actions of the Fluke Synthesizers and Baseband Control and Filter modules, precise center frequency tuning and selectable bandwidth filtering is accomplished and coordinated under computer control via the DCS System. The Flukes/L16's are serviced by DCS-0, Data Set 3 and the filter selection through Data Set 5 of the associated DCS Channel.

The output of the Fluke Synthesizers are not sent to the four T3 Converter modules (per antenna) directly. The outputs are processed by Synthesizer Phase Lock modules, type L17, one for

synthesizer pair AC, another for pair BD, to ensure these LO pairs are phase-locked to the MLO to support polarization mode observing. In polarization mode, IF A is the RH polarization signal, with the corresponding LH polarization signal being IF C. Note the sum difference between A (100-150 Mhz) and C (200-250 Mhz) is always 350 Mhz. Polarization analysis requires the phase coherence between A (RH pol) and C (LH Pol) signals to be maintained within a fraction of a cycle with a 350 Mhz +/- 2 Hz sum difference. To preserve this phase, the local oscillator signals AC must likewise be properly phased. The same is true for IF B (RH pol) and D (LH pol) pairs.

The Synthesizer Phase Lock modules L17 perform two major functions:

1. Since the Fluke Synthesizers can not tune above 160 Mhz, and LO's B and C must be tunable over 200-250 Mhz, the L17 performs the frequency doubling required to LO B and C. The Flukes are tunable with a 1 Hz accuracy; however this accuracy is multiplied to +/- 2 Hz through the frequency doublers. LO signals A and D are not modified by their respective L17's.

2. LO AC phase locking is performed by a portion of the A and 'Cx2 signal being applied to a mixer to produce the 350 Mhz sum signal. Phase referenced 50 Mhz is multiplied x7 by the L17 to form a 350 Mhz reference. This reference and the 350 Mhz AC sum is compared, the resultant difference an error signal driving a 5 Mhz VCXO phase-locked oscillator loop. This phase-locked 5 Mhz is sent to the "A" Synthesizer as the external 5 Mhz reference.

(The L17 for channels BD functions in an identical manner).

The B and C Fluke Synthesizers receive 5 Mhz external reference from the MLO system (un-locked), while the A and D Flukes receive their external 5 Mhz reference from the phase adjusted 5 Mhz output from their respective L17's. Any phase difference occurring in either the AC or BC Synthesizer pair output, or in the external 5 Mhz Synthesizer reference, will produce a 350 Mhz phase error signal in the L17. The action of the phase-lock 5 Mhz VCXO will immediately compensate for the phase to null the error. Thus, even though separate synthesizers are used to generate four tunable LO's, the AC and BD signals to the T3 Baseband Converters are always maintained at the 350 Mhz +/- 2 Hz sum difference with the phase relationship always known. This scheme also virtually eliminates all relative phase noise and spurious mixer products.

The outputs from the L17's, A, Bx2, Cx2, and D, are amplified by Variable Frequency Driver module L18. In VLBI Rack MT-2, the L18 outputs feed the various distribution loads directly. In Rack MT-1, the Fluke synthesizer output are split by power dividers and suppplied to two sets of L17's simultaneously; one

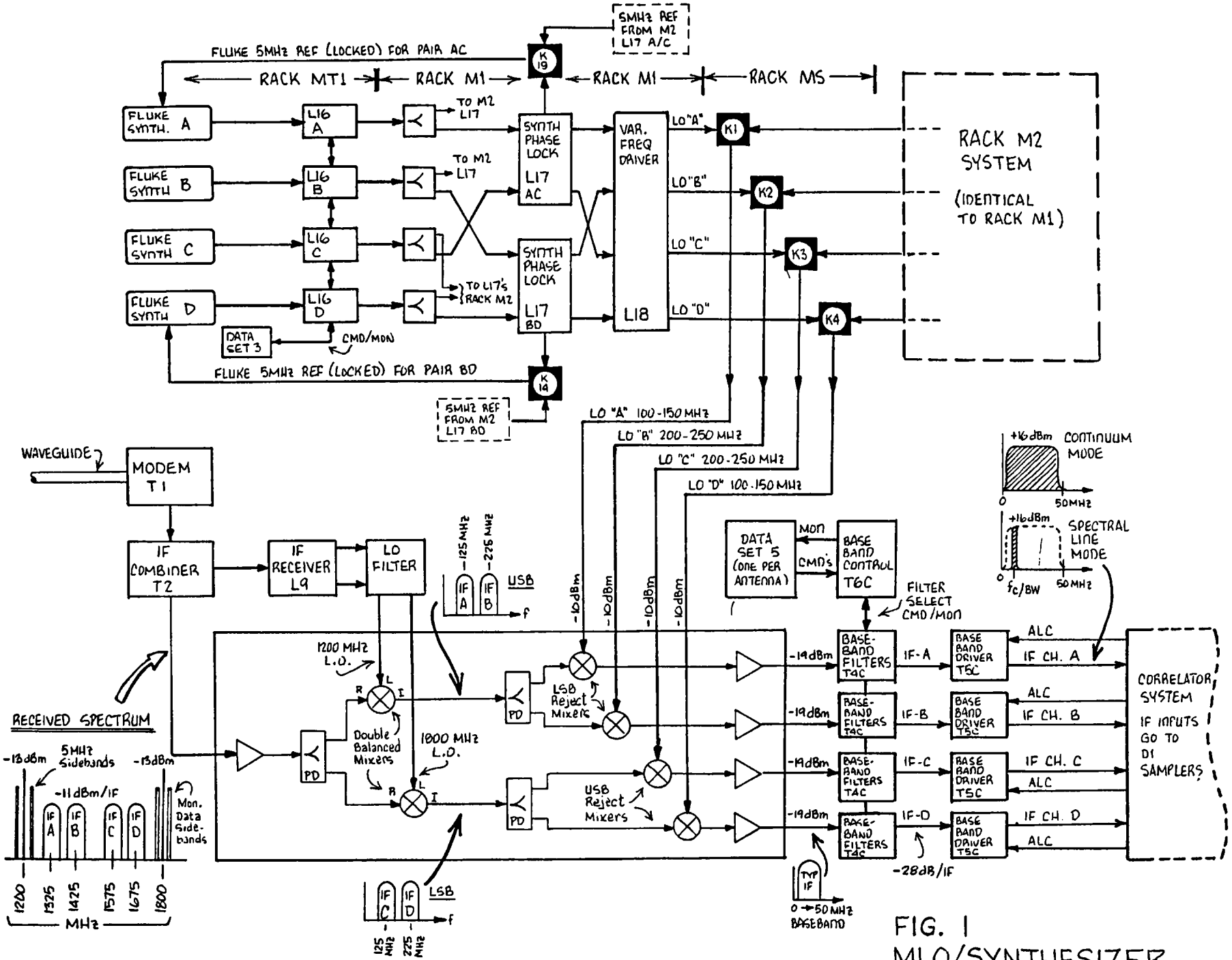


FIG. 1
MLO/SYNTHESIZER
BLOCK DIAGRAM

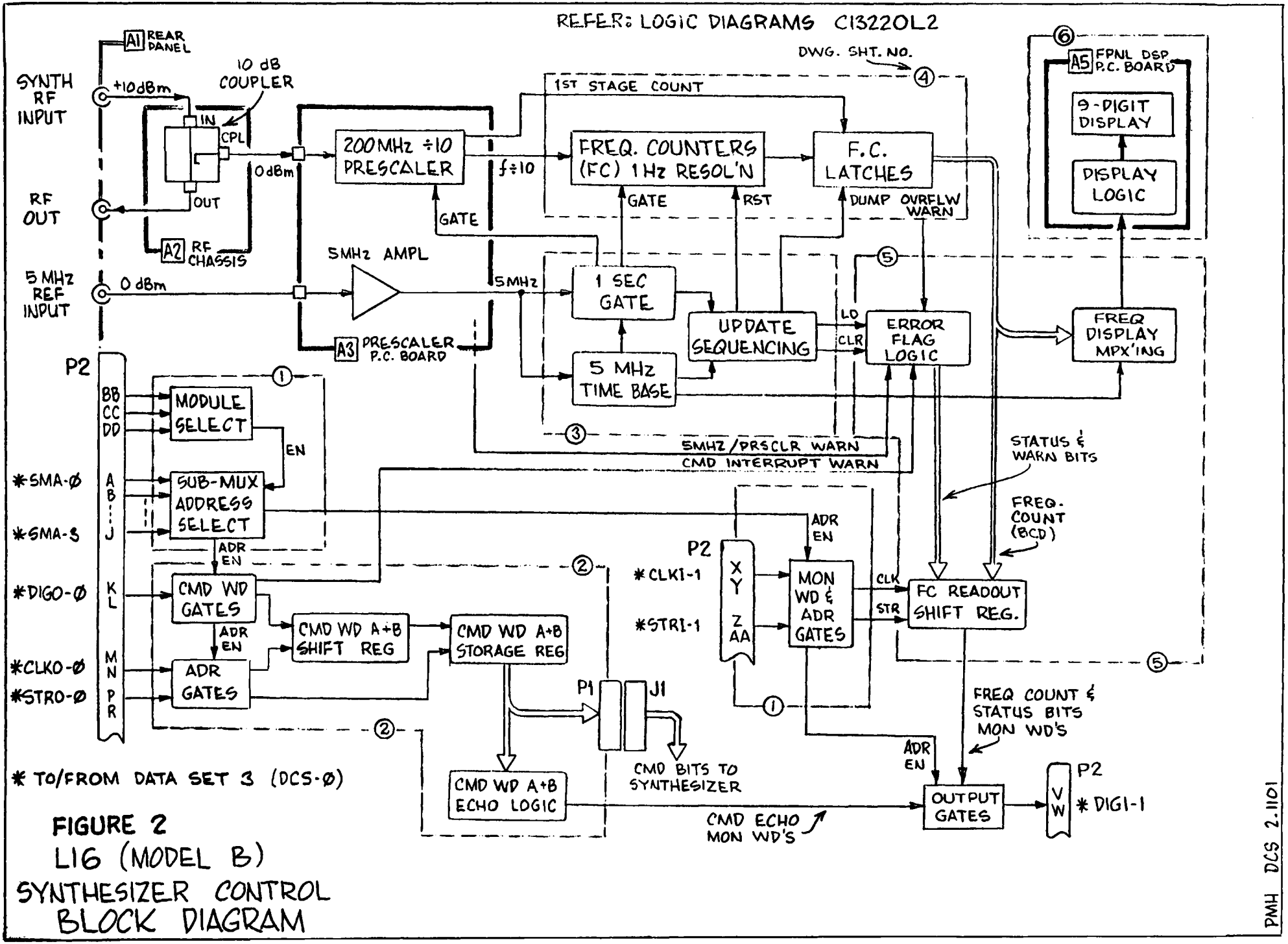


FIGURE 2

L16 (MODEL B)
SYNTHESIZER CONTROL
BLOCK DIAGRAM

PMH DCS 2.1101

set in M1, another set in Rack M2. The outputs of the L18 Drivers in both M1 and M2 Racks are inputs to RF relays. Both M1 and M2 racks are processing the Synthesizer signals, with all L17's "locked up". The RF relays determine which system, M1 or M2 is used for the "on-line" MLO. Relay outputs of LO's A, B, C, D, are sent to power dividers for distribution to each D Rack/T3 Baseband converters. The "off-line" rack LO signals are terminated into 50 ohm loads by the relays to simulate system loading.

2.0 BRIEF FUNCTIONAL DESCRIPTION (Fig. 2)

This section presents a brief functional description of the logic and circuitry of the L16, with the sub-sections organized by the primary functions of the module. Detailed circuit analysis for troubleshooting is in Section 3. See Figure 2.

2.1 MODULE DCS ADDRESSING

There are eight 116's serviced by DCS-0, Data Set 3. The Command and Monitor Sub-mux addresses (SMA's) are listed below:

	MT-1 Rack L16's				MT-2 Rack L16's			
Channel -->	A	B	C	D	AA	BB	CC	DD
Commands:								
Synth Cmd Wd A	320	322	324	326	340	342	344	346
Synth Cmd Wd B	321	323	325	327	341	343	345	347
Data Set Cmds:	DIGO-0	CLKO-0	STRO-0		DIGO-1	CLKO-1	STRO-1	
Outputs Mon:	DIGI-0	CLKI-0	STRI-0		DIGI-1	CLKI-1	STRI-1	
Monitor Data:								
Cmd Wd A Echo	220	222	224	226	240	242	244	246
Cmd Wd B Echo	221	223	225	227	241	243	245	247
Synth Freq (1-100Mhz)	230	232	234	236	250	252	254	256
Synth Freq (1-100Khz)	321	233	235	237	251	253	255	257

The command and monitor addresses shown above are selected by the states of the four SMA lines during the proper command or monitor time of the Data Set. The LSB (SMA-0) and MSB (SMA-3) specify the proper function within the L16 (i.e., whether the MSB or LSB of the command or monitor word), while address lines SMA-1 and SMA-2 identify the proper L16. Coding is provided by hard-wiring of the bin connector, which "programs" the L16 response address and illuminates the proper ID LED on the front panel. The SMA lines and the monitor and command data, clock and strobe lines are daisy chained to all eight L16's, with only one module responding as a result of this channel address coding.

2.2 COMMAND PROCESSING

The Fluke Synthesizers require a steady-state 34-bit parallel TTL command word for remote tuning. This word is eight BCD (32 bits) defining the 1-Hz to 10 Mhz digits, a 100 Mhz bit, and a 1-12 Mhz or 10-160 Mhz range bit. This 34 bit tuning command is derived from two DCS 24-bit serial commands from the Data Set. The commands are serially loaded into shift registers by Data Set terms DIGO (data), CLKO (load clocks) and STRO (terminating load strobe). The load strobe stores the command into a latch for static storage. This latch, requiring two serial commands to specify the full Fluke Synthesizer command, is sent to the Fluke remote frequency command connector. The latch output is also loaded into a paralel in/serial out shift register for command echo readback to accomplish a bit-for-bit verification that the frequency command was correctly received. The storage latch is used to store the tuning command for long periods, as Fluke tuning commands are normally infrequently issued by the control computers only during source changes.

2.3 FREQUENCY COUNTER

To verify proper frequency setting of the Fluke Synthesizers over its useful range, a frequency counter is provided to match the 1 Hz resolution required. The Fluke +10 dbm output is routed through a 10 db coupler in the L16, providing 0 dbm of RF for the frequency counter stages. This coupled signal, in the nominal range of 100-150 Mhz, is applied to a divide-by-ten high speed ECL digital prescaler IC. The divide by ten ECL output is buffered to TTL and used to clock the following eight stages of TTL decade counters, enabled over a precise 1-second gating period. This forms a nine-digit frequency count to 160 Mhz (the maximum Fluke setting) in 1 Hz steps. The BCD count of the prescaler IC forms the least significantl-9 Hz digit, the subsequent stages forming the 10 Hz to 100 Mhz BCD digits. The frequency count is formatted for DCS monitor word readout and local LED display, as discussed in 2.5 and 2.6.

2.4 1-SEC. GATING AND TIME BASE

The time base is driven by an external 5 Mhz sinusoidal signal from the MLO system, 0 dbm nominal, which is converted to a TTL clock by an LM 360 differential comparator. The time base establishes the 1-second gate period and provides clocks and discrete timing terms to the update (housekeeping) and LED multiplexed display logic. The 5 Mhz clock is applied to seven stages of TTL decade counters producing a 1-second terminal count used to clock the GATE flip flop OFF. When GATE is off, the frequency counter is halted, a binary counter is enabled to sequence through the various update terms to latch the frequency count, and upon completion, clocks the GATE on to begin another 1-second counting period. Display multiplexing is pulled off the

10 Khz stage to form the LED scanning terms.

The time base is basically free-running during both the 1-sec. count period and the 10 usec update period, synchronized to a count of zero at the end of the update cycle. Synchronization to "re-start" the time base to the 5 Mhz external input ensures a consistent gating period to compensate for propagation delays reducing frequency counter inaccuracies due to time base errors. Since a 5 Mhz one-half cycle error can easily cause a 10-Hz error in the frequency count, or a one-digit error. Synchronization keeps the count error within +/- 3 Hz and consistent to avoid last digit flickering.

2.4 UPDATE SEQUENCING

At the termination of the 1-sec GATE counting period, the frequency count is latched into registers to drive the local LED display and to be ready as monitor data when polled by the Data Set. Data Set monitor data polling (and command transmissions) are asynchronous to the L16 functions. Once the frequency count and flags are latched, the next count period is immediately commenced. A new tuning command is processed by the L16 and Fluke to "settle out" at the new frequency in less than a second. Keeping the update sequencing cycle at less than 10 usec between count cycles ensures that while the Fluke output is slewing to a new frequency, no more than two count cycles will be contaminated by an erroneous count; the third cycle will be stable for the control computers to read for new tuning command verification.

The update actions are as follows in the order of their occurrance:

1. HALT the GATE enable flip flop.
2. HALT the Prescaler IC counter, then remaining frequency counter stages.
3. LATCH the Prescaler 1-9 Hz count. (if no overflow)
4. DUMP remaining count stages into latches. (if no overflow)
5. LATCH flags (command interrupt, 5 Mhz OK, Prescaler warning, Overflow and frequency slewing.
6. RESET Prescaler IC and frequency counter stages to zero.
7. CLEAR error flags. (unlatched flags)
8. SYNC Time Base and start next count.

2.5 MONITOR DATA ACTIONS

Four monitor data words are polled from the L16 by the Data Set: 2 words containing the command echo and 2 words constituting the 9 digit frequency count and status flags.

Command echo monitor data is simply a parallel load shift register loaded by the Data Set load (STRI) term to read the contents of the tuning command register. Two DCS monitor words

are required to read out the 34 command bits and two status flags (Fluke power ON and local/remote mode switch). The MSB bits in one register are polled by the Data Set during one VLA waveguide cycle, the LSB's polled during the next cycle.

Frequency counter monitor data is formatted in like fashion; two 24-bit parallel-load, serial-out shift registers; one containing the status and 1-100 Mhz count; the second containing the 1 Hz-100Khz count. At the end of each count period, the frequency count latches are updated. The FC latch outputs are the parallel inputs to the monitor word shift registers, being loaded by the Data Set load (STRI) term to the register corresponding to the SMA address. Data Set clocks (CLKI) follow, shifting the count bits to the Data Set. When the Data Set polls either of the monitor word shift registers, a Monitor Data Interrupt term is generated that halts the update sequencer, if active, for the duration of the data shifting operation. Halting the update actions ensures the frequency counter latches will not be updated while actively shifting out monitor data since the Data Set timing and L16 sequencing is asynchronous. Monitor data shifting does not interrupt the time base when in the frequency counting cycle.

The status flags Overflow, Prescaler warning, 5 Mhz warning and Command Update are loaded by the STRI load term to the shift register containing the most significant frequency count.

2.6 FREQUENCY DISPLAY

The frequency counters are BCD counters, each stage being one digit. The eight frequency counter stages are stored into FC latches at the end of the counting cycle. The FC latch outputs, in addition to loading the monitor word shift registers, is also routed to a bank of 4 bit multiplexers to select one of eight digits plus the 100 Mhz bit. The selected digit and multiplexer address is sent to the front panel LED display logic to drive the 9 digit scanning LED numeric displays. The LED readout thus provides the full frequency count resolution of 150 Mhz +/- 1 Hz. The front panel display is primarily for local indication and control of Flukes, the same frequency of the display being the same count read by the Data Set as monitor data for remote monitoring and control.

2.7 ERROR/STATUS FLAGS

Various status and error events are captured to monitor and report the operation of the L16 and associated Fluke, summarized below:

1. PWR FLAG indicates the Fluke Synthesizer is on and power supplies within operating range.

2. REMOTE FLAG indicates the Fluke Synthesizer mode switch is selected to remote commanding. If in Local mode, DCS commands through the L16 will be ignored. (note: power and remote flags are part of the Command Echo word).

3. 5 Mhz WARNing is activated upon loss of or insufficient level to drive the time base. It indicates the time base and hence the frequency counters are not running and the count values are not being updated. This error illuminates a front panel LED.

4. PRESCALER ERROR is generated by the Prescaler Board upon loss of prescaler output being in the 100-150 Mhz range. This indicates loss of or incorrect Fluke Synthesizer RF output due to a Fluke failure, a frequency outside the normal system 100-150 Mhz range, or failure of the prescaler IC. This error illuminates a front panel LED. When active indicates the frequency count is erroneous.

5. OVERFLOW is generated by the Frequency Counters when a count of 200 Mhz or greater is reached to indicate obvious malfunction in the frequency counter. This error illuminates a front panel LED. When active indicates the frequency count displayed is the last good count, as the frequency latches are not updated on Overflow. The frequency should thus be questioned.

6. CMD UPDATE is generated upon receipt of a new tuning command to verify the command was received and that the Fluke Synthesizer output is likely slewing. Indicates the frequency count may be erroneous when active, the duration nominally only a couple of 1-sec count cycles.

All flags are latched during the update cycle, while the capturing circuitry is cleared such that the condition can be re-checked during the next count cycle. Thus temporary and permanent error conditions can be determined.

3. DETAILED CIRCUIT ANALYSIS

This section presents detailed circuit descriptions necessary for the troubleshooting and maintenance of the L16. The main function and purpose of this logic is described in Section 2. Refer to the L16 Logic Diagram, C13220L2 and Prescaler Schematic, C13220S12.

3.1 MODULE INTERCONNECTIONS AND SPECIFICATIONS

The L16 requires the following INPUTS:

1. 5 Mhz REF IN - via OMQ P15, 0dbm 5 Mhz from the MLO system.
2. SYNTH RF INPUT - via OMQ P13, +10 dbm 100-150 Mhz from the Fluke Synthesizer.

3. Data Set Interconnections - via P2, the SMA address lines, clocks, strobes and command data line to execute Data Set communications with the L16.

4. Synthesizer Status - via P1, the Fluke Power and Remote mode flags (part of the Synthesizer Command cable).

The L16 provides the following OUTPUTS:

1. SYNTH RF OUT - via OMQ P14, +10 dbm 100-150 Mhz from the Fluke Synthesizer through the L16 10 db coupler.

2. SYNTH COMMAND CABLE - a multi-wire cable via P1 carrying the 34 bit parallel tuning command to the Fluke remote input connector.

3. MONITOR DATA - via P2, the serially shifted digital monitor data when polled by the Data Set.

NOTE: Fluke Synthesizer RF output is routed through the 10db coupler in the L16. Therefore, an L16 module (or suitable patch between P13 and P14) must be installed for proper system distribution.

The L16 satisfies the following specifications as per Memo, Feb. 21, 1980, L16 Specifications by Larry Beno:

1. Signal Input - 100-150 Mhz nominal into 50 ohm load via OMQ connector, +10 dbm nominal level, with frequency counte operation to 0 dbm sensitivity.

2. External Time Base - 5 Mhz, approximatly 250 mv RMS (0 dbm) sinusoidal input into 50 ohm load via OMQ connector.

3. Accuracy of Counter - +/- 1 count +/- time base error.
   Resolution - 1 Hz
   Display - nine digit numeric LED

4. The L16 shall produce no reflections on inputs and generate system noise within acceptable limits for proper MLO operation.

3.2 MODULE SELECTION/ADDRESSING (Logic Diagram Sheet 1)

To ensure only the proper L16 responds to Data Set commands and monitor polling, each L16 is hardwired through the bin connectors to be programmed to execute actions associated with the assigned MUX addresses. SMA address inputs are compared to the hardwired address by digital comparator 7485 E8, producing a MODULE EN term on the receipt of the proper SMA address. SMA lines SMA-0 and SMA-3, with MODULE EN, is decoded by 9301 E12 to produce discrete enabling terms associated with the SMA address.

Gates 7402 E6 and E11 further produce enabling to route the Data Set clocks and strobes to the proper devices. SMA address functions are listed in Section 2.1. The hard-wired address drives 9301 decoder E13 to illuminate one-of-four front panel LED's indicating the Channel (A,B,C,D) the L16 is programmed to respond to.

3.3 5 MHZ TIME BASE (Sheet 3; Fig 3)

External 5 Mhz input is carried from rear panel OMQ P15 to SMA P3 on the Prescaler Board using .161 Semi-rigid coax. On the Prescaler board, the 5 Mhz is terminated by a 51-ohm resistor, with approximatly 100 mv peak (-10 dbm) applied to the input to high speed comparator LM 360 U2. Loaded LM360 output goes HI at +50 mv input and LO at -50 mv with hysteresis. Rise and fall times are tr = 15 ns and tf = 9 ns. The LO to HI Lm360 output transition occurs at about 30 deg after the zero crossing point, provides consistent switching in relation to the 5 Mhz sinusoidal input. This stability in generating the TTL 5 Mhz clock is important as the 20:1 time base to frequency ratio (5 Mhz :100 Mhz input) produces a 1 Hz count error every 18 degrees of 5 Mhz. The LM 360 stability in comparator performance and temperature stability (< 5 ns over 0 deg C to 25 deg C) maintains a count accuracy within 3 counts over the worst case signal and temperature operating range.

The (-) LM360 output is the 5 Mhz TTL referenced clock sent to the time base on the logic assembly. The (+) output drives retriggerable one-shot AM26S02 U3b such that loss of 5 Mhz or marginal signal level is detected and reported.

LM360 TTL output enters the logic assembly via ribbon connector A4P2 at IC location C21-10, 11 and inverted by 74S04 (low delay time) C22. The two inverters C22-2 and C22-4 split the 5 Mhz TTL distribution to equalize fan-out loading to keep propagation times as balanced as possible. (Driving all 5 Mhz loads off one 74S04 section approaches the fan-out limit with a very "mushy" rising edge for switching). 5 Mhz is divided by 5 to 1 Mhz by 74160 C17, producing a carry at 1 usec intervals so the following six stages of 74160 are operating at base ten units of one second. The 74160 stages C19, 20, 23, 24 and 25 are cascaded and clocked by 5 Mhz. The terminal count (TC) at 74160 C25-15 occurs on the rising 5 Mhz edge at 1.000000 sec. +/- 5 ns, being < 20 ns in duration, and captured by 74LS109, the master GATE FF. Though the 1 second period has been reached, the time base is allowed to continue providing a 1 Mhz clock to the input sequencer (see Sect 3.6) and display multiplexer terms (to avoid blanking of the display during the update cycle).

The Prescaler IC count is inhibited upon the 1-sec switching of the GATE FF, halting the frequency counters. At 9 usec following the 1-sec GATE trigger, update actions have been completed and

term SYNC TB - is generated, initiating the start of the next 1-sec GATE period. SYNC TB - is applied to the preset load enable (PE) on all time base stages (except 1 Mhz stage C17) and to the GATE FF clear C30-1. This switches the GATE FF "ON" and restarts the time base stages at a count of all zeros upon the next rising edge of the 5 Mhz clock. This scheme produces the same propagation delay in starting the counter as the delay produced when the 1-sec. terminal count was reached, ensuring both the start and end of the 1-sec gate is synchronized to 5 Mhz.

3.4 COMMAND LOADING (Sheet 2; Fig. 4)

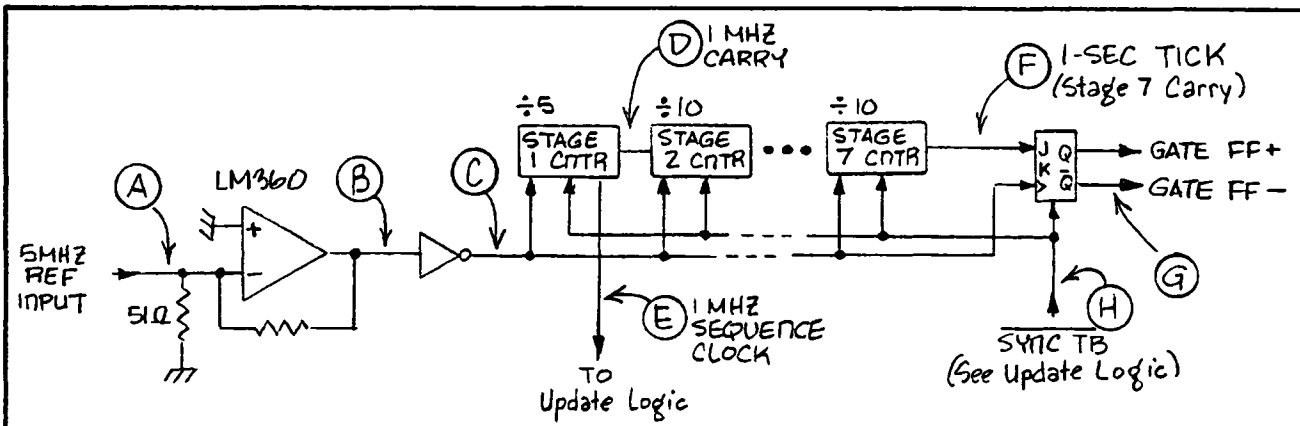
Data Set commands, clocks and load strobes (DIGO, CLKO, STRO) enters the L16 through J2 (being daisy changed to all L16's). When a command destined for the L16 is detected by the SMA address and module select logic, command enable terms MADR - 0 or MADR - 1 are generated. DIGO and CLKO inputs are routed to the correct set of command loading shift registes by gates 7402 D4. The most significant command word is serially loaded into 74164 shift registers D17, D22, and D27, enabled by MADR - 0; the least significant command word is serially loaded into shift registers D2, d7, and D12, enabled by MADR - 1. The command strobe STRO is distributed by 7402 D19-4, the MSB word, and D19-1, the LSB word, to dump the parallel outputs of the shift registers into the corresponding latches; 74174 D21, D26, D29 MSB command, and D1, D6 D11 LSB command. Fluke tuning commands from the Data Set occur infrequently (usually only at source changes). The latches provide static storage of the command word for the Fluke Synthesizer remote input and continuous command echo monitoring.

The tuning command, requiring two successive DCS command words to load, are nine sets of BCD digits representing the 1 Hz to 100 Mhz digits bits CB0 - CB23 and CA0 - CA8. MSB CA23, when HI, selects the 10 - 160 Mhz tuning range of the Flukes, the intended range. Each command must contain MSB CA23.

3.6 FREQUENCY COUNTER (Sheet 4 and Schematic C13220S12; Fig.5)

Fluke Synthesizer RF output is routed through a 10 db coupler in the L16, with th 0 db coupled port providing the RF power to drive the frequency counter circuit and logic. Connections to and from the coupler uses semi-rigid coax, with the coupled port terminated into 51-ohms on Prescaler PCB Assy A3 through SMA A3J1. The 0 dbm (~500 mv) RF signal is capacitively coupled to Prescaler IC U7, a Plessy SP8637 400 Mhz ECL decade divider. (See data sheets in the Appendix). The actions of the Prescaler Board elements vary depending whether the L16 is in the counting or update cycle.

The COUNT CYCLE is defined by the GATE + term being HI (1 second duration). GATE + (TTL) is translated to ECL by MC10124 U8



FUNCTIONAL BLOCK DIAGRAM

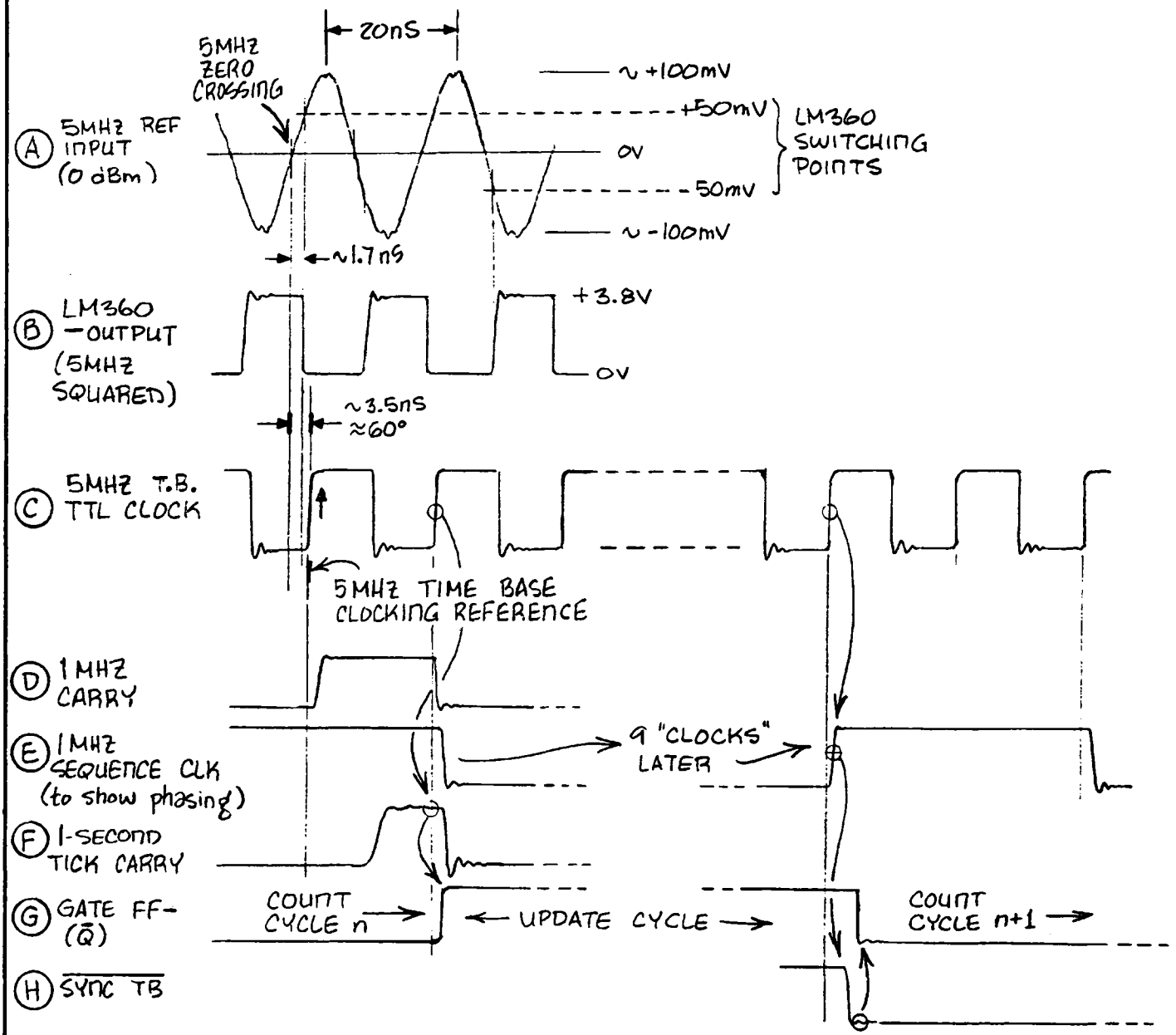
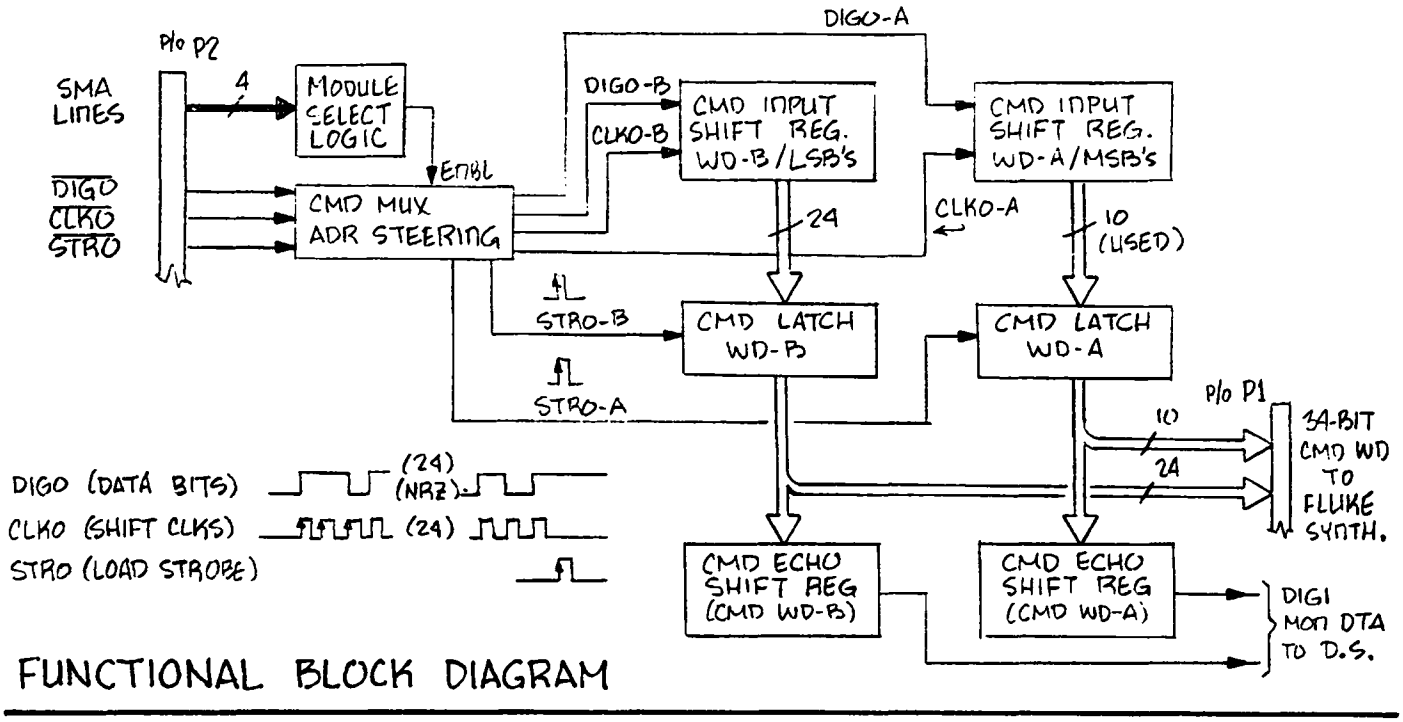


FIGURE 3
TIME BASE & 5 MHZ

QUICK-LOOK DATA

TB



FUNCTIONAL BLOCK DIAGRAM

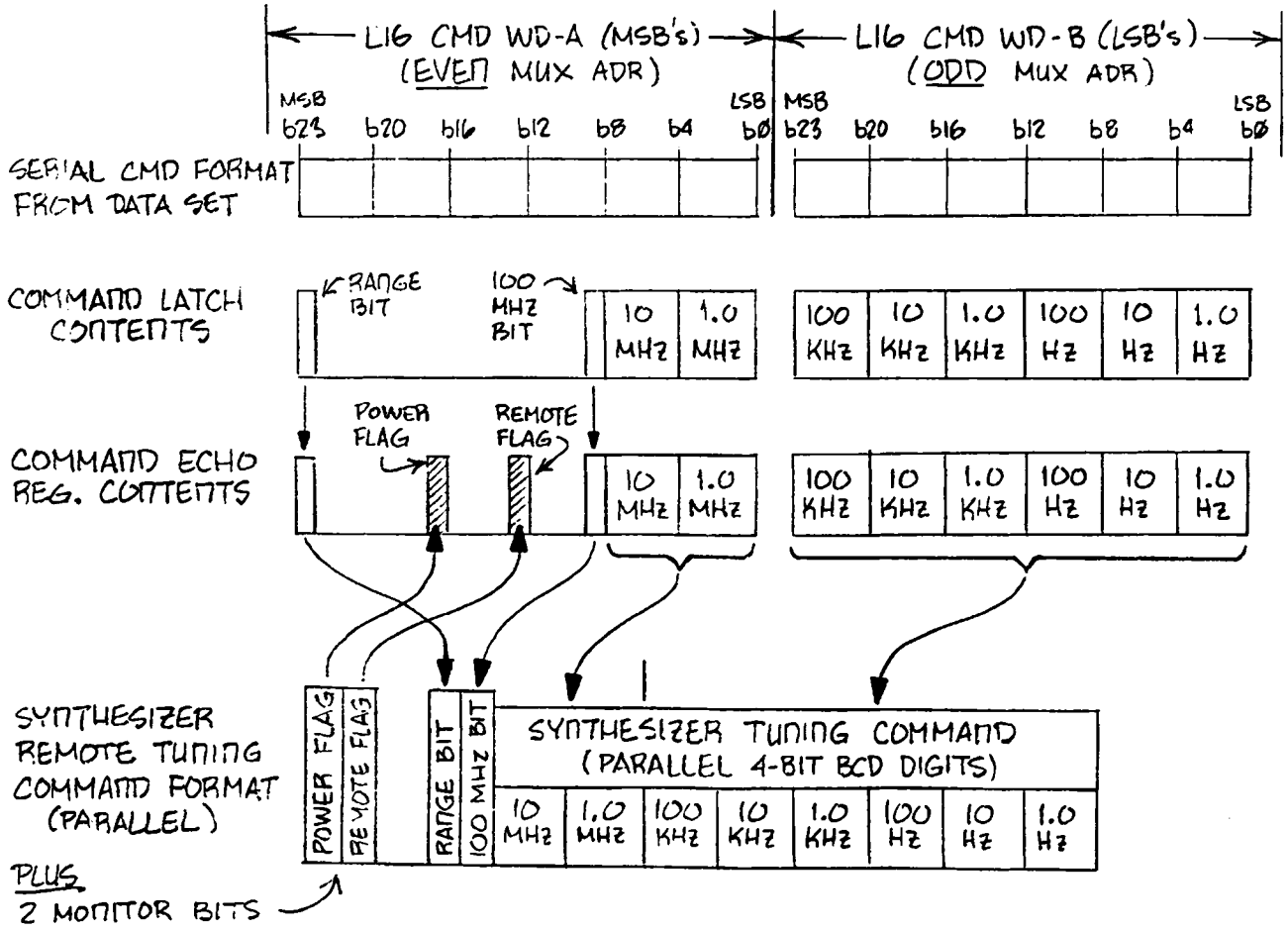
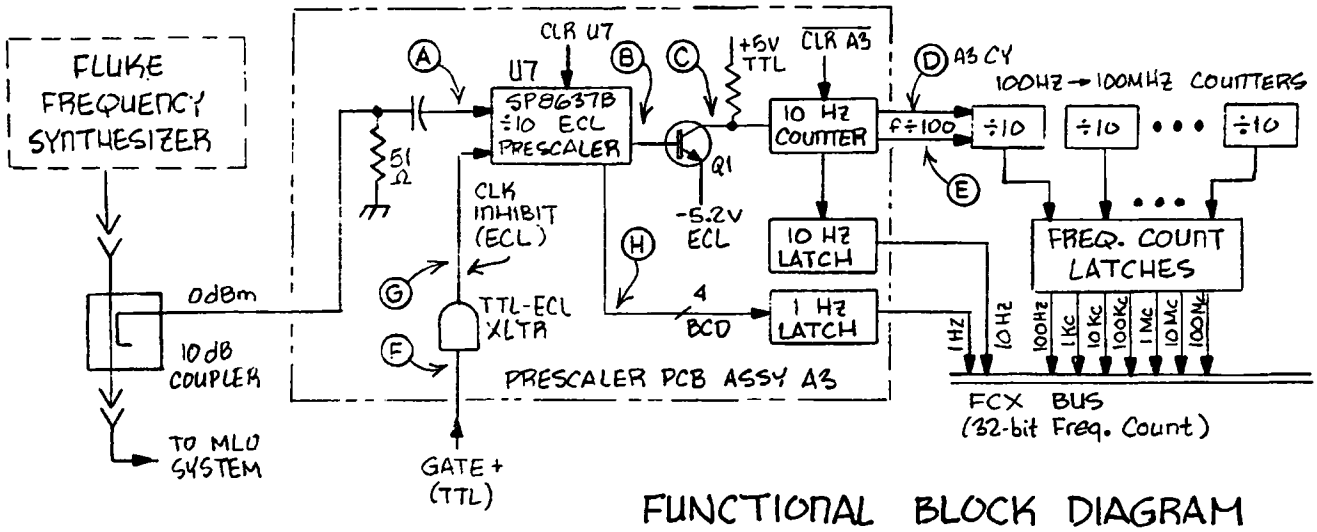


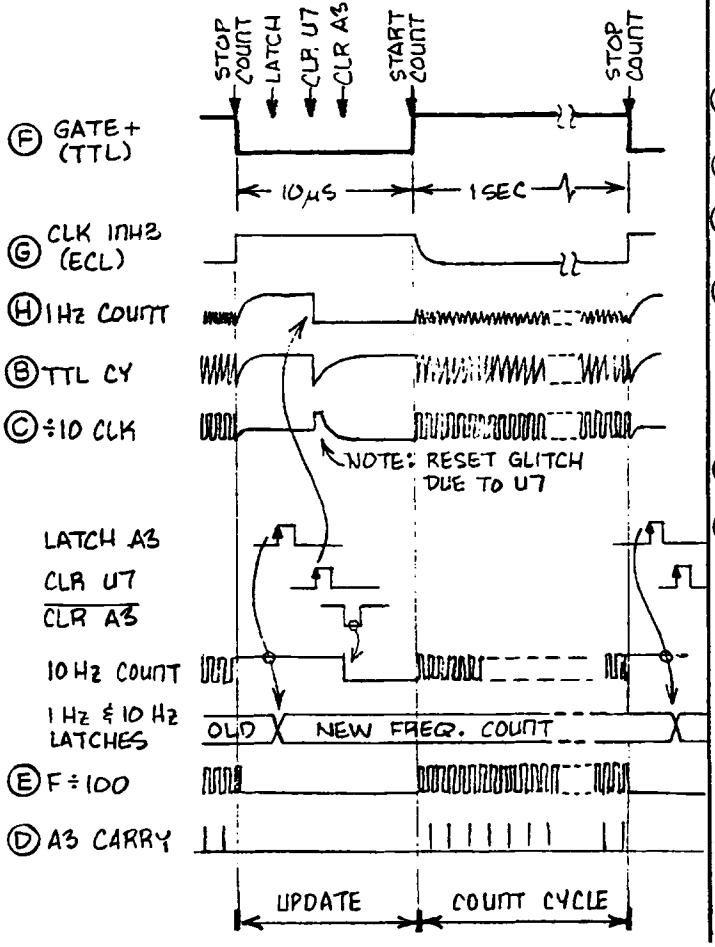
FIGURE 4
COMMAND LOADING - QUICK-LOOK DATA

CL



FUNCTIONAL BLOCK DIAGRAM

OVERALL TIMING



DETAILED TIMING & PHASING

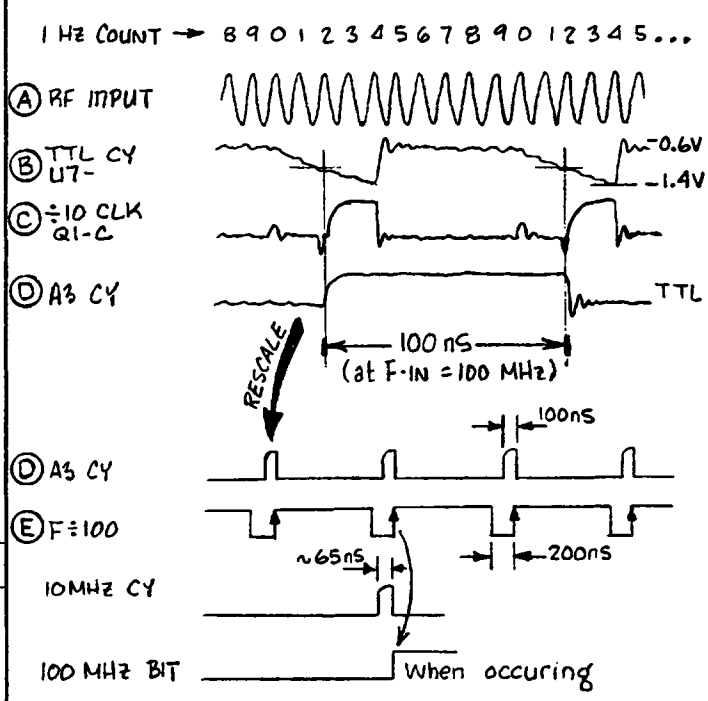


FIGURE 5
FREQUENCY COUNTERS

QUICK-LOOK DATA

FC

to ECL CLK INH term on the Prescaler. When CLK INHB goes ECL LO, providing a BCD A,B,C,D output and and a TTL divide by 10 carry (U7-11). While counting, the A,B,C,D outputs are < 1 v and unable to be used. The TTL carry (an anemic TTL) is "squared up" by saturating amplifier 2N2907 Q1, forming the clock to 74LS160 decade counter U6, the 10 Hz counter stage. The Q3 output of U6 counter is used for the divide by 100 clock, the clock source for the following seven stages of counters on the logic assembly. Q3 is used for the clock as its rising edge occurs at the zero crossing point of the input RF (CLK INPUT) to the Prescaler, keeping the phase of the various counting devices in phase. U6 output Q0, representing divide by 20, clocks retriggerable one-shot AM26S02 U3 as an activity sensor for the Prescaler, transistor amplifier and 2nd stage counter U6 to detect a failure in the frequency counter "front end". Additionally, the one-shot will fail to retrigger at a frequency below about 4 Mhz, representing a frequency 80 Mhz (4 Mhz x 20) of the input RF, to indicate the Fluke Synthesizer is operating at a frequency below the normal system range. In these cases, the one-shot U3 will illuminate the PRESCALER ERROR front panel LED and associated error flags being set. (Momentary power glitches can clear the command latches. A zero command word to the Flukes will cause it to wander wildly in the 20-30 Mhz range. A PRESCALER error with a wandering frequency display indicates this state, corrected by re-issuing valid tuning commands). A PRESCALER error with a zero frequency display indicates loss of Fluke RF input, or failure of the Prescaler "front end" circuitry.

The divide by 100 clock from U6 enters the logic assembly by ribbon connector A4P1, IC location C1-6. It is buffered by 7404 D9-12 and D9-14 which adds propagation delay to ensure the A3 CY term from the Prescaler is captured by 3rd stage (1Khz) counter 74160 C2 and following stages C3 thru C8. All frequency counter stages on both the Prescaler and logic assemblies will continue to count each cycle of the input RF for the 1-sec. duration of the Count/GATE cycle.

The UPDATE CYCLE is defined by the GATE + term being LO, a function of the time base/gate logic. TTL GATE + going LO is translated by prescaler IC U8 to ECL HI, the CLK INHB (inhibit) state of prescaler IC U7. This halt the counting action of U7. The TTL CY term U7-11 becomes static, halting the clock generation to the following counter stages, freezing the BCD counts of the frequency count in all nine counters. BCD outputs A,B,C,D on U7 prescaler settle within 2 usec to a TTL level, pulled up by 10 k resistors R10 - R13 and applied to the inputs of quad latch 74LS75 U5. At UPDATE +2 usec, sequence term LATCH A3 clocks the 1 Hz BCD count into latch U5, and the 10-Hz U6 BCD count into latch 7475 U4. (Note:term LATCH A3 is not generated if OVERFLOW error is detected). Term FC DUMP latches the remaining counters 74160 C2 thru 12. The 100 Mhz bit is latched into D-FF 7474 C13.

At UPDATE + 4 usec, sequence term RESET A3 + resets the BCD count in U7 prescaler to all zero. This inadverdently produces a TTL CY output and clocks counter U6, incrementing the frequency count by 10 Hz. For this reason, 74LS160 10 Hz counter U6 is cleared by term RESET - at time UPDATE + 6 usec, after the occurrance of the false U7 TTL CY to prevent an initial count of 10 Hz from occurring. At UPDATE + 7 usec the remaining frequency counter stages are cleared by term FC RST. All counter stages have now been read, latched and cleared awaiting the next count/gate cycle to begin. The outputs of the frequency count latches store the last count until the next update cycle, thus remaining static to drive the display and monitor word logic.

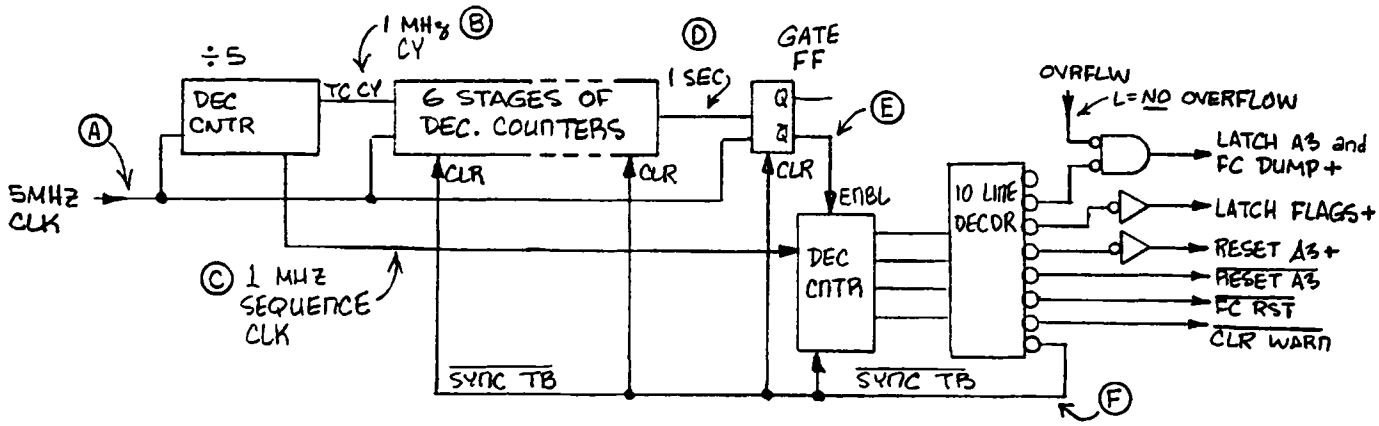
The last frequency counter stage, 74160 C8, develops the 100 Mhz count bit at Q0; output Q1, if HI, would represent 200 Mhz, an impossible count for the Fluke Synthesizer range. C8-13 Q1 is used as an OVERFLOW ERROR detector, indicating a malfunction in either the frequency counter stages or the time base operating beyond its 1-second interval. Frequency counts are not latched if an OVERFLOW occurs, so that the latched count represents the last "good" count. The term illuminates the OVRFLW front panel LED and is captured as an error flag.

3.6 UPDATE SEQUENCING & CONTROL LOGIC (Sheet 3; Fig. 6)

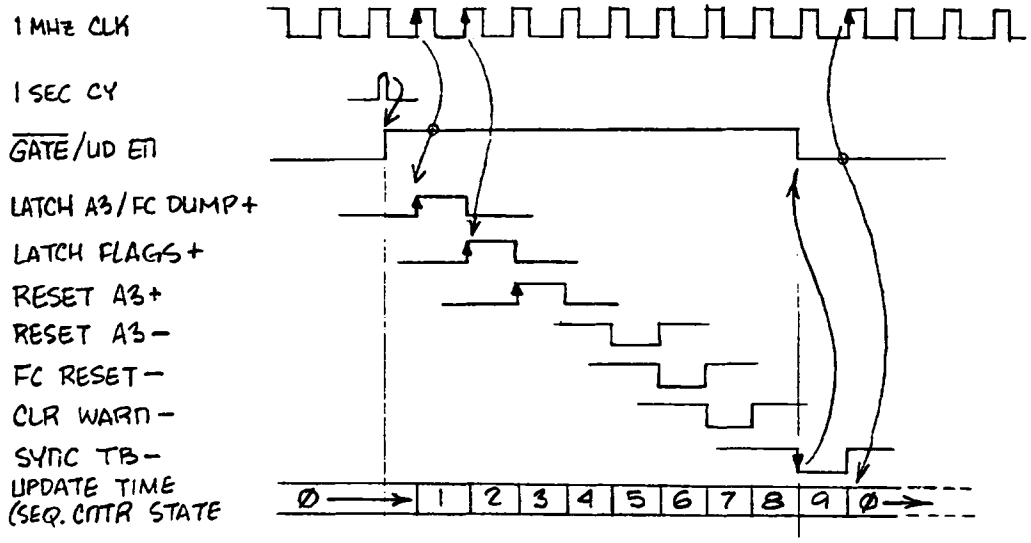
Of the main functions of the L16, the frequency counting components must be synchronous to the 1-second gating, while command and monitor functions between the L16 and Data Set are asynchronous (can occur at any time in relation to the gate timing). The updating logic must therefore be synchronous to preserve the precise 1-second count period.

All the update logic centers around the MASTER GATE flip flop, 74LS109 C30-6,7. When GATE + goes HI (C30-7), the 1-second count period begins; when GATE + goes LO, as a result of the time base reaching the 1-second +/- 5 ns point, the count cycle ends and the update cycle begins.

At time base = 1.000000 second, 74160 C25-15 terminal count (TC) is clocked into GATE FF by the 5 Mhz clock, toggling GATE + to LO (C30-7) and GATE - to HI (C30-6). The time base continues to run, however, to generate 1 Mhz CLK required by the update logic. When GATE + goes LO, the transition triggers 9602 one-shot E17-6 to produce a 180 ms period to illuminate the UPDATE front panel LED. GATE FF term GATE - going HI enables the update sequence counter 74160 C16, clocked by the time base 1 Mhz, such that counter C16 increments its BCD count every 1.0 usec. The BCD counter outputs Q0 - Q3 drive 9301 10-line decoder C26 to produce ten sequential discrete outputs Y0 through Y9, each being active lo for 1 usec.



OVERALL UPDATE CYCLE TIMING



1- and 5-MHz PHASING & 1-SEC GATE GENERATION

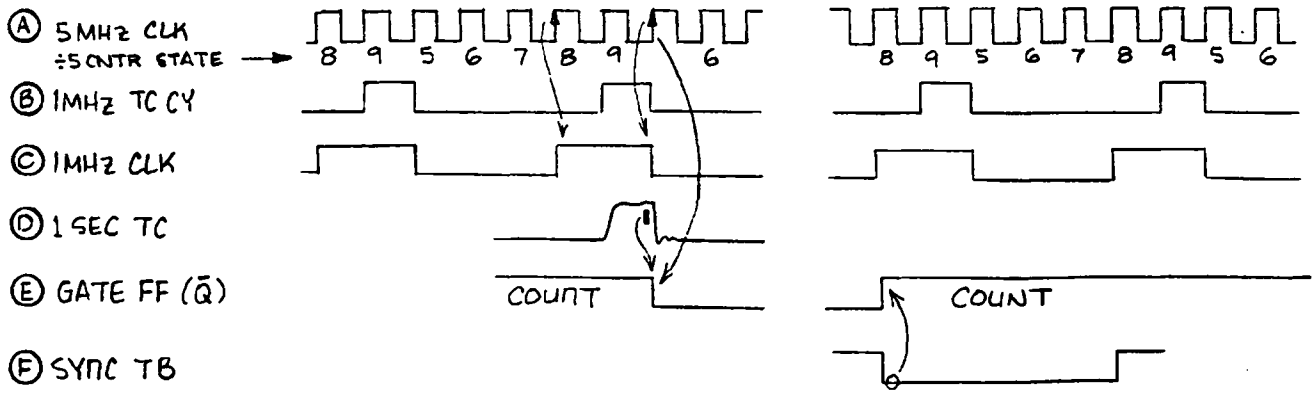


FIGURE 6
UPDATE LOGIC

QUICK-LOOK DATA

UD

At UPDATE + 1 usec (Y0, C26-13), no action occurs to allow the frequency counters, particularly the prescaler, to halt and settle. At UPDATE + 2 usec (Y1, C26-12), the LO output is and'd with the OVFLOW flag to produce terms LATCH A3FC DUMP if no OVERFLOW occurred. LATCH A3 latches the 1- and 10 Hz counts on the prescaler board, FC DUMP latching the seven 100 Hz to 100 Mhz count stages.

At UPDATE + 3 usec (Y2, C26-11), inverter C22-12 produces active HI term LATCH FLAGS, the L-H edge clocking the error states into the respective error latches.

At UPDATE + 4 usec (Y3, C26-10), inverter C22-14 produces active HI term RESET A3 +, clearing the prescaler IC BCD count, readying it for the next count cycle.

At UPDATE + 5 usec nothing happens because I couldn't think of anything for it to do!

At UPDATE + 6 usec (Y5, C26-5), term CLR WARN - clears the various error detecting capturing FF's.

This completes the update sequencing required to latch the frequency counts and restoring the logic for the next count cycle. The update cycle is now terminated and the count cycle initiated.

At UPDATE + 10 usec (Y9, C26-7), the SYNC TB - term going LO immediately clears the GATE FF, the transition of GATE + going HI defining the start of the count/gate cycle. GATE + going HI also triggers 26S02 one-shot E19 producing variable delayed GATE of 10 - 50 ns, adjusted by potentiometer E9-7. A3 GATE FF 7474 C15 develops a special GATE period for the prescaler IC that is delayed slightly beyond the true gate start time, but is stopped in union with the MASTER GATE FF. This delay compensates for some chattering in the prescaler IC when first re-enabled for counting in which a few counts tend to accumulate before the first RF cycle. UPDATE + 10 usec/sync TB - is also used by the update sequence counter C16 for the PE - enable, loading a count of zero on the next 1 Mhz count, ensuring it is ready for the next count cycle. When SYNC TB - cleared the GATE FF to the count state, term MSTR GATE - going LO, the update counter enable term, inhibits the counter from sequencing during the next count/gate cycle. The next 1 Mhz time base clock does, however, clear the sequence counter through the PE preset, where it remains for the duration of the 1-sec. count cycle.

The update cycle actions are accomplished in 10 usec. The only interruption to the sequencing actions is caused by a monitor interrupt, caused when the Data Set, being asynchronous to the L16 timing, happens to poll for monitor data during the 10 usec update cycle. If either of the frequency count monitor words is

polled, the Data Set shift clocks (CLKI) trigger one-shot 9602 E17 (Sheet 5) to produce a 270 usec pulse MON INTR -. The update sequence counter is inhibited while MON INTR - is active LO, preventing the sequence logic from updating the frequency count and error latches until Data Set monitor polling is completed. This of course prevents monitor data from being "read" while the register contents are changing. (Additionally, the MON INTR - feature keeps all L16's count cycles closely synchronous to each other, as the Data Set polls each L16 for monitor data in sequence, causing the MON INTR to occur in each L16 within two waveguide cycles of each other. This is evident by the UPDATE LED's on the four L16's in each MT-1 and MT-2 racks "blinking" at the same time). During the MON INTR 270 usec period, the sequence counter is halted and held at the state it was in when interrupted. When MON INTR is completed, update actions will continue where they left off.

3.7 MONITOR DATA PROCESSING

Two monitor data values are polled by the Data Set: 2 words of Command Echo and 2 words of Frequency Count. The L16's are hardwired addressed to segment the L16's to respond only to the correct Data Set SMA address. (See Section 3.2)

3.7.1 COMMAND ECHO LOGIC (Sheet 2)

The two DCS tuning commands are stored in 74174 latches D1, D6, D16, D21 and D29, outputs being static between updates and sent to the Flukes as the parallel command word. The latch outputs are also loaded into the parallel inputs of 74165 shift registers D18, D23, D28, the high order command bits, and D3, D8, D13, the 24 low order bits. Loading occurs upon receipt of the DS STRI, being routed to the proper shift registers (terms MCLK-0, MCLK-1), the shift register contents being serially marched out to the Data Set. There is a bit-to-bit image (or "echo") of the command word format. The control computers use the Command Echo word to verify the tuning commands were received by the L16 as sent. Note the difference between the Command Mux and Echo Mux is 100 (octal); thus Command Mux 320 can be seen "echoing" back on Mux 220. (See also Sect 3.4)

3.7.2 FREQUENCY COUNT MONITOR LOGIC (Sheet 4 and Sheet 5)

The frequency count is latched into registers on both the Prescaler board and main logic assembly. The 100 Hz to 100 Mhz digits from 74714 latches C9 - C12 are combined with the 1 Hz and 10 Hz digits from the Prescaler board on Sheet 4, forming the FCX BUS. The 9 digit frequency count is delivered to the display logic and the monitor data registers via the FCX BUS. Shift registers 74165 load the FCX BUS upon receipt of the Data Set stroge STRI, being sent to the proper shift register by steering gates on Sheet 1. Shift registers D5, D10, D15 contain the 1-Hz

to 100 Khz BCD digits, and D30 the error flags. The format of the duo word used for tuning commands, command echo and frequency count are identical, allowing a direct BCD readout on a DCS Data Tap by viewing the appropriate MUX's.

3.8 FREQUENCY DISPLAY LOGIC (Sheet 5 and 6; Fig 7)

The frequency count, in addition to being provided as DCS monitor data, is also available on the L16 front panel as a local numeric display. The full 150 Mhz range with 1 Hz accuracy and resolution is displayed as a nine-digit word.

The full frequency count from the latches is sent via the FCX BUS to display multiplexers 9312 E1 throuh E4 to select one-of-eight frequency digits. The address scanning is derived from the time-base, the selected digit further multiplexedby 74157 E10 to merge in the 100 Mhz bit (F1J+). If the 100 Mhz bit is HI, 7402 D19 forms BCD "1" (0001) on the 74157 inputs; if the 100 Mhz bit is LO, all 74157 BCD inputs become HI producing an LED blanking code (1111).

The four-bit scanning address and selected 4-bit BCD frequency digit is sent to the Display Board Assembly A5 through a ribbon cable. The selected digit is sent to the BCD-to-7 segment decoder CD4511 U1, (Sheet 6) the output sent to the segment select inputs on the numeric LED displays. Resistors R1 through R7 are current limiters for proper display intensity. The 4-bit scanning address is sent to CMOS BCD-Decimal decoder CD4028 U2 producing active HI digit select strobes, amplified by 2N918 transistors Q1 through Q8 to form the proper digit drive voltages of +2.4 volts (OFF) and 0 volts (ON). The multiplexer display scans from right to left at 5 Khz, each digit illuminated for 200 usec. CMOS devices were selected for U1 and U2 to keep currents at a minimum so the switching currents during LED scanning would not cause EMI interference to the sensitive MLO environment. The active HI feature of CMOS also eliminated using inverters for proper logic sense with the DL-330M common-anode display units.

Discrete LED's on the front panel/Display Board are driven by logic on the main logic assembly for status and error indications as follows:

5 MHZ REF AVAIL - illuminated to show 5 Mhz availability.
COUNT - "blinks" to show 1-sec. time base operation.
GATE - illuminated during the update cycle.
OVRFLW - illuminated upon Overflow condition of frequency counters.
PRESCALER - illuminated to show prescaler error or failure.
LOSS OF 5 MHZ - illuminated upon loss of 5 Mhz.

3.9 ERROR FLAG AND STATUS (Sheet 5)

Several status and error flags are generated to indicate normal and abnormal operation of the L16 and associated Fluke Synthesizer.

CMD INTR - OR gate C29-15 senses the arrival of either tuning command words, and when sensed is captured for presetting 7474 FF C13-11. During update, the event is clocked into error latch 74715 E15 and reported during the next monitor word polling. This flag indicates a new frequency command has been received, the Flukes likely "slewing", and thus the frequency count may not yet be settled. The capture FF C13-11 is cleared during each update cycle by CLR WARN -.

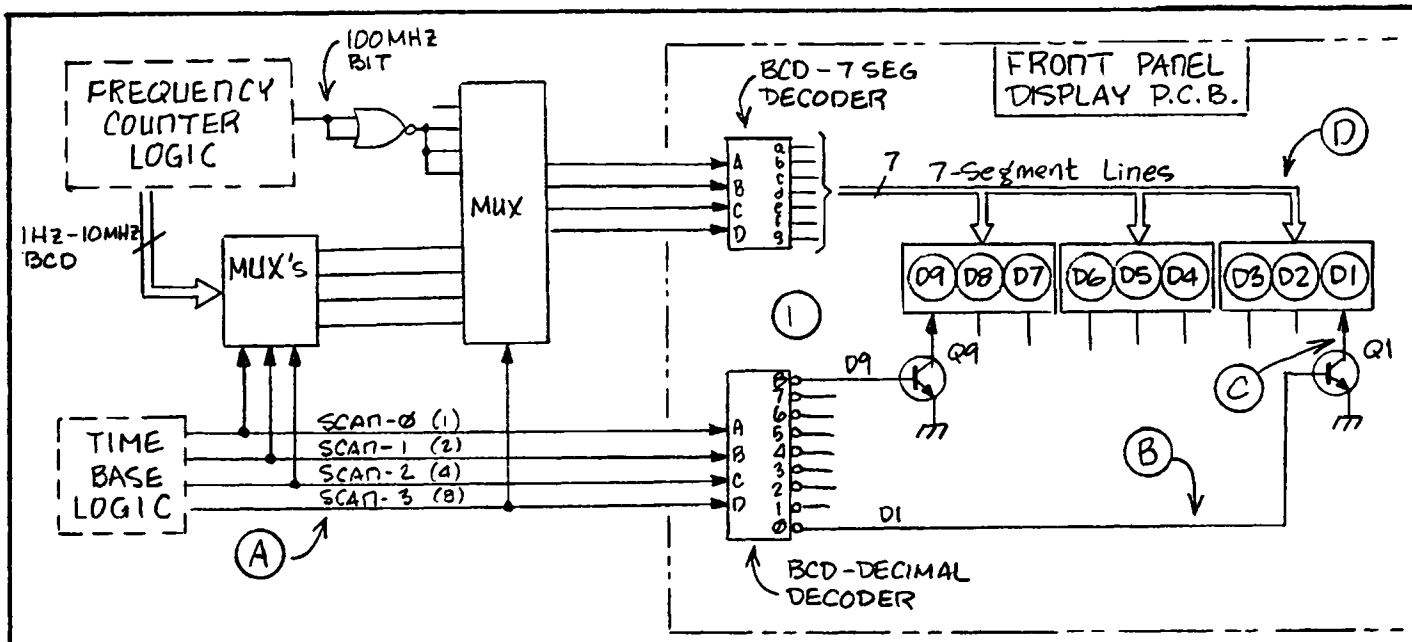
5MHZ OK - is generated by a retriggerable one-shot on the Prescaler Board. Should the external 5 Mhz fail, or be of insufficient level to clock the time base, 5 Mhz OK goes LO to indicate the error condition, captured by the 7474 FF C14-5 and sent directly to the monitor data register. 5 MHZ OK error is not latched since loss of 5 Mhz would render the update sequence inoperative, the event being otherwise unreported. A front panel LED is also illuminated.

PRESCALER error - is generated by a retriggerable one-shot on the Prescaler Board, an error indicated by PRESCALER ERROR being LO, captured by 7474 FF C14-10 and clocked into error latch E15 and reported during the next monitor word polling. The capture FF C14-10 is cleared during each update cycle.

OVERFLOW error is produced when a count of 200 Mhz or greater is accumulated in the frequency counter. The 200 Mhz bit, when set HI defines overflow and is clocked into error latch E15 and reported during the next monitor word polling. A front panel LED is also illuminated. The overflow condition is cleared when the frequency counters are cleard during the update cycle.

NOTE: The 74175 error latch E15 provides temporary storage of error conditions for reporting by DCS monitor data. If the error condition is momentary, the flag will be cleared upon the next latch update. (next 1-second gate end) and may not be active when monitor data is polled. Error flag reporting through monitor data is intended for a persistent error.

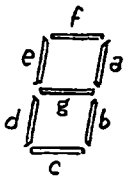
The Fluke Synthesizers provide two status monitor bits, the POWER on flag (H=ON) and REMOTE/local flag (H=remote) to indicate the mode of operation. These two status flags are loaded into the command echo monitor word shift registers 74165 D23-3 (REMOTE) and D28-11 (POWER) on Sheet 2.



FUNCTIONAL BLOCK DIAGRAM

DISPLAY SCANNING →

FREQUENCY DISPLAY	1 HZ	10 HZ	100 HZ	1 KHZ	10 KHZ	100 KHZ	1 MHZ	10 MHZ	100 MHZ	1 HZ	10 HZ	• • •
FORMAT	D1	D2	D3	D4	D5	D6	D7	D8	D9	D1	D2	• • •
SCAN COUNT (SCAN Ø → 3)	Ø	1	2	3	4	5	6	7	8	9	Ø	1 • • •



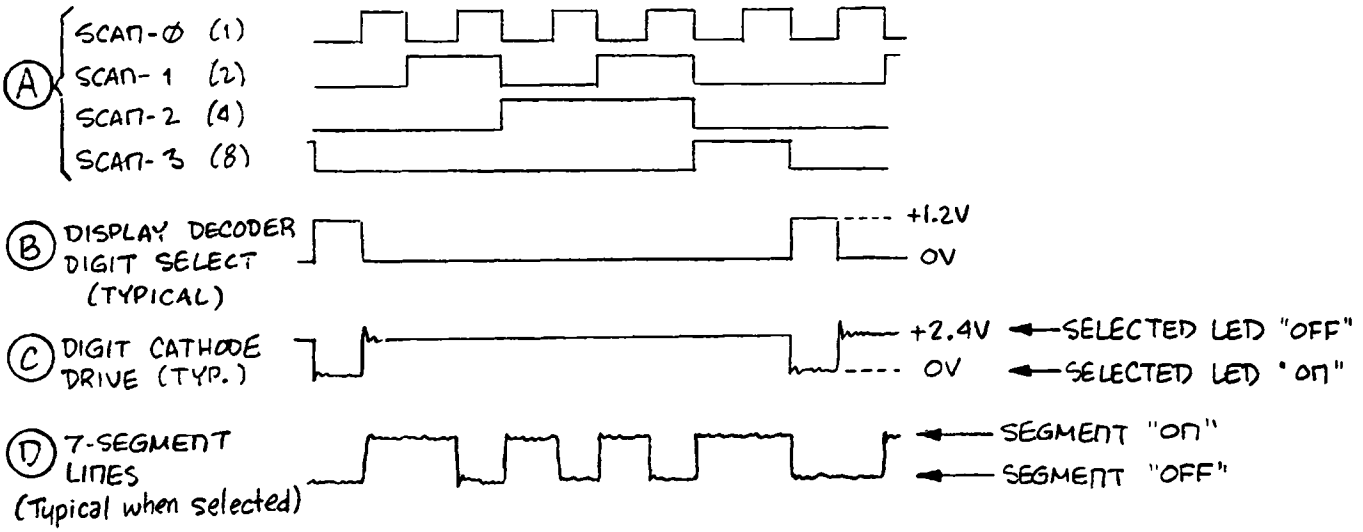


FIGURE 7
FREQUENCY DISPLAY

QUICK-LOOK DATA

FD

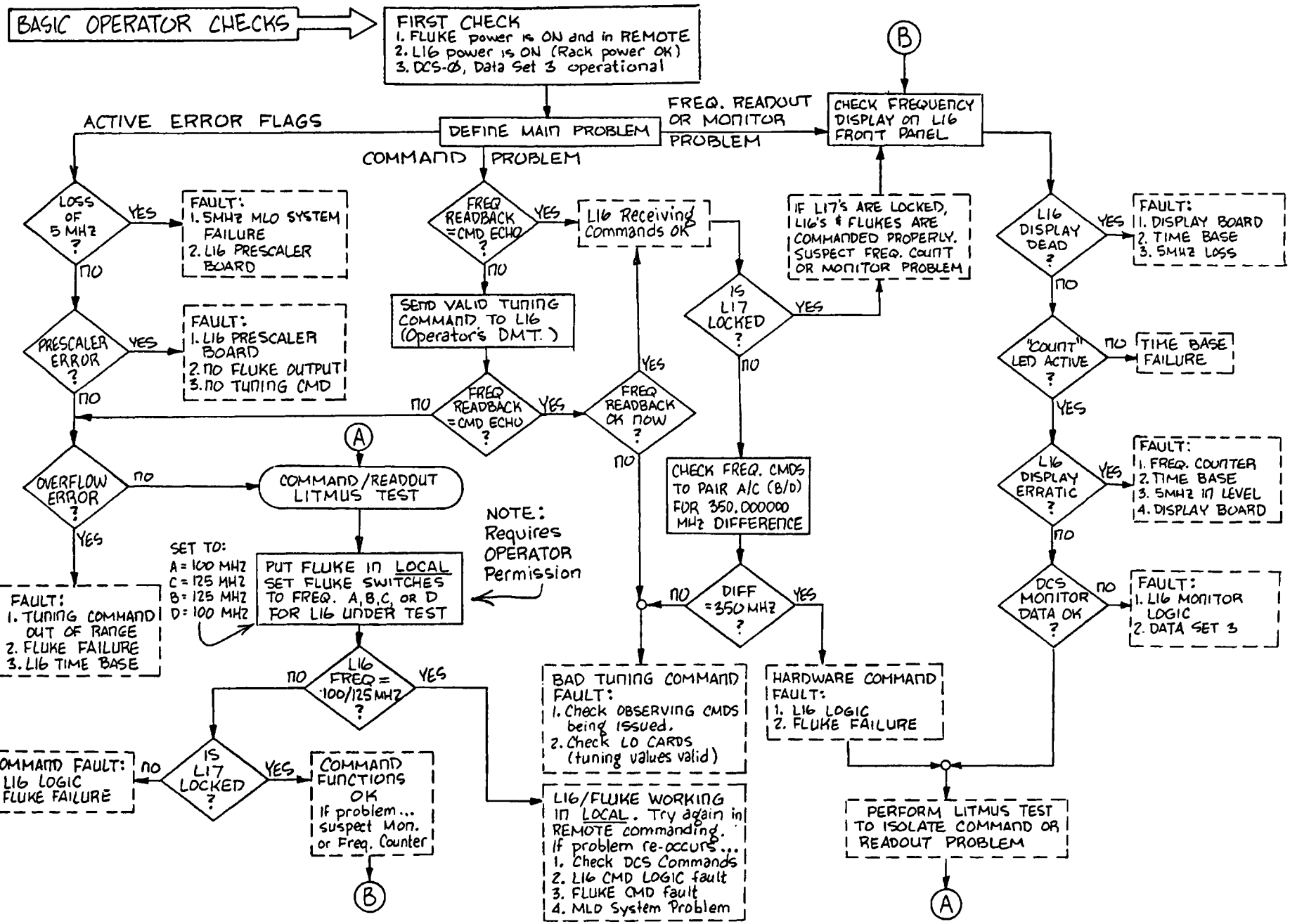


FIGURE 8
TROUBLESHOOTING TREE

4.0 LIST OF L16 DRAWINGS

Top Assembly Drawings

D13220P18 Top Assembly Drawing
A13220Z18 Top Assembly Bill of Materials
C13220L12 L16 Logic Diagram
C13220S12 L16 Prescaler PCB Schematic

Sub-Assembly Drawings

Assembly A3 - Prescaler P.C.B. Assembly

C13220P21 Prescaler Assembly Drawing
A13220Z17 Prescaler B.O.M.
C13220AB13 P.C.B. 2:1 Artwork
C13220M34 P.C.B. Drill Drawing

Assembly A4 - I.C. Module Logic Assembly

C13220P20 I.C. Module Assembly Drawing
A13220Z16 I.C. Module B.O.M.
A13220P24 Dip Header Assembly
A13220Z21 Dip Header B.O.M.
A13220W10 Wire List, Master
A13220W11 Wire List, Machine
A13220W12 Wire List, Hand
A13220W13 Wire List, Connector

Assembly A5 - Front Panel Display Assembly

C13220M33 Front Panel
C13220M36 Front Panel Engraving
C13220AA12 Front Panel Silk Screen
D13220P23 Display P.C.B. Assembly Drawing
A13220Z20 Display P.C.B. B.O.M.
C13220AB24 Display P.C.B. 2:1 Artwork
C13220M39 Display P.C.B Drill Drawing

Miscelleneous

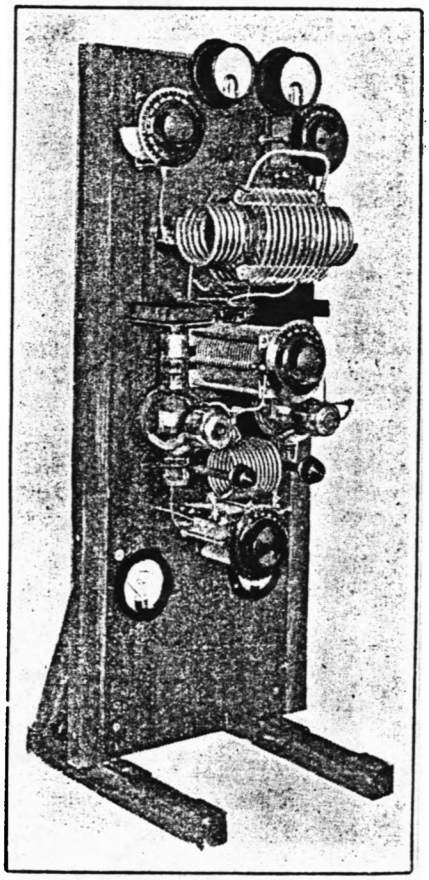
C13220M35 Assembly A1 - Rear Panel
B13220M42 Assembly A2 - RF Coupler Mounting Plate

For a list of drawings of major mechanical components (Side Panels, Module Rails, etc), see Top Assembly B.O.M. A13220Z18

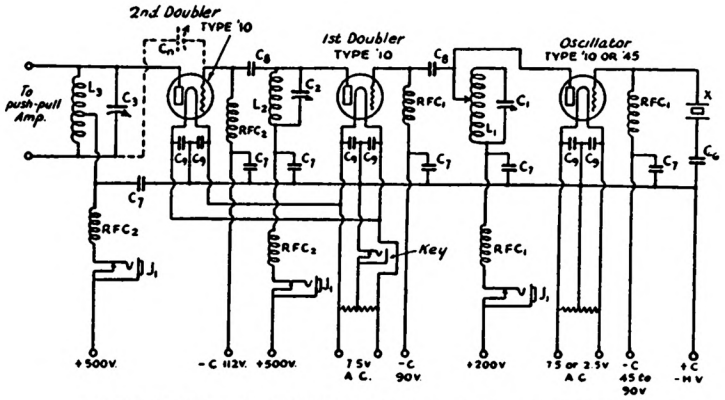
5.0 LIST OF MASTER LOCAL OSCILLATOR (MLO) DRAWINGS

D16000B4	MLO Block Diagram (older, Dumke version)
D16000B10	MLO System Rack Layout
D16000B11	MLO System Block Diagram (as-built version)
A13220W15	MLO Rack MT1, Rack Wire List
A13220W16	MLO Rack MT2, Rack Wire List
A13220W14	MLO Rack MT1, Bin "E" Wire List
A13220W17	MLO Rack MT2, Bin "E" Wire List

L16 DRAWINGS



A HIGH-POWER AMPLIFIER OF THE PUSH-PULL TYPE

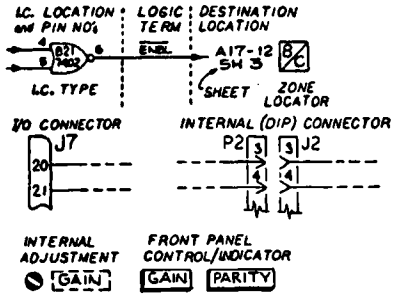


THE OSCILLATOR AND FREQUENCY-DOUBLER CIRCUIT

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	12-80			ROUTED FPNL WIRING THRU A4J4 (E20)
B	10-81			PRESCALER A3 GATING IMPROVEMENTS
C	10-86			ADDED CHAN. READOUT D25 & COUNT LED, MT-2 NOTES

GENERAL NOTES

1. CIRCUIT SYMBOLOGY USED



2. I.C. PIN NUMBERS ARE ALL REFERENCED TO 16-PIN DUAL-IN-LINE SOCKETS AND MAY DIFFER FROM I.C. PIN-OUT.
3. UNLESS OTHERWISE INDICATED
   ALL INVERTERS ARE 7404
   ALL D-TYPE FF's ARE 7474

SPECIFIC NOTES

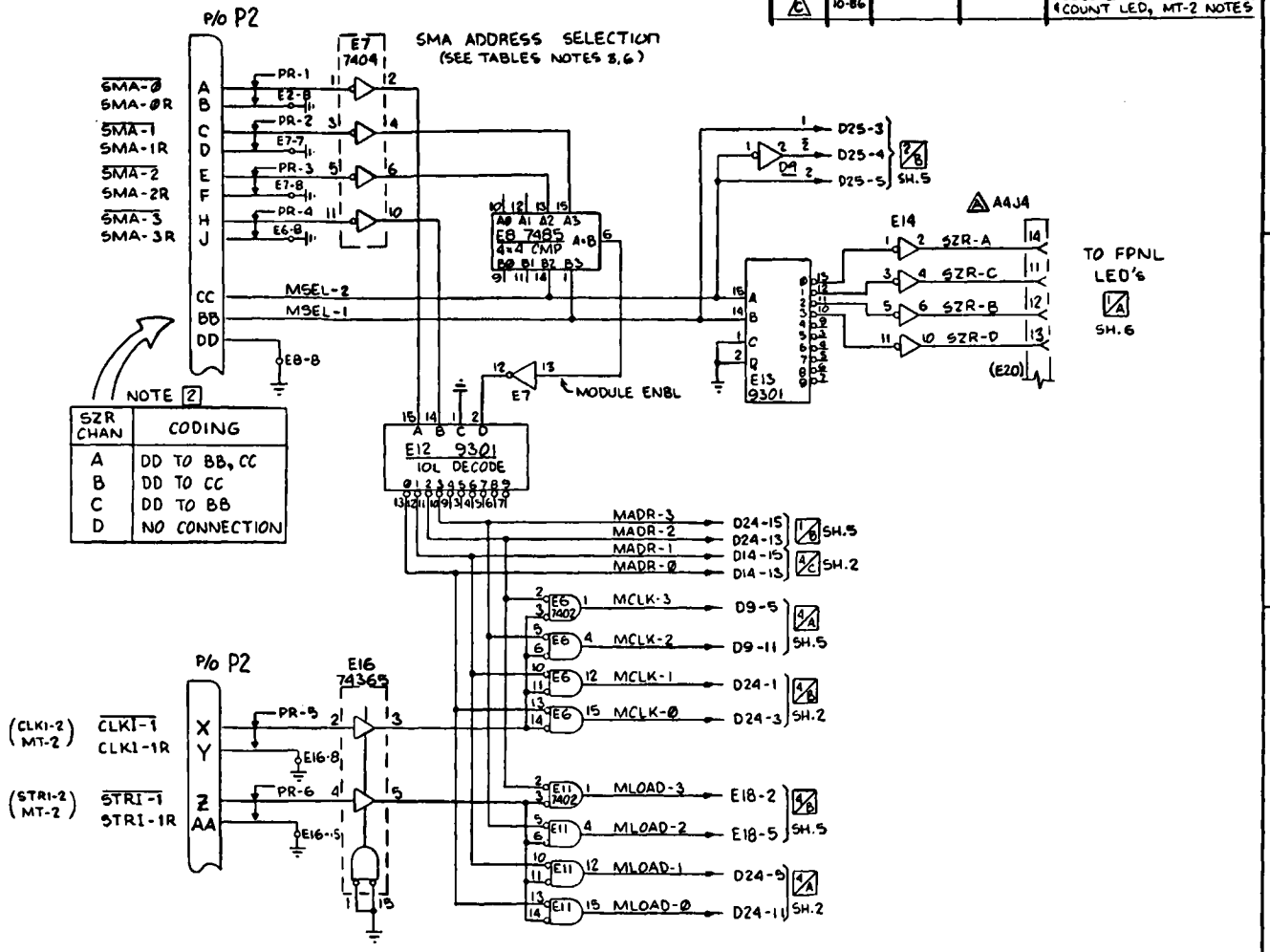
1. (H) DENOTES HAND WIRE; OTHERS MACHINE WIRES
2. L16 BIN SLOTS CODED VIA P2/J2- BB, CC, DD TO SERVICE SYNTHESIZERS A, B, C, D
3. RACK MT-1 SMA ADDRESS SELECTION

CMD/MON DATA	SUB-MUX ADR SEL A	B	C	D	L16 ADR ENABLE
SZR CMD WD-A	320	322	324	326	MADR-0
SZR CMD WD-B	321	323	325	327	MADR-1
CMD-A ECHO MON	220	222	224	226	MADR-0
CMD-B ECHO MON	221	223	225	227	MADR-1
SZR FREQ WD-A	230	232	234	236	MADR-2
SZR FREQ WD-B	231	233	235	237	MADR-3

WHERE; WD-A = MSB's WD-B = LSB's

4. L16 SUB-ASSEMBLY NOMENCLATURE
   A1 - REAR PANEL
   A2 - RF CHASSIS
   A3 - PRESCALER PCB
   A4 - I.C. LOGIC ASSY
   A5 - FRONT PANEL
5. CUT POWER PADS (PIN 16) AT C1, C21, E5
6. RACK MT-2 SMA ADDRESS SELECTION

CMD/MON DATA	SUB-MUX ADR SEL A	B	C	D	L16 ADR ENABLE
SZR CMD WD-A	340	342	344	346	MADR-0
SZR CMD WD-B	341	343	345	347	MADR-1
CMD-A ECHO MON	240	242	244	246	MADR-0
CMD-B ECHO MON	241	243	245	247	MADR-1
SZR FREQ WD-A	250	252	254	256	MADR-2
SZR FREQ WD-B	251	253	255	257	MADR-3



SIGNAL M PREFIX

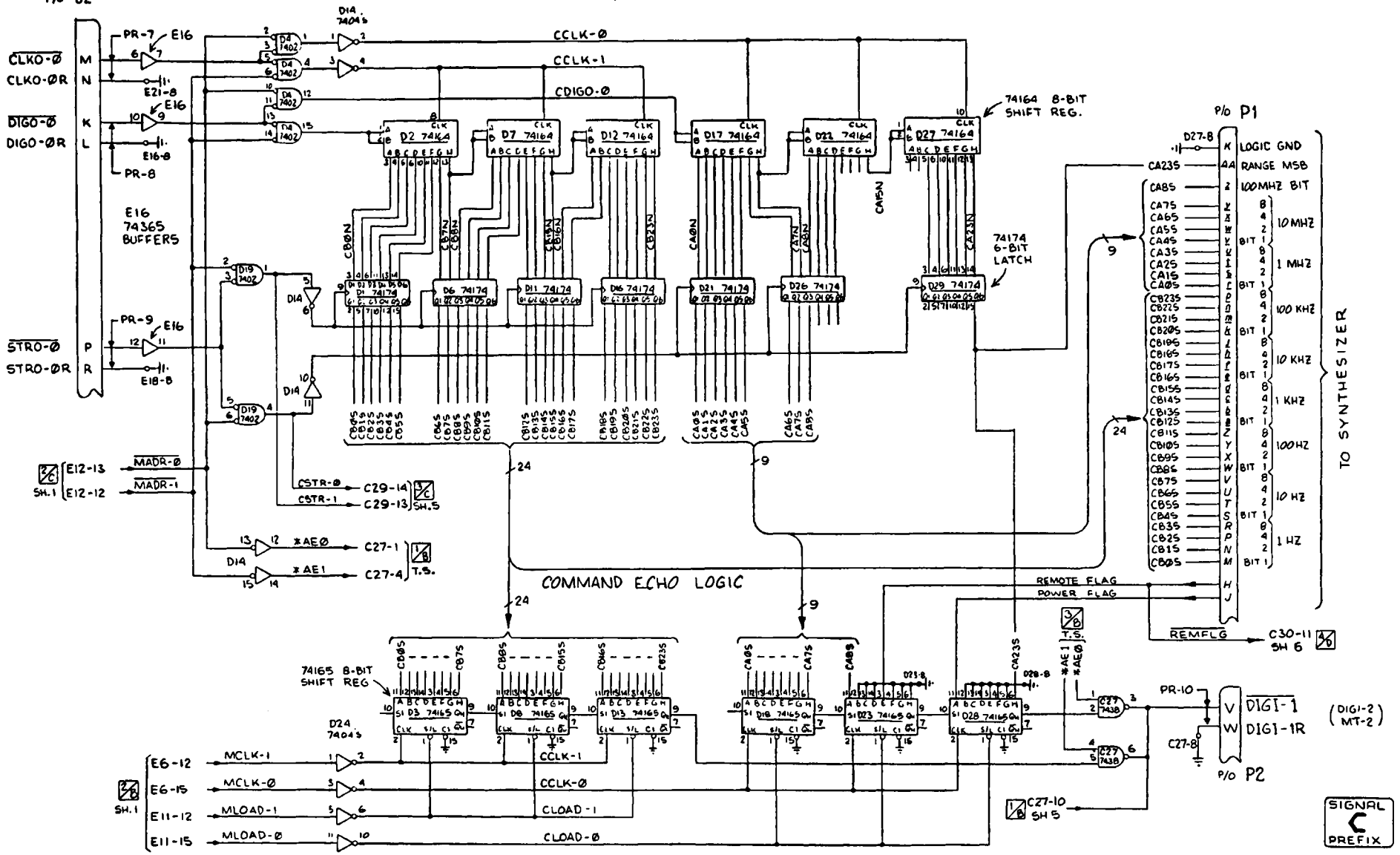
MODULE SELECT/ADDRESSING LOGIC

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 3 PLACE DECIMALS (.XXX): ± 2 PLACE DECIMALS (.XX): ± 1 PLACE DECIMALS (.X): ±	VLA PROJECT	L16 MODEL B SYNTHESIZER CONTROL	NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO NEW MEXICO 87801
C13220512 / ASSY "A3" MATERIAL: FINISH: NEXT ASSY / USED ON	TITLE	LOGIC DIAGRAMS	DRAWN BY — DATE MAY 1980 DESIGNED BY — DATE MAR-80 APPROVED BY — DATE SHEET NUMBER 1 OF 7 — DRAWING NUMBER C1322012 — REV B — SCALE —

LAST CLK'D 11/6/86

REV	DATE	DRAWN BY	APPR'D BY	DESCRIPTION
B	10-81			SEE SHT. 1

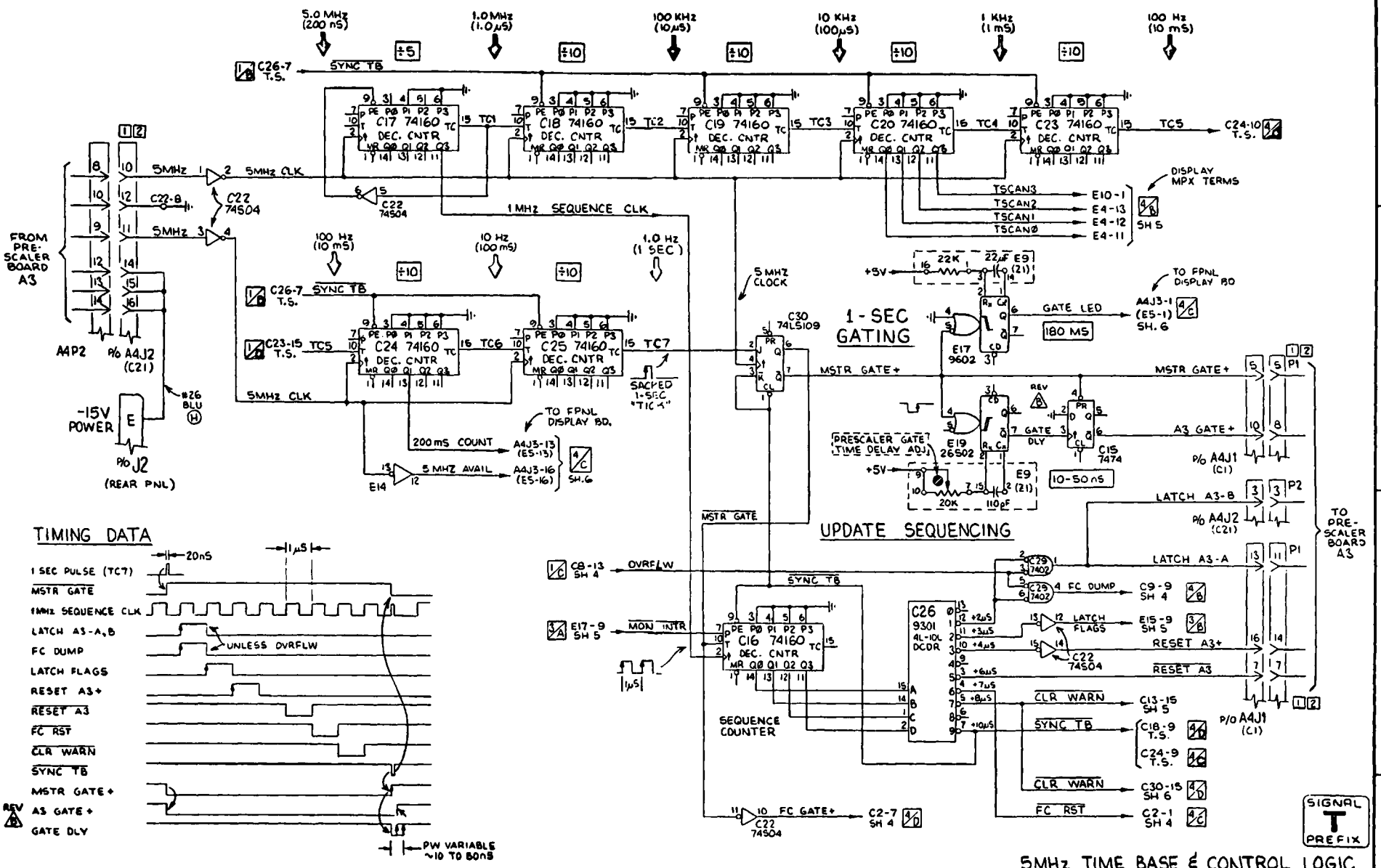
COMMAND LOAD/STORAGE REGISTERS



SYNTHESIZER COMMAND LOADING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	VLA PROJECT	NATIONAL RADIO ASTRONOMY OBSERVATORY
TOLERANCES: ANGLES ± / 3 PLACE DECIMALS (.XXX): ± / 2 PLACE DECIMALS (.XX): ± / 1 PLACE DECIMALS (.X): ±	L16 MODEL B SYNTHESIZER CONTROL	SOCORRO NEW MEXICO 87801
MATERIAL:	TITLE: LOGIC DIAGRAMS	DRAWN BY — DATE MAY-80
FINISH:		DESIGNED BY — DATE MAR-80
NEXT ASSY / USED ON		APPROVED BY — DATE
	SHEET NUMBER 2 OF 7	DRAWING NUMBER C13220L2 REV. B SCALE

5MHZ TIME BASE (TB)



TIMING DATA

NOTES

1. CUT +Vcc PAD PIN 16 AT LOC: C1 & C21
2. A4P1 & A4P2 14-PIN DIP PLUG
   A4J1 & A4J2 16-PIN DIP SOCKET
3. THIS SHT REDRAWN 12-81 FOR CLARITY (SUBJECT TO OPINION)

REV	DATE	DESCRIPTION
B	10-81	A3 PRESCALER GATING DELAY LOGIC ADDED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±

MATERIAL:

FINISH:

NEXT ASSY | USED ON

VLA PROJECT: L16 MODEL B SYNTHESIZER CONTROL

TITLE: LOGIC DIAGRAMS

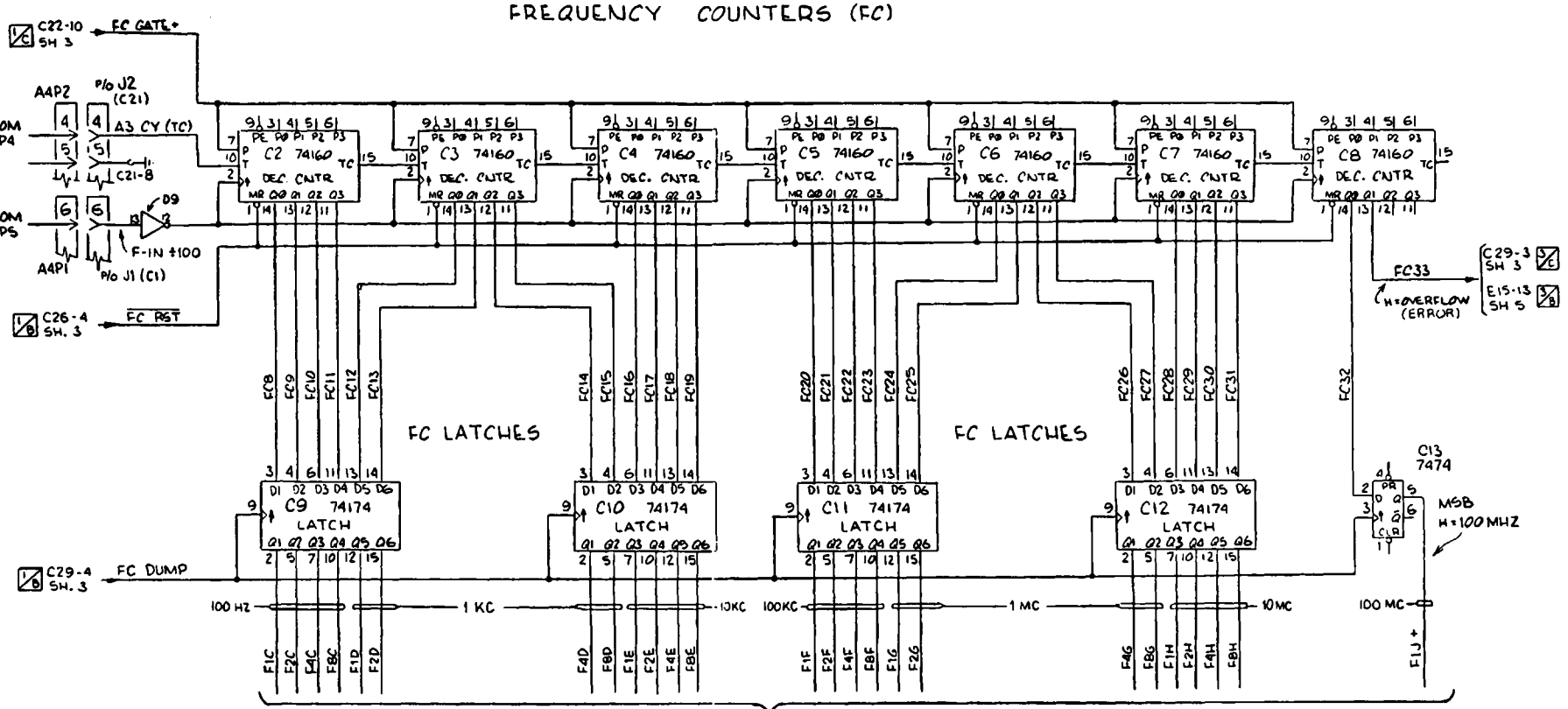
5MHz TIME BASE & CONTROL LOGIC

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY		DATE 12-81
DESIGNED BY		DATE 3-80
APPROVED BY		DATE

SHEET NUMBER 3 OF 7 | DRAWING NUMBER C13220L2 | REV. B | SCALE

FREQUENCY COUNTERS (FC)

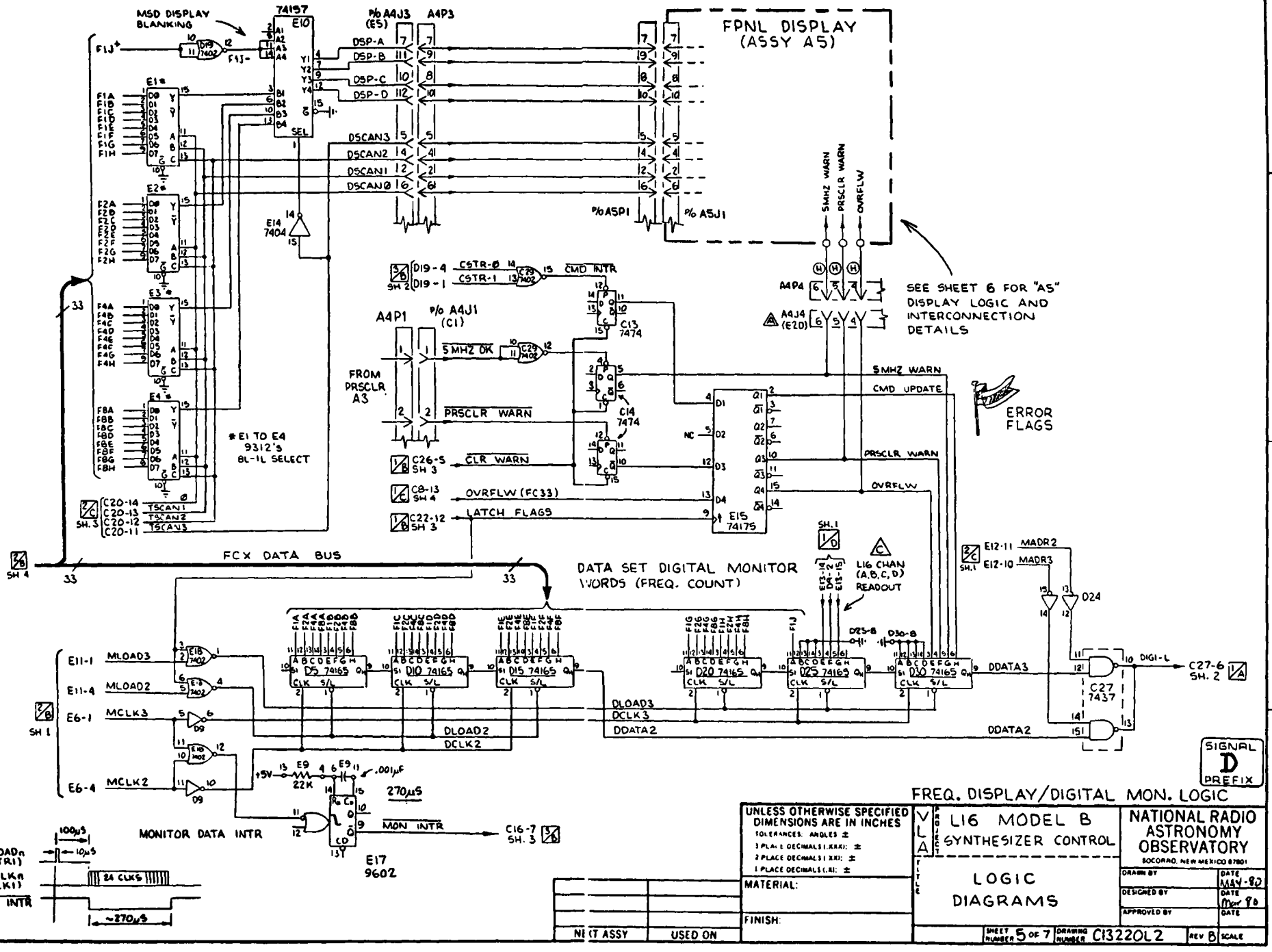


SIGNAL F PREFIX

FREQUENCY COUNTER LOGIC

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± 3 PLACE DECIMALS (.XXX): ± 2 PLACE DECIMALS (.XX): ± 1 PLACE DECIMALS (.X): ± MATERIAL: FINISH:	VLA PROJECT L16 MODEL B SYNTHESIZER CONTROL TITLE LOGIC DIAGRAMS	NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO NEW MEXICO 87801	DRAWN BY — DATE MAR-80 DESIGNED BY — DATE Mar 80 APPROVED BY — DATE
NEXT ASSY / USED ON	SHEET NUMBER 4 OF 7 — DRAWING NUMBER C13220L2 — REV. B — SCALE		

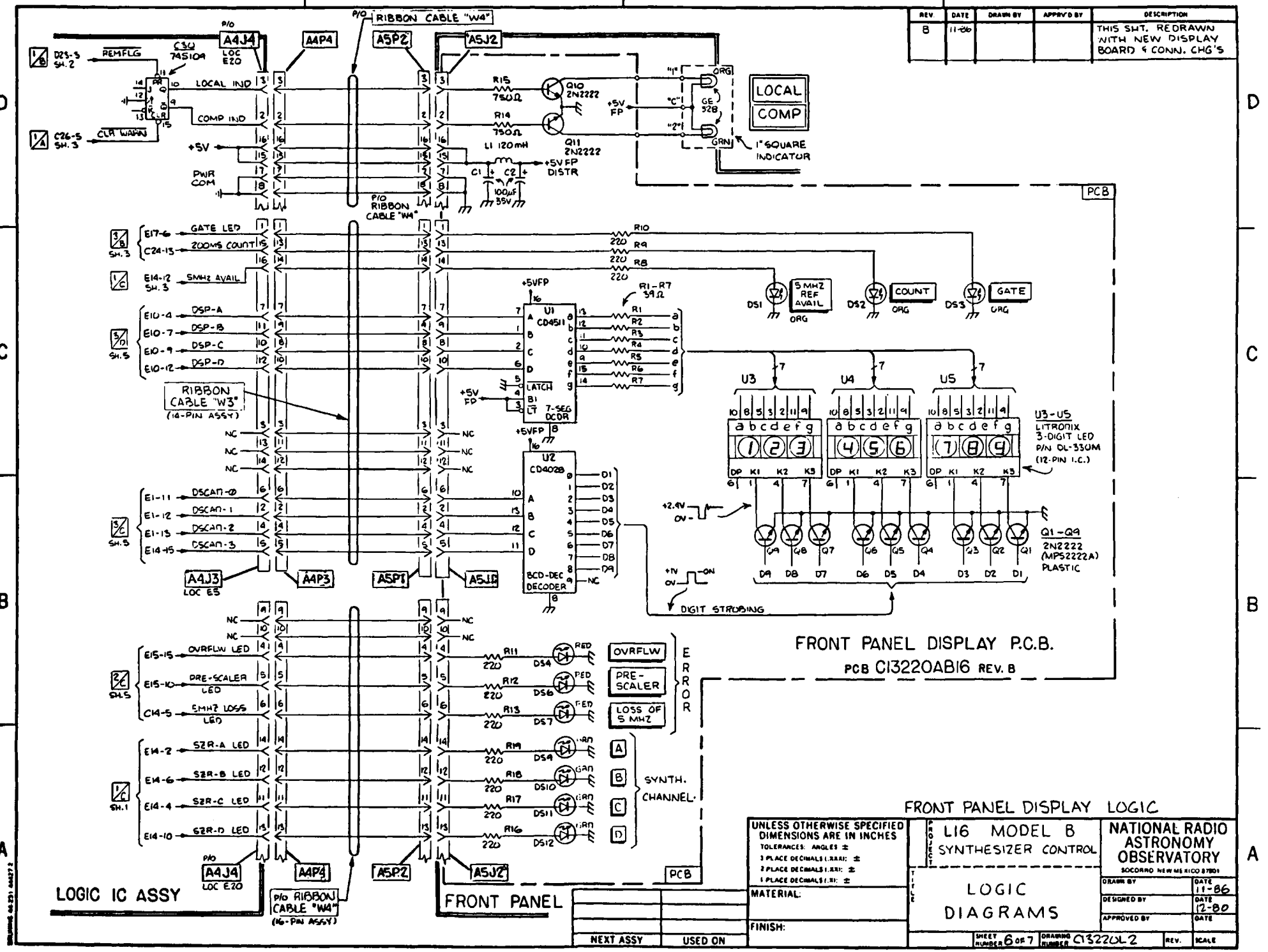
FREQUENCY DISPLAY MULTIPLEXING

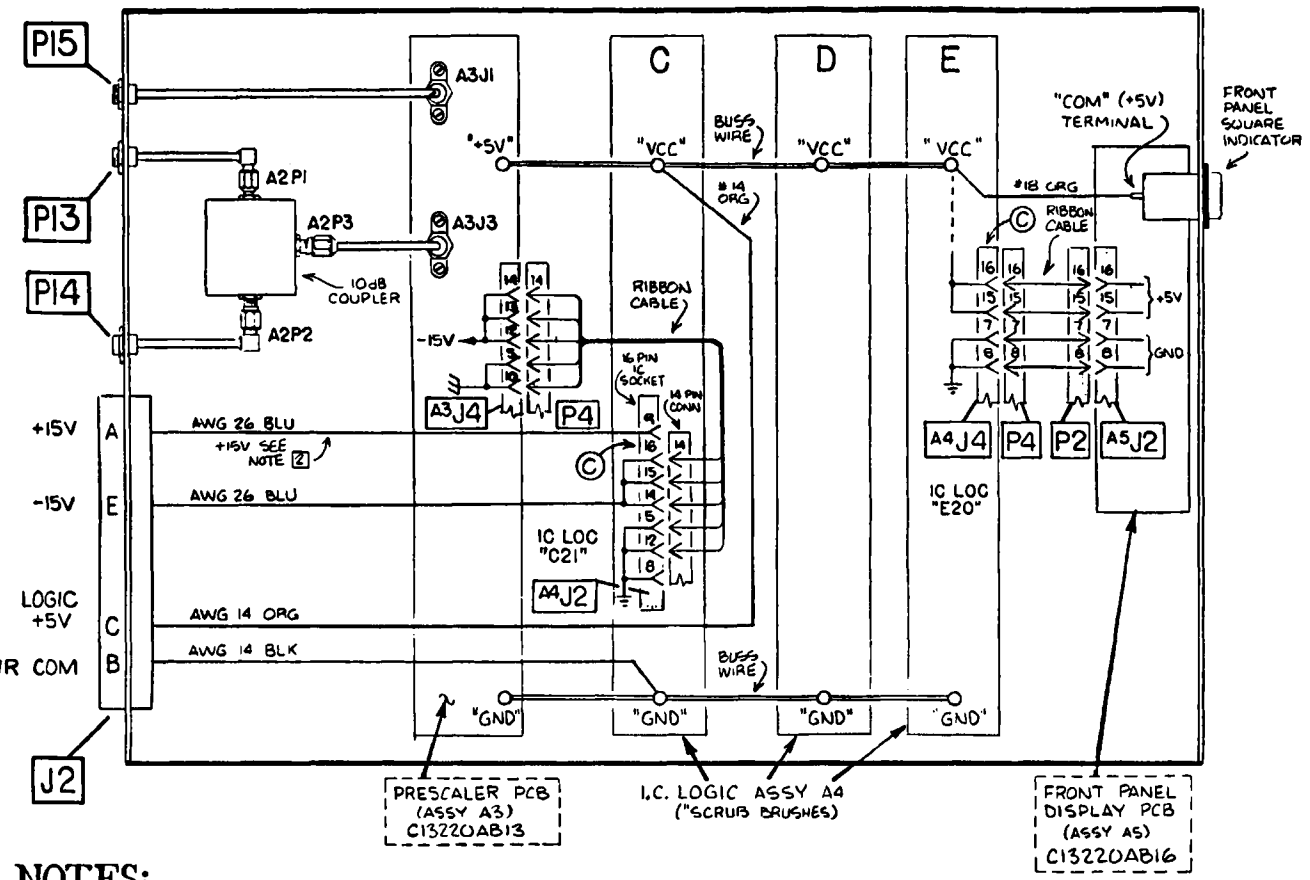


SIGNAL D PREFIX

FREQ. DISPLAY/DIGITAL MON. LOGIC

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± 3 PLACE DECIMALS (.XXX): ± 2 PLACE DECIMALS (.XX): ± 1 PLACE DECIMALS (.X): ±	VLA PROJECT: L16 MODEL B SYNTHESIZER CONTROL
MATERIAL:	FILE: LOGIC DIAGRAMS
FINISH:	NATIONAL RADIO ASTRONOMY OBSERVATORY, SOCORRO, NEW MEXICO 87801
NEXT ASSY / USED ON	DRAWN BY / DESIGNED BY / APPROVED BY; DATE M&Y-90 / Mar 90
	SHEET NUMBER 5 OF 7 · DRAWING NUMBER C13220L2 · REV B · SCALE


4
3
2
1
D
C
B
A
REV. | DATE | DRAWN BY | APPR'D BY | DESCRIPTION
B | 11-86 | | | THIS SHT. REDRAWN WITH NEW DISPLAY BOARD & CONN. CHG'S
P/O RIBBON CABLE "W4"
A4J4 LOC E20
A4P4
A5P2
A5J2
C3U 74S109
REMFLG
LOCAL IND
COMP IND
CLR WARN
+5V
PWR COM
R15 750Ω
R14 750Ω
Q10 2N2222
Q11 2N2222
L1 120mH
C1
C2
100µF 35V
+5V FP DISTR
LOCAL
COMP
"1"
"C"
"2"
ORG
GRN
GE 528
1" SQUARE INDICATOR
PCB
GATE LED
200MS COUNT
5MHz AVAIL
DSP-A
DSP-B
DSP-C
DSP-D
RIBBON CABLE "W3" (16-PIN ASSY)
DSCAN-0
DSCAN-1
DSCAN-2
DSCAN-3
A4J3 LOC E5
A4P3
A5P1
A5J1
U1 CD4511 BCD-TO 7-SEG DCDR
LATCH
BI
LT
R1-R7 39Ω
R10 220
R9 220
R8 220
DS1 5 MHZ REF AVAIL ORG
DS2 COUNT ORG
DS3 GATE ORG
U2 CD4028 BCD-DEC DECODER
U3
U4
U5
U3-U5 LITRONIX 3-DIGIT LED P/N DL-33UM (12-PIN I.C.)
+2.4V
0V
+5V
ON
DIGIT STROBING
Q1-Q9 2N2222 (MPS2222A) PLASTIC
OVRFLW LED
PRE-SCALER LED
5MHZ LOSS LED
SZR-A LED
SZR-B LED
SZR-C LED
SZR-D LED
R11 220 DS4 RED
R12 220 DS6 RED
R13 220 DS7 RED
R19 220 DS9 GRN
R18 220 DS10 GRN
R17 220 DS11 GRN
R16 220 DS12 GRN
OVRFLW
PRE-SCALER
LOSS OF 5 MHZ
ERROR
A
B
C
D
SYNTH. CHANNEL
P/O A4J4 LOC E20
A4P4
A5P2
A5J2
P/O RIBBON CABLE "W4" (16-PIN ASSY)
LOGIC IC ASSY
FRONT PANEL
PCB
FRONT PANEL DISPLAY P.C.B.
PCB C13220AB16 REV. B
FRONT PANEL DISPLAY LOGIC
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMAL (.X): ±
MATERIAL:
FINISH:
NEXT ASSY
USED ON
PROJECT L16 MODEL B SYNTHESIZER CONTROL
TITLE LOGIC DIAGRAMS
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO NEW MEXICO 87801
DRAWN BY DATE 11-86
DESIGNED BY DATE 12-80
APPROVED BY DATE
SHEET NUMBER 6 OF 7
DRAWING NUMBER C13220L2
REV.
SCALE



REAR PANEL CONNECTOR DATA

J2/P2 — 50-PIN AMP

PIN	FUNCTION
A	+15V PWR
B	LOGIC COMMON
C	+5V LOGIC
D	
E	-15V PWR
F	
H	SYNTH. REMOTE FLAG
J	SYNTH. POWER FLAG
K	SYNTH CMD LOGIC GND
L	LOGIC COMMON
M	SYNTH. CMD. BIT-0
N	
P	
R	
S	
T	
U	
V	
W	
X	
Y	
Z	
AA	SYNTH. RANGE BIT
BB	
CC	
DD	
EE	
FF	
HH	HI-Q GROUND

J1/P1 — 34-PIN AMP

PIN	FUNCTION
A	SMA-0
B	SMA-0 RET
C	SMA-1
D	SMA-1 RET
E	SMA-2
F	SMA-2 RET
H	SMA-3
J	SMA-3 RET
K	DIGO-0
L	DIGO-0 RET
M	CLKO-0
N	CLKO-0 RET
P	STRO-0
R	STRO-0 RET
S	
T	
U	
V	DIGI-1
W	DIGI-1 RET
X	CLKI-1
Y	CLKI-1 RET
Z	STRI-1
AA	STRI-1 RET
BB	SELECT CODE 1
CC	SELECT CODE 2
DD	SELECT CODE GND
EE	
FF	
HH	
JJ	
KK	
LL	
MM	
NN	

NOTES:

1. © CUT PIN 16 FROM POWER PLANE AT C21 (A4J2) AND E20 (A4J4)
2. +15VDC IS NOT USED IN L16 BUT AVAILABLE AT C21-9 AS SHOWN
3. DC POWER LOADING:

+5VDC	2.75 A
-15VDC	185 mA
+15VDC	NONE

INTERNAL CONNECTORS (RIBBON CABLES)

TO/FROM PRESCALER BOARD

A3 P4/J4 → A4 P4/J4				A3 P5/J5 → A4 P5/J4
FC4	1	14		SMHZ OK	1	14	RESET A5+
FC5	2	13	-15VDC	PRSCLR OK	2	13	FC0
LATCH A3+	3	12		PRSCLR OK	5	12	FC1
A3 CY	4	11			4	11	LATCH A5+
LOGIC RET	5	10	SMHZ RET	A3 ENBL	5	10	FC3
FC6	6	9	SMHZ CLK	F÷100	6	9	FC2
FC7	7	8		A5 RESET	7	8	GATE+

TO/FROM FRONT PANEL DISPLAY BOARD

A4 P3/J3 → A5 P1/J1				A4 P4/J4 → A5 P2/J2
GATE LED	1	14	SMHZ LED	NC	1	16	+5V
DSCAN-1	2	13	COUNT LED	COMP IND	2	15	FPNL
NC	3	12	NC	LOCAL IND	3	14	SZR-A LED
DSCAN-2	4	11	NC	OVRFLW LED	4	13	SZR-D LED
DSCAN-3	5	10	DSP-D	PRSCLR LED	5	12	SZR-B LED
DSCAN-0	6	9	DSP-B	SMHZ LED	6	11	SZR-C LED
DSP-A	7	8	DSP-C	POWER COM	7	10	NC
					8	9	NC

RF & DC PWR DISTRIBUTION / CONNECTOR INFO

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ANGLES ±
3 PLACE DECIMALS (.XXX): ±
2 PLACE DECIMALS (.XX): ±
1 PLACE DECIMALS (.X): ±
MATERIAL:
FINISH:

NEXT ASSY	USED ON

VLA — PROJECT: L16 MODEL B SYNTHESIZER CONTROL

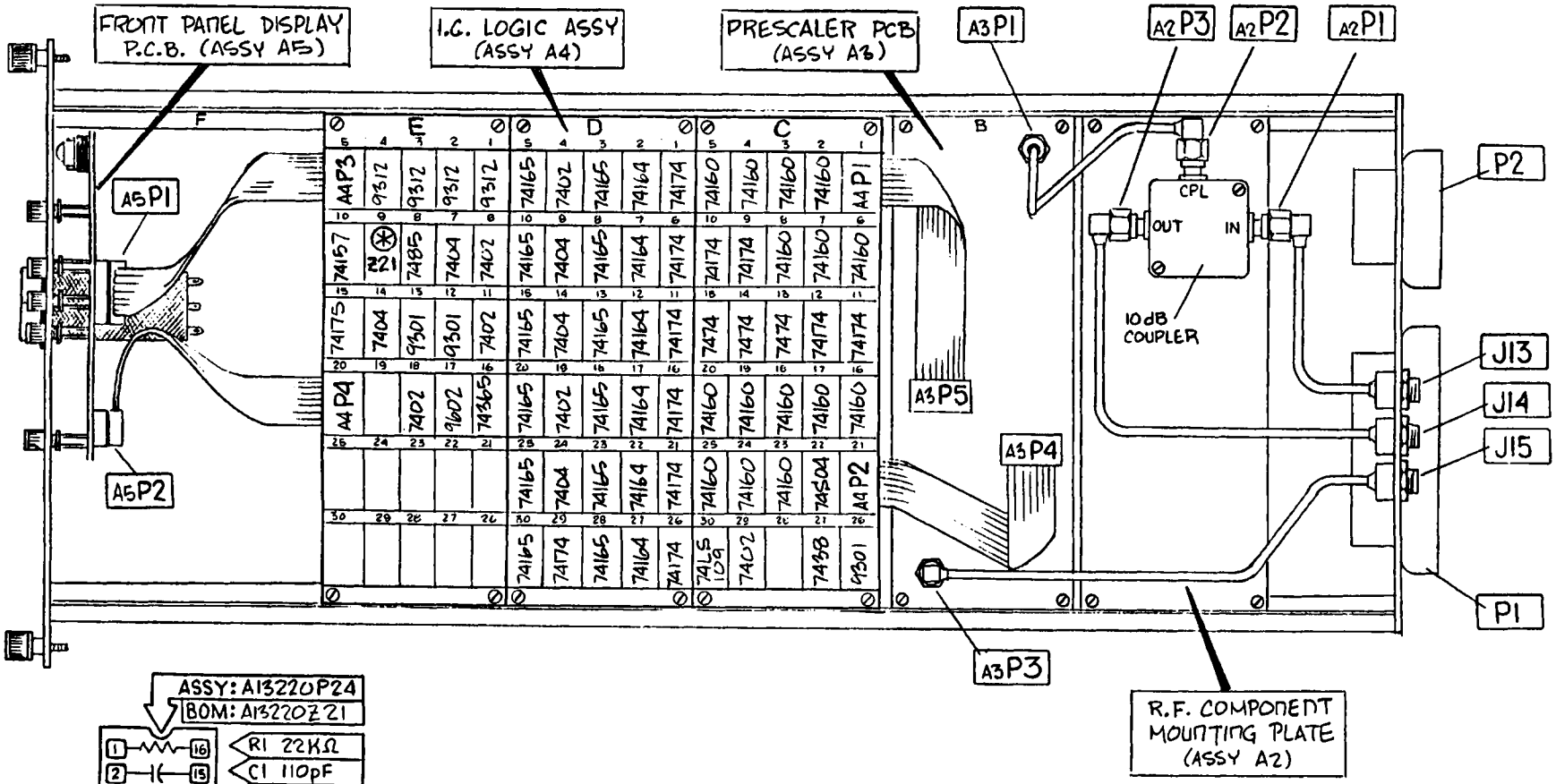
TITLE: LOGIC DIAGRAMS

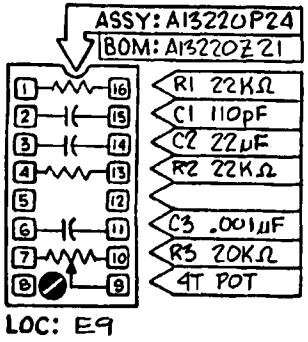
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE NOV 86
DESIGNED BY	DATE 12-80
APPROVED BY	DATE

SHEET NUMBER 7 OF 7 | DRAWING NUMBER C13220L2 | REV. | SCALE

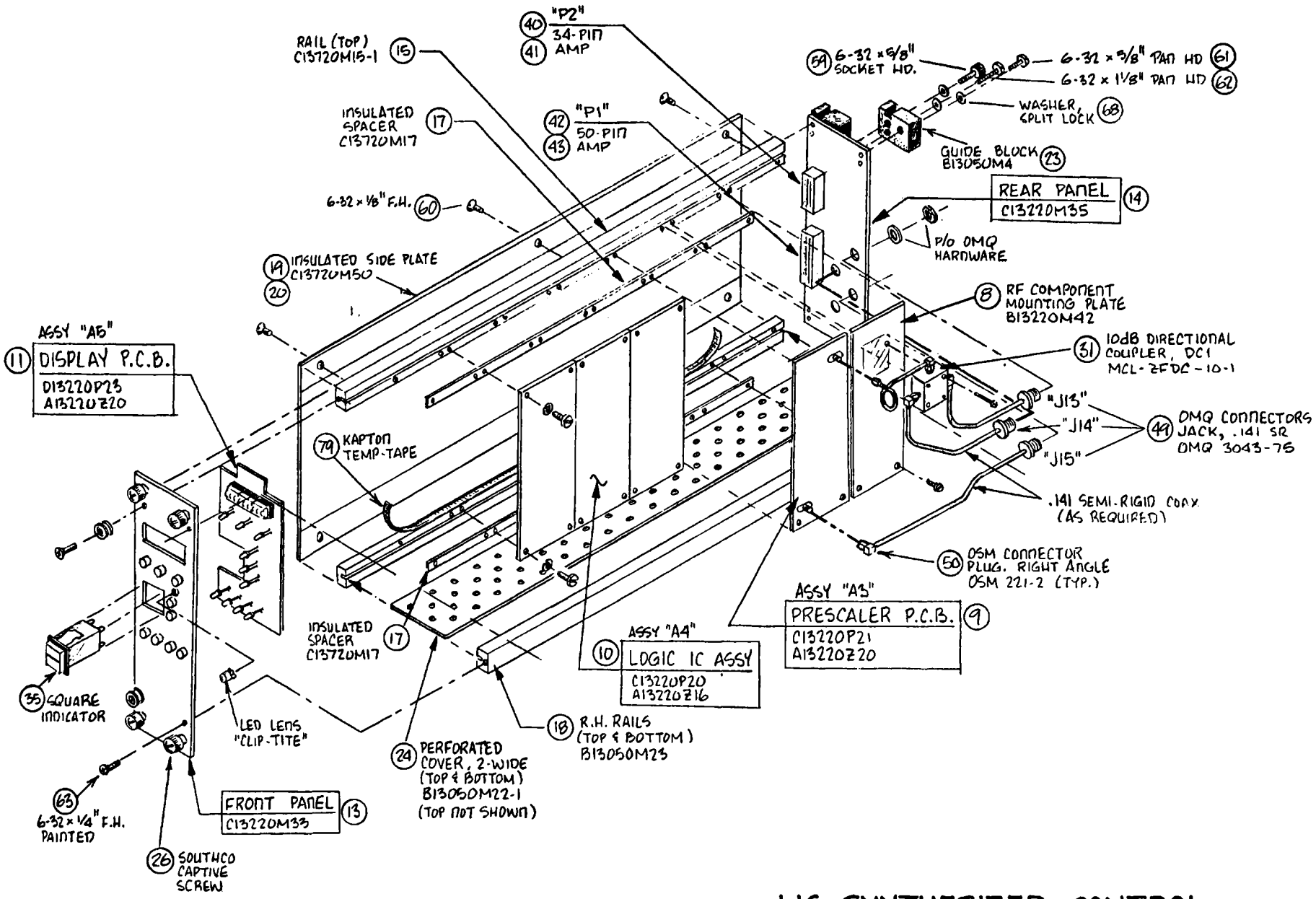
DRAWING A6 231 A6A272





LOC: E9

L16 SYNTHESIZER CONTROL
I.C. and COMPONENT LOCATIONS



L16 SYNTHESIZER CONTROL
EXPLODED VIEW
(ILLUSTRATED PARTS BREAKDOWN)

BILL OF M IAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☒ MECHANICAL BOM # A13220Z18 REV B DATE 31 OCT 1980 PAGE 1 OF 5
REV: 10 JUL 1981

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
1		NRAO	A13220Z18	L16-SYNTHESIZER CONTROL	–	
2						
3			A13220W10	WIRE LIST- MASTER		
4			A13220W11	WIRE LIST- MACHINE		
5			A13220W12	WIRE LIST- HAND		
6			A13220W13	WIRE LIST- CONNECTOR		
7						
8	A2		B13220M42	R.F. CHASSIS SUB-ASSY	1	
9	A3		A13220Z17/P21	PRESCALER SUB-ASSY	1	
10	A4		A13220Z16/P20	I.C. MODULE PANEL SUB-ASSY	1	
11	A5		D13220P23 A13220Z20	L.E.D. DISPLAY SUB-ASSY	1	
12						
13	P/O A5		C13220M33	PANEL, FRONT	1	
14	A1		C13220M35	PANEL, REAR	1	
15			C13720M15-1	RAIL, MODIFIED (TOP LEFT)	1	
16			C13720M15-2	RAIL, MODIFIED (BOTTOM LEFT)	1	
17		NRAO	C13720M17	RAIL, INSULATED SPACER	2	

BILL OF IAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☒ MECHANICAL BOM # A13220Z18 REV B DATE 31 OCT 1980 PAGE 2 OF 5

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
18		NRAO	B13050M23	RAIL, SIDE SUPPORT (R.H. SIDES)	2	
19			C13720P68	SIDE PLATE (L.H. SIDE)	1	
20			B13720M49	INSULATION (FOR # 7 ABOVE)	1	
21			B13050M18	SIDE PLATE (R.H. SIDE)	1	
22			B13720M47	RAIL, END SPACER	4	
23			B13050M4	GUIDE BLOCK	4	
24			B13050M22-1	COVER, PERFORATED (2UA)	2	
25		NRAO	(T.A.D. NOTE)	DISPLAY FILTER (RED)	1	
26		SOUTHCO MFG.	47-10-204-10	CAPTIVE SCREW	4	
27		NRAO			2	
28						
29						
30						
31	DC1	MINI-CIRCUITS LAB	MCL-ZFDC10-1	DIRECTIONAL COUPLER, 10dB	1	
32	A4P1, P2	A-P PRODUCTS	924108-6	JUMPER CABLE, 14-PIN, 8 INCH	2	
33	A4P3	A-P PRODUCTS	924110-6	JUMPER CABLE, 14-PIN, 10 INCH	1	
34	A4P4	CANNON	CA16P-11MW	I.C. DIP PLUG	1	

BILL OF M IAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☒ MECHANICAL BOM # A13220218 REV B DATE 31 OCT 1980 PAGE 3 OF 5

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
35	DS7, DS8	ELECTROMECH	674-3210L815-C-GY-V328	INDICATOR, SQUARE, 2-COLOR	1	
36			XC556 CLIPLITE	L.E.D. LENS/MOUNT	10	
37						
38						
39						
40	P2	AMP SPECIAL INDUSTRIES	601488-2	CONNECTOR, 34-PIN	1	
41		↓	202434-4	SHIELD, 34-PIN CONN.	1	
42	P1		601488-3	CONNECTOR, 50-PIN	1	
43			202394-2	SHIELD, 50-PIN CONN.	1	
44			200833-4	GUIDE PIN	2	
45			202514-1	GUIDE PIN (GROUND)	2	
46			202964-6	GUIDE SOCKET	4	
47		↓	204219-1	CONNECTOR PIN, CRIMP	2	
48		AMP SPECIAL INDUSTRIES	66460-6	CONNECTOR PIN, WIRE WRAP	80	
49	J13-J15	OMNI-SPECTRA	OMQ-3043-75	JACK, .141SR BULKHEAD	3	
50	A2P1, A2P2 A3P1, A3P3	↓	OSM 221-2	PLUG, RIGHT ANGLE, .141SR	4	
51	A2P4	↓	OSM 201-2A	PLUG, .141 SEMI-RIGID	1	

BILL OF IAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☒ MECHANICAL BOM # A13220218 REV B DATE 31 OCT 1980 PAGE 4 OF 5

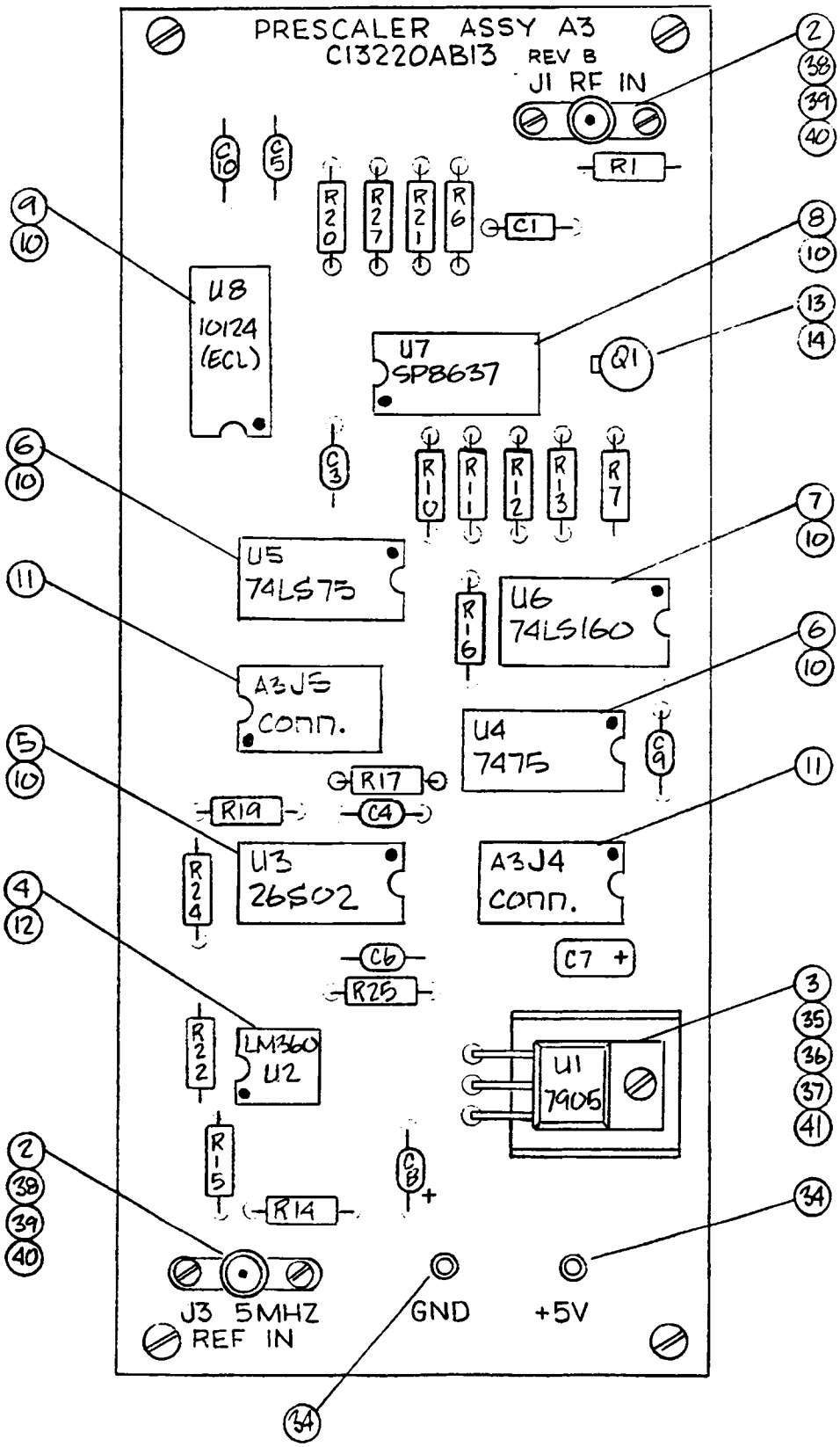
ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
52	A2P3	OMNI-SPECTRA	OSM 219	ADAPTER, RIGHT ANGLE, PLUG/JACK	1	
53						
54	"+5V"	H.H. SMITH	2010D	TERMINAL, SPLIT-LUG	4	
55	"GND"	H.H. SMITH	2025D	TERMINAL, MIN. THROUGH	4	
56		G.C. ELECTRONICS	5706-C	SOLDER LUG	3	
57						
58						
59		BOSCO OR EQUIV.	6-32 × 5/8	SCREW, HEX SOCKET	2	
60			6-32 × 1/8	SCREW, ~~PAN HD~~ FLAT HD.	14	
61			6-32 × 5/8	SCREW, PAN HD.	4	
62			6-32 × 1 1/8	SCREW, PAN HD.	4	
63			6-32 × 1/4	SCREW, FLAT HD (PAINTED)	2	
64			4-40 × 3/8	SCREW, PAN HD	16	
65			4-40 × 1/2	SCREW, PAN HD	4	
66			4-40	NUT, ST. STEEL, HEX	4	
67			#2	WASHER, FLAT	4	
68			#4	WASHER, SPLIT-LOCK	16	

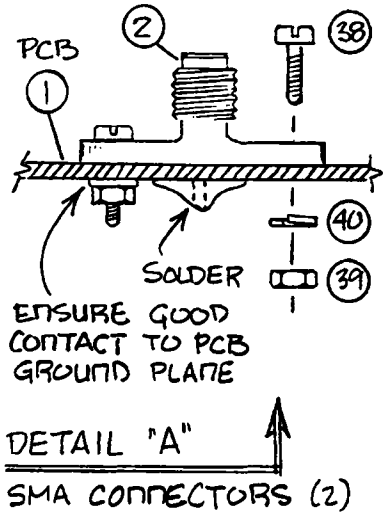
BILL OF IAL

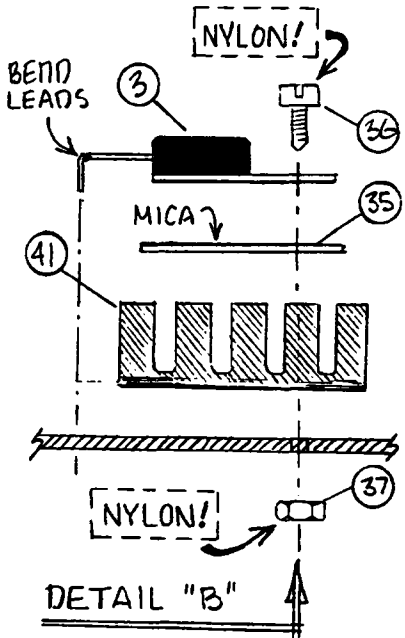
NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☒ MECHANICAL BOM # A13220718 REV B DATE 31 OCT 1980 PAGE 5 OF 5

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
69		BOSCO OR EQUIV.	#6	WASHER, EXT. TOOTH	12	
70						
71						
72		ALPHA WIRE CO.	286	WIRE, BUS TINNED COPPER #14	A/R	
73		ALPHA WIRE CO.	PVC-105/6	PLASTIC TUBING, .066 DIA. PVC	A/R	
74				WIRE, #16 STRANDED (BLK & ORG)	A/R	
75				WIRE, #22 STRANDED	A/R	
76				WIRE, #26 SOLID KYNAR	A/R	
77				WIRE, #30 SOLID KYNAR	A/R	
78						
79		CONN. HARD RUBBER CO.	K350	KAPTON TEMP-R-TAPE 32/64"	A/R	







BOM: A13220Z17

L16 SYNTHESIZER CONTROL

ASSY A3 - PRESCALER P.C.B. ASSEMBLY DETAILS

BILL OF [illegible]

NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☒ MECHANICAL BOM # A13220217 REV B DATE 16MAR 80 PAGE 1 OF 3
REV: 29 SEP 83

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
1		NRAO	C13220AB13	PRESCALER ASSY P.C.B.	1	
2	J1, J2	OMNI-SPECTRA	OSM 244-2	CONNECTOR, SMA P.C. MOUNT	2	
3	U1	NATIONAL, OR EQUIV.	LM320K-5.2	I.C., REGULATOR TO-220 -5.2v	1	
4	U2	↓	LM160N	I.C., COMPARATOR (8-PIN DIP)	1	
5	U3	↓	26S02	I.C., ONE-SHOT	1	
6	U4, U5	↓	74LS75	I.C., QUAD LATCH	2	
7	U6	↓	74LS160	I.C., DEC. COUNTER	1	
8	U7	PLESSY SEMICONDUCTOR	SP8637B	I.C., 400MHz ÷10 PRESCALER	1	
9	U8	FAIRCHILD	10124	I.C., TTL-ECL TRANSLATOR	1	
10	-	T.I. OR EQUIV.	C8516	SOCKET, I.C., 16-PIN, S.T.	6	
11	-		C8514	SOCKET, I.C., 14-PIN, S.T.	2	
12	-		C8508	SOCKET, I.C., 8-PIN, S.T.	1	
13	Q1	SYLVANIA OR EQUIV.	2N2907	TRANSISTOR, TO-5	1	
14	-			SOCKET, TO-5 TRANISTOR	1	
15	C1	MALLORY		CAP., 1000pF NPO	1	
16	C2			CAP., 33pF NPO CHIP	1	
17	C3, C5, C9			CAP., 0.1μF	3	

BILL OF [illegible]

NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☒ MECHANICAL BOM # A13220217 REV B DATE 16MAR 80 PAGE 2 OF 3
REV: 29SEP 83

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
18	C4			CAP., 100pF	1	
19	C6			CAP., 30pF	1	
20	C7			CAP., 2.2μF	1	
21	C8			CAP., 1.0μF	1	
22	C10			CAP., 0.01μF	1	
23	R1, R14			RES., 51Ω 1/8W	2	
24	R6, R19-20			RES., 2K	3	
25	R7, R16			RES., 1K	2	
26	R10-R13			RES., 10K	4	
27	R15			RES., 7.5K	1	
28	R17			RES., 30K	1	
29	R21			RES., 68K	1	
30	R22			RES., 200K	1	
31	R24			RES., 2.4K	1	
32	R25			RES., 39K	1	
33	R27			RES., 820Ω	1	
34	"+5", "GND"	H.H. SMITH	2025D	TERMINAL LUG, SOLDER	2	

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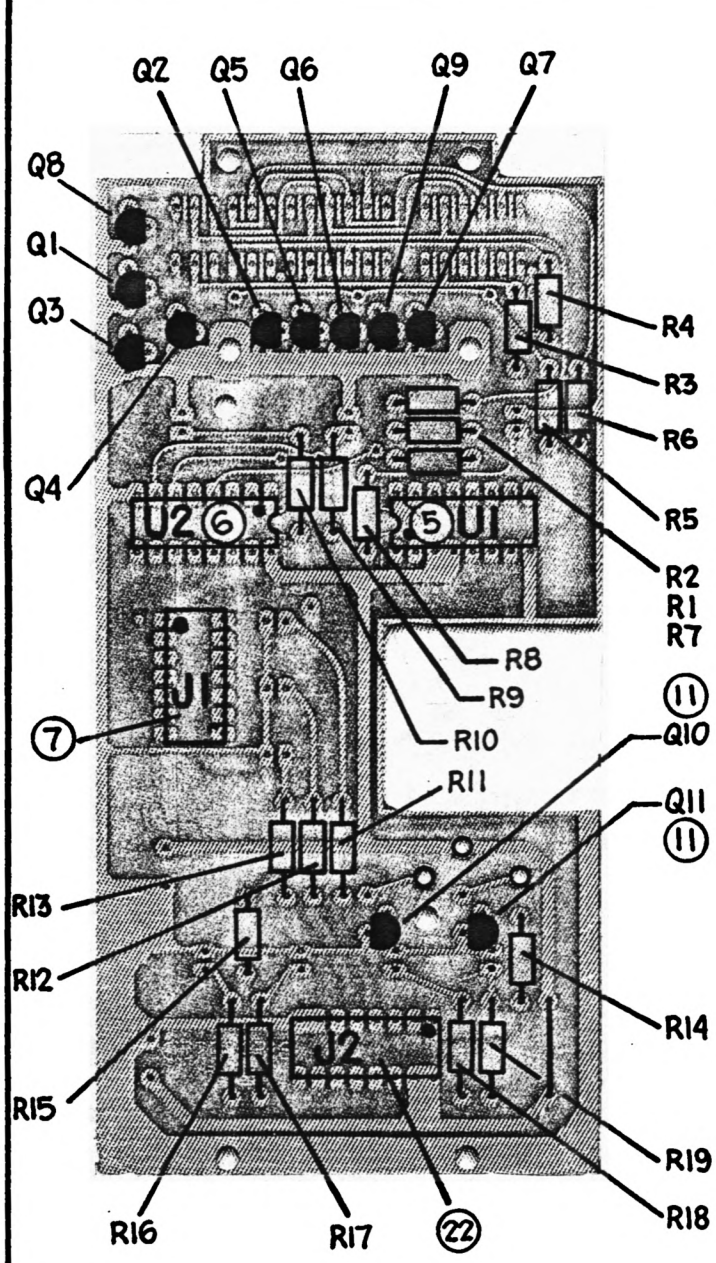
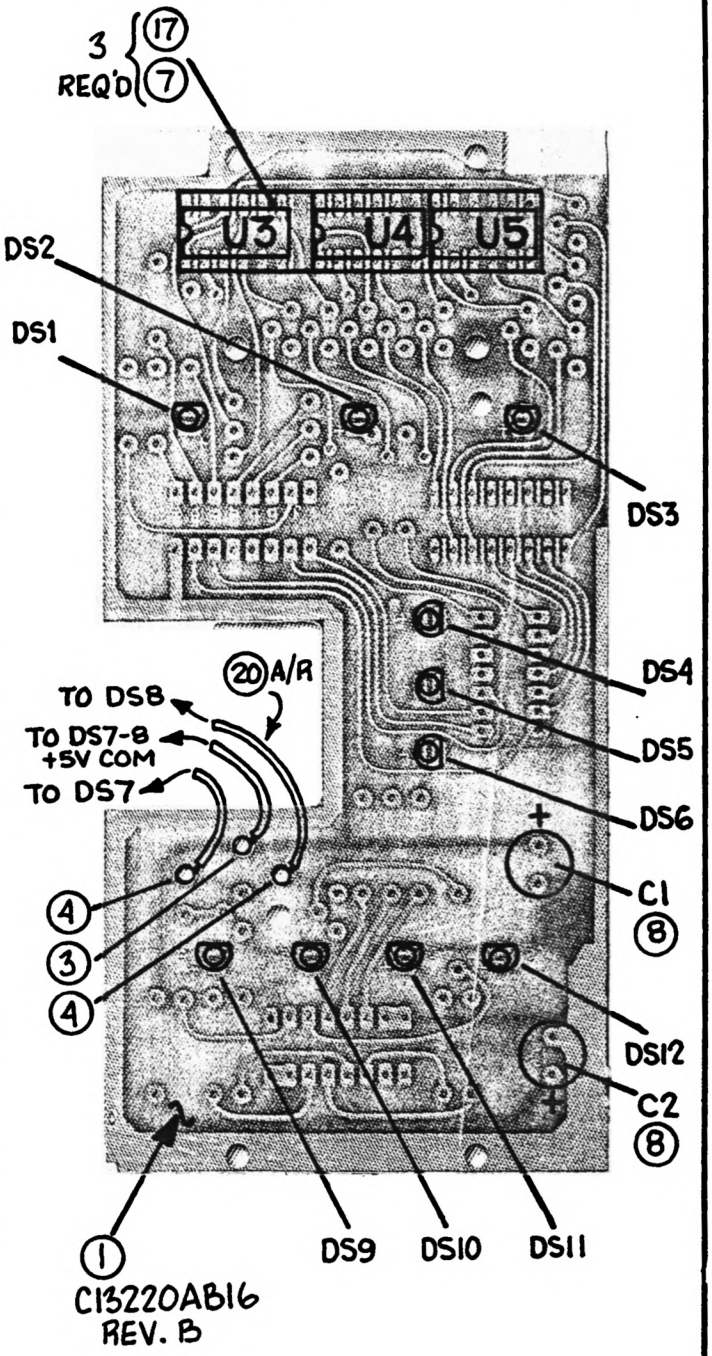
NATIONAL RADIO ASTRONOMY OBSERVATORY

☐ ELECTRICAL ☒ MECHANICAL BOM # A13220217 REV B DATE 16MAR 80 PAGE 3 OF 3

REV: 29 SEP 83

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
35				MICA INSULATOR, TO-220	1	
36		AMATOM OR H.H. SMITH	4-40 x 1/4 LG	SCREW, NYLON 4-40	1	
37		" " "	HHS 2554	NUT, HEX NYLON 4-40	1	
38		ACME NUT & BOLT	2-56 x 1/4 PH	SCREW 2-56 PAN HD.	6	
39			2-56	NUT, HEX 2-56	6	
40			#4	WASHER, SPLIT LOCK	6	





RESISTORS

ITEM (15)	R8-R13, R16-R19	220Ω	1/4W
(16)	R14, R15	750Ω	1/4W
(18)	R1-R7	39Ω	1/4W

TRANSISTORS

ITEM (10)	Q1-Q9	2N2222
(11)	Q10, Q11	2N2219

L.E.D.'s

ITEM (12)	DS4, DS5, DS6	T-1 3/4 RED
(13)	DS9 - DS12	T-1 3/4 GREEN
(14)	DS1, DS2, DS3	T-1 3/4 AMBER

BOM: A13220Z20

PROJECT	L16 MODEL B	NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801
TITLE	FRONT PANEL PCB (A5) ASSEMBLY	DRAWN BY — DATE 5-86
		DESIGNED BY — DATE 4-89
		APPROVED BY — DATE
	SHEET NUMBER 1 — DRAWING NUMBER — REV. B — SCALE	

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

☒ ELECTRICAL ☐ MECHANICAL BOM # A13220220 REV C 4-84 DATE 6NOV1980 PAGE 1 OF 2

L16 DISPLAY (ASSY A5) PCB B.O.M.

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
1A	A5-1	NRAO	C13220AB16-1	PRINTED CIRCUIT A5-1	1	
1B	A5-2		C13220AB16-2	PRINTED CIRCUIT A5-2.	1	
2						
3	+5V, GND	H.H. SMITH CO.	HHS 2010	TERMINAL, SPLIT LUG	2	
4	+5, G, Y	H.H. SMITH CO.	HHS 1502-4	TERMINAL, MIN. THROUGH	3	
5	U1	RCA (OR EQUIV)	CD4511	I.C., DISPLAY DECODER (CMOS)	1	
6	U2	RCA (OR EQUIV)	CD4028	I.C., DECIMAL DECODER (CMOS)	1	
7	A5J1	T.I. (OR EQUIV.)	C8114-ST	SOCKET, 14-PIN I.C., IN-LINE	4	
8	C1, C2	PANASONIC	220-10R	CAPACITOR, ELECTROLYTIC 220μF	2	
9	L1	NYTRONICS	WEE100	INDUCTOR, 100μH 5%	1	
10	Q1-Q9	T.I. (OR EQUIV.)	2N2222	TRANSISTOR, NPN-HSS, PLASTIC	9	
11	Q10, Q11	T.I. (OR EQUIV.)	2N2219	TRANSISTOR, NPN-HSS, METAL TO-5	2	
12	DS4-DS6	H.P. (OR EQUIV.)	5082-4655	L.E.D., T1-3/4, RED	3	
13	DS9-DS12	H.P. (OR EQUIV.)	5082-4955	L.E.D., T1-3/4, GREEN	4	
14	DS1-DS3	H.P. (OR EQUIV)	5082-4555	L.E.D., T1-3/4, AMBER	3	
15	R8-R13 R16-R19	A-B	RCR07G221J	RESISTOR, 220Ω 5% 1/4 W	10	
16	R14, R15	A-B	RCR07G751J	RESISTOR, 750Ω 5% 1/4 W	2	

A13220220

BILL OF MATERIAL

NATIONAL RADIO ASTRONOMY OBSERVATORY

☒ ELECTRICAL ☐ MECHANICAL BOM # A13220220 REV C 4-84 DATE 6NOV1980 PAGE 2 OF 2

ITEM #	REF DESIG	MANUFACTURER	MFG PART #	DESCRIPTION	TOTAL QUA	
17	U3-U5	LITRONIXS	DL-330M	I.C., TRIPLE 7-SEG DISPLAY	3	
18	R1-R7	A-B	RCR07G390J	RESISTOR, 39Ω 5% 1/4W	7	
~~19~~		~~H.H. SMITH~~		~~SPACER, THREADED 4-40×1/4~~	~~4~~	
19		ALPHA WIRE CO	RX26C-10P	RIBBON CABLE, 10 COND #26 SOLID	A/R	
20		ALPHA WIRE CO	#22	WIRE, #22 STRANDED	A/R	
21	TERM. DS4-DS12	AUGAT	314-17PS	WIRE WRAP PIN	9	
22	A5J2	T.I. (or Equiv.)	C8116-ST	SOCKET, I.C., 16-PIN	1	

A13220220

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8634B ÷ 10 700 MHz
SP8636B ÷ 10 500 MHz
SP8635B ÷ 10 600 MHz
SP8637B ÷ 10 400 MHz

The SP8634B, SP8635B, SP8636B and SP8637B are divide-by-ten circuits with binary coded decimal outputs for operation from DC up to specified input frequencies of 700, 600, 500 and 400 MHz, respectively, over a guaranteed temperature range of 0°C to +70°C.

These devices, optimised for counter applications in systems using both ECL and TTL, are intended to be operated between 0V and −5.2V power rails and to interface with TTL operating between 0V and +5V. The BCD outputs and one of two carry outputs are TTL-compatible, while the second carry output is ECL-compatible. The clock input, which is normally capacitively coupled to the signal source, is gated by an ECL III/ECL 10k-compatible input. The TTL-compatible reset forces the 0000 state regardless of the state of the other inputs.

FEATURES

- Direct gating capability at up to 700 MHz
- TTL-compatible BCD outputs
- TTL and ECL-compatible carry outputs
- Power consumption less than 500 mW
- Wide dynamic input range

APPLICATIONS

- Counters
- Timers
- Synthesisers

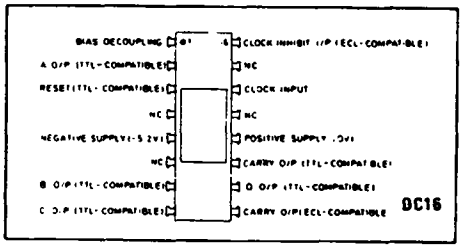


Fig. 1 Pin connections (top)

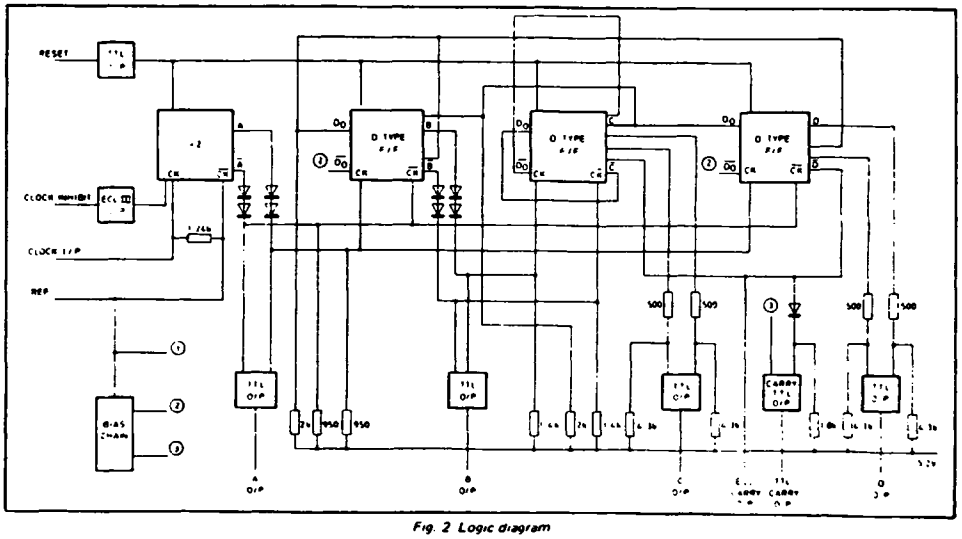


Fig. 2 Logic diagram

QUICK REFERENCE DATA

Power Supplies	V_{CC}	0V
	V_{EE}	5.2V ± 0.25V
Range of clock input amplitude		400-800mV p-p
Operational temperature range		0°C to +70°C
Frequency range with sinusoidal I/P		40-700 MHz (SP8634B)
Frequency range with square wave I/P		DC to 700 MHz (SP8634B)

ELECTRICAL CHARACTERISTICS (All types except where otherwise stated)

Test Conditions (unless otherwise stated)

T_{amb}		0°C to +70°C
Power Supplies	V_{CC}	0V
	V_{EE}	−5.2V ± 0.25V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Clock Input (pin 14)					
Max. input frequency					
SP8634B	700			MHz	Input voltage 400-800mV p-p
SP8635B	600			MHz	
SP8636B	500			MHz	
SP8637B	400			MHz	
Min. input frequency with sinusoidal I/P			40	MHz	
Min. slew rate of square wave for correct operation down to DC			100	V/μs	
Clock inhibit input (pin 16)					
Logic levels					
High (inhibit)	−0.960			V	T_{amb} = +25°C
Low			−1.650	V	(see Note 1)
Edge speed for correct operation at maximum clock I/P frequency			2.5	ns	10%–90%
Reset input (pin 3)					
Logic levels					
High (reset)	See Note 2				
Low			+0.4	V	
Reset ON time	100			ns	
TTL outputs ABCD (pins 2,7,8,10)					See Note 3 and Fig. 4
Output Voltage					
High	+2.4			V	10k Ω resistor and TTL gate from O/P
Low			+0.4	V	to +5V rail
TTL carry output (pin 11)					
Output Voltage					
High state	+2.4			V	5kΩ resistor and 3 TTL gates from o/p
Low			+0.4	V	to 5V rail
ECL carry output (pin 9)					
Output Voltage					
High	−0.975			V	T_{amb} = +25°C External current
Low			−1.375	V	= 0mA (See Note 4)
Power supply drain current		75	90	mA	V_{EE} = 5.2V

NOTES

1 The clock inhibit input levels are compatible with ECL III and ECL 10000 levels throughout the temperature range 0°C to +70°C

2 For a high state, the reset input requires a more positive input level than the specified worst case TTL V_{OH} of +2.4V. Resetting should be done by connecting a 1.8k Ω resistor from the output of the driving TTL gate and only fanning out to the reset input of the SP8000 series device

3 These outputs are current sources which can be readily made TTL compatible voltages by connecting them to +5V via 10kΩ resistors

4 The ECL carry output is compatible with ECL II throughout the temperature range but can be made compatible with ECL III using the simple interface shown in Fig. 3

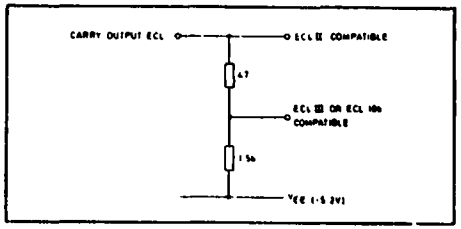


Fig. 3 ECL III/ECL 10000 interfacing

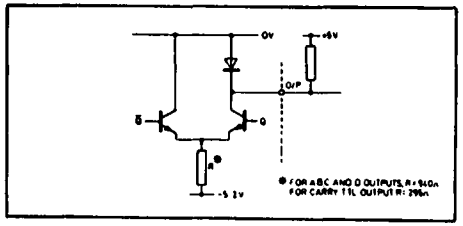


Fig. 4 TTL carry and ABCD output structure

OPERATING NOTES

The devices are intended to be used with TTL and ECL in a counting system – the ECL and the decade counter being connected between voltage rails of 0V and −5.2V and the TTL between voltage rails of 0V and +5.0V. Provided that this is done ECL and TTL compatability is achieved (see Figs. 4 and 5).

The clock is normally capacitively coupled to the signal source: a 1000pF UHF capacitor is normally adequate. If low frequency operation is required the 1000pF capacitor should be connected in parallel with a higher value capacitor. The bias decoupling (pin 1) should be connected to earth via a capacitor – preferably a chip type – but in any case a low inductance type suitable for UHF applications. The devices normally have an input amplitude operating range far greater than the specified 400 to 800 mV pk/pk. However, if the decoupling capacitor is not of a UHF type, or it is connected to an earth point that has a significant impedance between the capacitor and the V_{CC} connection, then the input dynamic range will suffer and the maximum signal for correct operation will be reduced.

Under certain conditions, the absence of an input signal may cause the device to self-oscillate. This can be prevented (while still maintaining the specified input sensitivity) by connecting a 68kΩ resistor between the clock input and the negative supply. If the transition of either the clock input or the clock inhibit input is slow the device may start to self-oscillate during the transition. For this reason, the input slew rates should be greater than 100 V/μs. It should also be noted that a positive-going transition on either the clock input or the clock inhibit input will clock the device, provided that the other input is in the low state.

The BCD outputs give TTL compatible outputs (fanout = 1) when a 10kΩ resistor is connected from the output to the +5V rail. In this configuration the outputs will be very slow compared with the clocking rate of the decade and so the state on the BCD outputs can only be determined when the clock has stopped or is inhibited.

The fan out capability of the TTL carry output can be increased by buffering it with a PNP emitter follower. The interface is shown in Fig. 5.

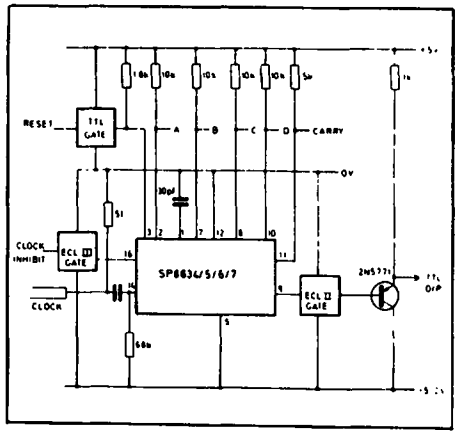


Fig. 5 Typical application configuration

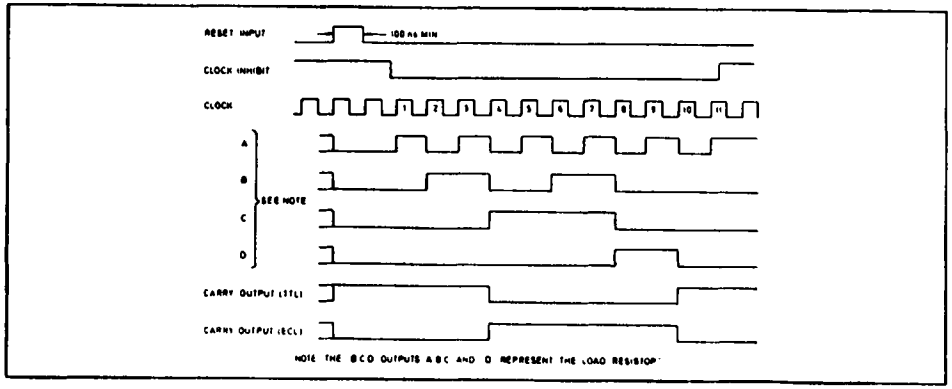
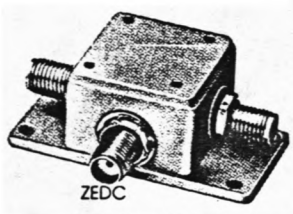


Fig. 6 Decade counter timing diagram

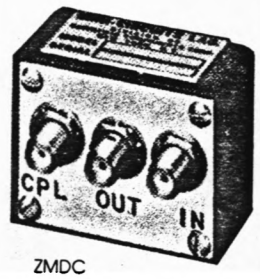
50 ohms and 75 ohms

Mini-Circuits

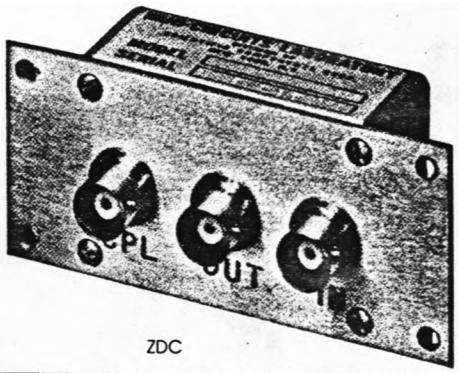
L16


ZEDC


ZFDC
ZFDC-H



ZMDC



ZDC

	MODEL NO.	FREQ. MHz f_L-f_U	COUPLING dB Nom.	COUPLING dB Flatness	MAINLINE LOSS* dB L Typ.	L Max.	M Typ.	M Max.	U Typ.	U Max.	DIRECTIVITY dB L Typ.	L Min.	M Typ.	M Min.	U Typ.	U Min.	VSWR Typ.	POWER INPUT, W L Max.	M,U Max.	PRICE, $ Ea.	Qty.
ZEDC case V37	ZEDC-10-2B	1-1000	11±0.5	±0.75	1.3	1.5	1.5	1.8	1.5	1.8	35	30	30	20	18	13	1.3	1.5	3	54.95	(4-24)
	ZEDC-15-2B	1-1000	15±0.5	±0.5	0.5	1.0	0.8	1.2	1.0	1.4	35	30	30	25	25	15	1.15	1.5	3	54.95	(4-24)
ZFDC case K18	ZFDC-10-1	1-500	10.5±0.25	±0.6	1.0	1.3	0.8	1.1	1.0	1.3	32	25	33	25	22	15	1.2	1.5	3	29.95	(4-24)
	ZFDC-10-2	10-1000	10.75±0.5	±0.5	1.5	2.0	1.2	1.6	1.5	2.0	35	28	30	25	27	20	1.5	1.5	3	39.95	(4-24)
	ZFDC-10-6	0.005-20	11±0.5	±0.5	0.4	1.2	0.4	0.8	0.4	1.0	40	30	40	30	35	25	1.3	1.5	3	38.95	(4-24)
	△ZFDC-10-21	1-1000	11±0.5	±0.5	1.2	1.7	1.2	1.7	1.6	2.0	40	30	25	20	25	20	1.2	1	2	44.95	(4-24)
	ZFDC-10-21-75	10-750	11±0.5	±0.75	1.5	1.8	1.5	1.9	1.7	2.1	36	30	30	20	26	20	1.4	1	2	44.95	(4-24)
	ZFDC-10-22	1-750	11±0.5	±0.5	1.1	1.6	1.2	1.7	1.4	1.9	35	30	25	20	25	20	1.25	1	2	34.95	(4-24)
	ZFDC-15-5	1-2000	15.5±0.5	±1.0	1.0	1.8	1.2	1.8	1.3	2.3	30	20	25	20	18	11	1.3	0.5	2	79.95	(1-4)
	ZFDC-15-6	0.03-35	15±0.5	±0.5	0.3	0.6	0.2	0.4	0.3	0.6	38	30	35	25	28	20	1.15	2	4	34.95	(4-24)
	■ZFDC-15-6-75	0.02-35	14.5±0.5	±0.5	0.3	0.7	0.3	0.7	0.3	0.7	35	20	35	20	35	20	1.3	1.5	4	35.95	(4-24)
	ZFDC-20-3	0.2-250	19.5±0.5	±0.25	0.35	0.6	0.25	0.5	0.35	0.6	36	25	33	25	25	20	1.2	1.5	4	29.95	(4-24)
	■ZFDC-20-3-75 NEW	10-250	19.3±0.5	±0.3	0.25	0.4	0.3	0.5	0.4	0.6	29	25	29	25	28	24	1.2	1	2	35.95	(4-24)
	ZFDC-20-4	1-1000	19.5±0.5	±0.5	1.2	1.5	0.6	0.8	1.2	1.5	36	28	27	20	23	18	1.1	5	2	59.95	(1-4)
	●ZFDC-20-5	0.1-2000	19.5±0.5	±0.5	0.3	1	0.7	1.4	1.5	2.3	30	20	27	20	22	10	1.2	5	2	79.95	(1-4)
	■ZFDC-3375 NEW	0.2-200	30.5±0.5	±0.6	0.5	0.8	0.6	0.9	0.7	1.0	30	25	25	20	19	15	1.6	5	2	31.95	(4-24)
ZFDC-H case J17	◇ZFDC-20-1H NEW	30-400	20.5±0.5	±0.25	0.15	0.3	0.15	0.3	0.3	0.4	30	25	30	25	30	25	1.2	25	25	59.95	(1-4)
ZMDC case M21	ZMDC-10-1	0.5-500	11.5±0.5	±0.6	0.85	1.3	0.65	1.0	0.85	1.3	32	25	32	25	22	15	1.2	1.5	3	39.95	(4-24)
	ZMDC-10-2	250-1000	10.5±0.5	±0.5	1.1	1.4	—	—	1.6	1.9	40	30	30	20	20	15	1.5	—	5	47.95	(4-24)
	ZMDC-15-6	.01-35	15±0.5	±0.5	0.4	0.6	0.2	0.4	0.4	0.6	38	30	35	25	28	20	1.15	2	4	47.95	(4-24)
	†ZMDC-20-1	25-400	21±0.75	±0.5	0.2	0.25	0.3	0.35	0.35	0.5	25	20	35	25	25	20	1.25	3	5	47.95	(4-24)
	ZMDC-20-3	0.2-250	19.5±0.5	±0.5	0.35	0.5	0.25	0.5	0.35	0.6	36	30	33	25	25	20	1.2	1.5	4	39.95	(4-24)
	ZMDC-30-1	0.1-250	30±0.5	±0.5	0.4	0.6	0.5	0.8	0.55	0.85	23	18	20	15	17	10	1.5	1.0	3	39.95	(4-24)
ZDC case M22	ZDC-10-1	0.5-500	11.5±0.5	±0.6	0.85	1.3	0.65	1.0	0.85	1.3	32	25	32	25	22	15	1.2	1.5	3	29.95	(4-24)
	△ZDC-10-2	250-1000	10.5±0.5	±0.5	1.1	1.4	—	—	1.6	1.9	40	25	—	—	20	15	1.5	—	4	37.95	(4-24)
	ZDC-15-2 NEW	0.5-250	15±0.5	±0.5	0.8	1.2	0.7	1.0	0.9	1.2	32	28	32	28	32	28	1.4	1.5	3	37.95	(4-24)
	ZDC-15-6	.01-35	15±0.5	±0.5	0.3	0.6	0.2	0.4	0.3	0.6	38	30	35	25	28	20	1.15	2	4	37.95	(4-24)
	†ZDC-20-1	25-400	20±0.5	±0.5	0.2	0.25	0.3	0.35	0.35	0.5	25	20	35	25	25	20	1.25	3	5	37.95	(4-24)
	ZDC-20-3	0.2-250	19±0.5	±0.5	0.35	0.6	0.25	0.5	0.35	0.6	36	30	33	25	25	20	1.2	1.5	4	29.95	(4-24)
	■ZDC-10-1-75	1-250	10.5±0.5	±0.75	1.1	1.5	1.1	1.5	1.1	1.5	30	20	30	20	30	20	2	2	4	29.95	(4-24)
	■ZDC-15-6-75	.02-35	14.5±0.5	±0.6	0.3	0.6	0.2	0.4	0.4	0.6	35	30	35	25	28	20	1.5	2	4	38.95	(4-24)
	■ZDC-20-3-75	1-150	19.5±0.5	±0.75	0.35	0.8	0.35	0.8	0.35	0.8	25	20	25	20	25	15	2	2	4	30.95	(4-24)
	■ZDC-2375	50-100	10.5±0.3	0.2	—	—	—	—	1.1	1.3	—	—	—	—	35	30	1.3	—	4	38.95	(4-24)
	■ZDC-20-3-75-1	55-90	18.6±0.5	±0.3	0.4	0.6	0.4	0.6	0.4	0.6	35	30	35	30	35	30	1.2	—	4	38.95	(4-24)

L = low range (f_L to 10 f_L) M = mid range (10f_L to f_U/2) U = upper range (f_U/2 to f_U)

computer-automated performance data

typical production unit / for data of other models consult factory

PDC-10-1

FREQUENCY (MHz)	MAINLINE LOSS (dB)	COUPLING (dB)	DIRECTIVITY (dB)	VSWR IN	VSWR OUT	VSWR CPL
.50	.73	11.17	37.21	1.11	1.13	1.09
26.789	.62	11.50	36.92	1.10	1.13	1.06
53.078	.66	11.49	36.96	1.09	1.13	1.08
105.656	.72	11.52	36.48	1.06	1.14	1.09
158.234	.74	11.52	35.07	1.04	1.14	1.12
210.812	.81	11.60	32.60	1.02	1.15	1.12
263.39	.84	11.59	30.32	1.01	1.15	1.12
315.968	.92	11.56	27.36	1.01	1.15	1.13
368.546	.95	11.50	24.22	1.01	1.15	1.15
421.124	1.02	11.49	21.84	1.01	1.14	1.17
500.00	1.12	11.43	18.71	1.01	1.12	1.22

In Stock... Immediate Delivery