VLA Technical Report No. 68
FRONT END CONTROL INTERFACE
Module Type F14

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1.0 INTRODUCTION

This manual describes the VLA F14, Front End Control Interface module used to control and monitor three Single-Band, Front End Receivers on the VLA antennas. The emphasis of this manual is on the F14 theory of operation (Section 2) and maintenance (Section 3). Construction details are not included but all drawings used in F14 fabrication are listed in the BOM (Bill of Materials) drawing. Section 4 contains the drawings and Section 5 contains data sheets for the special-purpose components used in F14.

Features of the Single-Band, Front End Receivers that are relevant to the F14 functions are also described. These include receiver command and digital monitor data formats, analog signal levels and their normal range. The Appendix lists NRAO reports that describe the various Single-Band, Front End Receivers and related equipment.

Single-Band, Front End Receivers are used in both the VLA and VLBA projects and have been implemented in a number of frequency bands. A Single-Band, Front End Receiver is a complete, independent, modular assembly consisting of a dewar, RF amplifiers, refrigerator, vacuum and cryogenic plumbing, and interface circuitry. Since it is a modular design, differences between receivers are principally in the RF circuitry. This modularity provides greater commonality among receivers which reduces construction costs, eases installation and simplifies maintenance. In contrast to the older VLA front end receivers which share a common dewar, these newer receivers may be quickly removed from the antenna for maintenance or replacement without disturbing the other receivers. In removing a Single-Band, Front End Receiver, the receiver's vacuum is closed, the vacuum and cryogenic lines to the receiver are disconnected. (The cryogenic lines use self-sealing connectors.) Finally, the receiver AC power and interface cables are disconnected. After completing these simple operations, the receiver may then be unbolted and replaced by another unit.

F14 replaces the C1 Front End Control Interface module which was previously used to control and monitor one (X-band) Single-Band, Front End Receiver. The F14 is installed in F-Rack Slot 4, Bin N - a location previously assigned to the C1 module. The F-Rack F14 currently controls the X-band receivers, some L-band Single-Band, Front End Receivers and could control a third receiver. (L-band versions of the Single-Band, Front End Receivers are replacing the older A-Rack L-band receivers.) F5, the A-Rack receiver interface, currently controls the receivers in the A-Rack Dewar: C-band, older L-band, K-band and Ku-band receivers.

If more than three Single-Band, Front End Receivers are installed, a second F14 will be added to the F-Rack. In any case, the existing F5 Front End Interface will still be used to control other A-Rack functions. The 75 and 327 MHz receivers are not (and will not be) controlled by F14.

On the F-Rack F14, P2 and P3 connect to the 3.5cm (X-band) receiver, P4 and P5 connect to the 20cm (L-band), and P6 and P7 will connect to a future 0.7cm (Q-band) or 13cm (K-band) receiver.

F14 Physical Description

At this point, the reader should refer to drawing D13190P10 (in Section 4) which depicts the F14 Assembly. The F14 is a 4-wide VLA module with one rear-panel 50-pin AMP pin connector (P1) that mates with the 50-socket AMP bin connector. DC power, Critical Power (described below) monitor and control signals (from M1) and the 9.6 Hz (from L8) switching signal are routed through this connector. Three pairs of DB25 connectors (P2-P3, P4-P5 and P6-P7) on the module back panel contain the three sets of receiver interface signals. (P2, P4 and P6 are socket connectors; P3, P5 and P7 are pin connectors.) Three pairs of shielded, 25-conductor cables connect these signals to corresponding DB25

connectors on the three front ends. Since the cables are connected to the module back panel, a mechanical interlock may be installed on the bin back panel to mechanically lock the F14 in place until the interface cables are disconnected. This feature inhibits removal of the F14 if any DB25 cable connector is still connected. An obvious and very important concern is that, since the DB25 connectors are not keyed, **care should be taken to properly connect the three pairs of interface cables when performing maintenance on the receivers or F14. If they are cross- or mis-connected, the receiver's control and monitor states will be confused and the problem will not be obvious in the monitor data.**

The F14 front panel has three sets of LED displays, one set for each receiver. The displays are vertically aligned on the panel and are for receivers A, B and C (left to right respectively). The **Serial Number** display consists of three four-digit alpha-numeric LED's that show the three associated receiver (decimal) serial numbers. The **Band** display consists of three, four-digit alpha-numeric LED's that show the receiver frequency bands (in cm). Discrete LED's for each receiver show: **Red** - Pump Request (powered by Critical Power); **Green** - drive to "Normal" cals is active; **Yellow** - drive to "Solar" cals is active.

The **Serial Number** and **Band** alpha-numeric displays are developed from a ten-bit plus parity hard-wired code from the receiver via the interface cables. The display logic converts the encoded values to ASCII code for the displays.

The receiver **Serial Number** is unique to each receiver and ranges from 1 through 63. The receiver serial number is a six-bit, straight binary code. The two leading Serial Number display characters are blanked.

The **Band** displays show the receiver operating wave length in centimeters. The Band data is coded in a four-bit straight binary code and has an **even** parity bit (Band codes are shown in Section 2). The leading Band display character is blanked if only three digits are used. (The decimal point is a digit.) In the event of a Band Code parity error or an unassigned Band Code state, the display logic causes the word **BAD** to be displayed (the leading digit is blanked).

All F14 circuitry is contained on five wire-wrap connector boards. These boards, front panel and rear panel are wire-wrapped in one wiring machine set-up. Sheet 3 of the Assembly Drawing shows the board layout and IC location designators. Note that connector board "E" is located in the front of the module and board "A" is located at the back of the module. These board location designators are a component of the chip location designator. Thus for boards A through D, a typical location designator might be B20, designating IC location 20 on board B. Pin 3 on this chip is designated B20-3. An important designation convention should be mentioned here: Since all IC locations on these five logic connector boards are for 16-pin chips, when a 14-pin chip is used, pins 1 and 14 are inserted into sockets 1 and 16. Thus IC pins 8 through 14 are physically located in sockets 10 through 16. **On the schematic diagrams, these (i.e. IC pins 8 through 14) pins are designated in the 16-pin connector board format.** Thus pin B09-12 on chip B09 (a 7406) is really pin 10 of the IC. Although this may seem unusual, it is an easy convention and should not lead to confusion as the IC socket numbers (1 through 16) are printed on the connector boards. The F14 circuit schematic drawing (D13190S4) uses these designators to identify the physical location of the chips.

The logic connector board IC pin designation convention for board "E" is shown on Assembly Drawing Sheet 4. This board is a "universal" board which accommodates chips having more than 16 pins or transverse pin spacings that are multiples of 0.300 inch. This board has nine columns (A through J) of sockets numbered 1 through 50. The chip location designators are derived from the column-row location of pin 1 of the chip. Thus, the 24 pin chip EG19 has chip pin 1 inserted into the socket at column location G, row 19. All schematic diagram IC pin numbers for this board refer to the chip pin number, not the column-row socket locations; thus pin EG19-20 designates pin 20 on chip EG19. Sheet

6 of the IC Location Diagram, A13190P11, shows the locations of these board E chips in terms of the column-row socket designators.

Sheet 4 of the assembly drawing shows the front panel display PC board IC locations and wire-wrap pin locations and designators.

Although it is not a maintenance concern, the IC location designators described above are those used in wiring the module; the Master, Machine and Hand wire lists all use these designators.

The F14 and C1 50 pin AMP connector pin-outs are different so it is necessary to rewire the bin when replacing C1 with an F14.

Receiver Description

For a better perspective of F14 functions, a very brief functional description of the Single-Band, Front End Receiver follows. The emphasis is on the control and data aspects; RF properties are treated lightly. Readers are referred to the NRAO technical reports listed in the Appendix for detailed descriptions of the receivers and related equipment.

A waveguide polarizer on the receiver input separates the left and right circular polarized (LCP and RCP) signals for amplification by two, cooled amplifiers. Normal and Solar calibration signals are coupled into the receiver inputs via a power splitter and directional couplers. After passing through the dewar walls, the signals are filtered by band-pass filters and are further amplified by room temperature post-amplifiers. The two signals are then output to the mixers-IF system. An LED in the cooled amplifiers stabilizes HEMT sensitivity. The Normal and Solar noise source power level varies as a function of receiver frequency band; the noise drive voltage is the same for all receivers but the source current differs between bands. At 20cm and 3.6cm (L and X bands), an amplifier is required to achieve the required noise level. The amplifier is switched by the Solar cal drive.

The receiver is enclosed in an evacuated dewar which is cooled by a closed-cycle, Helium-cooled refrigerator. The dewar is connected to a vacuum manifold through an electrically operated vacuum valve and quick-disconnect coupling. The refrigerator is connected to Helium supply and return manifolds via Arequipt couplings and operates continuously (in the COOL state) but the vacuum pump operates only when commanded by a receiver. When the vacuum pump is not operating, the vacuum manifold is vented to atmospheric pressure; this helps to seat the receiver's vacuum valve. The Helium supply supply pressure should be 270 +/- 10 psi. The Helium return pressure should be 60 +/-15 psi.

Dewar vacuum, refrigeration and heating control is performed by control logic in the receiver (described below); control bits X, C and H define the receiver control states as shown on the next page.[1]

Receiver Control State Table

Control bit	X	C	H	
Cryo off	1	0	1	No refrigerator power, heater power, or vacuum pumping.
Cool	1	1	1	Normal cooled operation.
Stress	1	0	0	COOL with small added heat to stress-test cryogenics.
Heat	0	1	0	Fast warm-up of dewar, 65 Watts of heater power.
Pump	0	1	0	No refrigerator or heater power.

[1]The receiver manuals designate X and M (described below) as $\overline{X}$ and $\overline{M}$. The F14 logic drawing uses the notation X and M for these terms; the drawing convention is used in this manual for consistency.

The reason for the all-1's COOL code, is that in the event of an "X, C and H stuck high" failure of the receiver controller or the receiver J5 cable is disconnected, the control logic defaults to the COOL state, the desired default condition for a receiver. The STRESS command causes a small amount of heat to be generated in the Dewar; the response of the refrigerator to this additional load may be seen in the 15 and 50 degree stage temperatures. The HEAT command is a maintenance feature which causes the Dewar to be heated; this permits the dewar to be warming up while receiver maintenance personnel are on the way to the Antenna. The PUMP command causes the vacuum valve and vacuum pump to be turned on. These states are controlled by receiver control logic described below.

Dewar vacuum and temperature transducers are conditioned by a control and monitor electronics card cage attached to the dewar. A mode control switch on the card cage enables the receiver vacuum, refrigeration and heater circuitry to be manually set to any of six states: CPU, OFF, COOL, STRESS, HEAT, and PUMP. The CPU position permits central control of these functions via F14 and the Monitor and Control System. In the CPU position, the X, C and H control bits from F14 set the control states to OFF, COOL, STRESS, HEAT or PUMP. When the mode switch is set to any position other than CPU, these functions are determined by X, C and H control bits from the control logic as a function of the local control switch position.[2]

Control logic in the card cage controls the operation of the vacuum pump request, vacuum valve, refrigerator, and heater. The control logic inputs are the mode control switch X, C and H bits; the F14 X, C and H control bits; dewar and port (manifold) vacuum; dewar (15 deg stage) temperature and AC current load. Control outputs are the discretes: vacuum valve solenoid drive (S), pump request (P), refrigerator motor power, dewar heater power, and the mode control switch state (M). The operations performed by the control logic are described in the next paragraph.

The vacuum valve (S) operation is inhibited if the pump port (i.e., manifold) vacuum is above 50 microns. The vacuum valve is opened if the pump port vacuum is less than the dewar vacuum and the dewar vacuum is greater than 7 microns. The pump request (P) signal becomes true (i.e., a "1") if dewar vacuum exceeds 5 microns and goes false ("0") if the dewar vacuum becomes less than 3 microns. The refrigerator operation is inhibited if the dewar vacuum is above 50 microns. The control logic is designed to continue the refrigerator operation in the event that the J5 cable (power, control bits and ID code) from F14 is disconnected. This permits maintenance of the system electronics but does not affect the cryogenics operation. The control logic turns on the heater when the mode switch is set to HEAT or when the central computer commands the HEAT state. The control logic also protects the dewar from overheating by the heater when in the HEAT state.

Monitor circuitry in the card cage reads out the three current control bits (X, C and H from either F14 or the mode control switch, depending upon the switch position) and control output discretes (P, S and M). The monitor circuitry also reads out the following analog values: vacuum (dewar and pump port); linear temperature measurements (15, 50 and 300 degree stages); a non-linear temperature measurement (SENS, on the 15 degree stage); AC current load (total); HEMT and FET gate bias levels, and the LED voltage. With the exception of SENS, these parameters are output to F14 analog multiplexers via monitor connector J2. The normal values and working range are tabulated in Section 2.1.

A 12-position manual selector switch and integral DMM on the card cage permits the analog parameters to be monitored locally.

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[2]In normal operation, this switch is left in the manual COOL position. The F14 X, C and H control bits are ignored by the control logic.

The receivers read out digital values that indicate the receiver serial number, the frequency band and the modification level. These codes are hard-wired in the receiver when it is manufactured and are output to the F14 on the Power-Control-ID connector J2. These codes are described in Section 2.1.

Two DB25 connectors on the receiver provide the +/- 15V Critical Power and the F14 control and monitor connections. Two shielded, 25 conductor cables connect a receiver to F14. J5 (25 pin contacts) carries Critical Power, the central control computer X, C and H control bits, the band ID bits, the receiver serial number ID bits and receiver modification level ID bits. J2 (25 socket contacts) carries analog and discrete monitor signals.

A Critical Power Panel (CPP) in the F-Rack provides power and system support for six Single-Band, Front End Receivers. Two F14's are required for six receivers (the use of two F14's in the F-Rack is discussed below). The CPP has +15V and -15V Critical Power supplies; this power is routed to the receivers via F14 connectors P3, P5 and P7. If these connectors are disconnected from F14 or F14 is removed from the bin, Critical Power is not available to the receivers. The CPP also provides two-phase, 150 volts AC power for the refrigerators. The unshifted phase of this 150 volt AC also powers the vacuum valves and dewar heaters. This 150 volts AC power is provided by an isolation transformer and phase shift networks. The receiver manuals show this AC circuitry in a P112 power supply but in the VLA application, the CPP contains this AC circuitry. The CPP also differs from the VLBA application in that the receiver AC current monitor circuitry is not used. The CPP also monitors the vacuum pump 110 volt AC current; this current monitor is connected to the Common Analog inputs of both F14's.

In addition to the two DB25 connectors mentioned above, the Single-Band, Front End Receiver has an "AUX" DE9 (9 socket contacts) J4 connector, which carries the Pump Request (P) and the AC current analog monitor signal and their returns. A 9-conductor, shielded cable connects this DE9 connector to corresponding connectors on a small, 3-receiver "Auxiliary" chassis mounted on the back of the F-Rack in bin N locations 11 and 12. In the VLA application, the receiver's AC current monitor signals are not routed through the Auxiliary chassis to F14. Pump requests (P) from the Front-Ends are OR-ed together in the Auxiliary chassis to activate the vacuum pump via the CPP. The Auxiliary Chassis logic is powered by +5V derived from +15V Critical Power from the receivers via the receiver's J4 (AUX) connector. **When the F14 is removed from the bin or the F14 J3, J5 and J7 cables are disconnected, the Auxiliary chassis logic power is removed. In this state the Pump Request (P) is disabled and the Vacuum Pump cannot be activated.**

The Single-Band, Front End Receivers do not have an internal transfer capability in which the LCP and RCP signals can be interchanged for test purposes. As implemented at the VLA, the transfer command interchanges the signals in F6, down-stream from the receiver outputs so this capability is still useable.

Figure 1 (next page) depicts the interconnect cabling between three Single-Band, Front End Receivers, F14, CPP, the Aux Chassis and Data Set. In the six-receiver configuration, a second F14 (not pictured in Figure 1) would be added with connections for 9.6 Hz, Data Set command and monitor messages and analog monitor data. The Appendix (Section 6) lists the F14 connector pins and signals.

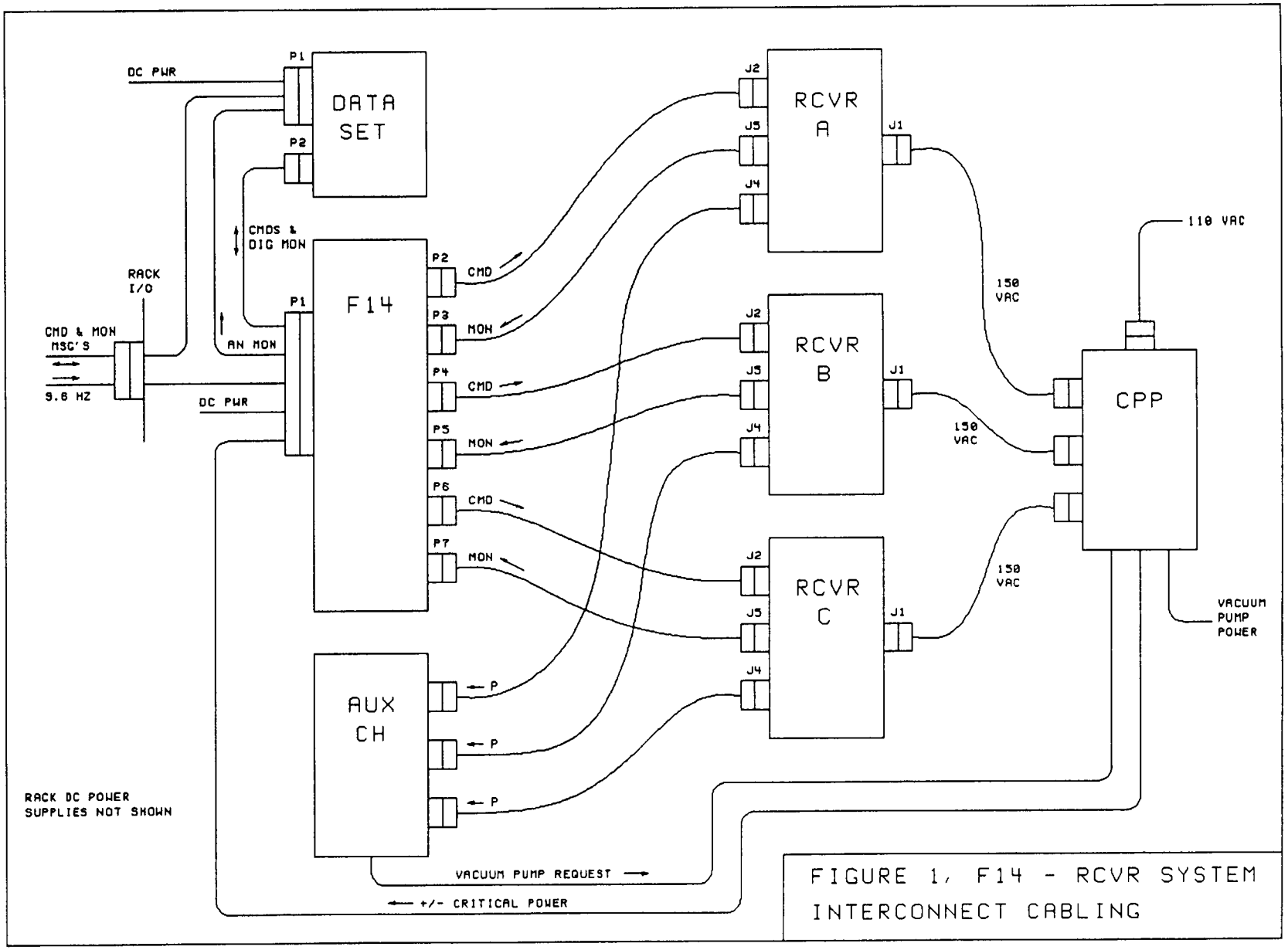

FIGURE 1, F14 - RCVR SYSTEM INTERCONNECT CABLING

2.0 THEORY OF OPERATION

In this section, we first consider the F14 Command and Monitor functions. This is followed by a description of the circuits that implement these functions.

2.1 RECEIVER CONTROL AND MONITOR REQUIREMENTS

Command Functions

The Single-Band, Front End Receivers have a small set of command functions. These fall into two categories: **Observing Commands** and **Diagnostic Commands.** **Observing Commands** (MUX address 322_8) are those invoked for Astronomical purposes and are a set of commands to control the receiver calibration circuitry (i.e., to turn on or off a continuous or switching drive to two noise source diodes). **Diagnostic Commands** (MUX address 323_8) are used to control or test the receiver cryogenic and vacuum functions. The specific command arguments and multiplex address for these commands are tabulated below. The digital command multiplex address is a unique address that enables the two types of commands to be loaded into two static command storage registers.

An unusual (for the VLA) feature is the format and usage of the two command arguments. Although the F14 receiver drive circuitry is capable of driving only three receivers, the receivers actually require only a small number of command states for both types of commands - only three bits are required to encode all receiver command states but four bits are used. The unused command bit is designated U (for unused) in the tables below. Therefore it was decided to structure the F14 command format so that for each type of command (i.e., Observing and Diagnostic), the command format conveys commands for six receivers, even though this would appear to be a useless feature. The reason for this unusual provision is the potential future use of two F14's in the F-Rack. In this application, two F14's would control six receivers and both F14's would store the same commands. The first set of receiver commands are designated A, B and C, and the second set of receiver commands are designated A', B' and C'. A back-panel wire jumper (to F14 digital selector logic) determines which set of three receiver commands are connected to the receiver drive circuits. Thus F14 #1 would use the A, B and C commands and F14 #2 would use the A', B' and C' commands. In the F-Rack, the jumper is set to select F14 #1's A, B and C commands. If a second F14 is added, this jumper will not be installed.

Designating the six F-Rack receivers A through C (F14 #1), A' through C' (F14 #2), the 24-bit command arguments are assigned to six four-bit command functions as shown below. **Note that the format shows the control bits as they appear in the F14 command registers.**

Command Format

F14	#1	#2	#1	#2	#1	#2
Rcvr	A	A'	B	B'	C	C'
Bit	0 1 2 3	4 5 6 7	8 9 10 11	12 13 14 15	16 17 18 19	20 21 22 23
	C C C U	C C C U	C C C U	C C C U	C C C U	C C C U

C = Active command bit. U = Unused command bit. Bit 0 = Least significant bit.

For each receiver, the two sets of calibration command states are designated **Observing Commands** and are as shown below. **Remember that the formats show the command bits as they appear in the command registers.**

Observing Command Format, MUX 322_8

Rcvr	A	A'	B	B'	C	C'
Bit	0 1 2 3	4 5 6 7	8 9 10 11	12 13 14 15	16 17 18 19	20 21 22 23
	S N A U	S N A U	S N A U	S N A U	S N A U	S N A U

S = Solar command bit, N = Normal command bit, A = Auto command bit, U = Unused command bit.

F14 logic maps these **Observing Command** bits into a state table as follows:

Condition	MSB			LSB		
F14 Reg bit label	U	A	N	S	Hex	Cal State
Cals off	0	0	0	0	0	No drive to either noise source
Solar continuous	0	0	0	1	1	Solar (only) continuous noise source drive
Normal continuous	0	0	1	0	2	Norm (only) continuous noise source drive
Both continuous	0	0	1	1	3	Both noise sources on continuously
** Solar auto	0	1	0	1	5	9.6 Hz drive to Solar (only) noise source
* Norm auto	0	1	1	0	6	9.6 Hz drive to Norm (only) noise source
Both auto	0	1	1	1	7	9.6 Hz drive to both noise sources

** is the usual Solar observing condition. * is the usual Normal observing condition. U can be either 0 or 1, shown as a 0 for the table hex code.

In the this table, there are "Normal" and "Solar" calibration states. These control the drive to the two noise source diodes. Since the signal level of solar flux is much higher than that of typical astronomical sources, the solar cal noise signal is a higher level than the normal level. Secondly, a continuous cal command state causes a constant (i.e., non-switching) drive to the noise source diode. The auto states cause the 9.6 Hz signal from L8 to drive the noise diodes when it is a logic 1 or high.

F14 provides the central computer control discretes X, C and H to the receiver control logic that controls the vacuum, refrigerator and heater control circuits (see the Receiver Description above). These commands are designated **Diagnostic Commands** and the state table is as shown below.

Diagnostic Command Format, MUX 323_8

Rcvr	A	A'	B	B'	C	C'
Bit	0 1 2 3	4 5 6 7	8 9 10 11	12 13 14 15	16 17 18 19	20 21 22 23
	H C X U	H C X U	H C X U	H C X U	H C X U	H C X U

The receiver's control logic maps these **Diagnostic Command** bits into a state table as follows:

F14 Reg bit label	U	X	C	H	Hex	Receiver Control State
Cryo off	0	0	1	0	2	No refr. or heater power, no vacuum pumping
* Cool	0	0	0	0	0	Normal cooled operation
Stress	0	0	1	1	3	COOL with small added heat to test cryo
Heat	0	0	0	1	1	Fast warm-up of dewar, 65 W of heat
Pump	0	1	0	1	5	No refr. or heater power.

* Usual or normal observing condition. U = can be either 0 or 1, shown as a 0 for the table hex code.

An important point needs to be emphasized here: these control bits are the complement of those required by the receiver control logic (see the Receiver Description above). The F14 inverts these command message bits to attain the states required by the receiver control logic. Note that in the table above, the COOL command states are all 0's. The reason for this inversion is, that in the event of a momentary power drop-out, the Diagnostic Command storage register will be be cleared (to 0's) by the power clear logic. This state is also set when the F14 is powered on. This state defaults the receiver control logic to the COOL state, the desired condition for a receiver in the event of control ambiguities such as disconnected cables, etc. The receiver control logic operations are described in Section 1.0.

The states of the F14 command registers are read back as command echo monitor data; the formats are identical to the command formats. This command echo verifies that the commands were loaded into the F14 command registers and permits comparison of the F14 command register states with the command states generated by the central control computers.

A Critical +5 volt power, derived from the CPP Critical +15V, is used to power the three F14 front panel Pump Request Mon LED's. The LED's are driven by the Pump Request Monitor bit P, in the digital monitor data registers.

Since maintenance personnel may need to locally control the F14 for test purposes, Section 2.6 describes the Command Simulator (M5) switch settings to command the receiver control logic.

Monitor Functions

The monitor data read from F14 is indicative of the performance of the receivers, F14, and the Helium-Vacuum systems. Monitor data is divided into two classes, analog and digital, according to the character of the data sources. For example, the frequency band, receiver serial number and mod level are digital values because they are hard-wired digital codes in the receiver, but Helium supply and return manifold pressures and dewar and pump port vacuum are derived from continuous output analog pressure sensors. The analog monitor data is, of course, converted to digital values in the Data Set but has a format which differs from the digital data.

Digital Monitor Data

There are two types of digital monitor data. The first type, Observing and Diagnostic Command Echos, are formatted as an exact replica of the two types of commands. The second type, the digital monitor points, are a composite of several sets of digital data as described below. Remembering that one F14 is currently used in the F-Rack and that a second one may be added, the octal mux addresses of the digital data are as shown below. For convenience, the command echo addresses are 100_8 lower than the command addresses.

F14 Usage	F-Rack #1	F-Rack #2
Obs'vg Cmd Echo	222	232
Diag Cmd Echo	223	233
Dig Mon Data, Rcvr A	224	A' 234
" " " , Rcvr B	225	B' 235
" " " , Rcvr C	226	C' 236

The F-Rack Digital Monitor Data are input to the Data Set on the DIGI-1 port (address range 220_8 - 237_8). The Digital Monitor Data is shown in **Register Format** on the next page.

Receiver Digital Monitor Data Format

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
Funct	H	C	X	M	P	S	M_0	M_1	S_0	S_1	S_2	S_3	S_4	S_5	0	0	B_0	B_1	B_2	B_3	P_B	0	0	0

Consider monitor data bits 8 through 23 as four Hex digits in **Numeric Format** (as they would appear on a Data Tap's binary bit display or a CRT screen, the reverse of the **Register Format** shown above).

The receiver's frequency band code is two Hex digits (B_0 through B_3). The top digit is always a 0 or 1 and contains an **even** parity bit P_B, for the four bits of frequency band code. The wavelength, frequency, frequency band encoding **(numeric format)** and associated display digits are shown below.

Receiver Frequency Band Code and Band Display

Wav'lth cm	Frequency	Band	Parity, P_B	Code$_{16}$ B_0-B_3	Mon Readback$_{16}$ P_B, B_0-B_3	Band Display, Centimeters
400	75 MHz	P	0	0	00 XXXX	400.
50/90	600/327 MHz	P	1	1	11 XXXX	^50.0
20	1.4 GHz	L	1	2	12 XXXX	^20.0
13	2.3 GHz*	S	0	3	03 XXXX	^13.0
6	4.8 GHz	C	1	4	14 XXXX	^6.0
4	8.4 GHz	X	0	5	05 XXXX	^3.6
2.8	10.7 GHz*	X	0	6	06 XXXX	^2.8
2	15 GHz	U	1	7	17 XXXX	^2.0
1.3	23 GHz	K	1	8	18 XXXX	^1.3
0.7	43 GHz	Q	0	9	09 XXXX	^0.7
0.35	86 GHz *	W	0	A	0A XXXX	0.35
(not assigned)			1	B	1B XXXX	^BAD
(not assigned)			0	C	0C XXXX	^BAD
(not assigned)			1	D	1D XXXX	^BAD
(not assigned)			1	E	1E XXXX	^BAD
(not assigned)			0	F	0F XXXX	^BAD

Notes: * Denotes receiver bands are not installed on the VLA but included in the F14 frequency band code display logic for potential future use. XXXX are the lower four hex digits of the digital monitor data. ^ denotes a blanked display digit. The period (.) character is one display digit.

The middle two Hex digits are the receiver serial number code, S_0 through S_5. For example, a readback of XX 13 XX (**Numeric Format**) indicates receiver serial number 19_{10}.

Bits 6 and 7 are M_0 and M_1 which indicate the receiver's modification level, 00 for the initial design.

X, C, H, M, P and S are control logic monitor bits which indicate the state of the receiver's control logic. S, P and M are discretes which indicate the following:

M = Manual State, 1 = CPU, (i.e., central computers), 0 = manual control switch off CPU position.
P = Pump request, 0 = request vacuum pump, 1 = don't pump.
S = Vacuum valve monitor, 0 = closed, 1 = open.

X, C and H are the current Receiver Control Bits (see the Receiver Description above) from the receiver control logic. Remember that these are **complement** of the Diagnostic Register state table shown above. In **Numeric Format** the states are shown on the next page.

Monitor Data Receiver Control Bits

State	X	C	H	$Code_{16}$
Cryo Off	1	0	1	5
Cool	1	1	1	7
Stress	1	0	0	4
Heat	1	1	0	6
Pump	0	1	0	2

Analog Monitor Data

Analog monitor data falls into two classes: **Common Analog Functions** and **Receiver-Specific.**

Most of the **Common Analog** Functions are power supply voltages but Helium supply and return pressures and Vacuum pump current are also measured.[3] These functions are classed as Common because they are not particular to a receiver. The table below shows these Common Analog functions.

An internal (to the F14) pair of accurate + 10 and - 10 volt references are included in the Common Analog Monitor functions to provide a means of checking the Data Set A/D gain drift. The Analog Ground parameter provides a means of checking the Data Set A/D zero drift. The Common Analog Functions are tabulated below.

Common Analog Functions

Function	Mux $addr_8$	1V =	Normal Value	Data Range
Analog gnd	140	1V	0.000	-0.020 to +0.020
+10V ref	141	1V	+10.000	+9.980 to +10.020
-10V ref	142	1V	-10.000	-10.020 to -9.980
Gnd (spare)	143	1V	0.000	-0.020 to +0.020
+15V/2	144	2V	+7.500	+7.480 to +7.520
-15V/2	145	2V	-7.500	-7.520 to -7.480
+5V	146	1V	+5.000	+4.980 to +5.020
+28V/4	147	4V	+7.000	+6.985 to +7.015
+15V/2 (Crit)	150	2V	+7.500	+7.480 to +7.520
-15V/2 (Crit)	151	2V	-7.500	-7.520 to -7.480
Vac pump curr	152	1A	0.000*	*
He sup pres	153	100psi	2.700	+2.400 to +3.000
He ret pres	154	100psi	0.750	+0.500 to +1.000
Gnd (spare)	155	1V	0.000	-0.020 to +0.020
Gnd (spare)	156	1V	0.000	-0.020 to +0.020
Gnd (spare)	157	1V	0.000	-0.020 to +0.020

* Vacuum Pump quiescent, pump-on Normal value and Working Range not yet established.

The spare channels are connected to analog common but could be assigned to some future F14 function but would require a modification of F14 wiring. There is one spare (unassigned) pin on P1 which could be connected to one of these spare channels.

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[3]The Single-Band, Front End Receivers have a dedicated Helium compressor with its supply and return manifolds. These service several receivers. Supply and return pressures are measured on the manifolds by a single set of pressure transducers; the pressure signals and returns are connected to the F14 Common Analog multiplexers. The A Rack monitors the first (older) Helium supply and return pressures.

The **Receiver-Specific** functions are those particular to a receiver and will typically have different values for each receiver. These are tabulated below.

Receiver-Specific Functions

Function	Rcvr A Mux_8	Rcvr B Mux_8	Rcvr C Mux_8	1V =	Normal Value	Data Range
Pump Vac	060	100	120	****	+10.000	+9.950 to +10.100
Dewar Vac	061	101	121	****	0.000	-0.200 to +0.200
15 Deg Sta	062	102	122	100K	+0.150	+0.100 to 0.200
50 Deg Sta	063	103	123	100K	+0.550	+0.400 to +0.700
300 Deg Sta	064	104	124	100K	+2.900	+2.000 to +3.000
* Norm Cal V/4	065	105	125	4V	+7.000	+6.900 to +7.100
AB Stage 1 **	066	106	126	1V	-0.600	-1.000 to +1.000
AB Stage 2ff ***	067	107	127	1V	-0.600	-1.000 to +1.000
CD Stage 1 **	070	110	130	1V	-0.600	-1.000 to +1.000
CD Stage 2ff ***	071	111	131	1V	-0.600	-1.000 to +1.000
LED Voltage	072	112	132	1V	+7.000	+5.000 to +8.000
* Solar Cal V/4	073	113	133	4V	+7.000	+6.900 to +7.100
Gnd (spare)	074	114	134	1V	1.000	-0.020 to +0.020
Gnd (spare)	075	115	135	1V	0.000	-0.020 to +0.020
* Norm Cal Curr	076	116	136	10mA	*****	*****
* Solar Cal Curr	077	117	137	10mA	*****	*****

* These functions are sampled while the cal is on and held for asynchronous readback as in C1.
** AB and CD Stage 1 signals are the gate voltages of the cooled amplifier first stages.
*** AB and CD Stage 2 signals are the summed gate voltages of sucessive stages of the cooled amplifiers. These four gate voltages should not vary from the value observed when the receiver is installed.
**** Non-linear scale, see the Appendix (Section 6) which has a vacuum vs monitor output voltage curve.
***** The Normal and Solar cal currents are different for each receiver band.
The SENS temperature measurement is not read out to F14.

There are five unassigned lines on the receiver J2 connector and four unassigned lines on the receiver J5 cable. These lines could be assigned to the spare channels but would require F14 and receiver wiring modifications to connect these J2 and J5 pins to the multiplexers.

The addresses shown in the tables above are those presently assigned to F-Rack, F14 #1. The Data Set is capable of multiplexing 128 channels of analog data from eight 16-channel sources. F12 is also installed in the F-Rack and provides 16 channels of analog monitor data to one Data Set analog input. In the event that a second F14 is added to the F-Rack, three additional sets of Data Set multiplex addresses would be required for the three new Receiver-Specific analog functions. The F14 #2 Common Analog functions need not be used since they are redundant with F14 #1. In this dual-F14 configuration, the six Receiver-Specific, Common Analog and F12 analog data will use all the analog multiplexing capacity of the Data Set. The addresses assignments shown above might be changed for this configuraton.

2.2 DATA SET INTERFACE

All F14 command-monitor data operations are a response to command or monitor data message stimulus from the Data Set. This section describes these interface signals and their usage in the F14.

Multiplex Address

The Multiplex Address is four, low-true, TTL logic signals having binary weights of 2^0 through 2^3. These permit decoding up to sixteen unitary enables (five monitor and two command enables are decoded in the F14). These four bits are the lower portion of the eight-bit address component of Data Set command and data messages. The Data Set decodes the upper four bits to select a Data Set digital output or input to/from a device controlled by the Data Set. In the case of analog inputs to the Data Set, the upper four bits enable one of eight Data Set analog input multiplexer channels. Between command or data operations, the Multiplex Address lines are quiescent and a logic high ("0" state).

For example, for the Observing Command, Mux 322_8 F14 decodes the lower four bits (0010) to generate CMD EN2 (a command enable) that permits the F14 Observing Command Register to be serially loaded by the Data Set. The Data Set decodes the upper four bits (1101) to activate the DIGO-0 output.

An analagous digital data example is the Observing Command Echo Mux 222_8. F14 decodes the lower four bits (0010) to generate EN2 (a monitor enable) that permits the F14 Observing Command Echo Register to be serially read out to the Data Set. The Data Set decodes the upper four bits (1001) to active the DIGI-1 input.

In the case of analog signals multiplexed by the F14, two eight-channel analog multiplexers select one analog signal from a group of sixteen analog signals for output to the Data Set. One multiplexer selects one of the lower eight signals and the second selects one of the upper eight signals. The multiplexers have internal one-of-eight decoders which drive the analog switches. The decoder has an enable input which permits the decoder outputs to drive the analog switches. Thus the three lower Multiplex Address bits (2^0, 2^1 and 2^2) activate (via the one-of-eight decoder) one of the channels on each multiplexer and the most significant bit, 2^3, enables the lower or upper multiplexer decoder. The two multiplexer outputs are tied together and drive the Data Set Analog multiplexer.

Digital Command Output DIGI-0

The Data Set digital command output used by F14 is DIGO-0, which consists of three low-true lines: DIGO-0, CLKO-0 and STRO-0. The DIGO-0 signal is a serial data line, clocked into an F14 serial input command register by CLKO-0. After 24 shift clocks, the data is parallel-loaded into a static storage register by the STRO-0 signal. In the interval between command messages directed to DIGO-0, the Data Sets sets the DIGO-0 lines high. Figure 2 (Section 2.3) depicts the DIGO-0 timing. DIGO-0 address are 320_8 - 337_8.

Digital Monitor Input DIGI-1

The Data Set digital monitor data input used by F14 is DIGI-1, which consists of three low-true lines: DIGI-1, CLKI-1 and STRI-1. The STRI-1 signal parallel-loads an F14 monitor register. The DIGI-1 signal is a serial data line, the output of a serial monitor register. The DIGI-1 line is clocked into the Data Set monitor input register by CLKI. In the interval between monitor messages evoked from DIGI-1, the Data Set sets the DIGI-1 lines high. Figure 3 (Section 2.3) depicts the DIGI-1 timing. DIGI-1 addresses are 220_8 - 237_8.

Analog Monitor Inputs ALGI-3 to ALGI-6

The Data Set analog monitor data inputs presently used by F14 #1 are ALGI-3 through ALGI-6 and the associated addresses range from 60_8 through 157_8. These accept four differential analog signals from 16-channel analog multiplexers in the F14. In the event that a second F14 is added to the F-Rack, these assignments could change.

The Data Set differential inputs have a common-mode rejection ratio > 80 db. Input impedance is greater than 10^{10} ohms. Settling time to less than one bit error is less than 18 microseconds but the Data Set provides 30 microseconds of settling time; 30 microseconds after the start of an analog to digital conversion sequence, the Analog to Digital converter sample/hold is set to the hold mode and the conversion sequence is started.

2.3 DIGITAL LOGIC OPERATION

Command and Monitor Data Enable Decode Logic (Sheet 3)

The four (low-true) Mux address bits (SMA0- through SMA3-) are inverted to high-true format by open-collector buffer B09. The buffer output levels swing between 0 and 5 volts. A 7406 buffer and pull-up resistors are used in place of a simple inverter in the event that it becomes necessary to use analog multiplexer chips with overvoltage protection (typically an HI 508A). These multiplexers require a logic 1 greater than 4.0 volts.

The Command and Digital Monitor enables are decoded by different 1-of-eight decoders. This is the result of the requirement for the use of a six-argument command for two F14's in the F-Rack. For simplicity, all digital monitor data is input to the Data Set on port DIGI-1. In this case, the second F14 digital monitor data addresses are translated 10 (octal) addresses higher but the command addresses are not because all six command arguments are packed into a single command argument. This usage is described in Section 2.1 above.

The Command Address Enable decoder B17, a 74LS138, is enabled by the low-true SMA3-, high for multiplex addresses 00_8 through 07_8. (See a TTL data book for details on the operation of the 74LS138.) The low-true CMD EN2 and CMD EN3 outputs are decodes of mux codes 02_8 and 03_8 respectively. These two enables permit the CLKO-0 clock to load the DIGO-0 data into the two command registers as described below.

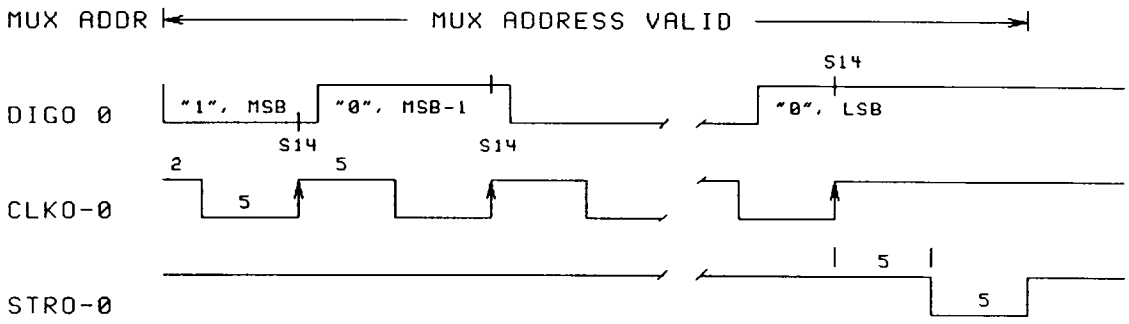
The Digital Monitor Address Enable Encoder B04, a 74LS138, performs an identical decode but the G2A input is driven by an 74LS86, an exclusive-or with high-true SMA3 and Slot B/A- as inputs. The Slot B/A- term is a hard-wired term in the bin wiring. When Slot B/A- is tied low via a bin jumper between J1-N and J1-L, the low-true exclusive-or output enables B04's G2A for mux addresses 00_8 through 07_8. The high-true exclusive-or output disables the decoder for mux addresses 10_8 through 17_8. The jumpered-to-ground configuration is used to detect digital monitor addresses 222_8 through 226_8, the F-Rack F14 #1 addresses. The floating B/A- configuration is used to detect digital monitor addresses 232_8 through 236_8, the F-Rack F14 #2 addresses.

The Slot B/A- term is also used to control the selection of command arguments in the Command Register Multiplexer described below.

Command Register Logic (Sheet 1)

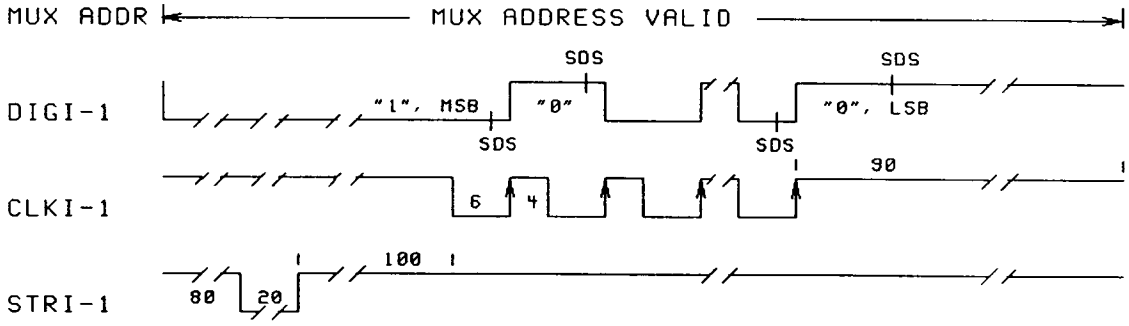
Two identical (except for the unitary enables described above) command registers are loaded by the DIGO-0 command output. Consider the Observing Command register logic on the upper left of Sheet 1. The command register logic consists of three serial-in-parallel-out shift registers and four parallel-input storage registers. Three sets of gates, enabled by a command enable (described above), load the registers under control of the Data Set DIGO-0 lines. The state of the 74LS164 A and B inputs is shifted into Q_A and the contents are shifted to the right on the rising edge of the clock input. The two 74LS02 low-true AND-gates (A05-1 and A010-3) enable the low-true serial data (DIGO-0) and the low-true clock (CLKO-0) to serially shift the 24 command argument bits into 74LS164's A04, A09 and A14. The low-true CLKI-0 signal has 24 falling (leading) edges which become rising edges through A10-3. 5 microseconds after the serial load has been completed, the trailing edge of the 5 microsecond low-true strobe STRO-0 parallel-loads the 24-bit contents of the serial register (A04 - A14) into the static storage registers A03, A08, A13 and A18. Figure 2, (next page) depicts the digital command timing operations.

FIGURE 2, DIGO-0 TIMING



NOTE: S14 DENOTES F14 SAMPLING POINT

FIGURE 3, DIGI-1 TIMING



NOTE: SDS DENOTES DATA SET SAMPLING POINT

NOTES:
1 SIGNALS SHOWN AT INPUT TO F14 LOGIC
2 TIME IN MICROSECONDS
3 UP ARROWS DENOTE CLOCKING EDGE

FIGURES 2 AND 3
F14 COMMAND AND MONITOR
TIMING DIAGRAMS

The static storage registers are cleared by the power clear circuit when the F14 is powered up or when a momentary power drop-out occurs. This reset clears the Cal command bits (the Cals off state, an innocuous condition) in the Observing Command storage register and the H, C and X command bits to all zeros in the Diagnostic Command register. The zero's state in the Observing Command register is not a concern but the zero's state in the Diagnostic Command storage register is. An all zero's state drive to the receiver control logic is a **STRESS** state and hence undesirable. This problem is solved in the Command Multiplexer logic (described below) which uses 74LS158's (an inverting output, quad 2-line-to-1-line, multiplexer) to select between the A, B and C or A', B' and C' control arguments for the receiver's control logic. Thus the receiver's control logic sees "1's" for the reset state of the Diagnostic Command storage register; this is the COOL command, the desired default control state for the receiver control logic.

Command Register Multiplexers (Sheet 3)

Section 2.1 described the six-argument formats of the Observing and Diagnostic commands which are the result of the requirement for the potential use of two F14's in the F-Rack. The usage of the Slot B/A- term to decode monitor data enables was described in Digital Command and Monitor Data Enable Decode Logic above. The Slot B/A- term is used to control the selection of either the A, B and C or A', B' and C' arguments of the two command messages for control of the three receivers. Quad 2-line-to-1-line multiplexers are used for these selections.

Three 74LS157's (B03, B08 and B13) select either the Observing Command A, B and C or A', B' and C' arguments for control of the Noise Switching Logic (described below).

Three 74LS158's (B18, B23 and B28) are used for selection of the three sets of Diagnositc Command bits which drive the receiver control logic. As noted in the description of the Command Register Logic above, the 74LS158's have inverted outputs so the reset state of the Diagnostic Command register becomes the COOL command state of the receiver control logic.

When the Select input to these multiplexers is low, the 1A, 2A, 3A and 4A inputs are selected for output to the 1Y, 2Y, 3Y and 4Y outputs. A high on the Select input selects the B1, B2, B3 and B4 inputs. Thus when Slot B/A- is tied to logic ground via the J1-1 to J1-N jumper, the command register's A, B, and C inputs are selected. This is the F-Rack F14 #1 configuration. The jumper is omitted for F14 #2. The multiplexer strobe input G is tied to logic ground to continuously enable the multiplexers.

Digital Monitor Logic (Sheets 1 and 2)

The digital monitor data logic is similar to the digital command logic - a set of three serial shift registers. Three parallel-input, serial-output shift registers (74LS165) are parallel-loaded and serially unloaded into the Data Set under control of the Data Set DIGI-0 input lines. Three gates, enabled by a monitor data enable (described above in Command and Monitor Data Enable Logic), permit the low-true STRI-1, DIGI-1 and CLKI-1 signals to read the digital monitor data. Gate A15-3 impresses the 20 microsecond STRI-1 strobe on the three 74LS165 Shift/Load (S/L) inputs. This loads the register with the state on the A through H inputs. 100 microseconds after the rise of STRI-1, the CLKI-1 shift clocks start the serial unload of the 24 monitor data bits in the register to the Data Set DIGI-1 input via gate A06-3.

The DIGI line is driven by an open-collector buffer that is enabled by the monitor data enable. The buffer pull-up resistor is in the Data Set and all the other monitor data sources on the DIGI-1 line sink current through this resistor as they input digital monitor data to the Data Set. The 74LS165 Clock Inhibit inputs are tied to logic ground which permits the shift clocks to unload the register. The LSB

serial input A01-10 is tied to ground so that the register fills with zero's during unload, although this would not be a problem as the shift register is always parallel-loaded by STRI-1 at the start of a new shift sequence.

If the CLKI-1 signal is viewed on an oscilloscope, a curious feature will be seen: there are two pauses in the clock train. These have a duration of one bit period and occur after eight shift clocks. This pause is an artifact of the Data Set monitor shift logic. The monitor data is not stored in a register in the Data Set; the serial stream of data from the F14 is merged directly into the Data Set's message output logic. The pause is used to inject the Data Set's serial parity bit into the message data stream.

A natural question is: is there a possibility of time contention between Data Set command and monitor operations which could obscure the readout of the command echo monitor data? The answer is no; the Data Set command and monitor operations are widely separated in time so there is no possibility of conflict.

Figure 3 (page 16 above) shows the timing of the digital monitor data logic.

Noise Calibration Switching Logic (Sheet 3)

The receivers normally use a 9.6 Hz signal from the L8 to drive the calibration noise sources. For test purposes, the noise source drives can be commanded to seven states via the Observing Command. These states were described in Section 2.1 and are repeated here for convenience.

Observing Commands, Mux 322_8

Condition	MSB			LSB		
F14 Reg bit label	U	A	N	S	H	Cal State
Cals off	0	0	0	0	0	No drive to either noise source
Solar continuous	0	0	0	1	1	Solar (only) continuous noise source drive
Normal continuous	0	0	1	0	2	Norm (only) continuous noise source drive
Both continuous	0	0	1	1	3	Both noise sources on continuously
** Solar auto	0	1	0	1	5	9.6 Hz drive to Solar (only) noise source
* Norm auto	0	1	1	0	6	9.6 Hz drive to Norm (only) noise source
Both auto	0	1	1	1	7	9.6 Hz drive to both noise sources

* Usual observing condition.
** Usual Solar observing condition.
U Denotes an unused command bit.

The calibration control logic (coordinates D3 on Sheet 3) implements this state table to drive the receivers A, B and C calibration switching circuits. This logic is driven by the Observing Command register control bits, Auto, Norm and Solar that are selected from either the A, B, and C set or the A', B' and C' set by the Command Register Multiplexers (B03, B08 and B13, described above).

B02, a 74LS367 non-inverting bus driver, buffers the 9.6 Hz signal from L8 to this calibration control logic and to the three receivers's cal switching circuits on Sheets 4, 5 and 6.

These three mode control bits drive three gates to implement the state table. Consider the receiver A path. If the **Auto** bit is a 1, gate B07-3 passes the inverted 9.6 Hz signal to gates B01-3 and B01-6. If either (or both) the **Norm** or **Solar** bits on these two gates are a 1, and the **Auto** bit is a 1, the inverted 9.6 Hz signal drives the cal switching logic on Sheets 4, 5 and 6. If **Auto** is a 0, gate B07-3 is forced high which inhibits the passage of the 9.6 Hz drive and B07-3 provides a continuous enable to gates B01-3 and B01-6. If either (or both) **Norm** or **Solar** is a 0, gates B01-3 and/or B01-6 are inhibited

and there is no drive to the associated calibration noise sources. If either (or both) **Norm** or **Solar** is a 1 and **Auto** is a 0, the noise sources are driven continuously.

Normal and Solar Cal Drive Logic (Sheets 4, 5 and 6)

These circuits implement the power switching drive to the Normal and Solar calibration noise sources. The noise source drive voltages and currents are sensed and input to Sample/Hold circuits. Since these signals are normally switching and the Data Set analog data sampling is not synchronized to the "On" state of the drive, the Sample/Hold circuits have a constant output which is sampled by the Data Set via the F14 analog multiplexers. The Solar and Normal cal drive and monitor circuits for all three receivers are identical except for component locations.

For simplicity, the Normal and Solar noise cal drive circuits are identical; the noise power delivered to the cooled amplifiers is determined by RF circuitry in the receiver. Examples of such are power splitters, directional couplers, gated amplifiers, etc.

There are two important requirements for a cal switching circuit. It must have a low "On" impedance and must have short rise and fall times so that the noise source operates at a known power level. To meet these power and speed requirements, fast heavy-drive components are used in F14. This heavy drive reduces the time to charge and discharge the capacitances of F14 circuit wiring and F14 to receiver cables.

The cal switch circuitry uses a power MOSFET (Motorola MTP8P08) driven by an open-collector, high-current, high-voltage, power Darlington driver. A 74LS367 buffer (B02, Sheet 3) buffers the 9.6 Hz signal to the Darlington driver. The 74LS367 has a high-power totem-pole output circuit with typical rise and fall times of about 10 ns with a 45 pf load capacitance. For comparison, this is about the same rise and fall time as a 74LS04 with a 15 pf load capacitance. The TTL-compatible ULN2023A Darlington driver is capable of driving large surge currents (up to 500 ma); this high current drive can quickly charge and discharge the circuit shunt capacitances and the MOSFET's 1200 pf gate input capacitance. The typical turn on/off delay of the Darlington is about 250 ns. The MOSFET rise and fall times are 150 ns, the turn-on delay is 80 ns and the turn-off delay is 200 ns. The rough value for the rise or fall times of the noise suorces is thus about 400 ns, a fractional uncertainty in the noise source drive of about 7 parts/million of the drive on period.

The Darlington load is two 2000 ohm resistors to +28 volts. The junction of the two resistors drives the MOSFET gate so that the resultant gate signal swings between +28V (Darlington off) to about +14V (Darlington on). The MTP8P08 MOSFET is a P-channel, enhancement mode FET in which the source-drain current is zero with a source-gate bias of zero. The gate must be driven negative (relative to the source) past a threshold voltage to turn on the source-drain channel. The MTP8P08 threshold (gate to source) is -4.5 volts max, and the Darlington drive is -14 volts so the MOSFET drive is more than adequate. The source-drain resistance is typically 0.25 ohms at room temperature (0.35 ohms at 100^0 C) for currents up to 14 amps. The cal switching circuitry is thus both fast and a low impedance in the "on" state. Section 5.0 has data sheets for the ULN2023A and MTP8P08.

It is useful to monitor the noise source drive voltage and current. Operational amplifiers C01-1 and C01-10 perform this function. The amplifier is an LF347N, JFET input operational amplifier with an internally trimmed input offset voltage (2 mV). The amplifier has a large gain-bandwidth product (4 MHz) and high output slew rate (13 V/usec). The input bias current is 50 pA and input impedance is 10^{12} ohms.

Consider Solar cal circuits on Sheet 4 with amplifiers C01-A and C01-C. Amplifier C01-A is a differential amplifier that is driven by the I_{ND} voltage drop across a 10 ohm resistor. The inverted output

of C01-A drives inverting amplifier C01-C. The output of C01-C, V_C, is a measure of the noise source current and the current/voltage transfer function of the two amplifiers is:

$$I_{ND}/V_C = 1/R_D\{(R_{FA}/R_{IA})(R_{FC}/R_{IC})\}$$

I_{ND} is the noise diode current, R_D is the 10 ohm resistor, R_{FA}, R_{IA}, R_{FC} and R_{IC} are the feedback and input resistors of C01-A and C01-C respectively. Using the circuit values we see that the scaling is 10 mA/V. Thus to determine the value of the noise source current, multiply the data value (in volts) by this transfer function.

Potentiometer C08-1,2,3 is a zero-adjustment on the two-amplifier circuit. The adjustment of this pot is described in Section 3.0.

Amplifier C01-B is a voltage-follower (non-inverting, unity gain) to buffer the divided cal voltage to the voltage Sample/Hold circuit (Analog Devices AD582). This buffering eliminates perturbations of the C01-A and C by Sample/Hold charge transfer effects. Note that the pot and two associated resistors are a voltage divider with a factor of 4.

The Sample/Hold circuits are set to the sample mode by the (always active) 9.6 Hz signal from the 74LS367 buffer which drives the +LOGIC S/H input. The S/H is set to the Hold mode when the +LOGIC input is high (it must be > 2.0 volts). When this input is <0.8 volts the S/H is in the Sample mode. Note that this 9.6 drive is opposite in phase to the drive to the (inverting) ULN2032A driver. The driver's output is in phase with the 9.6 Hz +LOGIC drive so the S/H is in the sample mode when the noise source is being driven. The hold capacitor is charged during the sample period and this charge drives the S/H output amplifier during the hold period. The droop rate during the hold period is 10 mV/sec with the 0.01 uf hold capacitor. Over the 55,000 usec of hold period, the output droop is thus about 0.55 mV.

The AD582 is configured as a voltage follower, i.e., the signal is applied to the + input and the output is fed back to the -input. A pair of back-to-back 10-volt zener diodes and limiting resistor limit the output swing of the AD582. This is done to protect the analog multiplexers from an over-range input in the event that the 9.6 Hz drive is lost. This could happen on the test bench or when an antenna cable is disconnected. Section 5.0 has data sheets for the AD582 and the LF347N.

Power Reset Logic and +5V Critical Power Regulator (Sheet 3)

The power reset circuit is a simple RC circuit with a diode clamp. When 5-volt power is applied, the 22 uF capacitor charges to +5 volts through the 1 Kohm resistor; the time constant is 22 msec. The capacitor output is connected to the Clear inputs of the command storage registers which holds them reset until the capacitor voltage exceeds the logic threshold of the chip input, about 1.6 volts. Assuming that the 5-volt power is applied as a step and the capacitor charge rate is roughly linear below the 1 TC point, the time delay to the threshold voltage is about 11 msec, a period more than adequate to reset the storage registers. The diode protects the chips from the capacitor charge (+5 volts) when the power is turned off. When the power is removed, the Clear inputs are limited to the 0.6V diode forward drop.

An LM7805 linear IC regulator powered by Critical +15V provides +5 volt power to the 7406 Pump Request Monitor drive (front panel) indicator LED drivers (EG10). The Critical power common is ground-referenced to the Rack F DC power common in the bin wiring.

2.5 FRONT PANEL DISPLAY LOGIC (Sheet 9)

The front panel alphanumeric displays are an important feature of the F14. The display consists of three pairs of **Serial Number** (upper) and **Band** (lower) LED displays for receivers A, B and C (left-to-right). Sequencing and code conversion logic on the left side of Sheet 9 select the serial number ID code and frequency ID code bits for conversion to ASCII codes and storage in the display. The HPDL-2416 is a "smart" display with an internal RAM memory which stores the display characters in ASCII format. This section describes the process of storing the two parameters in the display memory; a detailed description of all the display features is unnecessary and beyond the scope of this manual. The display chip has several features such as decimal points, blanking, a cursor character, etc., which are not used by the F14; since they are not used, they will not be described. A data sheet for the HPDL-2416 is included in Section 5; the interested reader may wish to refer to it in the following discussion. The timing diagram on page 7-40, the logic diagram on page 7-42 and truth table on page 7-43 are of particular interest.

The 2416 inputs for functions that are not used are tied low or high as required by the 2416 truth table.

The display logic can be considered to consist of two parts: 1) The bit selection and memory address-load logic; 2) The code conversion logic. The bit selection and memory address-load logic develops sequencing terms which are used to drive both the Serial Number and Band displays. The two sets of bit selection logic each use three identical selector chips for code bit selection. The code conversion logic implementations are different for the two displays; this will be described later.

We will first consider the bit selection and memory address-load logic. The three sets of display chip RAM memories (for receivers A, B and C, left to right) are each loaded serially with four ASCII characters: Dig0, Dig1, Dig3 and DIG3, right-to-left. There are two aspects: 1) display chip selection; 2) digit memory selection and loading. This logic cycles continuously and is clocked by the 9.6 Hz cal switching signal.

The reader should refer to Figure 4 (next page) and Sheet 9 during the following discussion.

The 9.6 Hz cal switching signal clocks B16, a 74LS161 synchronous binary counter (at coordinates D7 of Sheet 9). The counter's four Q outputs (terms T0, T1, T2 and T3) are the sequence logic control terms. The 74LS161 sequences through sixteen states, 0 through 15.

Terms T2 and T3 control the selection of the receiver ID and band code ID bits. The code bit selector is a parallel multiplexer which simultaneously selects all 6 code bits from a receiver. Receiver A bits are selected first, receiver B bits secondly and receiver C bits thirdly. Two sets of dual 4-line-to-1 line multiplexers (74LS155) implement the code bits multiplexer. (The reader should review the 74LS155 multiplexer logic in a TTL data book.) Chips C05, C10 and C15 select the receiver ID code bits and chips C20, C25 and C30 select the receiver band code bits. The T2 and T3 terms sequence through four states during the 16 state sequence of counter B16; the first three T2-T3 states are used; the last is not. The first T2-T3 state (counter states 0 through 3) selects receiver A code bits, the second state (counter states 4 through 7) selects receiver B code bits and the third state (counter states 8 through 11) selects receiver C code bits. The six-bit parallel outputs of these two multiplexers are presented to two ASCII code converters for sequential conversion to four ASCII characters for input to the 2416's; the code converters are described below.

We will next consider the RAM loading logic. Terms T2 and T3 also drive the A and B inputs of a 74LS138 decoder (3-lines-to-8-lines); the C, G2A and G2B inputs are tied to logic ground. The 9.6 Hz clock drives the G1 input. (The reader should review the 74LS138 decoder in a TTL data book.) Assuming for the moment that G1 (the 9.6 Hz signal) is always high, only the 74LS138 Y0, Y1, Y2 and

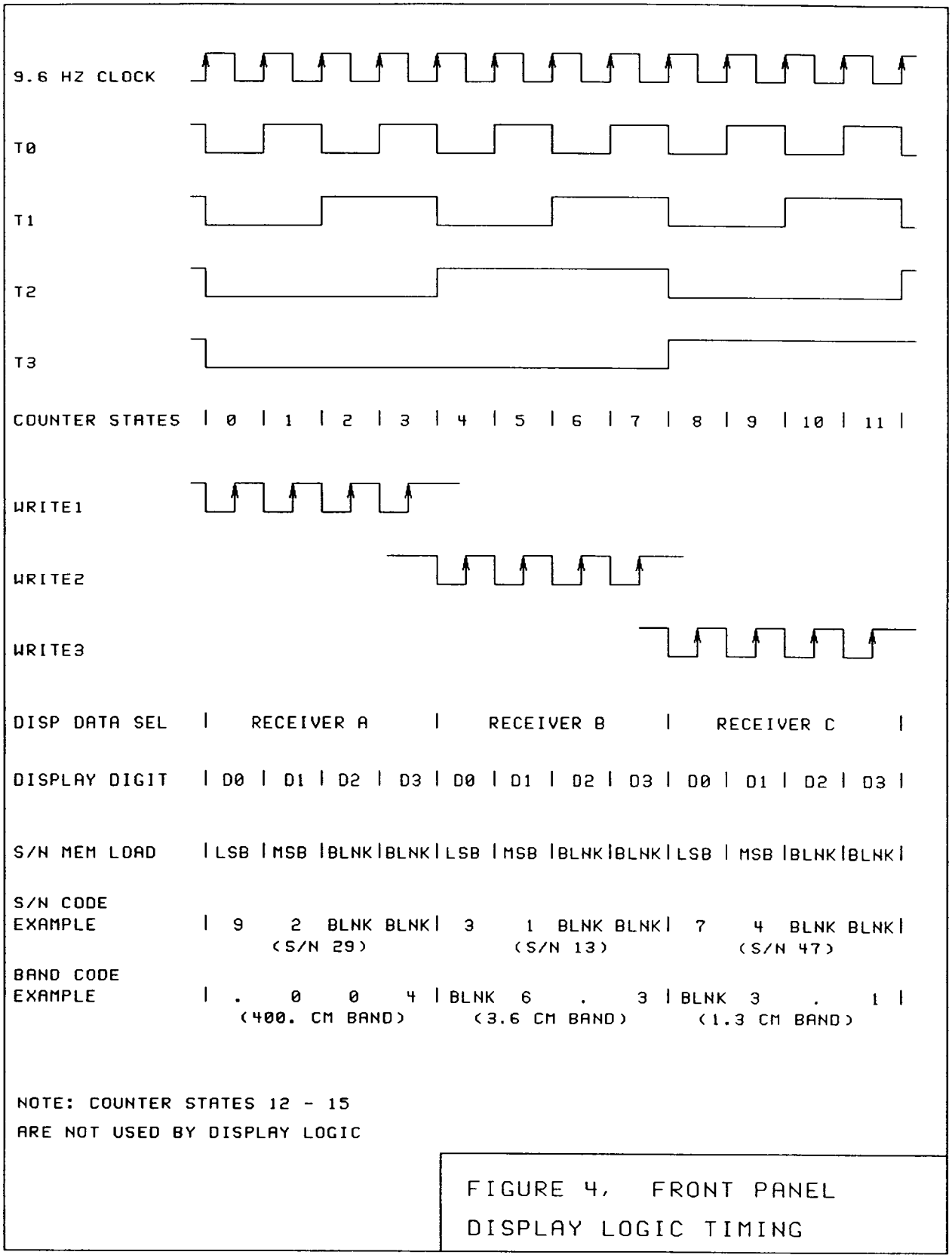


FIGURE 4. FRONT PANEL DISPLAY LOGIC TIMING

Y3 outputs will ever be active (low) for the sequencing inputs T2 and T3 because the C input is grounded. The Y0, Y1 and Y2 outputs (labelled WRITE1, WRITE2 and WRITE3) are used to load the three receiver display chip RAM memories. Now consider the action of the 9.6 Hz clock on the G1 input. When G1 is high, the Y0, Y1 and Y2 outputs are active (low) and when it is low, the three outputs are high; thus the 9.6 Hz signal is passed through the 74LS138 and inverted; T2 state changes are the result of four counts of the 9.6 Hz clock. The Y0, Y1 and Y2 outputs thus have four 9.6 Hz clock components as shown on Figure 3. Note that the Y0, Y1 and Y3 outputs are low for the first half of each 9.6 Hz period. These three sets of four clocks are the Write clocks for each memory digit of the three 2416's. WRITE1 is the display chip WR- term and drives the receiver A displays, WRITE2 drives the receiver B displays and WRITE3 drives the receiver C displays. (The reader should review the HPDL-2416 timing diagrams on 2416 data sheet page 7-40). Note that the trailing edge of the WR- pulse is used to strobe the memory). Since the 2416 addresses and input data are formulated at the start of each counter state, there is about 55,000 microseconds of settling time before the data is strobed into the 2416.

The 2416 display chips use a two-bit address, A_0 and A_1, to select each RAM location address. Terms T0 and T1 (from counter B16) drive these address inputs. Thus T0 and T1 address the four memory locations and the four WRITEn clocks strobe the ASCII character on the chip data inputs (D0 ... D6) into the addressed RAM locations.

Remember that the receiver serial number code is a six-bit binary code and the receiver band code is a 4-bit binary code with even parity bit; two different processes are required but both must generate a sequence of four ASCII values.

We will first consider the receiver ID code converter which is a binary to BCD process. The receiver ID code is a 6-bit value ranging from 1 through 63 and the converter sequentially generates four ASCII characters. The four digits always have leading zeros and are right-adjusted in the display. Receiver ID code display values thus range from --01 to --63 (- denotes a blanked or non-illuminated digit, more about the blanking later).

A 74185 binary to BCD converter chip is used to convert the 6-bit value. (The reader should review the operation of the 74185 chip in a TTL data book.) This case of binary to BCD conversion is very simple. The least significant bit (2^0) is identical in both code formats. Binary code bits 2^1 through 2^5 are input to the 74185 A through E inputs. The 74185 Y1 (MSB), Y2 and Y3 outputs in conjunction with the 2^0 bit form the least significant BCD digit. These four bits are connected to the "A" inputs of C05, a 74LS157 quad 2-line-to-1-line multiplexer. C05's Select input (-A/B on the logic diagram) is connected to T0 and the strobe input is connected to T1. When the strobe input is low, the four Y outputs follow the four inputs selected by the -A/B input. If -A/B is low and strobe is low, the outputs follow the A inputs. If -A/B is high and strobe is low, the outputs follow the B inputs. If the strobe is high, the outputs are forced low, irrespective of the state of the -A/B input.

Remember that T0 and T1 cycle through a four state sequence starting with 00 (state 0) and ending with 11 (state 3). Thus in state 0, C05 selects the A inputs (the LSD of the converted value) for input to the lowest 2416 data inputs (D0, D1, D2 and D3; the state of the other inputs are described below). In state 1, C05 selects the B inputs, the MSD of the converted value. Since the code value is never greater than 63, the most significant bit in the MSD is always a zero; thus input 4B on C05 is connected to logic ground.

At this point, the 74185 converter has generated two digits of BCD code. We know that the upper display digits are 0's; how are they generated? During states 2 and 3, the strobe input of C05 is set high by T1; this forces all outputs to the zero state which produces a BCD value of zero.

The reader should refer to the 2416 ASCII codes shown on 2416 data sheet, page 7-44. Note that this is an abbreviated code set; not all ASCII codes are recognized by the 2416's 64-character code generator. Note that there is a code for a decimal point; this character is used in the display and uses one digit space. Codes which are not in this set are ignored by the character generator.

At this point four sets of BCD digits have been sequentially generated and presented to the 2416's D0, .. D3 inputs. How are the upper three bits of ASCII code for these four characters generated? The 2416's ASCII code table shows that for the 0 through 9 character set, ASCII code bits D6, D5 and D4 are 0, 1 and 1, respectively. The 2416's D5 and D4 inputs are forced high by a pull-up resistor to +5V making bits D5 and D4 a 1. Bit D6 is driven by T1, which is low for T0-T1 states 0 and 1 (the periods for conversion and entry of the LSD and MSD characters). The proper upper ASCII bits (D4, D5 and D6) are thus appended to the lower four converted bits for each of the first two display characters. T1 drives D6 high during states 2 and 3 (the periods for conversion of the upper two display characters). This produces a 1, 1, 1 code on 2416 inputs D6, D5 and D4. Referring to 2416 data sheet page 7-41, when D5 = D6 in the RAM, the associated display character is blanked. Thus the two left digits of the display are blanked.

During the first half of each T0-T1 state, a memory write signal, (one of the WRITEn clocks) clocks the associated ASCII character into the RAM. This was described above.

The receiver band code converter is quite simple and uses an Intel 2732 (4K by 8 bits) EPROM for conversion logic.

The band ID code is shown below. The most significant bit is always a 0 or 1 and is an **even** parity bit for the four bits of receiver band code.

Receiver Frequency Band Code and Band Display

Parity P_B	Code$_{16}$ B_0-B_3	P_B + B_0-B_3	Display	EPROM Data	Parity P_B	Code$_{16}$	P_B + B_0-B_3	Display	EPROM Data
0	0	00	400.	'.004'	1	0	10	^BAD	'DAB '
1	1	11	^BAD	'DAB '	0	1	01	50.0	'0.05'
1	2	12	^BAD	'DAB '	0	2	02	20.0	'0.02'
0	3	03	13.0	'0.31'	1	3	13	^BAD	'DAB '
1	4	14	^BAD	'DAB '	0	4	04	^6.0	'0.6 '
0	5	05	^3.6	'6.3 '	1	5	15	^BAD	'DAB '
0	6	06	^2.8	'8.2 '	1	6	16	^BAD	'DAB '
1	7	17	^BAD	'DAB '	0	7	07	^2.0	'0.2 '
1	8	18	^BAD	'DAB '	0	8	08	^1.3	'3.1 '
0	9	09	^0.7	'7.0 '	1	9	19	^BAD	'DAB '
0	A	0A	0.35	'53.0'	1	A	1A	^BAD	'DAB '
1	B	1B	^BAD	'DAB '	0	B	0B	^BAD	'DAB '
0	C	0C	^BAD	'DAB '	1	C	1C	^BAD	'DAB '
1	D	1D	^BAD	'DAB '	0	D	0D	^BAD	'DAB '
1	E	1E	^BAD	'DAB '	0	E	0E	^BAD	'DAB '
0	F	0F	^BAD	'DAB '	1	F	1F	^BAD	'DAB '

Notes: ^ denotes a blanked display digit. The (') character delimits the EPROM data. The period (.) character is one display digit. A blank space ( ) in the EPROM data is an ASCII space character. The EPROM start address is 000_{16}.

The four band code and parity bit are an address which drives EPROM 2732 address inputs A2,... A6 (2^2,...2^6, respectively) and the T0 and T1 sequencing terms drive the A0 and A1 inputs (2^0 and 2^1 respectively). Address lines A7,...A11, the chip enable (CE-) and Output Enable (OE-) are grounded. The ASCII code portion of the 2732 can be considered to be a memory consisting of 32 sets of four-byte wavelength values, where each byte contains an ASCII character to be loaded into the 2416 RAM memory.

Eight of these sets are assigned to error-free, assigned wavelength values and 24 are assigned to parity error or unassigned cases. The selected bytes set is addressed by the A2,...A6 address (the band ID code plus parity) and each byte in the four-byte set is addressed by the T0, T1 states on the A0, A1 inputs. The base address of each set is 00 and the top address is 11, corresponding to the beginning and end of the T0-T1 four-state sequence.

Seven of the eight 2732 EPROM data outputs (O0, O1, ... O7), are connected to the seven 2416 display D0....D6 inputs. As T0 and T1 sequence through the four states, the four-byte contents of the addressed byte set is read into the 2416 RAM by the strobe logic described above. The eight assigned, error-free, band ID code wavelength values are stored in the EPROM locations defined by the addresses. All parity error and unassigned code cases have the four ASCII bytes "-BAD" stored in these sets of locations. The -BAD and the error-free wavelength values are shown in the table above.

2.4 ANALOG SIGNAL MULTIPLEXING AND CONDITIONING

This section describes the analog signal multiplexing and signal conditioning. Remember that there are two classes of analog data: Common Analog and Receiver-Specific functions. Each set consists of 16 parameters and were listed in Section 2.1 above. Channels labled gnd (spare) are available for future use but would require a non-trivial modification of the F14 wiring. These channels have been provided with RC filters but the filter inputs are connected to analog ground.

Analog Signal Conditioning (Sheets 8 and 9)

Each channel has an RC filter that provides some charge-transfer isolation to reduce perturbations to signal sources during sampling. The multiplexer chips (HI-508's) have break-before-make properties but circuit wiring and chip capacitances (although small) can retain charges between actuation of the multiplexer channels. The Data Set defaults the four multiplex address lines to address 15_{10} (Hex F) between command or monitor operations; the stored charge associated with this address state is the charge that exists on this capacitance when an analog signal is selected. The 0.1 uF capacitor in the RC filter will be charged to the signal source voltage (all the signals are DC values); this capacitor must charge the multiplexer-wiring capacitances. Assuming a channel filter capacitor is charged to +10 volts and the multiplexer default address (F_{16}) had selected a -10 volts source, the worst case signal swing on a multiplexer output is 20 volts. Estimating 50 pF for the HI-508 chip and wiring capacitances and using Data Set multiplexer "on" capacitance of 100 pF, the filter capacitor charge is reduced by about 3 mV, about a 1/2 count error in the converted value. This (worst case) 3 mV charge must be replaced by the signal source through the 1000 ohm filter resistor. The charge time constant is about 50 ns so the output, wiring and Data Set input capacitance is charged within about 1 us. The Data Set A/D shifts to the "Hold" mode 30 us after the multiplex address goes true; thus there is more than adequate time for analog settling before A/D conversion is initiated.

Signal voltages greater than 10 volts are divided by a divider resistor across the filter capacitor. These are 15 and 28 volt signal cases.

Clamping diodes on the HI-508 inputs and outputs will clamp over-range inputs or outputs to the +15V or -15V chip inputs. Chip damage under these conditions is very unlikely because the 1000 ohms (or 5110) ohm resistors in the RC filter circuits will limit "On" channel current to less than the 20 mA limit.

An HI-508 data sheet is included in Section 5.

Analog Signal Multiplexing (Sheets 8 and 9)

The F14 has four 16-channel analog multiplexers - one for the Common Analog parameters and one for each of the three Receiver-Specific parameters. Each of these multiplexer outputs is connected to a differential-input multiplexer in the Data Set. Each 16-channel multiplexer consists of two eight-channel, single-ended analog multiplexer chips. One multiplexer selects one of the lower eight signals and the second selects one of the upper eight signals. The multiplexers have internal one-of-eight decoders which drive the analog switches. The decoder has an enable input which permits the decoder outputs to drive the analog switches. Thus the three lower Multiplex Address bits (2^0, 2^1 and 2^3) activate (via the one-of-eight decoder) one of the channels on each multiplexer and the most significant bit (2^3) enables the lower or upper multiplexer decoder. The two multiplexer outputs are tied together and drive the + (signal high) input of the Data Set multiplexer.

Each receiver provides an analog ground reference line (QGND) that is connected to a Data Set analog multiplexer - (signal low) input. This ground reference may differ from the F14 analog common by a small common-mode voltage resulting from the voltage drop of the +/- 15 Critical power wire between the CPP and receiver. Since the Data Set analog inputs are differential and have a high common-mode rejection (about 80 db), the receiver common-mode signals have a negligable effect upon the converted values.

The Common Analog ground reference is the F14 +/- 15V common which is tied to the - (low side) input of the Data Set multiplexer.

10 Volt Reference (Sheet 8)

To provide a means of checking the Data Set A/D converter gain drift, the F14 has an Analog Devices AD2702 precision reference. The +10 volt and -10 volt outputs are connected to the inputs of the Common Analog multiplexers. The A/D converter zero drift can be checked by the Analog Ground value. The AD2702 data sheet is included in Section 5.

2.6 COMMAND SIMULATOR CONTROL OF THE SINGLE-BAND, FRONT END RECEIVER

For test or maintenance purposes it may be useful to locally command the receivers cryo or the cal circuitry via the Command Simulator. This section describes how this may be done. (The Command Simulator is easy to use but the reader may wish to refer to the Command Simulator manual for additional details.) Single-Shot commands should be used; this avoids the possibility of sending garbage commands to the receivers when the thumbwheel switches are being set up in the recurrent command mode.

Remember that the F-Rack F14's are controlled by Data Set #4.

Consider the **Diagnostic Commands** which have the following **F14 Register** format.

Diagnostic Command Format, MUX 323_8

Rcvr	A	A'	B	B'	C	C'
Bit	0 1 2 3	4 5 6 7	8 9 10 11	12 13 14 15	16 17 18 19	20 21 22 23
	H C X U	H C X U	H C X U	H C X U	H C X U	H C X U

F14 Reg bit label	U	X	C	H	
OFF	0	0	1	0	
COOL	0	0	0	0	(Usual observing condition)
STRESS	0	0	1	1	
HEAT	0	0	0	1	
PUMP	0	1	0	1	

The Command Simulator's octal command argument thumb-wheel switches (S0 ... S8) are in **Numeric Format**, i.e., LSD on the right - the reverse of the **Register Format** shown above. Rearranging the table above to **Numeric Format** and adjusting the column spacing to conform to octal format, we get the table shown below. These switch settings can be verified by checking the hex format LED display.

Diagnostic Command Thumbwheel Switch Settings

F14 Arg bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Function	U	X	C	H	U	X	C	H	U	X	C	H	U	X	C	H	U	X	C	H	U	X	C	H
F14 #1							¦---- C ------¦						¦---- B ------¦						¦---- A -----¦			
F14 #2	¦---- C'-----¦						¦----- B'-----¦						¦---- A' -----¦											
Switch	(MSD) S8				S7			S6			S5			S4			S3			S2			S1 (LSD)	

	U	X	C	H									
COOL	0	0	0	0	0	0	0	0	0	0	0	0	0
OFF	0	0	1	0	1	0	4	2	1	0	4	2	
STRESS	0	0	1	1	1	4	6	3	1	4	6	3	
HEAT	0	0	0	1	0	4	2	1	0	4	2	1	
PUMP	0	1	0	1	2	5	2	5	2	5	2	5	

Next consider the **Observing Commands** in **Register Format.**

Observing Command Format, MUX 322_8

Rcvr	A				A'				B				B'				C				C'			
Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
	S	N	A	U	S	N	A	U	S	N	A	U	S	N	A	U	S	N	A	U	S	N	A	U

S = Solar command bit, N = Normal command bit, A = Auto command bit, U = Unused command bit.

F14 logic maps these **Observing Command** bits into a state table as follows:

Condition	MSB			LSB	
F14 Reg bit label	U	A	N	S	Cal State
Cals off	0	0	0	0	No drive to either noise source
Solar continuous	0	0	0	1	Solar (only) continuous noise source drive
Normal continuous	0	0	1	0	Norm (only) continuous noise source drive
Both continuous	0	0	1	1	Both noise sources on continuously
** Solar auto	0	1	0	1	9.6 Hz drive to Solar (only) noise source
* Norm auto	0	1	1	0	9.6 Hz drive to Norm (only) noise source
Both auto	0	1	1	1	9.6 Hz drive to both noise sources

** is the usual Solar observing condition. * is the usual Normal observing condition. U can be either 0 or 1, shown as a 0 for the table hex code.

Rearranging the table above in the same manner as the Diagnostic Command case above we get the following:

Observing Command Thumbwheel Switch Settings

F14 Arg bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Function	U	A	N	S	U	A	N	S	U	A	N	S	U	A	N	S	U	A	N	S	U	A	N	S
F14 #1							C								B							A		
F14 #2				C'					B'								A'							
Switch	(MSB) S8				S7				S6				S5				S4				S3			S2				S1 (LSD)

	U	A	N	S																
CALS OFF	0	0	0	0	0			0			0			0			0			0
SOL CONT	0	0	0	1	0			4			2			1			0			4			2			1
NORM CONT	0	0	1	0	1			0			4			2			1			0			4			2
BOTH CONT	0	0	1	1	1			4			6			3			1			4			6			3
SOL AUTO	0	1	0	1	2			5			2			5			2			5			2			5
NORM AUTO	0	1	1	0	3			1			4			6			3			1			4			6
BOTH AUTO	0	1	1	1	3			5			6			7			3			5			6			7

3.0 MODULE ALIGNMENT AND TEST

This Section describes the test bench module alignment and test functions that consists of two parts: analog tests and digital tests.

A vital factor in the quality of a module test is the realism of the test environment and the rigor of the tests. The essentials of this environment are as follows:

1) A source for Data Set-compatible Digital commands and digital monitor signals. The VLA Monitor and Control Lab test bench provides all the requisite features to stimulate F14 and to evaluate the response of the F14 digital and analog circuitry.

2) A set of power supplies to power F14: +/-15 volts, +5 volts and +28 volts.

3) A TTL-level signal of about 10 Hz to simulate the L8 9.6 Hz signal. The frequency is not critial but it should be a square wave.

4) An F14 test harness to connect the test bench to F14 connectors P1, P2, P4, P6 and P3, P5, P7. The harness would have only one set of DB25 connectors which are first connected to the P2-P3 pair, next to the P4-P5 pair and then to the P6-P7 pair for sucessive tests of the receiver interface signals. The details of implementing this simple test harness are not included here.

Features of this test harness are:

A) The test bench +/-15 is connected to both the P1 module power and Critical Power pins.

B) The 28 volt supply is connected to the P1 28 volt pins.

C) The P3 connector has jumpers to connect the receiver control signals X, C and H to P3 control mode monitor signals X, C, H and discretes S, P and M. This permits simulation of the response of the receiver's control logic and connector wiring. When the three receiver's control signals are sequenced through the test states by digital commands, the receiver's response can be evaluated on the digital monitor data.

D) The 10 Hz TTL signal is connected to the 9.6 Hz input on P1.

E) A set of 12 toggle switches to simulate the receiver's serial number ID code, frequency band ID code and the modification code. An additional toggle switch is used on the Slot B/A- P1 pins to actuate the command register multiplexers.

F) A pair of resistors on the P5 connector to simulate the noise source loads.

G) A set of voltage divider resistors powered by the + and - 15 volt power supplies to provide unique test voltages to stimulate the following analog signals: 1) The P1 analog inputs Vacuum pump current, Helium supply and return pressures; 2) The P2 analog inputs Pump and Dewar vacuum, AC current, four temperature (15, 50, 300 and Sens.), the six receiver amplifier gate voltages (RCP and LCP Stage 1's and Stage 2-3 sums) and the LED voltage. The dividers output levels should be accurately measured and recorded for comparison with the F14 test data.

The F14 to be aligned should be power-short tested before installation of chips and dip headers. If there are no apparent problems, the IC chips and dip headers should be properly installed and checked before installation of power. Check for bent-over IC pins that could cause shorts to the ground plane or

stuck signals. In the test environment outlined above, apply power to F14; if there are no smoke signals, perform the following tests in sequence.

1) Apply digital commands to test the two sets of command loading and storage registers. Read the command echo registers by stimulating digital monitor channels. First command a sequence of command states consisting of: (a) all 1's, (b) all 0's, (c) alternating 1's an 0's, (d) an lsb and msb of 1's, all other bits 0's, (e) an lsb and msb of 0's, all other bits 1's. Secondly, sequence through the receiver's A, B, C, A', B' and C' operating states shown in Section 2. Actuate the Slot B/A- switch during these tests to exercise the command multiplexer logic.

   Observe the response of the command echo digital monitor outputs to these command states. If the command echo monitor data output does not identically agree with the commanded states, trouble-shoot the command and command echo monitor data logic circuits. The details of these checks are straight-forward and involve checks of the stimulus signals through the enable circuits, presence of load and shift clocks on the registers and flow of serial data through the registers.

2) Test the response of the digital monitor circuitry by actuating the receiver serial number ID, receiver band ID and Modification toggle switches. It should not be necessary to sequence through all possible states; toggling actuations of each switch should be adequate. During this test, verify that the serial number and band display values on the front panel displays are correct. Sequence the test harness through the three sets of DB25 rear panel connectors to check all connector inputs.

   Test the response of the digital monitor circuitry to the receiver discretes monitor inputs by commanding 1's and 0's for the six receiver's X, C and H control inputs. Actuate the Slot B/A- switch for these tests. Verify that the six monitor discretes (X, C, H, P, S and M) are correct in the digital monitor data output. If not correct, check the monitor data logic with tests similar to that suggested in step 1 above. Check the front panel Pump LED when the P discrete becomes a 1.

   Check the receiver serial number ID, the frequency band ID and the Mod codes on the digital monitor data output. During this test, set invalid band codes on the frequency band ID switches and check that the front panel band display shows -BAD. Next set improper parity on the parity switch and observe that the display shows -BAD.

3) Test the response of the Observing Command circuitry by commanding the cal states shown in Section 2. Observe the 28 volt signals impressed upon the two resistors which simulate the solar and normal noise sources. Check the Solar and Normal LED's on the front panel.

4) Command the cal switching circuitry to the continuous on state without a load to simulate a noise source. Adjust the current zero potentiometer for a zero volts +/- 5 mV output from the second stage of the current-to-voltage amplifier. Connect a load resistor to simulate a noise source to the noise cal output and verify that the amplifier output is a correct measure of the load current. The current-to-voltage scaling of this amplifier is 10 mA/V. Verify that the current Sample-and-Hold output is correct.

   With the switching circuit in the on state, verify that the cal voltage follower amplifier and associated Sample-and-Hold output is +7 volts.

   With an oscilloscope check the voltage and current Sample and Hold circuits for droop. The droop should be less than 5 mV over the hold period.

5) Check the Common Analog and three Receiver-Specific analog signals for proper correspondance with the test stimulus values.

4.0 DRAWINGS

This section contains B-sized reductions of the following drawings:

D13190S04 F14 Schematic Diagram

D13190P10 F14 Assembly Drawing

C13190P10 F14 Front Panel Assembly Drawing

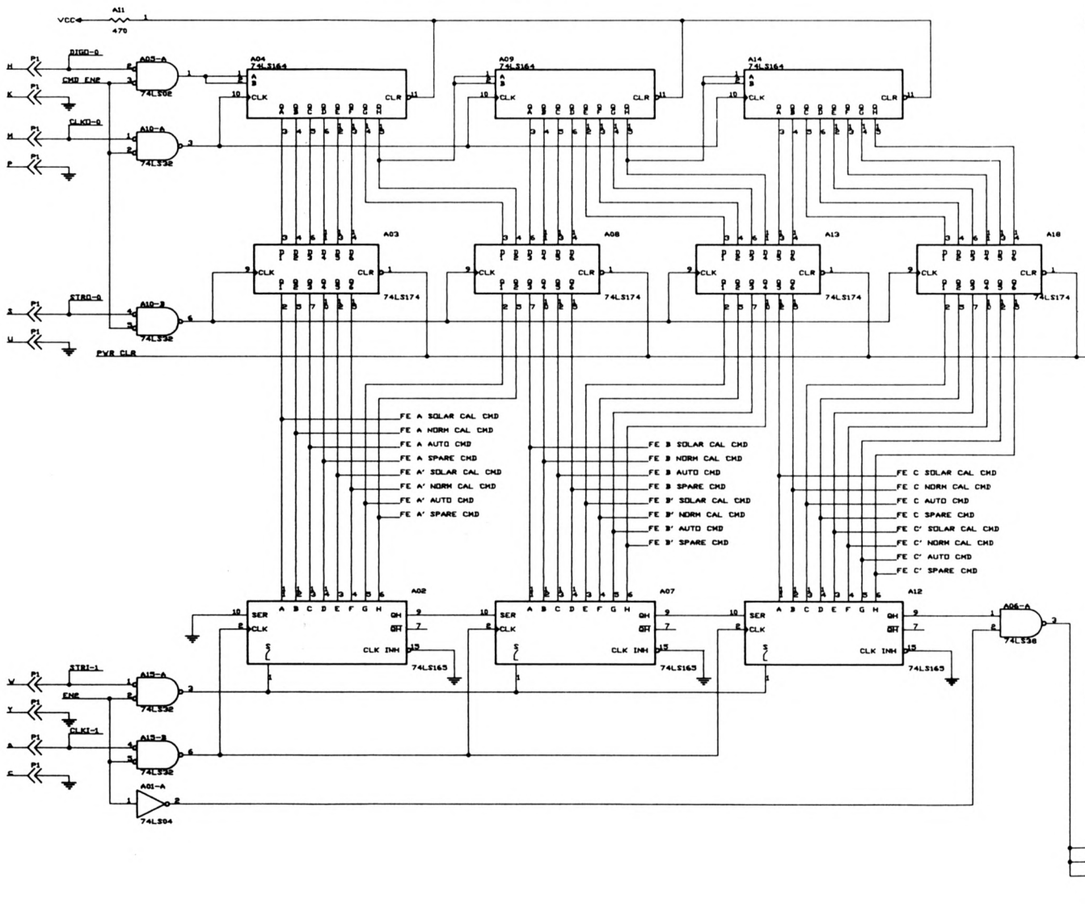
A13190Z06 F14 Assembly Bill of Materials

A13190P11 F14 IC Location Diagram

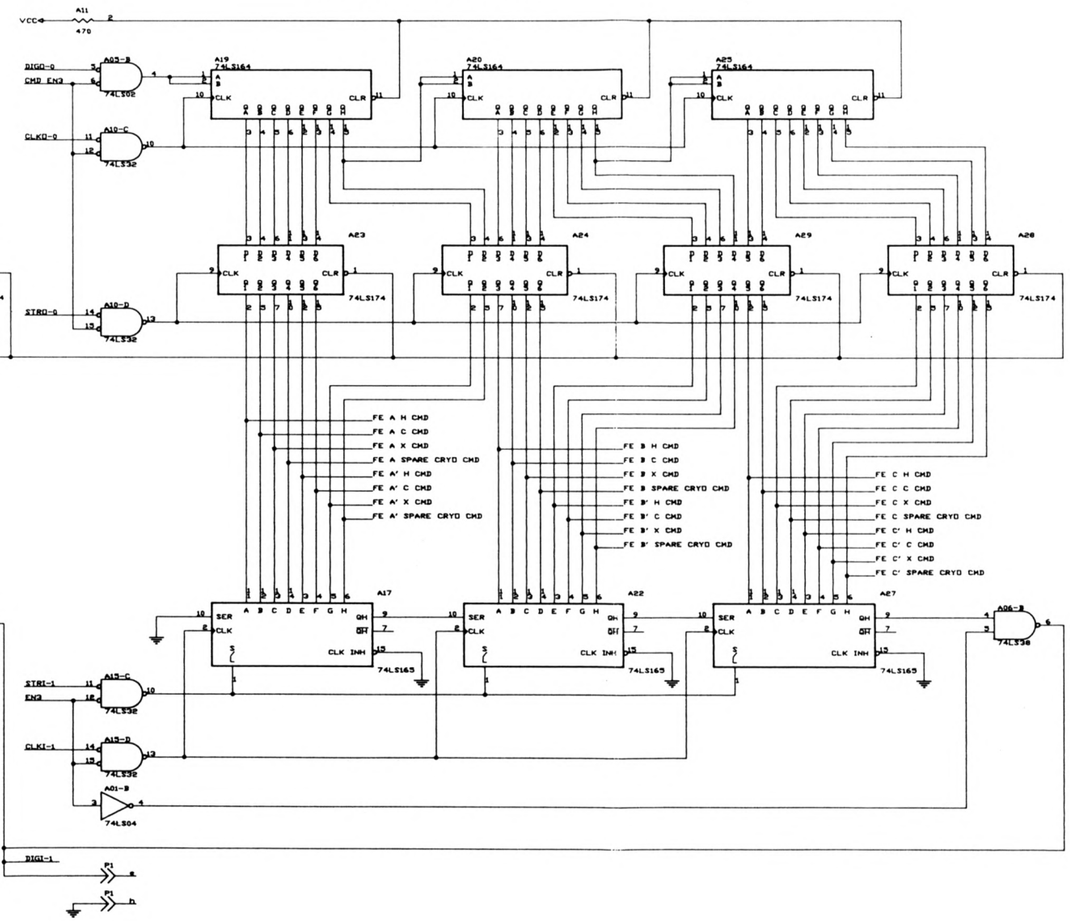
A13190P12 F14 Dip Header Assembly Drawing

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

OBSERVING COMMAND AND ECHO



DIAGNOSTIC COMMAND AND ECHO

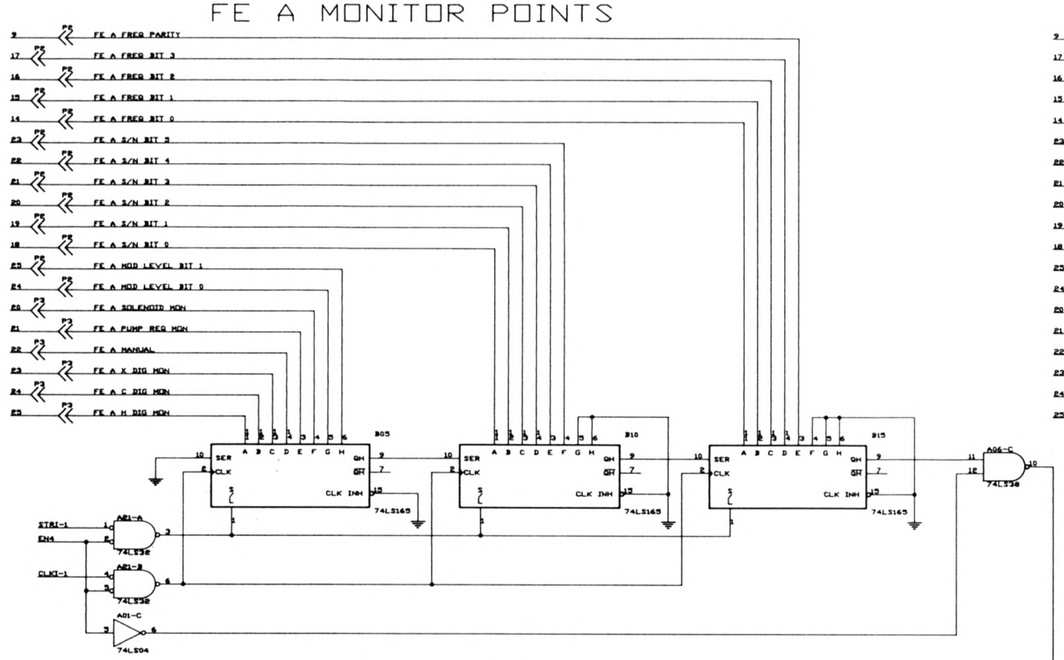


ACAD : F14SK-1

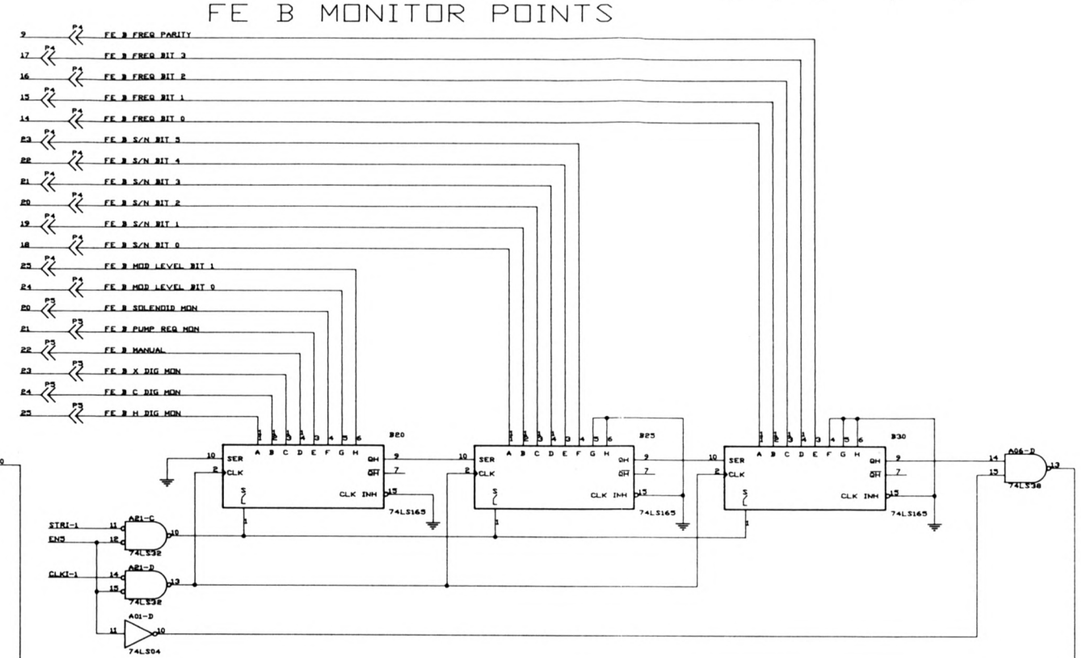
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	VLA PROJECT: F14 FE CONTROL INTERFACE	NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801
TOLERANCES : ANGLES ± ——	TITLE: F14 FE CONTROL INTERFACE SCHEMATIC DIAGRAM	DRAWN BY ANDREATTA DATE 8-90
3 PLACE DECIMALS (.000) ± ——		DESIGNED BY KISKI DATE 8-90
2 PLACE DECIMALS (.00) ± ——		APPROVED BY DATE
1 PLACE DECIMALS (.0) ± ——		
MATERIAL : ——		
FINISH : ——		
NEXT ASSEMBLY / DWG. TYPE	SHEET NUMBER 1 of 9 / DRAWING NUMBER D13190S04	REV. / SCALE —

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

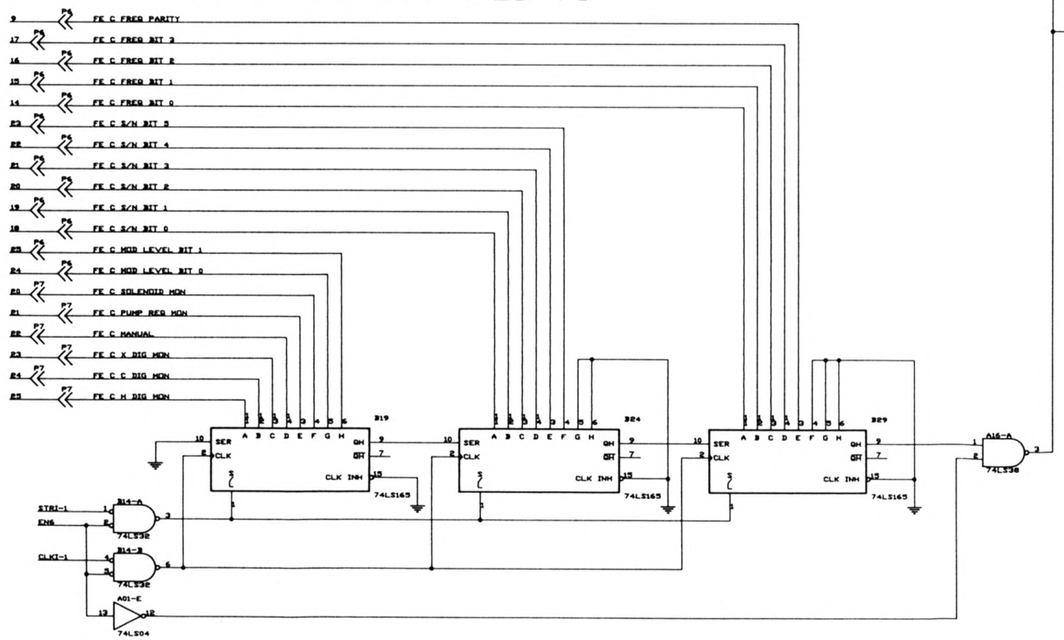
FE A MONITOR POINTS



FE B MONITOR POINTS



FE C MONITOR POINTS



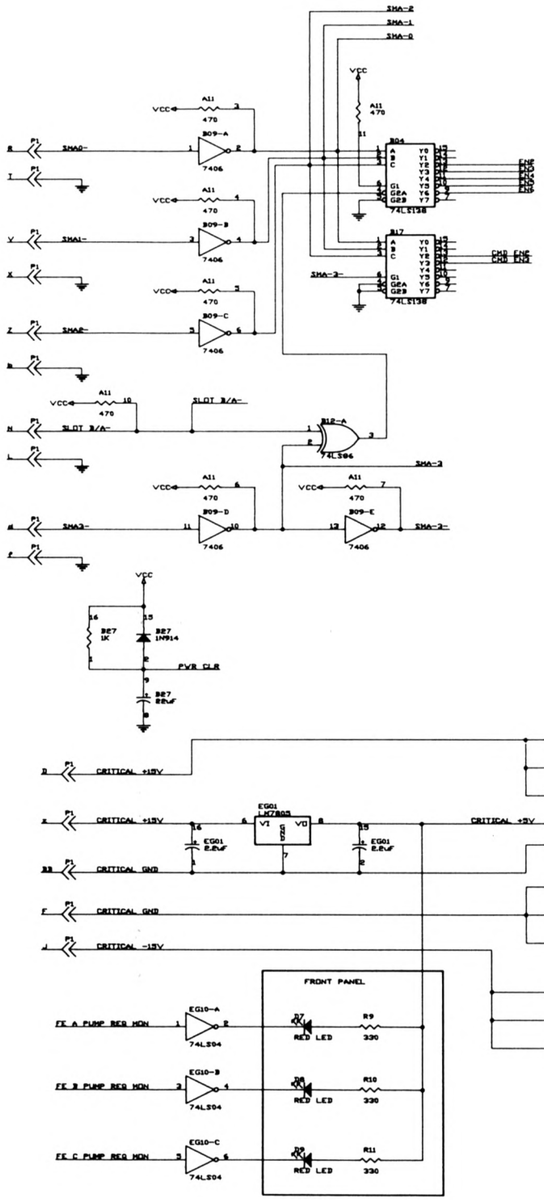
ACAD : F14SK-2

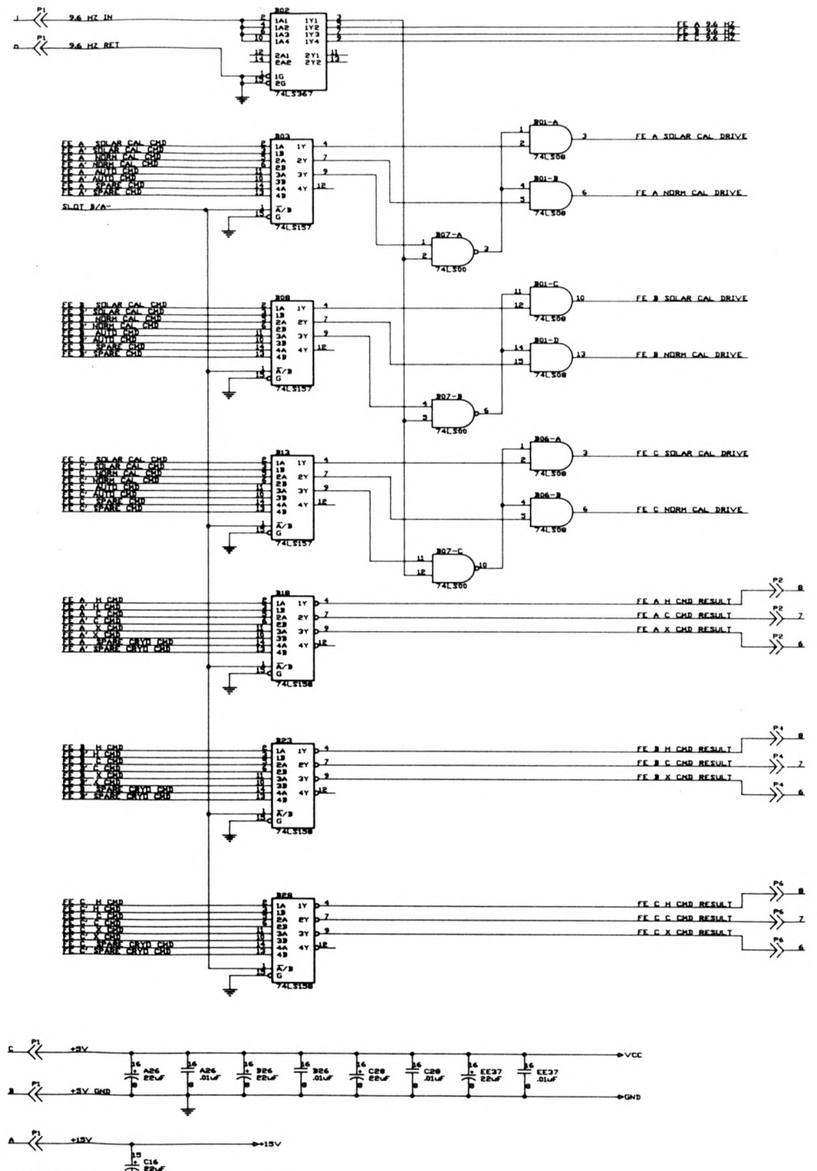
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES			
TOLERANCES : ANGLES ±	——	MATERIAL :	——
3 PLACE DECIMALS (.XXX) ±	——		
2 PLACE DECIMALS (.XX) ±	——		
1 PLACE DECIMALS (.X) ±	——	FINISH :	——

NEXT ASSEMBLY	DWG. TYPE

PROJECT	VLA	F14 FE CONTROL INTERFACE	NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801
TITLE		F14 FE CONTROL INTERFACE SCHEMATIC DIAGRAM	DRAWN BY ANDREATTA — DATE 8-90
			DESIGNED BY KOSKI — DATE 8-90
			APPROVED BY — DATE
SHEET NUMBER	2 of 9	DRAWING NUMBER D13190S04	REV. — SCALE —

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

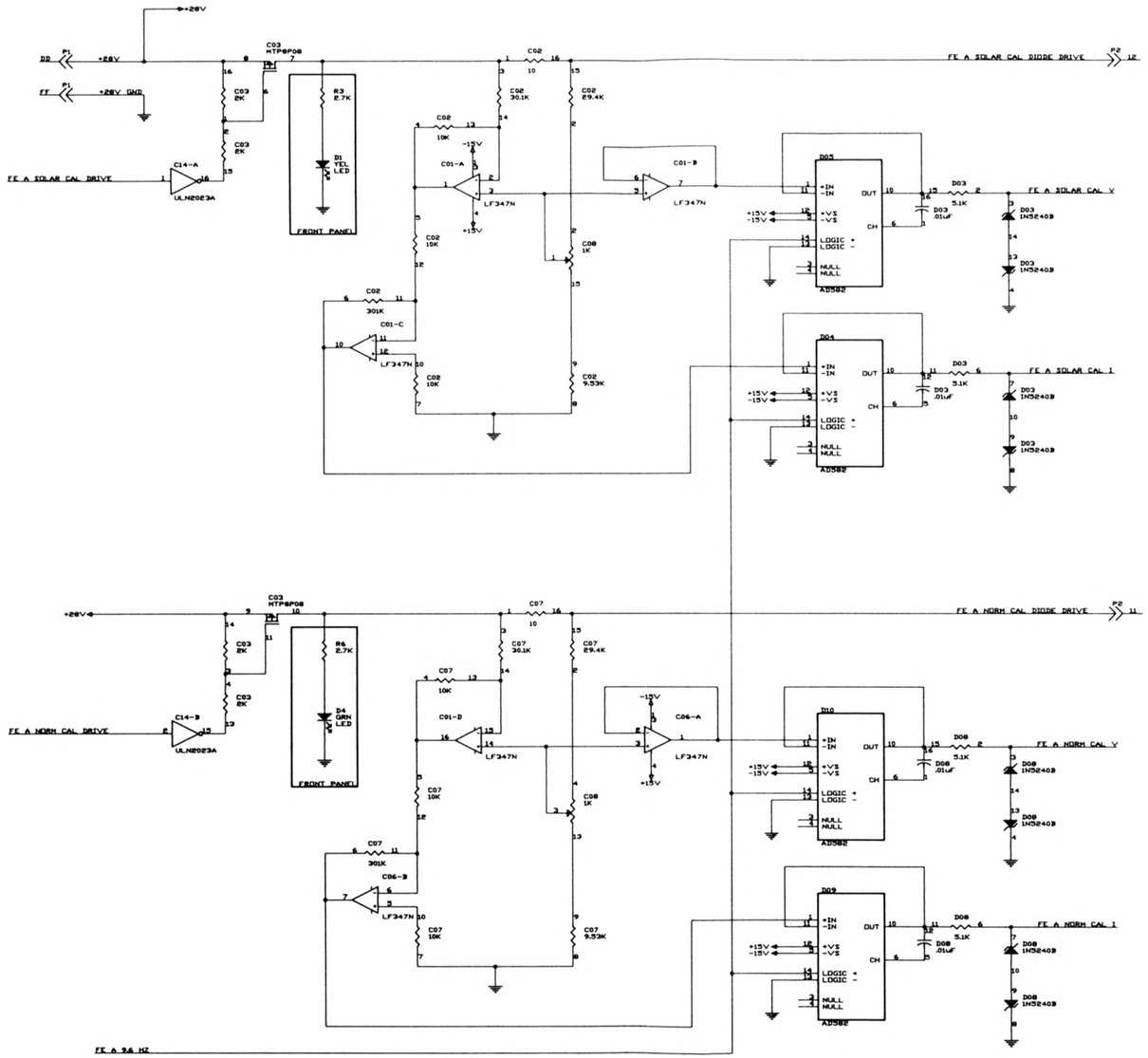




ACAD : F14SK-3

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	VLA PROJECT	F14 FE CONTROL INTERFACE	NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801
TOLERANCES : ANGLES ± ——	TITLE	F14 FE CONTROL INTERFACE SCHEMATIC DIAGRAM	DRAWN BY ANDREATTA DATE 8-90
3 PLACE DECIMALS (.000) ± ——			DESIGNED BY KOSKI DATE 8-90
2 PLACE DECIMALS (.00) ± ——			APPROVED BY DATE
1 PLACE DECIMALS (.0) ± ——			
MATERIAL : ——			
FINISH : ——			
NEXT ASSEMBLY / DWG. TYPE		SHEET NUMBER 3 of 9 / DRAWING NUMBER D13190S04	REV. / SCALE —

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION



NOTES:

1. CUT PIN 16 AT LOCATIONS C01, C02, C03, C06, C07, C14, D03, AND D08.
2. CUT PIN 8 AT LOCATIONS C03.

ACAD : F14SK-4

PROPERTY OF NRAO

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES : ANGLES ± —
3 PLACE DECIMALS (.000) ± —
2 PLACE DECIMALS (.00) ± —
1 PLACE DECIMALS (.0) ± —
MATERIAL : —
FINISH : —

NEXT ASSEMBLY | DWG. TYPE

VLA SCHEMATIC F14 FE CONTROL INTERFACE

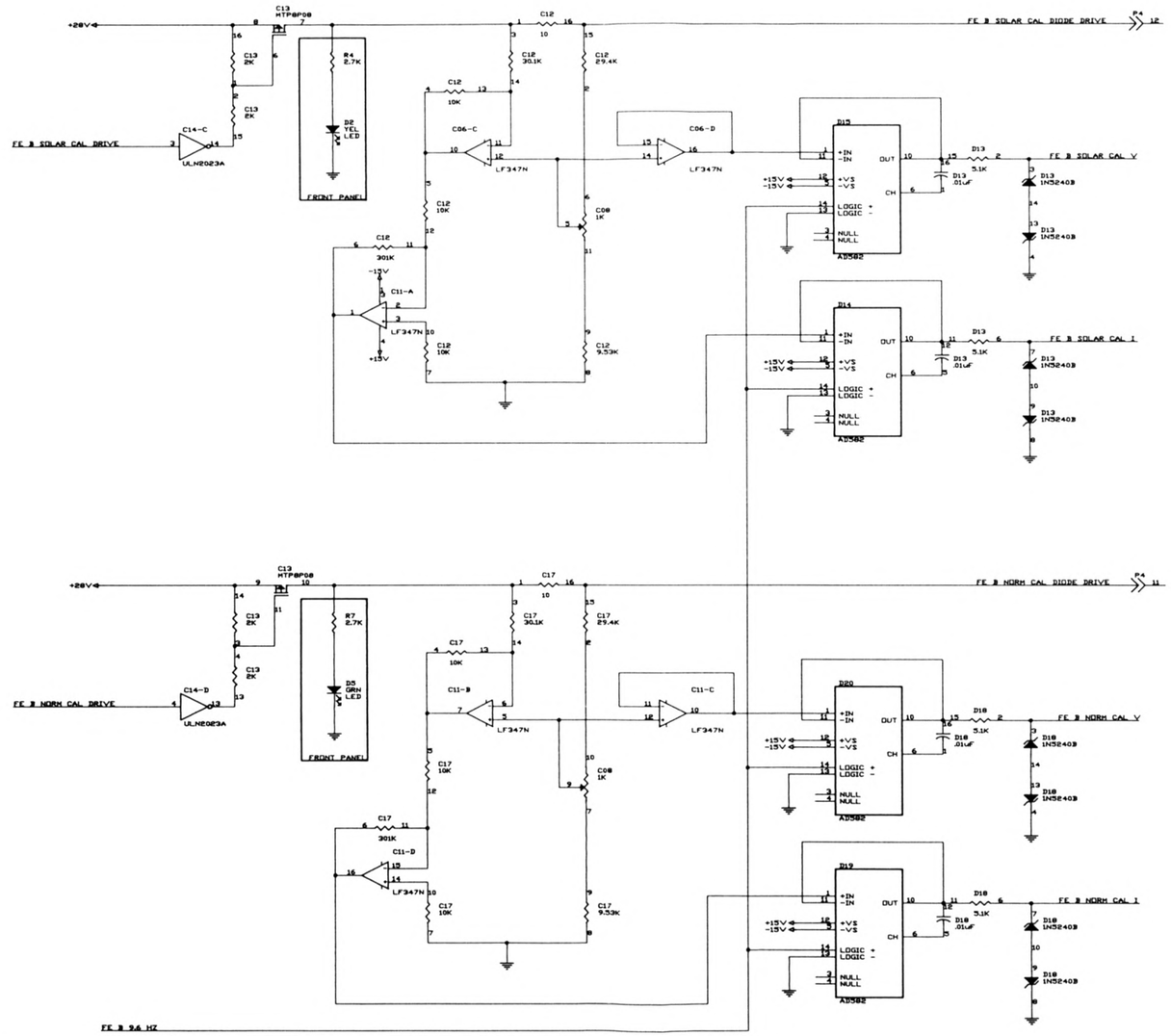
TITLE: F14 FE CONTROL INTERFACE SCHEMATIC DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY ANDREATTA	DATE 8-90	
DESIGNED BY KOSKI	DATE 8-90	
APPROVED BY	DATE	

SHEET NUMBER 4 of 9 | DRAWING NUMBER D13190S04 | REV. | SCALE —

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION



NOTES:

1. CUT PIN 16 AT LOCATIONS C11, C12, C13, C17, D13, D18.
2. CUT PIN 8 AT LOCATIONS C13.

ACAD : F14SK-5

NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES : ANGLES ± —
3 PLACE DECIMALS (.000) ± —
2 PLACE DECIMALS (.00) ± —
1 PLACE DECIMALS (.X) ± —
MATERIAL : —
FINISH : —

VLA SOCORRO

F14
FE CONTROL
INTERFACE

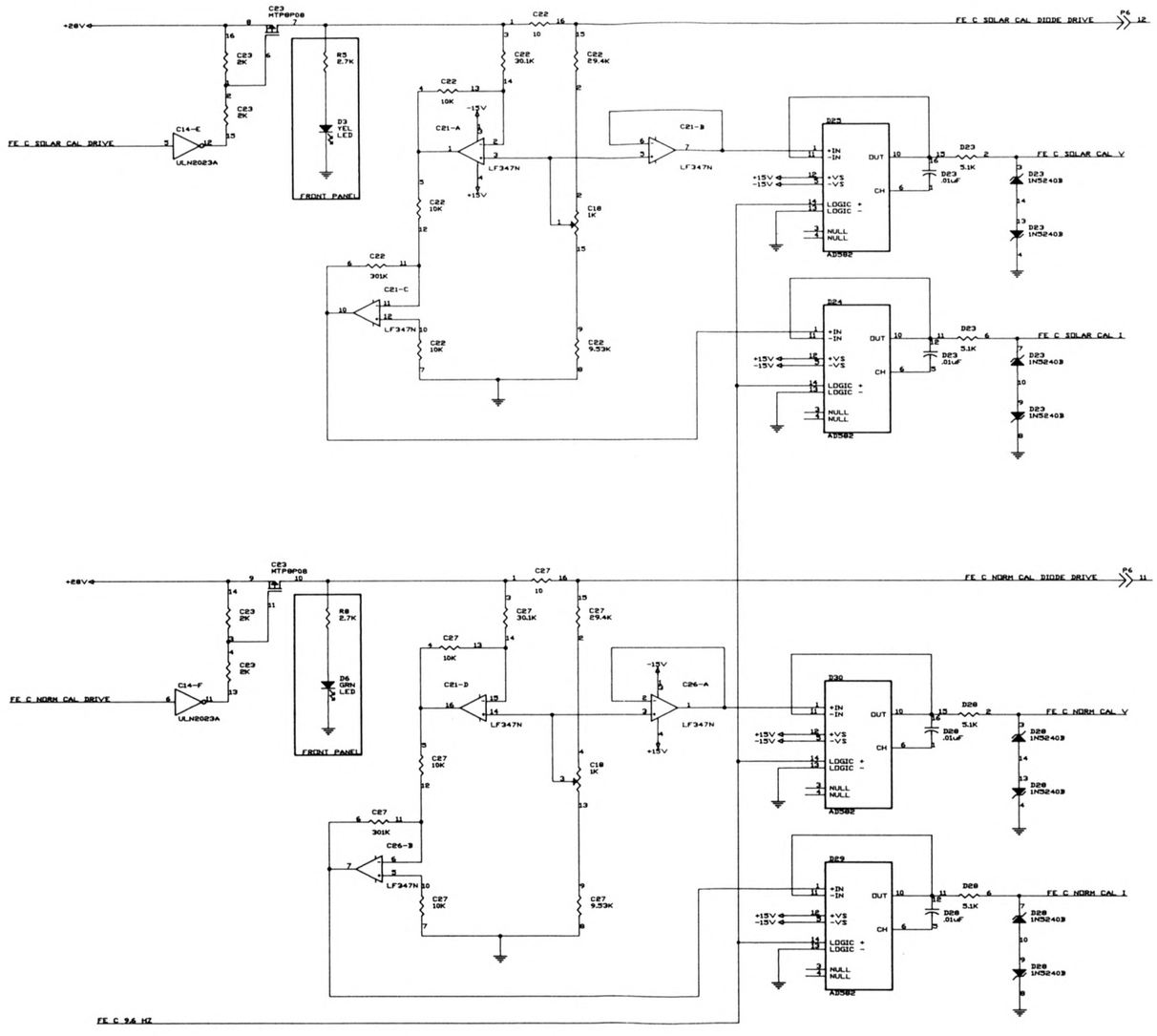
TITLE
F14
FE CONTROL INTERFACE
SCHEMATIC DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	ANDREATTA	DATE	8-90
DESIGNED BY	KOSKI	DATE	8-90
APPROVED BY		DATE	

SHEET NUMBER 5 of 9 | DRAWING NUMBER D13190S04 | REV. | SCALE —

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION



NOTES:

1. CUT PIN 16 AT LOCATIONS C21, C22, C23, C26, C27, D23, AND D28.
2. CUT PIN 8 AT LOCATIONS C23.

ACAD : F14SK-6

NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES : ANGLES ± ——
3 PLACE DECIMALS (.000) ± ——
2 PLACE DECIMALS (.00) ± ——
1 PLACE DECIMALS (.0) ± ——
MATERIAL : ——
FINISH : ——

VLA PROJECT: F14
FE CONTROL INTERFACE

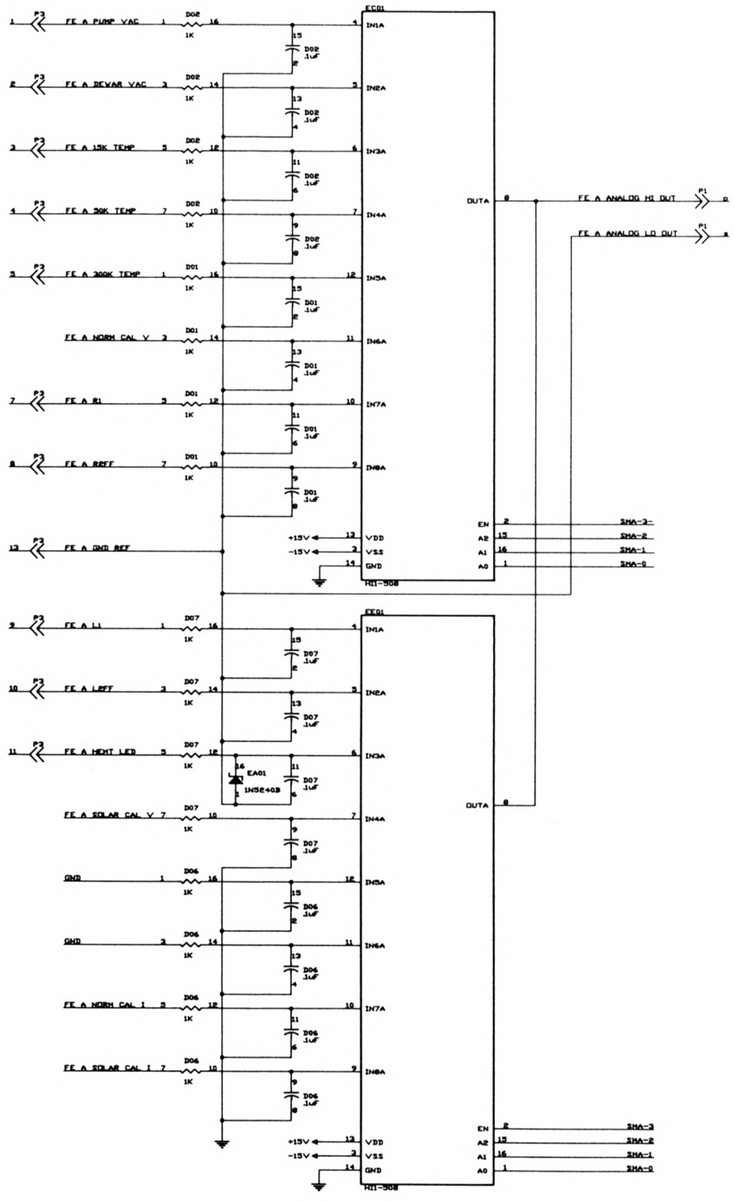
TITLE: F14
FE CONTROL INTERFACE
SCHEMATIC DIAGRAM

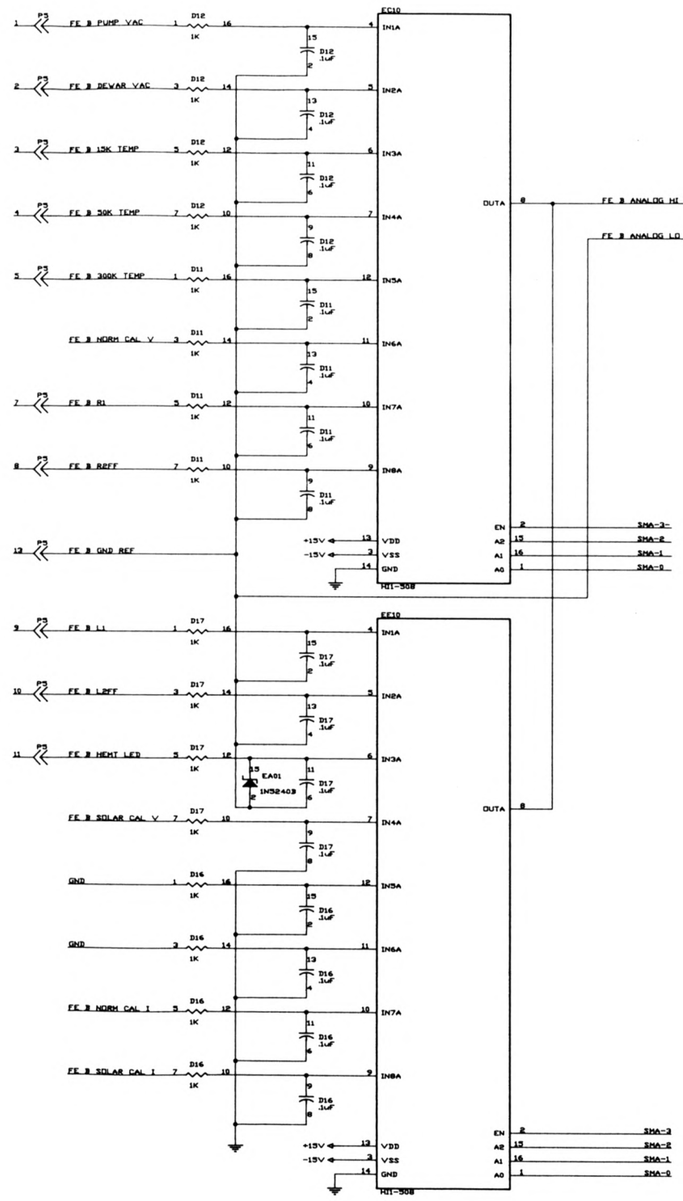
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE
ANDREATTA	8-90
DESIGNED BY	DATE
KOSKI	8-90
APPROVED BY	DATE

SHEET NUMBER 6 of 9 | DRAWING NUMBER D13190S04 | REV. | SCALE —

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION





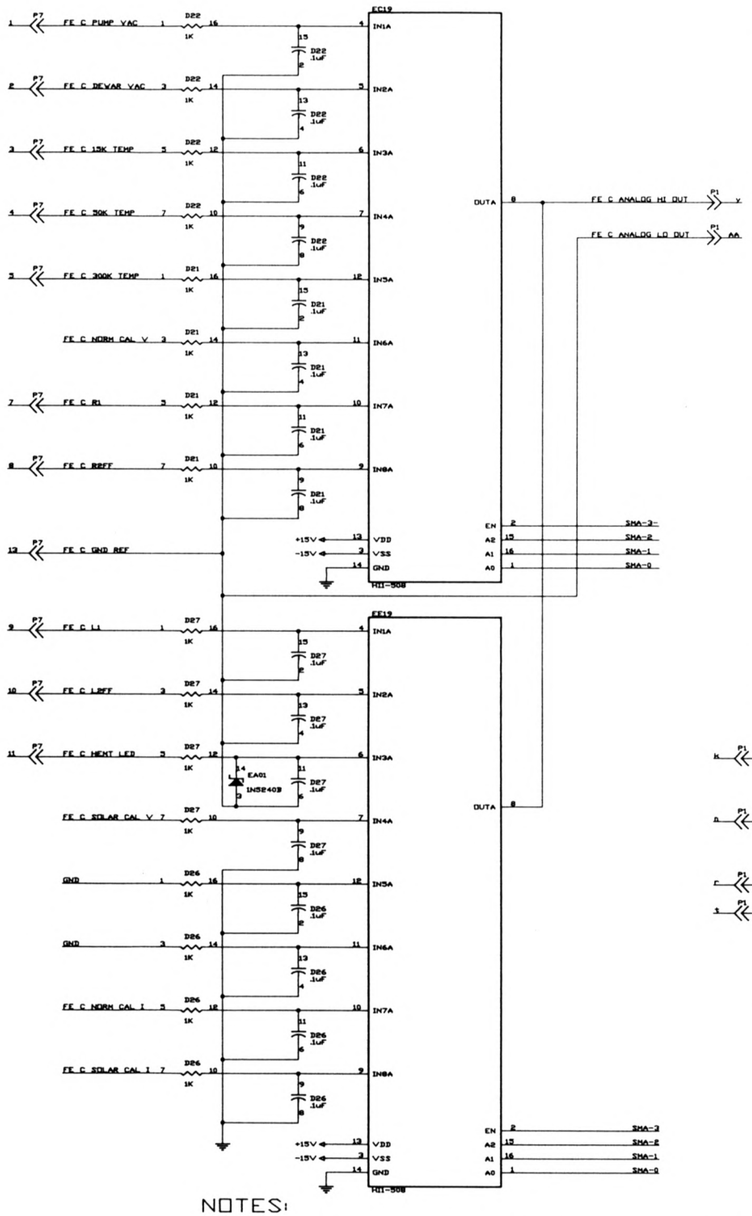
NOTES:

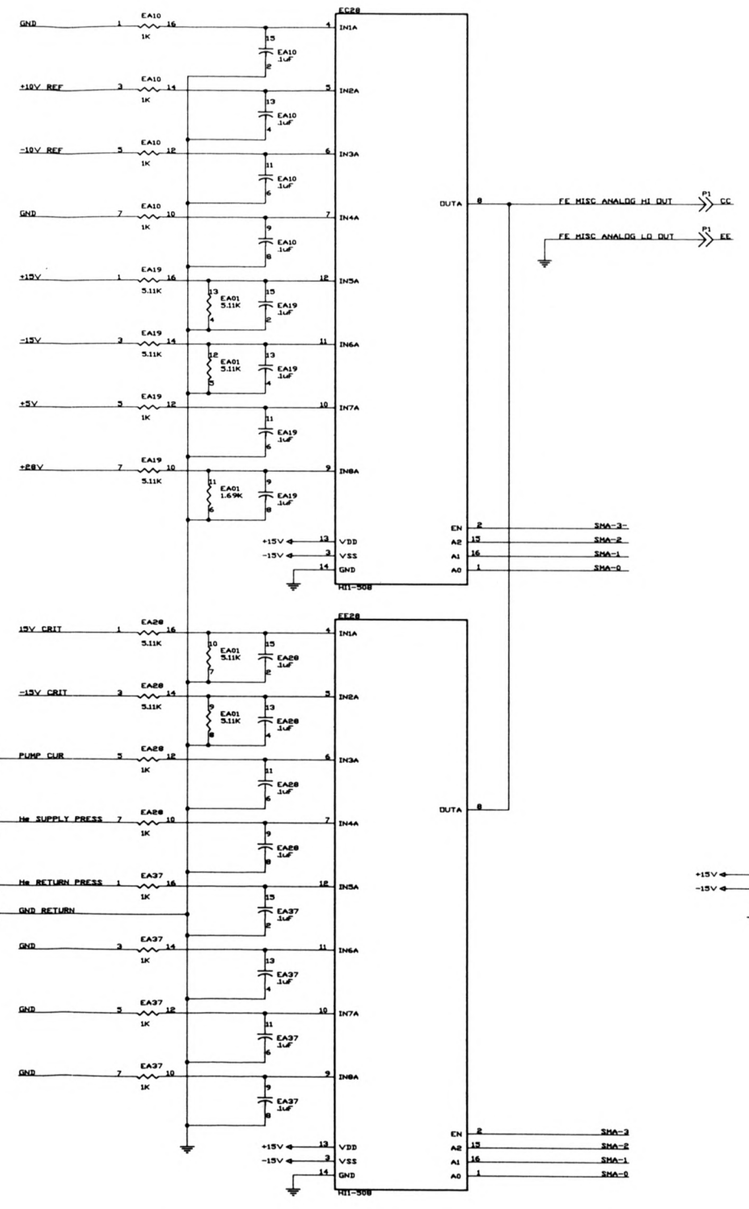
1. CUT PIN 16 AT LOCATIONS D01, D02, D06, D07, D11, D12, D16, AND D17.

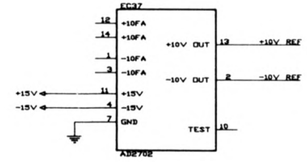
ACAD : F14SK-7

NEXT ASSEMBLY	DWG. TYPE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES : ANGLES ± 3 PLACE DECIMALS (.000) ± 2 PLACE DECIMALS (.00) ± 1 PLACE DECIMALS (.0) ± MATERIAL : FINISH :	VLA PROJECT	F14 FE CONTROL INTERFACE	NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801
			TITLE	F14 FE CONTROL INTERFACE SCHEMATIC DIAGRAM	DRAWN BY ANDREATTA — DATE 8-90 DESIGNED BY KOSKI — DATE 8-90 APPROVED BY — DATE
			SHEET NUMBER	7 of 9	DRAWING NUMBER D13190S04 — REV. — SCALE —

REV	DATE	DRAWN BY	APPR'D BY	DESCRIPTION







NOTES:

1. CUT PIN 16 AT LOCATIONS D21, D22, D26, AND D27.

ACAD : F14SK-8

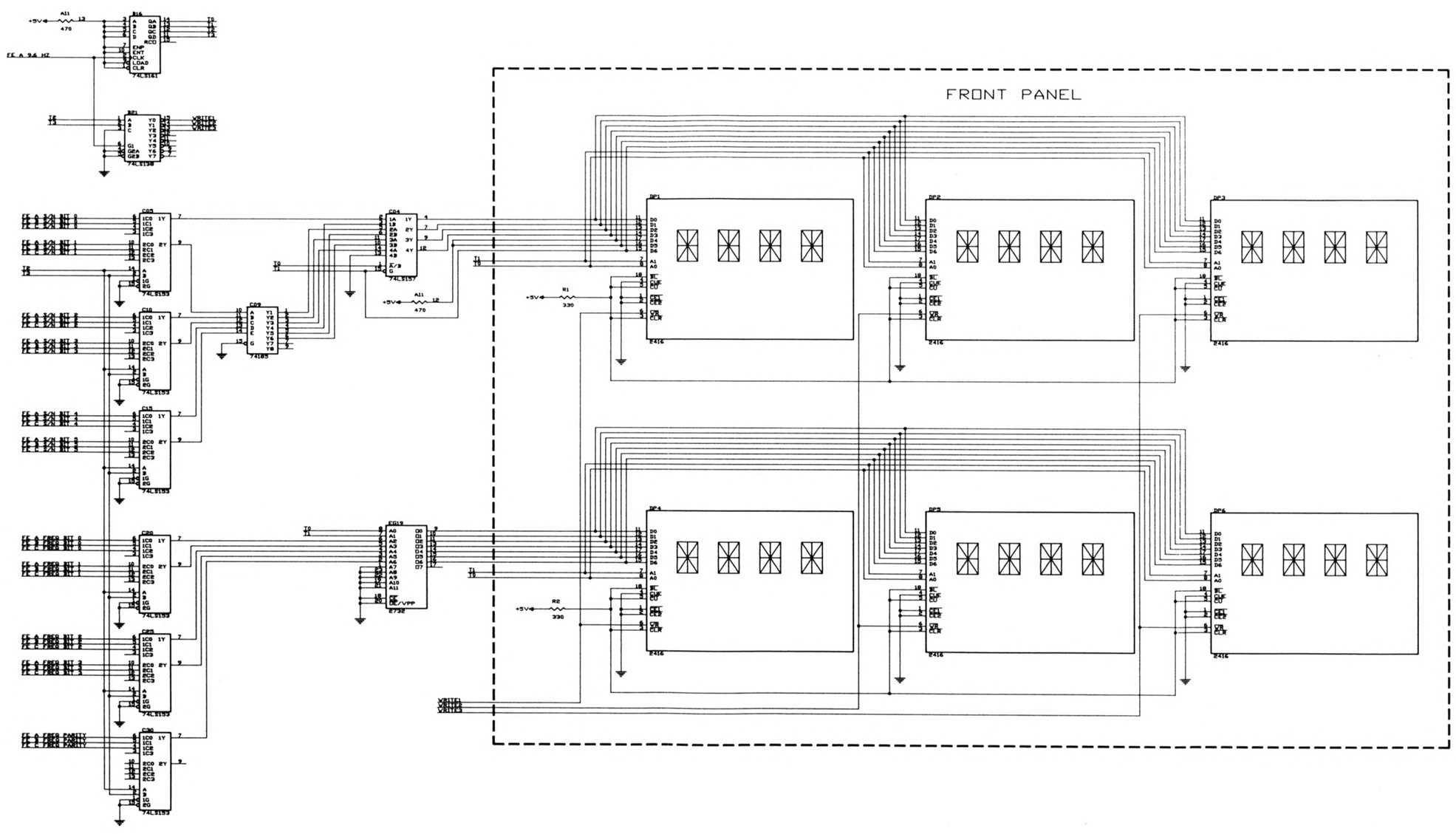
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	
TOLERANCES : ANGLES ±	—
3 PLACE DECIMALS (.000) ±	—
2 PLACE DECIMALS (.00) ±	—
1 PLACE DECIMALS (.0) ±	—
MATERIAL :	—
FINISH :	—
NEXT ASSEMBLY	DWG. TYPE

PROJECT	F14 FE CONTROL INTERFACE
TITLE	F14 FE CONTROL INTERFACE SCHEMATIC DIAGRAM
SHEET NUMBER	8 of 9
DRAWING NUMBER	D13190S04
REV.	
SCALE	—

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	ANDREATTA
DATE	8-90
DESIGNED BY	KOSKI
DATE	8-90
APPROVED BY	
DATE	

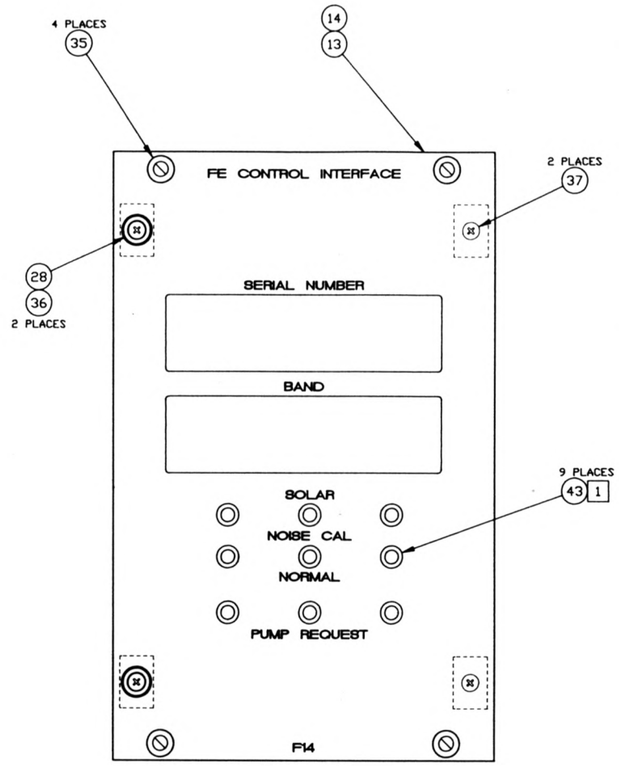
REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION



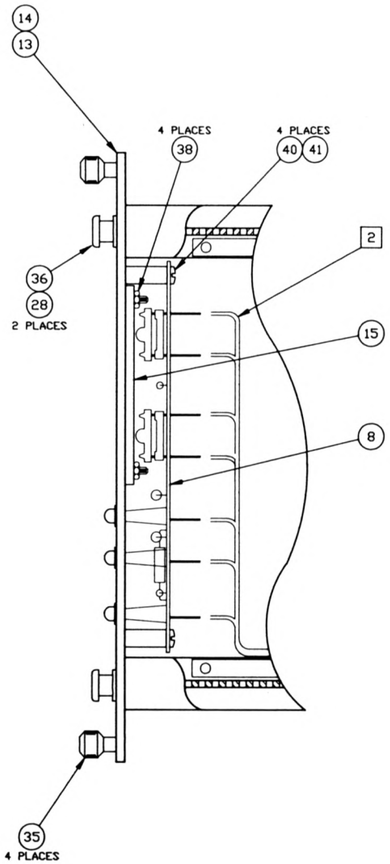
ACAD : F14SK-9

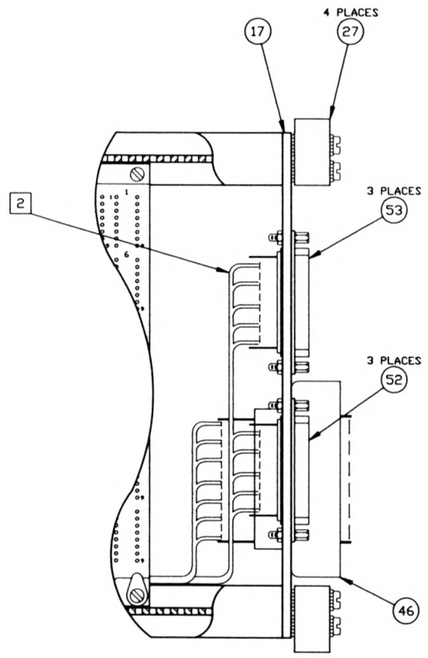
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	VLA PROJECT	F14 FE CONTROL INTERFACE	NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801
TOLERANCES: ANGLES ± —	TITLE	F14 FE CONTROL INTERFACE SCHEMATIC DIAGRAM	DRAWN BY ANDREATTA DATE 8-90
3 PLACE DECIMALS (.XXX) ± —			DESIGNED BY KISKI DATE 8-90
2 PLACE DECIMALS (.XX) ± —			APPROVED BY DATE
1 PLACE DECIMALS (.X) ± —			
MATERIAL : —			
FINISH : —			
NEXT ASSEMBLY	DWG. TYPE	SHEET NUMBER 9 of 9	DRAWING NUMBER D13190S04 REV. SCALE —

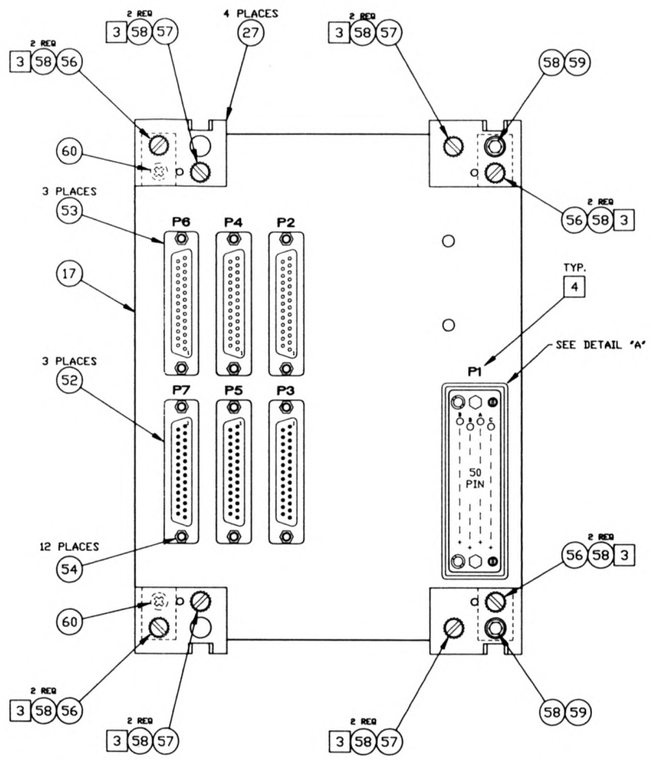
REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION



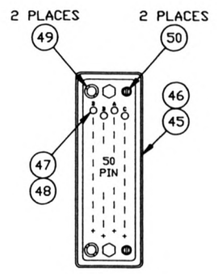
FRONT PANEL VIEW
SCALE 1/1







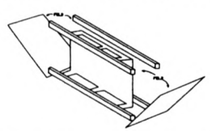
REAR PANEL VIEW
SCALE 1/1



DETAIL "A"
SCALE 1/1

NOTES :

1. SOLDER LED LEADS TO FRONT PANEL DISPLAY PCB (ITEM #8) AFTER INSTALLATION.
2. DRESS WIRE HARNESS PATH TO PERMIT FRONT AND REAR PANELS TO BE FOLDED OUTWARD FROM TOP. (SEE FIGURE)



3. WHERE TWO WASHERS (ITEM #58) ARE REQUIRED, PLACE ONE UNDER THE SCREW HEAD AND THE OTHER BETWEEN THE GUIDE BLOCK (ITEM #27) AND REAR PANEL (ITEM #17)
4. MARKING SHALL BE .125 HIGH, LEGIBLE AND PERMANANT, LOCATED APPROXIMATELY AS SHOWN.

ACAD : F14ASSY1

BOM - #A13190Z06

NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES : ANGLES ± —
3 PLACE DECIMALS (.000) ± .005
2 PLACE DECIMALS (.00) ± —
1 PLACE DECIMALS (.0) ± —
MATERIAL : —
FINISH : —

VLA PROJECT : F14 FE CONTROL INTERFACE

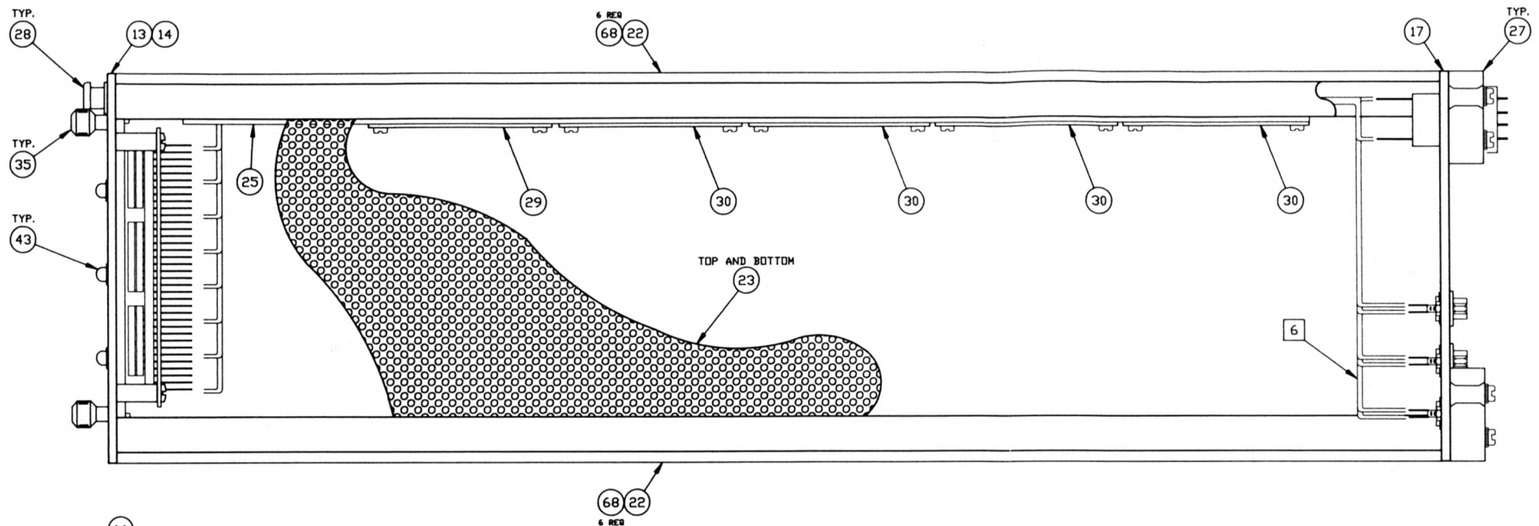
TITLE : F14 FE CONTROL INTERFACE MODULE ASSEMBLY

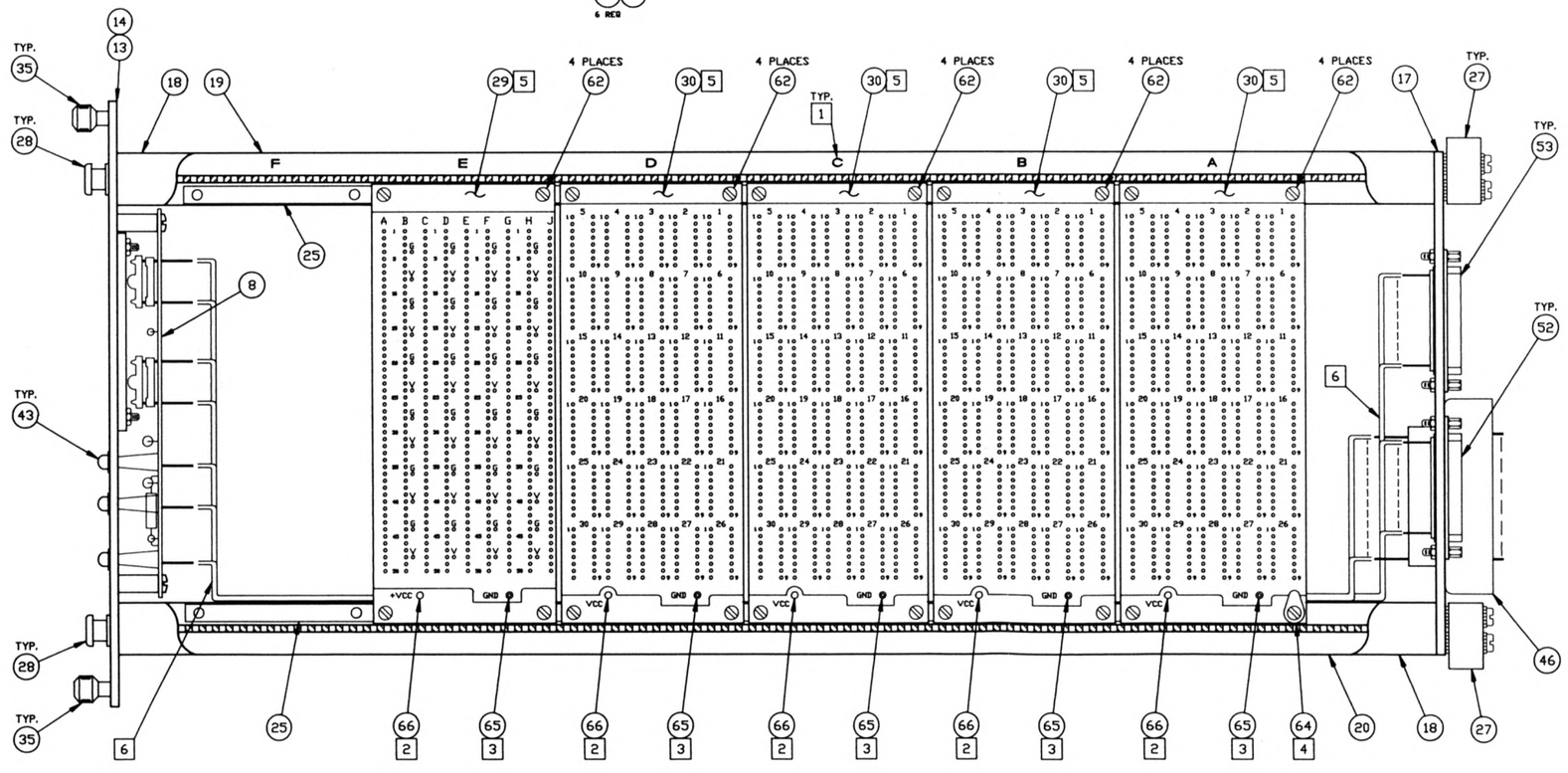
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE
ANDREATTA	9-90
DESIGNED BY	DATE
KOSKI	7-90
APPROVED BY	DATE

SHEET NUMBER 1 of 4 | DRAWING NUMBER D13190P10 | REV. | SCALE 1/1

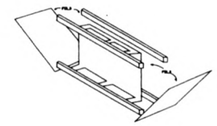
REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION





NOTES :

1. MARKING SHALL BE .125 HIGH, LEGIBLE AND PERMANENT, LOCATED APPROXIMATELY AS SHOWN.
2. SOLDER POWER TERMINAL (ITEM #66) TO POWER PLANE. (WIRE WRAP SIDE OF ITEM #29, AND #30)
3. SOLDER GND TERMINAL (ITEM #65) TO GROUND PLANE. (COMPONENT SIDE OF ITEM #29, AND #30)
4. SOLDER 'SOLDER LUG' (ITEM #64) TO GROUND PLANE AND PLACE UNDER SCREW HEAD AS SHOWN.
5. INSTALL IC'S INTO UNIVERSAL IC PANEL (ITEM #30) AND 16 X 32 IC PANEL (ITEM #29) USING DWG. #A13190P11.
6. DRESS WIRE HARNESS PATH TO PERMIT FRONT AND REAR PANELS TO BE FOLDED OUTWARD FROM TOP. (SEE FIGURE)



BOM - #A13190Z06

ACAD : F14ASSY2

NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES : ANGLES ± —
3 PLACE DECIMALS (.000) ± .005
2 PLACE DECIMALS (.00) ± —
1 PLACE DECIMALS (.0) ± —
MATERIAL : —
FINISH : —

VLA PRODUCT: F14 FE CONTROL INTERFACE

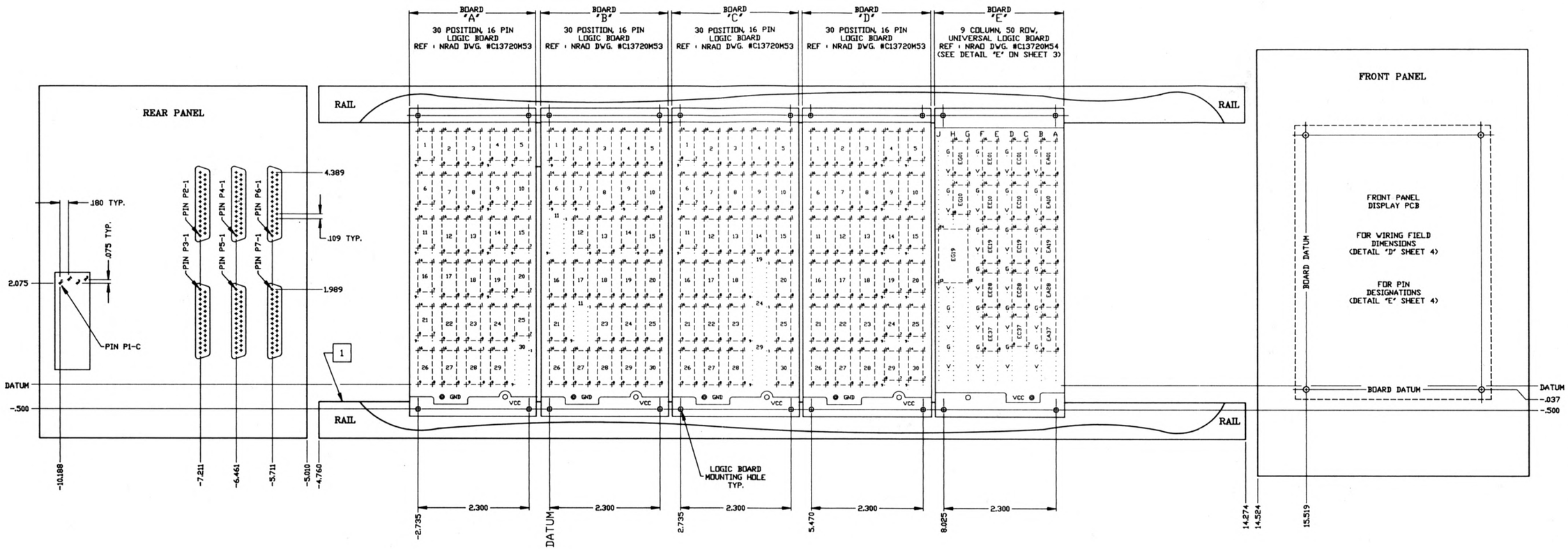
TITLE: F14 FE CONTROL INTERFACE MODULE ASSEMBLY

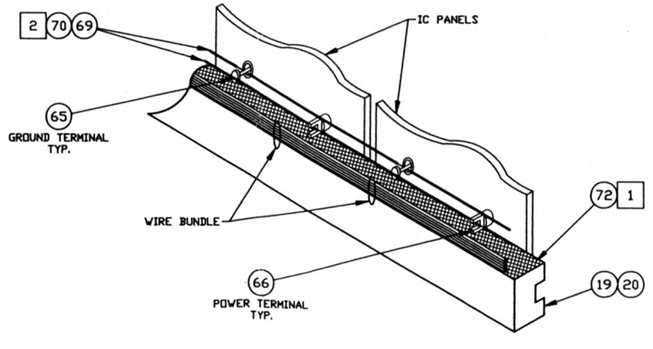
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY ANDREATTA	DATE 9-90
DESIGNED BY KOSKI	DATE 7-90
APPROVED BY	DATE

SHEET NUMBER 2 of 4 | DRAWING NUMBER D13190P10 | REV. | SCALE 1/1

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION





DETAIL "B"
SCALE 1/1

NOTES :

1. KAPTON TAPE (ITEM #72) SHALL RUN THE FULL LENGTH OF THE RAILS (ITEM #19 AND #20). SEE DETAIL 'B'.
2. POWER AND GROUND BUS WIRING SHALL BE ON THE WIRE WRAP SIDE OF THE UNIVERSAL IC PANEL AND THE 16 X 30 IC PANELS (ITEMS #29 AND #30).

ACAD : F14ASSY3

BOM - #A13190Z06

NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES : ANGLES ± —
3 PLACE DECIMALS (.000) ± .005
2 PLACE DECIMALS (.00) ± —
1 PLACE DECIMALS (.0) ± —
MATERIAL : —
FINISH : —

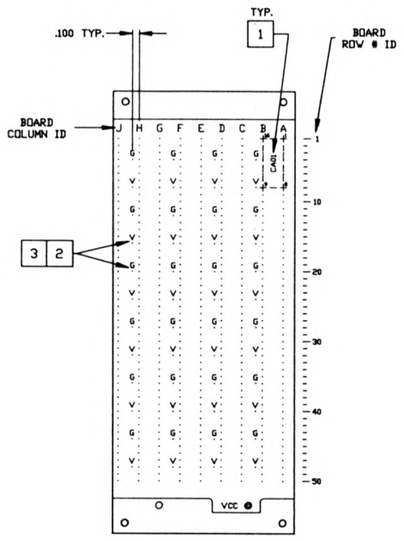
VLA PROJECT : F14 FE CONTROL INTERFACE

TITLE : F14 FE CONTROL INTERFACE MODULE ASSEMBLY

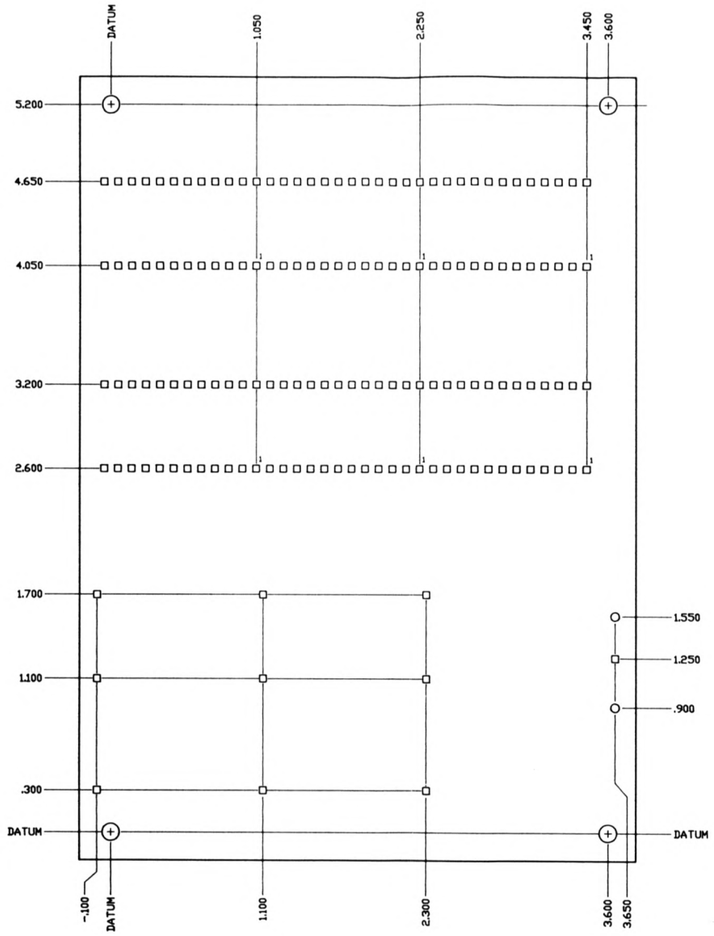
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY ANDREATTA	DATE 9-90
DESIGNED BY KOSKI	DATE 7-90
APPROVED BY	DATE
SHEET NUMBER 3 of 4	DRAWING NUMBER D13190P10
REV.	SCALE 1/1

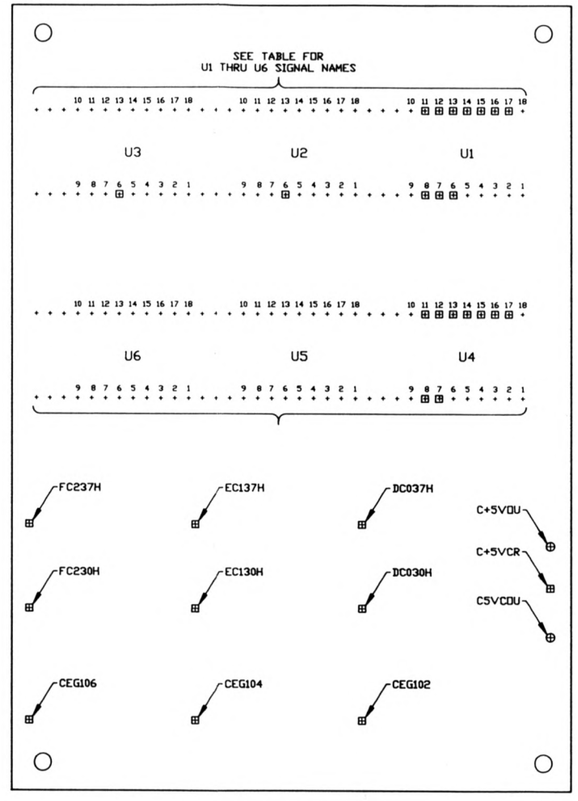
REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION



DETAIL "C"
SCALE 1/1



DETAIL "D"
SCALE 2/1



DETAIL "E"
SCALE 2/1

NOTES :

1. PIN #1 LOCATION ID = X X X X
   - ROW #
   - COLUMN
   - BOARD LOCATION
2. VCC AND GND PIN LOCATIONS FOR BOARD 'E' ARE AS FOLLOWES:
   COLUMNS B, D, F, AND H
   VCC PINS : 8, 16, 24, 32, 40, AND 48
   GND PINS : 4, 12, 20, 28, 36, AND 44
3. TYPICAL WIRE LIST VCC AND GND PIN LOCATION ID = X X XX - XX
   - PIN #
   - VD=VCC, GN=GND
   - COLUMN
   - BOARD LOCATION

O = POINT TO BE SOLDERED
□ = POINT TO BE WIRE WRAPPED

TABLE

PIN	SIGNAL	PIN	SIGNAL
U1-6	IB2115	U2-6	IB2114
U1-7	IG1907	U3-6	IB2113
U1-8	IG1908	U4-7	IG1907
U1-11	IC0404	U4-8	IG1908
U1-12	IC0407	U4-11	IG1909
U1-13	IC0409	U4-12	IG1910
U1-14	IC0412	U4-13	IG1911
U1-15	IG1907	U4-14	IG1913
U1-16	IA1112	U4-15	IG1916
U1-17	IA1112	U4-16	IG1915
		U4-17	IG1914

ACAD : F14ASSY4

BOM - #A13190Z06

NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES : ANGLES ± ——
3 PLACE DECIMALS (.000) ± .005
2 PLACE DECIMALS (.00) ± ——
1 PLACE DECIMALS (.X) ± ——
MATERIAL : ——
FINISH : ——

VLA SCIENTIFIC
F14
FE CONTROL INTERFACE

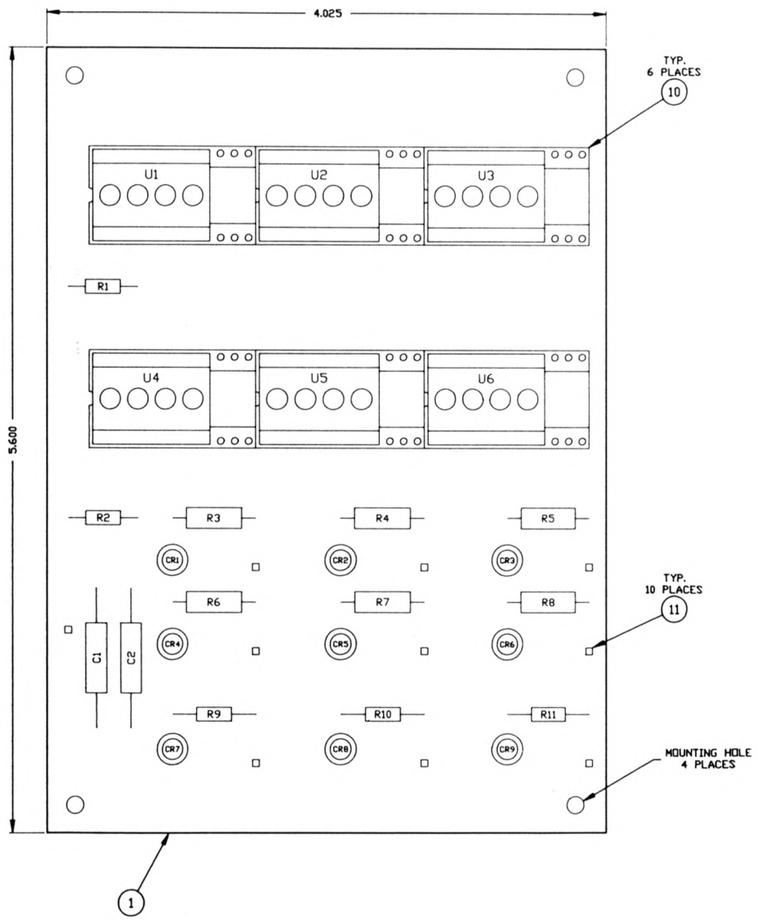
TITLE
F14
FE CONTROL INTERFACE
MODULE ASSEMBLY

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	ANDREATTA	DATE 9-90
DESIGNED BY	KISKI	DATE 7-90
APPROVED BY		DATE

SHEET NUMBER 4 of 4 | DRAWING NUMBER D13190P10 | REV. | SCALE 1/1

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION



ITEM #	REF. DES.	MANUFACTURE	PART NUMBER	DESCRIPTION	QTY.
1	———	NRAO	SEE NOTE #1	CIRCUIT BOARD	1
2	C1	SPRAGUE	150D226X9015B2	22uF, 15WVDC, CAPACITOR	1
3	C2	SPRAGUE	192P10392	.01uF, 200WVDC, CAPACITOR	1
4	CR1 - CR3	HEWLETT PACKARD	HLMP-3862	YELLOW LED LAMP	3
5	CR7 - CR9	HEWLETT PACKARD	HLMP-3762	RED LED LAMP	3
6	R1, R2	ALLEN BRADLY	RCR07CB102JS	1K OHM, 1/4W, 5%, RESISTOR	2
7	R3 - R8	ALLEN BRADLY	RCR20EB272JS	2.7K OHM, 1/2W, 5%, RESISTOR	6
8	R9 - R11	ALLEN BRADLY	RCR07CB331JS	330 OHM, 1/4W, 5%, RESISTOR	3
9	U1 - U6	HEWLETT PACKARD	HPDL-2416	SMART ALPHANUMERIC DISPLAY	6
10	———	AUGAT	524-10F	24 WW PIN IC SOCKET	6
11	———	AUGAT	814-17P2	WW PIN TERMINAL	10
12	CR4 - CR6	HEWLETT PACKARD	HLMP-0103	GREEN LED LAMP	3

NOTES :

1. ARTWORK = NRAO DWG. #C13190AB08
   DRILL DWG. = NRAO DWG. #C13190M08

SCHEMATIC	D13190S04
DRILL DWG.	C13190M08
ARTWORK	C13190AB08
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES : ANGLES ± ——
3 PLACE DECIMALS (.000) ± .005
2 PLACE DECIMALS (.00) ± ——
1 PLACE DECIMALS (.0) ± ——
MATERIAL : ———
FINISH : ———

PROJECT: VLA
F14 FRONT END CONTROL INTERFACE

TITLE: F14 FRONT END CONTROL INTERFACE FRONT PANEL DISPLAY PCB ASSEMBLY

SHEET NUMBER 1 of 1 | DRAWING NUMBER D13190P09 | REV. | SCALE 2/1

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY ANDREATTA	DATE 7-90
DESIGNED BY KOSKI	DATE 7-90
APPROVED BY	DATE

ACAD : F14FPASY
REF : VLA-09

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

ACAD : F14BOM

NEXT ASSEMBLY	DWG. TYPE

VLA PROJECT: F14 FE CONTROL INTERFACE

TITLE: F14 FE CONTROL INTERFACE ASSEMBLY BOM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY ANDREATTA	DATE 9-90
DESIGNED BY KOSKI	DATE 7-90
APPROVED BY	DATE

SHEET NUMBER	DRAWING NUMBER	REV.	SCALE
1 of 5	A13190Z06		—

NATIONAL RADIO ASTRONOMY OBSERVATORY

PO BOX 0
SOCORRO, N.M. 87801

DWG # A13190Z06 REV ____ SHEET 2 of 5

ITEM #	REF DES	MANUFACTURER	MFG PART #	DESCRIPTION	QTY
1	---	NRAO	D13190P10	F14 ASSEMBLY DWG.	---
2	---	NRAO	A13190Z06	F14 ASSEMBLY BOM	---
3	---	NRAO	A13190W01	F14 WIRE LIST (MASTER)	---
4	---	NRAO	A13190W04	F14 WIRE LIST (HAND)	---
5	---	NRAO	A13190W05	F14 WIRE LIST (MACHINE)	---
6	---	NRAO	D13190S04	F14 SCHEMATIC DIAGRAM	---
7					
8	---	NRAO	D13190P09	F14 FRONT PANEL DISPLAY PCB	1
9					
10	---	NRAO	A13190P11	F14 IC LOCATION DIAGRAM	---
11	---	NRAO	A13190P12	F14 DIP HEADER ASSEMBLY	---
12					
13	---	NRAO	C13190AB07	F14 FRONT PANEL	1
14	---	NRAO	D13190AB09	F14 FRONT PANEL SILKSCREEN	---
15	---	NRAO	B13190M10	F14 FRONT PANEL FILTER	1
16					
17	---	NRAO	C13190M06	F14 REAR PANEL	1
18	---	NRAO	B13050M03	MODULE MOUNTING RAILS	2
19	---	NRAO	C13720M15-1	UPPER IC MOUNTING RAILS	1
20	---	NRAO	C13720M15-2	LOWER IC MOUNTING RAILS	1

NATIONAL RADIO ASTRONOMY OBSERVATORY
PO BOX 0
SOCORRO, N.M. 87801

DWG # A13190Z06 REV ____ SHEET 3 of 5

ITEM #	REF DES	MANUFACTURER	MFG PART #	DESCRIPTION	QTY
21					
22	---	NRAO	B13050M18	RIGHT AND LEFT SIDE PLATES	2
23	---	NRAO	C13050M22-3	4 WIDE PERFORATED COVER	2
24					
25	---	NRAO	C13740M45	RAIL INSULATING SPACER	2
26					
27	---	NRAO	B13050M04	MODULE GUIDE BLOCK	4
28	---	NRAO	C13050M70	MODULE PULLER KNOB	2
29	---	NRAO	C13720M53	16 PIN X 30 LOGIC BOARD	4
30	---	NRAO	C13720M54	UNIVERSAL LOGIC BOARD	1
31					
32					
33					
34					
35	---	SOUTHCO	47-10-204-10	CAPTIVE THUMB SCREW	4
36	---	-----	#6-32 X .75"	FH PHP SS SCREW	2
37	---	-----	#6-32 X .50"	FH PHP SS SCREW	2
38	---	-----	#4-40	SS HEX NUT	4
39					
40	---	HH SMITH	8681	#4-40 X .25 OD X .687 PHENOLIC SPACER	4

NATIONAL RADIO ASTRONOMY OBSERVATORY

PO BOX 0
SOCORRO, N.M. 87801

DWG # A13190Z06 REV ____ SHEET 4 of 5

ITEM #	REF DES	MANUFACTURER	MFG PART #	DESCRIPTION	QTY
41	---	-----	#4-40 X .25"	NYLON SCREW	4
42					
43	---	HEWLWTT PACKARD	HLMP-0103	1 3/4 LAMP MOUNTING CLIP	9
44					
45	---	AMP	201358-3	50 PIN CONNECTOR BLOCK	1
46	---	AMP	202394-2	50 PIN CONNECTOR SHIELD	1
47	---	AMP	204219-1	#16 WIRE CRIMP PIN	6
48	---	AMP	601488-1	.025 WIRE WRAP POST	44
49	---	AMP	203964-6	GUIDE SOCKET	2
50	---	AMP	200833-4	GUIDE PIN	2
51					
52	---	AMPHENOL	DB25P-F179	25 PIN MALE D-CONNECTOR	3
53	---	AMPHENOL	DB25S-F179	25 PIN FEMALE D-CONNECTOR	3
54	---	KEYSTONE	7231	D-CONNECTOR MOUNTING JACKS	12
55					
56	---	-----	#6-32 X 1"	BH SS SCREW	4
57	---	-----	#6-32 X .75"	BH SS SCREW	4
58	---	-----	#6	SS EXTERIOR TOOTH LOCKWASHER	18
59	---	-----	#6-32 X .500"	SCH SS CAP SCREW	2
60	---	-----	#6-32 X .375"	FH PHP SS SCREW	2

NATIONAL RADIO ASTRONOMY OBSERVATORY

PO BOX 0
SOCORRO, N.M. 87801

DWG # A13190Z06 REV ____ SHEET 5 of 5

ITEM #	REF DES	MANUFACTURER	MFG PART #	DESCRIPTION	QTY
61					
62	---	------	#4-40 X .50"	BH SS SCREW	20
63					
64	---	GC ELECTRONICS	13-280-C	SOLDER LUG	1
65	---	HH SMITH	2025-D	TERMINAL (THRU TURRET)	5
66	---	HH SMITH	2010-D	TERMINAL (SPLIT)	5
67					
68	---	------	#6-32 X .25"	FH SS SCREW	12
69	---	ALPHA	286	BUSS BAR TINNED #14 AWG COPPER	---
70	---	ALPHA	TFT-200-13-NAT	TEFLON EXTRUDED TUBING	---
71					
72	---	CONN HARD RUBBER	TYPE K350	KAPTON TEMP-R TAPE .50" WIDE	---
73					
74					
75					
76					
77					
78					
79					
80					

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

ACAD : F14ICLOC

A13190Z06	BOM
D13190P10	ASSEMBLY
NEXT ASSEMBLY	DWG. TYPE

VLA PROJECT: F14 FE CONTROL INTERFACE

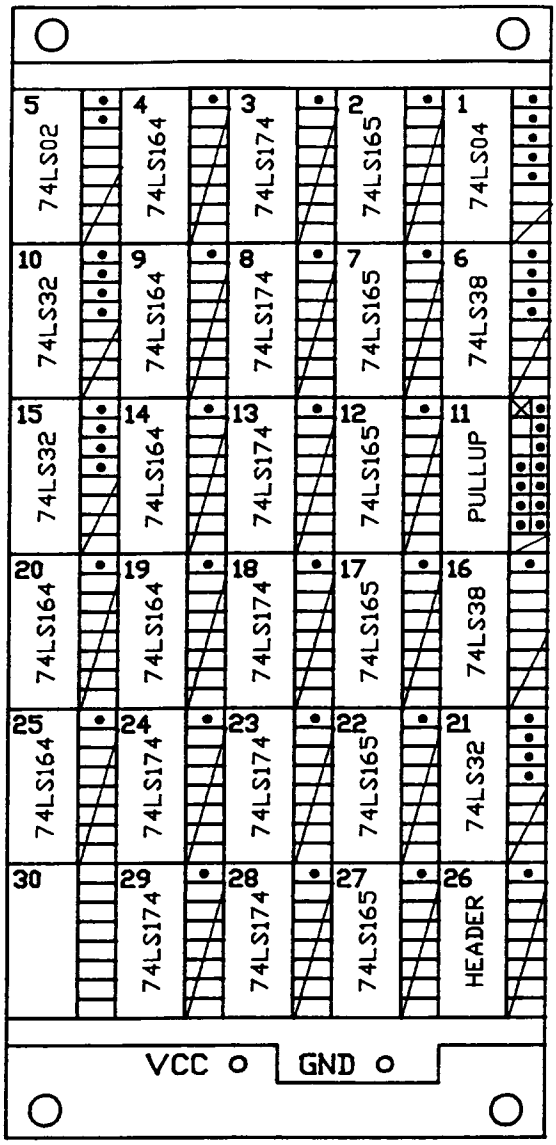
TITLE: F14 FE CONTROL INTERFACE IC LOCATION DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY: ANDREATTA	DATE: 9-90
DESIGNED BY: KOSKI	DATE: 9-90
APPROVED BY	DATE

SHEET NUMBER	DRAWING NUMBER	REV.	SCALE
1 of 6	A13190P11		—

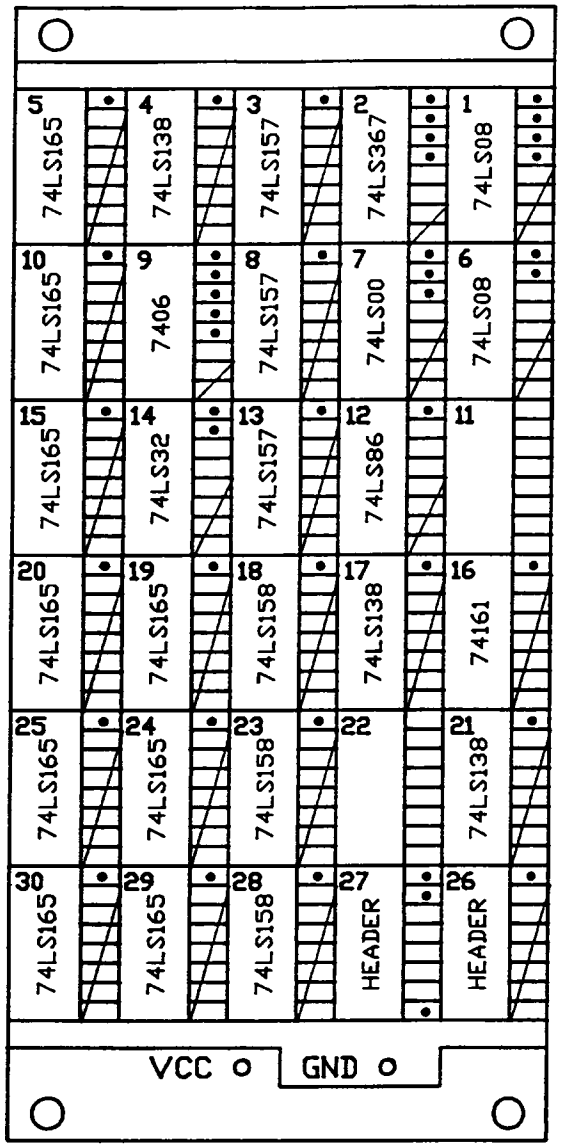
LOCATION A



SPECIAL SUB-ASSY'S

ITEM #	DWG #	SHT #
A26	A13190P12	2

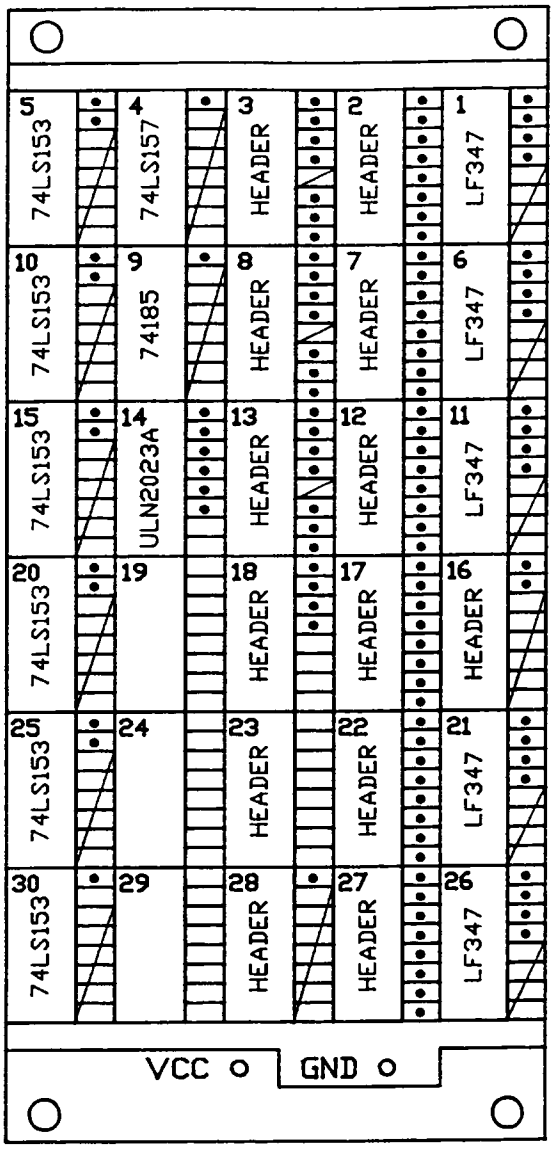
LOCATION B



SPECIAL SUB-ASSY'S

ITEM #	DWG #	SHT #
B26	A13190P12	2
B27	A13190P12	3

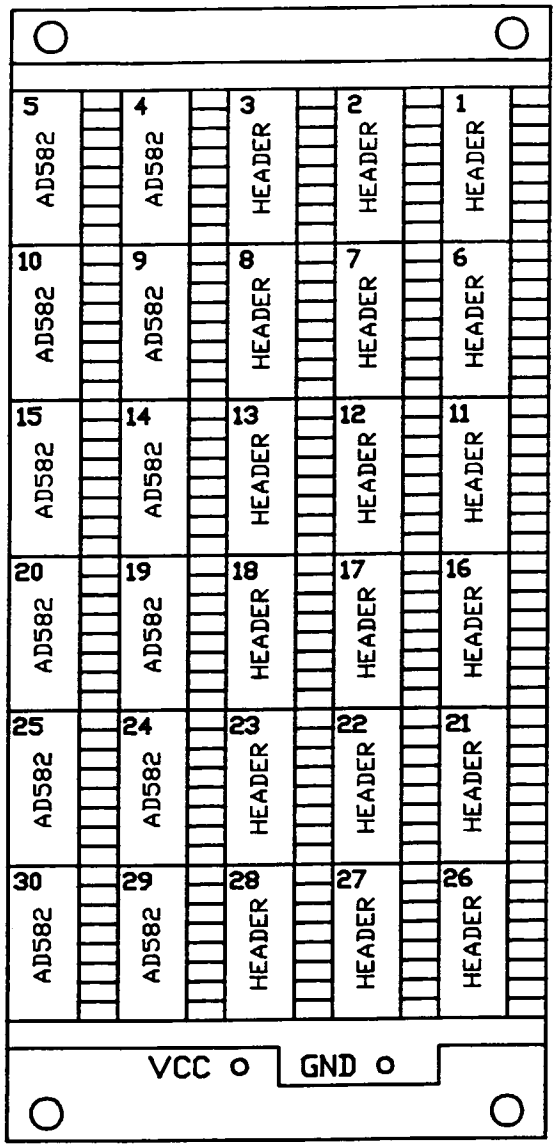
LOCATION C



SPECIAL SUB-ASSY'S

ITEM #	DWG #	SHT #
C2,C7,C12	A13190P12	4
C17,C22,C27	A13190P12	4
C3,C13,C23	A13190P12	5
C16	A13190P12	6
C8	A13190P12	7
C18	A13190P12	8
C28	A13190P12	2

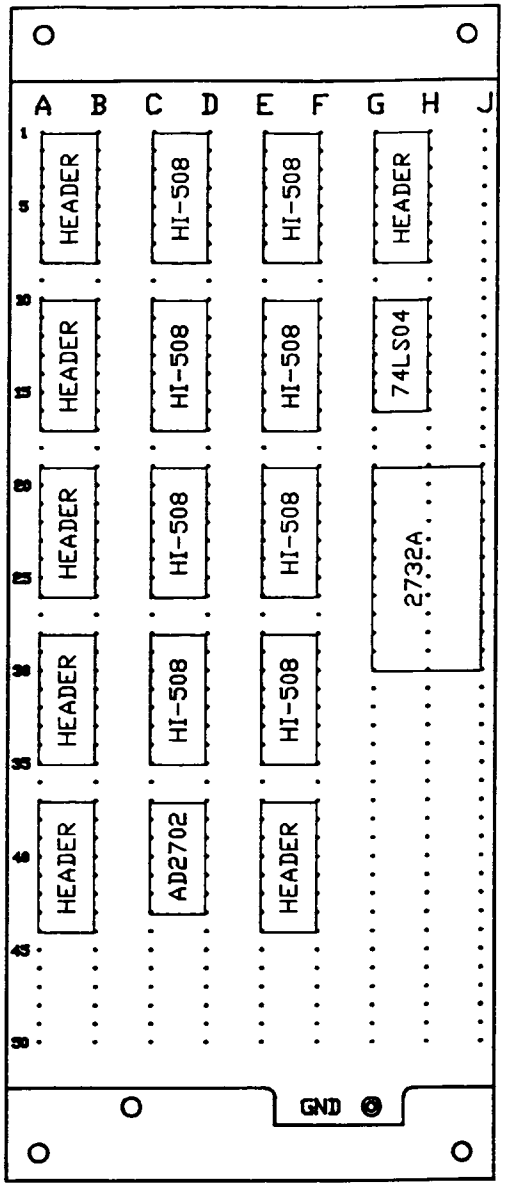
LOCATION D



SPECIAL SUB-ASSY'S

ITEM #	DWG #	SHT #
D1, D2	A13190P12	9
D6, D7	A13190P12	9
D11, D12	A13190P12	9
D16, D17	A13190P12	9
D21, D22	A13190P12	9
D26, D27	A13190P12	9
D3,D8,D13	A13190P12	10
D18,D23,D28	A13190P12	10

LOCATION E



SPECIAL SUB-ASSY'S

ITEM #	DWG #	SHT #
EA01	A13190P12	11
EA10, EA37	A13190P12	9
EA19	A13190P12	12
EA28	A13190P12	13
EE37	A13190P12	2
EG01	A13190P12	14

DWG. NO.	A13190P11	SHT. NO.	6 of 6	REV.

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

ACAD : F14DIPHD

NEXT ASSEMBLY	DWG. TYPE

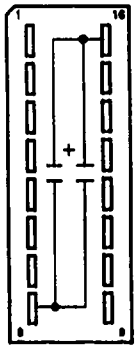
VLA PROJECT: F14 FE CONTROL INTERFACE

TITLE: F14 FE CONTROL INTERFACE DIP HEADER ASSEMBLY

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY ANDREATTA	DATE 9-90
DESIGNED BY KOSKI	DATE 7-90
APPROVED BY	DATE

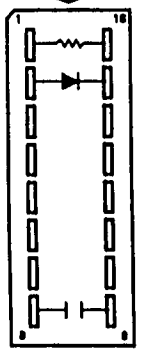
SHEET NUMBER 1 of 14	DRAWING NUMBER A13190P12	REV.	SCALE —



DESCRITION	VALUE	MFG	MFG PART #
DIP HEADER			
CAPACITOR, TANTALUM	22 uF, 15 WVDC	SPRAGUE	150D226X9015B2
CAPACITOR, POLYESTER	.01 uF, 200 VDC	SPRAGUE	192P10392

MODULE F14 FE CONTROL INTERFACE

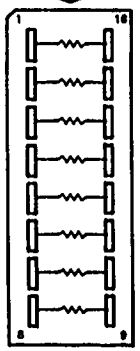
BOARD LOCATION A26, B26, C28, EE37



DESCRITION	VALUE	MFG	MFG PART #
DIP HEADER			
RESISTOR	1K OHM, 5%	ALLEN BRADLEY	RCR07CB10215
DIODE	1N914	MOTOROLA	
CAPACITOR, TANTALUM	22 uF, 16 WVDC	SPRAGUE	199D226X0016DA1

MODULE F14 FE CONTROL INTERFACE

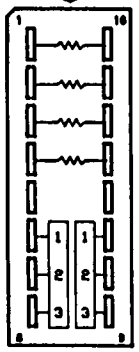
BOARD LOCATION B27



DESCRITION	VALUE	MFG	MFG PART #
DIP HEADER			
RESISTOR	10 OHM, 1%	DALE	RN60D10R0F
RESISTOR	29.4K OHM, 1%	DALE	RN55D2942F
RESISTOR	30.1K OHM, 1%	DALE	RN55D3012F
RESISTOR	10K OHM, 1%	DALE	RN55D1002F
RESISTOR	10K OHM, 1%	DALE	RN55D1002F
RESISTOR	301K OHM, 1%	DALE	RN55D3013F
RESISTOR	10K OHM, 1%	DALE	RN55D1002RF
RESISTOR	9530 OHM, 1%	DALE	RN55D9531F

MODULE F14 FE CONTROL INTERFACE

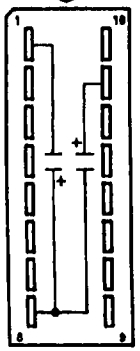
BOARD LOCATION C2, C7, C12, C17, C22, C27



DESCRITION	VALUE	MFG	MFG PART #
DIP HEADER			
RESISTOR	2K OHM, 5%	ALLEN BRADLEY	RCR07CB202JS
RESISTOR	2K OHM, 5%	ALLEN BRADLEY	RCR07CB202JS
RESISTOR	2K OHM, 5%	ALLEN BRADLEY	RCR07CB202JS
RESISTOR	2K OHM, 5%	ALLEN BRADLEY	RCR07CB202JS
MOSFET, POWER	P CHANNEL MOSFET	MOTOROLA	MTP8P08
MOSFET, POWER	P CHANNEL MOSFET	MOTOROLA	MTP8P08

MODULE F14 FE CONTROL INTERFACE

BOARD LOCATION C3, C13, C23

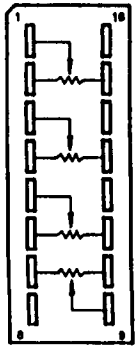


DESCRITION	VALUE	MFG	MFG PART #
DIP HEADER			
CAPACITOR	22 uF, 15 WVDC	SPRAGUE	150D226X9015B2
CAPACITOR	22 uF, 15 WVDC	SPRAGUE	150D226X9015B2

MODULE F14 FE CONTROL INTERFACE

BOARD LOCATION C16

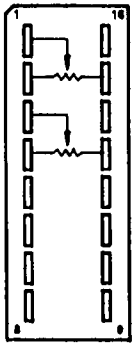
DWG. NO.	A13190P12	SHT. NO.	6 of 14	REV.



DESCRITION	VALUE	MFG	MFG PART #
DIP HEADER			
TRIMMING POT	1K OHM	BOURNS	3262W-102
TRIMMING POT	1K OHM	BOURNS	3262W-102
TRIMMING POT	1K OHM	BOURNS	3262W-102
TRIMMING POT	1K OHM	BOURNS	3262W-102

MODULE F14 FE CONTROL INTERFACE

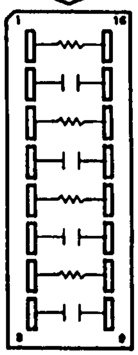
BOARD LOCATION C8



DESCRITION	VALUE	MFG	MFG PART #
DIP HEADER			
TRIMMING POT	1K OHM	BOURNS	3262W-102
TRIMMING POT	1K OHM	BOURNS	3262W-102

MODULE F14 FE CONTROL INTERFACE

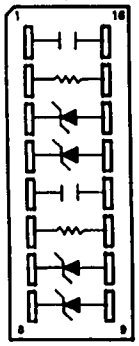
BOARD LOCATION C18



DESCRITION	VALUE	MFG	MFG PART #
DIP HEADER			
RESISTOR	1K OHM, 5%	ALLEN BRADLEY	RCR07CB102JS
CAPACITOR	.1 uF	SPRAGUE	IC20Z5U104M050B
RESISTOR	1K OHM, 5%	ALLEN BRADLEY	RCR07CB102JS
CAPACITOR	.1 uF	SPRAGUE	IC20Z5U104M050B
RESISTOR	1K OHM, 5%	ALLEN BRADLEY	RCR07CB102JS
CAPACITOR	.1 uF	SPRAGUE	IC20Z5U104M050B
RESISTOR	1K OHM, 5%	ALLEN BRADLEY	RCR07CB102JS
CAPACITOR	.1 uF	SPRAGUE	IC20Z5U104M050B

MODULE F14 FE CONTROL INTERFACE

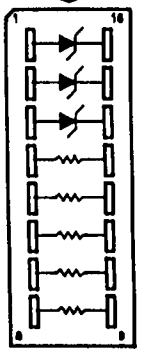
BOARD LOCATION D1, D2, D6, D7, D11, D12, D16, D17, D21, D22, D26, D27, EA10, EA37



DESCRITION	VALUE	MFG	MFG PART #
DIP HEADER			
CAPACITOR, POLYESTER	.01 uF	MALLORY	168103J100A
RESISTOR	5.1K OHM, 5%	ALLEN BRADLEY	RCR07CB512JS
DIODE	10V ZENER	MOTOROLA	1N5240B
DIODE	10V ZENER	MOTOROLA	1N5240B
CAPACITOR, POLYESTER	.01 uF	MALLORY	168103J100A
RESISTOR	5.1K OHM, 5%	ALLEN BRADLEY	RCR07CB512JS
DIODE	10V ZENER	MOTOROLA	1N5240B
DIODE	10V ZENER	MOTOROLA	1N5240B

MODULE F14 FE CONTROL INTERFACE

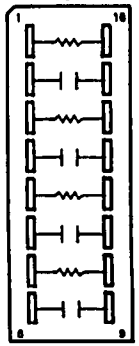
BOARD LOCATION D3, D8, D13, D18, D23, D28



DESCRITION	VALUE	MFG	MFG PART #
DIP HEADER			
DIODE	10V ZENER	MOTOROLA	1N5240B
DIODE	10V ZENER	MOTOROLA	1N5240B
DIODE	10V ZENER	MOTOROLA	1N5240B
RESISTOR	5.11K OHM, 1%	DALE	RN55D5111F
RESISTOR	5.11K OHM, 1%	DALE	RN55D5111F
RESISTOR	1.69K OHM, 1%	DALE	RN55D1691F
RESISTOR	5.11K OHM, 1%	DALE	RN55D5111F
RESISTOR	5.11K OHM, 1%	DALE	RN55D5111F

MODULE F14 FE CONTROL INTERFACE

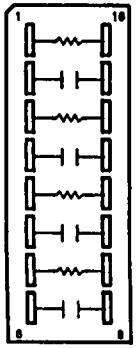
BOARD LOCATION EA01



DESCRITION	VALUE	MFG	MFG PART #
DIP HEADER			
RESISTOR	5.11K OHM, 1%	DALE	RN55D5111F
CAPACITOR	.1 uF	SPRAGUE	IC20Z5U104M050B
RESISTOR	5.11K OHM, 1%	DALE	RN55D5111F
CAPACITOR	.1 uF	SPRAGUE	IC20Z5U104M050B
RESISTOR	1K OHM, 5%	ALLEN BRADLEY	RCR07CB102JS
CAPACITOR	.1 uF	SPRAGUE	IC20Z5U104M050B
RESISTOR	5.11K OHM, 1%	DALE	RN55D5111F
CAPACITOR	.1 uF	SPRAGUE	IC20Z5U104M050B

MODULE F14 FE CONTROL INTERFACE

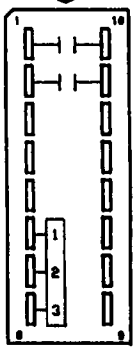
BOARD LOCATION EA19



DESCRITION	VALUE	MFG	MFG PART #
DIP HEADER			
RESISTOR	5.11K OHM, 1%	DALE	RN55D5111F
CAPACITOR	.1 uF	SPRAGUE	IC20Z5U104M050B
RESISTOR	5.11K OHM, 1%	DALE	RN55D5111F
CAPACITOR	.1 uF	SPRAGUE	IC20Z5U104M050B
RESISTOR	1K OHM, 5%	ALLEN BRADLEY	RCR07CB102JS
CAPACITOR	.1 uF	SPRAGUE	IC20Z5U104M050B
RESISTOR	1K OHM, 5%	ALLEN BRADLEY	RCR07CB102JS
CAPACITOR	.1 uF	SPRAGUE	IC20Z5U104M050B

MODULE F14 FE CONTROL INTERFACE

BOARD LOCATION EA28



DESCRITION	VALUE	MFG	MFG PART #
DIP HEADER			
CAPACITOR, TANTALUM	2.2 uF, 35 WVDC	SPRAGUE	199D225X9035BA2
CAPACITOR, TANTALUM	2.2 uF, 35 WVDC	SPRAGUE	199D225X9035BA2
VOLTAGE REGULATOR	LM78M05CT	NATIONANL SEMI	LM78M05CT/LM314T-5.0

MODULE F14 FE CONTROL INTERFACE

BOARD LOCATION EG01

5.0 DATA SHEETS

This section contains the following data sheets:

Plot of Receiver Vacuum Pressure as a function of Monitor Output Voltage

Receiver Card Cage Assembly, D53203A004

Hewlett-Packard HPDL-2416

National Semiconductor LF347

Motorola MTM8P08

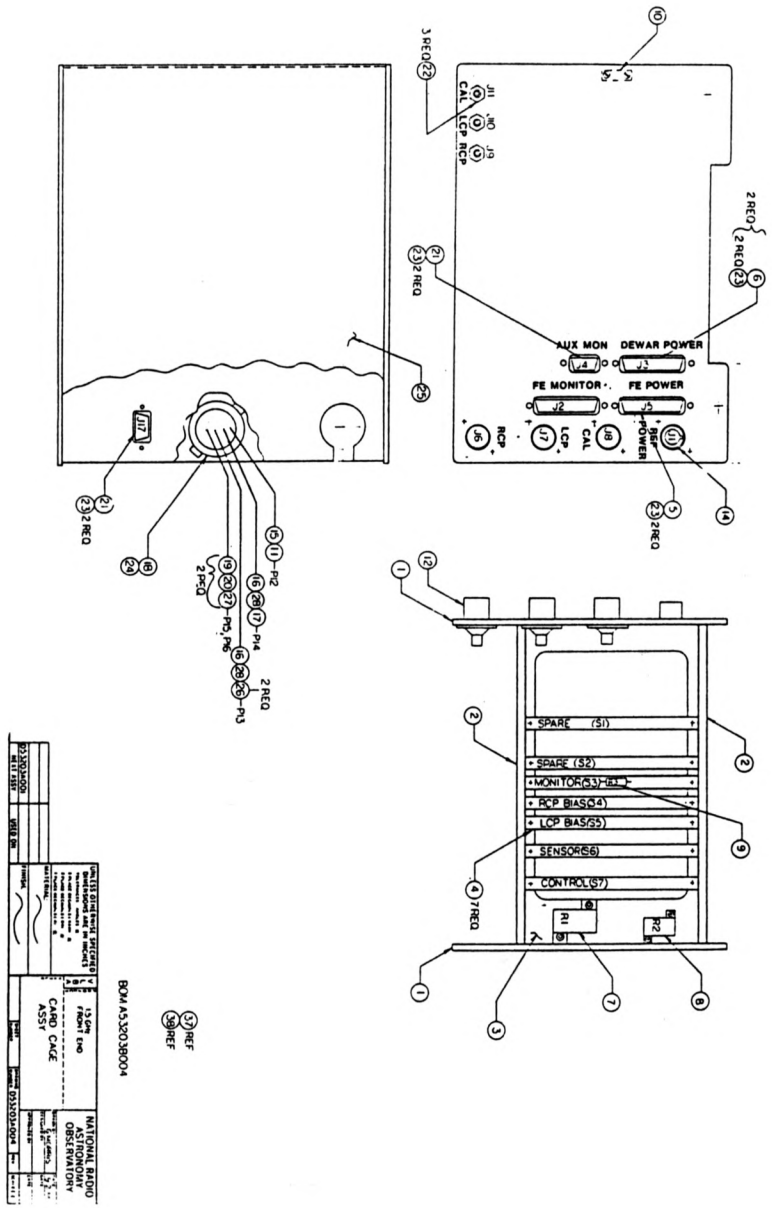
Sprague ULN2023A and Allegro 2023

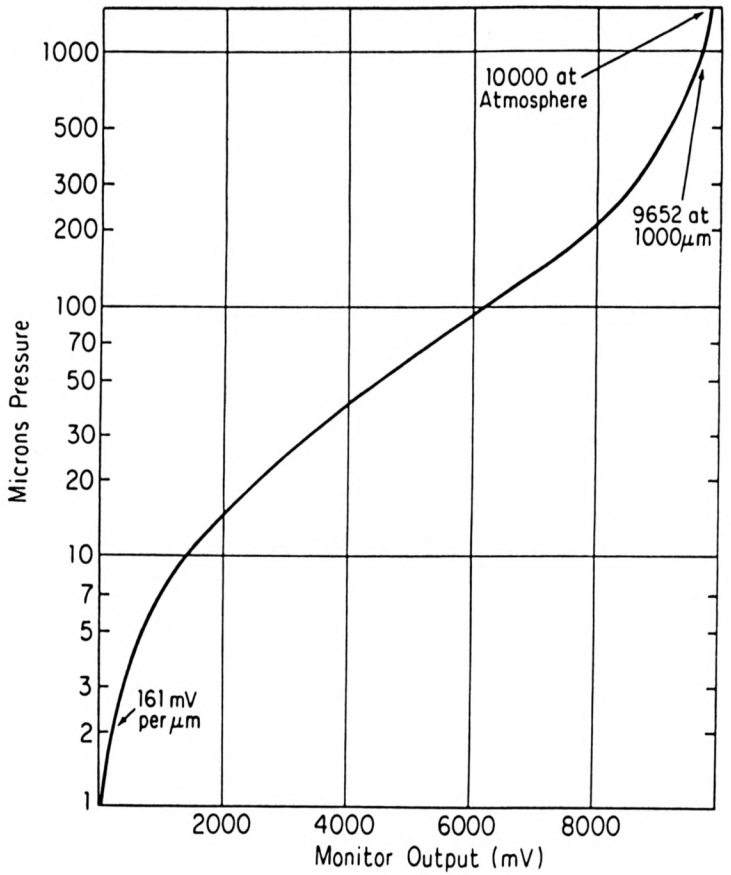
Analog Devices AD582

Harris HI508

Analog Devices AD2702

Intel 2732





Vacuum Pressure as a Function of Monitor Output Voltage

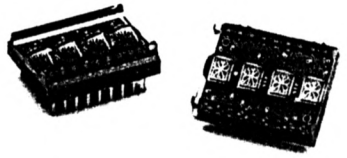
HEWLETT PACKARD

FOUR CHARACTER 4.1 mm (0.16 in.) SMART ALPHANUMERIC DISPLAY

HPDL-2416

Features

- **SMART ALPHANUMERIC DISPLAY**
  Built-in RAM, ASCII Decoder, and LED Drive Circuitry
- **WIDE OPERATING TEMPERATURE RANGE**
  –40° C to +85° C
- **VERY FAST ACCESS TIME**
  160 ns
- **EXCELLENT ESD PROTECTION**
  Built-in Input Protection Diodes
- **CMOS IC FOR LOW POWER CONSUMPTION**
- **FULL TTL COMPATIBILITY OVER OPERATING TEMPERATURE RANGE**
  V_{IL} = 0.8 V
  V_{IH} = 2.0 V
- **WAVE SOLDERABLE**
- **RUGGED PACKAGE CONSTRUCTION**
- **END-STACKABLE**
- **WIDE VIEWING ANGLE**



Description

The HPDL-2416 has been designed to incorporate several improvements over competitive products. It has a wide operating temperature range, fast IC access time and improved ESD protection. The HPDL-2416 is fully TTL compatible, wave solderable, and highly reliable. This display is ideally suited for industrial and commercial applications where a good looking, easy-to-use alphanumeric display is required.

The HPDL-2416 is a smart 4.1 mm (0.16 in) four character, sixteen-segment red GaAsP display. The on-board CMOS IC contains memory, ASCII decoder, multiplexing circuitry, and drivers. The monolithic LED characters are magnified by an immersion lens which increases both character size and luminous intensity. The encapsulated dual-in-line package construction provides a rugged, environmentally sealed unit.

Typical Applications

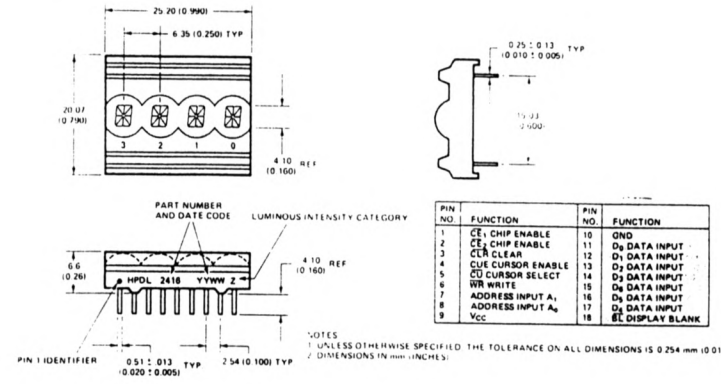
- **PORTABLE DATA ENTRY DEVICES**
- **MEDICAL EQUIPMENT**
- **PROCESS CONTROL EQUIPMENT**
- **TEST EQUIPMENT**
- **INDUSTRIAL INSTRUMENTATION**
- **COMPUTER PERIPHERALS**
- **TELECOMMUNICATION EQUIPMENT**

Absolute Maximum Ratings

Supply Voltage, V_{CC} to Ground ..... -0.5 V to 7.0 V
Input Voltage, Any Pin to Ground .... -0.5 V to V_{CC} +0.5 V
Free Air Operating, No Cursors On[1]
Temperature Range, T_A ..... -40° C to +85° C
Relative Humidity (non-condensing) at 65° C 90%
Storage Temperature, T_S ..... -40° C to +85° C
Maximum Solder Temperature, 1.59 mm (0.063 in.) below Seating Plane, t ≤ 5 sec. ..... 260° C

Note:
1. Free air operating temperature range
   T_A > 75° C No Cursors On
   T_A ≤ 75° C 1 Cursor On
   T_A ≤ 68° C 2 Cursors On
   T_A ≤ 60° C 3 Cursors On
   T_A ≤ 55° C 4 Cursors On

Package Dimensions



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	$\overline{CE}_1$ CHIP ENABLE	10	GND
2	$\overline{CE}_2$ CHIP ENABLE	11	D_6 DATA INPUT
3	$\overline{CLR}$ CLEAR	12	D_1 DATA INPUT
4	$\overline{CUE}$ CURSOR ENABLE	13	D_2 DATA INPUT
5	$\overline{CU}$ CURSOR SELECT	14	D_3 DATA INPUT
6	$\overline{WR}$ WRITE	15	D_4 DATA INPUT
7	ADDRESS INPUT A_1	16	D_5 DATA INPUT
8	ADDRESS INPUT A_0	17	D_6 DATA INPUT
9	V_{CC}	18	$\overline{BL}$ DISPLAY BLANK

Recommended Operating Conditions

Parameter	Symbol	Min.	Nom.	Max.	Units
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage High	V_{IH}	2.0			V
Input Voltage Low	V_{IL}			0.8	V

DC Electrical Characteristics Over Operating Temperature Range

TYPICAL VALUES

Parameter	Symbol	Units	-40° C	-20° C	25° C	70° C	85° C	Test Condition
I_{CC} 4 digits on (10 seg/digit)[1,2]	I_{CC}	mA	100	95	85	75	72	V_{CC} = 5.0 V
I_{CC} Cusor[2,3]	I_{CC} ($\overline{CU}$)	mA	147	140	125	110	105	V_{CC} = 5.0 V
I_{CC} Blank	I_{CC} ($\overline{BL}$)	mA	1.85		1.5		1.15	V_{CC} = 5.0 V $\overline{BL}$ = 0.8 V
Input Current, Max.	I_{IL}	μA	20		17		14	V_{CC} = 5.0 V V_{IN} = 0.8 V

GUARANTEED VALUES

Parameter	Symbol	Units	25° C V_{CC} = 5.0 V	Maximum Over Operating Temperature Range V_{CC} = 5.5 V
Icc 4 digits on (10 seg/digit)[1,2]	I_{CC}	mA	115	170
Icc Cursor[2,3]	I_{CC} ($\overline{CU}$)	mA	165	232
Icc Blank	I_{CC} ($\overline{BL}$)	mA	3.5	8.0
Input Current, Max.	I_{IL}	μA	30	40
Power Dissipation[4]	P_D	mW	575	910

Notes:
1. 16 illuminated in all four characters.
2. Measured at five seconds.
3. Cursor character is sixteen segments and DP on.
4. Power dissipation = V_{CC} × (I_{CC} (10 seg.)

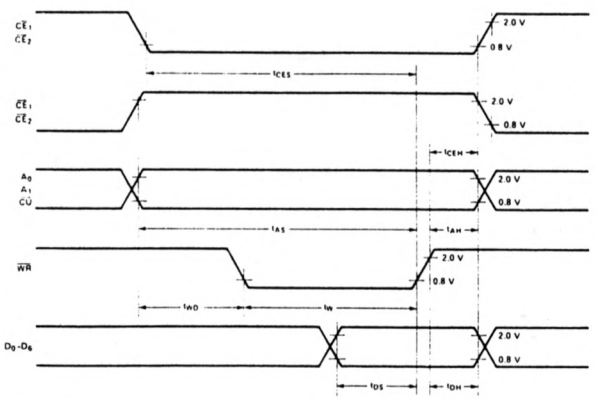
AC Timing Characteristics Over Operating Temperature Range at V_{CC} = 4.5 V

Parameter	Symbol	-20°C t_{MIN}	25°C t_{MIN}	70°C t_{MIN}	Units
Address Setup Time	t_{AS}	90	115	150	ns
Write Delay Time	t_{WD}	10	15	20	ns
Write Time	t_W	80	100	130	ns
Data Setup Time	t_{DS}	40	60	80	ns
Data Hold Time	t_{DH}	40	45	50	ns
Address Hold Time	t_{AH}	40	45	50	ns
Chip Enable Hold Time	t_{CEH}	40	45	50	ns
Chip Enable Setup Time	t_{CES}	90	115	150	ns
Clear Time	t_{CLR}	2.4	3.5	4.0	ms
Access Time		130	160	200	ns
Refresh Rate		420-790	310-630	270-550	Hz

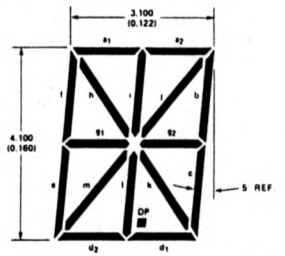
Optical Characteristics

Parameter	Symbol	Test Condition	Min.	Typ.	Units
Peak Luminous Intensity per digit, 8 segments on (character average)	Iv Peak	V_{CC} = 5.0 V "X" illuminated in all 4 digits.	0.5	1.25	mcd
Peak Wavelength	λpeak			655	nm
Dominant Wavelength	λ_d			640	nm
Off Axis Viewing Angle				±50	degrees
Digit Size				4.1	mm

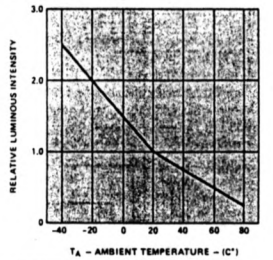
Timing Diagram



Magnified Character Font Description



Relative Luminous Intensity vs. Temperature



Electrical Description

Display Internal Block Diagram

Figure 1 shows the internal block diagram for the HPDL-2416 display. The CMOS IC consists of a four-word ASCII memory, a four-word cursor memory, a 64-word character generator, 17 segment drivers, four digit drivers, and the scanning circuitry necessary to multiplex the four monolithic LED characters. In normal operation, the divide-by-four counter sequentially accesses each of the four RAM locations and simultaneously enables the appropriate display digit driver. The output of the RAM is decoded by the character generator which, in turn, enables the appropriate display segment drivers. For each display location, the cursor enable (CUE) selects whether the data from the ASCII RAM (CUE = 0) or the stored cursor (CUE = 1) is to be displayed. The cursor character is denoted by all sixteen segments and the DP ON. Seven-bit ASCII data is stored in RAM. Since the display utilizes a 64-character decoder, half of the possible 128 input combinations are invalid. For each display location where $D_5 = D_6$ in the ASCII RAM, the display character is blanked. The entire display is blanked when $\overline{BL} = 0$.

Data is loaded into the display through the data inputs (D_6-D_0), address inputs (A_1, A_0), chip enables ($\overline{CE}_1$, $\overline{CE}_2$), cursor select ($\overline{CU}$), and write ($\overline{WR}$). The cursor select ($\overline{CU}$) determines whether data is stored in the ASCII RAM ($\overline{CU}$ = 1) or cursor memory ($\overline{CU}$ = 0). When $\overline{CE}_1 = \overline{CE}_2 = \overline{WR} = 0$ and $\overline{CU} = 1$, the information on the data inputs is stored in the ASCII RAM at the location specified by the address inputs (A_1, A_0). When $\overline{CE}_1 = \overline{CE}_2 = \overline{WR} = 0$ and $\overline{CU} = 0$, information on the data input, D_0, is stored in the cursor at the location specified by the address inputs (A_1, A_0). If D_0 = 1, a cursor character is stored in the cursor memory. If D_0 = 0, a previously stored cursor character will be removed from the cursor memory.

If the clear input ($\overline{CLR}$) equals zero for one internal display cycle (4 ms minimum), the data in the ASCII RAM will be rewritten with zeroes and the display will be blanked. Note that the blanking input ($\overline{BL}$) must be equal to logical one during this time.

Data Entry

Figure 2 shows a truth table for the HPDL-2416 display. Setting the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) to their low state and the cursor select ($\overline{CU}$) to its high state will enable data loading. The desired data inputs (D_6-D_0) and address inputs (A_1, A_0) as well as the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) and cursor select ($\overline{CU}$) must be held stable during the write cycle to ensure that the correct data is stored into the display. Valid ASCII data codes are shown in Figure 3. The display accepts standard seven-bit ASCII data. Note that $D_6 = D_5$ for the codes shown in Figure 2. If $D_6 = D_5$ during the write cycle, then a blank will be stored in the display. Data can be loaded into the display in any order. Note that when $A_1 = A_0 = 0$, data is stored in the furthest right-hand display location.

Cursor Entry

As shown in Figure 2, setting the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) to their low state and the cursor select ($\overline{CU}$) to its low state will enable cursor loading. The cursor character is indicated by the display symbol having all 16 segments and the DP ON. The least significant data input (D_0), the address inputs (A_1, A_0), the chip enables ($\overline{CE}_1$, $\overline{CE}_2$), and the cursor select ($\overline{CU}$) must be held stable during the write cycle to ensure that the correct data is stored in the display. If D_0 is in a low state during the write cycle, then a cursor character will be removed at the indicated location. If D_0 is in a high state euring the write cycle, then a cursor character will be stored at the indicated location. The presence or absence of a cursor character does not affect the ASCII data stored at that location. Again, when $A_1 = A_0 = 0$, the cursor character is stored in the furthest right-hand display location.

All stored cursor characters are displayed if the cursor enable (CUE) is high. Similarly, the stored ASCII data words are displayed, regardless of the cursor characters, if the cursor enable (CUE) is low. The cursor enable (CUE) has no effect on the storage or removal of the cursor characters within the display. A flashing cursor is displayed by pulsing the cursor enable (CUE). For applications not requiring a cursor, the cursor enable (CUE) can be connected to ground and the cursor select ($\overline{CU}$) can be connected to V_{CC}. This inhibits the cursor function and allows only ASCII data to be loaded into the display.

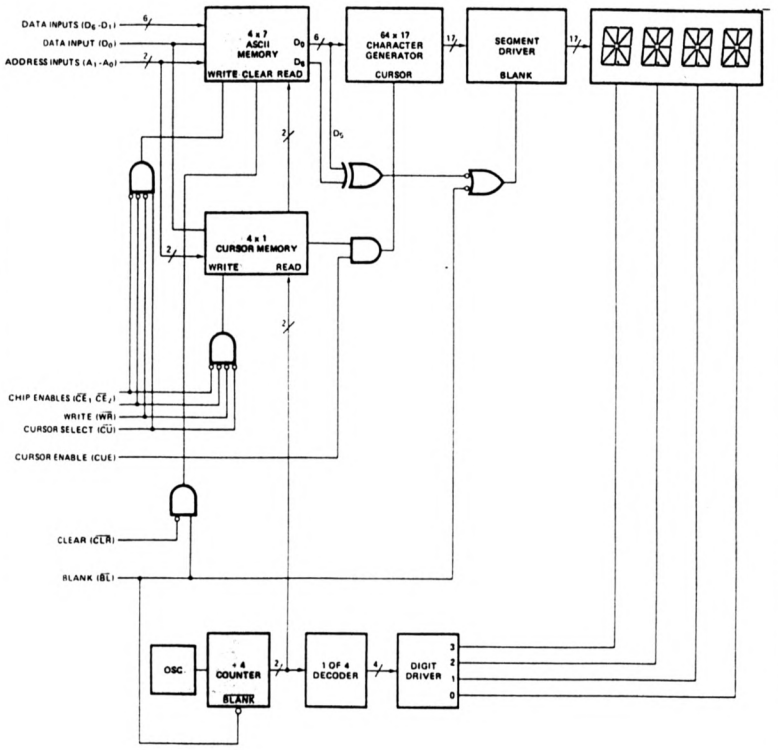


Figure 1. HPDL-2416 Internal Block Diagram

Display Clear

As shown in Figure 2, the ASCII data stored in the display will be cleared if the clear ($\overline{CLR}$) is held low and the blanking input ($\overline{BL}$) is held high for 4 ms minimum. The cursor memory is not affected by the clear ($\overline{CLR}$) input. Cursor characters can be stored or removed even while the clear ($\overline{CLR}$) is low. Note that the display will be cleared regardless of the state of the chip enables ($\overline{CE}_1$, $\overline{CE}_2$). However, to ensure that all four display characters are cleared, $\overline{CLR}$ should be held low for 4 ms following the last write cycle.

Display Blank

As shown in Figure 2, the display will be blanked if the blanking input ($\overline{BL}$) is held low. Note that the display will be blanked regardless of the state of the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) or write ($\overline{WR}$) inputs. The ASCII data stored in the display and the cursor memory are not affected by the blanking input. ASCII data and cursor data can be stored even while the blanking input ($\overline{BL}$) is low. Note that while the blanking input ($\overline{BL}$) is low, the clear ($\overline{CLR}$) function is inhibited. A flashing display can be obtained by applying a low frequency square wave to the blanking input ($\overline{BL}$). Because the blanking input ($\overline{BL}$) also resets the internal display multiplex counter, the frequency applied to the blanking input ($\overline{BL}$) should be much slower than the display multiplex rate. Finally, dimming of the display through the blanking input ($\overline{BL}$) is not recommended.

For further application information please consult Application Note 1026.

Function	$\overline{BL}$	$\overline{CLR}$	CUE	$\overline{CU}$	$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WR}$	A_1	A_0	D_6	D_5	D_4	D_3	D_2	D_1	D_0	DIG_3	DIG_2	DIG_1	DIG_0
Write Data Memory	L	X	X	H -OR-	L	L	L	L	L	a	a	a	a	a	a	a	NC	NC	NC	A
								L	H	b	b	b	b	b	b	b	NC	NC	B	NC
	X	H	X	H	L	L	L	H	L	c	c	c	c	c	c	c	NC	C	NC	NC
								H	H	d	d	d	d	d	d	d	D	NC	NC	NC
Disable Data Memory Write	X	X	X	H	X	X	H	X	X	X	X	X	X	X	X	X	Previously Written Data			
	X	X	X	H	X	H	X													
	X	X	X	H	H	X	X													
Write Cursor	X	X	X	L	L	L	L	L	L	X	X	X	X	X	X	H	NC	NC	NC	▩
								L	H	X	X	X	X	X	X	H	NC	NC	▩	NC
								H	L	X	X	X	X	X	X	H	NC	▩	NC	NC
								H	H	X	X	X	X	X	X	H	▩	NC	NC	NC
Clear Cursor	X	X	X	L	L	L	L	L	L	X	X	X	X	X	X	L	NC	NC	NC	⬚
								L	H	X	X	X	X	X	X	L	NC	NC	⬚	NC
								H	L	X	X	X	X	X	X	L	NC	⬚	NC	NC
								H	H	X	X	X	X	X	X	L	⬚	NC	NC	NC
Disable Cursor Memory	X	X	X	L	X	X	H	X	X	X	X	X	X	X	X	X	Previously Written Cursor			
	X	X	X	L	X	H	X													
	X	X	X	L	H	X	X													

L = LOGIC LOW INPUT
H = LOGIC HIGH INPUT
X = DON'T CARE

"a" = ASCII CODE CORRESPONDING TO SYMBOL "A"
NC = NO CHANGE
▩ = CURSOR CHARACTER (ALL SEGMENTS ON)

Figure 2a. Cursor/Data Memory Write Truth Table

Function	$\overline{BL}$	$\overline{CLR}$	CUE	$\overline{CU}$	$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WR}$	DIG_3	DIG_2	DIG_1	DIG_0	
CUE	H	H	L	X	X	X	X	A	B	C	D	Display previously written data
	H	H	H	X	X	X	X	▩	▩	▩	▩	Display previously written cursor
Clear	H	L	X	X	X	X	X*	⬚	⬚	⬚	⬚	Clear data memory, cursor memory unchanged
	*NOTE: CLR should be held low for 4 ms following the last WRITE cycle to ensure all data is cleared.											
Blanking	L	X	X	X	X	X	X	⬚	⬚	⬚	⬚	Blank display, data and cursor memories unchanged.

Figure 2b. Displayed Data Truth Table

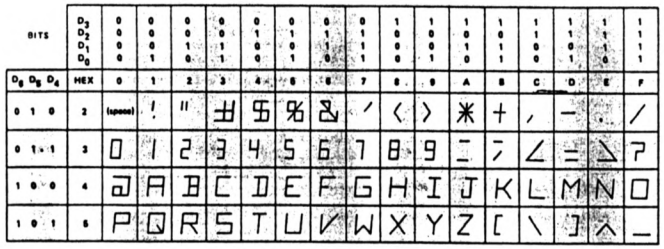


Figure 3. HPDL-2416 ASCII Character Set

Mechanical and Electrical Considerations

The HPDL-2416 is an 18 pin dual-in-line package that can be stacked horizontally and vertically to create arrays of any size. This display is designed to operate continuously between -40°C to +85°C with a maximum of 10 segments on per digit.

During continuous operation of all four Cursors the operating temperature should be limited to -40° C to +55° C. At temperatures above +55°C, the maximum number of Cursors illuminated continuously should be reduced as follows: No Cursors illuminated at operating temperatures above 75°C. One Cursor can be illuminated continuously at operating temperatures below 75°C. Two Cursors can be illuminated continuously at operating temperatures below 68°C. Three Cursors can be illuminated continuously at operating temperatures below 60°C.

The HPDL-2416 is assembled by die attaching and wire bonding the four GaAsP/GaAs monolithic LED chips and the CMOS IC to a high temperature printed circuit board. An immersion lens is formed by placing the PC board assembly into a nylon lens filled with epoxy. A plastic cap creates an air gap to protect the CMOS IC. Backfill epoxy environmentally seals the display package. This package construction provides the display with a high tolerance to temperature cycling.

The inputs to the CMOS IC are protected against static discharge and input current latchup. However, for best results standard CMOS handling precautions should be used. Prior to use, the HPDL-2416 should be stored in antistatic tubes or conductive material. During assembly a grounded conductive work area should be used, and assembly personnel should wear conductive wrist straps. Lab coats made of synthetic material should be avoided since they are prone to static charge build-up. Input current latchup is caused when the CMOS inputs are subjected either to a voltage below ground (V_{IN} < ground) or to a voltage higher than V_{CC} (V_{IN} > V_{CC}) and when a high current is forced into the input. To prevent input current latchup and ESD damage, unused inputs should be connected either to ground or to V_{CC}. Voltages should not be applied to the inputs until V_{CC} has been applied to the display. Transient input voltages should be eliminated.

Soldering and Post Solder Cleaning Instructions for the HPDL-2416

The HPDL-2416 may be hand soldered or wave soldered with SN63 solder. Hand soldering may be safely performed only with an electronically temperature-controlled and securely grounded soldering iron. For best results, the iron tip temperature should be set at 315°C (600°F). For wave soldering, a rosin-based RMA flux can be used. The solder wave temperature should be 245°C ±5°C (473°F ±9°F), and the dwell in the wave should be set at 1½ to 3 seconds for optimum soldering. Preheat temperature should not exceed 93°C (200°F) as measured on the solder side of the PC board.

Post solder cleaning may be performed with a solvent or aqueous process. For solvent cleaning, Allied Chemical Genesolv DES, Baron Blakeslee Blaco-Tron TES or DuPont Freon TE can only be used. These solvents are azeotropes of trichlorotrifluoroethane FC-113 with low concentrations of ethanol (5%). The maximum exposure time in the solvent vapors at boiling temperature should not exceed 2 minutes. Solvents containing high concentrations of alcohols, pure alcohols, isopropanol or acetone should not be used as they will chemically attack the nylons lens. Solvents containing trichloroethane FC-111 or FC-112 and trichloroethylene (TCE) are not recommended.

An aqueous cleaning process is highly recommended. A saponifier, such as Kester-Bio-kleen Formula 5799 or equivalent, may be added to the wash cycle of an aqueous process to remove rosin flux residues. Organic acid flux residues must be thoroughly removed by an aqueous cleaning process to prevent corrosion of the leads and solder connections. The optimum water temperature is 60°C (140°F). The maximum cumulative exposure of the HPDL-2416 to wash and rinse cycles should not exceed 15 minutes.

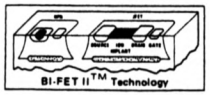
Optical Considerations/ Contrast Enhancement

The HPDL-2416 display uses a precision aspheric immersion lens to provide excellent readability and low off-axis distortion. The aspheric lens produces a magnified character height of 4.1 mm (0.160 in.) and a viewing angle of ±50°. These features provide excellent readability at distances up to 2 metres (6 feet).

Each HPDL-2416 display is tested for luminous intensity and marked with an intensity category on the side of the display package. To ensure intensity matching for multiple package applications, mixing intensity categories for a given panel is not recommended.

The HPDL-2416 display is designed to provide maximum contrast when placed behind an appropriate contrast enhancement filter. Some suggested filters are Panelgraphic Ruby Red 60, Panelgraphic Dark Red 63, SGL Homalite H100-1650, Rohm and Haas 2423, Chequers Engraving 118, and 3M R6510. For further information on contrast enhancement, see Hewlett-Packard Application Note 1015.

National Semiconductor Corporation



LF147/LF347/LF347B Wide Bandwidth Quad JFET Input Operational Amplifiers

General Description

The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

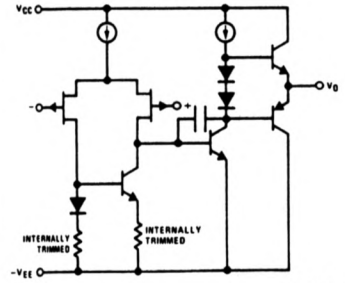
The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Features

- Internally trimmed offset voltage — 2 mV
- Low input bias current — 50 pA
- Low input noise current — 0.01 pA/√Hz
- Wide gain bandwidth — 4 MHz
- High slew rate — 13 V/μs
- Low supply current — 7.2 mA
- High input impedance — $10^{12}\Omega$
- Low total harmonic distortion $A_V = 10$, R_L10k, $V_O = 20$ Vp-p, BW = 20 Hz–20 kHz — <0.02%
- Low 1/f noise corner — 50 Hz
- Fast settling time to 0.01% — 2 μs

Simplified Schematic

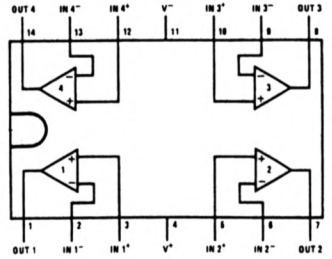
¼ Quad



TL/H/5647-13

Connection Diagram

Dual-In-Line Package



TL/H/5647-1

Top View

Order Number LF147D, LF347D, LF147J, LF347BJ, LF347J, LF347M, LF347WM, LF347BN or LF347N
See NS Package Number D14E, J14A, M14A, M14B or N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LF147	LF347B/LF347
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous
Power Dissipation (Notes 3 and 9)	900 mW	1000 mW
T_j max	150°C	150°C
θ_{jA}	105°C/W	90°C/W
Operating Temperature Range	(Note 4)	(Note 4)

	LF147	LF347B/LF347
Storage Temperature Range	$-65°C \le T_A \le 150°C$	
Lead Temperature (Soldering, 10 sec.)	260°C	260°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)		260°C
Small Outline Package		
Vapor Phase (60 seconds)		215°C
Infrared (15 seconds)		220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF147			LF347B			LF347			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$ Over Temperature		1	5 8		3	5 7		5	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$		10			10			10		μV/°C
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 5, 6) Over Temperature		25	100 25		25	100 4		25	100 4	pA nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 5, 6) Over Temperature		50	200 50		50	200 8		50	200 8	pA nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L \ge 2\ k\Omega$ Over Temperature	50 25	100		50 25	100		25 15	100		V/mV V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±12	±13.5		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	+15 −12		±11	+15 −12		±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10\ k\Omega$	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)	80	100		80	100		70	100		dB
I_S	Supply Current			7.2	11		7.2	11		7.2	11	mA

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF147			LF347B			LF347			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1 Hz – 20 kHz (Input Referred)		–120			–120			–120		dB
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$		13			13			13		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$		4			4			4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1000 Hz		20			20			20		nV/√Hz
i_n	Equivalent Input Noise Current	$T_j = 25°C$, f = 1000 Hz		0.01			0.01			0.01		pA/√Hz

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 4: The LF147 is available in the military temperature range $-55°C \le T_A \le 125°C$, while the LF347B and the LF347 are available in the commercial temperature range $0°C \le T_A \le 70°C$. Junction temperature can rise to T_j max = 25°C.

Note 5: Unless otherwise specified the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF147 and for $V_S = \pm 15V$ for the LF347B/LF347. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

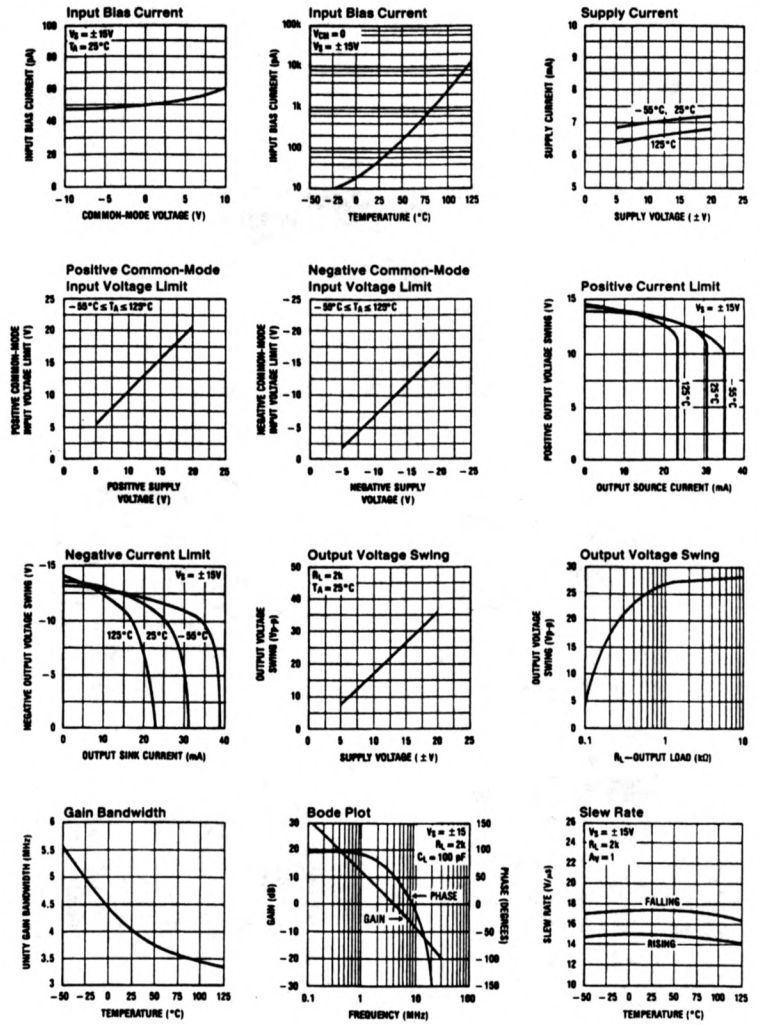
Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from $V_S = \pm 5V$ to $\pm 15V$ for the LF347 and LF347B and from $V_S = \pm 20V$ to $\pm 5V$ for the LF147.

Note 8: Refer to RETS147X for LF147D and LF147J military specifications.

Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

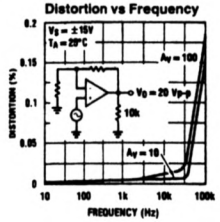
Typical Performance Characteristics



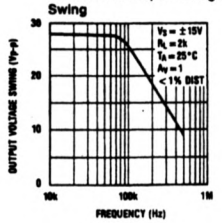
TL/H/5647-2

Typical Performance Characteristics (Continued)

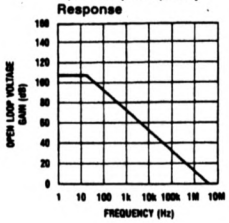
Distortion vs Frequency



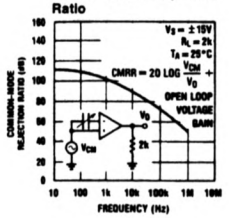
Undistorted Output Voltage Swing



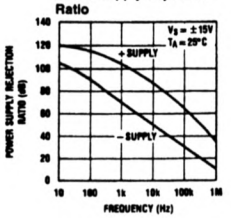
Open Loop Frequency Response



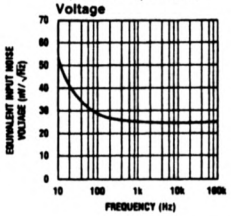
Common-Mode Rejection Ratio



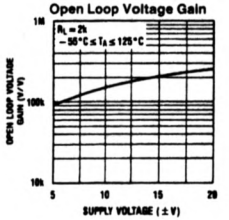
Power Supply Rejection Ratio



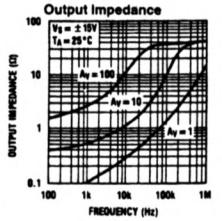
Equivalent Input Noise Voltage



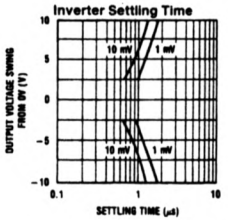
Open Loop Voltage Gain



Output Impedance



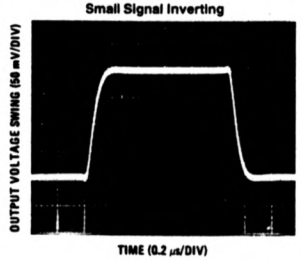
Inverter Settling Time



TL/H/5647-3

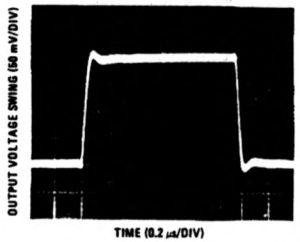
Pulse Response $R_L = 2\ k\Omega$, $C_L = 10\ pF$

Small Signal Inverting



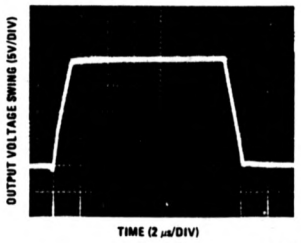
TL/H/5647-4

Small Signal Non-Inverting



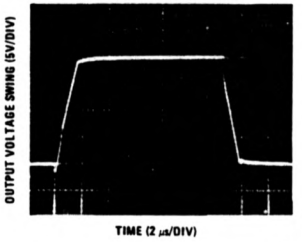
TL/H/5647-5

Large Signal Inverting



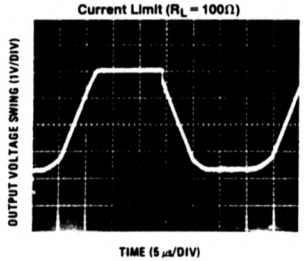
TL/H/5647-6

Large Signal Non-Inverting



TL/H/5647-7

Current Limit ($R_L = 100\Omega$)



TL/H/5647-8

Application Hints

The LF147 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier

Application Hints (Continued)

output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF147 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

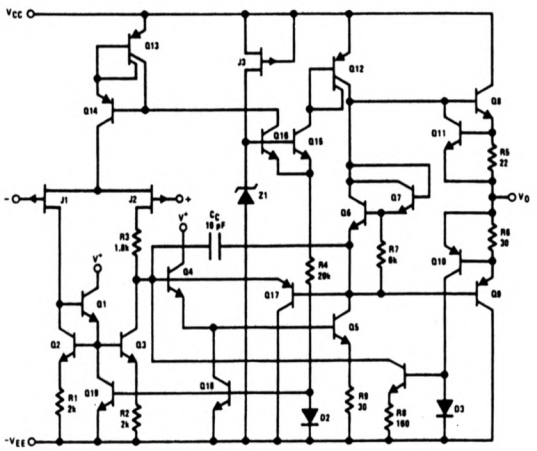
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

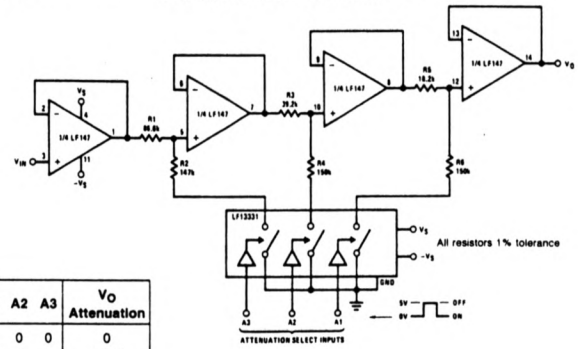
Detailed Schematic



TL/H/5647–9

Typical Applications

Digitally Selectable Precision Attenuator

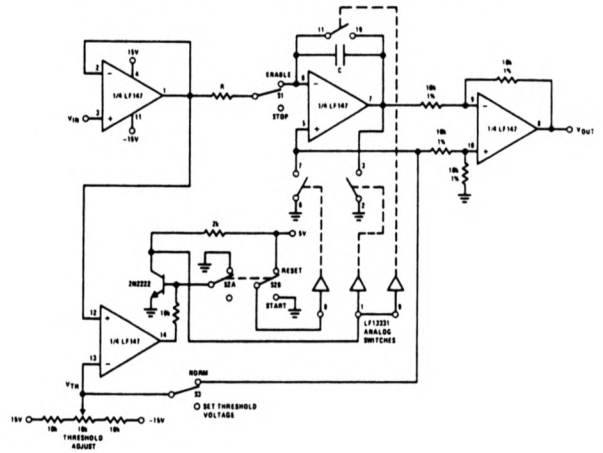


TL/H/5647–10

A1	A2	A3	VO Attenuation
0	0	0	0
0	0	1	−1 dB
0	1	0	−2 dB
0	1	1	−3 dB
1	0	0	−4 dB
1	0	1	−5 dB
1	1	0	−6 dB
1	1	1	−7 dB

- Accuracy of better than 0.4% with standard 1% value resistors
- No offset adjustment necessary
- Expandable to any number of stages
- Very high input impedance

Long Time Integrator with Reset, Hold and Starting Threshold Adjustment



TL/H/5647–11

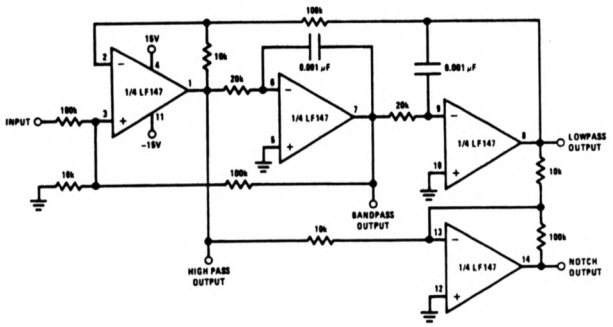
- V_{OUT} starts from zero and is equal to the integral of the input voltage with respect to the threshold voltage.

$$V_{OUT} = \frac{1}{RC}\int_0^t (V_{IN} - V_{TH})dt$$

- Output starts when $V_{IN} \geq V_{TH}$
- Switch S1 permits stopping and holding any output value
- Switch S2 resets system to zero

Typical Applications (Continued)

Universal State Variable Filter



TL/H/5647–12

For circuit shown:

f_o = 3 kHz, f_{NOTCH} = 9.5 kHz

Q = 3.4

Passband gain:

- Highpass—0.1
- Bandpass—1
- Lowpass—1
- Notch—10

- $f_o \times Q \leq 200$ kHz
- 10V peak sinusoidal output swing without slew limiting to 200 kHz
- See LM148 data sheet for design equations

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTM8P08
MTM8P10
MTP8P08
MTP8P10

Designer's Data Sheet

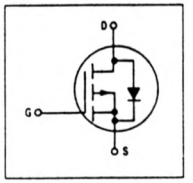
Power Field Effect Transistor
P-Channel Enhancement-Mode Silicon Gate TMOS

TMOS™

TMOS POWER FETs
8 AMPERES
$r_{DS(on)}$ = 0.4 OHM
80 and 100 VOLTS

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



MAXIMUM RATINGS

Rating	Symbol	MTM or MTP 8P08	MTM or MTP 8P10	Unit
Drain-Source Voltage	V_{DSS}	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	80	100	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50$ μs)	V_{GS} V_{GSM}	± 20 ± 40		Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	8 25		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Junction to Ambient — TO-204	$R_{\theta JA}$	30	
Junction to Ambient — TO-220		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

MTM8P08
MTM8P10
CASE 1-04
TO-204AA

MTP8P08
MTP8P10
CASE 221A-04
TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	MTM/MTP8P08 MTM/MTP8P10	$V_{(BR)DSS}$	80 100	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4 Adc)		$r_{DS(on)}$	—	0.4	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 8 Adc) (I_D = 4 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	4.8 3	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 4 A)		g_{FS}	2	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	1200	pF
Output Capacitance		C_{oss}	—	600	
Reverse Transfer Capacitance		C_{rss}	—	180	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	80	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	150	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V)	Q_g	33 (Typ)	50	nC
Gate-Source Charge		Q_{gs}	16 (Typ)	—	
Gate-Drain Charge		Q_{gd}	17 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	3 (Typ)	6	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	300 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

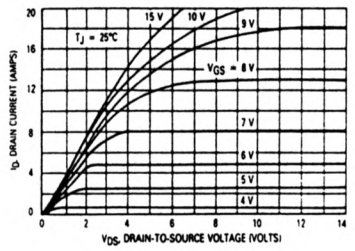


Figure 1. On-Region Characteristics

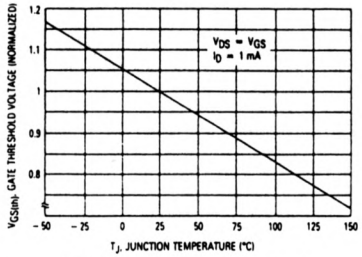


Figure 2. Gate-Threshold Voltage Variation With Temperature

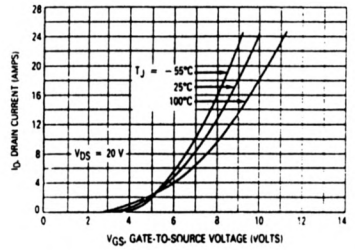


Figure 3. Transfer Characteristics

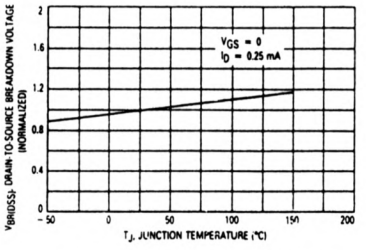


Figure 4. Normalized Breakdown Voltage versus Temperature

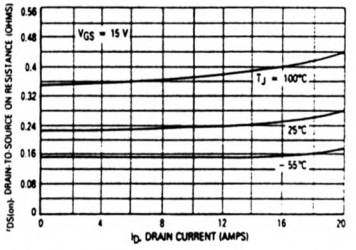


Figure 5. On-Resistance versus Drain Current

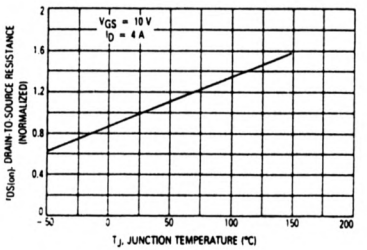


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

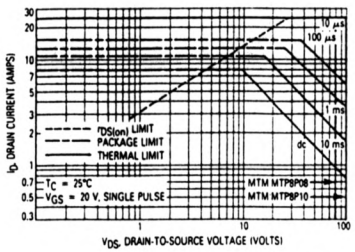


Figure 7. Maximum Rated Forward Biased Safe Operating Area

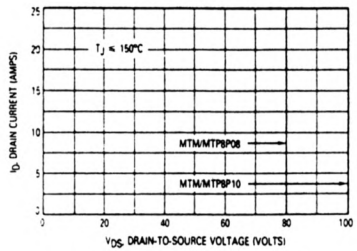


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

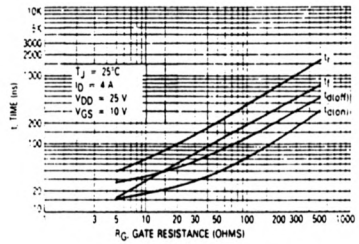


Figure 9. Resistive Switching Time Variation versus Gate Resistance

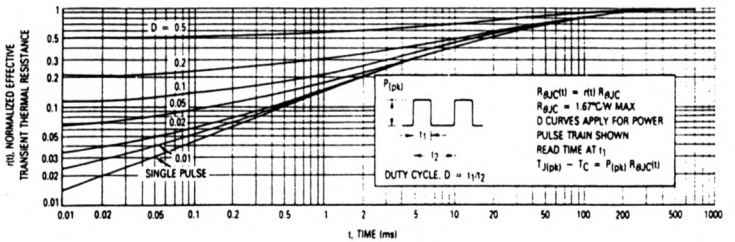


Figure 10. Thermal Response

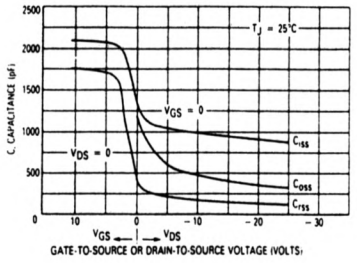


Figure 11. Capacitance Variation

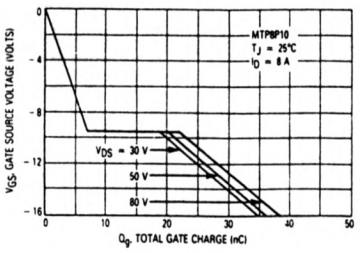


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

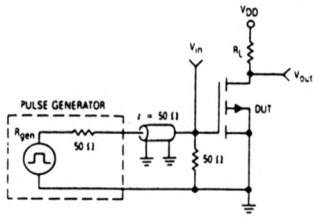


Figure 13. Switching Test Circuit

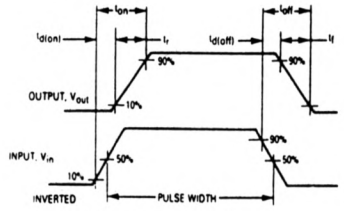
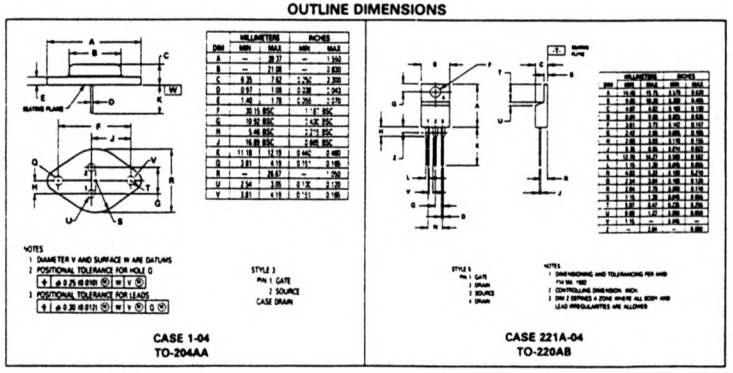


Figure 14. Switching Waveforms

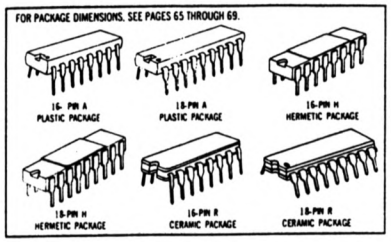
OUTLINE DIMENSIONS



SERIES 2000 and 2800 DARLINGTON ARRAYS

- High-voltage, high-current Darlington arrays comprised of seven or eight silicon NPN Darlington pairs on common monolithic substrate.
- All units feature open collector outputs and integral suppression diodes for inductive loads.
- Peak inrush currents to 600 mA are allowable, making them ideal for driving tungsten filament lamps.
- Output Voltage Up to 95 V (Series 2020 and 2820).
- Output Currents to 600 mA (saturated)
- Integral Suppression Diodes for Inductive Loads
- Inputs Compatible with DTL, TTL, PMOS, CMOS
- Package Power Dissipation to 2.25 W (Suffix 'A')
- Inputs Pinned Opposite Outputs—Lower PC Board Costs
- Able to Switch Loads of 125 W at + 70°C
- Hermetically-Sealed Package
- High Reliability Screening. See page 22.

FOR PACKAGE DIMENSIONS, SEE PAGES 65 THROUGH 69.



- Three Package Configurations:
  Plastic Dual In-Line A
  Glass/Metal Hermetic H
  Glass/Ceramic Hermetic R

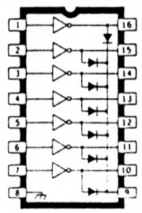
Catalog Number	See Note	No. Gates Per Pkg.	Logic/ Connection Diagram	Input Compatibility	Max. Output Rating Voltage (Volts)	Max. Output Rating Current (mA)	Operating Temperature Range	Package Style	Reference Engineering Bulletin (4)
ULN2001A	—	7	D17	General Purpose	50	500	−20°C to +85°C	16-Pin A	29304
ULN2001R	—	7	D17	General Purpose	50	500	−20°C to +85°C	16-Pin R	29304.1
ULN2002A	—	7	D17	15-25 V PMOS	50	500	−20°C to +85°C	16-Pin A	29304
ULN2002R	—	7	D17	15-25 V PMOS	50	500	−20°C to +85°C	16-Pin R	29304.1
ULN2003A	—	7	D17	5 V TTL, CMOS	50	500	−20°C to +85°C	16-Pin A	29304
ULN2003R	—	7	D17	5 V TTL, CMOS	50	500	−20°C to +85°C	16-Pin R	29304.1
ULN2004A	—	7	D17	6-15 V CMOS, PMOS	50	500	−20°C to +85°C	16-Pin A	29304
ULN2004R	—	7	D17	6-15 V CMOS, PMOS	50	500	−20°C to +85°C	16-Pin R	29304.1
ULN2005A	—	7	D17	High Output TTL	50	500	−20°C to +85°C	16-Pin A	29304
ULN2005R	—	7	D17	High Output TTL	50	500	−20°C to +85°C	16-Pin R	29304.1
ULN2011A	—	7	D17	General Purpose	50	600	−20°C to +85°C	16-Pin A	29304
ULN2011R	—	7	D17	General Purpose	50	600	−20°C to +85°C	16-Pin R	29304.1
ULN2012A	—	7	D17	15-25 V PMOS	50	600	−20°C to +85°C	16-Pin A	29304
ULN2012R	—	7	D17	15-25 V PMOS	50	600	−20°C to +85°C	16-Pin R	29304.1
ULN2013A	—	7	D17	5 V TTL, CMOS	50	600	−20°C to +85°C	16-Pin A	29304
ULN2013R	—	7	D17	5 V TTL, CMOS	50	600	−20°C to +85°C	16-Pin R	29304.1
ULN2014A	—	7	D17	6-15 V CMOS, PMOS	50	600	−20°C to +85°C	16-Pin A	29304
ULN2014R	—	7	D17	6-15 V CMOS, PMOS	50	600	−20°C to +85°C	16-Pin R	29304.1
ULN2015A	—	7	D17	High Output TTL	50	600	−20°C to +85°C	16-Pin A	29304
ULN2015R	—	7	D17	High Output TTL	50	600	−20°C to +85°C	16-Pin R	29304.1
ULN2021A	—	7	D17	General Purpose	95	500	−20°C to +85°C	16-Pin A	29304
ULN2021R	—	7	D17	General Purpose	95	500	−20°C to +85°C	16-Pin R	Note 1
ULN2022A	—	7	D17	15-25 V PMOS	95	500	−20°C to +85°C	16-Pin A	29304
ULN2022R	—	7	D17	15-25 V PMOS	95	500	−20°C to +85°C	16-Pin R	Note 1
ULN2023A	—	7	D17	5 V TTL, CMOS	95	500	−20°C to +85°C	16-Pin A	29304
ULN2023R	—	7	D17	5 V TTL, CMOS	95	500	−20°C to +85°C	16-Pin R	Note 1
ULN2024A	—	7	D17	6-15 V CMOS, PMOS	95	500	−20°C to +85°C	16-Pin A	29304
ULN2024R	—	7	D17	6-15 V CMOS, PMOS	95	500	−20°C to +85°C	16-Pin R	Note 1
ULN2025A	—	7	D17	High Output TTL	95	500	−20°C to +85°C	16-Pin A	29304
ULN2025R	—	7	D17	High Output TTL	95	500	−20°C to +85°C	16-Pin R	Note 1
ULN2801A	—	8	D18	General Purpose	50	500	−20°C to +85°C	18-Pin A	29304.3
ULN2801R	—	8	D18	General Purpose	50	500	−20°C to +85°C	18-Pin R	29304.4
ULN2802A	—	8	D18	15-25 V PMOS	50	500	−20°C to +85°C	18-Pin A	29304.3
ULN2802R	—	8	D18	15-25 V PMOS	50	500	−20°C to +85°C	18-Pin R	29304.4
ULN2803A	—	8	D18	5 V TTL, CMOS	50	500	−20°C to +85°C	18-Pin A	29304.3

continued on next page

2001 THRU 2025

HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

ULS20XXH/R



Dwg. No. A-9594

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{CE}
- (ULS200X*, ULS201X*) . . . . . 50 V
- (ULS202X*) . . . . . 95 V

Input Voltage, V_{IN}
- (ULS20X2*, X3*, X4*) . . . . . 30 V
- (ULS20X5*) . . . . . 15 V

Peak Output Current, I_{OUT}
- (ULS200X*, ULS202X*) . . . . . 500 mA
- (ULS201X*) . . . . . 600 mA

Ground Terminal Current, I_{GND} . . . . . 3.0 A

Continuous Input Current, I_{IN} . . . . . 25 mA

Power Dissipation, P_D
- (one Darlington pair) . . . . . 1.0 W
- (total package) . . . . . See Graph

Operating Temperature Range,
- T_A . . . . . -55°C to +125°C

Storage Temperature Range,
- T_S . . . . . -65°C to +150°C

X = digit to identify specific device. Characteristic shown applies to family of devices with remaining digits as shown.

*Complete part number includes a final letter to indicate package.

Comprised of seven silicon NPN Darlington power drivers on a common monolithic substrate, Series ULS2000EK, ULS2000H, and ULS2000R arrays drive relays, solenoids, magnetic print hammers, lamps, and other devices in high-reliability military or aerospace applications with up to 3 A of output current per package.

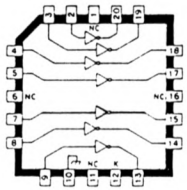
These devices are screened to MIL-STD-883, Class B and are supplied in a leadless ceramic chip carrier with Kovar lid (suffix 'EK'), the popular ceramic/metal side-brazed 16-pin hermetic package (suffix 'H'), or ceramic/glass cer-DIP hermetic package (suffix 'R'). All package styles conform to the dimensional requirements of MIL-M-38510 and are rated for operation over the full military temperature range of -55°C to +125°C. Reverse-bias burn-in and 100% high-reliability screening are standard.

The 35 integrated circuits described here permit the circuit designer to select the optimal device for any application. In addition to the three package styles (note that the ceramic chip carrier is available only for the ULS2001EK through ULS2005EK devices), there are five input characteristics, two output-voltage ratings, and two output-current ratings. The appropriate part for specific applications can be determined from the Device Part Number Designation chart. All units have open-collector outputs and on-chip diodes for inductive-load transient suppression.

FEATURES

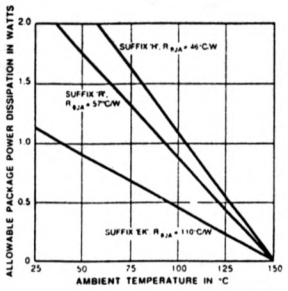
- TTL, DTL, PMOS, or CMOS Compatible Inputs
- Peak Output Current to 600 mA
- Transient-Protected Outputs
- High-Reliability Screening to MIL-STD-883, Class B
- -55°C to +125°C Temperature Range

ULS200XEK



Dwg. No. A-14,378

Always order by complete part number, e.g., ULS2013H883. See matrix on next page.



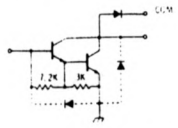
Dwg GM-004

DEVICE PART NUMBER DESIGNATION

$V_{CE(MAX)}$	50 V	50 V	95 V
$I_{C(MAX)}$	500 mA	600 mA	500 mA
Logic	**Part Number**		
General Purpose PMOS, CMOS	ULS2001*	ULS2011*	ULS2021*
14-25 V PMOS	ULS2002*	ULS2012*	ULS2022*
5 V TTL, CMOS	ULS2003*	ULS2013*	ULS2023*
6-15 V CMOS, PMOS	ULS2004*	ULS2014*	ULS2024*
High-Output TTL	ULS2005*	ULS2015*	ULS2025*

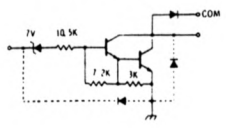
PARTIAL SCHEMATICS

ULS20X1* (Each Driver)



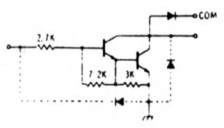
Dwg No A-9595

ULS20X2* (Each Driver)



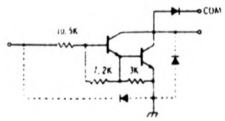
Dwg No A-9650

ULS20X3* (Each Driver)



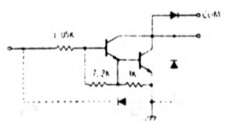
Dwg No A-9651

ULS20X4* (Each Driver)



Dwg No A-9898A

ULS20X5* (Each Driver)



Dwg No A-10,228

** Complete part number includes a final letter to indicate package (EK = leadless ceramic chip carrier, H = ceramic/metal side-brazed, R = cermic/glass cer-DIP.*

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

2001 THRU 2025
HIGH VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

ULS2001EK/H/R THRU ULS2005EK/H/R
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions Temp.	Voltage/Current	Fig.	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 50 V	1A	—	—	100	µA
		ULS2002*		V_{CE} = 50 V, V_{IN} = 6 V	1B	—	—	500	µA
		ULS2004*		V_{CE} = 50 V, V_{IN} = 1 V	1B	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	-55°C	I_C = 350 mA, I_B = 850 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 350 µA	2	—	1.1	1.3	V
			+25°C	I_C = 350 mA, I_B = 500 µA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.1	1.3	V
				I_C = 100 mA, I_B = 250 µA	2	—	0.9	1.1	V
			+125°C	I_C = 350 mA†, I_B = 500 µA	2	—	1.6	1.8	V
				I_C = 200 mA†, I_B = 350 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 250 µA	2	—	1.1	1.3	V
Input Current	$I_{I(ON)}$	ULS2002*		V_{IN} = 17 V	3	480	850	1300	µA
		ULS2003*		V_{IN} = 3.85 V	3	650	930	1350	µA
		ULS2004*		V_{IN} = 5.0 V	3	240	350	500	µA
				V_{IN} = 12 V	3	650	1000	1450	µA
		ULS2005*		V_{IN} = 3.0 V	3	—	1500	2400	µA
	$I_{I(OFF)}$	All	+125°C	I_C = 500 µA	4	25	50	—	µA
Input Voltage	$V_{I(ON)}$	ULS2002*	-55°C	V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	18	V
			+125°C	V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	13	V
		ULS2003*	-55°C	V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	3.3	V
				V_{CE} = 2.0 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	3.9	V
			+125°C	V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA†	5	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	3.0	V

Continued next page...

*Complete part number includes a final letter to indicate package
(EK = leadless/ceramic chip carrier, H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP)

NOTE 1: All limits stated apply to the complete Darlington series except as specified for a single device type.

NOTE 2: The $I_{I(OFF)}$ current limit guarantees against partial turn-on of the output.

NOTE 3: The $V_{I(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

†Pulse Test, $t_p \leq 1$ µs, see graph.

ULS2001EK/H/R THRU ULS2005EK/H/R ELECTRICAL CHARACTERISTICS continued

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Input Voltage (cont.)	$V_{IN(ON)}$	ULS2004*	-55°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	12	V
			+125°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA†	5	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	8.0	V
		ULS2005*	-55°C	V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	3.0	V
			+125°C	V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS2001*	-55°C	V_{CE} = 2.0 V, I_C = 350 mA	2	500	—	—	—
			+25°C	V_{CE} = 2.0 V, I_C = 350 mA	2	1000	—	—	—
Turn-On Delay	t_{PLH}	All	+25°C		8	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C		8	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 50 V	6	—	—	50	µA
Clamp Diode Forward Voltage	V_F	All		I_F = 350 mA†	7	—	1.7	2.0	V

*Complete part number includes a final letter to indicate package (EK = leadless ceramic chip carrier, H = ceramic metal side-brazed, R = ceramic glass cer-DIP)

NOTE 1: All limits stated apply to the complete Darlington series except as specified for a single device type.

NOTE 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.

NOTE 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

†Pulse Test, $t_p \leq 1$ µs, see graph.

ULS2011H/R THRU ULS2015H/R
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 50 V	1A	—	—	100	µA
		ULS2012*		V_{CE} = 50 V, V_{IN} = 6 V	1B	—	—	500	µA
		ULS2014*		V_{CE} = 50 V, V_{IN} = 1 V	1B	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	-55°C	I_C = 500 mA, I_B = 1100 µA	2	—	1.8	2.1	V
				I_C = 350 mA, I_B = 850 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 µA	2	—	1.3	1.5	V
			+25°C	I_C = 500 mA, I_B = 600 µA	2	—	1.7	1.9	V
				I_C = 350 mA, I_B = 500 µA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.1	1.3	V
			+125°C	I_C = 500 mA†, I_B = 600 µA	2	—	1.8	2.1	V
				I_C = 350 mA†, I_B = 500 µA	2	—	1.6	1.8	V
				I_C = 200 mA†, I_B = 350 µA	2	—	1.3	1.5	V
Input Current	$I_{IN(ON)}$	ULS2012*		V_{IN} = 17 V	3	480	850	1300	µA
		ULS2013*		V_{IN} = 3.85 V	3	650	930	1350	µA
		ULS2014*		V_{IN} = 5.0 V	3	240	350	500	µA
				V_{IN} = 12 V	3	650	1000	1450	µA
		ULS2015*		V_{IN} = 3.0 V	3	—	1500	2400	µA
	$I_{IN(OFF)}$	All	+125°C	I_C = 500 µA	4	25	50	—	µA
Input Voltage	$V_{IN(ON)}$	ULS2012*	-55°C	V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	23.5	V
			+125°C	V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	17	V
		ULS2013*	-55°C	V_{CE} = 2.0 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	3.9	V
				V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	6.0	V
			+125°C	V_{CE} = 2.0 V, I_C = 250 mA†	5	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	3.0	V
				V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	3.5	V

*Complete part number includes a final letter to indicate package (H = ceramic metal side-brazed, R = ceramic glass cer-DIP)

Continued next page...

NOTE 1: All limits stated apply to the complete Darlington series except as specified for a single device type.

NOTE 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.

NOTE 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

†Pulse Test, $t_p \leq 1$ µs, see graph.

ULS2011H/R THRU ULS2015H/R ELECTRICAL CHARACTERISTICS continued

Characteristic	Symbol	Applicable Devices	Test Conditions		Fig.	Limits			Units
			Temp.	Voltage/Current		Min.	Typ.	Max.	
Input Voltage (cont.)	$V_{IN(ON)}$	ULS2014*	-55°C	V_{CE} = 2.0 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	12	V
				V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	17	V
			+125°C	V_{CE} = 2.0 V, I_C = 275 mA†	5	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	9.5	V
		ULS2015*	-55°C	V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	3.0	V
				V_{CE} = 2.0 V, I_C = 500 mA	5	—	—	3.5	V
			+125°C	V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 500 mA†	5	—	—	2.6	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS2011*	-55°C	V_{CE} = 2.0 V, I_C = 500 mA	2	450	—	—	—
			+25°C	V_{CE} = 2.0 V, I_C = 500 mA	2	900	—	—	—
Turn-On Delay	t_{PLH}	All	+25°C		8	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C		8	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 50 V	6	—	—	50	µA
Clamp Diode Forward Voltage	V_F	All		I_F = 350 mA†	7	—	1.7	2.0	V
				I_F = 500 mA†	7	—	—	2.5	V

*Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic/glass cer-DIP).
NOTE 1: All limits stated apply to the complete Darlington series except as specified for a single device type.
NOTE 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
NOTE 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.
†Pulse Test, $t_p \leq 1$ µs, see graph.

2001 THRU 2025
HIGH VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

ULS2021H/R THRU ULS2025H/R ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions		Fig.	Limits			Units
			Temp.	Voltage/Current		Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	All		V_{CE} = 95 V	1A	—	—	100	µA
		ULS2022*		V_{CE} = 95 V, V_{IN} = 6 V	1B	—	—	500	µA
		ULS2024*	+25°C	V_{CE} = 95 V, V_{IN} = 1 V	1B	—	—	500	µA
			+125°C	V_{CE} = 95 V, V_{IN} = 0.5 V	1B	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	-55°C	I_C = 350 mA, I_B = 850 µA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 350 µA	2	—	1.1	1.3	V
			+25°C	I_C = 350 mA, I_B = 500 µA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 µA	2	—	1.1	1.3	V
				I_C = 100 mA, I_B = 250 µA	2	—	0.9	1.1	V
			+125°C	I_C = 350 mA†, I_B = 500 µA	2	—	1.6	1.8	V
				I_C = 200 mA†, I_B = 350 µA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 250 µA	2	—	1.1	1.3	V
Input Current	$I_{I(ON)}$	ULS2022*		V_{IN} = 17 V	3	480	850	1300	µA
		ULS2023*		V_{IN} = 3.85 V	3	650	930	1350	µA
		ULS2024*		V_{IN} = 5.0 V	3	240	350	500	µA
				V_{IN} = 12 V	3	550	1000	1450	µA
		ULS2025*		V_{IN} = 3.0 V	3	—	1500	2400	µA
	$I_{I(OFF)}$	All	+125°C	I_C = 500 µA	4	20	50	—	µA
Input Voltage	$V_{IN(ON)}$	ULS2022*	-55°C	V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	18	V
			+125°C	V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	13	V
		ULS2023*	-55°C	V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	3.3	V
				V_{CE} = 2.0 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2.0 V, I_C = 300 mA	5	—	—	3.9	V
			+125°C	V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA†	5	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA†	5	—	—	3.0	V

*Complete part number includes a final letter to indicate package (H = ceramic-metal side-brazed, R = ceramic glass cer-DIP)
NOTE 1: All limits stated apply to the complete Darlington series except as specified for a single device type
NOTE 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output
NOTE 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions
†Pulse Test, $t_p \leq 1$ µs, see graph.

Continued next page...

ULS2021H/R THRU ULS2025H/R ELECTRICAL CHARACTERISTICS continued

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.	Voltage/Current	Fig.	Min.	Typ.	Max.	Units
Input Voltage (cont.)	$V_{IN(ON)}$	ULS2024*	-55°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	5	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	12	V
			+125°C	V_{CE} = 2.0 V, I_C = 125 mA	5	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA†	5	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA†	5	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	8.0	V
		ULS2025*	-55°C	V_{CE} = 2.0 V, I_C = 350 mA	5	—	—	3.0	V
			+125°C	V_{CE} = 2.0 V, I_C = 350 mA†	5	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS2021*	-55°C	V_{CE} = 2.0 V, I_C = 350 mA	2	500	—	—	—
			+25°C	V_{CE} = 2.0 V, I_C = 350 mA	2	1000	—	—	—
Turn-On Delay	t_{PLH}	All	+25°C		8	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C		8	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 95 V	6	—	—	50	µA
Clamp Diode Forward Voltage	V_F	All		I_F = 350 mA†	7	—	1.7	2.0	V

*Complete part number includes a final letter to indicate package (H = ceramic/metal side-brazed, R = ceramic glass cer-DIP).

NOTE 1: All limits stated apply to the complete Darlington series except as specified for a single device type.

NOTE 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.

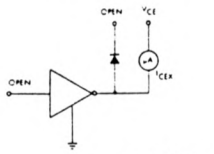
NOTE 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

†Pulse Test, $t_p \leq 1$ µs, see graph.

2001 THRU 2025
HIGH VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

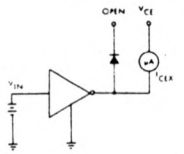
TEST FIGURES

FIGURE 1A



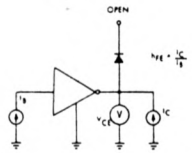
Dwg No. A-9729A

FIGURE 1B



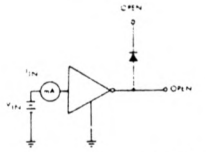
Dwg No. A-9730A

FIGURE 2



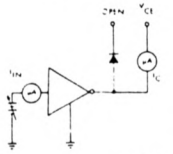
Dwg No. A-9731

FIGURE 3



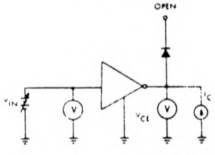
Dwg No. A-9732

FIGURE 4



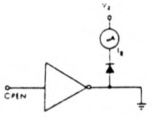
Dwg No. A-9733A

FIGURE 5



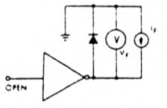
Dwg No. A-9734A

FIGURE 6



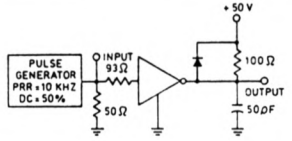
Dwg No. A-9735A

FIGURE 7

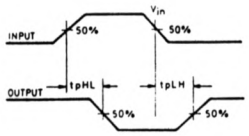


Dwg No. A-9736

	V_{IN}
ULS20X1*	3.5 V
ULS20X2*	13 V
ULS20X3*	3.5 V
ULS20X4*	12 V
ULS20X5*	3.5 V



Dwg No A-13,273



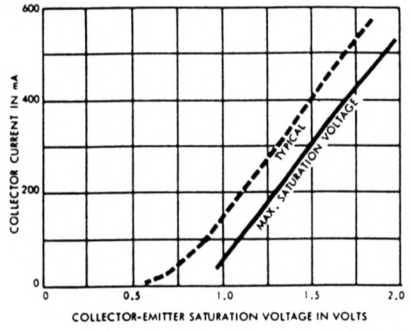
Dwg No A-13,272

* Complete part number includes a final letter to indicate package.

X= Digit to identify specific device. Specification shown applies to family of devices with remaining digits as shown.

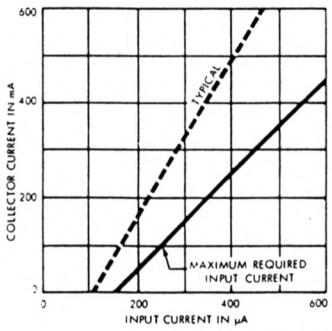
FIGURE 8

COLLECTOR CURRENT AS A FUNCTION OF SATURATION VOLTAGE



Dwg No A-9754C

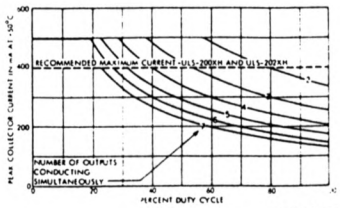
COLLECTOR CURRENT AS A FUNCTION OF INPUT VOLTAGE



Dwg No A-10,872B

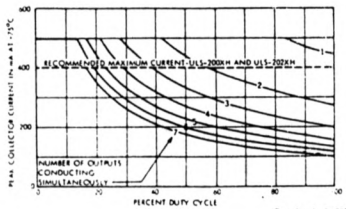
ULS20XXH

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +50°C



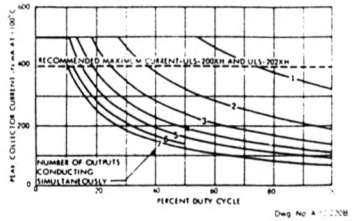
Dwg No A-12,947B

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +75°C



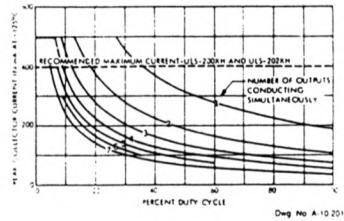
Dwg No A-10,199B

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +100°C



Dwg No A-10,200B

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +125°C

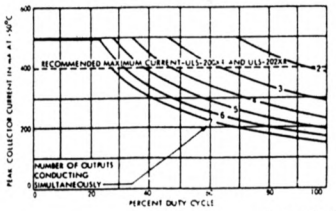


Dwg No A-10,201B

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

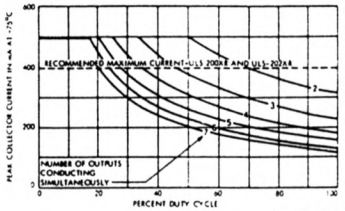
ULS20XXR

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +50°C



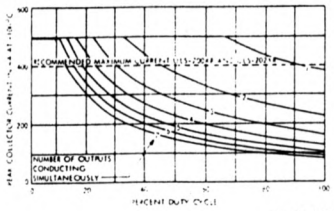
Dwg No A-10,883B

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +75°C



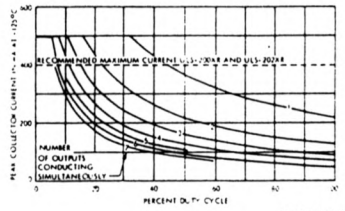
Dwg No A-10,887B

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +100°C



Dwg No A-12,434

RECOMMENDED PEAK CURRENT AS A FUNCTION OF DUTY CYCLE AT +125°C



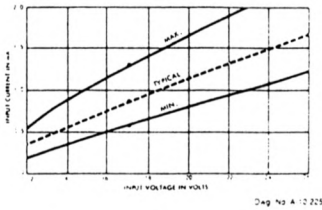
Dwg No A-12,435

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

2001 THRU 2025
HIGH VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

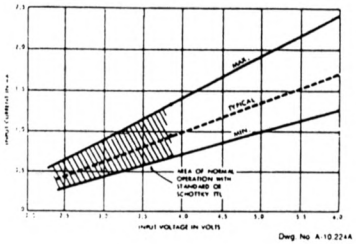
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

ULS20X2*



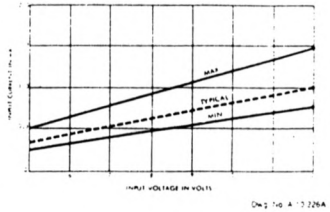
Dwg No A-12,225A

ULS20X3*



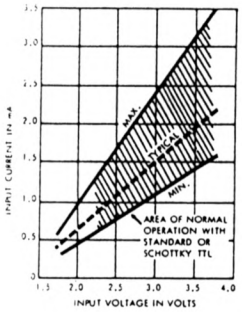
Dwg No A-10,224A

ULS20X4*



Dwg No A-12,226A

ULS20X5*



Dwg No A-10,874A

X = digit to identify specific device. Specification or limit shown applies to family of devices with remaining digits as shown.

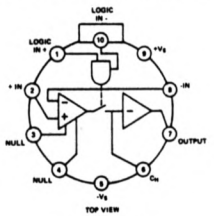
ANALOG DEVICES

Low-Cost Sample-and-Hold Amplifier

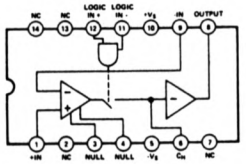
AD582

FEATURES
Suitable for 12-Bit Applications
High Sample/Hold Current Ratio: 10^7
Low Acquisition Time: 6μs to 0.1%
Low Charge Transfer: <2pC
High Input Impedance in Sample-and-Hold Modes
Connect in Any Op Amp Configuration
Differential Logic Inputs

AD582 PIN CONFIGURATIONS



10-Pin TO-100



14-Pin DIP TO-116

PRODUCT DESCRIPTION

The AD582 is a low-cost integrated circuit sample-and-hold amplifier consisting of a high performance operational amplifier, a low leakage analog switch and a JFET integrating amplifier – all fabricated on a single monolithic chip. An external holding capacitor, connected to the device, completes the sample-and-hold function.

With the analog switch closed, the AD582 functions like a standard op amp; any feedback network may be connected around the device to control gain and frequency response. With the switch open, the capacitor holds the output at its last level, regardless of input voltage.

Typical applications for the AD582 include sampled data systems, D/A deglitchers, analog de-multiplexers, auto null systems, strobed measurement systems and A/D speed enhancement.

The device is available in two versions: the "K" specified for operation over the 0 to +70°C commercial temperature range and the "S" specified over the extended temperature range, -55°C to +125°C. All versions may be obtained in either the hermetic sealed, TO-100 can or the TO-116 DIP.

PRODUCT HIGHLIGHTS

1. The specially designed input stage presents a high impedance to the signal source in both sample and hold modes (up to ±12V). Even with signal levels up to $\pm V_S$, no undesirable signal inversion, peaking or loss of hold voltage occurs.
2. The AD582 may be connected in any standard op amp configuration to control gain or frequency response and provide signal inversion, etc.
3. The AD582 offers a high, sample-to-hold current ratio: 10^7. The ratio of the available charging current to the holding leakage current is often used as a figure of merit for a sample and hold circuit.
4. The AD582 has a typical charge transfer less than 2pC. A low charge transfer produces less offset error and permits the use of smaller hold capacitors for faster signal acquisition.
5. The AD582 provides separate analog and digital grounds, thus improving the device's immunity to ground and switching transients.

SPECIFICATIONS (typical @ +25°C, $V_S = \pm 15V$ and $C_H = 1000pF$, A = +1 unless otherwise specified)

MODEL	AD582K	AD582S
SAMPLE/HOLD CHARACTERISTICS		
Acquisition Time, 10V Step to 0.1%, C_H = 100pF	6μs	*
Acquisition Time, 10V Step to 0.01%, C_H = 1000pF	25μs	*
Aperture Delay, 20V p-p Input, Hold 0V	200ns	*
Aperture Jitter, 20V p-p Input, Hold 0V	15ns	*
Settling Time, 20V p-p Input, Hold 0V, to 0.01%	0.5μs	*
Droop Current, Steady State, $\pm 10V_{OUT}$	100pA max	*
Droop Current, T_{min} to T_{max}	1nA	150nA max
Charge Transfer	5pC max (1.5pC typ)	*
Sample to Hold Offset	0.5mV	*
Feedthrough Capacitance 20V p-p, 10kHz Input	0.05pF	*
TRANSFER CHARACTERISTICS		
Open Loop Gain V_{OUT} = 20V p-p, R_L = 2k	25k min (50k typ)	*
Common Mode Rejection V_{CM} = 20V p-p	60dB min (70dB typ)	*
Small Signal Gain Bandwidth V_{OUT} = 100mV p-p, C_H = 100pF	1.5MHz	*
Full Power Bandwidth V_{OUT} = 20V p-p, C_H = 100pF	70kHz	*
Slew Rate V_{OUT} = 20V p-p, C_H = 100pF	3V/μs	*
Output Resistance Hold Mode, I_{OUT} = ±5mA	12Ω	*
Linearity V_{OUT} = 20V p-p, R_L = 2k	±0.01%	*
Output Short Circuit Current	±25mA	*
ANALOG INPUT CHARACTERISTICS		
Offset Voltage	6mV max (2mV typ)	*
Offset Voltage, T_{min} to T_{max}	8mV	8mV max (5mV typ)
Bias Current	1μA max (1.5μA typ)	*
Offset Current	300nA max (75nA typ)	*
Offset Current, T_{min} to T_{max}	100nA	400nA max (100nA typ)
Input Capacitance, f = 1MHz	2pF	*
Input Resistance, Sample or Hold 20V p-p Input, A = +1	30MΩ	*
Absolute Max Diff Input Voltage	30V	*
Absolute Max Input Voltage, Either Input	$\pm V_S$	*
DIGITAL INPUT CHARACTERISTICS		
+Logic Input Voltage Hold Mode, T_{min} to T_{max}, -Logic @ 0V	+2V min	*
Sample Mode, T_{min} to T_{max}, -Logic @ 0V	+0.8V max	*
+Logic Input Current Hold Mode, +Logic @ +5V, -Logic @ 0V	1.5μA	*
Sample Mode, +Logic @ 0V, -Logic @ 0V	1nA	*
-Logic Input Current Hold Mode, +Logic @ +5V, -Logic @ 0V	24μA	*
Sample Mode, +Logic @ 0V, -Logic @ 0V	4μA	*
Absolute Max Diff Input Voltage, +L to -L	+15V/-6V	*
Absolute Max Input Voltage, Either Input	$\pm V_S$	*
POWER SUPPLY CHARACTERISTICS		
Operating Voltage Range	±9V to ±18V	±9V to ±22V
Supply Current, R_L = ∞	4.5mA max (3mA typ)	*
Power Supply Rejection, ΔV_S = 5V, Sample Mode (see next page)	60dB min (75dB typ)	*
TEMPERATURE RANGE		
Specified Performance	0 to +70°C	-55°C to +125°C
Operating	-25°C to +85°C	-55°C to +125°C
Storage	-65°C to +150°C	*
Lead Temperature (Soldering, 15 sec)	+300°C	*
PACKAGE OPTIONS[1]		
TO-100 (H-10A)	AD582KH	AD582SH
TO-116 (D-14)	AD582KD	AD582SD

NOTES
*Specifications same as AD582K.
[1] See Section 13 for package outline information.
Specifications subject to change without notice.

APPLYING THE AD582

Both the inverting and non-inverting inputs are brought out to allow op amp type versatility in connecting and using the AD582. Figure 1 shows the basic non-inverting unity gain connection requiring only an external hold capacitor and the usual power supply bypass capacitors. An offset null pot can be added for more critical applications.

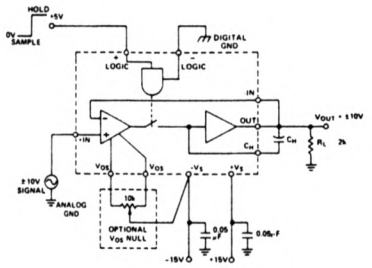


Figure 1. Sample and Hold with A = +1

Figure 2 shows a non-inverting configuration where voltage gain, A_V, is set by a pair of external resistors. Frequency shaping or non-linear networks can also be used for special applications.

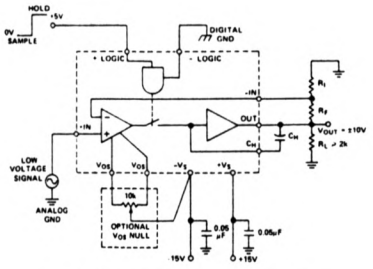


Figure 2. Sample and Hold with A = (1 + R_F/R_1)

The hold capacitor, C_H, should be a high quality polystyrene (for temperatures below +85°C) or Teflon type with low dielectric absorption. For high speed, limited accuracy applications, capacitors as small as 100pF may be used. Larger values are required for accuracies of 12 bits and above in order to minimize feedthrough, sample to hold offset and droop errors (see Figure 6). Care should be taken in the circuit layout to minimize coupling between the hold capacitor and the digital or signal inputs.

In the hold mode, the output voltage will follow any change in the $-V_S$ supply. Consequently, this supply should be well regulated and filtered.

Biasing the +Logic Input anywhere between -6V to +0.8V with respect to the -Logic will set the sample mode. The hold mode will result from any bias between +2.0V and ($+V_S$ - 3V). The sample and hold modes will be controlled differentially with the absolute voltage at either logic input ranging from $-V_S$ to within 3V of $+V_S$ (V_S - 3V). Figure 3 illustrates some examples of the flexibility of this feature.

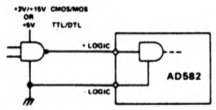


Figure 3A. Standard Logic Connection

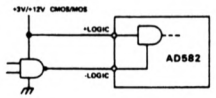


Figure 3B. Inverted Logic Sense Connection

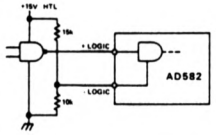


Figure 3C. High Threshold Logic Connection

DEFINITION OF TERMS

Figure 4 illustrates various dynamic characteristics of the AD582.

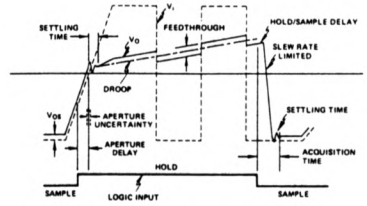


Figure 4. Pictorial Showing Various S/H Characteristics

Aperture Delay is the time required after the "hold" command until the switch is fully open and produces a delay in the effective sample timing. Figure 5 is a plot giving the maximum frequency at which the AD582 can sample an input with a given accuracy (lower curve).

Aperture Jitter is the uncertainty in Aperture Time. The Aperture Time can be eliminated by advancing the sample-to-hold command 200ns with respect to the input signal. The Aperture Jitter now determines the maximum sampling frequency (upper curve of Figure 5).

Acquisition Time is the time required by the device to reach its final value within a given error band after the sample command has been given. This includes switch delay time, slewing time and settling time for a given output voltage change.

Droop is the change in the output voltage from the "held" value as a result of device leakage. In the AD582, droop can be in either the positive or negative direction. Droop rate may be calculated from droop current using the following formula:

$$\frac{\Delta V}{\Delta T}\ (\text{Volts/sec}) = \frac{I(\text{pA})}{C_H(\text{pF})}$$

(See also Figure 6.)

Feedthrough is that component of the output which follows the input signal *after* the switch is open. As a percentage of the input, feedthrough is determined as the ratio of the feedthrough capacitance to the hold capacitance (C_F/C_H).

Sample-to-Hold Offset is an output shift or step caused by charge injection into the hold capacitor as the device is switched from sample to hold. The charge transfer generates a sample-to-hold offset where:

$$\text{S/H Offset (V)} = \frac{\text{Charge (pC)}}{C_H\ (\text{pF})}$$

This offset also has a dc component as shown in Figure 6.

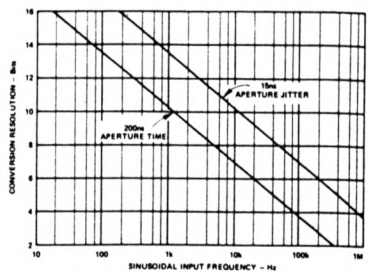


Figure 5. Maximum Frequency of Input Signal for ½LSB Sampling Accuracy

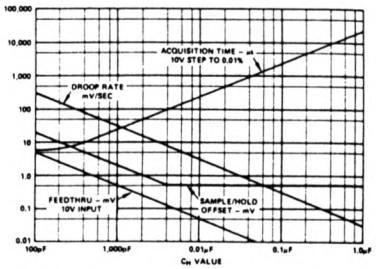


Figure 6. Sample-and-Hold Performance as a Function of Hold Capacitance

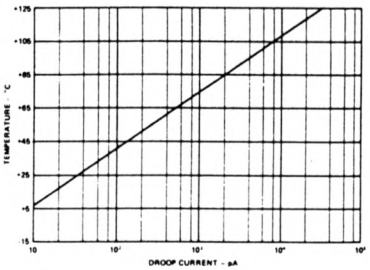


Figure 7. Droop Current vs. Temperature

HARRIS

HI-508/509

Single 8/Differential 4 Channel CMOS Analog Multiplexer

Features

- R_{ON} 180Ω
- Wide Analog Signal Range ..... ±15 V
- TTL/CMOS Compatible ..... 2.4 V (Logic "1")
- Fast Access ..... 250 ns
- Fast Settling (0.01%) ..... 600 ns
- 44V Maximum Power Supply
- Break-Before-Make Switching
- No Latch-Up
- Replaces DG508A/DG508AA and DG509A/DG509AA

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Demultiplexing
- Selector Switch

Description

These monolithic CMOS multiplexers each include an array of eight analog switches, a digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latch-up. Also, DI offers much lower substrate leakage and parasitic capacitance than conventional junction-isolated CMOS (see Application Note 521). Combined with the low ON resistance (180Ω typical), these benefits allow low static error, fast channel switching rates, and fast settling.

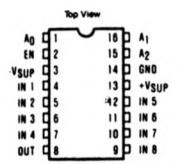
Switches are guaranteed to break-before-make, so that two channels are never shorted together.

The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4 V for "1" and Maximum 0.8 V for "0". This allows direct interface without pull-up resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and a diode clamp to each supply.

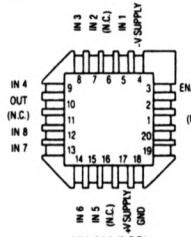
The HI-508 is an eight channel single-ended multiplexer, and the HI-509 is a four channel differential version. The recommended supply voltage is ±15 V; however, reasonable performance is available down to ±7 V. Each device is available in a 16 pin plastic or ceramic DIP, a 20 pin ceramic LCC or 20 pin plastic LCC (PLCC) package. If input overvoltage protection is needed, the HI-508A/509A multiplexers are recommended. For further information, see Application Notes 520 and 521.

The HI-508/509 is offered in both commercial and military grades, suitable for spacecraft/military applications. For additional HI-Rel screening including 160 hour burn-in, specify the "−8" suffix. For further information see Application Notes 520 and 521. For MIL-STD-883 compliant parts, request the 508/883 or 509/883 data sheet.

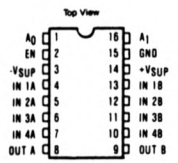
Pinouts



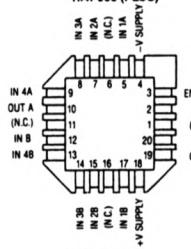
HI1-508 (ceramic)
HI3-508 (plastic)



HI4-508 (LCC)
HI4P508 (PLCC)

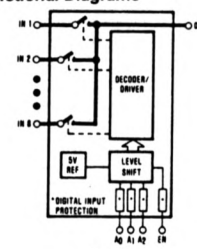


HI1-509 (ceramic)
HI3-509 (plastic)

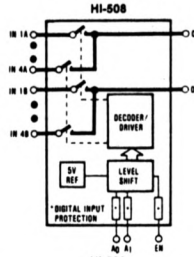


HI4-509 (LCC)
HI4P509 (PLCC)

Functional Diagrams



HI-508



HI-509

ABSOLUTE MAXIMUM RATINGS (Note 1)

$V_{Supply}(+)$ to $V_{Supply}(-)$	44 V
$V_{Supply}(+)$ to GND	22 V
$V_{Supply}(-)$ to GND	25 V
Digital Input Overvoltage:	
V_{EN}, V_A { $V_{Supply}(+)$	+4 V
$V_{Supply}(-)$	−4 V }
or 20 mA, whichever occurs first.	
Analog Signal Overvoltage (Note 7)	
V_D, V_S { $V_{Supply}(+)$	+2 V
$V_{Supply}(-)$	−2 V }

Continuous Current, S or D:	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% duty cycle max):	40 mA
Power Dissipation* (Cerdip)	1.09 W
Operating Temperature Range:	
HI-508/509-2,-8	−55°C to +125°C
HI-508/509-4	−25°C to +85°C
HI-508/509-5	0°C to +75°C
Storage Temperature Range	−65°C to +150°C

*Derate 10.9 mW/°C above T_A = 75°C

ELECTRICAL CHARACTERISTICS Unless Otherwise Specified:

Supplies = +15 V, −15 V; V_{AH}(Logic Level High) = +2.4 V, V_{AL} (Logic Level Low) = +0.8 V. For Test Conditions, consult Performance Characteristics Section.

PARAMETER	TEMP.	HI-508/HI-509 −2, −8 MIN.	TYP.	MAX.	HI-508/509 −4, −5 MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	−15		+15	−15		+15	V
*R_{ON}, On Resistance (Note 2)	+25°C		180	300		180	400	Ω
	Full			400			500	Ω
ΔR_{ON}, Any Two Channels	+25°C		5			5		%
*I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.03			0.03		nA
	Full			50			50	nA
*I_D (OFF), Off Output Leakage Current (Note 3)	+25°C		0.3			0.3		nA
HI-508	Full			200			200	nA
HI-509	Full			100			100	nA
*I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.3			0.3		nA
HI-508	Full			200			200	nA
HI-509	Full			100			100	nA
*I_{DIFF}, Differential Off Output Leakage Current (HI-509 Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
*V_{AL}, Input Low Threshold	Full			0.8			0.8	V
*V_{AH}, Input High Threshold	Full	2.4			2.4			V
*I_A, Input Leakage Current (High or Low) (Note 4)	Full			1.0			1.0	µA
SWITCHING CHARACTERISTICS								
*t_A, Access Time	+25°C		250	500		250		ns
	Full			1000			1000	ns
*t_{OPEN}, Break-Before-Make Interval	+25°C	25	80		25	80		ns
*t_{ON} (EN), Enable Turn-On	+25°C		250	500		250		ns
	Full			1000			1000	ns
*t_{OFF} (EN), Enable Turn-Off	+25°C		250	500		250		ns
	Full			1000			1000	ns
t_S, Settling Time to 0.1%	+25°C		360			360		ns
to 0.01%	+25°C		600			600		ns
"Off Isolation" (Note 5)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-508	+25°C		22			22		pF
HI-509	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		.08			.08		pF
POWER REQUIREMENTS								
*I+, Positive Supply Current (Note 6)	Full		1.5	2		1.5	2	mA
*I−, Negative Supply Current (Note 6))	Full		0.4	1		0.4	1	mA
P_D, Power Dissipation	Full			45			45	mW

*100% tested for Dash 8. Leakage currents not tested at −55°C.

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = −1 mA.
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Digital input leakage is primarily due to the clamp diodes (see Schematics). Typical leakage is less than 1 nA at 25°C.
5. V_{EN} = 0.8 V, R_L = 1 K, C_L = 15 pF, V_S = 7 V_{RMS}, f = 100 kHz. Worst case isolation occurs on channel 4 due to proximity of the output pins.
6. V_{EN}, V_A = 0 V or 2.4 V.
7. Signal voltage at any analog input or output (S or D) will be clamped to the supply rail by internal diodes. Limit the resulting current as shown under absolute maximum ratings. If an overvoltage condition is anticipated (analog input exceeds either power supply voltage), the HARRIS HI-508A/509A multiplexers are recommended.

TRUTH TABLES

HI-508

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509

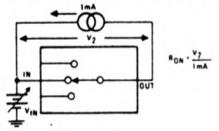
A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

Performance Characteristics and Test Circuits

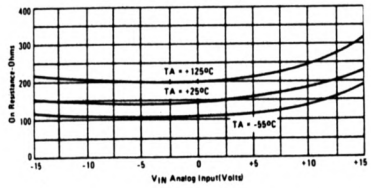
Unless Otherwise Specified; T_A = 25°C, V_{Supply} = ±15 V, V_{AH} = 2.4 V, V_{AL} = 0.8 V.

ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

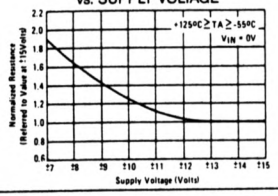
TEST CIRCUIT NO. 1



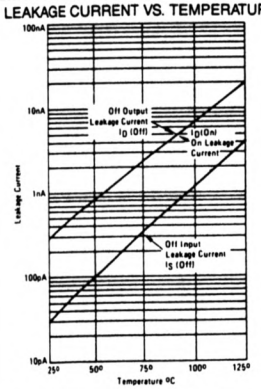
ON RESISTANCE vs. ANALOG INPUT VOLTAGE, TEMPERATURE



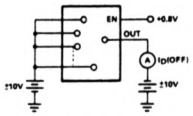
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



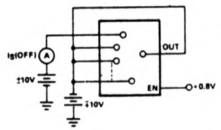
LEAKAGE CURRENT VS. TEMPERATURE



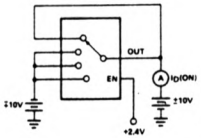
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 4*

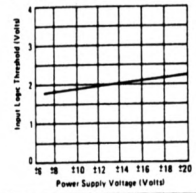


TEST CIRCUIT NO. 3*

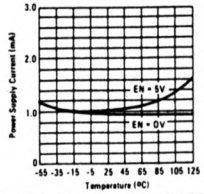


*Two measurements per channel: +10 V/−10 V and −10 V/+10 V. (Two measurements per device for ID(OFF): +10 V/−10 V and −10 V/+10 V.)

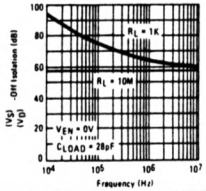
LOGIC THRESHOLD vs. POWER SUPPLY VOLTAGE



POWER SUPPLY CURRENT vs. TEMPERATURE

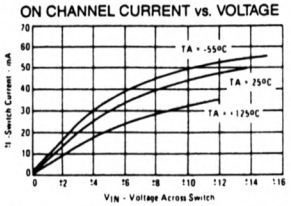


OFF ISOLATION vs. FREQUENCY



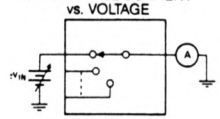
Performance Characteristics and Test Circuits (continued)

ON CHANNEL CURRENT vs. VOLTAGE

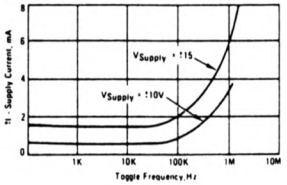


TEST CIRCUIT NO. 5

ON CHANNEL CURRENT vs. VOLTAGE

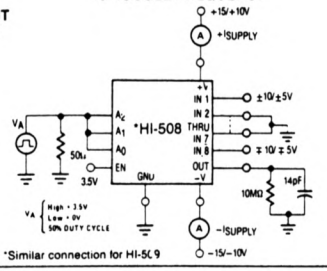


SUPPLY CURRENT vs. TOGGLE FREQUENCY



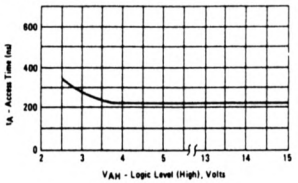
TEST CIRCUIT NO. 6

SUPPLY CURRENT vs. TOGGLE FREQUENCY



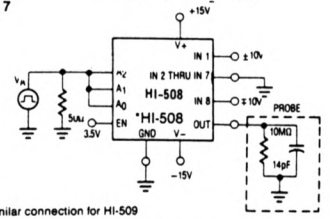
*Similar connection for HI-509

ACCESS TIME vs. LOGIC LEVEL (HIGH)



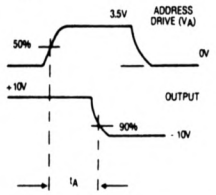
TEST CIRCUIT NO. 7

ACCESS TIME vs. LOGIC LEVEL (HIGH)

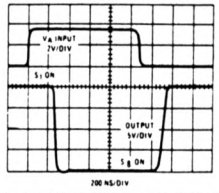


*Similar connection for HI-509

Switching Wav



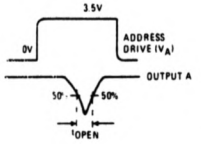
ACCESS TIME



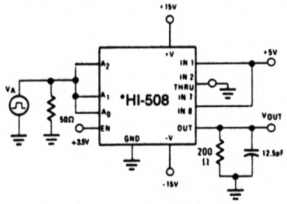
Switching Waveforms (continued)

TEST CIRCUIT NO. 8

ADDRESS DRIVE

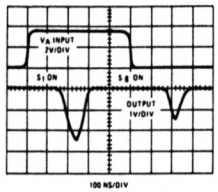


BREAK-BEFORE-MAKE DELAY (t_{OPEN})



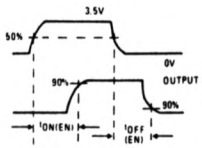
*Similar connection for HI-509

BREAK-BEFORE-MAKE DELAY(t_{OPEN})

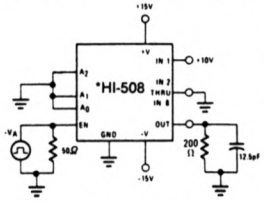


TEST CIRCUIT NO. 9

ENABLE DRIVE

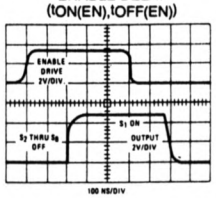


ENABLE DELAY ($t_{ON(EN)}$,$t_{OFF(EN)}$)



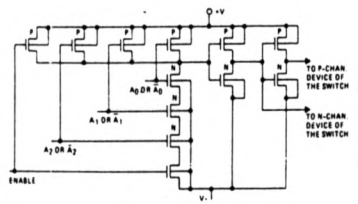
*Similar connection for HI-509

ENABLE DELAY ($t_{ON(EN)}$,$t_{OFF(EN)}$)



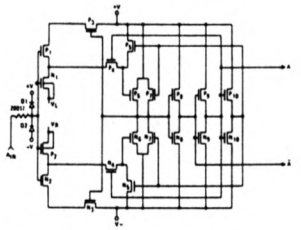
Schematic Diagrams

ADDRESS DECODER



Delete A_2 or $\overline{A_2}$ Input for HI-509

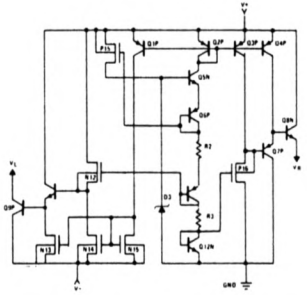
ADDRESS INPUT BUFFER LEVER SHIFTER



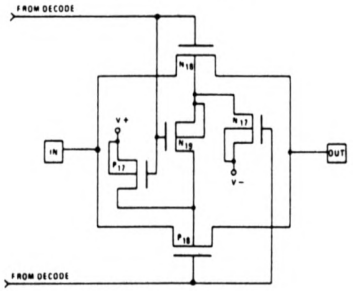
All N-Channel Bodies to V–
All P-Channel Bodies to V+ Unless Otherwise Indicated

Schematic Diagrams (continued)

TTL REFERENCE CIRCUIT

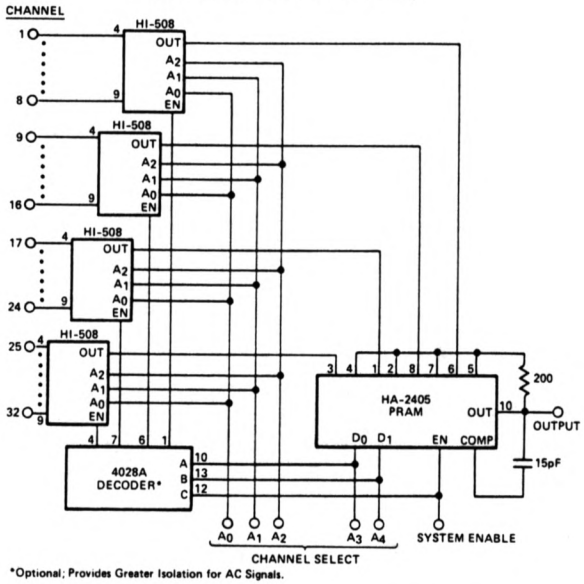


MULTIPLEX SWITCH



Applications

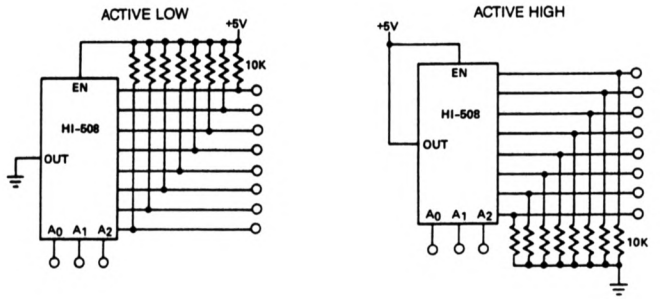
32 CHANNEL BUFFERED MULTIPLEXER



*Optional; Provides Greater Isolation for AC Signals.

Applications (continued)

ONE OF 8 DECODER



Die Characteristics

Transistor Count		243
Die Size		86 x 79 mils
Thermal Constants	θja	92°C/W } For Ceramic Dip
	θjc	37°C/W }
Tie Substrate to:		$-V_{Supply}$
Process:		CMOS - DI

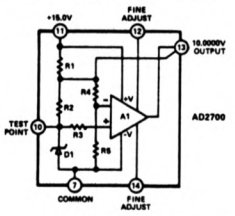
ANALOG DEVICES

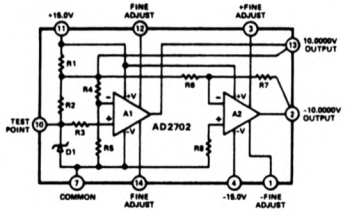
±10 Volt Precision Reference Series

AD2700/AD2701/AD2702

FEATURES
Very High Accuracy: 10.000 Volts ±2.5mV (L and U)
Low Temperature Coefficient: 3ppm/°C
Performance Guaranteed -55°C to +125°C
10mA Output Current Capability
Low Noise
Short Circuit Protected

AD2700 SERIES FUNCTIONAL BLOCK DIAGRAMS





PRODUCT DESCRIPTION

The AD2700 family of precision 10 volt references offer the user excellent accuracy and stability at a moderate price by combining the recognized advantages of thin film technology and active laser trimming. The low temperature drift (3ppm/°C) achieved with these technologies can be matched only by the use of ovens, chip heaters for temperature regulation, or with hand selected components and manual trimming. In addition, temperature-regulated devices are guaranteed only up to +85°C operation, whereas the U- and S-grade devices in the AD2700 family are guaranteed to +125°C.

The AD2700 is a +10 volt reference which is designed to interface with high accuracy bipolar D/A converters of 10 and 12 bit resolution. The 10mA output drive capability also makes the AD2700 ideal for use as a general positive system reference.

The AD2701 is a negative 10 volt reference especially designed to interface with CMOS D/A and A/D converters, as shown in the applications. For systems requiring a dual tracking reference, the AD2702 offers both positive and negative precision 10 volt outputs in a single package. Both are often used with 52XX Series 12-bit A/D converters which require -10V external references for high accuracy over wide temperature ranges.

All three devices are offered in "J" and "L" grades for operation from -25°C to +85°C and "S" and "U" grades for the -55°C to +125°C temperature range.

PRODUCT HIGHLIGHTS

1. Active laser trimming of both initial accuracy and temperature performance results in very high accuracy over the temperature range without external components. The AD2700/01/02 LD grades have a maximum output voltage error at 25°C of ±2.5mV with no external adjustments.
2. The performance of the AD2700 series is achieved by a well-characterized design and precise control over the manufacturing process.
3. The AD2700 series is well suited for a broad range of applications requiring an accurate, stable reference source such as high resolution data converters (12 or 14 bits), test and measurement systems and calibration standards.

Model	Output
AD2700	+10.000V
AD2701	-10.000V
AD2702	±10.000V

SPECIFICATIONS (max or min @ E_{in} ±15V @ +25°C, R_L = 2kΩ unless otherwise noted)

MODEL	JD	LD	SD	UD
ABSOLUTE MAX RATINGS				
Input Voltage (for applicable supply)	±20V	•	•	•
Power Dissipation @ +25°C – AD2700, 01	300mW	•	•	•
– AD2702	450mW	•	•	•
Operating Temperature Range	-25°C to +85°C	•	-55°C to +125°C	***
Storage Temperature Range	-65°C to +150°C	•	•	•
Lead Temperature (soldering, 10s)	+300°C	•	•	•
Short Circuit Protection (to GND)	Continuous	•	•	•
OUTPUT VOLTAGE ERROR @ +25°C				
AD2700 10.000V	±0.005V	±0.0025V	•	**
AD2701 -10.000V	±0.005V	±0.0025V	•	**
AD2702 ±10.000V	±0.005V	±0.0025V	•	**
OUTPUT CURRENT[1] – @ +25°C	±10mA	•	•	•
(V_{IN} = ±13 to ±18V) over op. temp. range	±5mA	+5mA, -2mA	**	**
OUTPUT VOLTAGE ERROR – AD2700,01	10ppm/°C	3ppm/°C	**	**
(T_{min} to T_{max})[2]	±11.0mV	±4.3mV	±8mV	±5.5mV
AD2702	10ppm/°C	5ppm/°C	**	3ppm/°C
	±11.0mV	±5.5mV	±10.0mV	±5.5mV
LINE REGULATION				
V_{IN} = ±13.5 to ±16.5V	300µV/V	•	•	•
LOAD REGULATION				
0 to ±10mA	50µV/mA	•	•	•
OUTPUT RESISTANCE	0.05Ω	•	•	•
INPUT VOLTAGE, OPERATING	±13V to ±18V	•	•	•
QUIESCENT CURRENT – AD2700, 01	±14mA	•	•	•
– AD2702	+17mA, -4mA	•	•	•
NOISE				
(0.1 to 10Hz)	50µV p-p typ	•	•	•
LONG TERM STABILITY (@ +55°C)	100ppm/1000 Hrs. (typ)	•	•	•
OFFSET ADJUST RANGE				
(See Diagrams)	±20mV (min)	•	•	•
OFFSET ADJUST TEMP DRIFT EFFECT	±4µV/°C per mV of Adjust (typ)	•	•	•
PACKAGE OPTION[3,4]	DH-14B	DH-14B	DH-14B	DH-14B

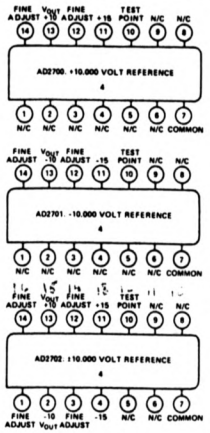
$52.65 ea, $61.30 ea

Lynn

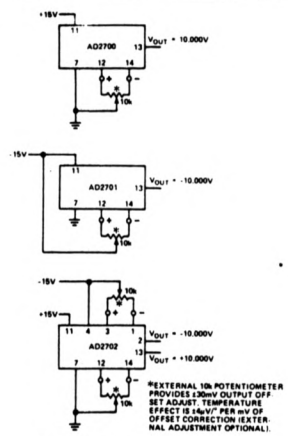
NOTES
*Same as "JD" grade performance.
**Same as "LD" grade performance.
***Same as "SD" grade performance.

[1] Specified with resistive load to common.
[2] Output voltage error as a function of temperature is determined using the box method. Each unit is tested at T_{min}, T_{max} and +25°C. At each temperature V_{OUT} must fall within the rectangular area bounded by the minimum and maximum temperature and whose maximum V_{OUT} value is equal to V_{OUT} nominal plus or minus the maximum +25°C error plus the maximum drift error from +25°C. The box limits are noted below the drift values used to calculate the box.
[3] Analog Devices reserves the right to ship metal packages in lieu of the standard ceramic packages for J and L grade parts.
[4] See Section 13 for package outline information.

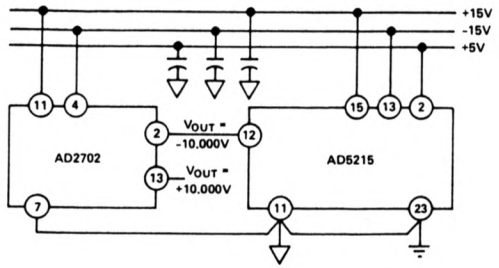
Specifications subject to change without notice.



Pin Designations



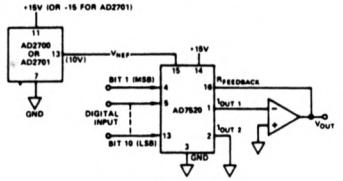
Fine Trim Connections



Using AD2702 Reference with the Fast, High Accuracy AD5215 – 12-Bit ADC

USING AD2700 REFERENCE WITH THE AD7520 AND AN IC AMPLIFIER TO BUILD A DAC

The AD2700 series is ideal for use with the AD7520 series of CMOS D/A converters. A CMOS converter in a unipolar application as shown below performs an inversion of the voltage reference input. Thus, use of the +10 volt AD2700 reference will result in a 0 to -10 volt output range. Alternatively, using the -10 volt AD2701 will result in a 0 to +10 volt range. Two operational amplifiers are used to give a bipolar output range of -10 volt to +10 volt, as shown in the lower figure. Either the AD2700 or AD2701 can be used, depending on the transfer code characteristic desired. For more detailed applications information, refer to the AD7520 Data Sheet.

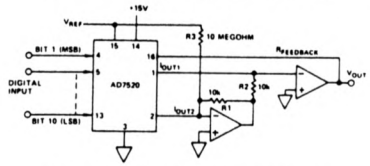


Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}(1 - 2^{-10})$
1000000001	$-V_{REF}(1/2 + 2^{-10})$
1000000000	$\frac{-V_{REF}}{2}$
0111111111	$-V_{REF}(1/2 - 2^{-10})$
0000000001	$-V_{REF}(2^{-10})$
0000000000	0

NOTE: 1 LSB = $2^{-10} V_{REF}$

Table I. Code Table – Unipolar Binary Operation



Bipolar Operation (4-Quadrant Multiplication)

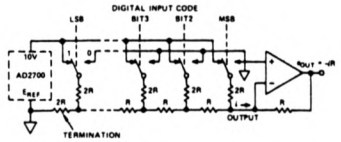
DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}(1 - 2^{-9})$
1000000001	$-V_{REF}(2^{-9})$
1000000000	0
0111111111	$V_{REF}(2^{-9})$
0000000001	$V_{REF}(1 - 2^{-9})$
0000000000	V_{REF}

NOTE: 1 LSB = $2^{-9} V_{REF}$

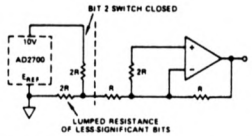
Table II. Code Table – Bipolar (Offset Binary) Operation

USING THE AD2700 VOLTAGE REFERENCE WITH D/A CONVERTER

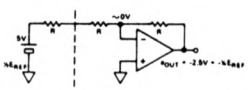
An AD2700 Voltage Reference can be used with an inverting operational amplifier and an R-2R ladder network. If all bits but the MSB are off (i.e., grounded), the output voltage is $(-R/2R)E_{REF}$. If all bits but Bit 2 are off, it can be shown that the output voltage is $\frac{1}{2}(-R/2R)E_{REF} = \frac{1}{4}E_{REF}$. The lumped resistance of all the less-significant-bit circuitry (to the left of Bit 2) is 2R; the Thevenin equivalent looking back from the MSB towards Bit 2 is the generator, $E_{REF}/2$, and the series resistance 2R; since the grounded MSB series resistance, 2R, has virtually no influence – because the amplifier summing point is at virtual ground – the output voltage is therefore $-E_{REF}/4$. The same line of thinking can be employed to show that the nth bit produces an increment of output equal to $2^{-n} E_{REF}$.



a. Basic Circuit



b. Example: Contribution of Bit 2; All Other Bits "0"



c. Simplified Equivalent of Circuit (b.)

intel

2732
32K (4K x 8) UV ERASABLE PROM

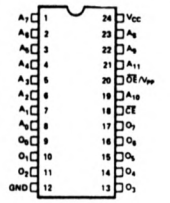
- **Fast Access Time:**
  - **390 ns Max. 2732-4**
  - **450 ns Max. 2732**
  - **550 ns Max. 2732-6**
- **Industry Standard Pinout — JEDEC Approved**
- **Pin Compatible to Intel's EPROM Family: 2716, 2732A, 2764**
- **Output Enable for MCS-85™ and MCS-86™ Compatibility**
- **Low Power Dissipation:**
  - **150 mA Max. Active Current**
  - **35 mA Max Standby Current**
- **Single +5V ± 5% Power Supply**

The Intel® 2732 is a 32,768-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2732 operates from a single 5-volt power supply, has a standby mode, and features an output enable control. The total programming time for all bits is three and a half minutes. The 2732 family with an access time up to 390 ns enhances microprocessor system performance. This family, in conjunction with the 250 ns 2732A family, solves the problem of WAIT states due to slow memories.

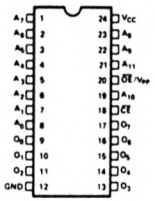
An important 2732 feature is the separate output control, Output Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems. Intel's Application Note AP-72 describes the microprocessor system implementation of the $\overline{OE}$ and $\overline{CE}$ controls on Intel's 2716 and 2732 EPROMs. AP-72 is available from Intel's Literature Department.

The 2732 has a standby mode which reduces the power dissipation without increasing access time. The maximum active current is 150 mA, while the maximum standby current is only 35 mA, a 75% savings. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input.

2732 PIN CONFIGURATION



2732A PIN CONFIGURATION



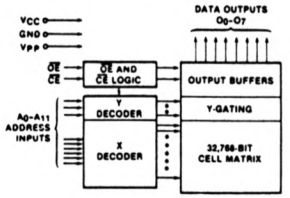
MODE SELECTION

MODE \ PINS	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	OUTPUTS (9-11,13-17)
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	Vpp	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	Vpp	+5	High Z

PIN NAMES

A_0-A_{11}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS

BLOCK DIAGRAM



PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions Section.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -10°C to +80°C
Storage Temperature ..... -65°C to +125°C
All Input or Output Voltages with Respect to Ground ..... +6V to -0.3V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ± 5%

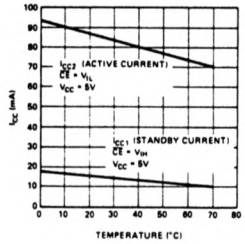
READ OPERATION

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Conditions
I_{LI1}	Input Load Current (except $\overline{OE}/V_{PP}$)			10	μA	V_{IN} = 5.25V
I_{LI2}	$\overline{OE}/V_{PP}$ Input Load Current			10	μA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.25V
I_{CC1}	V_{CC} Current (Standby)		15	35	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}
I_{CC2}	V_{CC} Current (Active)		85	150	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400μA

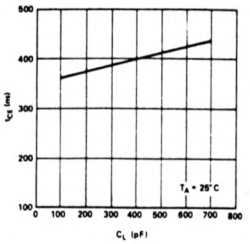
Note: 1. Typical values are for T_A = 25°C and nominal supply voltages.

TYPICAL CHARACTERISTICS

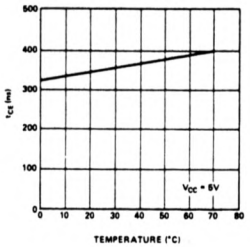
I_{CC} CURRENT VS. TEMPERATURE



$\overline{CE}$ TO OUTPUT DELAY (t_{CE}) VS. CAPACITANCE



$\overline{CE}$ TO OUTPUT DELAY (t_{CE}) VS. TEMPERATURE



A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ± 5%

Symbol	Parameter	2732-4 Limits (ns)		2732 Limits (ns)		2732-6 Limits (ns)		Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address to Output Delay		390		450		550	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		390		450		550	$\overline{OE} = V_{IL}$
t_{OE}	Output Enable to Output Delay		120		120		120	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Float	0	100	0	100	0	100	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		$\overline{CE} = \overline{OE} = V_{IL}$

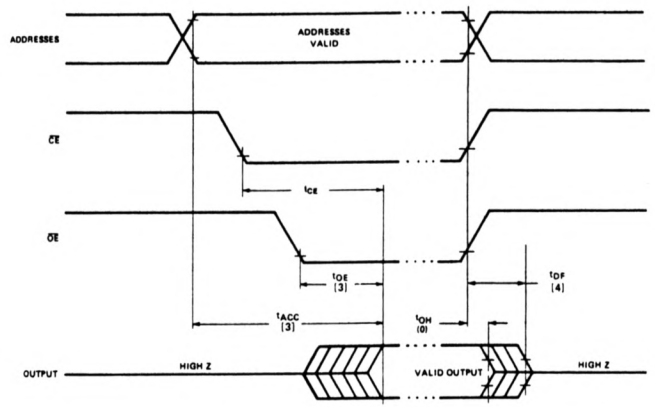
CAPACITANCE [1] T_A = 25°C, f = 1MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN1}	Input Capacitance Except $\overline{OE}/V_{PP}$	4	6	pF	V_{IN} = 0V
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance		20	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance		12	pF	V_{OUT} = 0V

A.C. TEST CONDITIONS

Output Load: 1 TTL gate and C_L = 100pF
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. WAVEFORMS [2]



NOTES:
1. THIS PARAMETER IS ONLY SAMPLED AND IS NOT 100% TESTED.
2. ALL TIMES SHOWN IN PARENTHESES ARE MINIMUM TIMES AND ARE NSEC UNLESS OTHERWISE SPECIFIED.
3. $\overline{OE}$ MAY BE DELAYED UP TO $t_{ACC} - t_{OE}$ AFTER THE FALLING EDGE OF $\overline{CE}$ WITHOUT IMPACT ON t_{ACC}.
4. t_{DF} IS SPECIFIED FROM $\overline{OE}$ OR $\overline{CE}$, WHICHEVER OCCURS FIRST.

ERASURE CHARACTERISTICS

The erasure characteristics of the 2732 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 2732 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 2732 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 2732 window to prevent unintentional erasure.

The recommended erasure procedure (see Data Catalog) for the 2732 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The 2732 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

DEVICE OPERATION

The five modes of operation of the 2732 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL level to 25V.

TABLE 1. Mode Selection

MODE \ PINS	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	OUTPUTS (9-11,13-17)
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

Read Mode

The 2732 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs 120ns (t_{OE}) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The 2732 has a standby mode which reduces the active power current by 75%, from 150mA to 35mA. The 2732 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

Because EPROMs are usually used in larger memory arrays, Intel has provided a 2 line control function that accommodates this use of multiple memory connections. The two line control function allows for:

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

PROGRAMMING (See Programming Instruction Section for Waveforms.)

Initially, and after each erasure, all bits of the 2732 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2732 is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 25V. It is required that a 0.1μF capacitor be placed across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50msec, active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time — either individually, sequentially, or at random. The program pulse has a maximum width of 55msec. The 2732 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple 2732s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2732s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled 2732s.

Program Inhibit

Programming of multiple 2732s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel 2732s may be common. A TTL level program pulse applied to a 2732's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 25V will program that 2732. A high level $\overline{CE}$ input inhibits the other 2732s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

6.0 APPENDIX

F14 I/O Connector Pin-Signal Assignments:

P1 - Amp 50 pin connector.

P3,P5,P7 - DB25P pin connector.

P2,P4,P6 - DB25S 25 socket connector.

P1	Signal	P1	Signal	P3,5,7	Signal	P2,4,6	Signal
A	+15V	d	SMA3-	1	Pwr Gnd	1	Port Vacuum Mon
B	+5V Gnd	e	DIGI-1-	2	+15V Critical	2	Dewar Vacuum Mon
C	+5V	f	SMA3- Ret	3	-15V Critical	3	15^0 Temp Mon
D	+15V Critical	h	DIGI-1- Ret	4	NA	4	50^0 Temp Mon
E	-15V	j	9.6 Hz	5	NA	5	300^0 Temp Mon
F	+/- Crit Gnd	k	Vac Pump Curr	6	X Command	6	AC Curr Mon
H	DIGO-0-	m	9.6 Hz Ret	7	C Command	7	AB (RCP) Stage 1 Mon
J	-15V Critical	n	He Supp Press	8	H Command	8	AB (RCP) Stage 2ff Mon
K	DIGO-0- Ret	p	ANLGI-0+	9	Band ID Par P_B	9	CD (LCP) Stage 1 Mon
L	Slot B/A- Jmpr	r	He Ret Press	10	NA	10	CD (LCP) Stage 2ff Mon
M	CLKO-0-	s	ANLGI-0-	11	Norm Cal Drive	11	LED Volts Mon
N	Slot B/A-	t	He Supp-Ret Gnd	12	Solar Cal Drive	12	NA
P	CLKO-0- Ret	u	ANLGI-1+	13	Rcvr Gnd Ref	13	Qual Gnd
R	SMA0-	v	NA	14	Band ID B_0	14	SENS Temp Mon
S	STRO-0-	w	ANLGI-1-	15	Band ID B_1	15	NA
T	SMA0- Ret	x	-15V Critical	16	Band ID B_2	16	NA
U	STRO-0- Ret	y	ANLGI-2+	17	Band ID B_3	17	NA
V	SMA1-	z	+15V Critical	18	Ser ID S_0	18	NA
W	STRI-1-	AA	ANLGI-1-	19	Ser ID S_1	19	NA
X	SMA1- Ret	BB	+/- Crit Gnd	20	Ser ID S_2	20	S Vac Valve Mon
Y	STRI-1- Ret	CC	ANLGI-3+	21	Ser ID S_3	21	P Pump Req Mon
Z	SMA2-	DD	+28V	22	Ser ID S_4	22	M Man Mon
a	CLKI-1-	EE	ANLGI-3-	23	Ser ID S_5	23	X Command Mon
b	SMA2- Ret	FF	+28 Ret	24	Mod M_0	24	C Command Mon
c	CLKI-1- Ret	HH	+/- 15V Gnd	25	Mod M_1	25	H Command Mon

List of Relevant NRAO Technical Reports, Memos and Supportive Data

VLBA Technical Report No. 1, Low Noise, 8.4 GHz, Cryogenic GASFET Front-End S. Weinreb, H. Dill, R. Harris August 1984

VLBA Technical Report No. 2, 1.5 GHz Cryogenic Front-End, R. Norrod, September 1986

VLBA Technical Report No. 3, 4.8 GHz Cryogenic Front-End, R. Norrod, December 1986

VLBA Technical Report No. 10, Model F104, 2.3 Ghz Cryogenic Front-End R. Norrod, M. Masterman, June 3, 1991

VLA Electronics Memorandum No. 215, Data Set 4 Command and Monitor Data for F14-equipped antennas P. Lilie, October 1989, revised March 1991

VLA Technical Report No. 58, The Data Set, Module Type M1 D. Weber 8/22/86

VLA Technical Report No. 62, The Command Simulator, Module Type M5 David Weber 9/9/86

VLA DCS Manual