VLA Technical Report No. 71
VOLUME 1

THE VLA WYE MONITOR SYSTEM HARDWARE

Philip Dooley, Arthur Sittler,
Nelson Atencio, David Weber
8/94

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

1.0 INTRODUCTION

WYE Monitor System Description

This manual describes the Very Large Array WYE Monitor system and its components. This system is a supervisory control system that provides the VLA telescope operator with comprehensive command and monitoring capabilities for VLA systems. The system was implemented to improve the control of antenna safety systems and to implement telescope operator control of major VLA facility support systems. Block Diagram C13900B12, following this section, shows the structure of this system. Important system properties and specifications are described in Section 2.1.

Implementation Concept and System Components

As shown on the block diagram, the heart of the system is an IBM-compatible personal computer (PC) that executes a control-monitor and operator interface program. The control program is the logical heart of the system; the balance of the system operates in response to program stimuli. The PC is the signal nexus and drives four buses that carry digital monitor and control messages in the WYE-COMM cables. Three of the buses are used for antenna systems and are carried in the existing North, East, and West Arm WYE-COMM cables. The fourth bus is carried in the existing Auxiliary WYE-COMM cable that is routed around the control-maintenance building complex. Devices in the control building are serviced by an extension of the Auxiliary bus.

The PC transmits command messages to the antennas and facility support systems and polls these devices for monitor data response messages. The narrow-band, time-serial digital messages operate in the half-duplex mode. The buses are multi-drop, single twisted-pair lines in the WYE-COMM cables. Message formats and protocol are described in Section 2.2

WYE Monitor system device interfacing is performed by control interface modules (M26, M27 and M29) bridged across the party-line buses. M26, M27 and M29's device interface circuitry is adapted to the requirements of the serviced device. A device is an antenna, HVAC system, generator system, etc. These modules and their interfaces to the controlled devices are described in Sections 2.8 through 2.11.

The VLA telescope operator interacts with the system via an Elographics Intellitouch Touch Screen CRT interface and a Covox Soundmaster II voice-message annunciator, both driven by the control PC. The Touch Screen display images resemble conventional system control panels equipped with illuminated push-button switches and display lights. The telescope operator initiates all commands via the Touch Screen interface and the Touch Screen displays system status and data. The Touch Screen displays are a set of nested heirarchal menus that provide detailed device control-monitor features. The PC drives a voice-message annunciator to alert the Telescope Operator to abnormal and alarm conditions. The operator interface is described in more detail in Section 2.3.

The system provides a high degree of reliability because it is not vulnerable to power losses and messages are subjected to rigorous error detection during reception. The command message protocol assures the correct reception of command messages because the addressed module echoes back the command message to the control PC for verification.

The system also has provisions to detect malfunctions in the execution of the PC control program. A Watch-Dog timer connected to the PC printer port senses periodic port activity. In the event of a

program crash or a loop hang-up, the Watch-Dog timer turns off the PC power for a few seconds to induce a power-on reset and program re-start. A hot spare back-up system can be quickly switched on-line in the event of a failure in the PC or the associated bus interface equipment.

The system also verifies that VLA observing control programs in the Modcomp computers are operating normally. Lines from these two computer's serial ports periodically signal that the program operations have reached a programmed flag point. In the event of a program crash or loop hang-up in either computer, these signals will not be emitted and the PC control program will alert the telescope operator by a voice alarm message.

The system does not perform astronomical observation control and monitor functions; this is done by the existing Monitor and Control System in conjunction with the antenna and control building electronics systems.

This brief system description highlights major aspects of the system. Section 2 below describes the system and components in more detail.

Manual Content

This manual describes the system's functional characteristics, command and monitor message formats, message protocol and error detection features, bus signal transmission and reception, telescope operator interface, the system component's theory of operation, hardware-software interactions and the M26, M27 and M29 control module's interfaces to controlled devices.

This manual does not describe the WYE-COMM voice communication system although the WYE-COMM cable drawings are included to show the WYE Monitor system signal distribution. Similarly, other than citing interface details, the manual does not describe the antenna ACU and antenna support equipment, the VLA facility back-up power generators and switch gear, the control building HVAC system and the computer and correlator UPS systems.

Although important features of the PC are cited, this manual does not describe the PC, the Touch Screen or annunciator equipment. Commercial documentation is available for this equipment.

Other than the hardware-software interactions, this manual does not describe the system's software and firmware programs; these are the subjects of a second manual, Volume II.

2.0 THEORY OF OPERATION

2.1 Important Properties and Specifications

Important Properties

Important system properties are:

- The system is not vulnerable to 110 VAC power failures. Some components are powered by Uninterruptable Power Sources (UPS's), others by M28, a battery-backed power supply module and the M26 antenna interface is powered by the antenna fire alarm batteries.

- Since time-division multiplexing is used on the single-pair party-line buses, the system is not limited by WYE-COMM cable conductor capacity. The previous implementation of the antenna reset, Emergency Stop and the fire alarm monitors was a hard-wired system that was very conductor-limited. As a result of these limitations, this earlier equipment had to share functions on a common line; for example, the NCP breaker reset function reset **all** antenna NCP breakers on an arm. Similarly, the ACU reset momentarily turned off the ACU power for **all** ACU's on an arm; this reset function perturbed the observations of all antennas on the affected arm. The antenna fire alarms were also sensed on an arm-wide basis. To identify the antenna that had activated the fire alarm, the telescope operator had to call up antenna overlays one-by-one to see if critical power had been shut down — a slow process that required several minutes. Because of the cable conductor limitations, it was not possible to monitor the antenna stow-pin states.

- The system includes the functions performed by the previous dissimilar, hard-wired antenna control-monitor equipment and also incorporates antenna monitoring functions that were not possible with the previous equipment and WYE-COMM cables. The system has the capacity to add new antenna control-monitor functions.

- The system improves the telescope operator's cognizance of the VLA system's status by providing control-monitor capability for important VLA facility systems hitherto either obscure or unimplemented.

- The system simplifies Telescope Operator control/monitor interactions because one simple, unified interface replaces several antenna/facility interface panels. The system provides equipment-specific voice messages that describe status and alarms — these immediately identify abnormal conditions and alarms and reduce the need for frequent visual status checks of the Touch Screen displays.

- Interface applications are implemented by the use of control interface modules driven by the WYE Monitor and Control bus. The control interface contains a standardized bus interface board subassembly that interacts with the party-line bus. Virtually any device control-monitor implementation is possible by "tailoring" the module's I/O circuitry to the device's interface requirements.

- The system can easily be expanded by adding additional interface modules to a capacity of 32 interface modules per bus.

- Since the digital messages have a 16-bit command and monitor data argument format, the interface's command and monitor data capacities are 16 bits of command or monitor discretes in any combination.

- Since the line drivers output a powerful signal on the bus lines and the signal detection is differential, the command-monitor messages are almost invulnerable to WYE-COMM cable cross-talk. Surge arrestors on the bus lines protect the equipment from surge voltages.

- Signal transmission is less sensitive to WYE-COMM cable length than the earlier antenna control-monitor circuitry.

- When an antenna is moved, reconfiguration of location and address are easily input to the control program in the PC.

- The system is independent of the antenna waveguide communication system so that it is not vulnerable to failures in this equipment.

- Optically-coupled isolators in the bus line receivers protect the receiving circuitry from high voltage spikes induced in the lines by lightning strikes to the antennas, rails, buildings and the earth. To date, no control interfaces have been damaged by lightning strikes.

- Optical isolators in the control module's parallel control/monitor lines protect the module's microcontroller from high voltage spikes in the device interface lines. These isolators also prevent ground-loop interactions between the devices and the control interface modules.

- A latent capability for expanding the interface module's command and monitor capacity has been incorporated in the message format but this feature has not been incorporated into the control interfaces because usage has shown that the present capacity is adequate. Implementing this capability would require changes in the hardware and firmware design. The message format assigns two address bits that could be used to designate 16-bit command or monitor functions. The four address states could expand the the capacity of the control interface to 64 bits by multiplexing I/O port lines. This 64 bit latent capacity could be any combination of command or monitor discretes.

- In addition to the system's simple discrete on-off command and monitor functions, it also performs more complex control and logical operations on some VLA equipment. For example, the antenna ACU reset function requires issuance of two commands at a five-second time interval. The antenna NCP breaker reset requires a similar dual command sequence. The system also issues phase synchronization commands to the Correlator and Computer UPS units. When the backup power generators are coming on line to assume the VLA loads, the Correlator and Computer UPS unit's output phase must be synchronized to the generator's phase before the UPS's can transfer their loads to the generator's AC power. The PC program's logic senses the loss of the commercial power and issues these UPS synchronization commands.

- Part of the operator interface is a Touch Screen CRT terminal that can display many control menus which are specialized for each device's control and monitor requirements. The hardware counterpart of the Touch Screen CRT and control menus would be a hardware control panel with many push-button, selector and toggle switches, status indicator lights, numeric displays, etc. In contrast, a hardware control panel for these functions would be very large and possibly intimidating to operate.

- The system monitors program execution in the two VLA Modcomp array control computers. The G10 and Dump programs each periodically output a serial message to the M29 module to indicate proper program execution. In the event of a program crash or loop hang-up in either computer, the periodic serial message will not be output and the system will alarm the telescope operator via annunciator messages and the Touch Screen's displays.

System Specifications

Message Bit Rate: 300 Baud.

Monitor Data Polling Rate per Bus: 450 mS/Interface.

Antenna Bus Monitor Data Polling Rate per Antenna: 4.05 Seconds.

Auxiliary Bus Monitor Data Polling Rate per device: 2.7 Seconds.

Bus Interface Unit Capacity: 32 interface module addresses.

Interface Unit Command Capacity: up to 16 discrete commands.

Interface Unit Monitor Capacity: up to 16 discrete monitor lines.[1]

Command Latency Time: 225 milliseconds.

Verification Time for Commanded States: 900 mS.

Number of Antenna Monitor Functions: 9/antenna.

Number of Antenna Command Functions: 3/antenna.

Number of Auxiliary Bus Command Functions: 3.

Number of Auxiliary Bus Monitor Functions: 31.

Number of Auxiliary Bus Analog Functions: 2.

---

[1] M29 has an analog multiplexer and A/D converter. See Section 2.11 for details.

Device Interface Line Signal Characteristics: There are no specifications since the interface circuitry is typically "tailored" to the the device's requirements.

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

NOTES:

1. NORTH, EAST, WEST ARM, AND AUXILIARY BUS PHYSICAL ROUTING ARE NOT SHOWN
2. WYE COMMUNICATIONS CABLE JUNCTION BLOCKS UNDER CONTROL ROOM FLOOR
3. HOT SPARE UNIT INSTALLED AND AVAILABLE FOR IMMEDIATE SERVICE IN CASE OF PROBLEM
4. ONE OF TWO PC'S PLUS TOUCH-SCREEN AND INTERFACE BIN. #1 IS ALWAYS ON-LINE. #2 IS A HOT SPARE
5. IDENTICAL TO NORTH ARM

CONTROL ROOM

2 NORTH ARM BUS 1 — TO OTHER NORTH ARM OBSERVING PADS

2 EAST ARM BUS 1 — TO 5 EAST ARM

2 WEST ARM BUS 1 — TO 5 WEST ARM

2 AUXILIARY BUS 1

A&B SWITCH BOX

TO INTERFACE BIN #2 (×4)

2

TOUCH-SCREEN MONITOR #1 3 4

MON AC

MON VIDEO

TOUCH SIGS

PRINTER PORT BIT (PPB)

LPT1

PC #1 SYSTEM CONTROL COMPUTER 486/33 MHZ PC

TOUCH INTERFACE CARD

QUAD RS232 SERIAL CARD

SOUND CARD

ANNUNCIATOR

PC 110VAC

SSR (BACK PANEL)

PC INTERFACE BIN #1

PC WATCHDOG TIMER	RS2321 WYE-COM INTERFACE	RS2321 WYE-COM INTERFACE	RS2321 WYE-COM INTERFACE	RS2321 WYE-COM INTERFACE	BIN POWER SUPPLY
POS. 3	NORTH ARM POS. 6	EAST ARM POS. 5	WEST ARM POS. 7	AUXILIARY POS. 4	3 POS. 8

4 RS232 MESSAGES

110VAC

RS232 HOLD-OFF SIGNAL

RS232 HOLD-OFF SIGNAL

OPERATOR CONSOLE BIN

M29 AUXILIARY UTILITY	M28 POWER SUPPLY/ BATTERY	
POS. 4	POS. 8	

110VAC

COMPUTER & CORRELATOR A/C AIR/TEMP/CHILL ALARMS, CHILLER & COND TEMPS

TOUCH-SCREEN MONITOR #2 3 4

TOUCH

VIDEO

AC

PC #2

PPB

110AC

4

TO A&B SWITCH BOX

INTERFACE BIN #2

PC AND WYE-COM SYSTEM UPS, 1KW (UNDER FLOOR)

110VAC

NORTH ARM ANTENNA

2

FOCUS/ROTATION BIN

M26 ANTENNA INTERFACE POS. 7

24V FIRE ALARM BATTERY POWER

ANTENNA MON/CMD FUNCTIONS

ACU FAULT PCB NRAO DWG #C13900P05

ACU

1 AUXILIARY BUS

2

GENERATOR BLDG

GENERATOR INTERFACE BIN

M28 POWER SUPPLY/ BATTERY	M27 AUXILIARY MONITOR	M27 AUXILIARY MONITOR	M27 AUXILIARY MONITOR
POS. 1-3	POS. 6	POS. 4	POS. 5

110VAC

MASTER CUBICLE CMD/MON FUNCTIONS

GENERATOR MONITOR FUNCTIONS

GENERATOR #1

GENERATOR #2

MASTER CUBICLE CONTROL & MONITOR SYSTEM

PROGRAMMABLE CONTROLLER

START GENERATORS

WYE MONITOR BIN

M28 POWER SUPPLY/ BATTERY	M27 AUXILIARY MONITOR	M27 AUXILIARY MONITOR
POS. 1-3	POS. 4	POS. 5

110VAC

UPS CMD/MON FUNCTIONS

UPS ROOM

CORRELATOR UPS

COMPUTER UPS

COMPUTER ROOM

MOD COMP #1

MOD COMP #2

ACAD : 13900B12

D13900B05	AUXILIARY
D13900B04	NORTH ARM
D13900B03	EAST ARM
D13900B02	WEST ARM
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES : ANGLES ±

3 PLACE DECIMALS (.###) ±

2 PLACE DECIMALS (.##) ±

1 PLACE DECIMALS (.X) ±

MATERIAL :

FINISH :

VLA PROJECT : WYE MONITOR SYSTEM

TITLE : WYE MONITOR MONITOR AND CONTROL SYSTEM BLOCK DIAGRAM

SHEET NUMBER 1 OF 1 | DRAWING NUMBER C13900B12 | REV. – | SCALE NONE

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 10-94
DESIGNED BY	DATE 10-94
APPROVED BY	DATE 10-94

2.2 Message Format and Protocol

Message Format

The system uses four types of five-byte, time-serial digital messages. Command and Monitor Request messages are output by the PC control program and addressed to the interface designated by the state of the Unit ID bits (described below). In response to either of these two messages, the addressed interface emits a Command or Monitor Acknowledge message that is read by the PC control program. The Command Acknowledge message is a literal "command echo" in which the command message Unit ID, Port 1 and Port 0 argument values are used in the Command Acknowledge message format. The Command Acknowledge message is used by the PC control program to verify that the Command message was correctly received. The state attained by a control interface in response to a Command message is read out as a Monitor Acknowledge message in response to a Monitor Request. The Monitor Acknowledge contains the data requested by the Monitor Request and is used by the program to evaluate the state of the system. The format of these messages is shown below; detailed descriptions of the bit functions follow the format definitions. SYNC, the most significant byte, is transmitted first and the CRC byte ends the message.

Byte Functions	Sync	Unit ID	Port 1 (LSB)	Port 0 (MSB)	CRC
Basic Format	$S_0 \cdots S_7$	X MM $U_0 \cdot\cdot U_4$	$A_0 \cdots A_7$	$A_8 \cdots A_{15}$	CCCCCCCC
Message Type					
Command	00010110	1 MM UUUUU	AAAAAAAA	AAAAAAAA	CCCCCCCC
Monitor Req	00010110	0 MM UUUUU	00000000	00000000	CCCCCCCC
Command Ack	E0000110	1 MM UUUUU	AAAAAAAA	AAAAAAAA	CCCCCCCC
Monitor Ack	E0000110	0 MM UUUUU	AAAAAAAA	AAAAAAAA	CCCCCCCC

The Sync byte signals the start of a message; a Unit ID (address) byte designates a specific control interface; Port 1 and Port 0 bytes are the command or data argument; and the CRC byte is an error detection code formulated over the first four message bytes.

The byte format is an 11 bit format; in time order these are Start, 8 Data Bits (LSB first), Parity Bit and Stop bit.

Note that the 8 bits of the Sync byte are identical in the Command and Monitor Request messages; this Sync byte designates messages output by the PC. Similarly, the upper 7 bits of the Command and Monitor Acknowledge messages are identical but different than the Command and Monitor Request messages; this Sync byte designates messages to be input to the PC. The E bit on the Command and Monitor Acknowledge message Sync bytes indicates that the addressed control interface detected a parity error in the message (see error detection below).

The first bit in the Unit ID byte designates the character of the message; a 1 designates a Command or Command Acknowledge message and a 0 designates a Monitor Request or Monitor Acknowledge message.

The five U bits in the Unit ID byte are a five-bit address that designates a specific control interface. U_0 is the least significant bit and U_4 is the most significant bit. The encoded address is hard-wired on the control interface bin backplane wiring to eliminate the requirement for address-encoding switches in the control interface module — these could be set erroneously during module changes or installation. In the case of M26, the antenna control interface, the encoded address corresponds to the antenna serial number.

The MM bits are reserved for potential future use as a multiplex address. At present these bits are set to the 0 state by the PC and the control interfaces.

The Port 1 and Port 0 bytes are the 16 bit message argument and the Port 1 byte is the most significant byte. These designations are those used by the control interface's 87C51 microcontroller I/O ports. A_0 is the least significant bit and A_{15} is the most significant bit. In most of the control interface applications, the message arguments are discrete functions but in the case of the M29 module, there are two monitor data arguments. One argument is an encoded analog value and the other argument is a set of 16 discretes. Four bits in the Command message determine the selection of the monitor data. Section 2.15 describes the M29 circuitry and usage of these bits in selecting the monitor data arguments.

Message Error Detection

The last byte (C bits) in the message is the CRC byte. This byte is a Cyclic Redundancy Code formulated over the first four bytes of message data by the message transmitter. During the reception of a message, the receiving unit (i.e. PC or control interface) analyzes the four data bytes of the incoming message data to formulate a CRC value. If the formulated CRC value matches that contained in the message CRC byte, the message has not been contaminated by errors. See Message Error Detection below. Since the CRC algorithm is rather complex, it is described in detail in the Appendix, Section 5.0.

Although the message E bits have been assigned the error reporting function for Command and Monitor Acknowledge messages, they have not been implemented.

There are three types of message error detection operations. First, the parity bit in each byte is analyzed by the receiving unit; any single bit error is detected and a flag set. The second level is the message CRC analysis and comparision described above. The CRC algorithm will detect any single-bit error and the probability of detecting a second erronous bit is 255/256. When an error is detected, the receiving unit sets an error flag. The third type of error detection has been implemented for Command messages. The PC control program compares the Command Acknowledge message Unit ID, Port 1 byte and Port 0 byte with those in the Command message just output. If the comparison shows a difference, the PC software assumes that there has been a transmission error.

In the event that a receiving unit detects a message error, there is no attempt to analyze the message contents to correct the error.

Message Protocol

Message protocol is the set of logical rules governing the generation, reception and usage of the command and monitor data messages. It is important to remember that the PC control program drives the system and the control interfaces only respond to the PC control program's stimulus.

Except when interrupted by a command from the telescope operator, the PC control program continuously operates all four buses in the monitor polling mode. Bus activities are completely independent and asynchronous and there are no common mode, time, address, etc., relationships between the bus signals.

Time is an important message protocol parameter; as noted above, the PC control program continuously polls monitor data from each control interface on the four buses and outputs telescope operator-generated commands. All the operations in these processes are time-dependent so the PC control program uses four timing terms to regulate the four bus's activities. The detailed steps in this time-ordered sequence are described in the Hardware-Software interactions paragraphs below.

The PC has a cassete interface that can be programmed to generate hardware interrupts at rates up to 1024 interrupts per second; this provides a time resolution of about 1 mS. The interrupt service routine is programmed to generate several timing terms that are used to time-regulate program functions. Commonly used timing terms are 1 pulse/450 milliseconds, 2 pulses/second, 1 pulse/second, 1 pulse/5 seconds, 1 pulse/5 seconds and 1 pulse/10 seconds.

Each bus has an independent 1 pulse/450 mS timing term that is used as a time-out clock for each stimulus message-response message interaction. The time required to transmit a message is about 183 mS, (55 bits at a rate of 300 baud). Interface interactions always involve two messages: a Command or Monitor request from the PC to the control interface and a Command or Monitor Acknowledge from the interface. The total transmission time for the two messages is thus about 367 mS so there is about 83 mS program execution time available for the PC and control interfaces. If the addressed control interface responds within the 450 mS period, the response message is analyzed and the data is stored. In the event that the addressed control interface does not respond within the time-out period, the interface is flagged non-responsive.

Although 450 mS is available for each PC-control interface message interaction, the actual message transmission-program execution times in the PC and control interfaces are slightly below this limit; so that when a PC-control interface interaction is completed, the PC control program proceeds to the next polling operation in the schedule without waiting for the end of the 450 mS period. As a result, bus activities are slightly faster than 2.2 interfaces interactions/second.

The control program continuously polls each arm for monitor data in a nine state sequential schedule: PN1, PN2, ... PN9, PN1, PN2, etc. in which time slot PN1 polls the closest antenna on an arm and PN9 polls the farthest antenna on an arm. After polling PN9, the sequence reverts to PN1 and continues. An important point is that the PN numbers are distinct from the Unit ID (antenna serial numbers) which range from 1 to 28. At the start of each of the nine polls in the sequence, the control program uses the PN number as an index in the configuration table to load the appropriate ID number into the Monitor Request message. A similar sequence is followed in polling the Auxiliary bus but PN6 is the last time slot in the sequence.

In polling monitor data, at the end of the 450 mS period, the PN number is incremented for the next Monitor Request message to be output. The PN number is related to the VLA WYE Monitor (main) screen described in the Telescope Operator Interface below. For each arm, the antenna screen and the associated E Stop screen switches are arranged in increasing distance order; the closest antenna is at the top of the column and the farthest antenna is at the bottom. For each column, the top switches designate PN1 and the bottom switches designate PN9.

In the PC control program, a bus's control mode is shifted to the command mode when the telescope operator inputs a command via the Touch Screen. The control program analyzes the command to identify the affected bus and formulates and outputs the command message. If a monitor data polling operation is active but incomplete, the command output operation pauses until the current monitor data input message operation has been completed. After completing the monitor data message input and storage cycle, the monitor polling sequence is interrupted and the control program emits the command message. After reception of the Command Acknowledge message, a Monitor Request message is sent to the control interface that had just been commanded to determine the device's state. This minimizes the latency time for verification of commanded states. After polling the commanded interface, monitor data polling resumes using the next sequential PN number.

When a command message is output on a bus, the other three busses continue to poll control interfaces for monitor data, unperturbed by the command message output on the affected bus.

When a control interface detects a Command message, it generates a Command Acknowledge message that is returned to the PC control program via the bus. The Command's Unit ID, Port 1 and Port 0 bits are returned as a "command echo" to enable the PC program to verify that the Command was correctly received. The Command Acknowledge message CRC will differ from the Command CRC because the Monitor Acknowledge message Sync character differs from the Command message Sync character.

When a Monitor Acknowledge message is received, the message data is stored in global common and the Operator Interfaces are updated with the message data.

Two antenna functions require the issuance of a double-command sequence; these are commands that set a state followed by a second command to reset the state. The second command is issued when the program receives the Command Acknowledge message for the first command. The ACU Reset command turns off the AC power to the ACU, which causes the ACU power supply to gradually discharge. Five seconds later, the second command re-connects the AC power and the ACU's power-on reset circuitry initiallizes the ACU logic. The second double-command function is the NCP breaker reset command. In this case, the second command is issued on the next cycle of the control program loop. See the hardware-software interactions description below.

Hardware-Software Interactions

The following software and firmware descriptions of the control PC, control interface and Watch Dog Timer programs are brief sketches that are intended to highlight major hardware-related program operations. The programs will be described in detail in another manual, Volume II.

Setting aside the control PC's operations with its internal components (hard disc, keyboard, etc.), the PC's hardware-software interactions are those involved in driving the buses, the Touch Screen and Annunciator.

The control PC's program operates continuously in a large loop that services the four bus serial ports, the Touch Screen, the annunciator and the printer port. Bus timing is regulated by the four dedicated 450 mSec software timers mentioned above. The loop operations are listed below in their sequential order.

1 Check for a pending Monitor Request or a Command message on any bus.

2 Have any command messages been sent?

3 Check the four buses for the return of any Command Acknowledge messages in response to Command message outputs. After reception of the Command Acknowledge message, monitor data polling is resumed but not at the PN number value that would have occurred if the command had not interrupted the sequence. The PN number for the next Monitor Request is that associated with the Unit ID value of the command that had just been output. After polling the commanded interface, monitor data polling continues with the next PN number and continues the polling sequence.

4 Check the four buses for the return of any Monitor Acknowledge messages in response to Monitor Request outputs.

5 When a Command Acknowledge or Monitor response has been detected on a bus, a flag is set in the current-pass arrays and data structures.

6 Compare the states of the current-pass arrays and data structures with the previous-pass arrays and data structures to see if a state change has occurred between passes. This is a test of the stability of the monitor data states reported by the control interfaces.

7 Process the Touch Screen interface to test for a new operator touch input. Start the process with the main screen and progress through the level 2 and level 3 screens to identify the required control action. This control action could cause a new command message to be sent to a control interface, call for a different Touch Screen display or squelch or clear the annunciator message.

8 Check to see if the second command of a dual command message sequence is to be output. If the command is not output at this time; step 14 causes the second command message to be output.

9 If it is a 1 PPS time, a second command of a dual command sequence is to be output. In the case of the ACU reset, this is a 5 second period.

10 If it is a 2 PPS time, strobe the printer port to signal PC program activity to the Watch-Dog Timer.

11 Also at a 2 PPS time, check to see if any alarms should be blinked. Alarms are blinked at a 2 PPS rate. Also check to see if a Kill/Voice input has colored a switch or indicator border red. If the Kill/Voice has been rescinded or cleared, remove the red border.

12 Process the abnormal and alarm states to determine if a voice message should be output to the annunciator. The voice message may be inhibited by the Kill/Voice switches.

13 Send a synchronization command to the Correlator and Computer UPS's if the generators have just been started. This causes the UPS's to synchronize their AC output to the generator's output.

14 Trigger the output of the second command for any pending dual-command sequences. Dual commands are unique to the antennas; there are no Auxiliary bus dual command sequences.

15 Move the contents of the current-pass arrays and data structures to the previous pass arrays and data structures.

16 If any key on the PC keyboard has been actuated, the program is stopped.

The control interface's hardware-firmware interactions are a response to the PC's Command and Monitor Request messages. In response to a Command message, the control interface's 87C51 firmware decodes the U Bits to determine if the interface is being addressed; if so, it then analyzes the message parity and formulates a CRC over the four message bytes for comparison with the message CRC byte. If the message is error free, the firmware sets the interface output lines (87C51 Ports 1 and 0) to the message's Port 1 and Port 0 states. It then formulates and outputs a Command Acknowledge message on the bus.

In responding to a Monitor Request message, the control interface's 87C51 firmware decodes the U Bits to determine if the interface is being addressed; if so, it then analyzes the message parity and formulates a CRC over the message contents for comparison with the message CRC. If the message is error free, it reads the device's interface lines state into Port 1 and Port 0, formulates the CRC, and outputs the Monitor Request message on the bus.

The Watch-Dog Timer module in the Control Room Interface bin also contains an 87C51 microcontroller; the 87C51 firmware executes the watch-dog timing and control functions. A watch-dog timer is a circuit that automatically invokes a reset unless the system being watched sends regular hold-off signals to the watch-dog. The Watch-Dog Timer's system function is to check the operation of the control PC program by checking the recurrence of the hold-off signal on the PC's parallel printer port. The hold-off signal is a character that is output at a rate of at least twice per second. The Watch Dog Timer initiates a PC reset sequence if it detects the loss of the hold-off signal within a one second period. The reset sequence has a 10 second pause to permit the telescope operator to invoke the maintenance mode, if desired. After the 10 second pause, the Watch-Dog Timer switches off the PC power for 10 seconds and then switches it back on to cause a power-on reboot. After turning on the PC power, the Watch-Dog Timer pauses 60 seconds before it resumes testing for the presence of the hold-off signal. If the reset attempt is unsuccesful, it is repeated and, if on the third reset attempt, the hold-off signal does not resume, the Watch-Dog Timer shifts to the alarm mode.

The Watch-Dog Timer is described in more detail in Section 2.6. The description includes a synopsis of the Watch-Dog Timer's firmware operations.

2.3 Telescope Operator Interface

As mentioned above, the telescope operator interface is both visual and audible. The visible portion of the interface is a Touch Screen CRT terminal that displays annotated control and display images that mimic conventional system control panels. The audible portion of the interface is an annunciator that pronounces voice messages that describe system states and alarm conditions.

The visual interface — the Touch Screen — is considered first. The Touch Screen images contain annotated psuedo-switches, psuedo-indicator lights and numeric displays grouped in labeled fields appropriate for the control function. The operator can enter a command by touching a fingertip to a psuedo control switch, just as is done on a conventional hardware control-display panel switch. Similarly, the psuedo-indicator lights and numeric displays show status and values, just as they would be displayed on a conventional hardware control-display panel. The control program assigns various solid and hatched colors to these switch, display and numeric indicator images and background as a function of the system command and monitor states. The color green in a switch or indicator signifies a non-fault or OK condition and red signifies an abnormal or fault condition. A blinking red signifies an antenna fault. Antenna Emergency Stop is red. Yellow signifies a stowed antenna. A border-hatched (with a band of broad diagonal black hatching around the periphery) switch or indicator signifies local control of the function. A gray color signifies a no-response condition from the associated control interface. If a control function's voice alarm has been disabled, the switch's border is outlined in red. See the annunciator inhibit description below. Some switches shift to a blue color for two seconds after actuation to show that the actuation caused a command to be sent to an antenna or some other device. Some switch actuations request a different screen and may not send out commands.

The control program provides a number of Touch Screen images arranged in heirarchal sets that are accessed from the highest level (main) image, the VLA WYE Monitor screen (Figure 1). These lower level images (called sub-screens) are accessed by touching any psuedo-switch. The accessed screen is inserted into the upper right corner of the VLA WYE Monitor screen and replaces the Master Emergency Stop, W Arm, N Arm, etc. switches and the "National Radio Astronomy Observatory" label. Figure 2 shows the Correlator UPS sub-screen inserted into the VLA WYE Monitor Screen. Psuedo-switches on theses sub-screens invoke commands or call up lower level sub-screens. Figures 3, 4, and 5 show typical sub-screens for the antennas, generators and other facility equipment. Note that these figures do not show every possible sub-screen; there are also similar sub-screens for identical equipment. Examples of such are sub-screens for other antennas, other arm-wide antenna functions and multiple identical facility units (e.g. generators and UPS's).

These sub-screens are the telescope operator's control and monitor interfaces for the VLA antenna and VLA facility systems equipment. There are thirteen types of level 2 sub-screens that can be accessed from the main screen and some systems have a third level sub-screen to provide an additional level of control expansion for complex systems. These other sub-screens are not described in detail in this manual but the equipment's functions are suggested by the annotations on the screen switches, lights and indicators. The control and monitor signals associated with these screens are described in the M26, M27 and M29 control interface application sections 2.9, 2.10, and 2.11. Drawing D13900B11 at the end of this section shows the screen hierarchy structure.

The VLA WYE Monitor (main) screen is the most complex and its usage typifies the operation of the other screens. The left side of Figure 1 has 9 antenna psuedo-switches for each arm in observing

pad order; these call up the antenna sub-screen (level 2) indicated by the antenna number. Emergency Stop psuedo-switches command the associated antenna Emergency Stop to be set. The antenna switches also show the antenna's observing location. At the top of these three columns are arm configuration switches labelled "West Arm", "North Arm" and "East Arm". These switches call up the Arm Configurator sub-screens described below.

Note that antenna E-Stop, ACU Reset and NCP Reset commands can be invoked on a single antenna basis (via an Antenna sub-screen) or on an arm-wide basis (via an Arm E-Stop, Arm ACU Reset and Arm NCP Reset sub-screens). In addition, the Emergency stop command can also be invoked on an array-wide basis via the Master E-Stop sub-screen. There are no comparable cases for the other VLA facility equipment.

A Date-Time switch above the three arm configuration switches shows the day, month, date, time (local time) and year. Touching this switch calls up the Set Date/Time screen to enable the operator to set in the appropriate values. This screen is described below.

A large Master Emergency Stop switch on the top right causes all antennas to be commanded to the Emergency Stop condition.

Below the Master Emergency Stop switch are three arm-associated switches: Emergency Stop, ACU Reset and NCP reset. The Emergency Stop switch causes all antennas on an arm to be set to the Emergency Stop condition. Similarly, the ACU Reset and NCP Reset switches cause all the ACU's and the NCP breakers on the arm to be reset.

Below the Arm-associated switches described above are eight switches that call up level 2 screens for major VLA systems components. These are: the ModComp control computers, the generators and switch gear (Master Cubicle), the computer and correlator UPS's, and the control building HVAC system.

The screens have provisions for control of the other portion of the telescope operator interface — the annunciator. The annunciator can be enabled or silenced in two ways; the main screen has a Clear Voice Alarms switch to reset all annunciator alarms. Secondly, some of the level 2 and level 3 screens have K/Voice switches that cause the associated alarm announcements to be squelched.

Level 2 and level 3 sub-screens have an Exit switch to return to the associated level 2 or main screens.

The main screen also shows the date and local time.

Several important level 3 sub-screens are the Transmission Log screens for major systems. These are system maintenance screens that show numeric values that characterize the quality of the WYE Monitor system message transmissions. The number of message transmissions, Acknowledge messages (both Command and Monitor), and No Response cases are shown on numeric indicators. The screens have a Clear Log switch that resets the indicators to zero and an Exit switch returns to the associated level 2 screen.

Two types of system configuration sub-screens are used to input reference data to the control program. The Set Date/Time sub-screen, activated by touching the Date-Time switch permits the telescope operator to input the year, date, month, day and local time to the program. This data appears in the upper

left side of the main (VLA WYE Monitor) screen. The West, East and North Arm Configurator sub-screens are activated when the operator touches the "West Arm", "North Arm" or "East Arm" switches above the antenna number-pad location columns on the top left side of the main screen. This Arm Configurator screen enables the telescope operator to quickly re-assign antennas to the observing pad locations during array reconfigurations. The antenna number-observing pad data is shown in increasing pad number order in the three antenna columns.

To relieve the operator from the necessity of constantly checking the Touch Screen displays, the annunciator alerts the operator when there are antenna and system facility equipment abnormal state or alarm conditions. The telescope operator can selectively squelch these voice alarms by touching the K/Voice switch on a sub-screen. The telescope operator can also clear all these voice alarms by touching the Clear Voice Alarm switch on the main screen.

The annunciator is a voice synthesizer that is driven by concatenated sets of vocal word synthesis files. The program formulates the voice file sets as a function of the program's abnormal state and alarm logic. A voice message start is signaled by a beep to alert the operator that a message is impending. A typical voice message might be: "Fire Alarm, West Arm, Antenna 22". The total set of annunciator message types roughly correspond to each type of command or monitor function implemented in the WYE Monitor system.

The voice message is repeated until either the alarm or abnormal condition is cleared or the operator actuates the associated K/Voice switch. If there is more than one voice message, the messages are repeated in a continuous sequence.

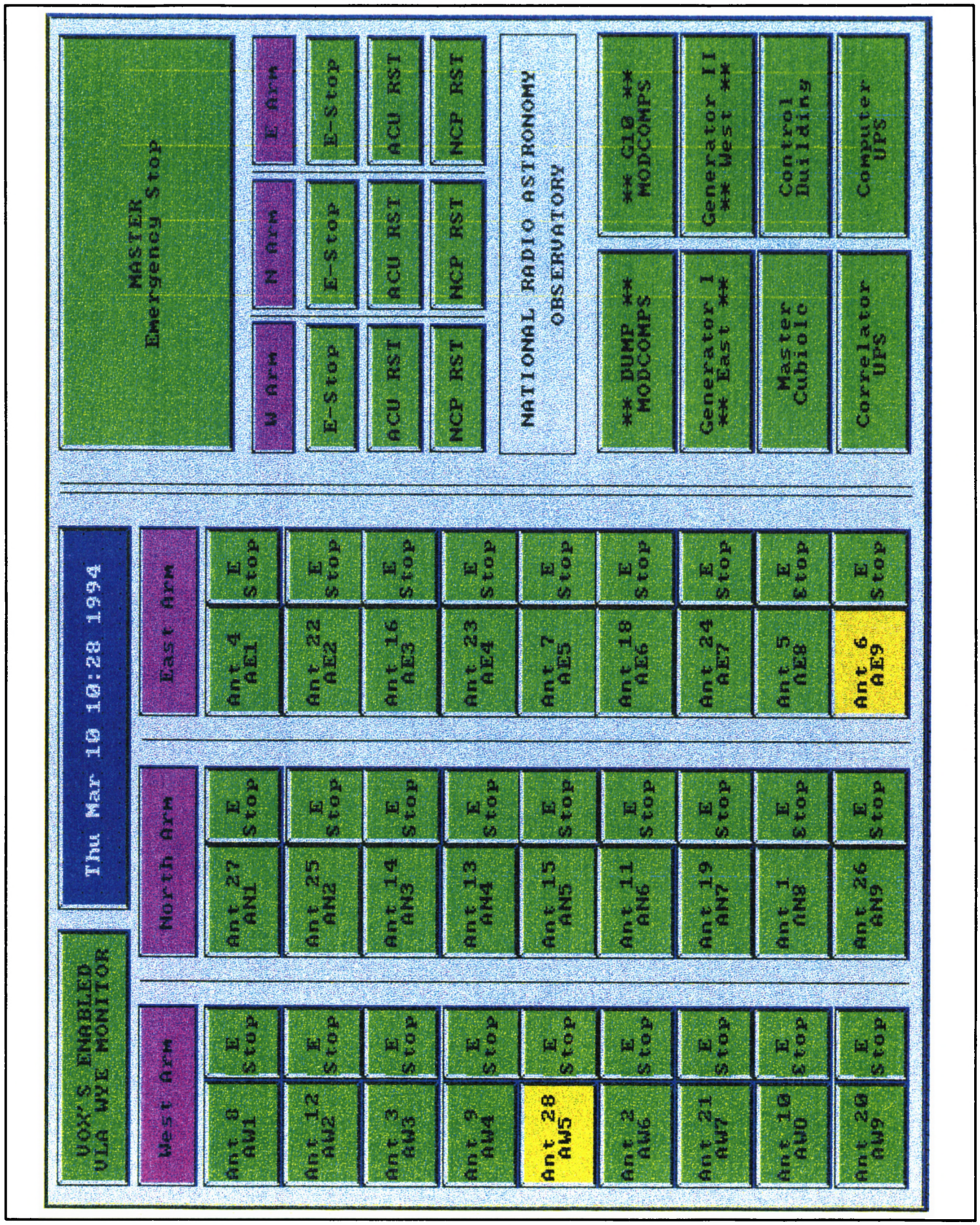


Figure 1 VLA WYE Monitor Screen

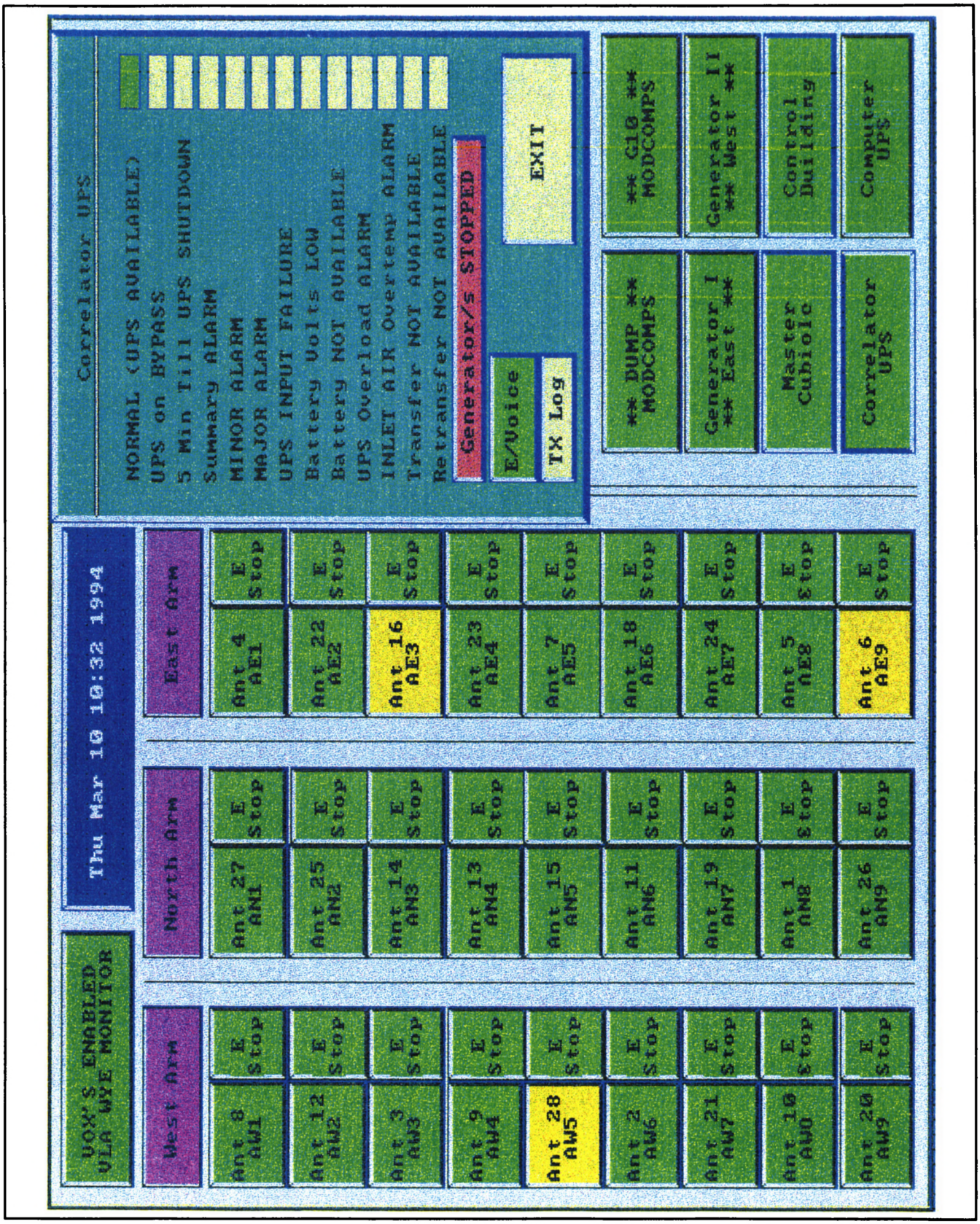


Figure 2 Correlator UPS Screen

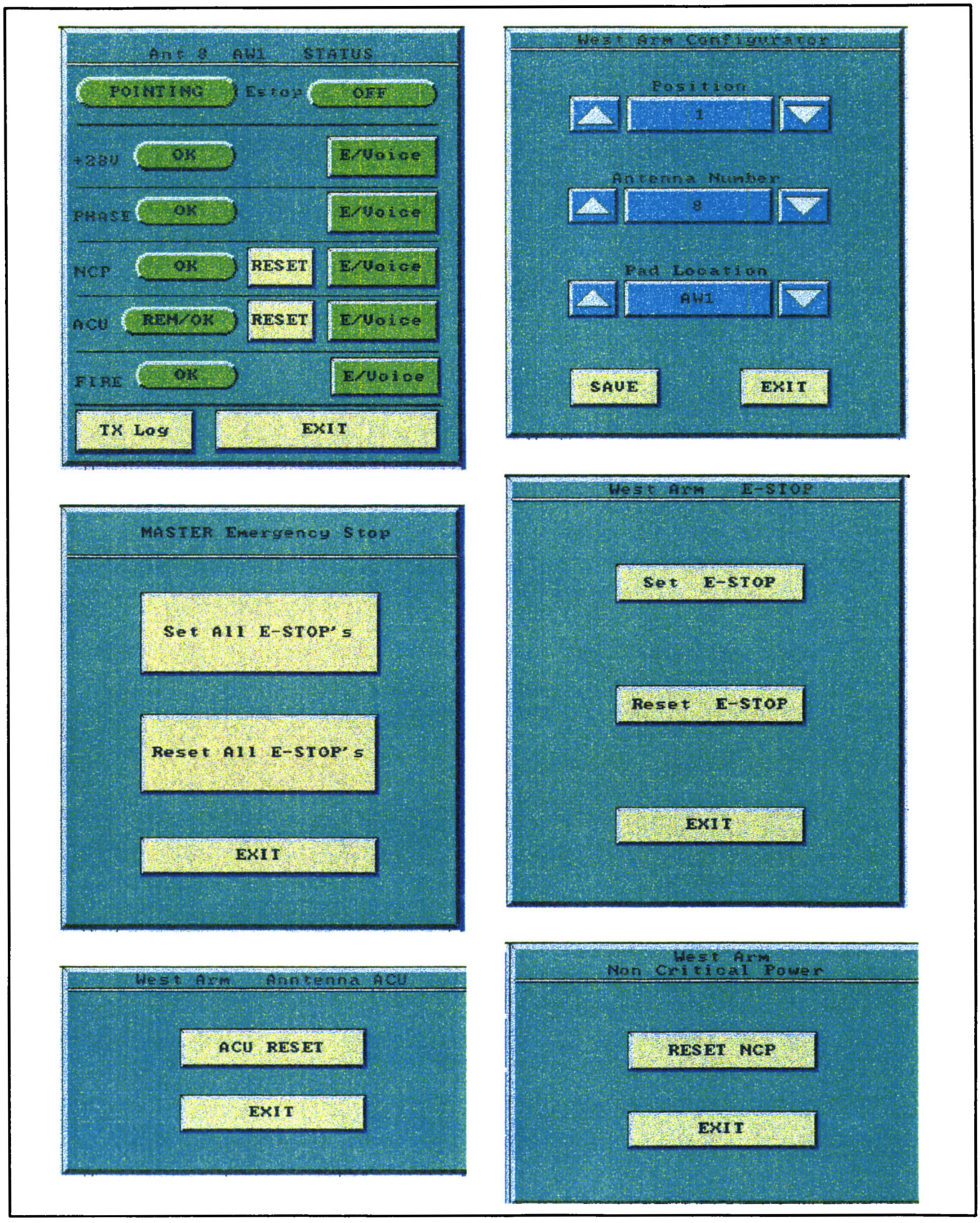


Figure 3 Typical Antenna Screens

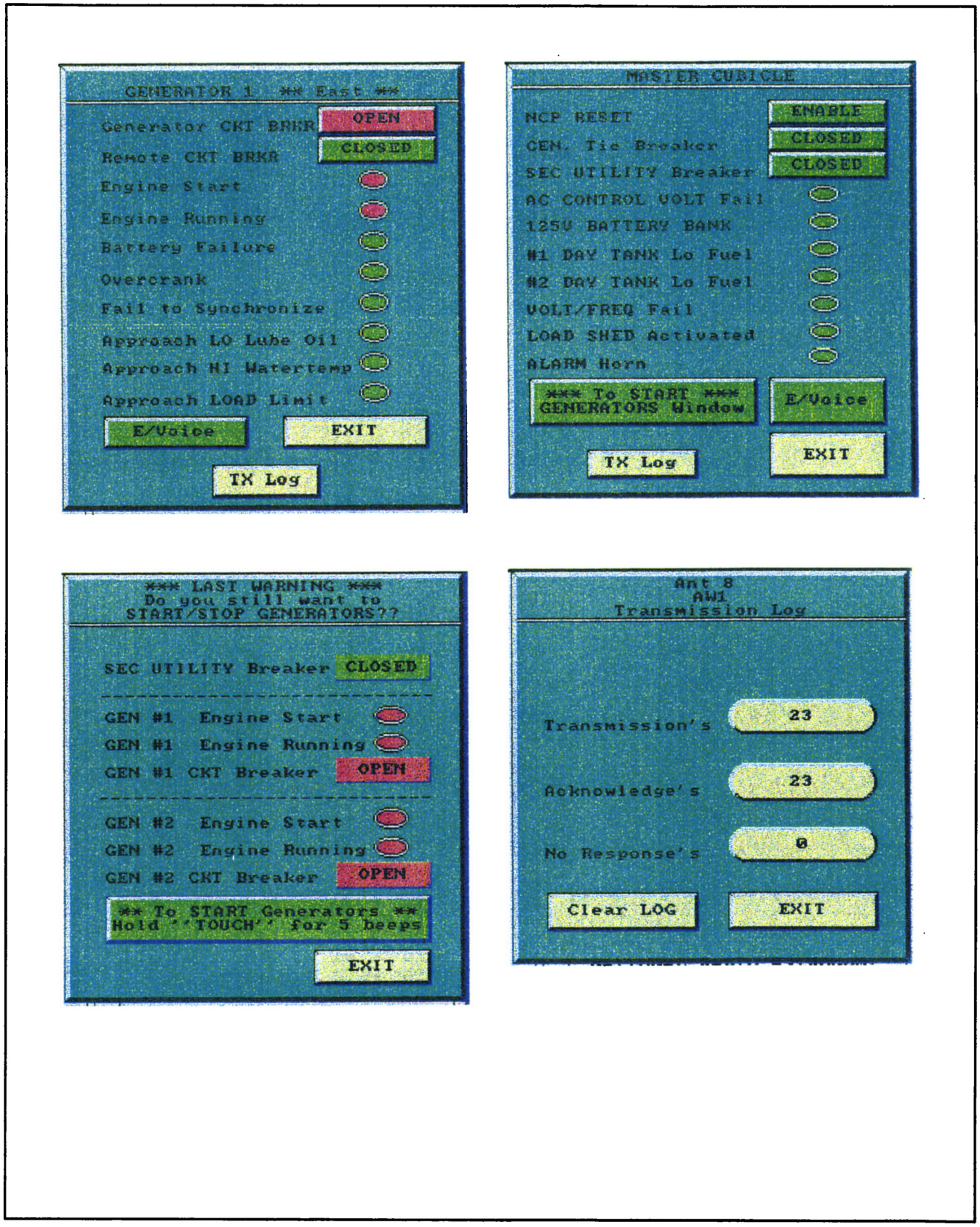


Figure 4 Typical Generator Screens

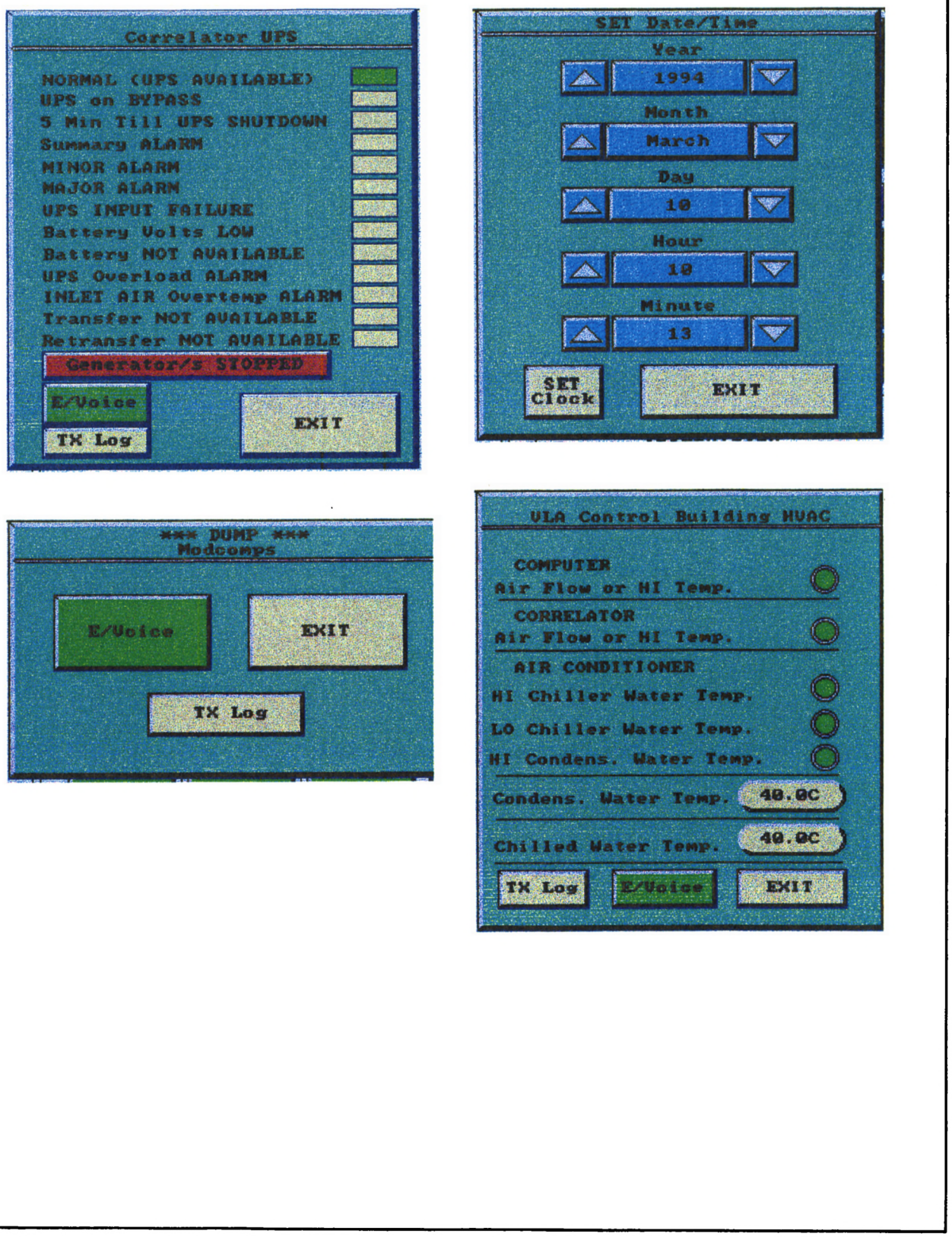
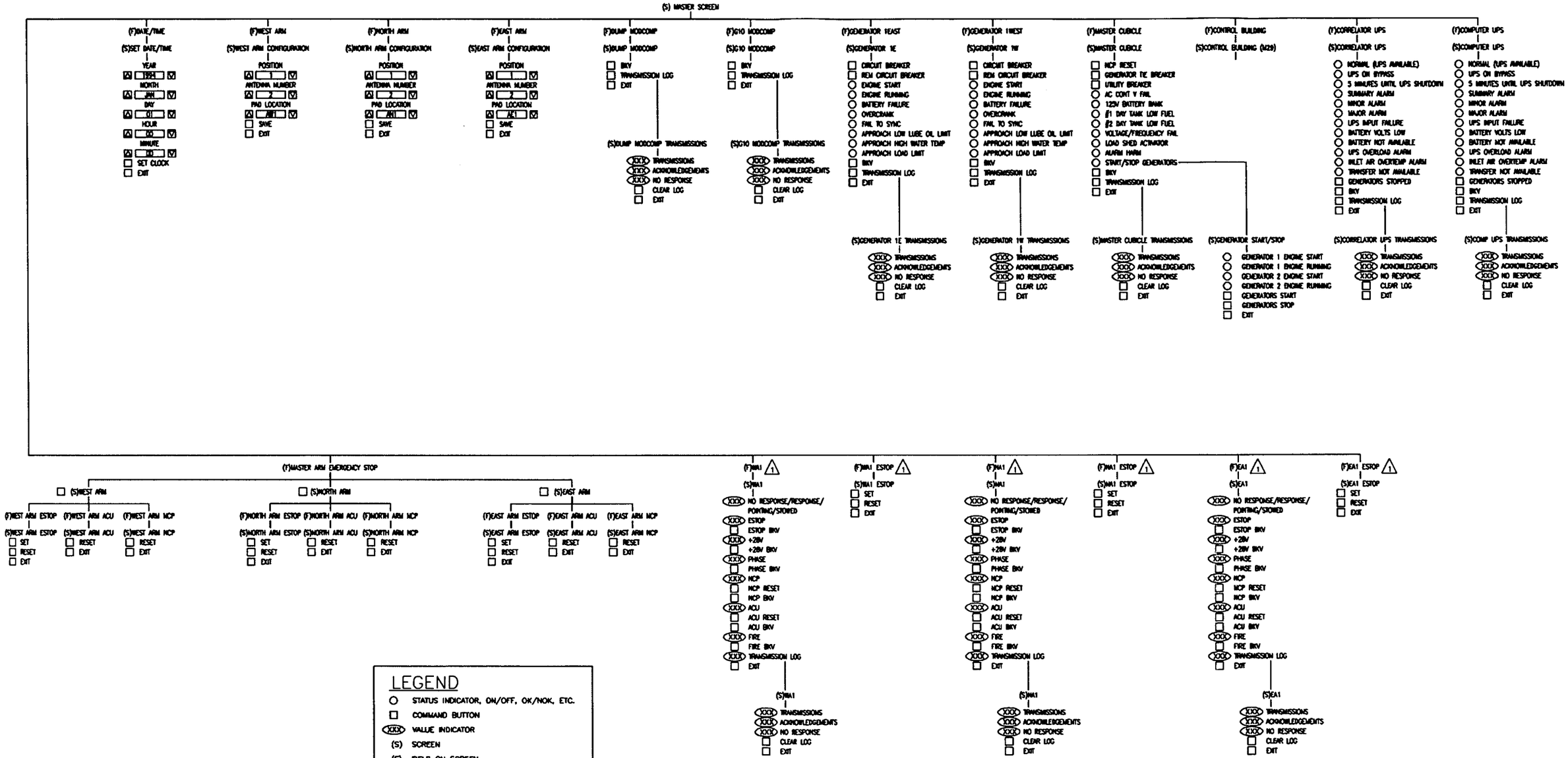


Figure 5 Typical Facility Screens

REV	DATE	DRAWN BY	APPR'V'D BY	DESCRIPTION

NOTES:

⚠1 INDENTICAL SCREENS EXIST FOR ALL 27 ANTENNAS.
ONLY ANTENNA 1 SCREENS ARE SHOWN FOR CLARITY



LEGEND

- ○ STATUS INDICATOR, ON/OFF, OK/NOK, ETC.
- □ COMMAND BUTTON
- (XXX) VALUE INDICATOR
- (S) SCREEN
- (F) FIELD ON SCREEN
- □ BKV – KILL VOICE MESSAGE

ACAD : 13900B11

NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL :

FINISH :

VLA PROJECT: WYE MONITOR

TITLE: WYE MONITOR TOUCH-SCREEN CONTROL/MONITOR MENU STRUCTURE BLOCK DIAGRAM

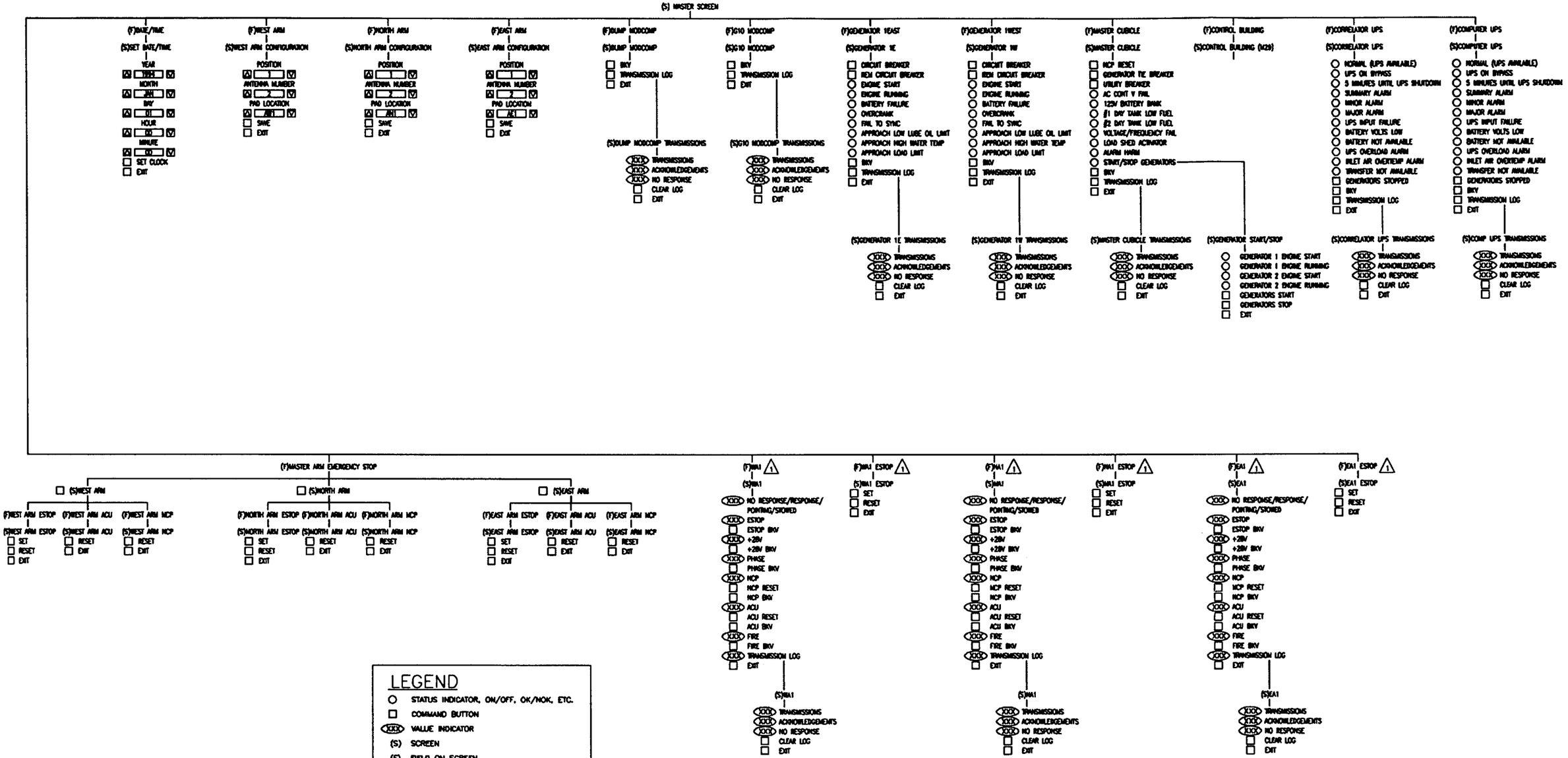
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 5-94
DESIGNED BY	DATE 5-94
APPROVED BY	DATE 5-94

SHEET NUMBER 1 of 1 | DRAWING NUMBER D13900B11 | REV. – | SCALE NONE

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

NOTES:
1. IDENTICAL SCREENS EXIST FOR ALL 27 ANTENNAS. ONLY ANTENNA 1 SCREENS ARE SHOWN FOR CLARITY



LEGEND

- ○ STATUS INDICATOR, ON/OFF, OK/NOK, ETC.
- □ COMMAND BUTTON
- (XXX) VALUE INDICATOR
- (S) SCREEN
- (F) FIELD ON SCREEN
- □ BKV – KILL VOICE MESSAGE

ACAD : 13900B11

NEXT ASSEMBLY	DWG. TYPE	MATERIAL :	
		FINISH :	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

VLA

WYE MONITOR

WYE MONITOR TOUCH-SCREEN CONTROL/MONITOR MENU STRUCTURE BLOCK DIAGRAM

SHEET NUMBER 1 OF 1 | DRAWING NUMBER D13900B11 | REV. — | SCALE NONE

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 5-94
DESIGNED BY	DATE 5-94
APPROVED BY	DATE 5-94

2.4 Bus Signal Driving and Receiving

Bus line driving and receiving are important functions because all control actions are conveyed by the bus lines in the long (up to 13 miles) WYE COMM system cables. It would have been virtually impossible to use conventional commercial digital line drivers and receivers for cable runs of this length and the problem is compounded by high cable shunt capacitance, high series resistance, low leakage resistance to ground and occasional surge voltages. Repeater amplifiers on the observing arms were considered during the design effort but they would have increased operational and circuit complexity, so they were rejected. Unconventional driver/receiver implementations were devised to deal with these problems.

Bus signal transmission and reception are differential to reduce common-mode inteference signal effects. The drivers are connected to the bus only when necessary for message transmission and the receiver circuits are optically-isolated from the control interface's logic circuitry. As a result, the PC and control interfaces are totally isolated from each other and from any grounds. In addition, the bus lines are each driven by powerful, opposite-polarity 30 volt signals (60 volt differential) to compensate for line loss and a slow data rate (300 baud) is used to charge and discharge the large bus line capacitance.

Only two types of circuit boards interact with the buses — the Isolated CPU Interface board (C13900S03) used in the control interface modules and the PC Transceiver board (C13900S02) used to translate the PC's RS-232 levels to the system bus levels. The WYE Monitor PC Transceiver is described in Section 2.7 and the WYE Monitor Isolated CPU Interface is described in Section 2.8.

Bus Conditions

The WYE-COMM cables are 25-pair, #22 AWG twisted-pair, unshielded cables that have high series resistance (22.25 Ω/1000 loop-feet), high shunt capacitance (about 20 pF/foot), and an impedance of about 100 Ohms (estimated). The bus lines are not terminated at the ends of the run. There is also a potential for crosstalk from the WYE-COMM voice signals. Cross-talk coupling is not specified and roughly varies as a function of the cable lay (number of twists/foot), proximity of the pairs and length of the cable run. Cross-talk levels as high as about 0.5 VRMS have been measured on some of the pairs. Lightning strikes to the earth, antennas, tracks and buildings can induce high voltage spikes in the cables as a result of couplings between the cables and antennas, railroad track and buildings. These high voltage spike levels have not been measured but are an important design consideration. Drawing C13900S05 is a model based upon recent measurements of the west arm cable at "A" array stations. The loop resistance from the Control Building to AW9 is 3106 Ω and the shunt capacitance is 1.21 to 1.25 μF; pair shunt resistance, leakage to other pairs and earth ground is not specified. West Arm WYE COMM drawing D13900B02 (circa 1981) shows similar loop resistance values. The east arm values are probably similar since it is about the same length as the west arm and the north arm values are somewhat less because the length is about 11 miles.

Bus Surge Voltage Limiting

Although lightning-induced voltages and energies are not quantified, VLA experience has shown that voltage surges can damage equipment. Three-terminal, semiconductor threshold voltage surge arrestors (P1602 Sidactors) in the control interfaces at each antenna or device drop point are triggered into conduction when a bus lines exceeds a threshold of 60 to 90 volts. The Sidactors are connected from each

line to ground. In conduction, the P1602 forward drop is about 1.5 volts and the peak current can be as high as 400 Amperes — these arrestors can dump a lot of energy to ground. The Sidactor's typical response time is about 1 nS. The surge arrestor's peak current is limited by the cable's series resistance as a function of the distance between the interfaces and the place where the voltage spike is induced. The combination of surge arrestors and the cable's distributed shunt capacitance and resistance tends to dampen cable voltage spikes. After a year's service, there have not been any control interface failures, which suggests that these devices provide effective protection.

The bus interface circuitry on the WYE Monitor Isolated CPU Interface Board (C13900S03, used in each control interface) shows MOV's (metallic oxide varistors) connected across the bus lines and from each line to ground. The MOV's are not installed but the board has provisions to install them if required. Operational experience has not shown a need for additional surge limiting measures.

The WYE Monitor PC Transciever module PC board (C13900S02) has K680 MOV's connected across the two bus lines and from each bus line to ground. The P1602 Sidactor used on the WYE Monitor Isolated CPU Interface are not used on the WYE Monitor PC Transceiver board.

Bus States

The bus lines always float relative to earth ground and line voltage levels are limited by the 60-volt threshold Sidactors described above. The buses can only have three states: inactive, a "1" state or a "0" state; the levels are described below. The buses are inactive between message transmissions and all drivers are disconnected from the bus lines. To prevent line noise perturbations to the receiving circuitry, the lines are biased to the "0" state in each receiving circuit by 51 kΩ resistors to the isolated power supply outputs; this pulls Line+ to -15 volts and Line- to +15 volts so that there is 30 volts across the lines.

Bus Drive Circuitry

The bus lines are each driven by opposite-polarity 30 volt signals powered by the driving unit's ± 15 volt power supply. If a "1" is being transmitted, Line+ is -15V and Line- is +15V and if a "0" is being transmitted, Line+ is +15V and Line- is -15V. The power supply is a Burr-Brown HPR105 powered by the module's 5 volt power supply. The HPR105 supply outputs are isolated from the input +5V and 5V common - an important requirement discussed below. The schematic designates the supply's +15V and -15V outputs as +15I and -15I and the ±15V Common is designated 0I.

Refer to drawing C13900S03, which is the schematic of the Isolated CPU Interface Interface Board. Each bus line is driven by a pair of optical isolators (OPTO1A/OPTO1B and OPTO1C/OPTO1D) that switch the + 15V or - 15V outputs of the isolated dual 15 volt power supply onto the lines as a function of the drive logic and bit state to be output. The power supply common is not ground-referenced to the line drivers; only the +15V and - 15V outputs are used by the optical isolator line drivers. Since the lines are switched between these two outputs, each bit change causes a 30 volt bus line swing. Since the 30 volt signal swings have opposite polarities, **for each bit change**, the **differential** signal swing across the lines is 60 volts.

As a result of the use of optical isolator bus drives, only the active interface driver is coupled to the bus; all the other drivers are isolated from the bus. The optical isolator photo transistors have a small leakage current, about 100 nA maximum at 25°C and V_{CE} = 40 volts.

The low-true TX ENABLE (87C51 WR-) enables the isolator drive via U2D to U2C-9 and U2B-5; this term is true only when the TXDATA is active during the 87C51's serial port byte output. The high-true TXDATA (87C51 TXD) data drives U2A and the inverted data (by U2A) drives U2B. Thus, either U2C or U2B sinks current as a function of the data bit state. If the TXDATA bit is a 1, U2C is active low and sinks current through the OPTO1C and OPTO1B LED's; this asserts -15I onto LINE+ and +15I onto LINE- via the isolator's output transistors. If the TXDATA is a 0, U2B is active low and sinks current through OPTO1D and OPTO1A LED's; this asserts +15I onto LINE+ and -15I onto LINE- via the isolator's output transistors. The 150 Ω resistors to VCC limit the isolator diode currents to about 12 mA.

During inactive periods between message transmissions and the intervals between a serial port's byte transmission, TX ENABLE, is low which sets gates U2C and U2B to the inactive-high state so that none of the optical isolators is sinking current. This state disconnects the optical isolator outputs from the bus lines.

The line driving circuitry in the WYE MONITOR PC TRANSCEIVER (C13900S02) is identical to that described above except the transmit enable is the RTS (Request To Send) line from the MAX233 RS-232 to TTL converter.

The NEC PS2501-4 optical isolator on-off switching delay times are typically about 3 μS, respectively; this delay is very small relative to the 3.33 mS data bit period.

As mentioned above, the bus lines may be subjected to voltage surges; the PS2501-4 optical isolators are capable of maintaining isolation with 1500 volts between the LED inputs and transistor outputs. The high voltage isolation of the Burr-Brown HPR105 power supply is 750 volts, peak for 10 seconds between the +5 volt and common inputs and the +15V, ±Common and -15V outputs.

Bus Signal Waveform

The bus lines are lossy transmission lines and drawing C13900S05 is a lumped-constant model of the west arm bus in the A array. The model values were measured at the stations noted.

The simplest model for the signal seen at the last A-array antenna on the west arm bus line is the output of an RC low pass filter where R = 3100 Ω and C = 1.2 μF — the values from C13900S05. The RC time constant is 3.6 mS and the period of a 300 baud bit is 3.33 mS, about the same as the RC time constant. An alternating 1 and 0 data signal input to the filter would be a 60 volt square wave with a 6.6 mS period. The output across the capacitor would be a simple, almost linear sawtooth function with a peak-to-peak amplitude of about 60% of the square wave input, about 37 volts. This simple RC low-pass filter model roughly represents the worst case of signal degradation on the arm and the AW9 signal waveform resembles the output of this model. Starting at AW9, observations of the signal waveform at each successive inbound station show step-like increases in amplitude and reductions in the capacitive loading.

Bus Receive Circuitry

The receiving circuitry of the Isolated CPU Interface is shown on C13900S03. The PC Transceiver receiving circuitry shown on C13900S02 is virtually identical to that in the Isolated CPU Interface.

The signal receivers use an open-loop operational amplifier as a bit sense detector. Three 330 kΩ resistors are bridged across the bus line. The amplifier's + and - inputs are connected across the center 330 kΩ resistor — an unconventional connection that puts about a third of the line signal difference across the inputs. Since the OP-15 operational amplifiers use JFET input transistors, they are capable of operation with inputs as high as ± 20 volts and a differential input as high as ± 40 volts. The first station on a bus will have the greatest signal amplitude and the levels at the two OP-15 inputs are + and - 5 volts, so the amplifier inputs are not voltage-stressed. The operational amplifier does not use feedback so the amplifier output is at either the + or - saturation levels of about ±13 volts as a function of the data bit state. The only time that the output is not at either extreme is the brief period when the difference between the inputs is zero volts during the signal's ramp-up or ramp-down slope. During this period the output swings from one saturation level to the other as a function of the sequence of bus data states.

Since each receive circuit's load across the bus is 1 megOhm, the total load imposed by all antenna receive circuits is only 111 kΩ.

The amplifier output sources current into the LED anode of OPTO2 through a 10 kΩ limiting resistor. The LED cathode is connected to the analog power suppy common, 0I. A 1N914 diode across the LED clamps the anode to -0.6 volts when the amplifier output is negative. The LED conducts when the amplifier output is greater than about +1.4 volts. When the LED conducts, OPTO2's output is low and gate U6A-3 is also low if enabled by the low-true drive from U2D-11 — the inversion of TX ENABLE. This receive enable is low at all times except when the interface is transmitting.

For interfaces near the control building when the bus signal is a "1", the amplifier's + input is about -5 volts, the - input is at +5 volts and the amplifier output is -13 volts. Gate U6A's output (RX DATA) is a high (a "1") which is input to the 87C51 RXD serial port input. When the bus signal is a "0", the amplifier's + input is about +5 volts, the - input is -5 volts and the amplifier output is +13 volts; thus gate U6A's output is a "0". In the case of an interface at the end of the arm, the amplifier's + and - inputs are reduced to about - and + 3 volts (peak) for a "1" and "0", respectively.

OPTO2 isolates the ampifier and power supply from the interface board's logic circuitry - an important requirement. The driver circuit and all interface's receive circuits are thus isolated from any interface's logic common. This eliminates any common-mode signal perturbations to bus receive circuitry.

When the bus is in the inactive state, all optoisolator drivers are disconnected from the bus which would leave both lines free to float around zero volts. This is an undesireable condition because the OP-15 inputs would follow the two line's noise voltages and the output would flip between + and - 13 volts. The line noise is principally audio frequency crosstalk from WYE-COMM cable voice lines. The modem frequency is 300 Hz; inevitably, the 87C51 UART receive circuitry would be randomly triggered by this audio crosstalk which could result in apparent error-contaminated message bytes. To avoid this problem, the lines are biased to the "0" state by 51 kΩ resistors connected to the isolated power supply outputs. In this state, the 51 kΩ resistor connected to -15I on the LINE+ and the 51 kΩ resistor connected to +15I on the LINE- bias the amplifier's output to +13 volts, the "0" state.

The 51 kΩ bias resistors in series with the three 330 kΩ resistors impose a current drain of 27 micro-Amperes on each isolated power supply. In the inactive and "0" states, the voltage drop across a 51 kΩ resistor is about 1.4 volts; thus the line voltages are each about 13.6 volts (relative to 0I) rather than the nominal 15 volt levels. Note that no current flows between the receive circuits for any line state because the interface's isolated DC-DC converter are isolated from ground.

During bus voltage surges, the operational amplifier floats at the line potential and is not stressed because its power is isolated from the interface module's logic circuitry.

RS-232/Bus Level Conversion

The control PC is the signal nexus of the four buses and uses a four-port RS-232 serial interface board. RS-232 signal standards were established for short-run, single-ended serial communications on cable lengths up to 15 meters and with transmit levels of ± 5V min to ± 15V max; positive voltages are a "0" and negative voltages are a "1". The receive thresholds are ± 3V. The RS-232 signal domain is inappropiate for transmission on the long WYE COMM system cables because of the cable's high resistance and capacitance.

Since standard commercial PC serial port boards use the RS-232 signal standard, the most economical RS-232 to bus level implementation is external to the PC; this is done in the WYE Monitor PC Transceiver boards (C13900P13) in the control room WYE Monitor PC Interface Bin Assembly (D13900P09). Four transceiver boards are used; one for each of the three buses.

A MAX233 RS-232 to TTL chip performs the signal transformation. The PC's RTS (Request to Send) term is transformed to TTL and enables the transceiver's bus drive circuitry in a manner similar to the TX ENABLE in the Isolated CPU Interface Board in the control interface units. The PC's RX and TX serial data terms are also transformed by the MAX233. The MAX233 is powered by the transceiver's logic power and has an internal flying capacitor power supply to supply the ±9 volt power used for RS-232 signal interfacing. The MAX233 has built-in filter capacitors and can supply + and -9V for small external loads.

The MAX233 transmit and receive circuits both invert the input signals. The receive circuits have about 0.5 volt volt hysteresis to reduce sensitivity to line noise effects.

After the three RS-232 PC terms have been transformed to TTL, they are input to the bus drive and receive circuits, similar to those described above.

Bus Driving Component Data Sheets

Data sheets for the P1602 Sidactors, the Burr-Brown HPR105 power supply, NEC PS2501-4 optical isolators, the OP-15 amplifier and the Maxim 233 RS-232 converter are included in Section 5.

Bus Transmission Errors

As in any long-haul digital transmission system, transmission rate is traded for bus length. Because of the large cable shunt capacitance with a transmission rate of 300 baud, the peak signal at the end of the 13 mile cable runs is about 60% of the signal level transmitted by the PC's line drivers. Repeater amplifiers on the observing arms were considered during the design effort, but they would have increased the operational and circuit complexity, so they were rejected. During development, experiments showed that the 300 baud transmission rate provided high reliability communications and a transmission rate of 600 baud is marginal. With a 300 baud transmission rate, monitored functions are each sampled at a 4 second rate; this is roughly the Telescope Operator's problem analysis and response time.

Transmission Log screens were briefly described in the Operator Interface discussion. The error analysis software and screens were developed to evaluate transmission reliability during system development and have been retained for maintenance purposes. In normal operation, transmission error rates (parity and no-response) are vanishingly small and have not been quantified. A few errors may occur during intense lightning storms and errors may also occur when antennas are being connected and disconnected during array reconfigurations.

2.5 87C51FA Micontroller Description

This section is a highlight description of the characteristics of the Intel 87C51FA microcontroller that are important to its use in the Isolated CPU Interface and the Watch-Dog Timer.

The 87C51FA is a member of the eight-bit Intel MCS-51 microcontroller family. The architecture is shown in Figure 6, next page. For a detailed description of the chip's characteristics, refer to the 87C51FA data sheets in Section 5. The 87C51FA has four 8-bit bidirectional parallel I/O ports, three timer/counters (Timer 0, 1 and 2), a programmable timer/counter array (PCA), a 256 byte on-chip RAM memory, an 8 Kbyte on-chip EPROM program memory, a full-duplex programmable serial I/O port, an interrupt structure with seven interruput sources, and power saving modes. The timer/counters, serial interface and interrupt features are controlled by a bank of Special Function Registers shown in Figure 5 as a block labelled SFRs, Timers, P.C.A. Figure 7 shows the SFRs, their addresses, and their state following a reset. The B register, Accumulator, I/O Ports and PSW addresses fall within the SFR block.

The MCS-51 series of microcontrollers was designed for control applications and has many convenient features for this class of usage. These features include programmable timer/counters, a programmable counter/timer array (PCA), a serial port and an interrupt system. In a typical application, one of the timers may be used as a baud-rate generator for the serial port and the others may be used as event counters, clock rate generators and watch-dog timers. Other valuable features are the use of separate program and data memories, a seven-source interrupt structure with two priority levels, four 8-bit I/O ports, a Boolean processor, and an Accumulator parity bit in the Program Status Word (convenient for serial transmissions). A portion of the on-chip RAM memory is bit addressable for convenient state manipulations. RAM memory provides four selectable bands of registers for operands storage and a stack for interrupt service storage. I/O ports are both byte and bit addressable. The bit-addressable I/O port property makes it easy to manipulate I/O port lines as discretes without having to perform byte mask-merge operations. I/O Port pins may be assigned to alternate functions such as interrupt inputs rather than standard I/O bit functions. Program and data memory are in separate address spaces and may be as large as 64 Kilobytes.

This description is restricted to chip features such as I/O ports, timer/counters, and the interrupt system. Emphasis is given to the operating modes of the timer/counters, PCA, and serial port; the intent is to describe only those features and modes that are relevant to the 87C51's functions in the WYE Monitor system. A brief review of the 87C51FA data sheets shows that the timer/counters, PCA, and serial port have many modes and combinations of these modes. Refer to the 87C51FA data sheets for a complete description of the other modes of the timer/counters, PCA, serial port, and the characteristics of the 87C51. Although chip architecture, registers, instruction types, program and data memory, address modes, instruction timing, etc. are very important topics, they are conventional and are adequately described in Section 5; there is no need to repeat the description.

The following description shows how the mode and control SFRs of these features are **set up or initialized but does not describe the firmware program's usage** of these features. In addition, the 87C51FA instruction set, assembly language programming techniques, and EPROM programming are not discussed. Lastly, the two firmware programs are not described; these are the subject of another manual.

In both applications, the 87C51FA clock is an on-chip oscillator that uses an external 11.0592 Mhz crystal. In the Isolated CPU Interface, Timer 0 and the PCA use a programmed subdivision of this clock

for I/O port sampling and to drive the MAX695 Watch-Dog Timer chip. Using this clock, Timer 1 functions as a baud-rate generator for the serial port transmit and receive clocks.

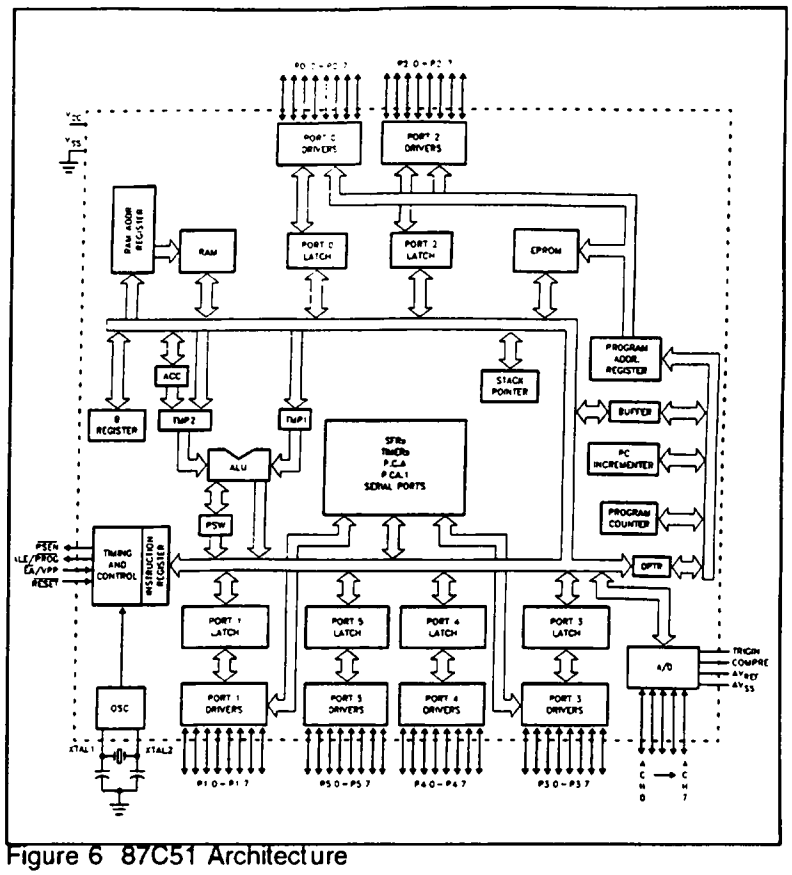


Figure 6 87C51 Architecture

Special Function Registers

Special Function Registers (SFR's) control the modes and operation of the timer/counters, PCA, serial port, and interrupt system. Arguments and values for these functions are stored as data in the SFR's. Some SFR's (e.g. IP, IE, T2CON and SCON) are both bit and byte addressable. The timers and PCA modes are controlled by mode registers (e.g. TMOD, T2MOD and CMOD) and they are turned on and off by control registers (e.g. TCON, T2CON and CCON). Thus TMOD's state determines the modes of timers 0 and 1 and TCON turns the timers on and off. SCON controls both the mode and operation of the serial port. Some SFRs (TL0, TH0, RCAP2L, RCAP2H, CCAP0L, CCAP0H, etc.) contain compare or count values for the timers and PCA. The SMOD1 bit in PCON causes the serial port baud rate to be doubled. Control bits in T2CON select timer/counter 1 or 2 as the clock for the serial port. The IE register enables the interrupts, some of which are the result of timer overflow. The IP register establishes the priority of the six interrupt sources. The functions performed by these SFR mode and control registers are mentioned here to introduce their function. The text below describes the way that the SFR mode and control registers control the timer/counters, PCA, serial port, and interrupt system. Figure 7, (next page) shows the SFR mapping and reset values.

I/O Ports

In the Isolated CPU Interface and Watch-Dog Timer module, the port 0 and port 1 latches are convenient state memories for command state outputs. The Isolated CPU Interface uses five, port 2 bits in the input mode to read the hard-wired antenna ID value, i.e. antenna serial number code. The Watch-Dog Timer module uses port 2.7 in the output mode to clock the MAX695 WDI (watch-dog input), port 2.6 in the output mode to reset the 74LS74 flip flop, and port 2.0 in the input mode to sense the Quiet switch state.

All four 87C51 I/O ports (Figure 8, next page) are bidirectional and each port bit can be individually set to input or output. Each port bit consists of a latch (SFR's P0 through P3), an output driver, and an input buffer. Ports 1, 2 and 3 have internal pullups. Port 0 has open drain outputs. The

pullup FET in the Port 0 output driver is used only when the port is emitting 1's during external memory accesses; otherwise the pullup FET is off. Port 0 output buffers can sink 3.2 mA at 0.45 volts. Ports 1, 2 and 3 output buffers can sink 1.6 mA at 0.45 volts. The control interface modules use Port 0 for command outputs because of the Port's higher drive capabilities.

F8	P5 00000000	CH 00000000	CCAP0H XXXXXXXX	CCAP1H XXXXXXXX	CCAP2H XXXXXXXX	CCAP3H XXXXXXXX	CCAP4H XXXXXXXX		FF
F0	*B 00000000				AD7 00000000			SEPSTAT XXXXX000	F7
E8	C1CON 00000000	CL 00000000	CCAP0L XXXXXXXX	CCAP1L XXXXXXXX	CCAP2L XXXXXXXX	CCAP3L XXXXXXXX	CCAP4L XXXXXXXX		EF
E0	*ACC 00000000				AD6 00000000			SEPDAT XXXXXXXX	E7
D8	CCON 00X00000	CMOD 00XXX000	CCAPM0 X0000000	CCAPM1 X0000000	CCAPM2 X0000000	CCAPM3 X0000000	CCAPM4 X0000000		DF
D0	*PSW 00000000				AD5 00000000			SEPCON XX000000	D7
C8	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			CF
C0	P4 00000000				AD4 00000000		EXICON X0000000	ACMP 00000000	C7
B8	*IP X0000000	SADEN 00000000	C1CAP0H XXXXXXXX	C1CAP1H XXXXXXXX	C1CAP2H XXXXXXXX	C1CAP3H XXXXXXXX	C1CAP4H XXXXXXXX	CH1 00000000	BF
B0	*P3 11111111				AD3 00000000	IPAH 00000000	IPA 00000000	IPH X0000000	B7
A8	*IE 00000000	SADDR 00000000	C1CAP0L XXXXXXXX	C1CAP1L XXXXXXXX	C1CAP2L XXXXXXXX	C1CAP3L XXXXXXXX	C1CAP4L XXXXXXXX	CL1 00000000	AF
A0	*P2 00000000				AD2 00000000	OSCR XXXXXXX0	WDTRST XXXXXXXX	IEA 00000000	A7
98	*SCON 00000000	*SBUF XXXXXXXX	C1CAPM0 X0000000	C1CAPM1 X0000000	C1CAPM2 X0000000	C1CAPM3 X0000000	C1CAPM4 X0000000	C1MOD XXXX0000	9F
90	*P1 00000000				AD1 00000000			ACON XX000000	97
88	*TCON 00000000	*TMOD 00000000	*TL0 00000000	*TL1 00000000	*TH0 00000000	*TH1 00000000			8F
80	*P0 11111111	*SP 00000111	*DPL 00000000	*DPH 00000000	AD0 00000000			*PCON** 00XX0000	87

* = Found in the 8051 core (see 8051 Hardware Description for explanations of these SFRs).
** = See description of PCON SFR. Bit PCON.4 is not affected by reset.
X = Undefined.

Figure 7 87C51 Special Function Registers

The 87C51's bidirectinal I/O ports are used as parallel interfaces by the Isolated CPU Interface Board. All the Port 1 and Port 3 pins are multifunctional. They are not only port pins, but also serve the functions of various special features listed below. The alternate functions are activated when the corresponding latch in the port SFR contains a 1; otherwise the port pin is stuck at 0.

The output drivers of Ports 0 and 2 and the input buffers of Port 0 are used in accesses to external memory. In this usage, Port 0 outputs the low byte of the external memory address, time-multiplexed with the byte being written or read. In the two WYE Monitor applications, the program memory is an on-chip EPROM, therefore these ports are not used as a multiplexed address-data bus.

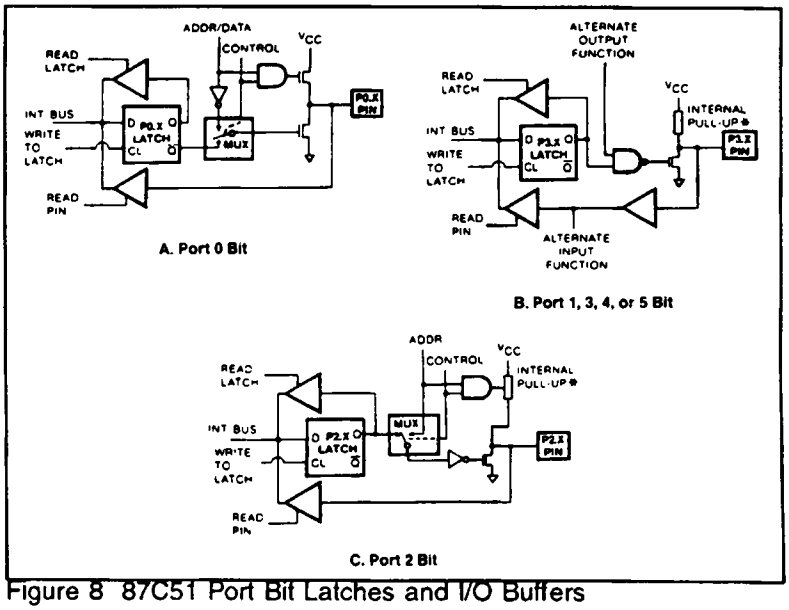


Figure 8 87C51 Port Bit Latches and I/O Buffers

Some instructions that read a port read the latch and others read the pin. Which ones do which? The instructions that read the latch rather than the pin are the ones that read a value, possibly change it, and then rewrite it to the latch. These are called "read-modify-write" instructions. The instructions listed below are read-modify-write instructions. When the destination operand is a port or a port bit, these

instructions read the latch rather than the pin:

```
ANL             (Logical AND, e.g., ANL P1,A)
ORL             (Logical OR, e.g., ORL P2,A)
XRL             (Logical EX-OR, e.g., XRL P3,A)
JBC             (Jump if bit=1 and clear bit, e.g., JBC P1.1, LABEL)
CPL             (Complement bit, e.g., CPL P3.0)
INC             (Increment, e.g., INC P2)
DEC             (Decrement, e.g., DEC P2)
DJNZ            (Decrement and jump if not zero, e.g., DJNZ P3, LABEL)
MOV PX.Y,C      (Move carry bit to bit Y of Port X)
CLR PX.Y        (Clear bit Y of Port X)
Set PX.Y        (Set bit Y of Port X)
```

The last three instructions in this list read the port byte, all 8 bits, modify the addressed bit, and then write the new byte back to the latch.

All of the Port 1 and Port 3 pins are multifunctional. They are not only port pins, but also serve alternate functions listed below. The alternate functions are selected when the associated port latch bits are set. Power reset sets all the alternate function latch bits.

```
P0.0/AD0-  Mulitplexed Byte of Address/Data for External Memory.  This alternate function is not used in the
P0.7/AD7   two WYE Monitor applications.

P1.0/T2 T2 Timer/Counter 2 external imput.  Not used in the WYE Monitor applications.
P1.1/T2EX  Timer/Counter 2 capture/reload trigger.  Not used in the WYE Monitor applications.
P1.2/T2EX  Timer 2 Reload/Capture/Direction control.  Not used in the WYE Monitor applications.
P1.3/CEX0  PCA Module 0 Capture Input, Compare/PWM output. Not used in the WYE Monitor applications.
P1.4/CEX1  PCA Module 1 Capture Input, Compare/PWM output.  Not used in the WYE Monitor applications.
P1.5/CEX2  PCA Module 2 Capture Input, Compare/PWM output.  Not used in the WYE Monitor applications.
P1.6/CEX3  PCA Module 3 Capture Input, Compare/PWM output.  Not used in the WYE Monitor applications.
P1.7/CEX4  PCA Module 4 Capture Input, Compare/PWM output.  Not used in the WYE Monitor applications.

P2.0/A8-   High Byte of Address for External Memory.  Not used in the WYE Monitor applications.
P2.7/A15

P3.0/RXD   Serial Port Input.  This function is used only in the Isolated CPU Interface.
P3.1/TXD   Serial Port Output. This function is used only in the Isolated CPU Interface.
P3.2/INT0- External Interrupt 0.  The Watch-Dog Timer module uses Interrupt 0 to sense the PC hold-off signal.
P3.3/INT1- External Interrupt 1.  Not used in the WYE Monitor applications.
P3.4/T0    Timer/Counter 0 external clock input.  Not used in the WYE Monitor applications.
P3.5/T1    Timer/Counter 1 external clock input.  Not used in the WYE Monitor applications.
P3.6/WR-   Write Strobe for External Data Memory.  Used only in the Isolated CPU Intreface.
P3.6/RD-   Read Strobe for External Data Memory.  Used in both applications.
```

Timer/Counters

The 87C51FA has three 16-bit timer/counter registers, Timer 0, Timer 1, and Timer 2. Each consists of two 8-bit registers, THx and TLx, (x =0, 1 and 2). All three can be configured to operate as timers or event counters.

In the "timer" function, TLx is incremented every machine cycle; therefore one can think of it as counting machine cycles. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the "counter" function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0, T1, or T2. In this function, the external input is sampled during S5P2 of every machine cycle. (See the internal clock states description in the 87C51FA data sheets in

Section 5.) When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register in the S3P1 of the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the exteral input signal but to insure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

In addition to the Timer or Counter selection, Timer 0, and Timer 1 have four operating modes. Timer 2 is has three modes of operation: "capture," "auto reload" and baud-rate generator.

Timer/Counters 0 and 1

The Isolated CPU Interface uses Timer/Counters 0 and 1. The Watch-Dog Timer does not use these timer/counters. For brevity, they are called Timer 0 and Timer 1.

Timers 0 and 1 are very similar and both operate in mode 2. Figure 9 shows the mode 2 configuration. Timer 0 is used as the baud-rate generator for the serial port and Timer 1 is used as a data sampling clock for the parallel I/O ports.

Register TMOD specifies Timer/Counters 0 and 1 modes. Register TCON controls the operation (i.e. turns them on and off) of these two timer/counters. Timer 2 uses a separate mode/control register T2CON.

Mode 2 for Timer/Counter 1 is used to generate the 300 baud serial port shift clocks in the Isolated CPU Interface Board application. Mode 2 configures the timer register as an 8-bit counter (TL1) with automatic-reload as shown in Figure 9. The initialization firmware loads A0H (160D) into TH1. Overflow from TL1 sets TF1, the interrupt flag, and reloads TL1 with the contents of TH1; the overflow-induced reload leaves TH1 unchanged. The interrupt flag TF1 does not cause an interrupt because the ET1 bit in the IE register is a 0. The processor clock is 11,059,200 Hz so the divide-by-12 counter produces a timer 0 and 1 clock rate of 921,600 Hz. C/T- (in TMOD) is 0 and TR1 (in TCON) is a 1. The Timer 1 overflow is 300 Hz and is used as the baud rate for the serial port; see figure 13, for the usage of the Timer 1 overflow.

Timer 0's mode 2 operation is identical to that in Timer 1. TF0, the interrupt flag, is set by overflow and is enabled in the interrupt system by ET0 in the IE. TH0 is set to 00H, which produces a Timer 0 overflow rate of 3600 Hz that is used by the Isolated CPU Interface firmware as a data sampling clock for the parallel I/O ports.

See the TMOD, TCON and IE tables in the 87C51 data sheets for additional details on the usage of these mode and control bits.

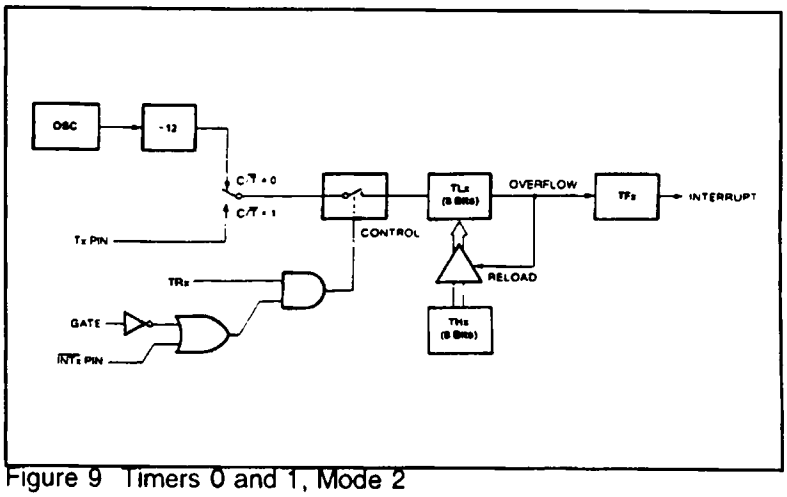


Figure 9 Timers 0 and 1, Mode 2

Timer 2

Timer 2 is a 16-bit timer/counter. Timer 2 is has three modes of operation: "capture," "auto reload", and baud-rate generator. Since neither WYE Monitor application uses this timer/counter, it is not described.

PCA, Programmable Timer/Counter Array

The PCA is used in both the Isolated CPU Interface and the Watch-Dog Timer module.

The Programmable Timer/Counter Array consists of a 16-bit counter/timer and five 16-bit compare/capture modules as shown in Figure 10. Figure 11 shows the PCA Timer/Counter. The PCA timer/counter serves as a common time base for the five modules and is the only timer that can service the PCA. Its clock input can be programmed to count any of the following signals: 1) Oscillator frequency ÷ 12; 2) Oscillator frequency ÷ 4; 3) Timer 0 overflow; 4) External input on EC1 (P1.2).

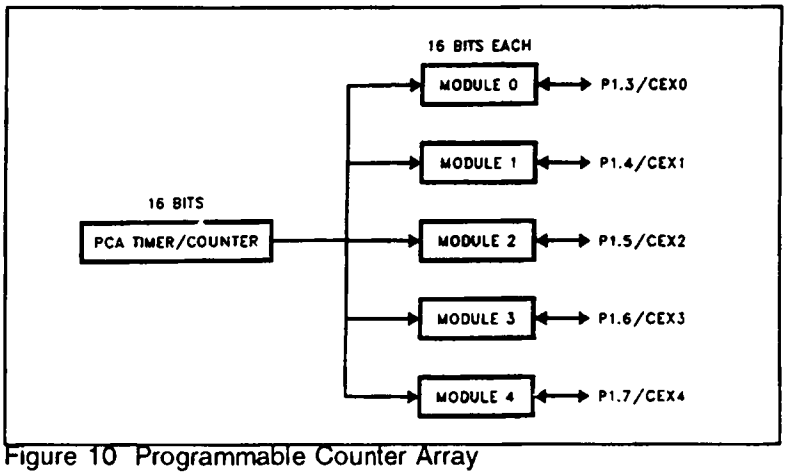


Figure 10 Programmable Counter Array

Each compare/capture module can be programmed in any of the following modes: 1) Rising and/or falling edge capture; 2) Software timer; 3) High speed output; 4) Pulse width modulator. Module 4 can also be programmed as a watch-dog timer.

The PCA Timer/Counter is controlled by CMOD, the PCA Counter Mode Register. Each module has a mode register, CCAPMn (n = 0, 1..4) to select the module function. Each module has a pair of 8-bit compare/capture registers, CCAPnH and CCAPnL, that store the time when a capture event occurred or when a comparator event should occur. The CMOD, CCAPnH, CCAPnL and CCAPMn registers are shown in the 87C51 data sheets.

In the Isolated CPU Interface Board application, PCA Module 4 is used to generate a 14 Hz clock for the MAX695 Watch-Dog chip. In this application, CMOD is set to 00H; this sets the PCA input clock mode to Fosc ÷ 12. CR, the Counter Run bit (in CCON), is set to 1; CH and CL are set to 00H. This setting makes the counter divide by 65,536. WDTE

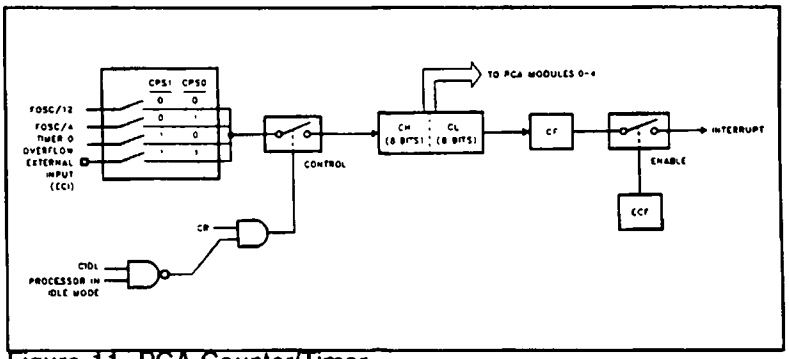


Figure 11 PCA Counter/Timer

(in CMOD) is set to 1, which enables the watch-dog timer function on PCA module 4. Figure 11 shows the PCA module 4 in the watch-dog timer mode. CCAPM4 is set to 4CH, which sets ECOM4, MAT4 and TOG4 to 1. This enables the comparator function, flags the CCF4 bit in CCON (flagging an interrupt), and causes the P1.7 pin to toggle when the interrupt is generated.

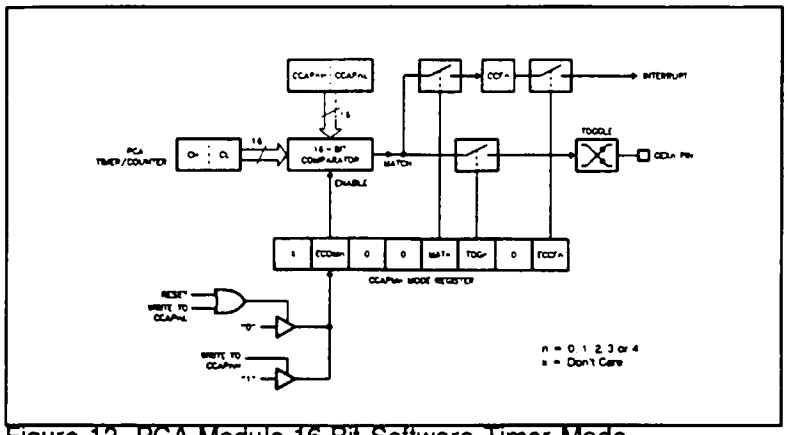


Figure 12 PCA Module 16-Bit Software Timer Mode

Since P1.7 is used for parallel I/O, any interrupt-driven activity on this pin would perturb the device interface. The CCAPM4 configuration described above is required for the operation of Module 4's timer function. To avoid activating P1.7, the firmware main loop recurrently tests the state of the PCA CH and CL counters. When the count reaches a threshold value, the Module 4 CCAP4H and CCAP4L capture registers are set to new values so they never match the PCA's CH and CL, therefore P1.7 is never interrupt-driven. When the capture registers are set to new values, the software also toggles the MAX695 WDI input via the RD- pin.

See the CMOD, CCON, CCAP4H, CCAP4L tables in Section 5 for details of these SFR registers.

The Watch-Dog Timer module does not use timers 0, 1 and 2. The PCA is used for four timing functions and modules 0 through 3 operate in the 16-bit Software Timer Mode. Figure 13 shows the module-counter configuration. Power reset clears the CPS1 and CPS0 bits (in CMOD); this selects Fosc ÷ 12 (e.g. 921,600 Hz) for the PCA clock. The firmware sets the CR bit in CCON; this enables the PCA clock to the counter. The PCA counter (CH and CL) overflow sets flag CF in CCON but does not cause an interrupt because ECF (in CMOD) is also a 0 as it was also cleared by the reset. The comparator enable bit, ECOMn in the CCAPMn register, is set to a 1 when the firmware loads a 16-bit value in CCAPnH and CCAPnL. The firmware sets the MATn and ECCF bits in CCAPMn; these permit a comparator match to set the CCFn interrupt flag in CCON. The five CCFn flags are OR-ed in the Interrupt Source Logic; the firmware must test the CCFn flag states to determine which module set the interrupt.

See the CMOD, CCON, CCAPMn tables in the 87C51FA data sheets in Section 5. The Interrupt Source Logic is described below.

Serial Port Interface

The Isolated CPU Interface uses the serial port for message byte reception and transmission and is assigned the highest priority in the IP register. The serial port is not used by the Watch-Dog Timer module because it is not involved in message activity.

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, which means that it can commence reception of a second byte before a previously received byte has been read from the receive register. However, if the first byte still hasn't been read by

the time reception of the second byte is complete, one of the bytes will be lost. The serial port receive and transmit registers are both accessed at Special Function Register SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

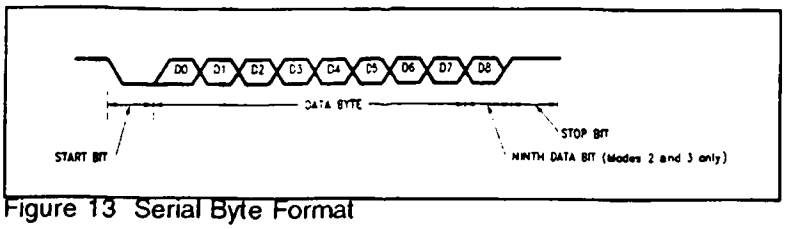


Figure 13 Serial Byte Format

The serial port can operate in 4 modes; Mode 3 is used in the Isolated CPU Interface Board. In Mode 3, 11 bits are transmitted through TXD or received into RXD: a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit (TB8 in SCON) can be assigned the value 0 or 1. Or, for example, the parity bit (P in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is ignored. The baud rate is variable and is generated by Timer 1. Figure 13 shows the serial byte format.

Figure 14 shows the operation of the Serial Port in Mode 3.

The serial port control and status register is the Special Function Register SCON. This register contains the mode selection bits SM0 and SM1, the 9th data bit for transmit and receive, TB8 and RB8, and the serial port interrupt bits TI and RI. SCON is initialized to Mode 3 by the firmware. SCON is shown in the 87C51FA data sheet in Section 5. The SMOD1 bit in PCCON is initialized to 0 by the power reset.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. In Mode 3, reception is initiated by the incoming start bit if REN = 1 in SCON.

Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal also loads TB8 into the 9th position of the transmit shift

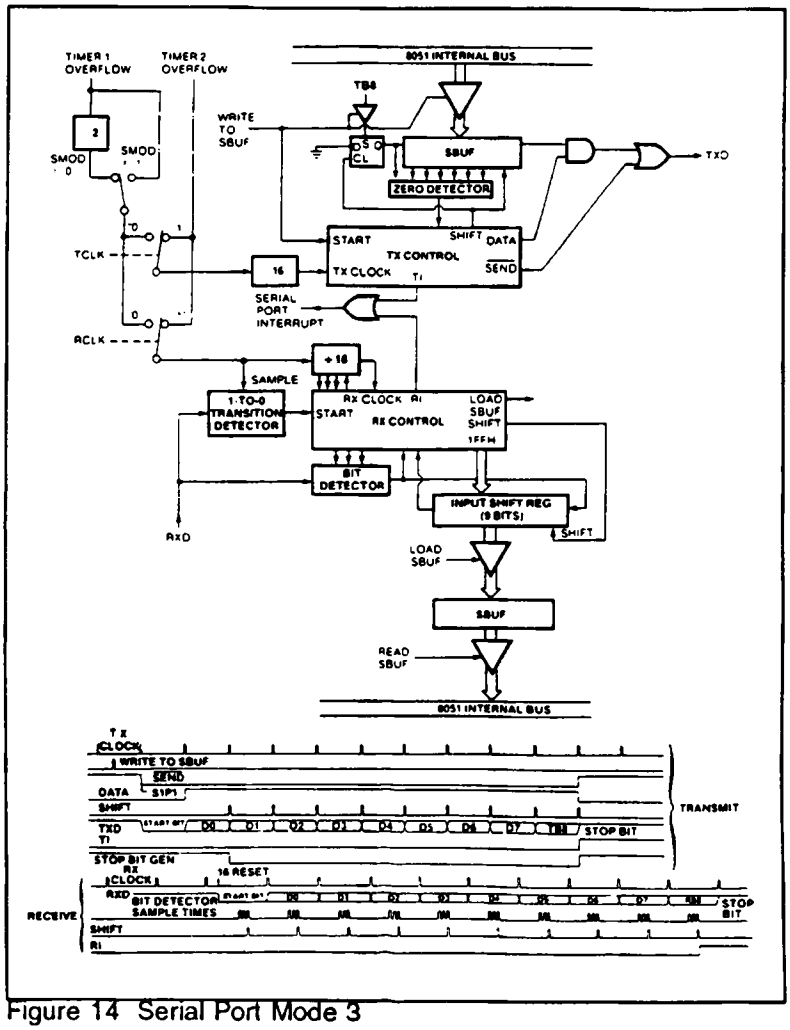


Figure 14 Serial Port Mode 3

register and flags the TX Control unit that a transmission is requested. Transmission commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter; therefore, the bit times are synchronized to the divide-by-16 counter, not to the "write to SBUF" signal.

Transmission begins with the activation of the "Write to SBUF" signal, which puts the start bit in TXD. One bit time later; DATA is activated, which enables the output bit of the transmit shift register to TXD. The first shift pulse occurs one bit time after that. The first shift clocks a 1 (the stop bit) into the 9th bit position of the shift register. Thereafter, only zeroes are clocked in.

As data bits shift out to the right, zeroes are clocked in from the left. When TB8 is at the output position of the shift register, then the stop bit is just to the left of TB8, and all positions to the left of that contain zeroes. This condition flags the TX Control unit to do one last shift, then deactivate SEND- and set TI. This occurs at the 11th divide-by-16 rollover after the "write to SBUF".

Reception is initiated by a detected 1-to-0 transition at RXD. For this purpose RXD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written to the input shift register.

At the 7th, 8th and 9th counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that appeared in at least 2 of the 3 samples. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit reverts back to looking for another 1-to-0 transition. If the start bit proves valid, it is shifted into the input shift register and reception of the rest of the frame will proceed.

As data bits come in from the right, 1's shift out to the left. When the start bit arrives at the leftmost position in the shift register, it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI in SCON. The signal to load SBUF and RB8 and to set RI, will be generated only if the following conditions are met at the time the final shift pulse is generated:

1) RI = 0, and 2) Either SM2 = 0 or the 9th data bit = 1.

If either of these conditions is not met, the received frame is irretrievably lost and RI is not set. If both conditions are met, the received 9th data bit goes into RB8 and the first 8 data bits go into SBUF. One bit time later, whether the above conditions were met or not, the unit goes back to looking for a new 1-to-0 transition at the RXD input.

Note that the received stop bit state is ignored; the validity of the stop bit can be checked with Framing Error Detection.

Interrupts

The Interrupt Source Logic is shown in Figure 15 (next page) and provides 7 interrupt sources.

The External Interrupts INT0- and INT1- can be either level-activated or transition-activated, depending on bits IT0 and IT1 in TCON. The flags that actually generate these interrupts are bits IE0 and IE1 in TCON. For external interrupts, there are two ways that the interrupt request flag that generated the interrupt is cleared. If the external interrupt is transition-activated, on-chip logic clears the flag when the service routine is vectored to. If the interrupt was level-activated, then the external requesting source

controls the request flag rather than the on-chip logic.

In the Watch-Dog Timer module, the PC hold-off signal clocks the 74LS74 flip-flop. The flip-flop's Q- output goes low, which activates INT0-. Bit IT0 in TCON is initialized to a 1 which makes INT0- negative-edge triggered.

The Timer 1 and Timer 0 Interrupts are generated by TF0 and TF1 in TCON, which are set by a rollover in their respective timer registers in mode 2. When a timer interrupt is generated, the flag that generated it is cleared by the on-chip logic when the service routine is vectored to.

The Serial Port Interrupt is generated by the logical OR of RI and TI in SCON. Neither of these flags is cleared by chip logic when the service routine is vectored to. The service routine will have to determine whether it was RI or TI that generated the interrupt, and the flag bit will have to be cleared in firmware.

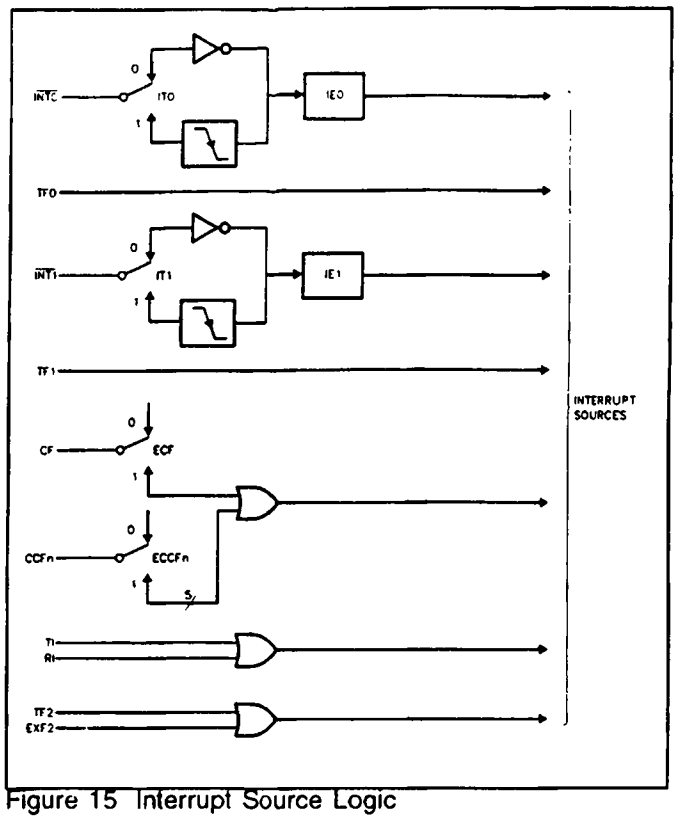


Figure 15 Interrupt Source Logic

The Timer 2 interrupt is generated by the logical OR of RF2 and EXF2. Neither of these flags is cleared by chip logic when the interrupt service routine is vectored to. The service routine will have to determine whether it was TF2 or EXF2 that generated the interrupt, and the flag bit will have to be cleared in firmware. Timer 2 is not used in either WYE Monitor application.

PCA interrupts are generated by the logical OR of the following flags: CF, CCF0, CCF1, CCF2, CCF3 and CCF4, all in CCON. None of these flag bits are cleared by chip logic when the service routine is vectored to. The service routine must determine which flag triggered the interrupt and clear it. The PCA interruput is enabled by bit EC in the IE register. In addition, the CF flag and each of the CCFn flags must be enabled by bit ECF in CMOD and ECF in

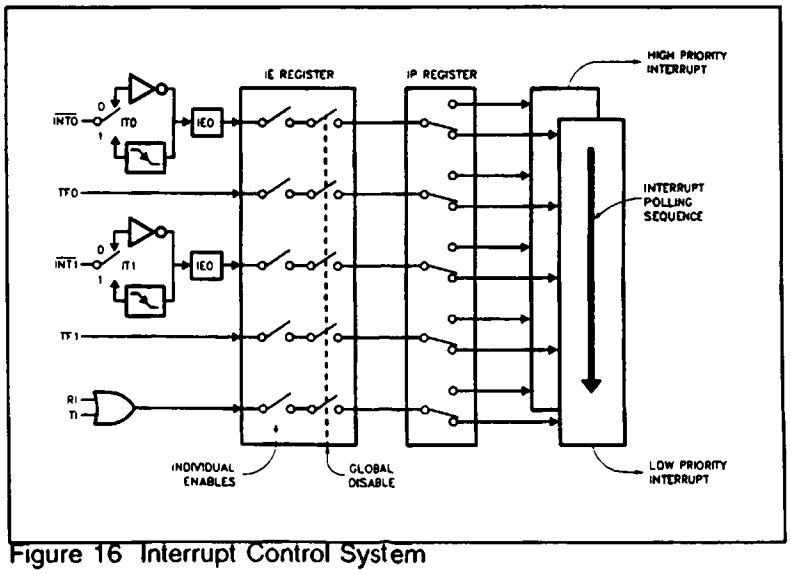


Figure 16 Interrupt Control System

CCAPMn before they can cause an interrupt.

All of the bits that generate interrupts can be set or cleared by software with the same result as though it had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be cancelled in software.

Each of these interrupts can be individually enabled or disabled by setting or clearing a bit in IE. Note that IE has a global disable bit, EA, which disables all interrupts at once. The IE and IP register tables are shown in the 87C51 data sheets. Figure 16 (previous page) shows the basic 8051 Interrupt Control System.

Priority Level Structure

Each interrupt source can also be individually programmed to one of two priority levels by setting or clearing a bit in IP. A low-priority interrupt can itself be interrupted by a high-priority interrupt but not by another low-priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt source.

If two requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If requests of the **same** priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level, there is a second priority structure determined by the polling sequence as follows:

	SOURCE	PRIORITY WITHIN LEVEL	VECTOR ADDRESS
1.	INTO-	(highest)	0003H
2.	Timer 0		000BH
3.	INT1-		0013H
4.	Timer 1		001BH
5.	PCA		0033H
6.	Serial Port		0023H
7.	Timer 2	(lowest)	002BH

Note that the "priority within level" structure is only used to resolve simultaneous requests of the same priority level.

How Interrupts Are Handled

The interrupt flags are sampled at S5P2 of every machine cycle. The samples are polled during the following machine cycle. If one of the flags was in a set condition at S5P2 of the preceding cycle, the polling cycle will find it and the interrupt system will generate an LCALL to the appropriate service routine, provided this hardware-generated LCALL is not blocked by any of the following conditions:

1. An interrupt of equal or higher priority level is already in progress.

2. The current (polling) cycle is not the final cycle in the execution of the instruction in progress.

3. The instruction in progress is RETI or any access to the IE or IP registers.

Any of these three conditions will block the generation of the LCALL to the interrupt service routine. Condition 2 ensures that the instruction in progress will be completed before vectoring to any service routine. Condition 3 ensures that if the instruction in progress is RETI or any access to IE or IP, then at least one more instruction will be executed before any interrupt is vectored to.

The polling sequence is repeated with each machine cycle, and the values polled are the values that were present at S5P2 of the previous machine cycle. Note that if an interrupt flag is active but not being responded to for one of the above conditions and if the flag does not continue to be active when the blocking condition is removed, the denied interrupt will not be serviced. The interrupt logic does not store the occurrence of unserviced interrupts. Every polling cycle is new. The user must take this potential loss of unserviced interrupts into account in the logic design.

The polling cycle/LCALL sequence is illustrated in Figure 17.

Note that in accordance with the above rules, if an interrupt of higher priority level goes active prior to S5P2 of the machine cycle labeled C3 in Figure 17, then it will be vectored to during C5 and C6 without any instruction of the lower priority routine having been executed. Therefore, the processor acknowledges an interrupt request by executing a hardware-generated LCALL to the appropriate servicing routine. In some cases it also clears the flag that generated the interrupt, and in other cases, it doesn't. It never clears the PCA, Serial Port, or Timer 2 flags. This has to be done in the user's software. It clears an external interrupt flag (IE0 or IE1) only if it was transition-activated. The hardware-generated LCALL pushes the contents of the Program Counter onto the stack (but does not save the PSW) and reloads the PC with an address that depends on the source of the interrupt being vectored to, as shown on the previous page.

Execution proceeds from that location until the RETI instruction is encountered. The RETI instruction informs the processor that this interrupt routine is no longer in progress, then pops the top two bytes from the stack and reloads the Program Counter. Execution of the interrupted program continues from where it left off.

Note that a simple RET instruction would also have returned execution to the interrupted program, but it would have left the interrupt control system thinking an interrupt was still in progress.

External Interrupts

The external sources can be programmed to be level-activated or transition-activated by setting or clearing bit IT1 or IT0 in Register TCON. If ITx = 0, external interrupt x is triggered by a detected low at the INTx- pin. If INTx- = 1, external interrupt x is edge-triggered. In this mode if sucessive samples of the INTx- pin show a high in one cycle and a low in the next cycle, interrupt request flag IEx in TCON is set. Flag bit IEx then requests the interrupt.

Since the extenal interrupt pins are sampled once each machine cycle, an input high or low should hold for at least 12 oscillator periods to ensure sampling. If the external interrupt is transition-activated, the

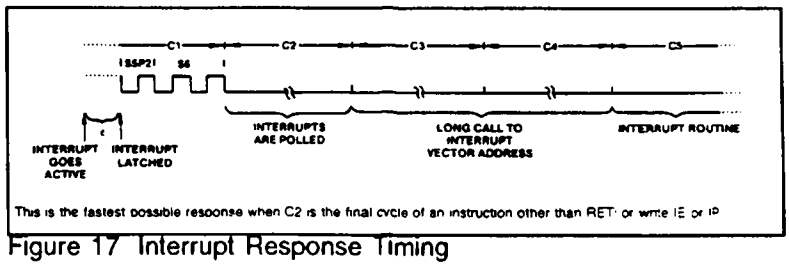


Figure 17 Interrupt Response Timing

external source has to hold the request pin high for at least one cycle, and then hold it low for at least one cycle to ensure that the transition is seen so that the interrupt request flag IEx will be set. IEx will be automatically cleared by the CPU when the service routine is called.

If the external interrupt is level-activated, the external source has to hold the request active until the requested interrupt is actually generated. Then it has to deactivate the request before the service routine is completed or else another interrupt will be generated.

Response Time

The INT0- and INT1- levels are inverted and latched into IE0 and IE1 at S5P2 of every machine cycle. The values are not actually polled by the circuitry until the next machine cycle. If a request is active and conditions are right for it to be acknowledged, a hardware subroutine call to the requested service routine will be the next instruction to be executed. The call itself takes two cycles. Thus a minimum of three complete machine cycles elapse between activation of an external interrupt request and the beginning of execution of the first instruction of the service routine. Figure 17 shows the interrupt response timing.

A longer response time will result if the request is blocked by one of the previously listed conditions. If an interrupt of equal or higher priority level is already in progress, the additional wait time obviously depends on the nature of the other interrupt's service routine. If the instruction in progress is not in the final cycle, the additional wait time cannot be more than 3 cycles, since the longest instructions (MUL AND DIV) are only 4 cycles long. If the instruction in progress is RETI or an access to IE or IP, the additional wait time cannot be more than 5 cycles (a maximum of one more cycle to complete the instruction in progress, plus 4 cycles to complete the next instruction if the instruction is MUL or DIV). Therefore, in a single-interrupt system the response time is always more than 3 cycles and less than 8 cycles.

Reset

The reset input is the RST pin, which is the input to a Schmidt Trigger. A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods) while the oscillator is running. The CPU responds by executing an internal reset. It also configures the ALE and PSEN- pins as inputs; they are quasi-bidirectional. The internal reset is executed during the second cycle in which RST is high and is repeated every cycle until RST goes low. It leaves the internal registers as shown in Figure 7.

The internal RAM is not affected by reset. When VCC is turned on, the RAM content is indeterminate unless the 87C51FA is returning from a reduced power mode of operation. The reduced power mode of operation is not used in the Isolated CPU Interface Board or the Watch-Dog Timer applications but one bit of the PCON power control Register in the Special Function Registers is important. This bit is SMOD1 which is bit PCON.7. It causes the serial port baud rate to be doubled when set.

2.6 WYE Monitor System PC Configuration

This section describes the configuration of the WYE Monitor System's control PC. The intent of this description is to provide an overview of the PC's important features. A very detailed description is unnecessary because the most of the components could be replaced by generic equivalents. However, in some cases important features or critical components are identified.

Two PC's are used in the system. One is on line and the other is a ready spare that can be powered up and put into service by turning on the power and actuating the bus switchover unit. Their reliability has been enhanced by using rotating components with high MTBF's.

The PC uses a 486DX processor with 8 MB of RAM on a generic mother-board. 2 MB of the RAM are used as virtual memory and 3 MB are used for program segment swapping. The Hard Disk is a Quantum 127 MB unit with an IDE controller that has a 250,000 hour (estimated) MTBF for long-term reliability. The following components are used for program development: a 3.5", 1.44 MB floppy disk, a keyboard and mouse. The keyboard can be used to stop the control program execution.

The power supply has been upgraded by replacing the sleeve-bearing cooling fan with a ball-bearing fan having a 60,000 hour MTBF (estimated).

The monitor is a 14" CTX super-VGA unit used in the VGA mode. An Elographics Intellitouch Touch Screen is installed on the monitor screen. This is a surface acoustic-wave device controlled by an interface board in the PC.

The following boards are installed in the PC:

1) An Elographics Intelitouch Controller.

2) A four-port serial I/O card supplied by Willie's Computer Software Company.

3) A TVGA 800CL video card.

4) A Covox Soundmaster 2 audio card with a microphone jack for voice message input. The speakers are outside the computer cabinet.

5) A Super I/O Card with an IDE hard disk interface and a 3.5" floppy disk controller, two serial ports, one parallel port and one game port. One serial port on the Super I/O Card is disabled and the other is connected to a mouse used for program development.

The four-port serial board drives the four buses and the ports share a common interrupt. The four ports are COM3, COM4, COM5 and COM6. The mouse is on COM1 and the Touch Screen controller is on COM2.

2.7 WYE Monitor PC Interface Bin

The WYE Monitor PC Interface Bin contains the modules that transform the computer's serial port RS-232 signals to the WYE Monitor bus levels and resets the PC in the event of an apparent control program crash. These modules are the PC Watchdog, the PC Transcievers and the Power Supply, which are described below. Drawing D13900P09 is the bin assembly drawing and shows the module and I/O connector locations. The bin interconnect and I/O wiring is shown on drawing C13900W04, the WYE Monitor PC Interface Bin Wiring Diagram. The WYE Monitor A&B Switch Box is not installed in this bin but is included for convenience.

The WYE Monitor PC Interface Bin Assembly drawings are listed below and for convenient reference, reduced-scale copies of these drawings follow this section.

D13900P09 WYE Monitor PC Interface Bin Assembly
C13900W04 WYE Monitor PC Interface Bin Wiring Diagram

C13900P13-20 PC Transceiver Module Assembly, East Arm
C13900P13-30 PC Transceiver Module Assembly, North Arm
C13900P13-40 PC Transceiver Module Assembly, West Arm

C13900P10 WYE Monitor PC Module Watchdog Assembly

C13900P14 WYE Monitor Power Supply Module Assembly

B13900W07 WYE Monitor A&B Switch Box Wiring Diagram

WYE Monitor Watch-Dog Timer

A watch-dog timer is a circuit that automatically invokes a reset unless the system being watched sends regular hold-off signals to the watch-dog. These circuits are used in applications where high reliability is required.

The WYE Monitor control PC's 110 VAC power is controlled by a firmware program in the Watch-Dog Timer module. The Watch-Dog Timer's function is to monitor the execution of the PC's program; in the event of a problem, it cycles the PC's power to induce a power reset and program reboot.

The WYE Monitor PC Watch-Dog Timer is installed in Slot 3 in the WYE Monitor PC Interface Bin. The Watch-Dog Timer's circuitry is packaged on a Vector CG2-95 Card Mount circuit board. The front panel has a green "Power On" LED, a yellow "Alarm" LED and a "Quiet" pushbutton switch; these LED's and switch's functions are described below. The major circuit components are an Intel 87C51 microcontroller and a Maxim MAX695 Microprocessor Supervisory Circuit to sense bin power failures and 87C51 firmware crashes. The other components are a 74LS74 "D" flip-flop, an alarm beeper, and an LM7805T power regulator to produce +5 volt logic power from the bin's +12 volt DC power supply. Three red LED's are installed in a dip header on the circuit board for bench test purposes.

The Watch-Dog Timer drawings are listed on the next page and for convenient reference, reduced-scale copies follow this section.

C13900P10	WYE Monitor PC Watchdog Module Assembly
C13900P11	WYE Monitor PC Watchdog Circuit Board Assembly
C13900S06	WYE Monitor PC Watchdog Circuit Board Schematic Diagram
A13900P12	WYE Monitor Watchdog Ciruit Board Dip Header Assembly

The firmware program contains the Watch-Dog Timer's logic. The program's operations are described by the text and synopsis below — a detailed description of the program is beyond the scope of this manual.

The Watch-Dog Timer has four operating modes: normal, PC restart, scream and maintenance. Normal mode verifies the proper execution of the PC control program. The PC restart mode is entered from the normal mode when the Watch-Dog Timer detects an apparent fault in the execution of PC control-monitor program or detects a bin power problem. The scream mode is entered when the Watch-Dog program detects an alarm condition; the beeper is pulsed to alert the telescope operator and the alarm LED is powered. The maintenence mode is used when the PC is taken off-line for program or hardware maintenance.

In the normal mode, the Watch-Dog program monitors the PC control program activity. After the control program has been started, it outputs a character on the printer port at 2 pulse/Second intervals. Bit D0 in this character is the PC program hold-off signal. The Watch-Dog Timer is connected to the D0 bit. If the timer's program detects a cessation of the hold-off signal, it decides that the PC program is not operating properly or has crashed, etc. The Watch-Dog program then shifts to the Restart Mode, in which the PC power is turned off for 10 seconds and then back on, to force a PC power-on reset. After a 10 second delay for the program to reach the point at which it should output the hold-off signal, the Watch-Dog program resumes testing for the presence of this hold-off signal. If the signal has not resumed, the Watch-Dog program makes two more attempts to induce a PC program reset. If the third reset attempt is unsuccessful, the Watch-Dog program shifts to the scream mode. During the normal mode, the power LED is illuminated.

The maintenance mode is entered by an operator intervention. Three quick actuations of the Quiet push button will activate the maintenance mode. Upon entry to the maintenance mode, the beeper is pulsed several times to acknowledge the maintenance mode request and the program starts an entry delay period of 60 seconds. During this period, the program holds the PC power on and ignores the presence of the hold-off, if it is present.

After the 60 second entry delay, the presence of the hold-off signal will trigger the program to exit from the maintenance mode. Before exiting the entry delay, the program will sound a 10 second series of beeps to query the telescope operator for exit confirmation. If the Quiet button is pushed within a 60 second grace period, the program will restart the maintenance mode. If the Quiet button is not pushed before the exit delay expires, the program will revert to the normal mode.

When the bin Power Supply is turned on, after the 87C51 microcontroller is power-on reset by the MAX695 (described below), the Watch-Dog program waits 60 seconds to permit the PC to boot up before it begins to test for the presence of the 2 pulse/second hold-off signal.

A synopsis of the Watch-Dog Timer's 87C51 firmware program is shown on the next page:

```
Begin:
        Initialize Stack, PCA, I/O

Set_Tries:
        Boot_Tries = Retries

While Boot_Tries > 0

        Boot_PC:
                Turn on Power to PC
                For Boot Delay
                        If Quiet Button is pressed
                                Call Maint_Test

        Check_PC:
                While PC is sending pulses

                Pulsing:
                        Make sure alarm and beeper are off
                        Boot_Tries = Retries
                        If Quiet Button is pressed
                                Call Maint_Test

                No_Pulse:
                        Turn on Alarm LED
                        For Exit Delay
                                Wait
                        Reset_PC:
                                Decrement Boot_Tries
                                Turn off PC power
                                Turn off Power LED
                                For Offtime
                                        Wait
                                Turn on PC power
                                Turn on Power LED

Scream:
        While Quiet Button is not pressed
                Pulse Alarm Beeper
                IF PC pulses resume
                        Go To Pulsing

Flash:
        While Quiet Button is pressed
                Wait
        While PC is not pulsing
                Flash Alarm LED
                If Quiet Button is Pressed
                        Call Maint_Test
                Go To Pulsing

Maint_Test:
        If Quiet Button is pressed quickly three times
                Call Maint_Mode
        Return

Maint_Mode:
        Send Audible Acknowledge
        For Entry Interval
                Flash Power LED
        While PC is not pulsing
                Flash Power LED
        For Grace Interval
                Flash Power LED
                Send audible Query every few seconds
                If Quiet Button is pressed
                        Go To Maint_Mode
        Return
```

Refer to the schematic diagram C13900S06, and note that the LED's and beeper are driven by 87C51 Port 0 bits 0.1 through 0.7 (bit 0.4 is not used). Port 0.2 senses the Quiet switch's state. Also note that 87C51 Port 2.6 clocks the MAX695 WDI input and Port 2.7 direct resets the 74LS74 flip-flop. Port 0.0 drives a solid state 110 VAC relay mounted on the back of the bin; this relay provides the PC's 110 VAC power. When the PC is powered, Port 0.0 is low and sinks current from V_{CC} through the solid state relay. To reset the PC, the program firmware sets Port 0.0 high which disconnects the PC's 110 VAC power.

The Watch-Dog timer uses the 87C51 Timer 1, Timer 2 and the PCA (programmable counter array) features. These are briefly described in Section 2.4. The Intel 87C51 Microcontroller is also used in the Isolated CPU Interface Board, Section 2.7.

The positive-going edge of the PC's printer port hold-off signal, bit D0, clocks the 74LS74 flip-flop. The 74LS74 Q- output goes low and the negative edge transition activates the 87C51 INTO- interrupt input. During the ensuing response to the interrupt, Port 2.7 is set low and then high to clear the flip-flop for the next hold-off signal.

Three red LED's are installed on dip header DV10 and are only visible when the module is operated on an extender cable. These LED's are intended to be used during bench tests. LD3 is driven by Port 0.7 and flashes each time the confirmation signal occurs. LD4 and LD5 do not have any functional assigment.

The application of the MAX695 chip in the Watch-Dog Timer is very similar to its usage in the Isolated CPU Interface board described in Section 2.7. See this section for a description of the chip's functions in these two applications. The only difference between the usage of this chip in the Watch-Dog Timer and Isolated CPU Interface is that in the Isolated CPU Interface, the chip's WDI input is driven by the 87C51 RD/ pulse. The Watch-Dog Timer uses Port 2.6 to drive the WDI input and this port is pulsed during each pass through the normal mode code.

The module is powered by 12 volts DC from the WYE Monitor Power Supply (see below). The 12 volts is regulated to +5 volts DC by an LM7805 regulator; this powers the Watch-Dog Timer circuitry.

WYE Monitor PC Transceiver Module

The WYE Monitor PC Transceiver translates the PC's serial RS-232 signal levels to the bus levels described in Section 2.5. Four types of transceivers are used, one for each bus and they are installed in bin slots 4 through 7; see D13900P09, the bin assembly drawing above. The four transcievers are functionally identical and differ only in the panel label. It is possible to use any transceiver type in another transceiver's slot but this is operationally confusing because it is misleading.

The transceiver's circuitry is contained on a PC board installed in the front of a Vector CG2-95 card mount module. The circuit board is common to all four types of transceivers. Five jumper wires connect the PC board to the Vector PC board 12 volt power, signal buss lines and earth ground. These are connected to the bin backplane wiring via the Vector Board's card edge connector contacts. The connections between the transceiver PC board and the CG2-95 card-edge contacts are shown on the PC Interface Bin Wiring Diagram, C13900W04. The PC's RS-232 bus signals are connected to the module's front panel 25-socket "D" connector. The RS-232 signals are RX (Receive Data), TX (Transmit Data) and RTS (Request to Send).

The transceiver modules are powered by +12 VDC from the WYE Monitor Power Supply (see below). The +12 VDC power is regulated to +5 V DC by an LM7805 regulator. The bus drive and receive circuitry is powered by a Burr-Brown HPR105 which produces + and - 15 VDC. The three power supply outputs are designated +15I, 0VI and -15I. These three outputs are isolated from the supply's + 5 volt and 5 volt common inputs.

The MAX233 RS-232 to TTL converter chip is powered by +5 volt logic power. The chip has an internal flying capacitor power supply to provide the ±9 volt power used for RS-232 signal interfacing. The MAX233 can also supply +9V and -9V for small external loads.

Two front panel LED's indicate bus signal activity; the amber LED (D5) flickers to show monitor message activity and the green LED (D6) flickers to show command and monitor request activity.

For convenient reference, the WYE Monitor PC Transceiver drawings follow the text at the end of this section; these drawings are:

```
C13900P13       WYE Monitor PC Transceiver Assembly
C13900P01       WYE Monitor PC Transceiver PCB Assembly
C13900S02       WYE Monitor PC Transceiver PCB Schematic
```

WYE Monitor line driving and receiving was described in Section 2.4; see this Section for a detailed description of these functions. The transceiver's line drive and receive circuitry is very similar to that in the Isolated CPU Interface Board circuitry and do not require additional description here. The only significant difference is that the transceiver's logic circuitry uses a 74HCT00 instead of a 74LS32. Secondly, instead of Sidactors, Panasonic ERZ-C10DK680 MOV surge arrestors are connected across the bus lines and from each bus line to ground.

WYE Monitor Power Supply Module

The WYE Monitor Power Supply provides +12 VDC to the four WYE Monitor Transceiver modules and the Watch-Dog Timer via the bin backplane wiring. Assembly drawing C13900P14 shows a front panel power supply switch; this is not used. The 110 VAC module power input is wired directly to the supply. A front panel power indicating LED is powered by the +12 VDC power.

The power supply uses a Vector CG2-95 Card Mount circuit board. An NRAO front panel and Lambda modular power supply is mounted on the card and wired to the card-edge connetors. The power supply module card edge connections are shown on the bin wiring schematic, C13900W04.

The power supply modue is a commmercial Lambda LVS-44-12-B switching power supply. The LVS-44-12-B is a switching regulation power supply rated at 12 volts, 2.1 amps, over a temperature range of 25 to 50 degrees C. Line and Load regulation is 0.4% and 0.8%, respectively. Ripple and noise are 15mV RMS and the temperature coefficient is 0.02%/°C. This power supply has overcurrent limiting and overvoltage protection. Molex-type connectors are used for AC and DC wiring connections. A data sheet for this power supply module is included in Section 5.

For convenient reference, a reduced-scale copy of the bin power supply assembly drawing C13900P14, follows the text at the end of this section. There is no schematic diagram; the bin wiring schematic C13900W04 shows the module's card-edge connections.

WYE Monitor A&B Switch Box

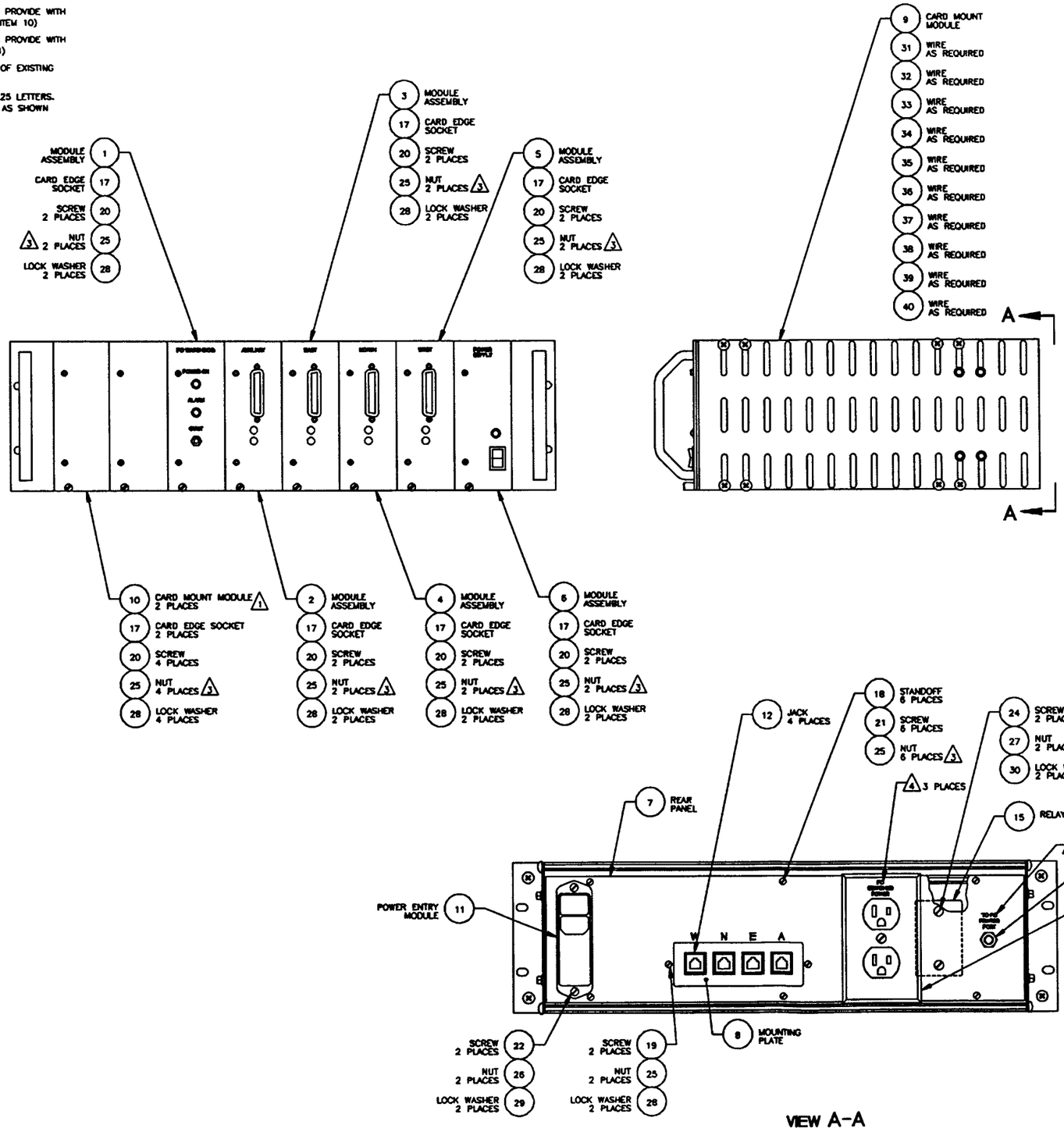
This unit is used to switch the four bus lines from the on-line PC and PC Interface to the backup system in the event of a PC or bus line driving-receiving problem.

The A&B Switch Box is a modification of a commercial printer selector switch box. Telephone line connectors are used for the bus line connections. Drawing B13900W07 shows the box wiring.

REV	DATE	DRAWN BY	APPR'D BY	DESCRIPTION

NOTES:

1. MOUNTING HARDWARE IS PROVIDE WITH CARD MOUNT MODULE (ITEM 10)
2. MOUNTING HARDWARE IS PROVIDE WITH OUTLET COVER (ITEM 14)
3. MOUNT NUT INTO SLOT OF EXISTING T-STRUT
4. MARK LEGIBLY USING .125 LETTERS. LOCATE APPROXIMATELY AS SHOWN



VIEW A-A

ITEM NO.	REF. DES.	MANUFACTURER	PART NUMBER	DESCRIPTION	QTY
40				WIRE, RED, #26	AR
39				WIRE, GRN, #26	AR
38				WIRE, RED/BLK, #26	AR
37				WIRE, BLK, #22	AR
36				WIRE, RED, #22	AR
35				WIRE, GRN, #20	AR
34				WIRE, WHT, #20	AR
33				WIRE, BLK, #20	AR
32				WIRE, GRN, #18	AR
31				WIRE, WHT, #18	AR
30				WASHER, LOCK, #8	2
29				WASHER, LOCK, #6	4
28				WASHER, LOCK, #4	18
27				NUT, HEX, 8-32UNC-2X	2
26				NUT, HEX, 6-32UNC-2B	4
25				NUT, HEX, 4-40UNC-2B	24
24				SCREW, PAN HEAD, SS, 8-32UNC-2A x 1.25	2
23				SCREW, PAN HEAD, SS, 6-32UNC-2A x .75	2
22				SCREW, PAN HEAD, SS, 6-32UNC-2A x 1.00	2
21				SCREW, PAN HEAD, SS, 4-40UNC-2A x 1.06	6
20				SCREW, HEX HEAD, SS, 4-40UNC-2A x .44	16
19				SCREW, PAN HEAD, SS, 4-40UNC-2A x .31	2
18				STANDOFF, ø.25 x .75	6
17		CINCH	9203	SOCKET, CARD EDGE	8
16		SWITCHCRAFT	795.954/88	JACK	1
15		TELEDYNE	611-2	RELAY, SOLID STATE	1
14				COVER, OUTLET	1
13				OUTLET, POWER	1
12				JACK, PHONE	4
11		CORCOM	JEFM1S F7271A	MODULE, POWER ENTRY	1
10		VECTOR	CM45B95-2	MODULE, CARD MOUNT	2
9		VECTOR	CCM14S/90	ASSY, CARD CAGE	1
8		NRAO	C13900M17	PLATE, JACK MOUNTING	1
7		NRAO	C13900M16	PANEL, REAR	1
6		NRAO	C13900P14	ASSY, POWER SUPPLY	1
5		NRAO	C13900P13-40	ASSY, PC TRANSCEIVER	1
4		NRAO	C13900P13-30	ASSY, PC TRANSCEIVER	1
3		NRAO	C13900P13-20	ASSY, PC TRANSCEIVER	1
2		NRAO	C13900P13-10	ASSY, PC TRANSCEIVER	1
1		NRAO	C13900P10	ASSY, PC WATCHDOG	1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL :

FINISH :

NEXT ASSEMBLY | DWG. TYPE

VLA PROJECT: WYE MONITOR

TITLE: WYE MONITOR PC INTERFACE BIN ASSEMBLY

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY | DATE 6-93
DESIGNED BY | DATE 6-93
APPROVED BY | DATE 6-93

SHEET NUMBER 1 OF 1 | DRAWING NUMBER D13900P09 | REV. — | SCALE 1/2

ACAD : 13900P09

REV.	DATE	DRAWN BY	APROV'D BY	DESCRIPTION

AUX TRANSCEIVER MODULE
NRAO DWG #C13900P13-10

TRANSCEIVER PCB
NRAO DWG # C13900P01

J1-1 RED
J1-2 BLK
J1-3 RED
J1-4 N/C
J1-5 GRN

GND
LINE+
LINE-
+12V
CINCH 9203

REAR PANEL JACK MTG PLATE
NRAO DWG # C13900M17

AUX
GRN
RED
PHONEJACK

EAST TRANSCEIVER MODULE
NRAO DWG #C13900P13-20

TRANSCEIVER PCB
NRAO DWG # C13900P01

EAST
PHONEJACK

NORTH TRANSCEIVER MODULE
NRAO DWG #C13900P13-30

TRANSCEIVER PCB
NRAO DWG # C13900P01

NORTH
PHONEJACK

WEST TRANSCEIVER MODULE
NRAO DWG #C13900P13-40

TRANSCEIVER PCB
NRAO DWG # C13900P01

WEST
PHONEJACK

REAR PANEL
NRAO DWG # C13900M16

AC OUTLET
POWER ENTRY MODULE CORCOM JEFMIS F7871A
RELAY
TELEDYNE 611-2
PRINTER PORT JACK
SWITCHCRAFT 795854/00

PC WATCHDOG MODULE
NRAO DWG #C13900P10

WATCHDOG PCB
NRAO DWG # C13900P11

POWER SUPPLY MODULE
NRAO DWG #C13900P14

POWER SUPPLY LAMBDA LVS-44-12-B

FRONT PANEL
NRAO DWG # C13900M14

LED
10K
VHT
AC GND
AC HOT
AC NEU
+12V

ORCAD : 13900W04

D13900P09	ASSEMBLY
NEXT ASSEMBLY	DVG TYPE

UNLESS OTHERVISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX) ±
2 PLACE DECIMALS (.XX) ±
1 PLACE DECIMALS (.X) ±

MATERIAL:

FINISH:

VLA PROJECT: WYE MONITOR

TITLE: WYE MONITOR PC INTERFACE BIN WIRING DIAGRAM

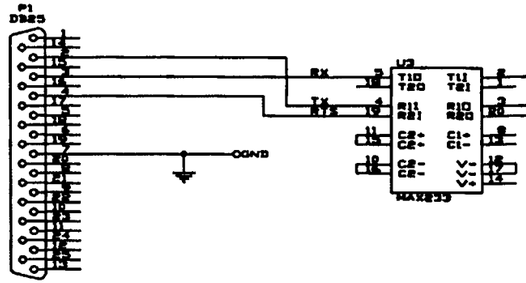
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO,NEW MEXICO 87801

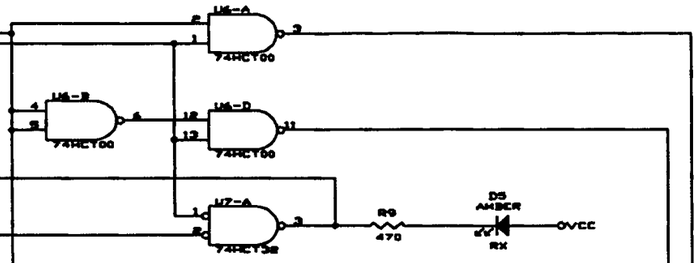
DRAWN BY		DATE 4-94
DESIGNED BY		DATE 4-94
APPROVED BY		DATE 4-94
SHEET NUMBER	1 OF 1	DRAWING NUMBER C13900W04 REV. - SCALE -

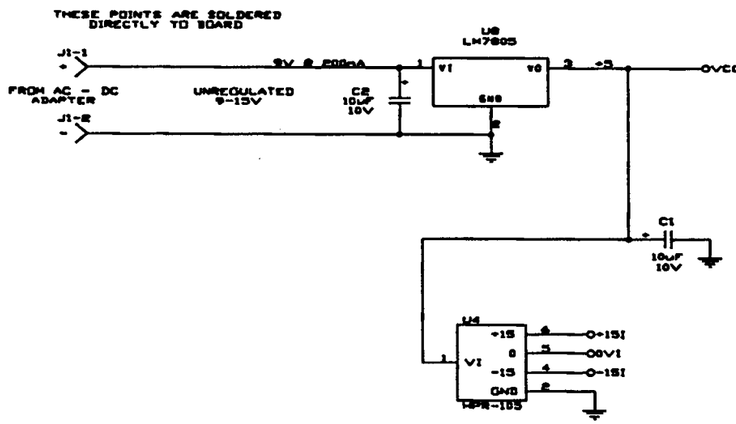
REV.	DATE	DRAWN BY	APROV'D BY	DESCRIPTION
A	4-94			CHGD U2 TO OP15FP

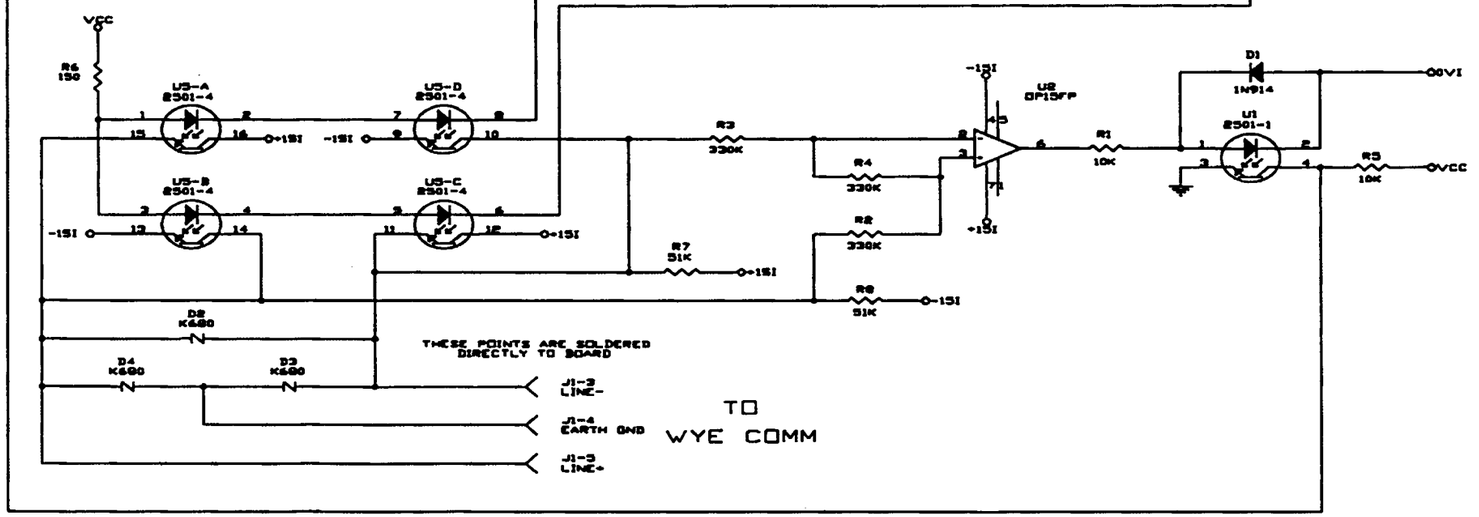
NOTES :

1. ALL RESISTORS ARE 1/8W, 5%
   5% UNLESS OTHERWISE SPECIFIED









C13900P01	ASSEMBLY
C13900N01	DRILL DWG
C13900AB02	SILKSCREEN
C13900AB01	ARTWORK
NEXT ASSEMBLY	DWG TYPE

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX) ±
2 PLACE DECIMALS (.XX) ±
1 PLACE DECIMALS (.X) ±

MATERIAL:

FINISH:

VLA PROJECT: WYE MONITOR

TITLE: WYE MONITOR
PC TRANSCEIVER
PCB SCHEMATIC

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO,NEW MEXICO 87801

DRAWN BY	DATE 2-92
DESIGNED BY	DATE 12-91
APPROVED BY	DATE 2-92

SHEET NUMBER 1 OF 1 | DRAWING NUMBER C13900S02 | REV. A | SCALE -

ORCAD : 13900S02

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

NOTES:

1. REMOVE ALL BURRS AND SHARP EDGES
2. MOUNTING HARDWARE IS INCLUDED WITH CARD MOUNT MODULE (ITEM 3)
3. SEE TABLE 1 FOR ASSEMBLY NUMBER AND APPROPRIATE FRONT PANEL NUMBER. -10 ASSEMBLY IS SHOWN

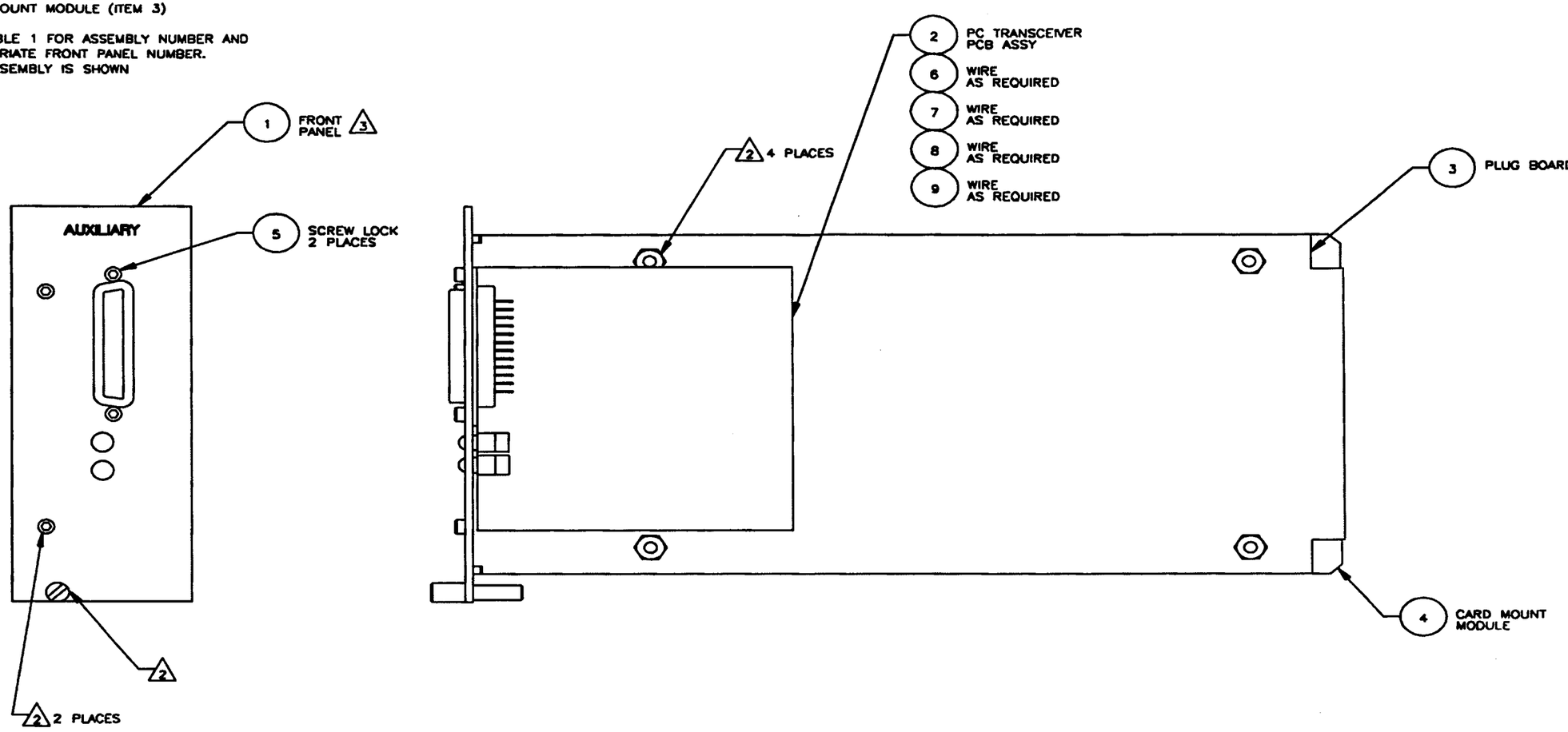


TABLE 1	
ASSEMBLY	FRONT PANEL
-10	C13900M13-1
-20	C13900M13-2
-30	C13900M13-3
-40	C13900M13-4

ITEM NO.	REF. DES.	MANUFACTURER	PART NUMBER	DESCRIPTION	QTY
9				WIRE, RED, #30	AR
8				WIRE, GRN, #30	AR
7				WIRE, YEL, #30	AR
6				WIRE, BLK, #30	AR
5		ITT	M24308/26-1	LOCK, SCREW	2
4		VECTOR	CG2-95	MODULE, CARD MNT.	1
3		VECTOR	3662-2	BOARD, PLUG	1
2		NRAO	C13900P01	PCB, PC TRANSCEIVER	1
3 1		NRAO	C13900M13	PANEL, FRONT	1

C13900S02	SCHEMATIC
D13900P09	ASSEMBLY
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX) ±
2 PLACE DECIMALS (.XX) ±
1 PLACE DECIMALS (.X) ±

MATERIAL : 2

FINISH :

VLA TYPE/CODE: WYE MONITOR

TITLE: WYE MONITOR PC TRANSCEIVER MODULE ASSEMBLY

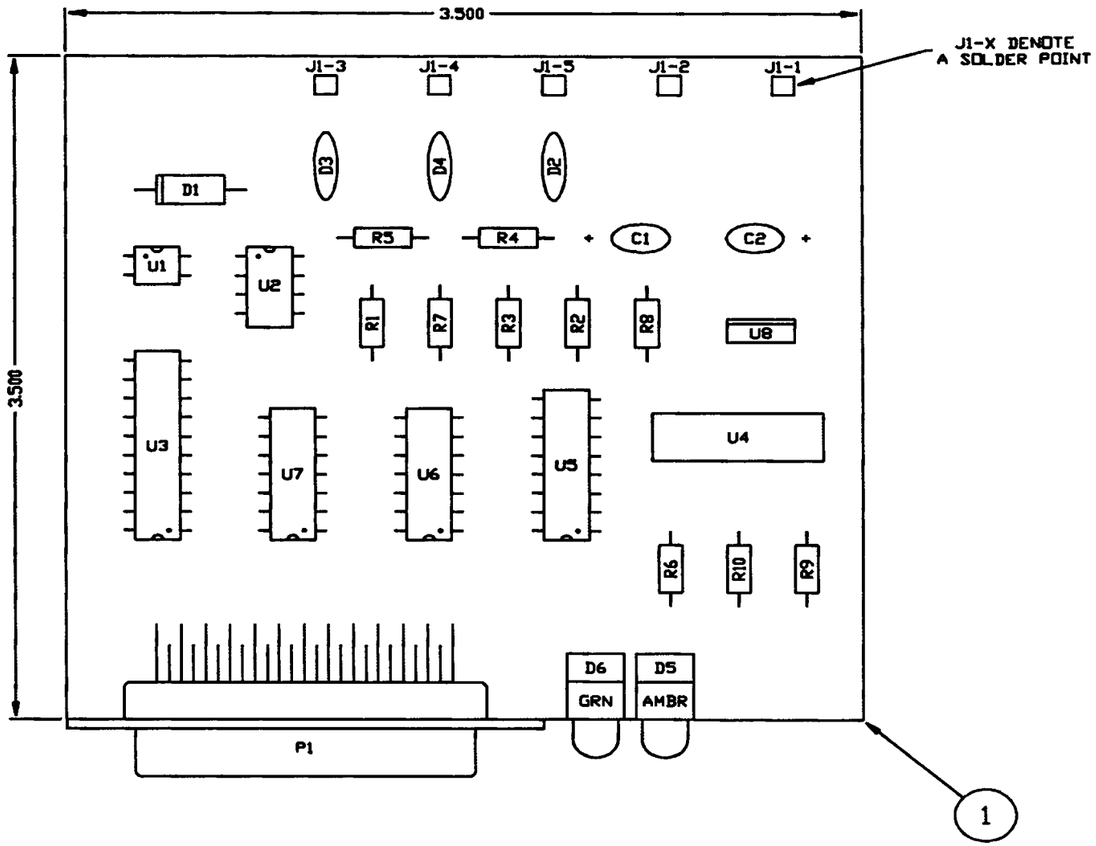
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 6-93
DESIGNED BY	DATE 6-93
APPROVED BY	DATE 6-93

SHEET NUMBER 1 OF 1 | DRAWING NUMBER C13900P13 | REV. - | SCALE 1/1

ACAD : 13900P13

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION



ITEM #	REF. DES.	MANUFACTURE	PART NUMBER	DESCRIPTION	QTY.
20	U8	NATIONAL	LM7805	REGULATOR	1
19	U7	SIGNETICS	74HCT32	14 PIN IC	1
18	U6	SIGNETICS	74HCT00	14 PIN IC	1
17	U5	NEC	DK# PS2501-4NEC	OPTOISOLATOR (4)	1
16	U4	BURR BROWN	HPR-105	DC - DC CONVERTER	1
15	U3	MAXIM	MAX233	RS-232 DRIVER/RECEIVER	1
14	U2	NATIONAL	LF155	OP AMP	1
13	U1	NEC	DK# PS2501-1NEC	OPTOISOLATOR (1)	1
12	R9, R10	———	———	470 OHM, 1/8W, 5% RESISTOR	2
11	R7, R8	———	———	51K OHM, 1/8W, 5% RESISTOR	2
10	R6	———	———	150 OHM, 1/8W, 5% RESISTOR	1
9	R2, R3, R4	———	———	330K OHM, 1/8W, 5% RESISTOR	3
8	R1, R5	———	———	10K OHM, 1/8W, 5% RESISTOR	2
7	P1	MOUSER	DB25-F	25 PIN, FEMALE CONNECTOR	1
6	D6	TDI	DK# L2006	PCB MOUNT LED, GRN	1
5	D5	TDI	DK# L2005	PCB MOUNT LED, AMBR	1
4	D2, D3, D4	PANASONIC	ERZ-C10DK680	ZNR TRANSIENT/SURGE ABSORBER	3
3	D1	———	1N914	DIODE	1
2	C1, C2	PANASONIC	———	10uF, 10V CAPACITOR	2
1	———	NRAO	SEE NOTE #1	CIRCUIT BOARD	1

NOTES :

1. ARTWORK = NRAO DWG# C13900AB01
   SILKSCREEN = NRAO DWG# C13900AB02
   DRILL DWG = NRAO DWG# C13900M01
2. DK = DIGI-KEY

C13900S02	SCHEMATIC
C13900M01	DRILL DWG.
C13900AB02	SILKSCREEN
C13900AB01	ARTWORK
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
3 PLACE DECIMALS (.XXX) ± .005
MATERIAL :
FINISH :

VLA PROJECT : WYE MONITOR

TITLE : WYE MONITOR
PC TRANSCEIVER
PCB ASSEMBLY

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

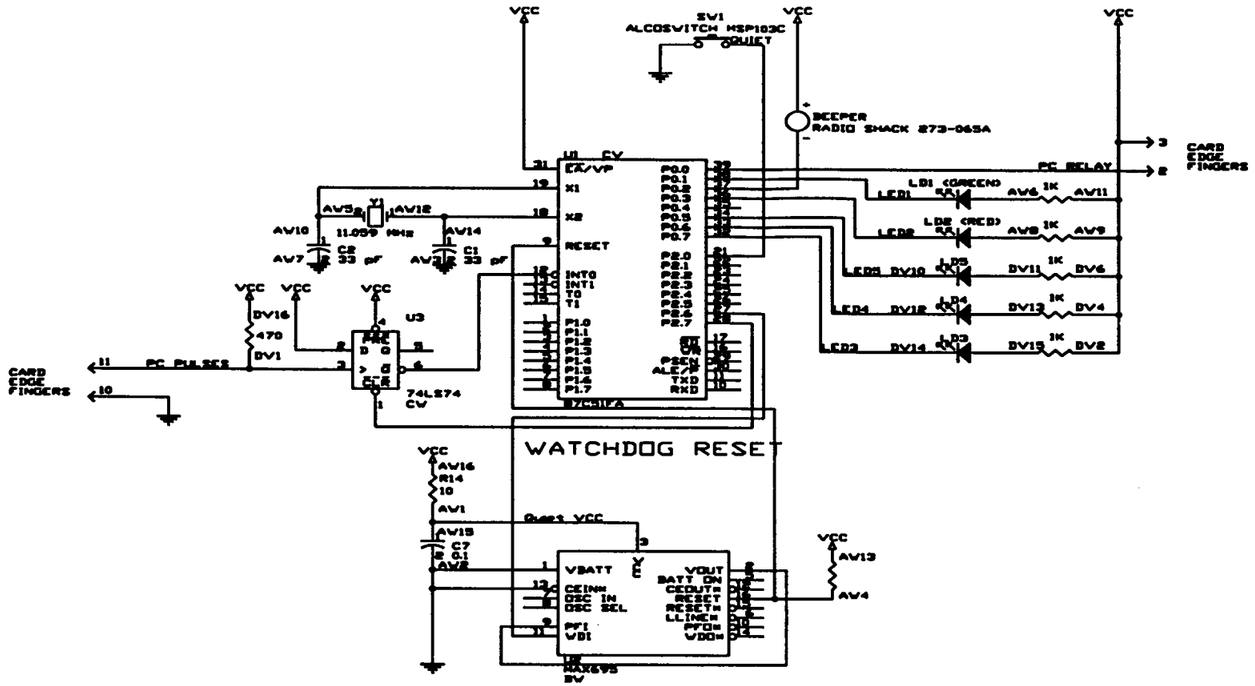
DRAWN BY	DATE 3-92
DESIGNED BY	DATE 1-92
APPROVED BY	DATE

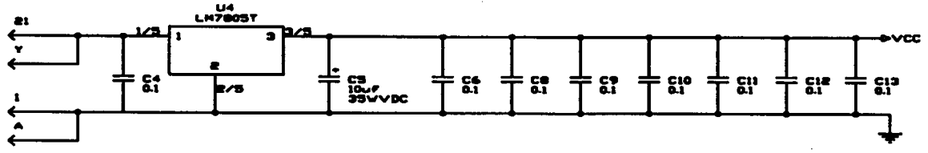
SHEET NUMBER 1 of 1 | DRAWING NUMBER C13900P01 | REV. | SCALE 2/1

ACAD : C3900P01
REF : VLA-11

NOTES:
1. LED1, LED2, AND SW1 ARE ON FRONT PANEL AND CONNECTED THROUGH WIRE-WRAP PINS

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	3-93			MINOR CORRECTIONS
B	6-93			ADDED POWER NEXT ASSY'S
C	8-93			REVERSED LEDS





ORCAD : 13900S06

PROPERTY OF NRAO

A13900P12	DIP HEADER ASSY
C13900P11	PCB ASSY
C13900P10	MODULE ASSY

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX) ±
2 PLACE DECIMALS (.XX) ±
1 PLACE DECIMALS (.X) ±

MATERIAL:

FINISH:

PROJECT: WYE MONITOR

TITLE: WYE MONITOR
PC WATCHDOG
CIRCUIT BOARD
SCHEMATIC DIAGRAM

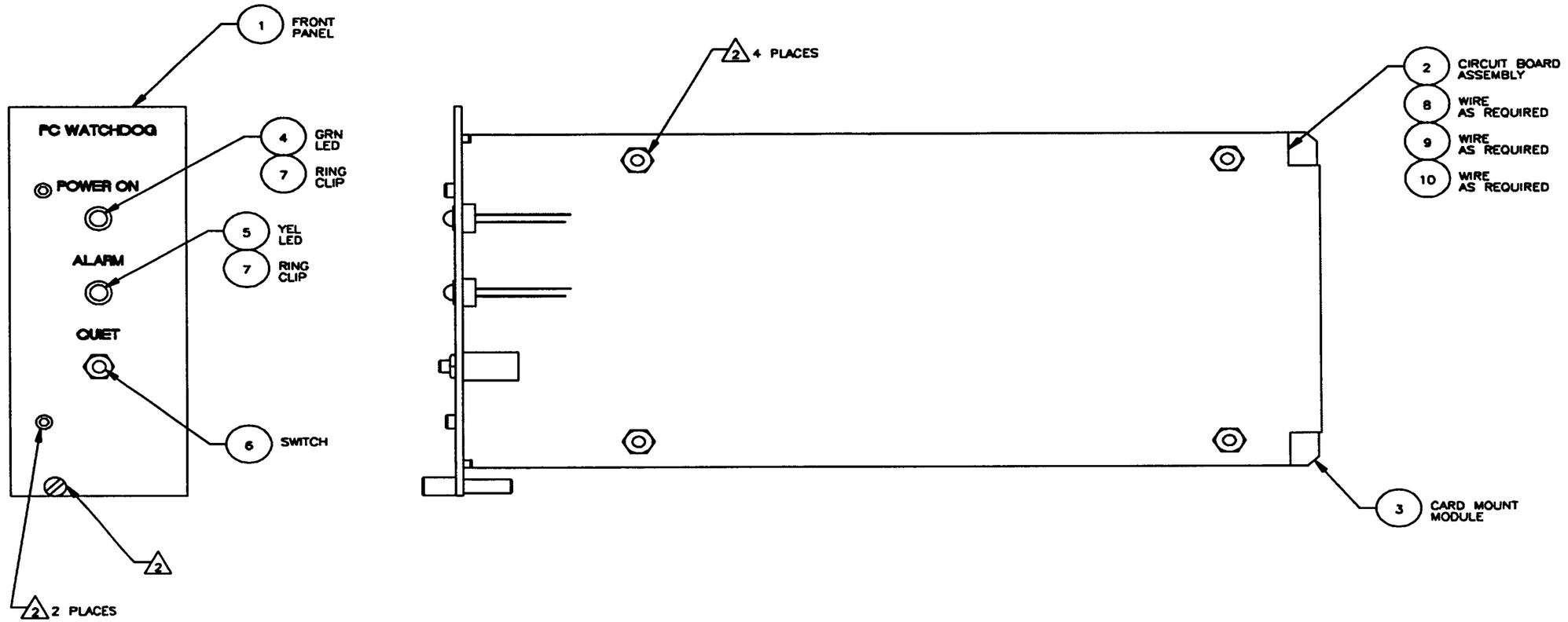
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO,NEW MEXICO 87801

DRAWN BY	DATE 2-93
DESIGNED BY	DATE 2-93
APPROVED BY	DATE 2-93
SHEET 1 OF 1	DRAWING C13900S06
REV C	SCALE NONE

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

NOTES:

1. REMOVE ALL BURRS AND SHARP EDGES
2. MOUNTING HARDWARE IS INCLUDED WITH CARD MOUNT MODULE (ITEM 3)



ITEM NO.	REF. DES.	MANUFACTURER	PART NUMBER	DESCRIPTION	QTY
10				WIRE, YEL, #30	AR
9				WIRE, BLU, #30	AR
8				WIRE, BLK/WHT, #30	AR
7		HEWLETT PACKARD	HLMP-0103	CLIP, RING	2
6	SW1	ALCOSWITCH	MSP103C	SWITCH, PSH. BUT.	1
5	LD2			LED, RED	1
4	LD1			LED, GREEN	1
3		VECTOR	CG2-95	MODULE, CARD MNT.	1
2		NRAO	C13900P11	ASSY, CIRCUIT BD.	1
1		NRAO	C13900M12	PANEL, FRONT	1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES : ANGLES ±
3 PLACE DECIMALS (.XXX) ±
2 PLACE DECIMALS (.XX) ±
1 PLACE DECIMALS (.X) ±

MATERIAL : 2

FINISH :

VLA PROJECT: WYE MONITOR

TITLE: WYE MONITOR
PC WATCHDOG
MODULE ASSEMBLY

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 6-93
DESIGNED BY	DATE 6-93
APPROVED BY	DATE 6-93

SHEET NUMBER 1 OF 1 | DRAWING NUMBER C13900P10 | REV. – | SCALE 1/1

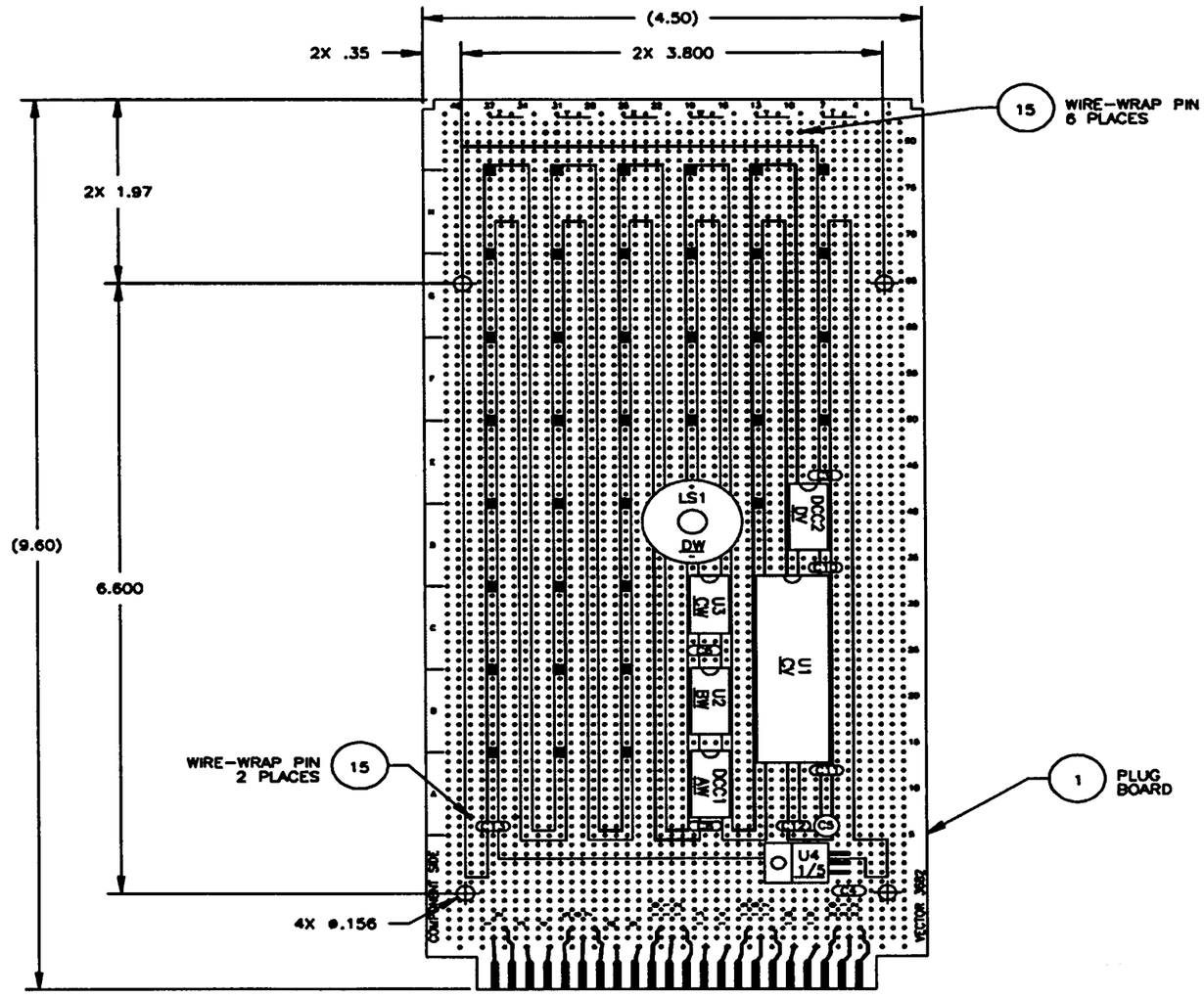
C13900S06	SCHEMATIC
D13900P09	ASSEMBLY
NEXT ASSEMBLY	DWG. TYPE

ACAD : 13900P10

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

NOTES:

1. REFER TO DIP HEADER ASSEMBLY, NRAO DRAWING NUMBER A13900P12
2. ASSEMBLED ON AUGAT 616-CG1T PLUG ADAPTER ASSEMBLY (ITEM 14)



DCC1 AW (1) (2)

1	10	16
	0.1uf	
	33pf	
	10K	
	11.0592 MHZ	
	1K	
	33pf	
8	1K	9

DCC2 DV (1) (2)

1	470	16
	1K	
	LED	
	1K	
	LED	
	1K	
	LED	
8		9

ITEM NO.	REF. DES.	MANUFACTURER	PART NUMBER	DESCRIPTION	QTY
15				PIN, WIRE-WRAP	8
14		AUGAT	616-CG1T	ADAPTER, PLUG	2
13	U1			SOCKET, 40-PIN	1
12	DCC1,DCC2, U2			SOCKET, 16-PIN	3
11	U3			SOCKET, 14-PIN	1
10	U4		LM7805T	IC, 3-PIN	1
9	U3	MOTOROLA	SN74LS74AN	IC, 14-PIN	1
8	U2	MAXIM	MAX695CPE	IC, 16-PIN	1
7	U1	INTEL	87C51FA	IC, 40-PIN	1
6	LS1	RADIO SHACK	273-065A	BEEPER	1
5	DCC1,DCC2	NRAO	A13900P12	ASSY, DIP HEADER	2
4	C5			CAPACITOR, 10uf	1
3	C3-C4 C6-C13			CAPACITOR, .01uf	10
2	C1, C2			CAPACITOR, 33pf	2
1		VECTOR	3682	BOARD, PLUG	1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES : ANGLES ±
2 PLACE DECIMALS (.XX) ± .005
3 PLACE DECIMALS (.XXX) ± .01
1 PLACE DECIMALS (.X) ±
MATERIAL :
FINISH :

PROJECT: VLA — WYE MONITOR

TITLE: WYE MONITOR PC WATCHDOG CIRCUIT BOARD ASSEMBLY

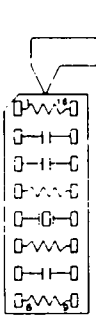
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY		DATE 6-93
DESIGNED BY		DATE 6-93
APPROVED BY		DATE 6-93

SHEET NUMBER 1 OF 1 | DRAWING NUMBER C13900P11 | REV. – | SCALE 1/1

C13900S06	SCHEMATIC
C13900P10	ASSEMBLY
NEXT ASSEMBLY	DWG. TYPE

ACAD : 13900P11



DESCRIPTION	VALUE	MFG.	PART NO.
DIP HEADER			
RESISTOR	10, 1/8W	ALLEN-BRADLEY	RC05GF100JS
CAPACITOR	0.1uf, 50VDC		
CAPACITOR	33pf, 200V	MALLORY	CK05BX330K
RESISTOR	10K, 1/8W	ALLEN-BRADLEY	RC05GF103JS
CRYSTAL	11.0592 MHZ	11.05ECS	
RESISTOR	1K, 1/8W	ALLEN-BRADLEY	RC05GF102JS
CAPACITOR	33pf, 200V	MALLORY	CK05BX330K
RESISTOR	1K, 1/8W	ALLEN-BRADLEY	RC05GF102JS

MODULE: PC WATCHDOG

BOARD LOCATION: AW

DIP HEADER

	DESCRIPTION	VALUE	MFG	PART NO
	RESISTOR	470, 1/4W	ALLEN-BRADLEY	RC07GF470JS
	RESISTOR	1K, 1/4W	ALLEN-BRADLEY	RC07GF102JS
	LED, GREEN			
	RESISTOR	1K, 1/4W	ALLEN-BRADLEY	RC07GF102JS
	LED, GREEN			
	RESISTOR	1K, 1/4W	ALLEN-BRADLEY	RC07GF102JS
	LED, GREEN			

MODULE: PC WATCHDOG

BOARD LOCATION: DV

A13900P12

SHEET 2 OF 3

NO. | DRAWING NO.

REVISIONS

REV	DATE	DRAWN BY	APPROVED BY	DESCRIPTION

C13900S06	SCHEMATIC	
C13900P11	ASSEMBLY	
NEXT ASSY	USED ON	

DRAWN BY DATE 6-93

DESIGNED BY DATE 6-93

APPROVED BY DATE 6-93

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

V L A

PROJECT WYE MONITOR

TITLE PC WATCHDOG CIRCUIT BOARD
DIP HEADER ASSEMBLY

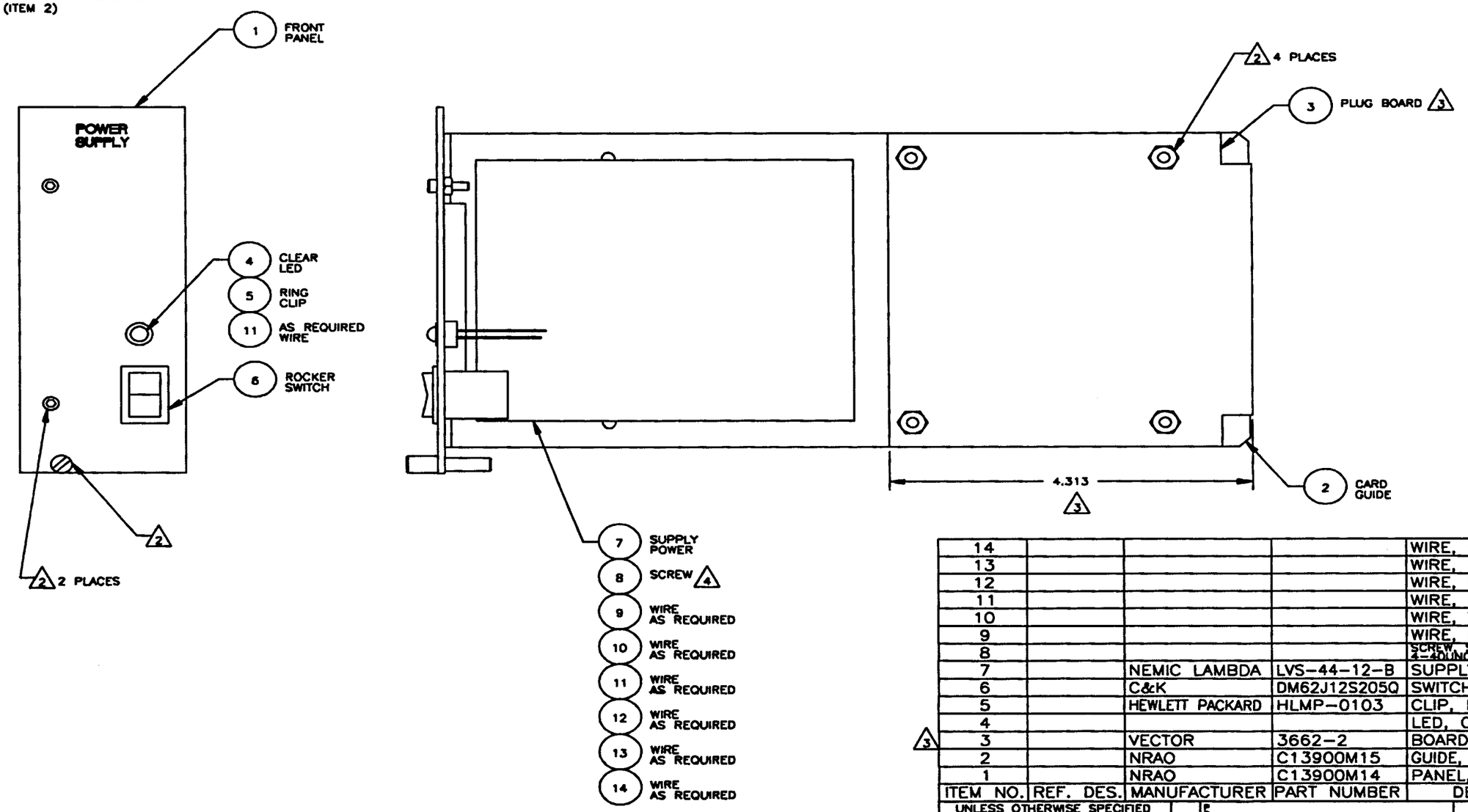
DWG NO A13900P12

SHEET 3 OF 3

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

NOTES:

1. REMOVE ALL BURRS AND SHARP EDGES
2. MOUNTING HARDWARE IS INCLUDED WITH CARD MOUNT MODULE (ITEM 3)
3. CUT PLUG BOARD (ITEM 3) AND MOUNT WITH EXISTING HARDWARE
4. LOCATED ON FAR SIDE OF CARD GUIDE (ITEM 2)



ITEM NO.	REF. DES.	MANUFACTURER	PART NUMBER	DESCRIPTION	QTY
14				WIRE, WHT, #22	AR
13				WIRE, GRN, #22	AR
12				WIRE, BLK, #22	AR
11				WIRE, RED/BLK, #30	AR
10				WIRE, YEL, #30	AR
9				WIRE, BLK, #30	AR
8				SCREW, SOCKET HEAD 4-40UNC-2A x .31	2
7		NEMIC LAMBDA	LVS-44-12-B	SUPPLY, POWER	1
6		C&K	DM62J12S205Q	SWITCH, ROCKER	1
5		HEWLETT PACKARD	HLMP-0103	CLIP, RING	1
4				LED, CLEAR	1
3		VECTOR	3662-2	BOARD, PLUG	1
2		NRAO	C13900M15	GUIDE, CARD	1
1		NRAO	C13900M14	PANEL, FRONT	1

D13900P09	ASSEMBLY
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES : ANGLES ±
3 PLACE DECIMALS (.XXX) ± .005
2 PLACE DECIMALS (.XX) ±
1 PLACE DECIMALS (.X) ±

MATERIAL : 2

FINISH :

VLA

WYE MONITOR

TITLE: WYE MONITOR POWER SUPPLY MODULE ASSEMBLY

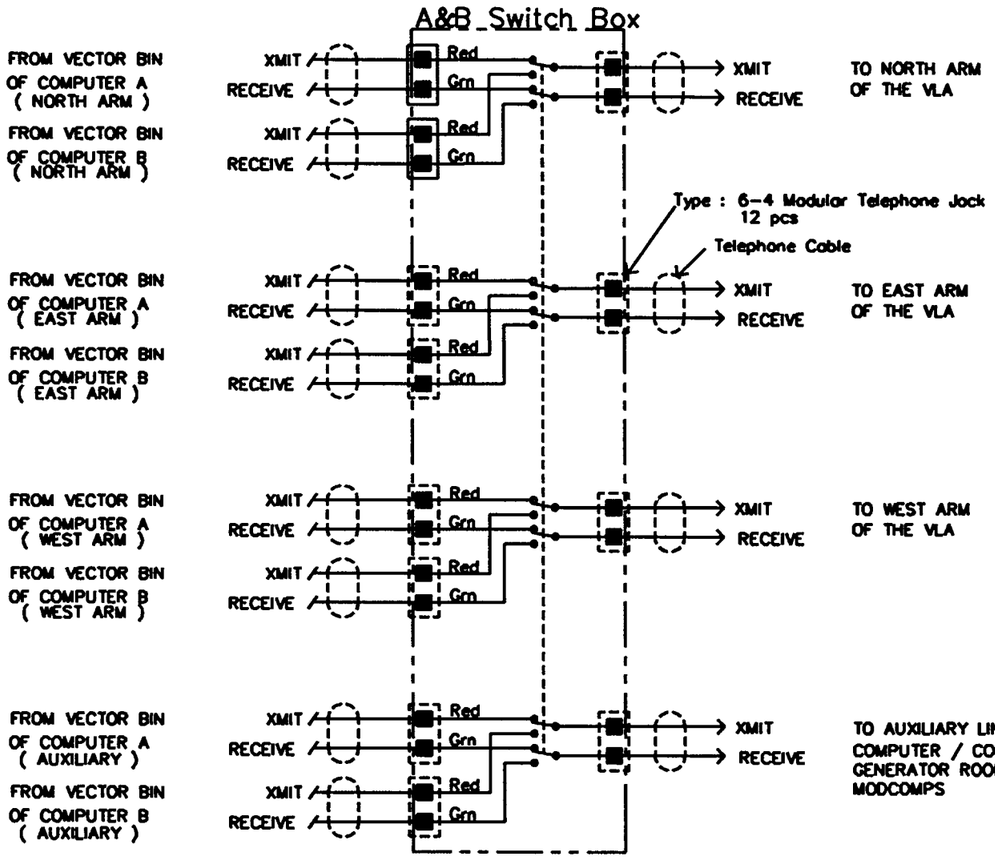
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 6-93
DESIGNED BY	DATE 6-93
APPROVED BY	DATE 6-93

SHEET NUMBER 1 OF 1 | DRAWING NUMBER C13900P14 | REV. – | SCALE 1/1

ACAD : 13900P14

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION



ACAD : 13900W07

NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES : ANGLES ±

3 PLACE DECIMALS (.XXX) ±

2 PLACE DECIMALS (.XX) ±

1 PLACE DECIMALS (.X) ±

MATERIAL :

FINISH :

VLA PROJECT: WYE MONITOR

TITLE: WYE MONITOR
A&B SWITCH BOX
WIRING DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 6-94
DESIGNED BY	DATE 6-94
APPROVED BY	DATE 6-94

SHEET NUMBER 1 OF 1 | DRAWING NUMBER B13900W07 | REV. — | SCALE NONE

2.8 Isolated CPU Interface Board

This section describes the Isolated CPU Interface PC Board that is used as a serial-to-parallel interface in all the control interface modules. The board transforms serial bus message interactions into 16 discrete parallel I/O lines that are connected to the control module's command and monitor interface circuitry. This board might be termed a "semi-standardized" interface in that while the bus line interface is standard for all applications, the board's parallel command/monitor interface circuitry is particularized to the module's device interface application. This particularliza tion is described below.

The device interface circuitry is installed on a logic connector board adjacent to the Isolated CPU Interface Board and is hard-wire connected to the board.

For convenience, the Isolated CPU Interface Board drawings follow this text; refer to them during the following description. The drawings are:

D13900P02 WYE Monitor Isolated CPU Interface Board Assembly

C13900S03 WYE Monitor Isolated CPU Interface Board Schematic Diagram

The board's bus line receive and drive circuitry is described in Section 2.4 above; refer to this description for details.

An important property is the isolation of the board's circuitry from high-voltage spikes on the I/O lines. Optically-coupled isolators in the board's bus line transmitter-receiver circuitry protect it from high voltage spikes that may be induced in the bus lines by lightning strikes to the antennas, rails, buildings and the earth. This also eliminates bus line common-mode signal perturbations to the receiving circuitry.

The board's parallel command/monitor lines are also optically isolated from the device interface circuitry; this protects the board's 87C51 microntroller and eliminates potential ground-loop interactions between the control interface modules and the controlled and monitored devices. Ground loop interactions can be very troublesome. The board's parallel interface circuitry is described below.

The optically-coupled isolators used on this board are NEC PS2501 and NEC PS2502 which have isolation break-down voltage ratings of $5kV_{RMS}$, MIN. The board's line driving and receiving circuitry power is provided by a Burr-Brown HPR105 which has an isolation voltage of 750 volts. Data sheets for the isolators and power supply are included in Section 5.

The heart of the board is an Intel 87C51FA microcontroller and its on-chip EPROM firmware. The 87C51FA, the serial interface and timers are described in Section 2.5; see that section and the 87C51 data sheets in Section 5 for details.

The 87C51's bidirectional I/O ports are the board's parallel interfaces. Ports 0 and 1 are the board's parallel command-monitor interface. The device's command state is written into the Port 0 and 1 latches and the two port's input circuitry reads the device's monitor state. The Port 0 and Port 1 latches are the interface board's command memories; the control module's device interface circitry performs only level adaption or inversion. The Port 2 lines read the Unit ID code hard-wired on the module's bin connector. The 87C51's I/O ports were described in Section 2.5 above. The Port 0 output buffers can sink 3.2 mA at 0.45 volts and require external pullups to drive inputs. Ports 1, 2 and 3 can sink 1.6 mA

at 0.45 volts. These ports can be driven by open-collector and open-drain outputs.

The parallel interface ports 0 and 1 levels are **active-low**; high is false and low is true. A Command message argument bit that is a 1 will be a low level on the associated 87C51 Port 0 and Port 1 command pins. Similarly, a low level monitor input to the 87C51 Ports 0 and 1 pins will be a 1 in the transmitted Monitor Acknowledge message. Port 2, the board's address line (Unit ID) inputs are **active-high**.

The board's 87C51 firmware requires that monitor (or fault) inputs be low. The firmware stores the active-low input state until the next Command or Monitor Request message from the control PC.

Section 2.2 has a very brief description of the board's 87C51 firmware; a separate manual will provide a more extensive description of the 87C51 firmware.

The system's message formats and protocol were discussed in Section 2.2.

The board's 16-bit parallel command output/monitor input circuitry consists of two sets of optical isolators; **either** (not both) a command opto-isolator **or** monitor opto-isolator is installed on each port line.

The **command output circuit** is a NEC PS2502-1 optically-coupled isolator with a Darlington output transistor pair. The isolator's current transfer ratio ranges between 200 to 2000%. When the Port 0 or Port 1 outputs are low, they sink about 0.3 mA current through a 10 kΩ resistor and the isolator's LED. A photo-Darlington isolator is used to avoid loading the 87C51's I/O ports. The isolator's switching times are about 3 microseconds. The isolation voltage is 5,000 volts and the transistor's BVCEO is 40 volts. The Darlington-output transistor's emittor and collector are connected to the board's parallel input/output pins. The output transistor's emittor and collector lines are referenced to the device's ground via the module's device interface circuitry. Note that when the port bit is a high, the output transistor is conducting and is non-conducting when the port output is a low. When a parallel input/output line is used for command output, the monitor input isolator is not installed and is out of the circuit. In some control interfaces (e.g. M26, M27), the command optical isolators are installed in the device interface circuitry.

The **monitor input circuit** is a NEC PS2501-1 optically-coupled isolator with a single photo-transistor output. The isolator's LED is connected to the same pair of pins as the command output isolator; only one isolator is permitted on a parallel bit line. The monitor input circuit is totally isolated from the board's circuitry. The isolator's current transfer ratio ranges between 80 to 600% and the LED drive current is determined by the device monitor circuitry. This current should be about 1.2 mA. The isolation voltage is 5,000 volts and the transistor's BVCEO is 80 volts. Switching times are about 3 microseconds. When a parallel input/output line is used for input, the output isolator is not installed. Both LED lines are connected to the parallel input/output pins. In some control interfaces (e.g. M26, M27), the monitor optical isolators are installed in the device interface circuitry.

The board's parallel input/output pins (J1 through J16) are 0.025 in, square wire-wrap pins. Wire-wrap wiring connects these outputs to the module's device interface circuitry. Since these pins are hard-wired to the device interface circuitry, this board is not a removable module.

To configure this board for service in one of the interface modules, install the command and monitor isolators as shown in the module's schematic diagram. Note that most of the board's isolators are monitor isolators because there are only a few command functions in the M26, M27 and M29 control

interface modules.

All eight 87C51 Port 2 pins are connected to J17 for use in the interface module. Pull-up resistors are not required because Port 2 has internal pull-up resistors. Six of the Port 2 pins and logic common are connected to the module I/O connector, P1. Five of these lines, Ports 2.0 through 2.4, are used to read the control module's 5-bit address (Unit ID) code and the bit weights are 2^0 (J17-1) through 2^4 (J17-5). The address code value is formed by jumpering the appropriate lines to logic common on the control interface module's bin backplane connector. As mentioned above, the address inputs are active-high so the address-encoding jumper connection are the **logic complement** of the address code. Port 2.5, address bit 2^5 (J17-6) is connected to P1, the control module's back-panel connector for potential future use as an address input in the event that the address space should ever exceed 32 addresses. In current use, this term is connected to logic ground on the bin backplane connector. Ports 2.6 and 2.7 (J17-7 and J17-8) have not been assigned any board or module function.

An 8-circuit dip-switch is connected to the Port 2 pins for convenience in bench-testing the board before installation in a control interface.

The board uses a MAX695 Microprocessor Supervisory chip to sense +5 volt power losses and as a watch-dog on the 87C51 program execution. If the +5 volt DC power drops below +4.65 volts, the MAX695 RESET pin outputs a high-true reset to the 87C51. When the DC power rises above the +4.65 volt threshold, an internal monostable holds the RESET line high an additional 200 mS to enable the processor clock oscillator to start. The 87C51 data sheet specifices a minimum reset period of 1 mS for crystal frequencies of 10 MHz. The 200 mS of additional delay on the RESET output is more than adequate.

The MAX695 has a WDI- input and an internal watch-dog timer. If OSC IN and OSC SEL are unconnected, the 87C51 firmware hold-off output (RD-, P3.7) must toggle the WDI pin once within a maximum period of 1.6 seconds; if this period is exceeded or the hold-off does not occur, the RESET output issues a 200 mS reset to the 87C51. In the event that the 87C51 does not toggle the WDI pin within the 1.6 second period, the MAX695 will issue another reset output. If program execution is not resumed, the reset pulse will be output at 1.6 second intervals. Each pass through the 87C51 firmware's main loop causes the hold-off output to toggle. There is no particular hold-off signal pulse rate because the recurrance rate may vary as a function of the program's message handling, etc. activity. The hold-off signal toggle period is much smaller than the MAX695's 1.6 second threshold value.

During development it was discovered that the MAX695 is rather sensitive to noise on the VCC terminal. This terminal is filtered by a 10Ω resistor and 0.1 µF capacitor RC filter to eliminate this problem. The VBATT pin is connected to ground. VBATT is a MAX695 battery backup function which is not implemented in the WYE Monitor system application.

The board is powered by an external 12 to 24 VDC DC power supply; the board's load on this power supply is 70 mA. The on-board logic, 87C51, and parallel interface circuitry is powered by an LM7805KC DC regulator. The board's line driver/receiver circuitry is powered by a Burr-Brown HPR105 flying capacitor ± 15 volt isolated power supply. The HPR105 is powered by +5 volt power from an LM7805KC DC regulator.

A 1N4007 series diode in the positive input power supply line protects the board and LM7805KC in the event that external power is inadvertently reversed. The 10 µF capacitor across the LM7805KC

input provides input filtering and a surge capacity for the regulator. The 10 μF and 0.1 μF capacitors on the output provide low and high frequency filtering of the regulator's output 5 volt power.

The LM7805KC DC input power is rated at a nominal +10 volts and the typical output voltage is +5 volts, and a minimum of +4.8 and a maximum +5.2 volts. Line regulation is ± 50 mV with a 100 mA load and load regulation is ±100 mV with a 500 mA load. The minimum input voltage is +7.2 to maintain line regulation. The LM7805 series has internal thermal overload and short circuit protection features.

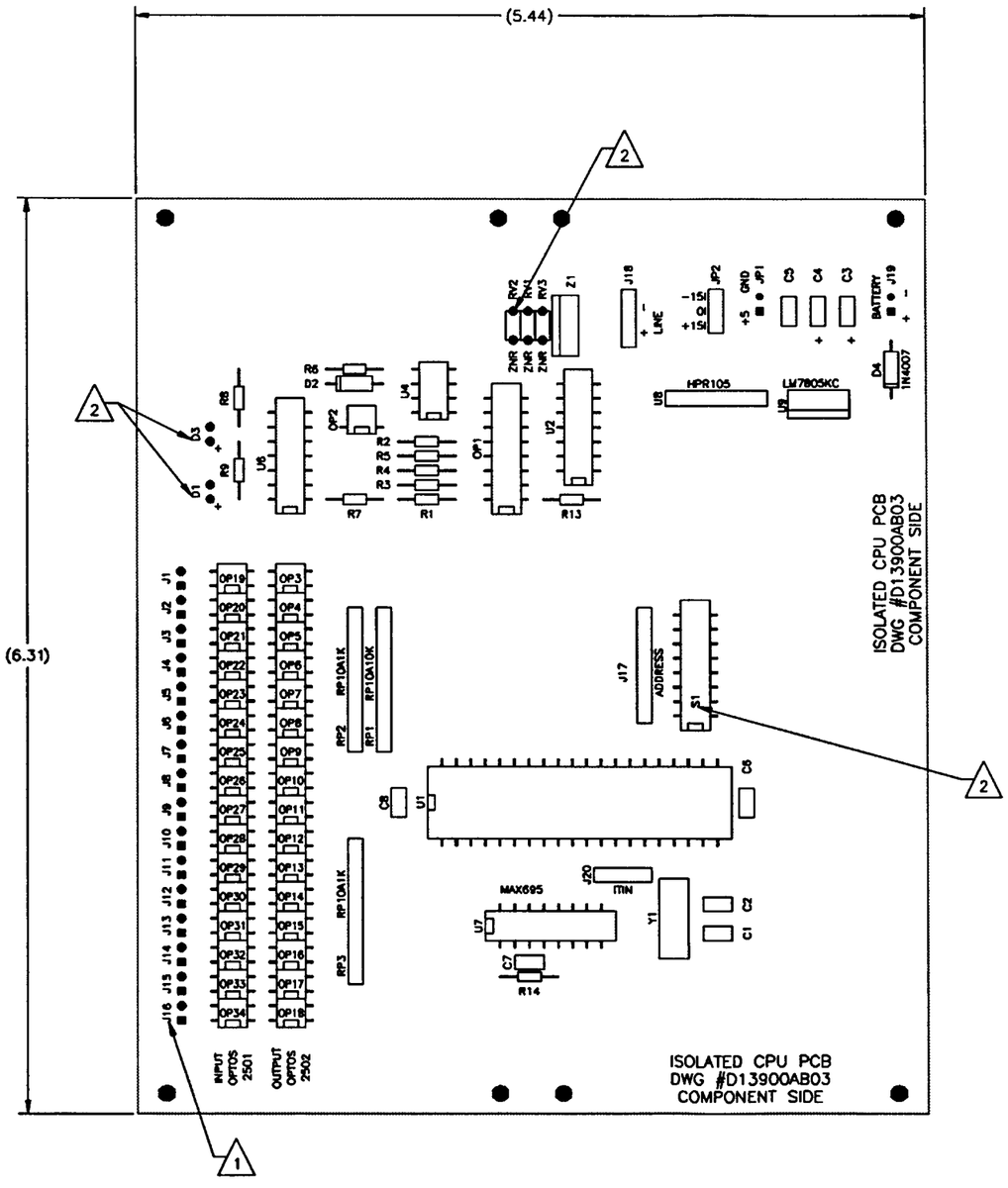
The HPR105 DC input power is rated at a nominal +5 volts with a minimum and maximum of +4.5 and +5.5, respectively. The power rating is 750 mW and the voltage setpoint accuracy is ±5%. Line regulation is 1%/%Vin and load regulation is 3% from 1 mA to rated load. The temperature coefficient is 0.01%/°C.

Data sheets for the 87C51FA, HPR105, NEC PS2501-1, NEC PS2502-1 and MAX695 are included in Section 5.

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

NOTES:

1. REFERENCE DESIGNATORS JXX AND JPXX = WIRE WRAP CONNECTIONS
2. NOT INSTALLED



ITEM NO.	REF. DES.	MANUFACTURER	PART NUMBER	DESCRIPTION	QTY
33	J1-J32 OP1-OP34			CONNECTOR, WIRE WRAP	51
32	U1	AMP	2-640379-3	SOCKET, 40-PIN	1
31	U4	AMP	2-640463-3	SOCKET, 8-PIN	1
30	OP1 W/ OP1-OP34	AMP	2-640358-3	SOCKET, 16-PIN	10
29	Z1	TECCOR	P1602	SURGE SUPPRESSOR	1
28	Y1	ECS	ECS-110.5-20-4	CRYSTAL, 11.0592 MHZ	1
27	U9	NATIONAL	LM7805KC	VOLTAGE REGULATOR	1
26	U8	BURR BROWN	HPR105	DC-DC CONVERTER	1
25	U7	MAXIM	MAX695	IC, 16-PIN	1
24	U6	SIGNETICS	74HCT32	IC, 14-PIN	1
23	U4	PMI	OP15	IC, 8-PIN	1
22	U2	SIGNETICS	74HCT00	IC, 14-PIN	1
21	U1	INTEL	87C51FA	IC, 40-PIN	1
20	S1		SW DIP-8	SWITCH	1
19	R14			RESISTOR, 10	1
18	R13			RESISTOR, 150	1
17	R8-R9			RESISTOR, 1K	2
16	R6-R7			RESISTOR, 10K	2
15	R3-R5			RESISTOR, 330K	3
14	R1-R2			RESISTOR, 51K	2
13	RV1-RV3	PANASONIC	ZNR 10K680	SURGE SUPPRESSOR	3
12	RP2-RP3		RP10A1K	RESISTOR PACK, 1K	2
11	RP1		RP10A10K	RESISTOR PACK, 10K	1
10	OP1-OP18	NEC	PS2502-1	OPTOISOLATOR	16
9	OP19-OP34	NEC	PS2501-1	OPTOISOLATOR	17
8	OP1	NEC	PS2501-4	OPTOISOLATOR	1
7	D4		1N4007	DIODE	1
6	D2		1N914	DIODE	1
5	D1, D3			LED	2
4	C5-C8			CAPACITOR, 0.1uf	4
3	C3, C4			CAPACITOR, 10uf	2
2	C1, C2			CAPACITOR, 33pf	2
1		NRAO	D13900AB03	CIRCUIT BOARD	1

C13900S03	SCHEMATIC
D13900M03	DRILL DWG
D13900AB06	SOLDER MASK
D13900AB05	SILKSCREEN
D13900AB03	ARTWORK
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
.005
MATERIAL :
FINISH :

PRODUCT: WYE MONITOR

TITLE: WYE MONITOR ISOLATED CPU INTERFACE BOARD ASSEMBLY

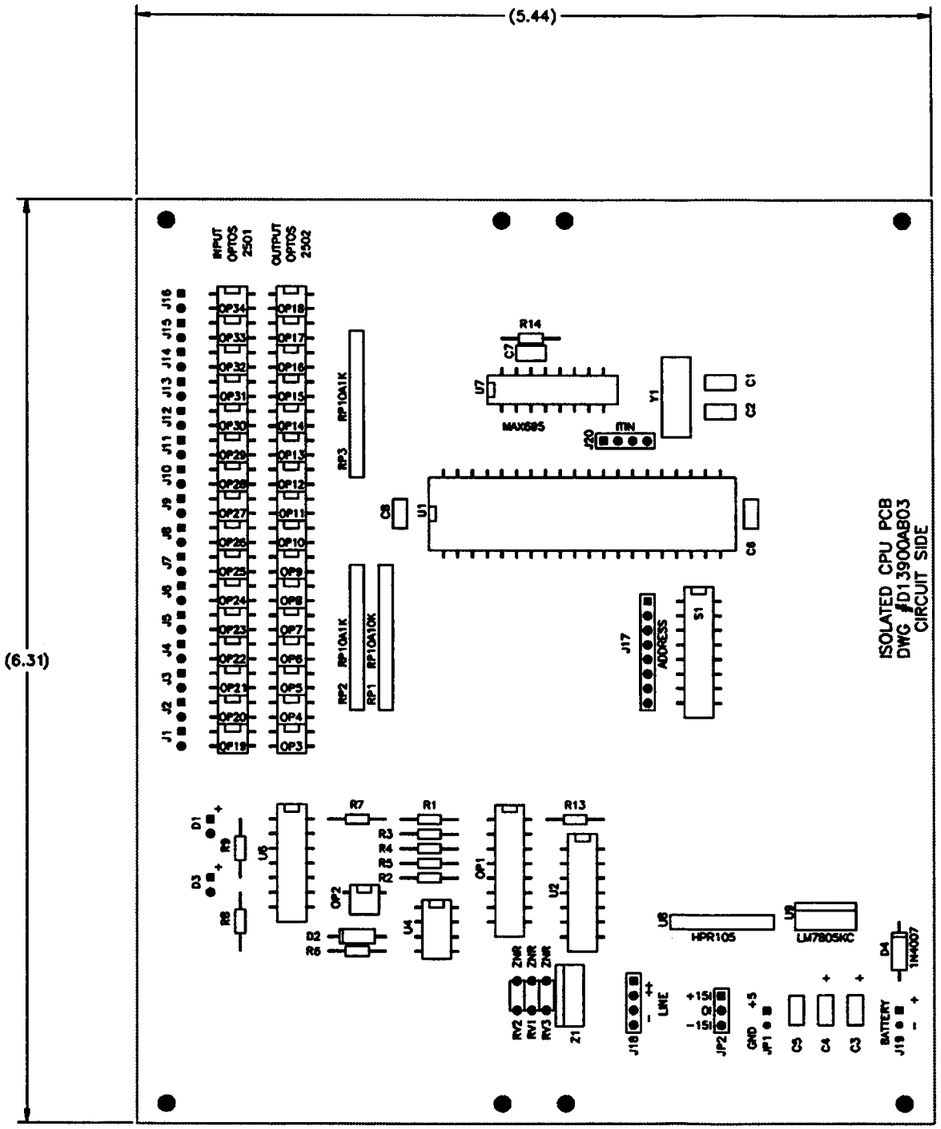
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY — DATE 9-92
DESIGNED BY — DATE 9-92
APPROVED BY — DATE 9-92

SHEET NUMBER 1 OF 2 | DRAWING NUMBER D13900P02 | REV. | SCALE 2/1

ACAD : 13900P2A

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION



ACAD : 13900P2B

C13900S03	SCHEMATIC
D13900M03	DRILL DWG
D13900AB06	SOLDER MASK
D13900AB05	SILKSCREEN
D13900AB03	ARTWORK
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
.005
MATERIAL :
FINISH :

VLA

WYE MONITOR

TITLE: WYE MONITOR ISOLATED CPU INTERFACE BOARD ASSEMBLY

SHEET NUMBER 2 or 2 | DRAWING NUMBER D13900P02 | REV. | SCALE 2/1

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 9-92
DESIGNED BY	DATE 9-92
APPROVED BY	DATE 9-92

REV.	DATE	DRAWN BY	APROV'D BY	DESCRIPTION
A	4-93			CHG3 U4 TO DP15FP

NOTES:

1. ⚠ ADDRESS MODULE. ADDRESS SWITCH S1 IS NOT INSTALLED EXCEPT FOR TESTING. ID IS BINARY WITH BITS GROUNDED TO DRIIVE TO 0 OR FLOATING FOR 1
2. ⚠ P1602 (Z1) REPLACES RV1, RV2, RV3
3. ⚠ INSTALL INPUT ISOLATORS PS2501 OR OUTPUT ISOLATORS PS2508 (BUT NOT BOTH TYPES) IN ANY I/O CHANNEL ID-0 TO ID-15
4. VCC = +5VOLTS

ISOLATED COMMUNICATION INTERFACE

ISOLATED I/O LINES ⚠

WATCHDOG RESET

POWER CONDITIONING

ORCAD : 13900S03

D13900P02	ASSEMBLY
D13900N03	DRILL DWG
D13900AB06	SOLDER MASK
D13900AB05	SILKSCREEN
D13900AB03	ARTWORK
NEXT ASSEMBLY	DWG TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX) ±
2 PLACE DECIMALS (.XX) ±
1 PLACE DECIMALS (.X) ±

MATERIAL:

FINISH:

VLA SCIENTIFIC

TITLE: WYE MONITOR

WYE MONITOR
ISOLATED CPU
INTERFACE BOARD
SCHEMATIC DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO,NEW MEXICO 87801

DRAWN BY	DATE 7-92
DESIGNED BY	DATE 7-92
APPROVED BY	DATE 7-92
SHEET NUMBER 1 OF 1	DRAWING NUMBER C13900S03 REV. A SCALE -

2.9 M26 Antenna Interface Module and its Interfaces with Antenna Systems

This section describes the M26 Antenna Interface Module and its interfaces with antenna systems. Like the other WYE Monitor control interface modules, M26 uses the Isolated CPU Interface Board to transform serial bus message interactions into 16 discrete parallel interactions with antenna interface circuitry. D13900S04 is the M26 schematic diagram. The antenna interface circuitry is installed on a wire-wrapped logic connector board in M26. Drawing D13900P06 is the M26 assembly drawing and drawing C13900P017 shows the interface circuit's component layout on the logic connector board. Reduced-scale copies of the M26 functional drawings follow this text.

Sections 2.2 and 2.4 described the message formats, protocol, and line driving and receiving. Section 2.8 described the Isolated CPU Interface Board.

The M26's are connected to the North, East and West arm WYE Monitor Buses.

The major subjects of this section are the character of the interface signals, the interface circuits that adapt these signals to the Isolated CPU Interface Board, and the M26 power circuitry.

M26 is installed in bin position 7 in the F/R System Bin "X"; there are no interconnections or functional links to the F/R System. The antenna systems interface signals are connected to M26 via the WYE Monitor System bin I/O connector installed behind bin position 5. The WYE Monitor bus signal from the antenna WYE-COMM terminal block is connected to this connector. Interface signals from this connector fan out to the ACU, Pedestal Room Junction Box, the Azimuth Drive Cabinet, the 28 volt relay power supply, and a 9 volt wall transformer (NCP power monitor). This antenna interface wiring is shown on drawing D13900W01.

M26 is powered by 24 volts DC from the antenna fire alarm system batteries - an uninterruptable power source. The battery's charge is maintained by a 110 VAC-powered, trickle-charger. Fire Alarm Control Panel terminals Aux 1 and 2 are the connection point for the M26 DC power lines that are routed through the WYE Monitor System bin I/O connector.

Antenna systems serviced by M26 are the ACU, ACU Fault Board, Emergency-Stop circuitry, Stow Monitor circuitry, Fire Alarm, Non-Critical Power (NCP), Non-Critical Power breaker, and the Critical Power phase-loss monitor circuitry. These functions and their interface characteristics are tabulated below. Descriptions of the command and monitor interface circuits follow the table.

The M26 command psuedo-switches and monitor states are shown in Figure 3, the Antenna status subscreen.

M26 outputs three command discretes and inputs nine monitor discretes. In the event that additional command or monitor functions are required, four spare parallel Isolated CPU Interface Board bits are available for assignment to command or monitor functions. M26 also monitors ACU functions not implemented in the ACU via an ACU Fault Board installed in the ACU. The ACU Fault Board is described below.

M26 functional and related drawings are listed below; for convenient reference, reduced-scale copies follow this section's text.

D13900P06	WYE Monitor M26 Antenna Interface Module Assembly
A13900Z01	M26 Antenna Interface Module BOM
D13900S04	WYE Monitor M26 Antenna Interface Module Schematic Diagram
C13900P07	M26 Antenna Interface Module Wire-Wrap Board Component Layout
C13900W02	M26 Module 37-Pin Connector Test Points Wiring Diagram
A13900P04	M26 Dip Header Assembly
D13900W01	WYE Monitor Wiring Diagram
C13900P05	ACU Fault Printed Circuit Board Assembly
C13900S09	ACU Fault Printed Circuit Board Schematic Diagram

Front Panel Test Point Connector

For convenience in locally checking the antenna system's interface signals, WYE Monitor bus signal and M26 power, M26 has a front panel test connector J1, which is a 37 contact "D" series socket connector. Note from the M26 module schematic drawing that a level-shifted version of all antenna systems interface signals are connected to this test point connector. Drawing A13900W02 shows the contact-signal assignments.

Note from the M26 schematic that the command and monitor and command test point signal levels are quite different. With the exception of the E-Stop command monitor which is +24 volts (when the command is active), the monitor signal test points are all across the input optoisolator's LED; therefore, the signal levels are small and depend upon the circuit's characteristics. The highest level will be about +1.1 volts, which is the optoisolator LED's forward voltage. The low levels will be 0 volts for contact closures or power supply inputs and about +0.2 volts for inverting optoisolator cases. In these optoisolator cases, the level is about +0.2 volts, which is the V_{CE} of the inverting optoisolator's output transistor.

In the cases of command outputs, the test point connections are all across the command circuit's relay coils; therefore the signal levels will be +24 or about +0.9 volts, the optoisolator's output transistor V_{CE}.

Antenna Systems Interface Signal Characteristics

Int Bd Signal	Function	Signal Type	M26 Module I/O Pins & Levels	Int BD Port State*	Signal Function
I000 (C)**	E-Stop Command	SPDT Relay Contacts	P1-P & P1-M open closed	 Low, 0 High, 1	 E-Stop Cmd No E-Stop Cmd
I001 (C)	DFR (ACU Reset) Command	SPDT Relay Contacts	P1-S & P1-U open closed	 Low, 0 High, 1	 Command Active Command Inactive
I002 (C)	NCP Breaker Reset	SPDT Relay Contacts	P1-W & P1-Y open closed	 Low, 0 High, 1	 Command Active Command Inactive
I003 (C or M)***	Spare function				
I004 (C or M)***	Spare function				
I005 (C or M)***	Spare function				

I006	(C or M)***	Spare function				
I007	(M)	ACU Manual Mode	DC voltage	P1-v & P1-x		
				+5 to 12 VDC	Low, 0	Manual Mode
				0 volts	High, 1	Computer Mode
I008	(M)	Emergency Stop Cmd State	DC voltage	P1-w & P1-y		
				+28 VDC	low, 0	E-Stop Mode
				0 volts	High, 1	Drive Mode
I009	(M)	ACU Fault Mon	TTL level	P1-T & P1-V		
				TTL high	Low, 0	ACU Fault
				TTL low	High, 1	No ACU Fault
I010	(M)	Non Critical Power Monitor	DC voltage	P1-X & P1-Z		
				+13 VDC	High, 1	NCP OK
				0 volts	Low, 0	NCP Fault
I011	(M)	28 VDC Relay PS Monitor	DC voltage	P1-F & P1-L		
				+28 VDC	High, 1	Relay PS OK
				0 volts	Low, 0	PS Fault
I012	(M)	Stow Monitor	DC voltage	P1-f & P1-j		
				+28 VDC	Low, 0	Ant Stowed
				0 volts	High, 1	Not Stowed
I013	(M)	Critical Power Phase Loss	DC Voltage	P1-m & P1-p		
				+28 VDC	High, 1	AC Power OK
				0 volts	Low, 0	AC Fault
I014	(M)	Fire Alarm	DC voltage	P1-s & P1-u		
				+28 VDC	High, 1	No Fire Alarm
				0 volts	Low, 0	Fire Alarm
I015	(M)	Local E-Stop Switch Mon	DC voltage	P1-w & P1-y		
				+28 VDC	High, 1	Loc E-Stop Off
				0 volts	Low, 0	Loc E-Stop On

* At the 87C51 port pin
** C denotes a command function and M denotes a monitor function.
*** These ports can be configured as either command or monitor functions.

Note that when WYE Monitor system commands are not active and there are no faults, the Isolated CPU Interface Board monitor data port states (at the 87C51 Port 0 and Port 1 pins) are all high. The 87C51 firmware inverts this port bit sense so that the Monitor Acknowledge message bits are all 0's for this no-fault case.

Command Interface Circuits

Command optoisolators (NEC PS2502-1) are installed in the Isolated CPU Interface Board ports IO0, IO1 and IO2. Monitor optoisolators are not installed in these ports.

Note that the three command circuits are very similar and use the same Hamlin SPDT relay. The differences between the three circuits are the relay contact assignments. In the three command circuits, only one set of relay contacts is connected to the module I/O connector; the other set is not used. When a command message bit is a 1, the associated 87C51 port bit state is a low. This low signal sinks current through the command output optoisolator's LED. This causes the Darlington-connected output transistors to conduct, thereby sinking current from the +28 volt relay supply through the relay, to the supply's return.

When active, the Emergency-Stop command NC relay contacts open to interrupt current flow in the E-Stop relay in the servo drive cabinet; this disables the antenna position servo amplifier drives and holds the antenna azimuth and elevation positions constant. The Emergency-Stop circuit consists of a series connection of these Emergency-Stop command NC contacts and the NC contacts in three manual Emergency Stop switches. If all NC contacts are closed, the relay supply +28 volts powers the E-Stop relay in the servo drive cabinet.

When active, the DFR (ACU Reset) command NO relay contacts closure applies 28 volt power to an external 28 volt relay. The ACU's 110 VAC power is routed through the relay's NC contacts. When the command is active, the ACU's power is interrupted and the ACU's +5 volt logic power supply quickly discharges. The command remains active for five seconds. At the end of this period, the command is reset to the inactive state and the ACU's 110 VAC power is re-applied. This induces a reset of the ACU's logic circuitry.

When active, the NCPR (Non-Critical Power Reset) command NO relay contacts apply 28 volt power to the reset coil of the Non-Critical Power circuit breaker. This command remains active for two seconds; at the end of this period, the command is reset to the inactive state.

The Hamlin HE721C2410 is a dry reed relay with a contact rating of 3 Watts, 0.25 Amps, and 175 volts. The coil resistance is 2000 Ohms, is designed for 24 volt operation and has an internal clipping diode.

Monitor Interface Circuits

Monitor optoisolators (NEC PS2501-1) are installed in the Isolated CPU Interface Board ports IO7 through IO15. Command optoisolators are not installed in these ports.

The M26 schematic diagram shows a variety of monitor circuit types. Roughly there are two classes: non-inverting inputs and inverting inputs. Inversion is implemented by adding a second series optoisolator to the monitor input circuit. Note from the table above that when there are no faults, no Emergency Stops, and the antenna is in the observing mode, the Isolated CPU Interface Board port states are all 0's (high). The 87C51 firmware inverts this sense so that the message data bits are all 0's. When a monitored signal is a voltage in the non-fault state without inversion, the Isolated CPU Interface port state would be a 0 because of the inversion of the monitor input optoisolator. The inverting optoisolators are used to make all the port states 1's for non-fault conditions. This all-1's state simplifies the PC control program's analysis of the monitor data.

When a monitor signal is an active high voltage, the inverting optoisolator's output transistor sinks about 0.9 mA and the V_{CE} is about +0.2 volts, which is below the monitor input optoisolator LED's 1.2 to 1.4 volts operating voltage. As a result, the monitor input LED does not emit and the port state is a high.

The monitored antenna functions active-high voltage levels fall into two classes: about +13 volts (ACU Fault Monitor and Non-Critical Power Monitor), and the balance at +24 to +28 volts. The current limiting resistors for the inverting and noninverting optoisolator's LEDs limit the input current to about 2 to 3 mA, except for the relay supply monitor which is about 6 mA.

A special case is the +28 volt relay power supply monitor, which has a 20-volt Zener diode in series with the 1 kΩ current limiting resistor on the inverting optoisolator's LED input. The relay power supply is a non-regulated supply that has a number of loads which make it's output somewhat variable. If the relay supply voltage is too low to reliably operate the relays, the +28 volt relay supply monitor will report a fault.

Another special case is the monitor circuit for the E-Stop command, port IO8. When the command is active, the E-Stop command relay's NO contact feeds about 2.5 mA from the +28 volt level of the E-Stop circuit into the monitor port optoisolator to verify that the E-Stop command is working. The optoisolator's LED anode is connected to the relay supply return.

The E-Stop command circuit description above mentioned a 28 volt E-Stop relay in the servo drive cabinet. The voltage across the relay coil is sensed by the Local E-Stop Monitor input. If an E-Stop command is not active, the Local E-Stop monitor input is 28 volts. When a manual E-Stop switch is actuated or the E-Stop command is active, the 28 volt power to the relay coil is interrupted and the input to the inverting optoisolator is zero volts. This level is inverted by an inverting optoisolator so that the IO15 port state is low.

The antenna stow position sensors are a pair of mercury switches in the Vertex Room junction box. The switches are mounted side-by-side and are oriented to make the contact closures a function of elevation position. Switch 1 closes when elevation position is < about 85° and switch 2 closes when elevation position > about 95°. When the antenna is properly stowed, both sets of switch contacts are open. The contacts are connected in parallel and wired to the Stow Monitor input; if the antenna is properly stowed, both sets of contacts open and current from the Fire Alarm batteries drives the monitor optoisolator LED through a 10 kΩ limiting resistor.

Spare Functions

Note that both command optoisolators (NEC PS2502-1) and monitor optoisolators (NEC PS2501-1) are not installed on spare Isolated CPU Interface Board ports IO3, IO4, IO5 and IO6. Monitor data readout of these spare ports is a 1 because the port pull-up resistors pull the floating port pins to +5 volts. Spare I/O ports can be assigned to either a command or a Monitor function by installing the appropriate optoisolators and interface circuitry.

M26 Address Inputs

The M26 address line (Unit ID) inputs are encoded to enable the Isolated CPU Interface board to determine if the module is the target of a Command or Monitor Request messages. It also uses the encoded value in formatting Command or Monitor Acknowledge messages transmitted to the control PC. The M26 address line inputs are **active-high** and the code is formed by connecting the appropriate address line inputs to logic common (J1-FF) on J1, the bin back-plane connector. The encoded address is the binary equivalent of the antenna serial number, and the ground connections are the complement of this encoded value. J1-DD is the LSB (2^0) and J1-z (2^4) is the MSB. J-1AA (2^5) is always connected to logic common in the address line ground string.

ACU Fault Board

The ACU Fault Board (schematic diagram C13900S09) is a printed circuit board installed in the ACU to monitor the ACU power supply voltages, drive limits, and drive-fault ACU discretes. This board is functionally an extension of the M26 but was installed in the ACU to reduce and simplify the ACU modification wiring that would otherwise have been required to implement the additional ACU monitoring functions. A 25-contact, 0.025 in square-post header on the board, connects the board circuitry to the ACU. The ACU's signal and power inputs are connected to the ACU Fault Board by a cable connected to the header.

The ACU Fault Board limit-tests the ACU's +5V, +15V, and -15V power supply voltages using the LTC1042 Window Comparator. This comparator uses a pair of externally-supplied voltages, a reference voltage (CENTER), and tolerance (WINDOW) voltage; these define the middle and width of the comparison window. The LTC1042 compares VIN with these two references to determine if voltage is within the comparison window. If it is within the window, the WITHIN window output is high, a logic 1; otherwise it is a logic 0. The LTC1042 features low reference and window comparison errors, ±1 mV max and ±2 max respectively. The LTC1042 is a sampling comparator that can be strobed or use an external resistor and capacitor on the OSC pin to determine the frequency of an internal sampling oscillator. When the voltage on the OSC pin is near VCC, the comparator samples the analog signal. The three comparator circuits use a +2.5 volt reference voltage (W.C.) and +0.187 volt (WIDTH/2) window voltage from a high-precision reference divider described below. In the ACU Fault Board application, the OSC pin is connected to VCC to force the sampling to be continuous. Section 5 includes a data sheet for the LTC 1042.

Power supply and reference voltages required by the ACU Fault Board circuitry are generated on the board. The ACU Fault board power division and regulator circuitry uses two ACU voltages, +28 VDC and -28 VDC, to generate: +5V (VCC): +15V (Z+15); -15V (Z-15); +2.5V REF; and +0.187V REF.

VCC is generated by a 7805 regulator from the ACU's +28 volt supply. The 7805 has 2.2 μF capacitors on the 7805 input and output and six additional 0.1 μF capacitors on the output filter VCC's noise because it is used as a reference by the LTC1042 analog limit comparator chips. VCC is also used to power the 74HCT688 comparators and 74HCT04 inverters.

Two 2.5 volt LT1004 precision, shunt-regulator diodes in a series voltage divider circuit provide three accurate reference voltages: +5V REF, +2.5V REF, and +.187V REF. The 2.5 V REF and .187V REF voltages are used as reference voltages by the LTC1042. The +5V REF voltage is not used. The LT1004 voltage outputs are accurate to ±5 mV. Section 5 includes a data sheet for the LT1004.

A resistive voltage divider on the ACU's +5V produces +2.5 volts and the divider output is filtered by a shunt 0.1 μF capacitor. This +2.5 volt level is connected to the LTC1042 VIN input. A 74HCT04 inverts the comparator's output for input to the 74HCT688 8-bit magnitude comparator, which performs exclusive NOR-sums ACU voltage or discrete faults for input to the M26 ACU Fault input.

A resistive voltage divider on the ACU's +15V provides +2.504 volts and the divider output is filtered by a shunt 0.1 μF capacitor. This +2.504 volt level is connected to the LTC1042 VIN input, as was the case in the +5V in the paragraph above. In a similar manner, the comparator's WITHIN output is connected to the 74HCT688 comparator via an inverter.

The ACU's -15V is translated to a positive voltage by the OP-15 operational amplifier connected as a simple inverting amplifier with a gain of 0.166. This polarity inversion is done because the LTC1042 operates on positive voltage inputs. The amplifier's output is +2.490 volts which is connected to a third LTC1042. Like the two circuits above, the LTC1042's WITHIN output is connected to the 74HCT688 via an inverter.

The 74HCT688 is an expandable 8-bit active-low equality detector. Two sets of 8-bit inputs, P_n and Q_n (where n = 1, ... 8), are compared by exclusive-NOR gates. The output is low-true when all $P_n = Q_n$ and enable input G is low-true. Refer to a TTL data book for more details on the chip's logic.

The P_n inputs to U2 are the three high-true voltage comparisons and four low-true drive fault discretes (AZ-1, AZ-2, EL-1 and EL-2) from the ACU[1]. If the ACU does not detect drive faults, these terms are low; in the event of a fault, one or more terms will go high and force the comparator output high. The Q_n inputs are connected to logic common; this requires the P_n inputs to be low-true for the comparison. The P_3 input on U2 is not used; therefore it is connected to logic common.

The P_n inputs to U1 are the eight high-true azimuth and elevation limit switch discretes from the ACU. During operation in the normal angular drive ranges, these terms are low. If either drive encroaches on the limits of its drive range, a limit switch is actuated. There are two sets of terms, AZ-1 and AZ-2; AZ-1 goes true first, and an additional drive in the same direction activates AZ-2. The ACU's internal control circuitry uses these terms in its logical control of the servo amplifiers. The M26 readout of these terms is a monitoring adjunct of the ACU because these limit and drive fault discretes are read out of the ACU in monitor words 212 (octal).

M26 Power

As mentioned above, the M26 is powered by the 24 volt output of the Fire Alarm batteries. The M26's +5 VDC power is provided by a Polytron TW1.8-24S5 regulated DC/DC converter installed on the logic connector board. The max output current load is rated at 360 mA and the efficiency is 55%. The converter has a 500 volt input-output isolation. The line and load regulation are ±0.5% Max and ±1% Max, respectively. The output voltage accuracy is ±5% and the voltage temperature coefficient is 0.02%/degree C. Ripple and noise are 50 mVp-p maximum. A TW1.8-24S5 data sheet is included in Section 5.

The +5 VDC power from the TW1.824S5 converter-regulator is connected to the Isolated CPU Interface board via JP1 on the Isolated CPU Interface Board, and the board's LM7805KC is not used. The board's HPR105 DC/DC converter is used and generates the isolated +15V and -15V used by the line driving-receiving circuitry.

---

[1] The installation of the four drive fault and eight limit switch inputs from the ACU is a future ACU modification. The ACU's +5 volt and + and - 15 volt power supply monitors are connected to the ACU Fault Board.

ACU Discretes and their relationships to M26 Discretes

A comparison of the antenna discretes monitored by the M26 and the ACU shows three apparent redundancies: ACU bits 22 (Stow Pin) and 23 (Emergency Stop) in ACU monitor word 211 and bit 24 (Fire Detection System Malfunction) in ACU monitor word 212_8. These bits and words are in octal format (See the ACU manual). A description of these two sets of functions follows.

The antenna azimuth and elevation drives each have a stow pin that can be inserted into a stow recess; a Stow Pin switch on each pin senses the position of the stow pin. The switches are input to the ACU to inhibit the drive servo amplifiers in the event that either stow pin is inserted into a stow recess. The ACU also formats the OR of the two switch states into bit 22 of word 211_8. The stow pins are seldom, if ever, used but are probably still operative. The stow state monitored by the WYE Monitor system is not related to the stow pin switches described above.

The two antenna smoke alarm units have a malfunction output (NO contacts) that indicates a **detector fault state**. These outputs are connected in parallel (OR connection) and sensed by the ACU, which formats the OR state into bit 24 of word 212_8. The WYE Monitor system monitors the OR of the smoke detector's **fire alarm** NO contacts; thus these two monitors are separate functions and the Fire Detection System Malfunction sensed by the ACU is still very important. See the interface circuit description below.

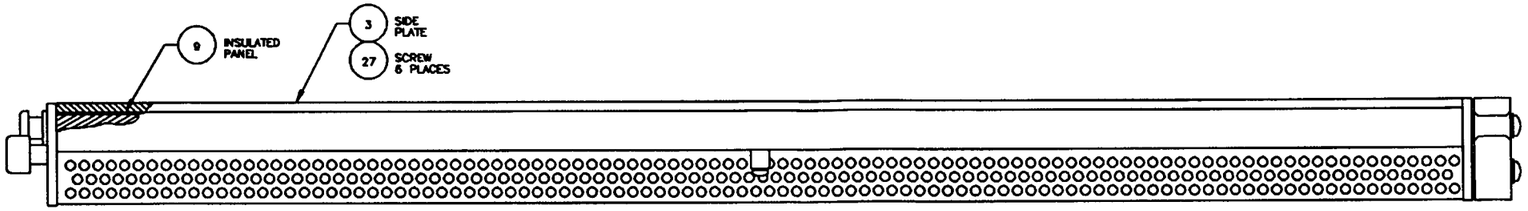
The Emergency-Stop relay in the drive cabinet was mentioned above. Contacts on this relay are connected to bit 23 of word ACU monitor word 211_8; this Emergency-Stop monitoring is used by the antenna control programs. Although both sets of Emergency-Stop command and monitoring circuitry are closely related, the WYE Monitor circuitry is electrically isolated from the ACU and antenna drive equipment.

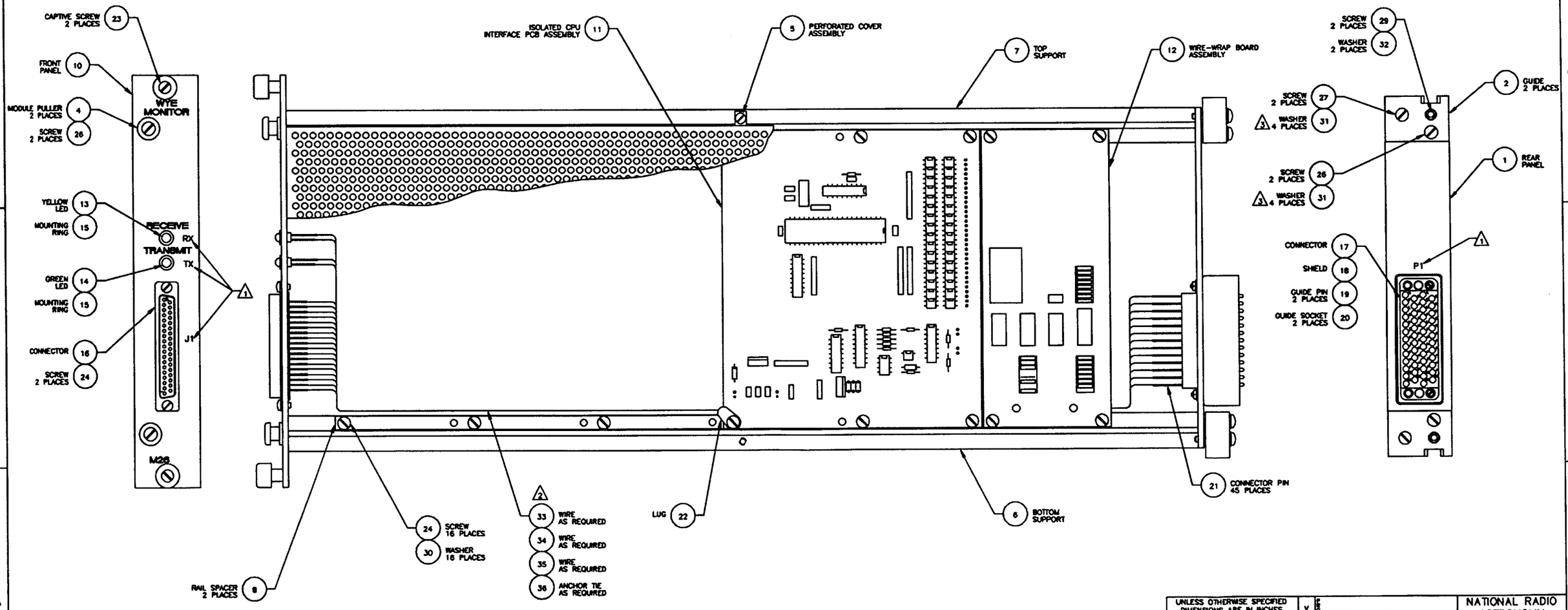
The Azimuth and Elevation limit discretes tested by the ACU Fault board are redundant because they are also included in the ACU's monitor word 211_8.

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	6-94			MINOR CORRECTIONS

NOTES:

1. MARKING SHALL BE .125 HIGH, LEGIBLE, AND PERMANENT. LOCATE ON INSIDE OF MODULE APPROXIMATELY AS SHOWN
2. A WIRING SERVICE LOOP OF SUFFICIENT LENGTH TO ALLOW FRONT AND REAR PANELS TO BE FOLDED FLAT MUST BE PROVIDED
3. PLACE ONE WASHER UNDER SCREW HEAD AND ONE WASHER BETWEEN REAR PANEL (ITEM 1) AND GUIDE (ITEM 2)





ACAD : 13900P06

A13900Z01	BOM
A13900W02	WIRING DIAG
D13900S04	SCHEMATIC
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL :

FINISH :

PROJECT: VLA

WYE MONITOR

TITLE: WYE MONITOR M26 ANTENNA INTERFACE MODULE ASSEMBLY

NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 6-93
DESIGNED BY	DATE 6-93
APPROVED BY	DATE 6-93

SHEET NUMBER 1 of 1 | DRAWING NUMBER D13900P06 | REV. A | SCALE 1/1

REV.	DATE	DRAWN BY	APROV'D BY	DESCRIPTION
A	8-93			ASB ACV MANUAL MONITOR
B	9-93			CHANGES ACV TO ACU
C	7-93			CHANGES OPTO87 TO OPTO86
D	11-93			MINOR CORRECTIONS
E	9-94			CHANGES PULLUP POWER TO VCC

NOTES:
1. OPTO87-OPTO34 ON PRINTED CIRCUIT BOARD ARE REPLACED BY A PS2501-4 QUAD OPTO ISOLATOR
2. OPTO35-OPTO38 ON SCRUB BRUSH ARE REPLACED BY A PS2501-4 QUAD OPTO ISOLATOR AT AG33
3. ADDRESS MODULE, ADDRESS SWITCH S1 IS NOT INSTALLED UNLESS FOR TESTING. ID IS BINARY WITH BITS GROUNDED TO DRIVE TO 0 OR FLOATING FOR 1
4. P1688 (Z1) REPLACES RV1, RV2, RV3

⚠ MODULE ADDRESS

ISOLATED COMMUNICATION INTERFACE

WATCHDOG RESE

ISOLATED I/O LINES

ACU FAULT MONITOR

NONCRITICAL POWER MONITOR

RELAY SUPPLY AND MONITOR

STOW MONITOR

PHASE LOSS MONITOR

FIRE ALARM

LOCAL ESTOP MONITOR

POWER CONDITIONING

ISOLATED DC-DC CONVERTER

ACU MANUAL MONITOR

ORCAD : 13900S04

C13900P07	WIRE-WRAP BOARD
D13900P06	ASSEMBLY
NEXT ASSEMBLY	SVG TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMAL (.XXX) ±
2 PLACE DECIMALS (.XX) ±
1 PLACE DECIMALS (.X) ±

MATERIAL:

FINISH:

VLA PROJECT: WYE MONITOR

TITLE: WYE MONITOR
M26 ANTENNA
INTERFACE MODULE
SCHEMATIC DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO,NEW MEXICO 87801

DRAWN BY		DATE 12-92
DESIGNED BY		DATE 12-92
APPROVED BY		DATE 12-92

SHEET NUMBER 1 OF 1 | DRAWING NUMBER C13900B04 | REV: E | SCALE -

BILL OF MATERIAL
NATIONAL RADIO ASTRONOMY OBSERVATORY

X ELECTRICAL X MECHANICAL BOM # A13900Z01 REV A DATE 6-02-94 PAGE 2 OF 4

MODULE M26 NAME ANTENNA INTERFACE DWG# D13900P06 SUB ASSY _____ DWG# _____

SCHEM. DWG# D13900S04 LOCATION WYE MON QUA/SYS. _____ PREPRD BY K. TATE APPRVD BY A. SITTLER

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
1		NRAO	C13050M02	PANEL, REAR	1
2		NRAO	B13050M04	GUIDE	2
3		NRAO	C13050M06	PLATE, SIDE	1
4		NRAO	C13050M70	KNOB, MODULE PULLER	2
5		NRAO	C13050P21	ASSY, PERFORATED COVER	1
6		NRAO	C13720M15-1	SUPPORT, BOTTOM	1
7		NRAO	C13720M15-2	SUPPORT, TOP	1
8		NRAO	C13720M17	SPACER, INSULATED RAIL	2
9		NRAO	C13720M49	PANEL, INSULATED SIDE	1
10		NRAO	C13900M04	PANEL, FRONT	1
11		NRAO	D13900P02	PCB, ISOLATED CPU INTERFACE	1
12		NRAO	C13900P07	CIRCUIT BOARD, WIRE-WRAP	1
13	RX			LED, YELLOW	1
14	TX			LED, GREEN	1
15		HEWLETT PACKARD	HLMP-0103	RING, LED MOUNTING	2
16	J1	AMPHENOL	17D-C37S-F179	CONNECTOR, 37-PIN D-SUB	1
17	P1	AMP	201358-3	CONNECTOR, 50-PIN	1
18		AMP	202394-2	SHIELD, CONNECTOR	1
19		AMP	200833-4	PIN, GUIDE	2
20		AMP	203964-6	SOCKET, GUIDE	2

REVISIONS

REV	DATE	DRAWN BY	APPRVD BY	DESCRIPTION
A	6-94	K. TATE	A. SITTLER	MINOR CORRECTIONS

			USED ON
			NEXT ASSY
DRAWN BY K. TATE	DESIGNED BY A. SITTLER	APPROVED BY A. SITTLER	
DATE 6-93	DATE 6-93	DATE 6-93	

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLA

PROJECT WYE MONITOR
TITLE M26 ANTENNA INTERFACE MODULE BOM
DWG NO. A13900Z01
SHEET 1 OF 4

BILL OF MATERIAL
NATIONAL RADIO ASTRONOMY OBSERVATORY

X ELECTRICAL X MECHANICAL BOM # A13900Z01 REV A DATE 6-02-94 PAGE 4 OF 4

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
39					
40		NRAO	C13900AB04	SILKSCREEN, FRONT PANEL	---
41		NRAO	A13900P04	ASSEMBLY, DIP HEADER	---
42		NRAO	D13900P06	ASSEMBLY, M26 MODULE	---
43		NRAO	D13900S04	SCHEMATIC, M26 MODULE	---
44		NRAO	A13900W02	WIRING DIAGRAM, CONNECTOR	---
45		NRAO	A13900Z01	BOM	---
46					
47					
48					
49					
50					
51					
52					
53					
54					
55					
56					
57					
58					
59					
60					

BILL OF MATERIAL
NATIONAL RADIO ASTRONOMY OBSERVATORY

X ELECTRICAL X MECHANICAL BOM # A13900Z01 REV A DATE 6-02-94 PAGE 3 OF 4

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
21		AMP	610488-1	PIN, CONNECTOR/WW POST	45
22		H.H. SMITH	1411-4	LUG, SOLDER #4	1
23		SOUTHCO	47-10-204-10	SCREW, CAPTIVE	2
24				SCREW, PAN HD, SS, 4-40UNC-2A x .25	18
25				SCREW, FLT HD, SS, 6-32UNC-2A x .25	6
26				SCREW, FLT HD, SS, 6-32UNC-2A x .75	2
27				SCREW, PN HD, SS, 6-32UNC-2A x .75	2
28				SCREW, PN HD, SS, 6-32UNC-2A x 1.00	2
29				SCREW, SOCK HD, SS, 6-32UNC-2A x 1.00	2
30				WASHER, #4, EXT. TOOTH	16
31				WASHER, #6, EXT. TOOTH	8
32				WASHER, #6, SPLIT RING LOCK	2
33		ALPHA	7053	WIRE, RED, #26 GA.	AR
34		ALPHA	7053	WIRE, BLK, #26 GA.	AR
35		ALPHA	7053	WIRE, YEL, #26 GA.	AR
36		PANDUIT	TA1S8	TIE, ANCHOR	AR
37					
38					

DESCRIPTION	VALUE	MFG.	PART NO.
DIP HEADER			
RESISTOR	10K, 1/4W	ALLEN-BRADLEY	RC07GF103JS
RESISTOR	4.7K, 1/4W	ALLEN-BRADLEY	RC07GF472JS
RESISTOR	4.7K, 1/4W	ALLEN-BRADLEY	RC07GF472JS
RESISTOR	0 OHM	NRAO	
RESISTOR	10K, 1/4W	ALLEN-BRADLEY	RC07GF103JS
RESISTOR	10K, 1/4W	ALLEN-BRADLEY	RC07GF103JS

MODULE: M26 WYE MONITOR

BOARD LOCATION: AC43

DRAWING NO. A13900P04 | SHEET 2 OF 4 | REV A

REVISIONS

REV	DATE	DRAWN BY	APPROVED BY	DESCRIPTION
A	2-93			ADDED 4.7K RESISTOR TO SHEET 3

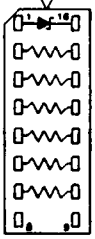
	DATE
DRAWN BY	1-93
DESIGNED BY	1-93
APPROVED BY	1-93

D13900S04 | SCHEMATIC | USED ON | NEXT ASSY

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLA

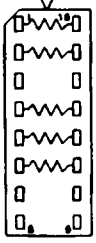
PROJECT WYE MONITOR
TITLE M26 DIP HEADER ASSEMBLY
DWG NO A13900P04
SHEET 1 OF 4

	DESCRIPTION	VALUE	MFG.	PART NO.
	DIP HEADER			
	ZENER DIODE	20 VOLTS	MOTOROLA	IN5250A
	RESISTOR	1.0K, 1/4W	ALLEN-BRADLEY	RC07GF102JS
	RESISTOR	4.7K, 1/4W	ALLEN-BRADLEY	RC07GF472JS
	RESISTOR	2.0K, 1/4W	ALLEN-BRADLEY	RC07GF202JS
	RESISTOR	10K, 1/4W	ALLEN-BRADLEY	RC07GF103JS
	RESISTOR	4.7K, 1/4W	ALLEN-BRADLEY	RC07GF472JS
	RESISTOR	10K, 1/4W	ALLEN-BRADLEY	RC07GF103JS

MODULE: M26 WYE MONITOR

BOARD LOCATION: AG43

DRAWING NO A13900P04 SHEET 4 OF 4 REV A

	DESCPIPTION	VALUE	MFG.	PART NO.
	DIP HEADER			
	RESISTOR	4.7K, 1/4W	ALLEN-BRADLEY	RC07GF472JS
	RESISTOR	2.0K, 1/4W	ALLEN-BRADLEY	RC07GF202JS
	RESISTOR	4.7K, 1/4W	ALLEN-BRADLEY	RC07GF472JS
	RESISTOR	4.7K, 1/4W	ALLEN-BRADLEY	RC07GF472JS
	RESISTOR	4.7K, 1/4W	ALLEN-BRADLEY	RC07GF472JS

MODULE: M26 WYE MONITOR

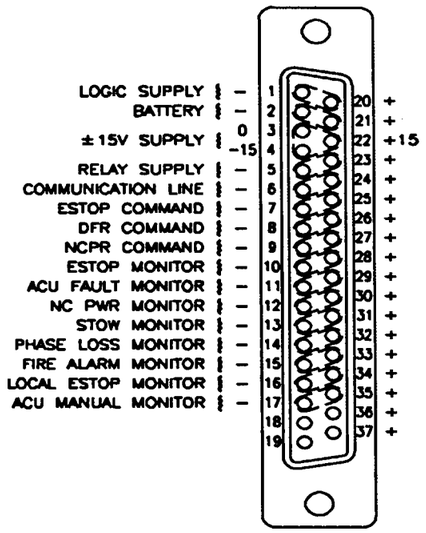
BOARD LOCATION: AG24

DRAWING NO A13900P04 SHEET 3 OF 4 REV A

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	7-93			ADDED ACU MANUAL MONITOR
B	6-94			ADDED CONNECTOR P1

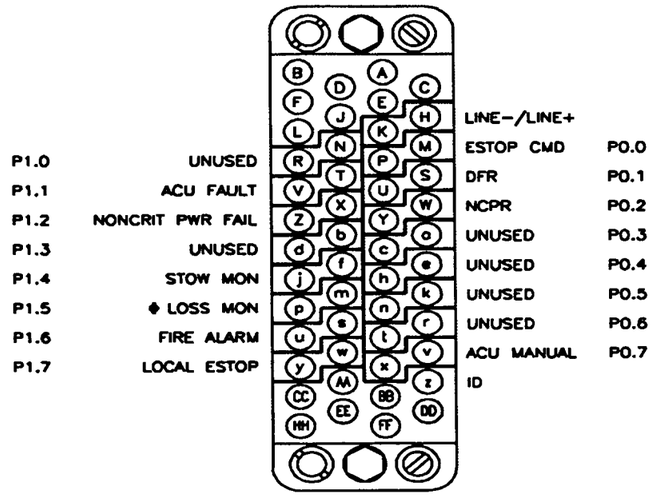
NOTE:

1. — — = GROUP SIGNALS



FRONT PANEL CONNECTOR – J1

VIEWED FROM MODULE FRONT



PIN	FUNCTION	PIN	FUNCTION
A		d	
B	BATTERY RTN	e	
C		f	STOW MON+
D	+12 VOLTS BATTERY	h	
E		j	STOW MON–
F	+28 VOLTS	k	
H	LINE+	m	◆ LOSS MON+
J		n	
K	LINE–	p	◆ LOSS MON–
L	28V RTN	r	
M	ESTOP CMD+	s	FIRE ALARM+
N		t	
P	ESTOP CMD–	u	FIRE ALARM–
R		v	ACU MANUAL+
S	DFR+	w	LOCAL ESTOP+
T	ACU FAULT+	x	ACU MANUAL–
U	DFR–	y	LOCAL ESTOP–
V	ACU FAULT–	z	ID4
W	NCPR+	AA	ID5
X	NONCRIT PWR FAIL+	BB	ID2
Y	NCPR–	CC	ID3
Z	NONCRIT PWR FAIL–	DD	ID0
a		EE	ID1
b		FF	ID GND
c		HH	ANALOG GND

REAR PANEL CONNECTOR – P1

VIEWED FROM MODULE REAR

ACAD : 13900W02

D13900S04	SCHEMATIC
A13900Z01	BOM
D13900P06	ASSEMBLY
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES : ANGLES ±

3 PLACE DECIMALS (.XXX) ±

2 PLACE DECIMALS (.XX) ±

1 PLACE DECIMALS (.X) ±

MATERIAL :

FINISH :

VLA PROJECT

WYE MONITOR

TITLE

M26 ANTENNA INTERFACE
MODULE CONNECTOR
TEST POINTS
WIRING DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

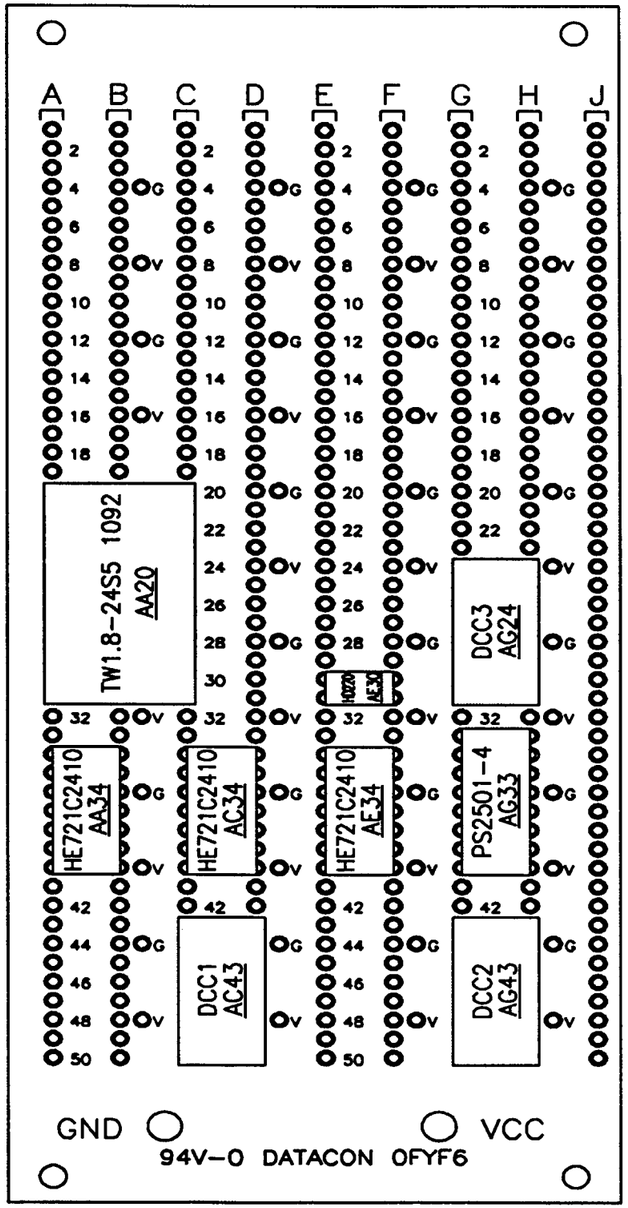
DRAWN BY	DATE 3-94
DESIGNED BY	DATE 10-92
APPROVED BY	DATE 10-92

SHEET NUMBER 1 OF 1 | DRAWING NUMBER C13900W02 | REV. B | SCALE 2/1

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

NOTES:

1. INSTALLED ON AUGAT 606-CG1 DIP HEADER.
   REF: DIP HEADER ASSEMBLY, DWG. #A13900P04



AC43 (1)

1	10K	16
	4.7K	
	4.7K	
	10K	
8	10K	9

AG24 (1)

1	4.7K	16
	2K	
	4.7K	
	4.7K	
	4.7K	
8		9

AG43 (1)

1	20V	16
	10K	
	4.7K	
	2K	
	10K	
	4.7K	
	10K	
8		9

D13900S04	SCHEMATIC
D13900P06	MODULE ASSY
A13900P04	DIP HEADER
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.###) ±
2 PLACE DECIMALS (.##) ±
1 PLACE DECIMALS (.#) ±

MATERIAL :

FINISH :

VLA

WYE MONITOR

TITLE: M26 ANTENNA INTERFACE MODULE WIRE-WRAP BOARD COMPONENT LAYOUT

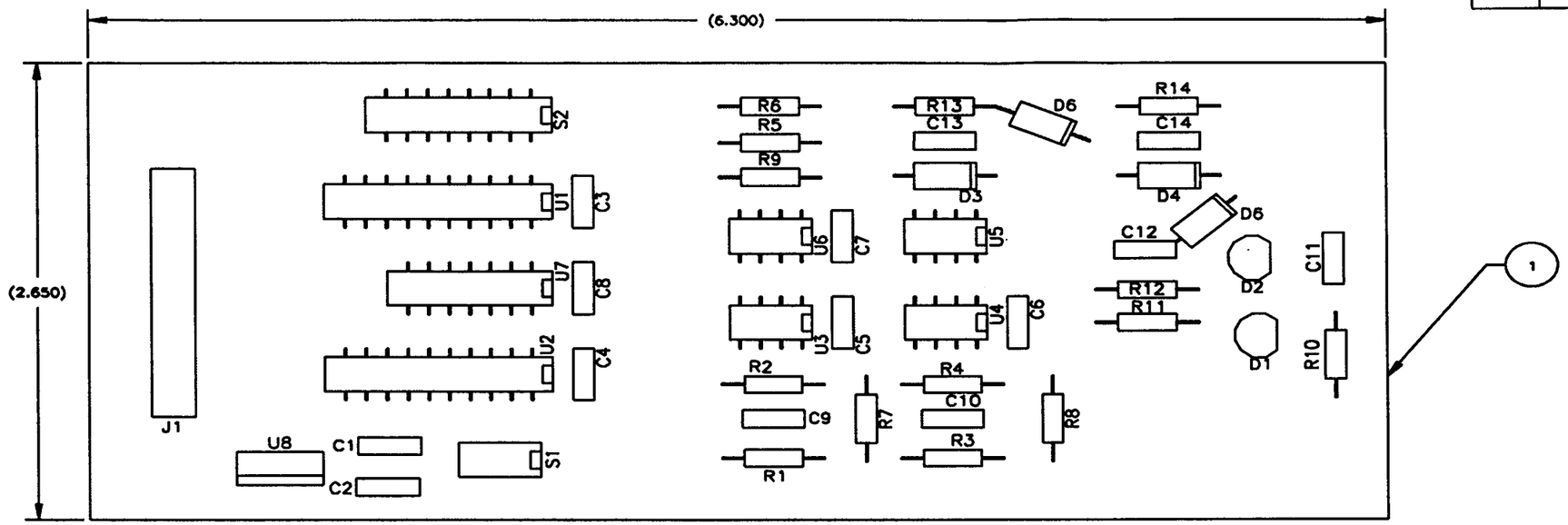
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 6-93
DESIGNED BY	DATE 6-93
APPROVED BY	DATE 6-93

SHEET NUMBER 1 OF 1 | DRAWING NUMBER C13900P07 | REV. — | SCALE 2/1

ACAD : 13900P07

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	5-93			MINOR CORRECTIONS
B	7-93			CHGD J1 PART NUMBER
C	8-93			ADDED D5, D6; NOTE 1



COMPONENT SIDE

NOTES:

1. ADD D5 AND D6 TO PRINTED CIRUIT BOARD AT TIME OF ASSEMBLY FOR LIGHTNING PROTECTION. DRILL MOUNTING HOLES NEAR TRACES. SOLDER SO THAT THERE IS A GOOD SOLER FLOW BETWEEN THE TRACE AND COMPONENT LEAD

ACAD : 13900P05

ITEM NO.	REF. DES.	MANUFACTURER	PART NUMBER	DESCRIPTION	QTY
23	U8		LM7805KC	VOLTAGE REGULATOR	1
22	U7		74HCT04	IC, 14-PIN	1
21	U5		OP-15	IC, 8-PIN	1
20	U3,U4,U6		LTC1042	IC, 8-PIN	3
19	U1, U2		74HCT688	IC, 20-PIN	2
18	S2		SW DIP-8	SWITCH	1
17	S1		SW DIP-4	SWITCH	1
16	R13, R14			RESISTOR,1K,1/4W,5%	2
15	R12			RESISTOR,750,1/4W,1%	1
14	R11			RESISTOR,9.31K,1/4W,1%	1
13	R10			RESISTOR,25K,1/4W,5%	1
12	R7-R9			RESISTOR,100K,1/4W,5%	3
11	R6			RESISTOR,15K,1/4W,1%	1
10	R5			RESISTOR,2490,1/4W,1%	1
9	R3			RESISITOR,49.9K,1/4W,1%	1
8	R1,R2,R4			RESISTOR,10K,1/4W,1%	3
7	J1	3M	4-103322-0	HEADER, BREAK AWAY	1
1 6	D5, D6		D6KE51A	SUPPRESSOR, TRANSIENT VOLTAGE	2
5	D3, D4		1N5245	DIODE	2
4	D1, D2		LT1004	DIODE	2
3	C3-C12			CAPACITOR, 0.1uf	10
2	C1, C2, C13, C14			CAPACITOR, 2.2uf	4
1		NRAO	C13900M08	CIRCUIT BOARD	1

C13900S09	SCHEMATIC
C13900M08	DRILL DWG
C13900AB14	SOLDER MASK
C13900AB13	SILKSCREEN
D13900AB12	ARTWORK
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES : ANGLES ±
3 PLACE DECIMALS (.XXX) ±
2 PLACE DECIMALS (.XX) ±
1 PLACE DECIMALS (.X) ±

MATERIAL :

FINISH :

VLA RESTRICTED — WYE MONITOR

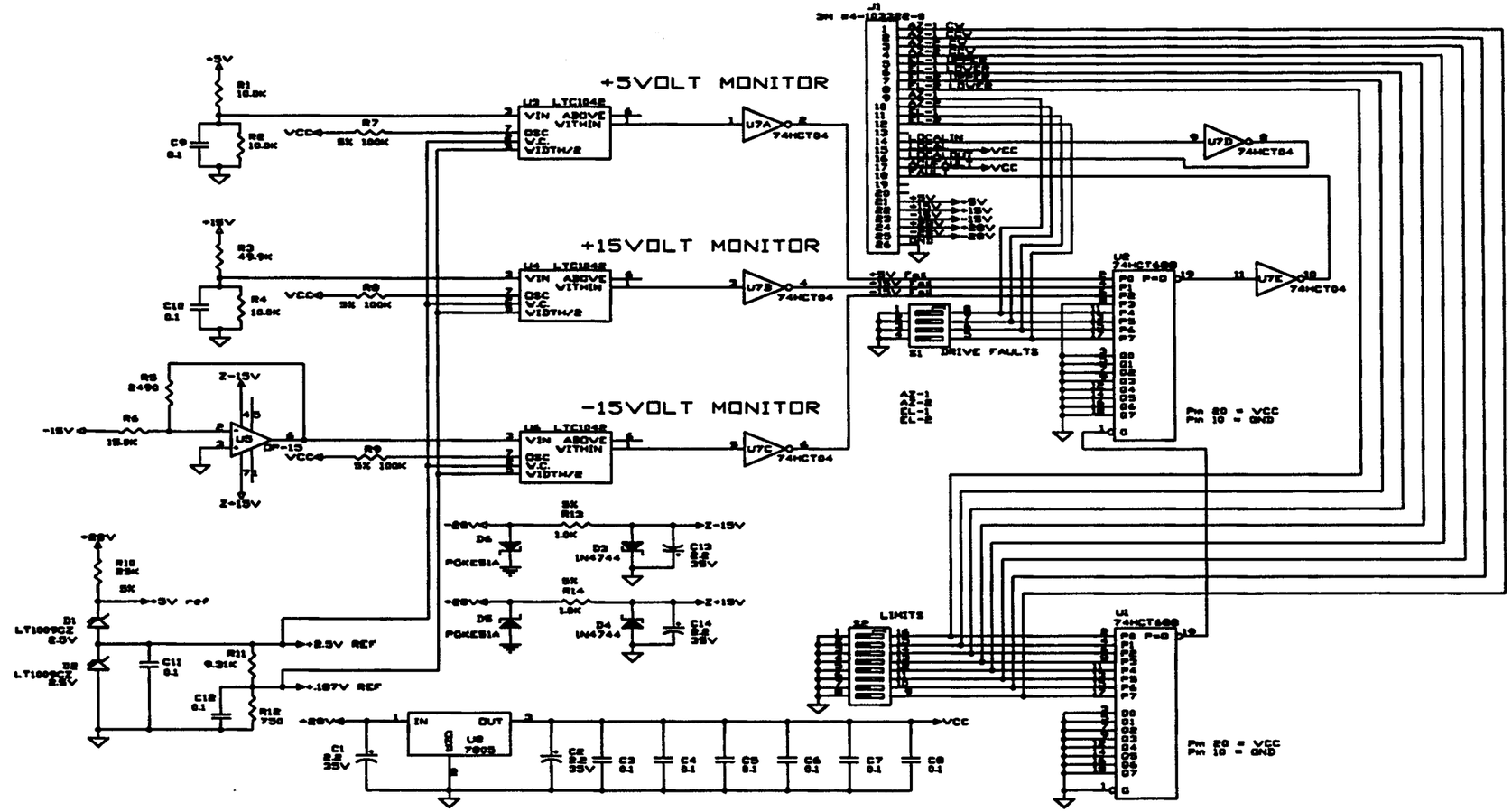
TITLE: ACUFAULT PRINTED CIRCUIT BOARD ASSEMBLY

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 4-93
DESIGNED BY	DATE 4-93
APPROVED BY	DATE 4-93

SHEET NUMBER 1 OF 1 | DRAWING NUMBER C13900P05 | REV. C | SCALE 2/1

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	7-93			CHGD P/N ON 3L04; ADD DIODES
B	10-93			CHGD P/N ON 3L06; ADD 33V



C13900P03	ASSEMBLY
C13900H08	DRILL DWG
C13900AB14	SOLDER MASK
C13900AB13	SILKSCREEN
D13900AB12	ARTWORK
NEXT ASSEMBLY	DVG TYPE

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX) ±
2 PLACE DECIMALS (.XX) ±
1 PLACE DECIMALS (.X) ±

MATERIAL:

FINISH:

PROJECT: VLA — WYE MONITOR

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO,NEW MEXICO 87801

TITLE: ACUFAULT PRINTED CIRCUIT BD. SCHEMATIC DIAGRAM

DRAWN BY	DATE 4-93
DESIGNED BY	DATE 4-93
APPROVED BY	DATE 4-93

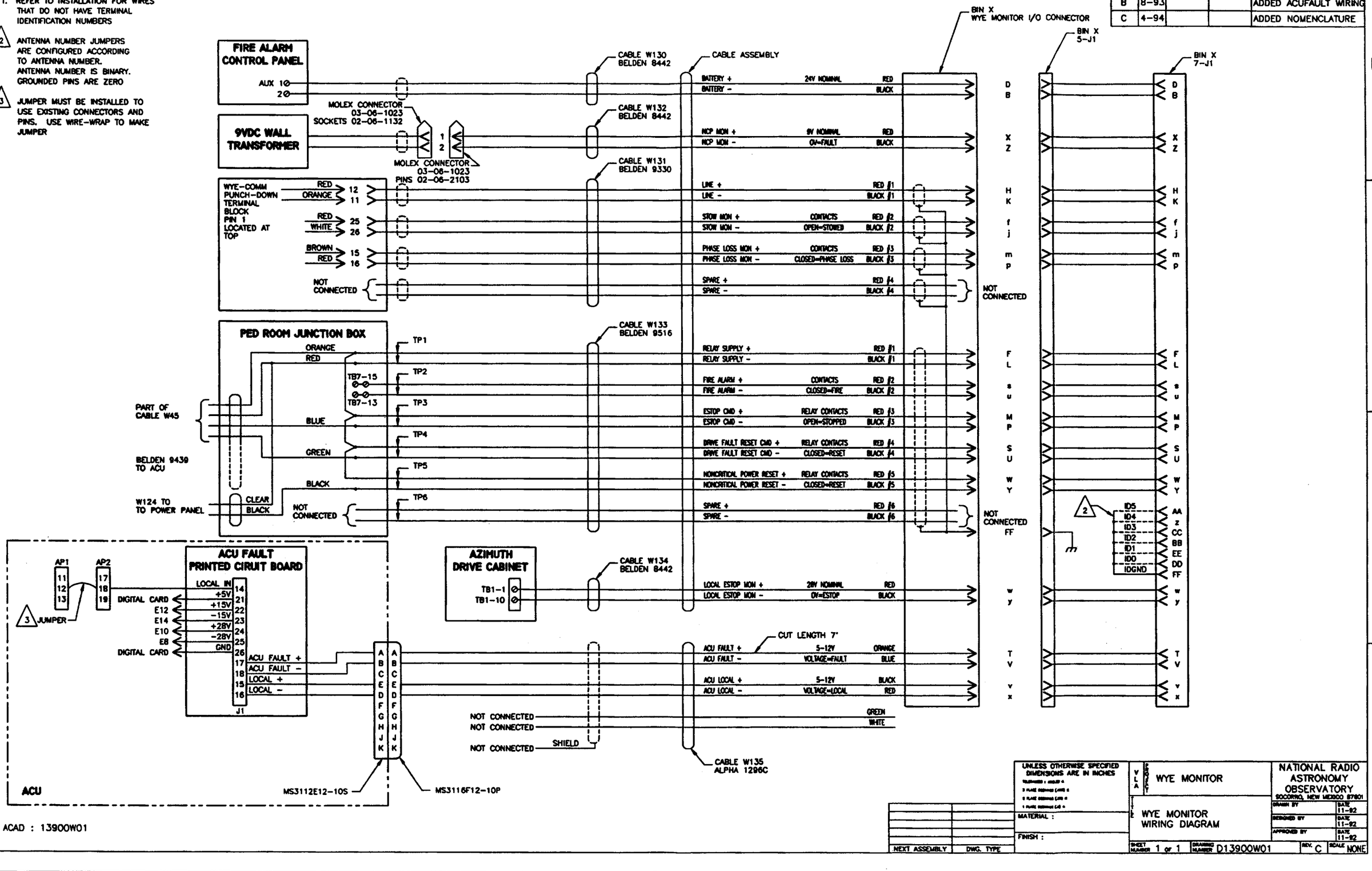
SHEET NUMBER 1 OF 1 | DRAWING NUMBER C13900S09 | REV. B | SCALE -

ORCAD : 13900S09

REV	DATE	DRAWN BY	APPR'D BY	DESCRIPTION
A	7-93			ADDED ACUFAULT LOCAL
B	8-93			ADDED ACUFAULT WIRING
C	4-94			ADDED NOMENCLATURE

NOTES:

1. REFER TO INSTALLATION FOR WIRES THAT DO NOT HAVE TERMINAL IDENTIFICATION NUMBERS
2. ANTENNA NUMBER JUMPERS ARE CONFIGURED ACCORDING TO ANTENNA NUMBER. ANTENNA NUMBER IS BINARY. GROUNDED PINS ARE ZERO
3. JUMPER MUST BE INSTALLED TO USE EXISTING CONNECTORS AND PINS. USE WIRE-WRAP TO MAKE JUMPER



ACAD : 13900W01

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL :

FINISH :

NEXT ASSEMBLY | DWG. TYPE

VLA

WYE MONITOR

WYE MONITOR WIRING DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801

DRAWN BY | DATE 11-92

DESIGNED BY | DATE 11-92

APPROVED BY | DATE 11-92

SHEET NUMBER 1 OF 1 | DRAWING NUMBER D13900W01 | REV. C | SCALE NONE

2.10 M27 Auxiliary Monitor and its Interfaces with the Generators and UPS's

This section describes the M27 Auxiliary Monitor Module and its interfaces with the generator system's Generators 1 and 2, Master Cubicle, and the Correlator and Computer UPS units. Like the other WYE Monitor control interface modules, M27 uses the Isolated CPU Interface Board to transform serial bus message interactions into 16 discrete paralell interactions with device interface circuitry. D13900S08 is the M27 schematic diagram. The device interface circuitry is installed on a wire-wrapped logic connector board in M27. Drawing D13900P20 is the module assembly drawing and drawing C13900P21 shows the interface circuit's component layout on the logic connector board. Reduced-scale copies of the M27 functional drawings follow this text.

This section does not describe the operating characteristics of the generator, computer or correlator UPS systems. However, the tables following the correlator and generator interface descriptions list the unit's control and monitor signal function names and the conditions associated with each signal state. Figures 2, 4 and 5 show the Correlator UPS, Generator and Facility sub-screens.

The M27's are connected to the WYE Monitor Auxiliary Bus that services the Control Building and service building complex.

Sections 2.2 and 2.4 described the message formats, protocol, and line driving and receiving. Section 2.8 described the Isolated CPU Interface Board.

The major subjects of this section are the character of the interface signals, the interface circuits that adapt these signals to the Isolated CPU Interface Board and the M27 power circuitry.

M27 is designed to output two command discretes and input fourteen monitor discretes. There are no unimplemented command/monitor discretes, as was the case in the M26 module.

M27 is a more general module than the M26 and M29 because its device interface circuitry on the logic connector board services the five devices mentioned above. This application commonality is the result of the fact that the control interfaces in the generators and Master Cubicle have identical circuitry; the two UPS units are identical, and the interface signal types and levels for the two types of applications are very similar. As a result of this similarity, it was possible to design the M27 device interface circuitry so that it would be compatible with both the generator and UPS systems.

Three M27's and the associated M28 Power Supply/Battery Module are installed in a bin in the Generator Control room. These units control and monitor the generators and Master Cubicle switching gear. The three M27 outputs are each connected to a generator system interface module, C9390028. A reduced-scale copy of this drawing follows this text. The generator systems interfaces are described below.

Two M27's and the associated M28 Power/Battery Module are installed in a bin in the Control Building's UPS room and control and monitor the Correlator and Computer UPS units; these interfaces are described below.

The M27 and related functional drawings are listed on the next page; for convenient reference, reduced-scale copies follow this section's text.

D13900P20	WYE Monitor M27 Auxiliary Monitor Module Assembly
A13900Z04	M27 Auxiliary Module Module BOM
D13900S08	WYE Monitor M27 Auxiliary Monitor Schematic Diagram
D13900P22	M27 Auxiliary Monitor Isolated CPU Interface Board Assembly
C13900P21	M27 Auxiliary Monitor Module Wire-Wrap Board Component Layout
A13900P23	M27 Auxiliary Monitor Module Dip Header Assembly
C13900W05	M27 Module 37-Pin Connector Test Points Wiring Diagram
A13900W06	M27 Auxiliary Monitor Module Wire List
D13900WW09	M27-Generator System Interface
B13900S12	WYE Monitor Master Cubicle Relay and Header Schematic Diagram
C9390028	Main Generator WYE COM Monitor Circuits
D13900W10	M27-Correlator and Computer UPS Interface

Front Panel Test Point Connector

For convenience in locally checking the M27's interface signals, WYE Monitor bus signal and M27 power, M27 has a front panel test point connector J1 that is a 37 contact, "D" series socket connector. Note from the M27 module schematic drawing that all the monitored functions are connected to J1 but command functions are not included. Note also that the J1 signals are connected to the Isolated CPU Interface Board Port 0 and Port 1 connectors. The levels are the TTL-compatible port inputs and are low-true when the input to the associated optoisolator is an active-high 24 volts.

M27 Command Interface Circuitry

The Isolated CPU's Interface Board's parallel I/O optical isolator configuration is shown on D13900P22.

Command optoisolators (NEC PS2502-1) are installed in the Isolated CPU Interface Board ports IO0 and IO1. Monitor optoisolators are not installed in these ports.

The two command interface circuits are SPDT relays and are functionally similar to those used in the command interface circuits of M26. The two sets of NO relay contacts are connected to P1, the M27 module I/O connector; the NC contacts are not used. Setting a 0 in command ports IO01 or IO02 closes the NO relay contact. Since the command outputs are NO relay contacts, they are electrically isolated from the M27 circuitry.

Note that the two relay command circuits are identical and use the same Hamlin SPDT relay and inductive-kick clipping diode as in M26. The relays are driven by the output transistor of the command optoisolators (NEC PS2502-1), which sinks current from the M28 Power Supply +28 output through the relay coil to the M28 28 volt return.

The Hamlin HE721C2410 is a dry reed relay with a contact rating of 3 Watts, 0.25 Amps, and 175 volts. The coil resistance is 2000 Ohms and is designed for 24 volt operation.

M27 Monitor Interface Circuitry

Monitor optoisolators (NEC PS2501-1) are not installed in the Isolated CPU Interface Board ports IO2 through IO15. In place of these isolators, Ports IO2 through IO15 use NEC PS2501-4 monitor input optoisolators installed on the logic connector board. These optoisolators are electrically identical to NEC

PS2501-1 but four optoisolators are packaged in one chip. Correspondingly, Command optoisolators are not installed in Ports IO2 through IO15.

The monitor interface circuits are all optically-isolated 24 volt inputs and all use a 10 kΩ series resistor to limit the isolator LED current to about 2.2 mA. Other than the inversion inherent in the monitor optoisolators, there are no logical inversions in the monitor circuitry. Therefore, a no-fault readout will not be all zero's as is the case in M26. If the input to the monitor circuits is 24 volts and is the correct polarity, the optoisolator output will be low, which is a 1.

The voltage sources are +24 volts in all M27 applications. The M28 Power Supply +24 volt output and its return are connected to the device interface circuitry where it is typically connected to monitor relay contacts. The contact outputs return this voltage as a function of the device's monitor states.

M27 Address Inputs

The M27 address line (Unit ID) inputs are encoded to enable the module's Isolated CPU Interface board to determine if the module is the target of a Command or Monitor Request messages. It also uses the encoded value in formatting Command or Monitor Acknowledge messages transmitted to the control PC. The M27 address line inputs are **active-high** and the code is formed by connecting the appropriate address line inputs to logic common (J1-FF) on the J1, the bin back-plane connector. The bin contacts connected to ground are the complement of the address code. J1-DD is the LSB (2^0) and J1-z (2^4) is the MSB. J-1AA (2^5) is always connected to logic common in the address line ground string. The M27 address code assignments are described below in the two M27 interface application descriptions.

M27 Power

M27's input power is +13.6 volts from the M28 Power Supply/Battery Module. The Isolated CPU Interface Board performs the power regulation and isolation for the M27 Module. This power circuitry is described in Section 2.8; see this section for details. VCC for the monitor input optoisolator's collector load resistors is provided by the Isolated CPU Interface Board's LM7805KC +5 volt regulator's output.

Generator and Master Cubicle Interfaces

The Generator System's M27's are installed in bin locations 4, 5, and 6 in the Generator Control Room. M28 is installed in positions 1, 2 and 3. The M27 in bin position 4 monitors Generator 1 (EAST), that in bin position 5 monitors Generator 2 (WEST), and the unit in position 6 controls and monitors the Master Cubicle. M28, the Power Supply/Battery Module provides 12-volt M27 power and 26-volt power to the monitor interfaces in the generator system's monitor interfaces.

The Generator 1 M27 (position 4) address code is 2; the Generator 2 M27 (position 5) address code is 3 and the Master Cubicle M27 (position 6) address code is 4.

Drawing D13900W09 shows the bin wiring and control-monitor wiring between the three M27's, Generator 1 and 2 cubicles and the Master Cubicle. Three 24-wire cables from TB 1 connect the M27 to the associated Generator and Master Cubicle monitor circuits. Both generators have identical monitor functions and wiring; the generator's M27s do not have any command functions. The generator start and stop functions are controlled by the Master Cubicle circuitry but the Master Cubicle M27 only outputs the start command. The Generator and Master Cubicle interface signal characteristics and bit assignments are

tabulated following this text.

Drawing C9390028, Main Generator WYE COM Monitor Circuits, shows the the physical layout of the three sets of identical monitor interface modules that read out the Generator 1, Generator 2, and Master Cubicle monitor states. Drawing B13900S12 shows the monitor interface circuit in larger scale. Refer to these drawings during the following description.

The monitor interface module's outputs to the M27 are on TB 2 and the inputs from the generator system are on TB 1. Each interface module has ten interface circuits. Each circuit consists of a relay, a state indicator LED, current limiting resistors, and relay contact-select jumpers. The resistors, LED, and jumpers are installed on a dip header. The resistors limit LED current and relay coil current; the jumper selects either the NO or NC relay contacts. The M28 +24 volt power supply output is connected to TB 2-23 and the 24 volt return is connected to TB 2-24. The relay center contacts are connected to +24 volts and the jumpers are configured for NO contact outputs. The relay coil is driven by the generator system's monitor circuits and when they actuate a relay, the NO contacts read out the function's state as a +24 volt signal. These +24 volt signals drive the optoisolator's anodes via the 10 kΩ limiting resistors. The M28's 24 volt return is connected to all ten low-side (optoisolator's LED cathode) M27 monitor inputs. The relay and LED circuit returns are connected to the generator system's circuit grounds; therefore, the generator systems monitor outputs are electrically isolated from the M27's.

Note from the tables below that the WYE Monitor System outputs only one command to the generator system, Start Generators, from the Master Cubicle M27. The command interface circuits (IO0 and IO1) in the generator M27's are not used. The Start Generators command pair is wired through the 24-wire interface cable to relays in the Allen-Bradley Process Control equipment in the Master Cubicle cabinet. When activated by setting a 0 in command port IO01, the relay NO contact closure activates the generator start function. See drawing D13900W09 for details.

Figure 4 shows the Generator, Master Cubicle and Generator START/STOP sub-screens.

Master Cubicle Interface Signal Characteristics

Int Bd Signal	Function	Signal Type	M27 Module I/O Pins & Levels	Int BD Port State	Signal Function
IO00 (C)*	Start Generaors Command	SPDT Relay Contacts	P1-P & P1-M		
			open	Low, 0	Cmd Active
			closed	High, 1	Cmd Inactive
IO01 (C)	Not Used	SPDT Relay Contacts	P1-S & P1-U		
			open	Low, 0	
			closed	High, 1	
IO02 (M)	Generator Tie Breaker Open	DC voltage	P1-W & P1-Y		
			+24 volts	Low, 0	Breaker Closed
			0 volts	High, 1	Breaker Open
IO03 (M)	SEC Utility Breaker Open	DC voltage	P1-a & P1-c		
			+24 volts	Low, 0	Breaker Closed
			0 volts	High, 1	Breaker Open
IO04 (M)	Not Used	DC voltage	P1-e & P1-h		
			+24 volts	Low, 0	
			0 volts	High, 1	

I005 (M)	Not Used	DC voltage	P1-k & P1-n +24 volts 0 volts	 Low, 0 High, 1	
I006 (M)	Not Used	DC voltage	P1-r & P1-t +24 volts 0 volts	 Low, 0 High,1	
I007 (M)	Not Used	DC voltage	P1-v & P1-x +24 volts 0 volts	 Low, 0 High, 1	
I008 (M)	AC Control Voltage	DC voltage	P1-N & P1-R +24 volts 0 volts	 Low, 0 High, 1	 No AC Voltage Voltage OK
I009 (M)	#1 Day Tank Low Fuel	DC voltage	P1-T & P1-V +24 volts 0 volts	 Low, 0 High, 1	 Fuel Low Fuel OK
I010 (M)	#2 Day Tank Low Fuel	DC voltage	P1-X & P1-Z +24 volts 0 volts	 Low, 0 High, 1	 Fuel Low Fuel OK
I011 (M)	Voltage/Freq Failure	DC voltage	P1-b & P1-d +24 volts 0 volts	 Low, 0 High, 1	 Volt/Freq Fail Volt/Freq OK
I012 (M)	Load Shed Activated	DC voltage	P1-f & P1-j +24 volts 0 volts	 Low, 0 High, 1	 Load is Shed Load OK
I013 (M)	Alarm Horn	DC Voltage	P1-m & P1-v +24 volts 0 volts	 Low, 0 High, 1	 Alarm On Alarm Off
I014 (M)	Not Used	DC voltage	P1-s & P1-u +24 volts 0 volts	 Low, 0 High, 1	
I015 (M)	Not Used	DC voltage	P1-w & P1-y +24 volts 0 volts	 Low, 0 High, 1	

* C denotes a command function and M denotes a monitor function.

Generators 1 and 2 Interfaces with M27

Int Bd Signal	Function	Signal Type	M27 Module I/O Pins & Levels	Int BD Port State	Signal Function
I000 (C)*	Not Used	SPDT Relay Contacts	P1-P & P1-M open closed	 Low, 0 High, 1	 Start Cmd Act'v Cmd Inactive
I001 (C)	Not Used	SPDT Relay Contacts	P1-S & P1-U open closed	 Low, 0 High, 1	 Stop Cmd Active Cmd Inactive
I002 (M)	Generator Ckt Breaker	DC voltage	P1-W & P11-Y +24 volts 0 volts	 Low, 0 High, 1	 Breaker Open Breaker Closed
I003 (M)	Remote Ckt Breaker	DC voltage	P1-a & P1-c +24 volts 0 volts	 Low, 0 High, 1	

I004	(M)	Not Used	DC voltage	P1-e & P1-h +24 volts 0 volts	 Low, 0 High, 1	
I005	(M)	Not Used	DC voltage	P1-k & P1-n +24 volts 0 volts	 Low, 0 High, 1	
I006	(M)	Not Used	DC voltage	P1-r & P1-t +24 volts 0 volts	 Low, 0 High, 1	
I007	(M)	Not Used	DC voltage	P1-v & P1-x +24 volts 0 volts	 Low, 0 High, 1	
I008	(M)	Engine Start	DC voltage	P1-N & P1-R +24 volts 0 volts	 Low, 0 High, 1	 Engine Starting Not Starting
I009	(M)	Engine Running	DC voltage	P1-T & P1-V +24 volts 0 volts	 Low, 0 High, 1	 Engine Running Not Running
I010	(M)	Battery Failure	DC voltage	P1-X & P1-Z +24 volts 0 volts	 Low, 0 High, 1	 Battery Failure Battery OK
I011	(M)	Overcrank	DC voltage	P1-b & P1-d +24 volts 0 volts	 Low, 0 High, 1	 Overcrank OK
I012	(M)	Fail to Synchronize	DC voltage	P1-f & P1-j +24 volts 0 volts	 Low, 0 High, 1	 Fail to Sync OK
I013	(M)	Approach Low Lube Oil	DC Voltage	P1-m & P1-v +24 volts 0 volts	 Low, 0 High, 1	 Lube Oil Lvl Low Lube Oil OK
I014	(M)	Approach High Water Temp	DC voltage	P1-s & P1-u +24 volts 0 volts	 Low, 0 High, 1	 High Water Temp Water Temp OK
I015	(M)	Approach Load Limit	DC voltage	P1-w & P1-y +24 volts 0 volts	 Low, 0 High, 1	 At Limit OK

* C denotes a command function and M denotes a monitor function.

Correlator and Computer UPS Interfaces

The Computer and Correlator UPS systems M27's are installed in a bin in the UPS Room. M28 is installed in bin positions 1, 2 and 3, and M27s are installed in bin positions 4 and 5. The M27 in location 4 controls the Correlator UPS, and the M27 in 5 controls the Computer UPS. M28, the Power Supply/Battery Module, provides 12-volt M27 power and 26-volt power to the monitor interfaces in the UPS's.

The Correlator UPS M27 (position 4) address code is 5 and the Computer UPS M27 (position 5) address code is 6.

Drawing D13900W10 shows the bin wiring, control-monitor wiring between the M27's and the UPS units and the UPS Command and Monitor interface circuits.

Both UPS units are identical. The UPS units use only one command function, Reduce Input Limit, port bit IO0. This is an M27 relay contact closure; the NO contacts are connected to terminals 8 and 9 on TB1 in assembly A24. Setting a 0 in this port closes the NO relay contact and activates a command relay in the UPS.

The UPS monitor circuitry is also shown on D13900W10. Thirteen monitor functions are connected to TB1 in assembly A23. These are NC relay contacts in the UPS circuitry that are connected to the M28 +24 volt output and 24 volt return. When a monitored UPS state or alarm is false or a 0, the contacts are closed so the M27 monitor input is zero volts. When the function goes true, the contacts open and 24 volts is applied to the monitor optical isolator circuits. The Correlator and Computer UPS unit's interface signal characteristics and bit assignments are tabulated below.

Figures 2 and 5 show the Correlator UPS sub-screen.

Correlator and Computer UPS Interfaces with M27

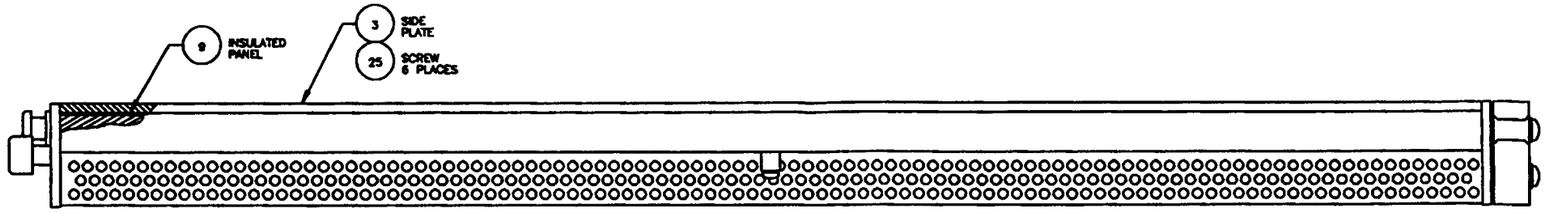
Int Bd Signal	Function	Signal Type	M27 Module I/O Pins & Levels	Int BD Port State	Signal Function
I000 (C)*	Reduce Input Limit	SPDT Relay Contacts	P1-P & P1-M open closed	Low, 0 High, 1	Cmd Active Cmd Inactive
I001 (C)	Not Used	SPDT Relay Contacts	P1-S & P1-U open closed	Low, 0 High, 1	
I002 (M)	Battery Volts Low	DC voltage	P1-W & P1-Y +24 volts 0 volts	Low, 0 High, 1	Low Batt Volts Batt Volts OK
I003 (M)	Battery Not Available	DC voltage	P1-a & P1-c +24 volts 0 volts	Low, 0 High, 1	Battery Not Avail Battery Avail
I004 (M)	UPS Overload Alarm	DC voltage	P1-e & P1-H +24 volts 0 volts	Low, 0 High, 1	UPS Overload No Overload
I005 (M)	Inlet Air Over Temp Alarm	DC voltage	P1-k & P1-n +24 volts 0 volts	Low, 0 High, 1	Temp Alarm No Alarm
I006 (M)	Transfer Not Available	DC voltage	P1-r & P1-t +24 volts 0 volts	Low, 0 High, 1	Transfer N/A Transfer Avail
I007 (M)	Retransfer Not Available	DC voltage	P1-v & P1-x +5 to 12 VDC 0 volts	Low, 0 High, 1	Manual Mode Computer Mode
I008 (M)	Not Used	DC voltage	P1-N & P1-R +24 volts 0 volts	Low, 0 High, 1	
I009 (M)	UPS Available	DC voltage	P1-T & P1-V +24 volts 0 volts	Low, 0 High, 1	UPS Avail UPS Not Avail
I010 (M)	UPS On Bypass	DC voltage	P1-X & P1-Z +24 volts 0 volts	Low, 0 High, 1	UPS On Bypass UPS Not On Bypass

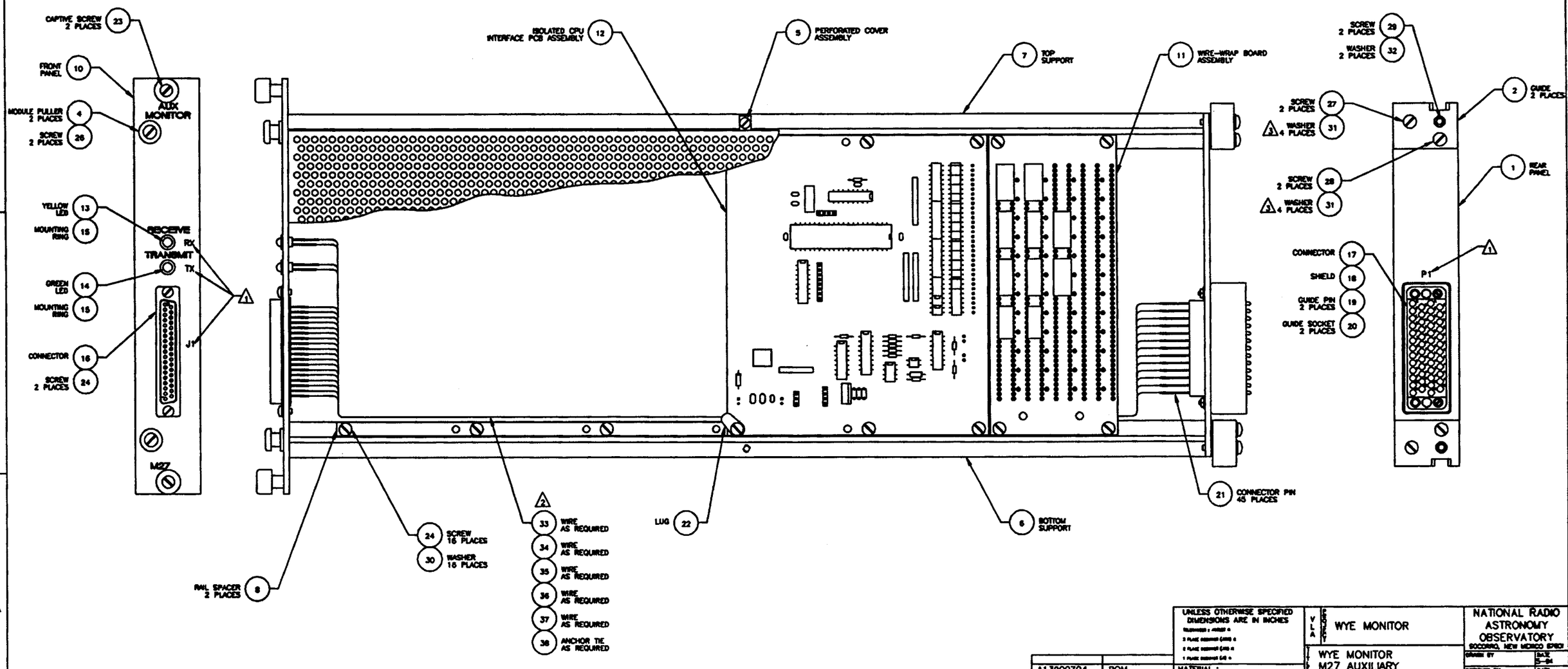
I011	(M)	5 Min Till UPS Shutdown	DC voltage	P1-b & P1-d +24 volts 0 volts	 Low, 0 High, 1	 5 Min Till S/D UPS OK
I012	(M)	Summary Alarm	DC voltage	P1-f & P1-j +24 volts 0 volts	 Low, 0 High, 1	 Summary Alarm No Alarm
I013	(M)	Minor Alarm	DC Voltage	P1-m & P1-u +24 volts 0 volts	 Low, 0 High, 1	 Minor Alarm No Alarm
I014	(M)	Major Alarm	DC voltage	P1-s & P1-u +24 volts 0 volts	 Low, 0 High, 1	 Major Alarm No Alarm
I015	(M)	UPS Input Failure	DC voltage	P1-w & P1-y +24 volts 0 volts	 Low, 0 High, 1	 UPS Input Fail UPS Input OK

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

NOTES:

1. MARKING SHALL BE .125 HIGH, LEGIBLE, AND PERMANENT. LOCATE ON INSIDE OF MODULE APPROXIMATELY AS SHOWN
2. A WIRING SERVICE LOOP OF SUFFICIENT LENGTH TO ALLOW FRONT AND REAR PANELS TO BE FOLDED FLAT MUST BE PROVIDED
3. PLACE ONE WASHER UNDER SCREW HEAD AND ONE WASHER BETWEEN REAR PANEL (ITEM 1) AND GUIDE (ITEM 2)





ACAD : 13900P20

A13900Z04	BOM
A13900W06	WIRE LIST
A13900W05	WIRING DIAG
D13900S08	SCHEMATIC
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL :

FINISH :

VLA PROJECT: WYE MONITOR

WYE MONITOR
M27 AUXILIARY MONITOR MODULE ASSEMBLY

SHEET NUMBER 1 or 1 | DRAWING NUMBER D13900P20 | REV. – | SCALE 1/1

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY | DATE 5-94
DESIGNED BY | DATE 5-94
APPROVED BY | DATE 5-94

BILL OF MATERIAL
NATIONAL RADIO ASTRONOMY OBSERVATORY

__X__ ELECTRICAL __X__ MECHANICAL BOM # A13900Z04 REV - DATE 6-01-94 PAGE 2 OF 4

MODULE M27 NAME AUXILIARY MONITOR DWG# D13900P20 SUB ASSY _____ DWG# _____

SCHEM. DWG# D13900S08 LOCATION WYE MON QUA/SYS. _____ PREPRD BY _____ APPRVD BY _____

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
1		NRAO	C13050M02	PANEL, REAR	1
2		NRAO	B13050M04	GUIDE	2
3		NRAO	C13050M06	PLATE, SIDE	1
4		NRAO	C13050M70	KNOB, MOUDLE PULLER	2
5		NRAO	C13050P21	ASSY, PERFORATED COVER	1
6		NRAO	C13720M15-1	SUPPORT, BOTTOM	1
7		NRAO	C13720M15-2	SUPPORT, TOP	1
8		NRAO	C13720M17	SPACER, INSULATED RAIL	2
9		NRAO	C13720M49	PANEL, INSULATED SIDE	1
10		NRAO	C13900M04	PANEL, FRONT	1
11		NRAO	C13900P21	CIRCUIT BOARD, WIRE-WRAP	1
12		NRAO	D13900P22	PCB, ISOLATED CPU INTERFACE	1
13	RX			LED, YELLOW	1
14	TX			LED, GREEN	1
15		HEWLETT PACKARD	HLMP-0103	RING, LED MOUNTING	2
16	J1	AMPHENOL	17D-C37S-F179	CONNECTOR, 37-PIN D-SUB	1
17	P1	AMP	201358-3	CONNECTOR, 50-PIN	1
18		AMP	202394-2	SHIELD, CONNECTOR	1
19		AMP	200833-4	PIN, GUIDE	2
20		AMP	203964-6	SOCKET, GUIDE	2

REVISIONS

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

USED ON | NEXT ASSY

DRAWN BY DATE 5-94
DESIGNED BY DATE 5-94
APPROVED BY DATE 5-94

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

V L A

PROJECT WYE MONITOR
TITLE M27 AUXILIARY MONITOR MODULE BOM
DWG NO. A13900Z04
SHEET 1 OF 4

BILL OF MATERIAL
NATIONAL RADIO ASTRONOMY OBSERVATORY

X ELECTRICAL X MECHANICAL BOM # A13900Z04 REV — DATE 6-01-94 PAGE 4 OF 4

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
39					
40		NRAO	D13900AB0	SILKSCREEN, FRONT PANEL	---
41		NRAO	D13900P20	ASSEMBLY, M27 MODULE	---
42		NRAO	A13900P23	ASSEMBLY, DIP HEADER	---
43		NRAO	D13900S08	SCHEMATIC, M27 MODULE	---
44		NRAO	A13900W05	WIRING DIAGRAM, CONNECTOR	---
45		NRAO	A13900W06	WIRE LIST, M27 MODULE	---
46		NRAO	A13900Z04	BOM	---
47					
48					
49					
50					
51					
52					
53					
54					
55					
56					
57					
58					
59					
60					

BILL OF MATERIAL
NATIONAL RADIO ASTRONOMY OBSERVATORY

X ELECTRICAL X MECHANICAL BOM # A13900Z04 REV - DATE 6-01-94 PAGE 3 OF 4

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
21		AMP	610488-1	PIN, CONNECTOR/WW POST	45
22		H.H. SMITH	1411-4	LUG, SOLDER #4	1
23		SOUTHCO	47-10-204-10	SCREW, CAPTIVE	2
24				SCREW, PAN HD, SS, 4-40UNC-2A x .25	18
25				SCREW, FLT HD, SS, 6-32UNC-2A x .25	6
26				SCREW, FLT HD, SS, 6-32UNC-2A x .75	2
27				SCREW, PN HD, SS, 6-32UNC-2A x .75	2
28				SCREW, PN HD, SS, 6-32UNC-2A x 1.00	2
29				SCREW, SOCK HD, SS, 6-32UNC-2A x 1.00	2
30				WASHER, #4, EXT. TOOTH	16
31				WASHER, #6, EXT. TOOTH	8
32				WASHER, #6, SPLIT RING LOCK	2
33		ALPHA	7053	WIRE, RED, #26 GA.	AR
34		ALPHA	7053	WIRE, BLK, #26 GA.	AR
35		ALPHA	7053	WIRE, ORG, #26 GA.	AR
36		ALPHA	7053	WIRE, GRN, #26 GA.	AR
37		ALPHA	7053	WIRE, BLU, #26 GA.	AR
38		PANDUIT	TA1S8	TIE, ANCHOR	AR

REV.	DATE	DRAWN BY	APROV'D BY	DESCRIPTION
A	6-93			REMOVED NOMENCLATURE
B	3-94			ADDED MODULE PORTS
C	6-94			ADDED WIRE LIST TABLE

NOTES:

1. ADDRESS MODULE, ADDRESS SWITCH S1 IS NOT INSTALLED UNLESS FOR TESTING. S1 IS BINARY WITH BITS GROUNDED TO DRIVE TO 0 OR FLOATING FOR 1
2. P1602 (Z1) REPLACES RV1, RV2, RV3
3. RETURN WIRES ARE TIED TO COMMON
4. VCC = +5VOLTS

MODULE ADDRESS

ISOLATED COMMUNICATION INTERFACE

POWER CONDITIONING

WATCHDOG RESET

PORT			CORRELATOR AND COMPUTER UPS	MASTER CUBICLE	GENERATORS 1 AND 2
PORT PIN	DESCRIPTION	AMP PIN	FUNCTION	FUNCTION	FUNCTION
P0.0	COMMAND PORT	M P	REDUCE INPUT RETURN	START GENERATOR RETURN	UNUSED UNUSED
P0.1	COMMAND PORT	S U	UNUSED UNUSED	UNUSED UNUSED	UNUSED UNUSED
P0.2	MONITOR PORT	V Y	BATTERY VOLTS LOW RETURN	NON-CRITICAL POWER RESET (ENABLE/DISABLE) RETURN	GENERATOR CIRCUIT BREAKER RETURN
P0.3	MONITOR PORT	a c	BATTERY NOT AVAILABLE RETURN	GENERATOR TIE BREAKER (OPERATE/CLOSED) RETURN	REMOTE CIRCUIT BREAKER RETURN
P0.4	MONITOR PORT	e h	UPS OVERLOAD ALARM RETURN	UTILITY BREAKER (OPERATE/CLOSED) RETURN	UNUSED UNUSED
P0.5	MONITOR PORT	k n	INLET AIR - OVER TEMPERATURE ALARM RETURN	UNUSED UNUSED	UNUSED UNUSED
P0.6	MONITOR PORT	r t	TRANSFER NOT AVAILABLE RETURN	UNUSED UNUSED	UNUSED UNUSED
P0.7	MONITOR PORT	v x	RETRANSFER NOT AVAILABLE RETURN	UNUSED UNUSED	UNUSED UNUSED
P1.0	MONITOR PORT	N R	UNUSED UNUSED	AC CONTROL VOLTAGE RETURN	ENGINE START RETURN
P1.1	MONITOR PORT	T V	UPS AVAILABLE RETURN	#1 DAY TANK LOW FUEL RETURN	ENGINE RUNNING RETURN
P1.2	MONITOR PORT	X Z	UPS ON BYPASS RETURN	#2 DAY TANK LOW FUEL RETURN	BATTERY FAILURE RETURN
P1.3	MONITOR PORT	b d	5 MINUTES TILL UPS SHUTDOWN RETURN	VOLTAGE/FREQUENCY FAIL RETURN	OVERCRANK RETURN
P1.4	MONITOR PORT	f j	SUMMARY ALARM RETURN	LOAD SHED ACTIVATED RETURN	FAILURE TO SYNCHRONIZE RETURN
P1.5	MONITOR PORT	m p	MINOR ALARM RETURN	ALARM HORN RETURN	APPROACH LOW LUBE OIL RETURN
P1.6	MONITOR PORT	s w	MAJOR ALARM RETURN	125V BATTERY RETURN	APPROACH HIGH WATER TEMP RETURN
P1.7	MONITOR PORT	u v	UPS INPUT FAILURE RETURN	UNUSED UNUSED	APPROACH LOAD LIMIT RETURN
		F L	+24V +24V GND	+24V +24V GND	+24V +24V GND
		H K	LINE+ LINE-	LINE+ LINE-	LINE+ LINE-

PRINTED CIRCUIT BOARD | SCRUB BRUSH

PRINTED CIRCUIT BOARD | SCRUB BRUSH

PRINTED CIRCUIT BOARD | SCRUB BRUSH

A13900Z04	BOM
C13900V05	WIRING DIAG
D13900P00	ASSEMBLY
NEXT ASSEMBLY	DVG TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMAL (.XXX) ±
2 PLACE DECIMALS (.XX) ±
1 PLACE DECIMALS (.X) ±

MATERIAL:

FINISH:

VLA PROJECT: WYE MONITOR

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO,NEW MEXICO 87801

TITLE: WYE MONITOR
M27 AUXILIARY
MONITOR MODULE
SCHEMATIC DIAGRAM

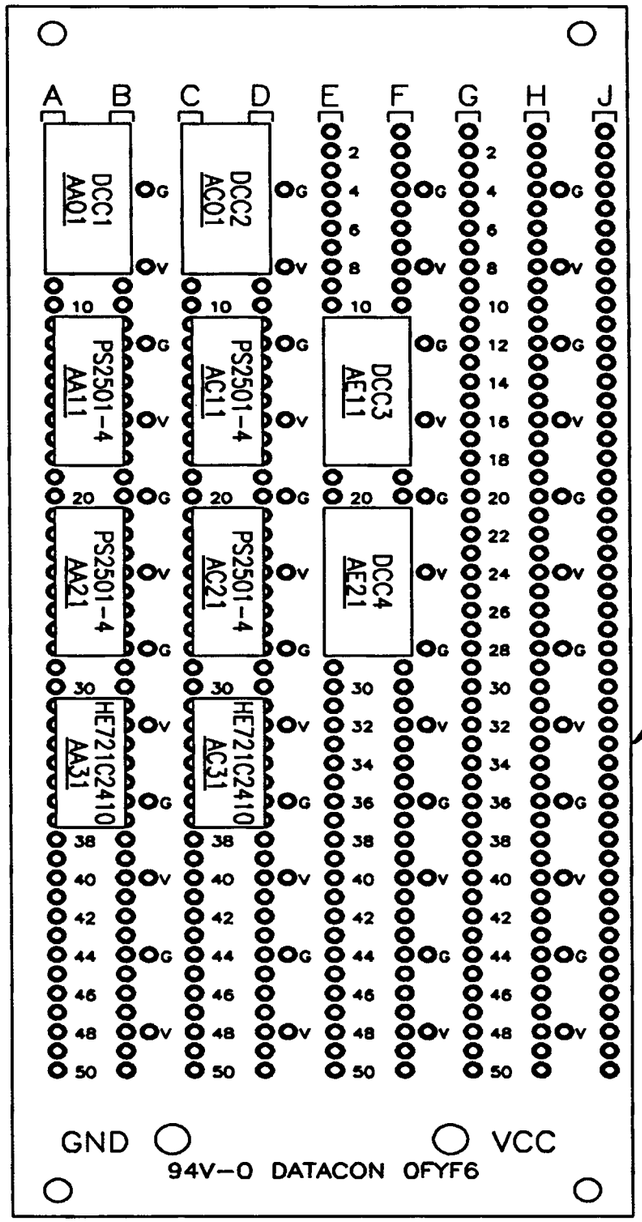
DRAWN BY		DATE	3-93
DESIGNED BY		DATE	3-93
APPROVED BY		DATE	3-93
SHEET NUMBER	1 OF 1	DRAWING NUMBER	D13900S08
REV.	C	SCALE	-

ORCAD : 13900S08

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

NOTES:

1. INSTALLED ON AUGAT 606-CG1 DIP HEADER.
   REF: DIP HEADER ASSEMBLY, DWG. #A13900P23



1 WIRE-WRAP BOARD

DCC1 AA01 (1)

1	4.7K	16
	4.7K	
	4.7K	
	4.7K	
	4.7K	
	4.7K	
	4.7K	
8	4.7K	9

DCC2 AC01 (1)

1	4.7K	16
	4.7K	
	4.7K	
	4.7K	
	4.7K	
	4.7K	
	4.7K	
8	4.7K	9

DCC3 AE11 (1)

1	10K	16
	10K	
	10K	
	10K	
	10K	
	10K	
	10K	
8	10K	9

DCC4 AE21 (1)

1	10K	16
	10K	
	10K	
	10K	
	10K	
	10K	
	10K	
8	10K	9

ITEM NO.	REF. DES.	MANUFACTURER	PART NUMBER	DESCRIPTION	QTY
3		HAMLIN	HE721C2410	RELAY, DIP	2
2		NEC	PS2501-4	OPTOISOLATOR	4
1				BOARD, WIRE-WRAP	1

D13900S08	SCHEMATIC
A13900P23	DIP HEADER
A13900P20	ASSEMBLY
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES : ANGLES ±
2 PLACE DECIMALS (.XX) ±
3 PLACE DECIMALS (.XXX) ±
1 PLACE DECIMALS (.X) ±

MATERIAL :

FINISH :

VLA ELECTRONICS

WYE MONITOR

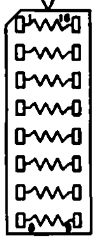
TITLE: M27 AUXILIARY MONITOR MODULE WIRE-WRAP BOARD COMPONENT LAYOUT

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 5-94
DESIGNED BY	DATE 5-94
APPROVED BY	DATE 5-94

SHEET NUMBER 1 OF 1 | DRAWING NUMBER C13900P21 | REV. — | SCALE 2/1

ACAD : 13900P21



DESCRIPTION	VALUE	MFG.	PART NO.
DIP HEADER			
RESISTOR	4.7K, 1/4W, 5%	ALLEN-BRADLEY	CB4725
RESISTOR	4.7K, 1/4W, 5%	ALLEN-BRADLEY	CB4725
RESISTOR	4.7K, 1/4W, 5%	ALLEN-BRADLEY	CB4725
RESISTOR	4.7K, 1/4W, 5%	ALLEN-BRADLEY	CB4725
RESISTOR	4.7K, 1/4W, 5%	ALLEN-BRADLEY	CB4725
RESISTOR	4.7K, 1/4W, 5%	ALLEN-BRADLEY	CB4725
RESISTOR	4.7K, 1/4W, 5%	ALLEN-BRADLEY	CB4725
RESISTOR	4.7K, 1/4W, 5%	ALLEN-BRADLEY	CB4725

MODULE: M27 AUXILIARY MONITOR

BOARD LOCATION: AA01, AC01

DRAWING NO. A13900P23 | SHEET 2 OF 3 | REV –

REVISIONS

REV	DATE	DRAWN BY	APPROVED BY	DESCRIPTION

DRAWN BY	DATE	5-94
DESIGNED BY	DATE	5-94
APPROVED BY	DATE	5-94

D13900S08	SCHEMATIC
C13900P20	ASSEMBLY
NEXT ASSY	USED ON

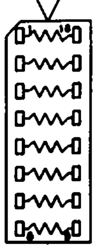
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLA

PROJECT: WYE MONITOR

TITLE: M27 AUXILIARY MONITOR MODULE DIP HEADER ASSEMBLY

DWG NO. A13900P23 | SHEET 1 OF 3



DESCRIPTION	VALUE	MFG.	PART NO.
DIP HEADER			
RESISTOR	10K, 1/4W, 5%	ALLEN-BRADLEY	CB1035
RESISTOR	10K, 1/4W, 5%	ALLEN-BRADLEY	CB1035
RESISTOR	10K, 1/4W, 5%	ALLEN-BRADLEY	CB1035
RESISTOR	10K, 1/4W, 5%	ALLEN-BRADLEY	CB1035
RESISTOR	10K, 1/4W, 5%	ALLEN-BRADLEY	CB1035
RESISTOR	10K, 1/4W, 5%	ALLEN-BRADLEY	CB1035
RESISTOR	10K, 1/4W, 5%	ALLEN-BRADLEY	CB1035
RESISTOR	10K, 1/4W, 5%	ALLEN-BRADLEY	CB1035

MODULE: M27 AUXILIARY MONITOR

BOARD LOCATION: AE11, AE21

DRAWING NO. A13900P23

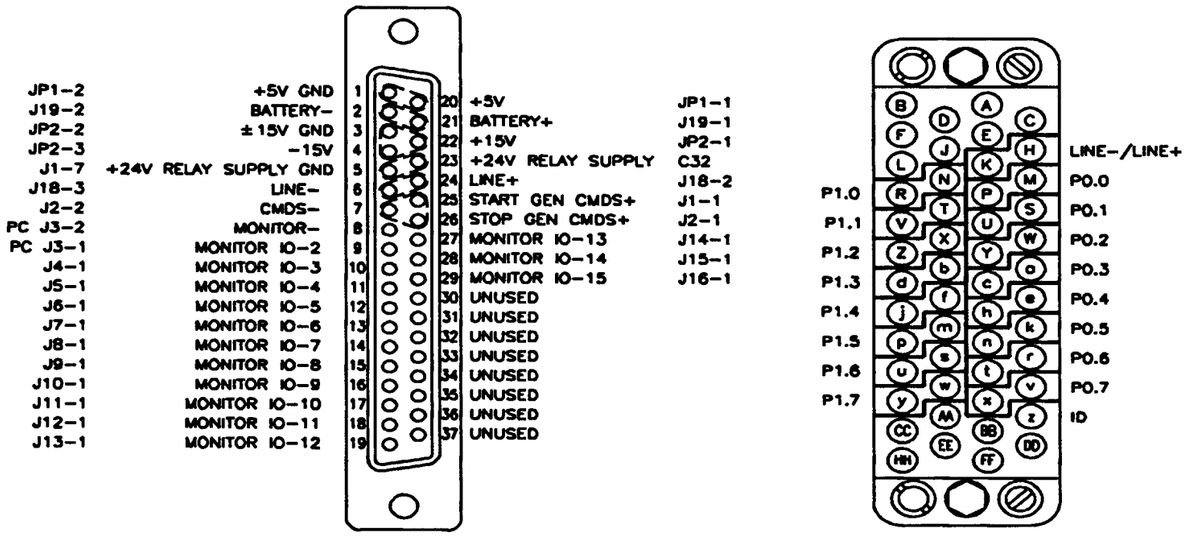
SHEET 3 OF 3

REV -

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	6-94			ADDED CONNECTOR P1

NOTE:

1. — — = GROUP SIGNALS



FRONT PANEL CONNECTOR — J1

VIEWED FROM MODULE FRONT

PORT			CORRELATOR AND COMPUTER UPS	MASTER CUBICLE	GENERATORS 1 AND 2
PORT PIN	FUNCTION	AMP PIN	FUNCTION	FUNCTION	FUNCTION
P0.0	COMMAND PORT	M P	REDUCE INPUT RETURN	START GENERATORS RETURN	UNUSED UNUSED
P0.1	COMMAND PORT	S U	UNUSED UNUSED	UNUSED UNUSED	UNUSED UNUSED
P0.2	MONITOR PORT	W Y	BATTERY VOLTAGE LOW RETURN	NCP RESET (ENABLE/DISABLE) RETURN	GENERATOR CIRCUIT BREAKER RETURN
P0.3	MONITOR PORT	a c	BATTERY NOT AVAILABLE RETURN	GEN TIE BREAKER (OPERATE/CLOSED) RETURN	REMOTE CIRCUIT BREAKER RETURN
P0.4	MONITOR PORT	e h	UPS OVERLOAD ALARM RETURN	UTILITY BREAKER (OPERATE/CLOSED) RETURN	UNUSED UNUSED
P0.5	MONITOR PORT	k n	INLET AIR-OVER TEMP ALARM RETURN	UNUSED UNUSED	UNUSED UNUSED
P0.6	MONITOR PORT	r t	TRANSFER NOT AVAILABLE RETURN	UNUSED UNUSED	UNUSED UNUSED
P0.7	MONITOR PORT	v x	RETRANSFER NOT AVAILABLE RETURN	UNUSED UNUSED	UNUSED UNUSED
P1.0	MONITOR PORT	N R	UNUSED UNUSED	AC CONTROL VOLTAGE RETURN	ENGINE START RETURN
P1.1	MONITOR PORT	T V	UPS AVAILABLE RETURN	#1 DAY TANK LOW FUEL RETURN	ENGINE RUNNING RETURN
P1.2	MONITOR PORT	X Z	UPS ON BYPASS RETURN	#2 DAY TANK LOW FUEL RETURN	BATTERY FAILURE RETURN
P1.3	MONITOR PORT	b d	5 MINUTES TILL SHUTDOWN RETURN	VOLATAGE/FREQUENCY FAIL RETURN	OVERCRANK RETURN
P1.4	MONITOR PORT	f j	SUMMARY ALARM RETURN	LOAD SHED ACTIVATED RETURN	FAILURE TO SYNCHRONIZE RETURN
P1.5	MONITOR PORT	m p	MINOR ALARM RETURN	ALARM HORN RETURN	APPROACH LOW LUBE OIL RETURN
P1.6	MONITOR PORT	s u	MAJOR ALARM RETURN	125V BATTERY RETURN	APPROACH HIGH WATER TEMP RETURN
P1.7	MONITOR PORT	w y	UPS INPUT FAILURE RETURN	UNUSED UNUSED	APPROACH LOAD LIMIT RETURN
		F L	+24V +24 GND	+24V +24 GND	+24V +24 GND
		H K	LINE+ LINE-	LINE+ LINE-	LINE+ LINE-

REAR PANEL CONNECTOR — P1

VIEWED FROM MODULE REAR

ACAD : 13900W05

D13900S08	SCHEMATIC
A13900Z04	BOM
D13900P20	ASSEMBLY
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES : ANGLES ±
3 PLACE DECIMALS (.XXX) ±
2 PLACE DECIMALS (.XX) ±
1 PLACE DECIMALS (.X) ±

MATERIAL :

FINISH :

VLA SCHEMATIC: WYE MONITOR

TITLE: M27 AUXILIARY MONITOR MODULE CONNECTOR TEST POINTS WIRING DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

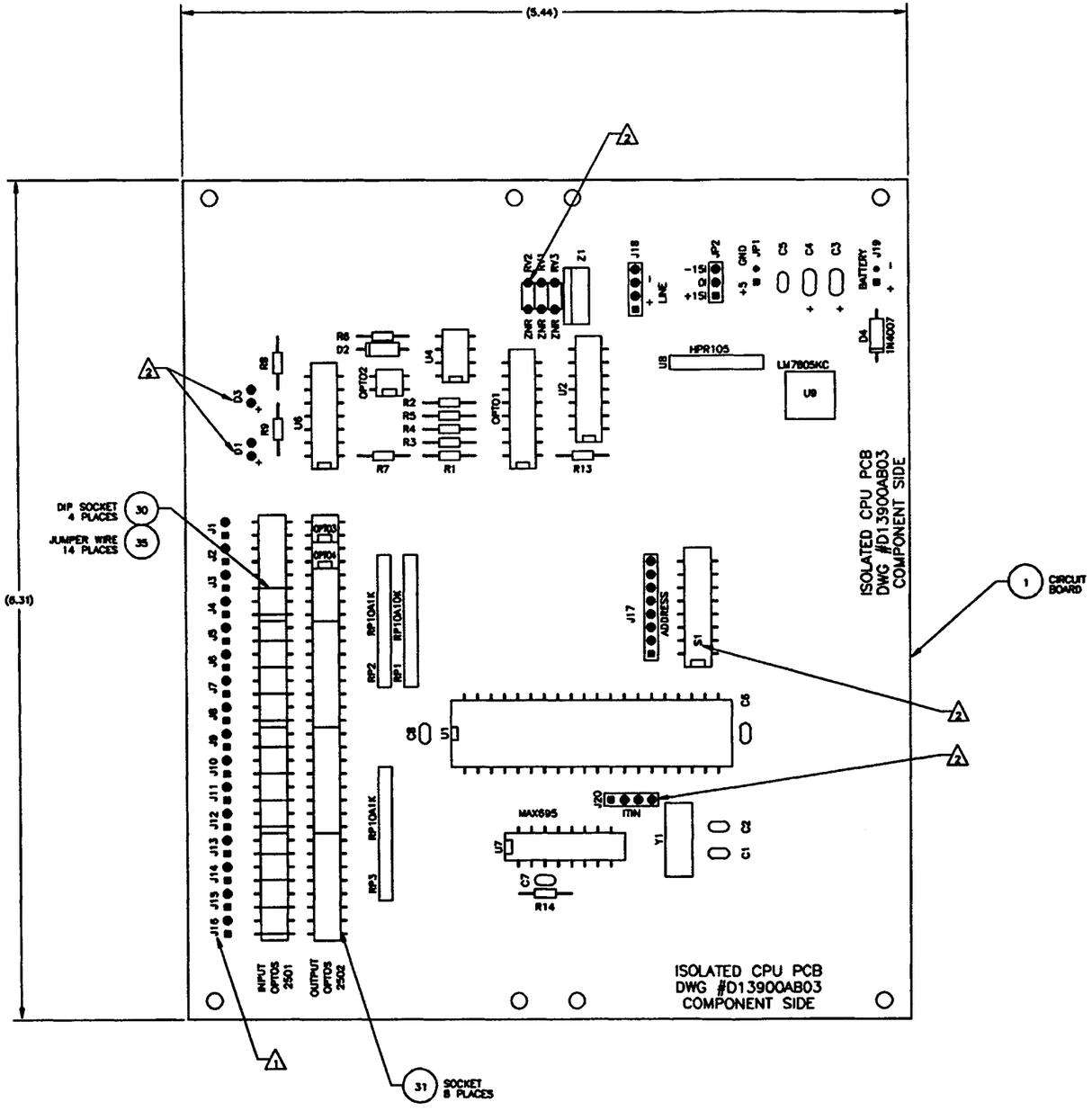
DRAWN BY	DATE 5-94
DESIGNED BY	DATE 5-94
APPROVED BY	DATE 5-94

SHEET NUMBER 1 OF 1 | DRAWING NUMBER C13900W05 | REV. A | SCALE 2/1

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

NOTES:

1. REFERENCE DESIGNATORS JXX AND JPXX = WIRE-WRAP CONNECTIONS. MOUNT WIRE-WRAP PINS ON CIRCUIT SIDE OF PC BOARD
2. NOT INSTALLED



COMPONENT SIDE

ITEM NO.	REF. DES.	MANUFACTURER	PART NUMBER	DESCRIPTION	QTY
35				WIRE, JUMPER	14
34	J1-J16 J1-J16			PIN, WIRE WRAP	55
33	U1	AMP	2-640379-3	SOCKET, 40-PIN	1
32	U4	AMP	2-640463-3	SOCKET, 8-PIN	1
31	OPTO1 OPTO1-OPTO4	AMP	2-640358-3	SOCKET, 16-PIN	10
30		AUGAT	616-CG1	SOCKET, 16-PIN	4
29	Z1	TECCOR	P1602	SURGE SUPPRESSOR	1
28	Y1	ECS	ECS-110.5-20-4	CRYSTAL, 11.0592 MHZ	1
27	U9	NATIONAL	LM7805KC	VOLTAGE REGULATOR	1
26	U8	BURR BROWN	HPR105	DC-DC CONVERTER	1
25	U7	MAXIM	MAX695	IC, 16-PIN	1
24	U6	SIGNETICS	74HCT32	IC, 14-PIN	1
23	U4	PMI	OP15	IC, 8-PIN	1
22	U2	SIGNETICS	74HCT00	IC, 14-PIN	1
21	U1	INTEL	87C51FA	IC, 40-PIN	1
20	S1		SW DIP-8	SWITCH	1
19	R14			RESISTOR, 10	1
18	R13			RESISTOR, 150	1
17	R8-R9			RESISTOR, 1K	2
16	R6-R7			RESISTOR, 10K	2
15	R3-R5			RESISTOR, 330K	3
14	R1-R2			RESISTOR, 51K	2
13	RV1-RV3	PANASONIC	ZNR 10K680	SURGE SUPPRESSOR	3
12	RP2-RP3		RP10A1K	RESISTOR PACK, 1K	2
11	RP1		RP10A10K	RESISTOR PACK, 10K	1
10	OPTO3,OPTO4	NEC	PS2502-1	OPTOISOLATOR	2
9	OPTO2	PMI	OP15	OPTOISOLATOR	1
8	OPTO1	NEC	PS2501-4	OPTOISOLATOR	1
7	D4		1N4007	DIODE	1
6	D2		1N914	DIODE	1
5	D1, D3			LED	2
4	C5-C8			CAPACITOR, 0.1uf	4
3	C3, C4			CAPACITOR, 10uf	2
2	C1, C2			CAPACITOR, 33pf	2
1		NRAO	D13900AB03	CIRCUIT BOARD	1

D13900S08	SCHEMATIC
D13900M03	DRILL DWG
D13900AB06	SOLDER MASK
D13900AB05	SILKSCREEN
D13900P20	ASSEMBLY
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL :

FINISH :

WYE MONITOR

M27
AUXILIARY MONITOR
ISOLATED CPU
INTERFACE BOARD ASSY

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

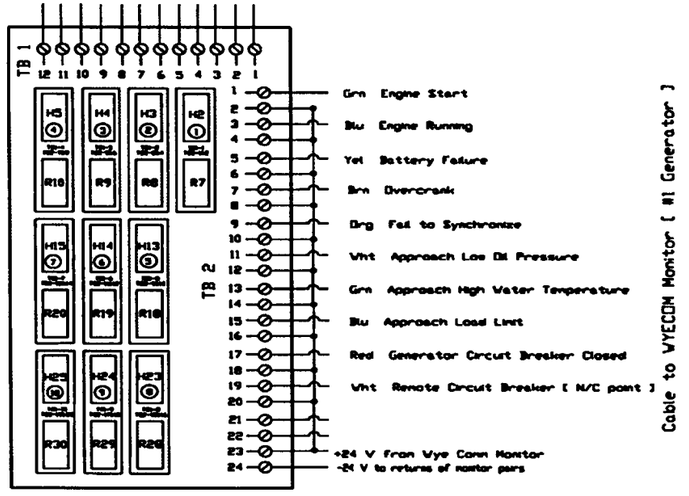
DRAWN BY — DATE 5-94
DESIGNED BY — DATE 9-92
APPROVED BY — DATE 5-94

SHEET NUMBER 1 OF 1 | DRAWING NUMBER D13900P22 | REV. — | SCALE 2/1

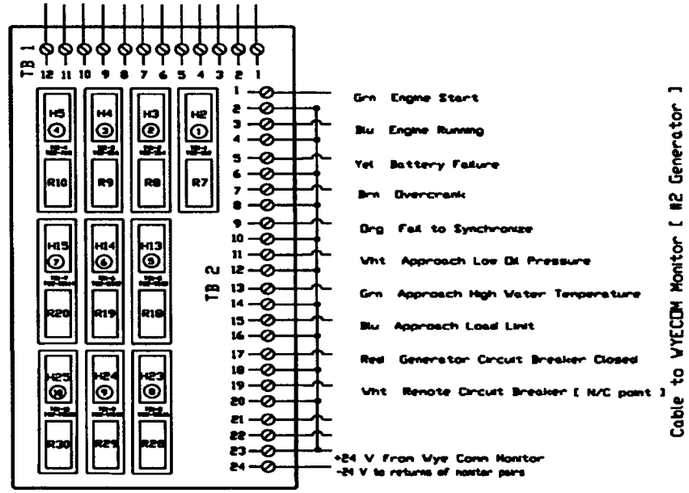
ACAD : 13900P22

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

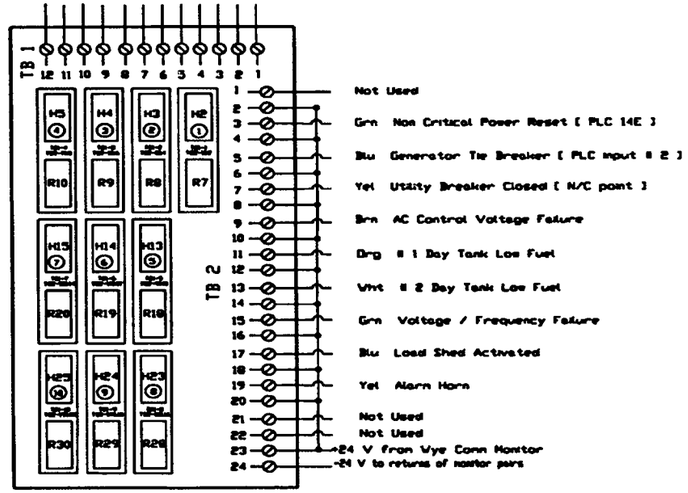
Generator 1 Monitor Board



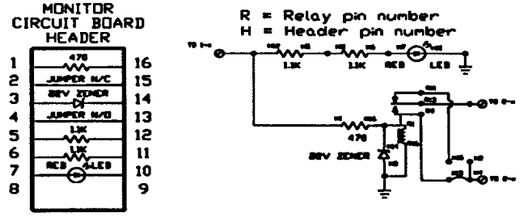
Generator 2 Monitor Board



Master Cubical Monitor Board



Typical Relay and Header Pair



NOTE: See board drawing for Relay - Header to terminal block locations.

ACAD LABEL: 9390028A

SEE ALSO SHEET NO.	QTY.	DESCRIPTION	MATL./SPECIFICATION	ITEM

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ± 1°
3 PLACE DECIMALS (.xxx) ± .005
2 PLACE DECIMALS (.xx) ± .01
1 PLACE DECIMALS (.x) ± .05

MATERIAL: _____

FINISH: _____

VLA

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE:
DESIGNED BY	DATE:
APPROVED BY	DATE:

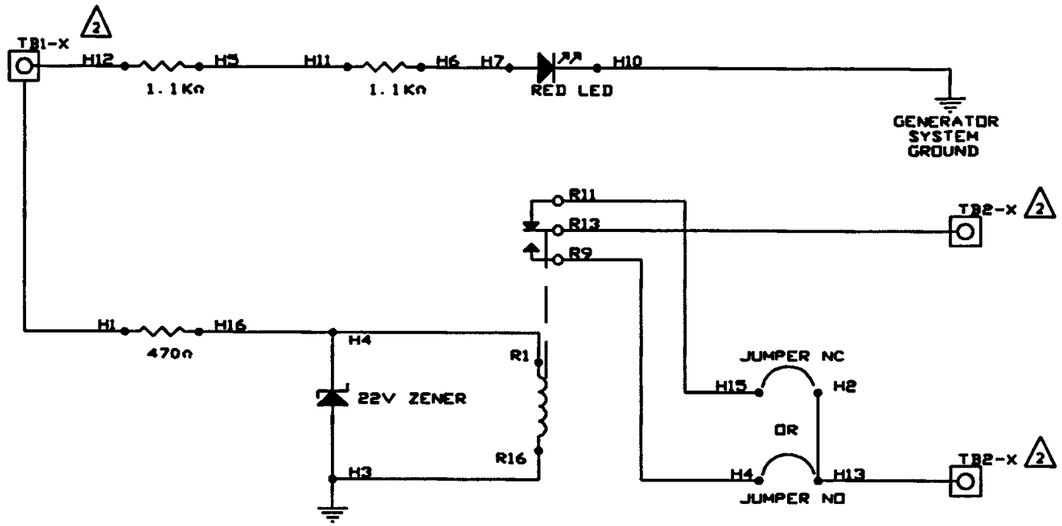
SHEET NUMBER 1 OF 1 | DRAWING NUMBER C9390028 | REV. | SCALE: NOTED

REV.	DATE	DRAWN BY	APROV'D BY	DESCRIPTION

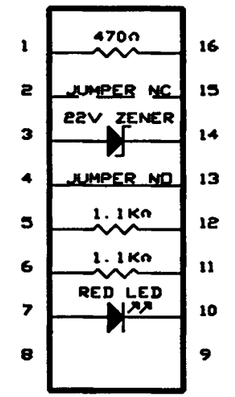
NOTES:

1. R = RELAYER PIN NUMBER
   H = HEADER PIN NUMBER

(2) REFERENCE NRAO DRAWING NUMBER C9390028 FOR HEADER TO TERMINAL BLOCK LOCATIONS



MONITOR CIRCUIT BOARD HEADER



ORCAD : 13900S12

NEXT ASSEMBLY	DWG TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX) ±
2 PLACE DECIMALS (.XX) ±
1 PLACE DECIMALS (.X) ±

MATERIAL:

FINISH:

VLA PROJECT: WYE MONITOR

TITLE: WYE MONITOR
MASTER CUBICLE
RELAY AND HEADER
SCHEMATIC DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO,NEW MEXICO 87801

DRAWN BY	DATE 5-94
DESIGNED BY	DATE 5-94
APPROVED BY	DATE 5-94

SHEET NUMBER 1 OF 1 | DRAWING NUMBER B13900S12 | REV. - | SCALE -

NOTES:

1. (CL) AND (OP) DESIGNATE CONTACT STATUS WHEN UPS INPUT POWER IS OFF
2. CSC CONTACTS ARE CLOSED TO "C" (COMMON) ON STATED CONDITION
3. THESE CSC CONTACT ASSIGNMENTS DISAGREE WITH IPM-LORTEC DRAWING #950-010-0413. THE IPM-LORTEC IS INCORRECT
4. LEGEND: (REFERENCE NRAO DRAWING #D13900S08)
   (C) COMMON OUTPUT PORT
   (M) MONITOR INPUT PORT
   J +24V JUMPER STRING

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

WYE MONITOR SYSTEM BIN

CORRELATOR M27 BIN POS 4

COMPUTER M27 BIN POS 5

M28 BIN POS 3

CORRELATOR UPS

TB1-3	CSC	K2 (CL)	BATTERY VOLTAGE LOW	TB1-1
TB1-6	CSC	K1 (CL)	UPS INPUT FAILURE WITH NO TIME DELAY	TB1-14
TB1-9	CSC (3)	K3 (CL)	UPS ON BYPASS	TB1-7
TB1-12	CSC	K4 (OP)	UPS AVAILABLE	TB1-11
TB1-15	CSC (3)	K5	UPS INPUT FAILURE WITH TIME DELAY	TB1-13
TB1-18	CSC (3)	K6 (CL)	SUMMARY ALARM	TB1-16
TB1-21	CSC (3)	K7 (CL)	MAJOR ALARM	TB1-19
TB2-3	CSC (3)	K8 (CL)	TRANFER NOT AVAILABLE	TB2-1
TB2-6	CSC (3)	K9 (CL)	RETRANSFER NOT AVAILABLE	TB2-4
TB2-9	CSC (3)	K10 (CL)	BATTERY NOT AVAILABLE	TB2-7
TB2-12	CSC	K11 (CL)	INLET AIR OVERTEMP ALARM	TB2-10
TB2-15	CSC	K12 (CL)	UPS OVERLOAD ALARM	TB2-13
TB2-18	CSC	K13 (OP)	MINOR ALARM	TB2-17
TB2-21	CSC	K14 (CL)	5 MIN TIL UPS SHUTDOWN	TB2-20

MONITOR INTERFACE ASSY, A23

CONTROL INTERFACE ASSY, A24

+24V — KX — TB1-8 (WHT/RED), TB1-9 (BLU/RED)

TB1-1	BLK	I02 (M)		
TB1-14	RED	I10 (M)		
TB1-7	RED/BLK	I09 (M)		
TB1-11	RED/GRN	I15 (M)		
TB1-13	NOT USED	I12 (M)		
TB1-16	RED/WHT	I14 (M)		
TB1-19	ORG	I06 (M)		
TB2-1	WHT/BLK	I07 (M)		
TB2-4	BLU/BLK	I03 (M)		
TB2-7	BLU/WHT	I05 (M)		
TB2-10	BLU	I04 (M)		
TB2-13	GRN	I13 (M)		
TB2-17	BLK/WHT	I11 (M)		
TB2-20	GRN/BLK/WHT	I08 (M)	NOT USED	
		I00 (C)		
		I01 (C)	NOT USED	
	WHT	+24V		
		+24V GND		
	AUX WYE MONITOR BUS LINE +	LINE +		
	AUX WYE MONITOR BUS LINE −	LINE −		
		+12V		
		+12V GND		

P2: A B C — 110 AC, NEUTRAL

P1: +12V, +12V GND, +24V, +24V GND — D B F L

J1: D B F L

BLK

RED

COMPUTER UPS

BLK	TB1-1	BATTERY VOLTAGE LOW	CSC	TB1-3
RED	TB1-14	UPS INPUT FAILURE WITH NO TIME DELAY	K2 (CL) CSC	TB1-6
RED/BLK	TB1-7	UPS ON BYPASS	K1 (CL) (3) CSC	TB1-9
RED/GRN	TB1-11	UPS AVAILABLE	K3 (CL) CSC	TB1-12
NOT USED	TB1-13	UPS INPUT FAILURE WITH TIME DELAY	K4 (OP) (3) CSC	TB1-15
RED/WHT	TB1-16	SUMMARY ALARM	K5 (3) CSC	TB1-18
ORG	TB1-19	MAJOR ALARM	K6 (CL) (3) CSC	TB1-21
WHT/BLK	TB2-1	TRANFER NOT AVAILABLE	K7 (CL) (3) CSC	TB2-3
BLU/BLK	TB2-4	RETRANSFER NOT AVAILABLE	K8 (CL) (3) CSC	TB2-6
BLU/WHT	TB2-7	BATTERY NOT AVAILABLE	K9 (CL) (3) CSC	TB2-9
BLU	TB2-10	INLET AIR OVERTEMP ALARM	K10 (CL) CSC	TB2-12
GRN	TB2-13	UPS OVERLOAD ALARM	K11 (CL) CSC	TB2-15
BLK/WHT	TB2-17	MINOR ALARM	K12 (CL) CSC	TB2-18
GRN/BLK/WHT	TB2-19	5 MIN TIL UPS SHUTDOWN	K13 (OP) CSC	TB2-21

MONITOR INTERFACE ASSY, A23

WHT/RED — TB1-8; BLU/RED — TB1-9 — KX — +24V

CONTROL INTERFACE ASSY, A24

NOT USED

WHT

COMPUTER UPS

CORRELATOR UPS CONTROL/MON

COMPUTER UPS CONTROL/MON

WYE MONITOR BIN

WYE MONITOR RACK LOCATED IN NORTHEAST CORNER OF UPS ROOM

BIN POSITION: M28, M27, M26; 3 4 5

FRONT VIEW

REAR VIEW: M27, M26; J1, J1, J2

ACAD : 13900W09

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL :

FINISH :

NEXT ASSEMBLY | DWG. TYPE

VLA — WYE MONITOR

TITLE: WYE MONITOR
M27 – CORRELATOR AND UPS INTERFACE WIRING DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY | DATE 9-94
DESIGNED BY | DATE 9-94
APPROVED BY | DATE

SHEET NUMBER 1 OF 1 | DRAWING NUMBER D13900W09 | REV. – | SCALE NONE

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

NOTES:

1. (CL) AND (OP) DESIGNATE CONTACT STATUS WHEN UPS INPUT POWER IS OFF
2. CSC CONTACTS ARE CLOSED TO "C" (COMMON) ON STATED CONDITION
3. LEGEND: (REFERENCE NRAO DRAWING #D13900S08)
   (C) COMMON OUTPUT PORT
   (M) MONITOR INPUT PORT
   J +24V JUMPER STRING

4. BLACK RETURNS ARE CONNECTED TO TB2-24 VIA BUTT SPLICE
5. RED RETURNS ARE CONNECTED TO TB2-24 VIA BUTT SPLICE
6. UNUSED PAIRS IN MASTER CUBICLE M27, POSITION 6 ARE STUBBED OFF

5. 125VDC BATTERY ALARM RELAY CLOSES AT 122VDC AND OPENS AT 119VDC

WYE MONITOR SYSTEM BIN

GENERATOR #1 (EAST) CONTROL CABINET

GENERATOR #1 (EAST) MONITOR INTERFACE NRAO DRAWING #C9390028

FROM WYE MONITOR SYSTEM

TB2-1	ENGINE START	GRN	N	N	N	I08, P1.0 (M)
TB2-2		BLK (4)	R	R	R	
TB2-3	ENGINE RUNNING	BLU	T	T	T	I09, P1.1 (M)
TB2-4 (J)		BLK (4)	V	V	V	
TB2-5	BATTERY FAILURE	YEL	X	X	X	I010, P1.2 (M)
TB2-6 (J)		BLK (4)	Z	Z	Z	
TB2-7	OVERCRANK	BRN	b	b	b	I011, P1.3 (M)
TB2-8 (J)		BLK (4)	d	d	d	
TB2-9	FAILURE TO SYNCHRONIZE	ORG	f	f	f	I012, P1.4 (M)
TB2-10 (J)		BLK (4)	j	j	j	
TB2-11	APPROACH LOW LUBE OIL	WHT	m	m	m	I013, P1.5 (M)
TB2-12 (J)		RED (5)	p	p	p	
TB2-13	APPROACH HIGH WATER TEMPERATURE	GRN	s	s	s	I014, P1.6 (M)
TB2-14 (J)		RED (5)	u	u	u	
TB2-15	APPROACH LOAD LIMIT	BLU	w	w	w	I015, P1.7 (M)
TB2-16 (J)		RED (5)	y	y	y	
TB2-17	GENERATOR CIRCUIT BREAKER	RED	W	W	W	I02, P0.2 (M)
TB2-18 (J)		BLK (4)	Y	Y	Y	
TB2-19	REMOTE CIRCUIT BREAKER	WHT	a	a	a	I03, P0.3 (M)
TB2-20 (J)		BLK (4)	c	c	c	
TB2-21		UNUSED	e	e	e	I04, P0.4 (M)
TB2-22 (J)			h	h	h	
TB2-23	+24V	UNUSED	k	k	k	I05, P0.5 (M)
TB2-24	+24V RET		n	n	n	
		UNUSED	r	r	r	I06, P0.6 (M)
			t	t	t	
		UNUSED	v	v	v	I07, P0.7 (M)
			x	x	x	
		UNUSED	M	M	M	I00, P0.0 (C)
			P	P	P	
		UNUSED	S	S	S	I01, P0.1 (C)
			U	U	U	
		GRY	F	F	F	+24V
		BLK	L	L	L	+24V RET
AUXILIARY WYE MONITOR BUS LINE +			H	H	H	LINE +
AUXILIARY WYE MONITOR BUS LINE −			K	K	K	LINE −
			D	D	D	+12V
			B	B	B	+12V RET

P1 J1 P1

GENERATOR #1

M27 BIN, POS 4

GENERATOR #2

M27 BIN, POS 5

P1 J2 P2

M28 BIN POS 3

110 AC NEUTRAL

P2 A B C

P1 D B F L (+12V, +12V RET, +24V, +24V RET)

J1 D B F L (GRY, BLK)

GENERATOR #2 (WEST) CONTROL CABINET

GENERATOR #2 (WEST) MONITOR INTERFACE NRAO DRAWING #C9390028

FROM WYE MONITOR SYSTEM

TB2-1	ENGINE START	GRN	N	N	N	I08, P1.0 (M)
TB2-2		BLK (4)	R	R	R	
TB2-3	ENGINE RUNNING	BLU	T	T	T	I09, P1.1 (M)
TB2-4 (J)		BLK (4)	V	V	V	
TB2-5	BATTERY FAILURE	YEL	X	X	X	I010, P1.2 (M)
TB2-6 (J)		BLK (4)	Z	Z	Z	
TB2-7	OVERCRANK	BRN	b	b	b	I011, P1.3 (M)
TB2-8 (J)		BLK (4)	d	d	d	
TB2-9	FAILURE TO SYNCHRONIZE	ORG	f	f	f	I012, P1.4 (M)
TB2-10 (J)		BLK (4)	j	j	j	
TB2-11	APPROACH LOW LUBE OIL	WHT	m	m	m	I013, P1.5 (M)
TB2-12 (J)		RED (5)	p	p	p	
TB2-13	APPROACH HIGH WATER TEMPERATURE	GRN	s	s	s	I014, P1.6 (M)
TB2-14 (J)		RED (5)	u	u	u	
TB2-15	APPROACH LOAD LIMIT	BLU	w	w	w	I015, P1.7 (M)
TB2-16 (J)		RED (5)	y	y	y	
TB2-17	GENERATOR CIRCUIT BREAKER	RED	W	W	W	I02, P0.2 (M)
TB2-18 (J)		BLK (4)	Y	Y	Y	
TB2-19	REMOTE CIRCUIT BREAKER	WHT	a	a	a	I03, P0.3 (M)
TB2-20 (J)		BLK (4)	c	c	c	
TB2-21		UNUSED	e	e	e	I04, P0.4 (M)
TB2-22 (J)			h	h	h	
TB2-23	+24V	UNUSED	k	k	k	I05, P0.5 (M)
TB2-24	+24V RET		n	n	n	
		UNUSED	r	r	r	I06, P0.6 (M)
			t	t	t	
		UNUSED	v	v	v	I07, P0.7 (M)
			x	x	x	
		UNUSED	M	M	M	I00, P0.0 (C)
			P	P	P	
		UNUSED	S	S	S	I01, P0.1 (C)
			U	U	U	
		GRY	F	F	F	+24V
		BLK	L	L	L	+24V RET
			H	H	H	LINE +
			K	K	K	LINE −
			D	D	D	+12V
			B	B	B	+12V RET

MASTER CUBICLE +24V
MASTER CUBICLE +24V RET
MASTER CUBICLE LINE +
MASTER CUBICLE LINE −
MASTER CUBICLE +12V
MASTER CUBICLE +12V RET

ACAD : 3900W10A

C13900S12 NEXT ASSEMBLY	SCHEMATIC DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES : ANGLES ±
2 PLACE DECIMALS (.XX) ±
3 PLACE DECIMALS (.XXX) ±
4 PLACE DECIMALS (.XX) ±

MATERIAL :

FINISH :

VLA — WYE MONITOR

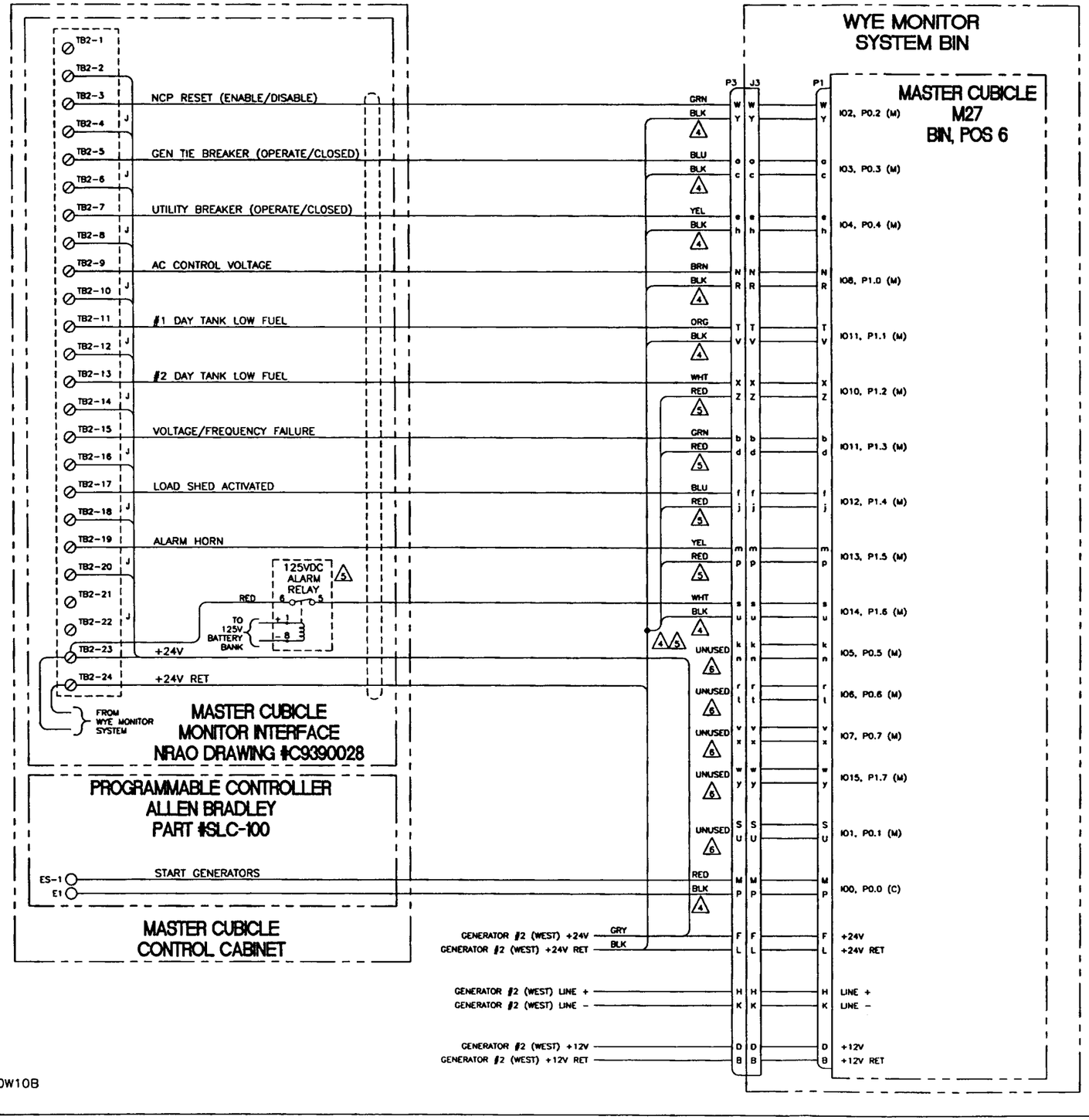
TITLE: WYE MONITOR M27 MODULE TO GENERATOR SYSTEM WIRING DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

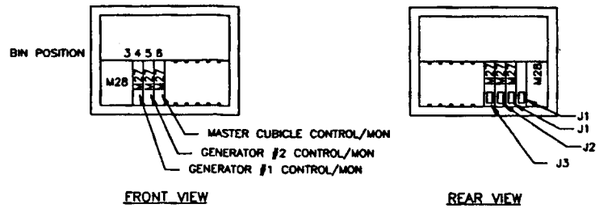
DRAWN BY	DATE 9-94
DESIGNED BY	DATE 9-94
APPROVED BY	DATE 10-94

SHEET NUMBER 1 OF 2 | DRAWING NUMBER D13900W10 | REV. — | SCALE NONE

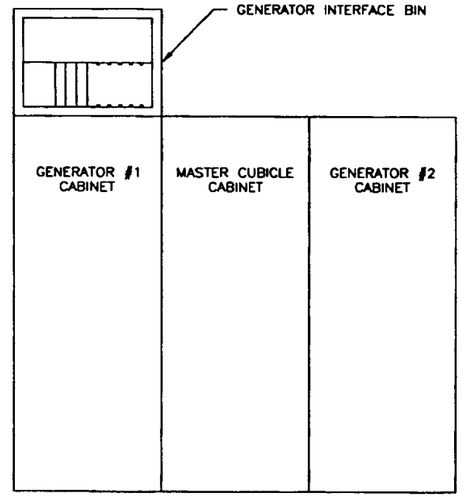
REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION



ACAD : 3900W10B



GENERATOR INTERFACE BIN



GENERATOR CONTROL SYSTEM CABINETS

C13900S12 NEXT ASSEMBLY	SCHEMATIC DWG. TYPE		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MATERIAL :
FINISH :

PROJECT: VLA — WYE MONITOR

TITLE: WYE MONITOR M27 MODULE TO GENERATOR SYSTEM WIRING DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 9-94
DESIGNED BY	DATE 9-94
APPROVED BY	DATE 10-94

SHEET NUMBER 2 of 2 | DRAWING NUMBER D13900W10 | REV. – | SCALE NONE

2.11 M29 Auxiliary Utility Module

This section describes the M29 Auxiliary Utility Module and its interfaces with the Computer and Correlator air conditioning systems and the control ModComp computers. Like the other WYE Monitor control interface modules, M29 uses an Isolated CPU Interface Board to transform serial bus message interactions into 16 discrete paralell interactions with device interface circuitry. The device interface circuitry is installed on a wire-wrapped logic connector board in M29. Drawing D13900P15 is the module assembly drawing and drawing C13900P17 shows the device interface circuit's component layout on the logic connector board. Drawing D13900S07 is the module schematic diagram. Reduced-scale copies of the M29 functional drawings follow this text.

M29 is installed in the VLA Control Room Console, Monitor and Control Bin, location 9 and M28 the Power Supply/Battery Module is installed in locations 10, 11 and 12. M28 provides the 12 volt DC power to M29 and 24 volts to monitor interfaces in the computer and correlator air conditioning system.

M29 is connected to the WYE Monitor Auxiliary Bus that services the Control Building and service buildings complex.

Sections 2.2 and 2.4 described the message formats, protocol, and line driving and receiving. Section 2.8 described the Isolated CPU Interface Board; a slightly different version is used in M29 and is described below.

Figure 5 shows M29's Control Building sub-screen.

The major subjects of this section are the M29 circuitry, the character of the device interface signals, and the interface circuits that adapt these device signals to the Isolated CPU Interface Board.

Monitor signals from the Correlator and Computer air conditioning systems and the ModComp computer's RS-232 signals are connected to M29 via the module's bin rear panel I/O connector. Drawing C13900W03 shows the M29's rear panel signal-pin assignments and drawing C13900W08 shows the connections to the computer and correlator air conditioning system and the ModComp computers.

M29 does not have command outputs but inputs five monitor discretes, two RS-232 serial holdoff signals from the control ModComp computers, and two analog monitor signals. The five monitor discretes are 24 volt level signals. The two RS-232 serial holdoff signals are single characters that are converted to monitor discretes. The two analog signals are AD590 temperature sensor outputs that monitor air temperature in the correlator and computer air conditioning systems. These two analog signals are converted to digital values and read out as monitor data.

One Isolated CPU Interface Board command port (IO3) is used to select the analog monitor mode and three other command ports (IO0, IO1 and IO2) are used to designate the multiplexer address for the M29's analog multiplexer-A/D converter. The analog multiplexer-A/D converter selects the analog signals and converts them to digital values that are parallel-input to the Isolated CPU Interface board. The multiplexer-A/D converter chip has an eight channel capacity; with modifications, the M29 could multiplex and convert an additional six analog signals.

The nature and variety of these monitor inputs make M29 a more complex and specialized module than the M26 and M27. M29 is the only module in the WYE Monitor system that performs analog signal

multiplexing and A/D conversion.

M29 functions as a sort of watch-dog timer in sensing the recurrent RS-232 level, hold-off signals from the two control ModComp computers; however, the ModComp computer reset is indirect in that it is commanded by the VLA telescope operator who is alerted to the loss of the hold-off signal by the VLA PC's Annunciator and Touch-Screen terminal.

In addition to the Isolated CPU Interface Board, M29's circuitry consists of the following functional groups: discretes monitor, RS-232 to discrete conversion, AD590 temperature sensor interface, analog mulitplexer-A/D converter, digital multiplexer to select either analog monitor data or discretes monitor data, and additional power supplies to service the analog functions. These functional groups are described below.

M29 functional drawings are listed below; for convenient reference, reduced-scale copies follow this text.

D13900P15	WYE Monitor M29 Auxiliary Utility Module Assembly
A13900Z03	M29 Auxiliary Utility Module BOM
D13900S07	WYE Monitor M29 Auxiliary Utility Module Schematic Diagram
D13900P16	M29 Auxiliary Utility Isolated CPU Interface Board Assembly
C13900P17	M29 Auxiliary Utility Module Wire-Wrap Board Component Layout
A13900P18	M29 Auxiliary Utility Module Dip Header Assembly
C13900W03	M29 Auxiliary Utility Module Test Points Wiring Diagram
C13900W08	M29 Module Control Building HVAC Interface Wiring Diagram

Front Panel Test Point Connector

For convenience in locally checking the M29's interface signals, internal control discretes, and M29 power, M29 has a front panel test point connector J1 that is a 37 contact, "D" series socket connector. Note from the M29 module schematic drawing that a level-shifted version of all the device monitor interface signals are connected to this test point connector. The signal levels vary as a function of the signal type; the discretes monitor test point signals are TTL levels, the RS-232 test point signals are RS-232 levels, and the AD590 temperature test point signal levels are the outputs of the current-to-voltage conversion amplifiers. Drawing C13900W03 shows the contact-signal assignments.

M29 Isolated CPU Interface Board

The M29 uses Isolated CPU Interface Board D13900P16 — a later version than the D13900P02 used in M26 and M27. This board is functionally identical to the earlier board but has a larger heat sink on the LM7805KC +5 volt regulator because the M29 5 volt power load is larger than the other modules. The signal and power I/O connections are physically identical to the other board. Two NEC PS2501-4 input optoisolator chips are installed on ports IO8 through IO15. These chips have four optoisolators per package but are functionally identical to the NEC PS2501-1 optoisolators. Note from the schematic diagram that the monitor data input to these isolators is the output of the digital multiplexer described below.

M29 Command Interface Circuitry

M29 does not output command discretes but four command optoisolators (NEC PS2502-1) are installed in the Isolated CPU Interface Board ports P0.0 through P0.3. These optoisolators use 1 kΩ pull-up resistors to VCC. Monitor optoisolators are not installed on these ports. As noted above, these four command ports do not control external device circuitry; they function as an analog/digital monitor readout selector discrete and an analog multiplexer address.

M29 Address Inputs

The M29 address line (Unit ID) inputs are encoded to enable the module's Isolated CPU Interface board to determine if the module is the target of a Command or Monitor Request messages. It also uses the encoded value in formatting Command or Monitor Acknowledge messages transmitted to the control PC. The M29 address line inputs are **active-high** and the code is formed by connecting the appropriate address line inputs to logic common (J1-FF) on the J1, the bin back-plane connector. The encoded value is the binary equivalent of the address code; M29's address code is 1. The bin contacts connected to ground are the complement of the address code. J1-DD is the LSB (2^0) and J1-z (2^4) is the MSB. J-1AA (2^5) is always connected to logic common in the address line ground string.

Discretes Monitor Interface Circuitry

Seven channels of discrete monitor signals are input through NEC PS2501-4 optoisolators installed on the logic connector board. Five of these signals are 24-volt level discretes from the computer and correlator handling systems and the other two are discretes from the two RS-232 interfaces, described below.

The seven outputs of the optoisolators are connected to seven inputs of a 74HC244 octal buffer chip (at location AA23) that is a part of the digital multiplexer. The digital multiplexer is described below.

Since the NEC PS2501-4 chips have four optoisolator channels, an additional channel is available in the chip at AA23. This spare channel is not shown on the schematic diagram, but its output transistor's collector is connected to pin 17 of the 74HC244 octal buffer in location AA23. The output transistor's emitter is connected to emitters of the seven other optoisolators in the circuit. The spare channel's LED anode and cathode are floating and with wiring modifications, they could be connected to another discrete monitor input.

The five 24-volt discretes consist of two types of circuits - voltage inputs and contact closure inputs. The voltage inputs are the CHILLER HOT, CHILLER COLD, and CONDENSER HOT signals. The contact closure inputs are the COMPUTER AIR and CORRELATOR AIR signals. In both types of circuits, a 10 kΩ series current limiting resistor limits the LED current to about 2.2 mA.

The voltage input ciruits use the +24 volt output of M28, which is connected to the input contacts of three NO contact pairs in the chiller-condenser circuitry. When a contact pair is closed, the +24 volt level is connected to the optoisolator LED anode through the 10 kΩ limiting resistor; this forces the optoisolator's transistor collector to a logic low or 1. (Remember that the Isolated CPU Interface Board's parallel inputs and outputs are active-low.) When the contacts are open, there is no current into the LED so the output transistor collector is a logic high or 0. Even though the optoisolator LED cathodes are

connected to the 24 volt return, the three set of circuits are connected to the three voltage sources by three pairs of wires via the following P1 pins: P1-f/P1-j; P1-m/P1-p and P1-s/P1-u.

In the contact closure circuits, the optoisolator LED current source is +24 volts through the 10 kΩ current limiting resistors RP4C and RP4D. When either set of contacts is closed, current flows through the LED and makes the transistor collector a logic low or 1. When the contacts are open, no LED current flows so the transistor collector is high or a 0. The contact circuits are connected to the two AIR switches by two pairs of wires via P1 pins: P1-X/P1-Z and P1-b/P1-d.

The discretes signal functions are tabulated at the end of this section.

RS-232 Interface

The two RS-232 interface circuits consist of a polarity detector, optoisolator, and a digital delay circuit. The digital delay circuit outputs drive two monitor optoisolators (AA49 and AA47) described above.

This interface circuit functions in a manner similar to a watch-dog timer. If the holdoff signal recurs within the time-out period, the alarm is not set and the timer is reset to zero. If the holdoff disappears or exceeds the time-out period, the alarm is set. In this circuit, the time-out period is about 42 seconds.

The holdoff signal is a single serial character on the RS-232 lines from the computers. The holdoff character recurrence rate is about 9.6 seconds. The character may be any possible symbol; the interface circuit is not particular.

RS-232 signals are bipolar, swinging between negative and positive levels relative to the signal return line. In the quiescent period (MARK) between character transmissions, the signal is more negative than -3 volts. The first bit in a character is the Start bit which is more positive than +3 volts. Serial bit logic 0's are positive polarity and logic 1's are negative polarity. The RS-232 lines from the ModComps are active-positive only when the computers are outputting the holdoff character; otherwise they are quiescent-negative. See the serial byte format in Figure 14.

The RS-232 specifications require that the minimum receive threshold be ±3 volts; the RS-232 interface must detect the holdoff character with a signal span as small as -3 to +3 volts.

From the above, it is clear that the RS-232 interface must respond to the ≥+3 volt Start bit and initiate a time-out period. If the Start bit does not reappear within the time-out period, an alarm level must be input to the associated monitor optoisolator.

Referring to the schematic diagram, the negative portions of the RS-232 signals are clipped. When the signal is negative, the input 1N4148 diode is forward biased and conducts a small current through the 10 kΩ limiting resistor. This limits the voltage across the optoisolator LED to about 0.6 volts. In this condition, the LED is back biased and does not conduct. The optoisolator output transistor is an emitter-follower circuit with a 10 kΩ emitter resistor. Since the LED does not conduct during negative inputs, the output transistor is cut off and the emitter is near ground. In this condition, the 4060 Reset input current is less than 20 μA so the drop across the 10 kΩ emitter resistor is less than 200 mV, below the CMOS 4060 Reset input V_{IL}, +1.0 volts. The 4060 is reset when the input exceeds V_{IH}, about +3.5 volts;

therefore, for negative RS-232 signal inputs, the 4060 is free to count the oscillator clock pulses.

If the RS-232 signal remains quiescent-negative, the 4060 Q12 stage goes high at 2048 counts of the oscillator signal; this forces the OSCIN pin high via the 1N4148 diode. The high on OSCIN disables the oscillator and stops the counter with Q12 static high. The Q12 high state (about +4.7 volts) drives the associated discretes monitor optoisolator LED through the 3.3 kΩ resistor. The LED current is about 4.5 mA.

When the RS-232 signal is positive, the 4060 Reset input is high, ≥+3.5 volts so the counter is reset to the zero state. When the signal reverts to the negative polarity, the oscillator starts and the counter advances from the zero state. If data bits in the holdoff character are also positive-polarity, they also reset the counter, which is not important. The Stop bit at the end of the character is negative; therefore the counter is free to count out the time-out count of 42 seconds.

The 4060 oscillator frequency is determined by the resistor connected to OSOUT1 and capacitor connected to OSOUT2. These are 47 KΩ and 0.22 μF respectively, and the frequency is determined by $f \approx 1/3RC$. Using these nominal values, the calculated frequency is about 42 Hz. M29 bench tests show an oscillator frequency of about 49 Hz; the difference is probably the result of the use of wide tolerance components.

AD590 Interface

The two analog temperature signals input to M29 are the outputs of AD590 two-terminal, temperature transducers in the heat pump refrigeration system that cools the correlator and computers in the Control Building. One transducer measures the temperature of the warm water coming out of the water-cooled condenser heat exchanger on the hot side of the refrigeration system. The other measures the temperature of the chilled water on the cold side of the refrigeration system.

For supply voltages between +4 and +30 volts DC, the AD590 acts as a high impedance, constant current regulator passing 1μA/°K. During manufacture, the chip is trimmed to calibrate the transducer to 298.2 μA output at 298.2K (+25°C).

The AD590 is particularly useful in remote sensing applications because it is insensitive to voltage drops over long lines since it is a high impedance, low current device. Secondly, the AD590 dissipates very little power, 1.5 mW @5V @ +25°C.

The AD590 interface circuits transform the AD590 currents to voltages and have gain and offset adjustments. The circuit is a simple inverting operational amplifier using the Precision Monolithics OP-15. The AD590 sinks current from the amplifier's summing junction (the minus input) to the -5V supply. This current is a linear function of the temperature sensed by the AD590. The OP-15 output, a positive voltage, feeds back a current to the summing junction so as to null the summing junction currents. The gain is determined by the feedback resistor 50 kΩ. This value requires that the output voltage change 50 mV in response to a 1 μA change in the AD590's current (i.e. 50mV/50kΩ = 1 μA). Therefore the amplifier's scaling is 50 mV/°C. The amplifier's gain is trimmed by the 2 kΩ potentiometer and the 298.2 μA offset current is trimmed by a current from the +5.120 volt supply through the 22.6 kΩ resistor and 1 kΩ trimming potentiometer.

The AD590 interface circuit was designed to cover the -51.2°C to +51.2°C temperature range; the corresponding AD590 current change is 102.4 μA. The AD590 interface circuit's gain and offset potentiometers are adjusted to make the amplifier's output voltage span 0 volts to +5.120 volts for this temperature range.

With the 50 kΩ feedback resistor, an AD590 current change of 102.4 μA will produce a 5.120 volt change in the amplifier output, which is the input voltage range of the ADC0808. An offset current of 273.15 μA will produce an amplifier output of +2.560 volts when the AD590 is passing a current of 273.15 μA, which corresponds to a temperature of 0°C. The A/D's 8-bit output has 256 possible states and the amplifier's voltage span is 5.120 volts; therefore, the A/D's voltage resolution is 20 mV/LSB. +2.560 volts is the mid-point of the ADC0808 range. With this output, the feedback current is 51.2 μA and the AD590 is sinking 273.15 μA; therefore, the offset current must be 221.95 μA. The offset current source is the +5.120 volt supply so the offset resistance must be 23068 Ω. When the gain and offset resistances are set to produce these values, the AD590 temperature range is -51.2°C to +51.2°C, which produces an ADC0808 output span of 0 to 256 counts straight binary code. The amplifier-A/D converter system temperature resolution is 102.4°/256 or 0.40°C/LSB.

The two temperature interface amplifier outputs are input to mulitplexer inputs IN0 and IN1 in the National Semiconductor ADC0808 multiplexer-A/D converter described below.

Section 2.14 describes the adjustment of the M29's AD590 interface circuit gain and offset potentiometers.

The 0.1 μF capacitor across the feedback resistor reduces the gain of the amplifiers to quickly changing signals. Typically, this is normal-mode noise that might be induced in the long cable run to the AD590 temperature sensors.

For temperature stability, the OP-15's + inputs are connected to analog ground through a 16 kΩ resistor.

An AD590 data sheet is included in Section 5.

Analog Multiplexing and A/D Conversion

The two analog voltages from the AD590 Temperature Transducer Circuitry described above are converted to digital values for readout to the control PC via a Monitor Acknowledge message.

This circuitry consists of a National Semiconductor ADC0808, 8-bit A/D converter with an 8-channel analog multiplexer, an Intersil 7555 clock, and an AMD PALCE22V10Z-25 (Programmable Array Logic) chip. The converter's analog multiplexer selects one of the temperature interface circuit outputs on mulitplexer inputs IN0 or IN1 as a function of the PAL's 3-bit address output, MUX1, MUX2, and MUX4. The PAL generates sequencing terms that cause the A/D converter to convert the selected signal to a digital value. The PAL inputs are the 7555 clock, the A/D end of conversion signal, EOC, the analog/digital mode discrete, DISCRETE and the analog multiplexer address bits ANA1, ANA2 and ANA3 (described below). The PAL chip and the programmed logic functions are described below.

The PC control program determines the M29 data readout mode. Refer to the message format description in Section 2.2. Four command message argument bits determine the character of the data read

out by subsequent Monitor Acknowledge Messages; the bit states remain static in the port 0 outputs until changed by a new M29 command message. Bit A_3 (ANALOG*) in port P0.3 controls the analog/digital mode. If A_3 is low (1), the analog signal specified by the multiplexer address is selected for A/D conversion and readout. Conversely, if A_3 is high (0), the discretes monitor data is read out during the next Monitor Acknowledge Message. In this case, the state of the three multiplexer address bits have no significance.

Message argument bits A_0, A_1, and A_2 are the three analog multiplexer address bits stored in ports P0.0, P0.1 and P0.2. On the logic schematic drawing, the mode control and address outputs from the port's output optoisolators are designated P03*, P00*, P01*, and P02*, respectively.

Although the A/D converter could be made to operate continuously by connecting the EOC to the START input, in the M29 application the conversion sequence is controlled by state transitions in the control PAL. The PAL state transitions are described below. Briefly, an A/D conversion is triggered by a commanded transition to the analog mode from the discrete mode or when the multiplex address is changed while in the analog mode. After the conversion, the converted digital value remains in the converter's output latches. If the analog mode continues unchanged and the multiplex address is not changed, there are no additional conversions and this one converted value will continue to be read out by all subsequent Monitor Acknowledge messages. In the analog mode, a new commanded multiplex address will initiate a conversion and the resultant converted value will remain static in the converter's output latches until a new conversion is commanded.

The National Semiconductor ADC0808 is a CMOS analog multiplexer-A/D converter chip. It features an 8-channel single-ended multiplexer, 8-bit successive-approximation conversion, low temperature sensitivity, long term stability, and the absolute accuracy is ± ½ LSB at 25° C. External gain and zero adjustments are not required. The analog signal input range is 0 to +5.100 VDC, typical conversion time is 100 µS with a 640 kHz clock; it is is typically powered by a single +5 volt volt supply, and power consumption is only 15 mW. An external clock is required — typically 640 kHz. The digital inputs and outputs are TTL-compatible, the multiplexer address and digital outputs are latched, and the digital data output is tri-state. Instead of the usual R/2R ladder network, the conversion uses a 256R network because of its inherent monotonicity, which guarantees no missing codes. Secondly, the 256R network does not cause load variations on the reference voltage. The reference voltage applied to the 256R resistor ladder determines the voltage conversion range.

The multiplexer address is latched on the low-to-high transition of the Address Latch Enable (ALE). The successive approximation register is cleared on the rising edge of the Start Conversion signal (START) and the the conversion operation is initiated by the falling edge of START. The End of Conversion (EOC) is clocked low by START and goes high at the end of conversion. Section 5 includes a data sheet for the ADC0808.

The 7555 clock rate is calculated to be 68.6 kHZ using the 7555 data sheet timing formulas and the M29 7555 timing circuit values. The measured clock rate is about 57.8 kHz and frequency discrepancy is probably the result of component tolerances. Although the A/D converter and PAL are capable of operation at a much higher clock rate, the low clock rate was chosen to reduce A/D converter and PAL power consumption. This clock rate increases the conversion time to about 1000 µS, which would be very long in typical data acquisition systems. The long conversion time is not a problem in the WYE Monitor system because the Auxiliary bus M29 polling rate is 2.7 seconds.

The A/D converter reference voltage (REF+) is +5.120 volts from the precision +5.120 volt supply (described below). The converter's REF- input is connected to analog ground AGND. This +5.120 volts is connected across the converter's 256R ladder network and determines the converter's scaling. The converter output has 256 possible states; therefore, the converter's quantization is +5.120/256, 20 mV/LSB.

This reference voltage also powers the converter which can operate with a V_{CC} as high as +6.5 volts. The converter's VREF+ input is connected to +5.120 volts and the VREF- input is connected to analog ground AGND, which is the +/- 15 volt power supply's 0OUT terminal. See the M29 Power Supplies description below.

The A/D converter-AD590 interface circuit's span and resolution were described in the AD590 Interface description above.

The A/D's Output Enable (OE) is connected to V_{CC} so that the latched output data is always available.

The ADC0808 data sheet states that the converter can be made to be self-sequencing by connecting the EOC to the START input; the rising edge of EOC initiates the next conversion. It also states that if this self-sequencing mode is used, an external START pulse should be applied after power is applied to avoid potential logic lock-up. Since there is no external indication of lockup and this state could continue indefinitely, it would be impossible to correct the fault. For this reason the PAL is used as a control sequencer.

The PAL is a programmable digital state machine, and in this implementation, it is controlled by the states of: DISCRETE, the input multiplex address (/ANA1, /ANA2 and /ANA3), the PAL's output mulitplex address (MUX1, MUX2 and MUX4), and the EOC (ADCE).

The PAL state equation's signal name notation differs from that used on the logic schematic. DISCRETE is the ANALOG* signal and the input multiplex address bits /ANA1, /ANA2 and /ANA3 are ANA1*, ANA2* and ANA4*, respectively.

Figure 18 is a simplified rendering of the logic circuitry implemented by the PAL. The AMD PALCE22V10Z-25 is a high speed CMOS programmable logic array (PAL) that can be programmed and erased. The PAL implements the Boolean sum of products and is a set of

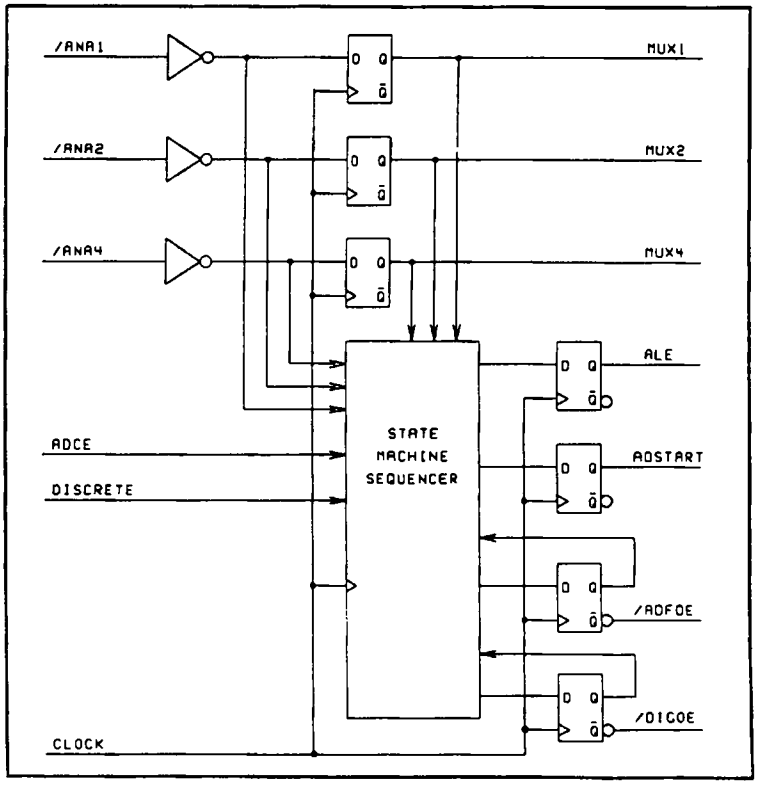


Figure 18 M29 PAL Logic Implementation

programmable AND arrays that drive fixed OR arrays. The AND arrays are programmed to create custom product terms, while the OR array sums selected terms at the outputs. The product terms are connected to the fixed OR's with a varied distribution of 8 to 16 AND output to the 10 OR inputs. The OR sums feed an output macrocell. Each macrocell can be programmed as registered ("D" flip-flop) or combinatorial, and active high or low outputs. The PAL has 12 inputs and 10 output macrocells. Combinatorial or Registered outputs can be fed back to the AND arrays to enable the generation of sequential logic functions. Unused inputs are connected to ground or VCC. The "D" flip-flop is clocked on the low-to-high transistion of the clock input. This PAL can be asynchronously cleared and synchronously preset for initialization. Refer to the block diagram in the PAL data sheet in Section 5.

In the M29 application, six logic inputs are used to form seven registered outputs that control the A/D conversion and digital multiplexer steering. State transitions occur only on the rising (positive-going) edge of the CLOCK which sets or resets the register flip-flops. Since the registers are clocked, each state transition has the clock period delay. The PAL equations and the PAL state transition diagram show that these seven terms are static until changed by a new command from the control PC program.

Referring to Figure 18, the low-true A/D converter multiplex address bits ANA1*, ANA2* and ANA3* are programmed to registered, active-high MUX1, MUX2 and MUX4 for the A/D converter's address inputs. The digital/analog mode select term DISCRETE is programmed to produce two low-true, digital multiplexer control terms — /ADOE and /DIGOE. These outputs are also fed back into the PAL inputs. The digital multiplexer is described below. ADCE, the A/D converter's end-of-conversion output, indicates that the conversion has been completed and the data is available in the output latches.

The PAL outputs do the following: The rising edge of the ALE output clocks the A/D converter's multiplex address bits MUX1, MUX2, and MUX4 into the converter's address latches. The rising edge of the ADSTART output initiates the A/D conversion sequence. /DIGOE and /ADOE control the digital multiplexer.

The /DIGOE and /ADOE states are a function of the three address inputs, /ANA1, /ANA2 and /ANA4, DISCRETE, ADCE, and the /DIGOE and /ADOE feedback terms. See the PAL state and conditional equations below.

Although /ADOE and /DIGOE are in a sense complementary; when either is active-low, the other is inactive. These terms are active-low only when the associated data is to be asserted onto the Isolated CPU Interface Board IO8 through IO15 inputs. When /ADOE is low, the A/D converter's digital data drives the Isolated CPU Interface Board inputs IO8 through IO15. When /DIGOE is low, the discretesmonitor data drives IO8 through IO15.

Figure 19 (next page) is the PAL A/D converter state sequence diagram; the diagram shows all possible states and the transition paths between states. The upper line of text in each state is the state name and the lower line is the name of the associated signal that is activated upon entry to the state. The six states are: DIG_OUT, PRESTART, START_A/D, A/D_BEGIN_WAIT, A/D_END_WAIT, and AD_OUT. The rules for the transitions are described in the state transition description below. All transitions are initiated by the rising edge of CLOCK; it has been omitted from the diagram for simplicity.

Note that when DISCRETE is true (high), there are no transitions out of the DIG_OUT state. When DISCRETE becomes false (low), it forces a transition to the sucessive A/D conversion states ending in the AD_OUT state. The PAL remains in this state until changed by an analog mode command with

a different multiplexer address; this initiates a new conversion sequence via the PRESTART state. When DISCRETE is commanded true, it forces a transition from any state to the DIG_OUT state.

ALE is output to the A/D to latch MUX1, MUX2 and MUX4 into the A/D address latches in the PRESTART state. The ADSTART signal is issued to the A/D converter in the START_AD state. Since the A/D conversion sequence is much larger than the CLOCK period, a wait condition is necessary. The BEGIN_WAIT state is the start of the wait period and the END_WAIT state terminates the wait period when the ADCE becomes true.

State and condition equations use the following notation: "and", "then", "otherwise", "or else" and "XOR" are logical operators and "/" denotes the negation of the signal. Commas are used for readability and have no logical function.

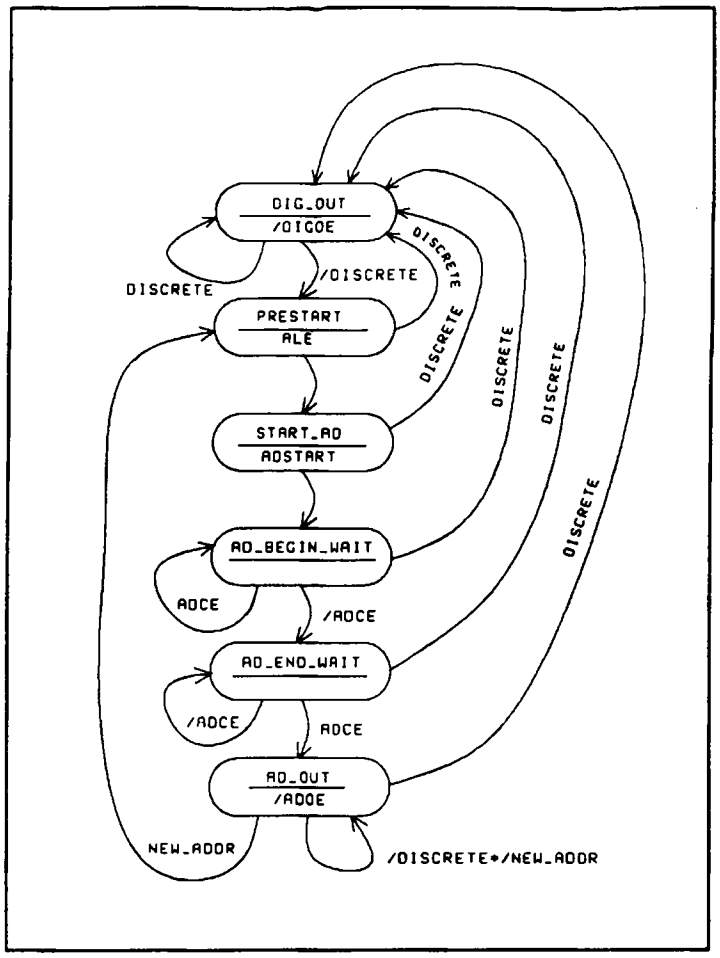


Figure 19 M29 PAL State Diagram

Three Condition equations are also used in the state transition equations. The first one is:
NEW_ADDRO = /DISCRETE and /DIGOE, or else /DISCRETE and (MUX1 XOR ANA1), or else (MUX2 XOR ANA2), or else (MUX4 XOR ANA4). This equation forces the transition to the analog mode from the digital mode or forces a new conversion sequence if the address is changed. The second one is: GO_CET = /DISCRETE and ADCE. The third is: GO_CEF = /DISCRETE and /ADCE. The second and third condition equations are terms used in the state transition equations.

The state equations are:

Assert discrete bits to cpu:
DIG_OUT: if /DISCRETE then PRESTART, otherwise DIG_OUT

Latch mux address in A/D:
PRESTART: if DISCRETE then DIG_OUT, otherwise START_AD

Send START pulse to A/D:
START_AD: if DISCRETE then DIG_OUT, otherwise AD_BEGIN_WAIT

Wait for EOC to go false:
AD_BEGIN_WAIT: if DISCRETE then DIG_OUT,
or else GO_CET, then AD_BEGIN_WAIT,
or else GO_CEF, then AD_END_WAIT

Wait for EOC to go true:
AD_END_WAIT: if DISCRETE then DIG_OUT,
or else GO_CEF, then A/D_END_WAIT,
or else GO_CET, then AD_OUT

Assert A/D conversion value to Isolated CPU Interface ports:
AD_OUT: if DISCRETE then DIG_OUT,
or else NEW-ADDRO, then PRESTART,
otherwise, AD_OUT

Note the correspondence of the state diagram to these equations.

A data sheet for the AMD PALCE22V10Z-25 PAL is included in Section 5.

7555 Clock

The Intersil 7555 is a CMOS version of the 555 timer with lower power dissipation, a higher maximum frequency, and much smaller supply current transients. The 7555 timing equations are identical to those for the 555; refer to the 7555 data sheet in Section 5. The clock frequency is determined by the timing parameters R_A (1 kΩ), R_B (10 kΩ) and C (1000 pF). The clock period T is given by: $T = 0.693(R_A + 2R_B)C$, which is 14.5 μS. The clock frequency is 68,700 Hz.

Digital Multiplexer

The digital multiplexer consists of two 8-bit, tri-state buffers that drive ports IO8 through IO15 on the Isolated CPU Interface Board. PAL output /DIGOE enables the discretes monitor data (described above) onto the Isolated CPU Interface ports IO8 through IO15 via the 74HCT244 (AA23) tri-state bus driver. PAL output /ADOE enables the converted analog value in the A/D converter output register onto these same ports via the 74HCT240 (AA12) tri-state bus drivers. When either term is low, the data on the buffer inputs is asserted on the output tri-state lines. These two signals are generated by the PAL and are, in a sense, logic complements; they were described above. Since the A/D converter output data is high-true, the discretes data are low-true, and the IO8, ... IO15 ports inputs are low-true, the A/D converter tri-state buffer is an inverting buffer, 74HCT240. Note that the discretes buffer (74HCT244) is a non-inverting buffer.

M29 Power Supplies

M29 has three additional power supplies that are required to support the analog and A/D converter functions. The bus driving-receiving supplies cannot be used because they are dedicated to bus line driving and receiving and must be kept isolated from the analog functions.

The module's power input is 12 volts DC from M28, the Power Supply/Battery Module. This powers a Burr-Brown HPR105 dual 15-volt, DC-DC converter that provides + and - 15 volt DC power

for the analog functions. This DC-DC converter was described in Section 2.8.

An LM7905 three-terminal, linear regulator that is powered by the -15 volts from the HPR105 provides a -5 volt current-sinking power for the AD590 temperature transducers described above. Since the AD590's operate with supply voltages between 4 and 30 volts without degradation of their performance, they are not sensitive to their excitation voltage. The LM7905's stability, line and load regulation are not significant factors in the AD590's function.

A precision +5.120 volt, DC power supply is used for the A/D converter's reference input, REF+. The +5.120 volt supply is also used for the converter's V_{CC} because REF+ cannot exceed V_{CC}. Similarly, REF- cannot be more negative than the converter's ground. However, REF+ and REF- can be symmetrically less than V_{CC} and greater than analog ground, respectively. Since the A/D converter is a CMOS chip and operates at a clock rate of 69 kHz, its power consumption is a few milli-Watts, a precision operational amplifier supply is used to supply both voltages. This prevents any possibility that the REF+ could exceed V_{CC}. The converter's V_{CC} supply can be as high as +6.5 volts.

This supply consists of an Analog Devices AD581 High Precision 10V IC reference, a voltage divider, and a Precision Monolithics OP-15 operational amplifier connected as a voltage follower. The AD581 is powered by +15 volts from the HPR105 power supply. The divider potentiometer provides a stable +5.120 voltage that is buffered by the OP-15 voltage follower. The 0.1 μF capacitor on the potentiometer wiper is a noise filter.

The AD581 is a three-terminal, temperature-compensated, monolithic band-gap voltage reference that provides a precise 10.00 volt output from an unregulated input level from 12 to 30 volts. The AD581 (grade L) has an error tolerance of ±5 mV and a voltage temperature coefficient of 5ppm/°C. The AD581's stability is enhanced by its constant load; the voltage follower buffers any load variations that the A/D might impose upon the AD581's output.

As mentioned above, this +5.120 volt level determines the converter's scaling; therefore it should be an accurate stable supply. If it were to drift, the resultant scaling change would not be detectable on the M29 output data. The supply's stability and accuracy are a function of the OP-15 and AD581 characteristics. The AD581's stability and accuracy were mentioned above. The OP-15's power supply rejection ratio is typically 15 μV/V.

M29 Interface Signal Characteristics, Discretes Signals

Int Bd Signal	Function	Signal Type	M29 Module I/O Pins & Levels	Int BD Port State	Signal Function
I000 (C)*	ANA1*	Mux Addr Bit	No Ext I/O		
				Low, 1	True
				High, 0	False
I001 (C)	ANA2*	Mux ADDR Bit	No Ext I/O		
				Low, 1	True
				High, 0	False
I002 (C)	ANA4*	Mux Addr Bit	No Ext I/O		
				Low, 1	True
				High, 0	False

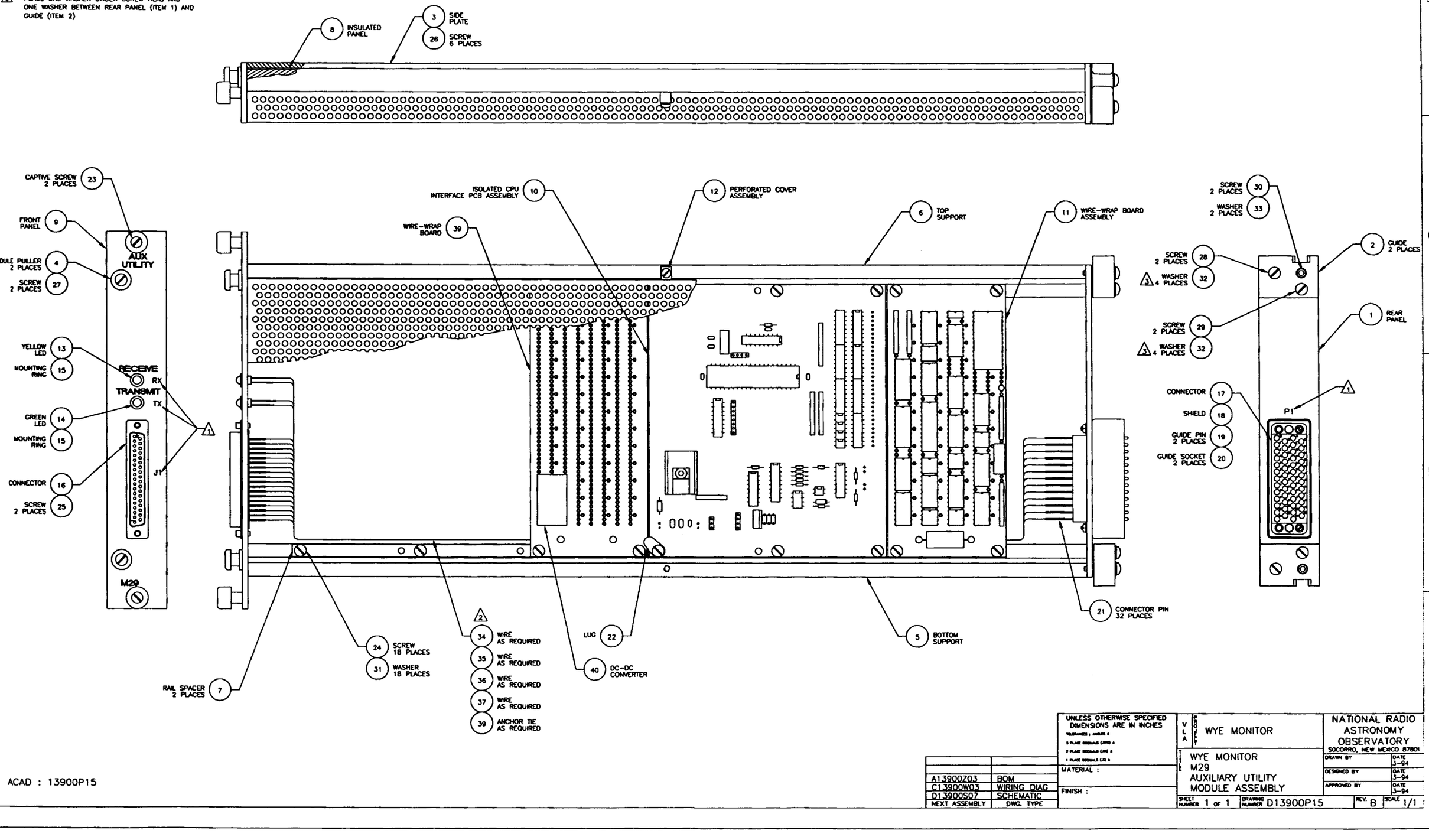
I003	(C)	DISCRETE	Analog/Digital Mode Control	No Ext I/O	Low, 1 High, 0	Discretes Mode Analog Mode
I004	(M)	Not Used				
I005	(M)	Not Used				
I006	(M)	Not Used				
I007	(M)	Not Used				
I008	(M)	ModComp Line 1	RS-232 >±3 volts <±3 volts	P1-N & P1-R	 High, 0 Low, 1	 ModComp OK ModComp Crashed
I009	(M)	ModComp Line 2	RS-232 >±3 volts <±3 volts	P1-T & P1-V	 High, 0 Low, 1	 ModComp OK ModComp Crashed
I010	(M)	Computer Air	Switch Contacts Open Closed	P1-X & P1-Z	 High, 0 Low, 1	 Comp Air OK Comp Air Fault
I011	(M)	Correl Air	Switch Contacts Open Closed	P1-b & P1-d	 High, 0 Low, 1	 Correl Air OK Correl Air Fault
I012	(M)	Chiller Hot Switch	Fault Switch 0 volts 28 volts	P1-f & P1-j	 High, 0 Low, 1	 Chill Hot OK Chill Hot Bad
I013	(M)	Chiller Cold Switch	Fault Switch 0 volts 28 volts	P1-m & P1-p	 High, 0 Low, 1	 Chill Cold OK Chill Cold Bad
I014	(M)	Cond Hot Switch	Fault Switch 0 volts 28 volts	P1-s & P1-u	 High, 0 Low, 1	 Cond Hot OK ConD Hot Bad
I015	(M)	Not Used				

* C denotes a command function and M denotes a monitor function.

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	5-94			MINOR CORRECTIONS
B	11-94			ADD WIRE-WRAP BOARD

NOTES:

1. MARKING SHALL BE .125 HIGH, LEGIBLE, AND PERMANENT. LOCATE ON INSIDE OF MODULE APPROXIMATELY AS SHOWN
2. A WIRING SERVICE LOOP OF SUFFICIENT LENGTH TO ALLOW FRONT AND REAR PANELS TO BE FOLDED FLAT MUST BE PROVIDED
3. PLACE ONE WASHER UNDER SCREW HEAD AND ONE WASHER BETWEEN REAR PANEL (ITEM 1) AND GUIDE (ITEM 2)



ACAD : 13900P15

A13900Z03	BOM
C13900W03	WIRING DIAG
D13900S07	SCHEMATIC
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL :

FINISH :

VLA RESOLUTE

WYE MONITOR

TITLE: WYE MONITOR
M29
AUXILIARY UTILITY
MODULE ASSEMBLY

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 3-94
DESIGNED BY	DATE 3-94
APPROVED BY	DATE 3-94

SHEET NUMBER 1 OF 1 | DRAWING NUMBER D13900P15 | REV. B | SCALE 1/1

BILL OF MATERIAL
NATIONAL RADIO ASTRONOMY OBSERVATORY

X ELECTRICAL X MECHANICAL BOM # A13900Z03 REV B DATE 11-04-94 PAGE 3 OF 4

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
21		AMP	610488-1	PIN, CONNECTOR MN POST	12
22		H.H. SMITH	1411-4	LUG, SOLDER #4	1
23		SOUTHCO	47-10-204-10	SCREW, CAPTIVE	2
24				SCREW, PAN HD, SS, 4-40UNC-2A x .25	18
25				SCREW, SOCK HEAD, SS, 4-40UNC-2A x .38	2
26				SCREW, FLT HD, SS, 6-32UNC-2A x .25	6
27				SCREW, FLT HD, SS, 6-32UNC-2A x .75	2
28				SCREW, PN HD, SS, 6-32UNC-2A x .75	2
29				SCREW, PN HD, SS, 6-32UNC-2A x 1.00	2
30				SCREW, SOCK HD, SS, 6-32UNC-2A x 1.00	2
31				WASHER, #4, LOCK	18
32				WASHER, #6, EXT. TOOTH	8
33				WASHER, #6, LOCK	2
34		ALPHA	7053	WIRE, WHT, #26 GA.	AR
35		ALPHA	7053	WIRE, BLK, #26 GA.	AR
36		ALPHA	7053	WIRE, RED, #26 GA.	AR
37		ALPHA	7053	WIRE, BLU, #26 GA.	AR
38		PANDUIT	TA1S8	TIE, ANCHOR	AR

BILL OF MATERIAL
NATIONAL RADIO ASTRONOMY OBSERVATORY

X ELECTRICAL X MECHANICAL BOM # A13900Z03 REV B DATE 11-04-94 PAGE 4 OF 4

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
39		DATACON	94V-0 OFYF6	BOARD, WIRE-WRAP	1
40		POLYTRON	TW1.8-24S5	CONVERTER, DC-DC, 24 TO 5V	1
41					
42		NRAO	C13900AB08	SILKSCREEN, FRONT PANEL	---
43		NRAO	D13900P15	ASSEMBLY, M29 MODULE	---
44		NRAO	A13900P18	ASSEMBLY, DIP HEADER	---
45		NRAO	D13900S07	SCHEMATIC, M29 MODULE	---
46		NRAO	A13900W03	WIRING DIAGRAM, CONNECTOR	---
47		NRAO	A13900Z03	BOM	---
48					
49					
50					
51					
52					
53					
54					
55					
56					
57					
58					
59					
60					

BILL OF MATERIAL
NATIONAL RADIO ASTRONOMY OBSERVATORY

X ELECTRICAL X MECHANICAL BOM # A13900Z03 REV B DATE 11-04-94 PAGE 2 OF 4
MODULE M29 NAME AUXILIARY UTILITY DWG# D13900P15 SUB ASSY _____ DWG# _____
SCHEM. DWG# D13900807 LOCATION WYE MON QUA/SYS. _____ PREPRD BY K. TATE APPRVD BY A. SITTLER

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
1		NRAO	C13050M10	PANEL, REAR	1
2		NRAO	B13050M04	GUIDE	2
3		NRAO	B13050M06	PLATE, SIDE	2
4		NRAO	C13050M70-1	PULLER, MODULE	2
5		NRAO	C13720M15-1	SUPPORT, BOTTOM	1
6		NRAO	C13720M15-2	SUPPORT, TOP	1
7		NRAO	C13720M17	SPACER, INSULATED RAIL	2
8		NRAO	C13720M49	PANEL, INSULATED SIDE	1
9		NRAO	C13900M04	PANEL, FRONT	1
10		NRAO	D13900P16	PCB, ISOLATED CPU INTERFACE	1
11		NRAO	C13900P17	CIRCUIT BOARD, WIRE-WRAP	1
12		NRAO	C13900P19	ASSY, PERFORATED COVER	1
13	RX			LED, YELLOW	1
14	TX			LED, GREEN	1
15		HEWLETT PACKARD	HLMP-0103	RING, LED MOUNTING	2
16	J1	AMPHENOL	17D-C37S-F179	CONNECTOR, 37-PIN D-SUB	1
17	P1	AMP	201358-3	CONNECTOR, 50-PIN	1
18		AMP	202394-2	SHIELD, CONNECTOR	1
19		AMP	200833-4	PIN, GUIDE	2
20		AMP	203964-6	SOCKET, GUIDE	2

REVISIONS

REV	DATE	DRAWN BY	APPROVED BY	DESCRIPTION
A	6-94			MINOR CORRECTIONS
B	11-94			ADDED ITEMS 39 AND 40

USED ON
NEXT ASSY

APPROVED BY DATE 3-94
DESIGNED BY DATE 3-94
DRAWN BY DATE 3-94

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLA

PROJECT WYE MONITOR
TITLE M29 AUXILIARY UTILITY MODULE BOM
DWG NO. A13900Z03 SHEET 1 OF 4

REV.	DATE	DRAWN BY	APPROV'D BY	DESCRIPTION
A	3-94			REVISED AND REDRAWN
B	6-94			CHG P1-EE - P1-EBC, WATCHDOG

DIGITAL INPUTS

HOSCMP LINE1
HOSCMP LINE1 RET
HOSCMP LINE2
HOSCMP LINE2 RET
COMPUTER AIR SWITCH CLOSED = FAULT
CORRELATOR AIR SWITCH CLOSED = FAULT
CHILLER HOT 28 VOLTS VOLTAGE = FAULT
CHILLER COLD 28 VOLTS VOLTAGE = FAULT
CONDENSER HOT 28 VOLTS VOLTAGE = FAULT

TEMPERATURE CHANNELS

CHILLER TEMP
CONDENSER TEMP
TEMPERATURE PROBE AD590
OFFSET
GAIN

CLOCK

A/D CONVERTER

CONTROL PAL

WATCHDOG RESET

MAX693

POWER CONDITIONING

ISOLATED DC-DC CONVERTER

POWER SUPPLY

+/- 15V SUPPLY

5.120V SUPPLY

-5V SUPPLY

ISOLATED CPU OUTPUTS TO CONTROL PAL

ISOLATED CPU INTERFACE PCB
NRAO DRAWING
#D13900P16

WIRE-WRAP BOARD
NRAO DRAWING
#C13900P17

NOTES:
▲ P1601 (Z1) REPLACES RV1, RV2, AND RV3

C13900W03	WIRE DIAG
D13900P15	ASSEMBLY
NEXT ASSEMBLY	DWG TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX) ±
2 PLACE DECIMALS (.XX) ±
1 PLACE DECIMALS (.X) ±

MATERIAL:
FINISH:

VLA PRODUCT: WYE MONITOR

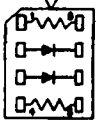
TITLE: WYE MONITOR
M29 AUXILIARY
UTILITY MODULE
SCHEMATIC DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY

DRAWN BY
DESIGNED BY
APPROVED BY

SHEET NUMBER 1 OF 1
DRAWING NUMBER D13900S07
REV B SCALE

ORCAD : 13900S07

	DESCRIPTION	VALUE	MFG.	PART NO.
	DIP HEADER			
	RESISTOR	3.3K, 1/4W, 5%	ALLEN-BRADLEY	RC07GF332J
	DIODE		PHILIPS	1N4148
	DIODE		PHILIPS	1N4148
	RESISTOR	3.3K, 1/4W, 5%	ALLEN-BRADLEY	RC07GF332J

MODULE: M29 AUXILIARY UTILITY

BOARD LOCATION: AC09

DWG NO. A13900P18 | SHEET 2 OF 8 | REV -

REVISIONS

REV	DATE	DRAWN BY	APPVD BY	DESCRIPTION

D13900S07 SCHEMATIC

C13900P17 ASSEMBLY

NEXT ASSY USED ON

DRAWN BY DATE 3-93

DESIGNED BY DATE 3-93

APPROVED BY DATE 3-93

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

VLA

PROJECT WYE MONITOR

TITLE M29 AUXILIARY UTILITY MODULE
DIP HEADER ASSEMBLY

DWG NO. A13900P18 SHEET 1 OF 8

DESCRIPTION	VALUE	MFG.	PART NO.
DIP HEADER			
RESISTOR	22.6K,1/8W,1%	DALE	RN55D2262F
TRIM POT	1K	BOURNS	3262W-102
TRIM POT	2K	BOURNS	3262W-202
RESISTOR	48.7K,1/8W,1%	DALE	RN55D4872F
CAPACITOR	0.1uF		
RESISTOR	16K, 1/8W, 5%	ALLEN-BRADLEY	RC07GF163J

MODULE: M29 AUXILIARY UTILITY

BOARD LOCATION: AC39, AE39

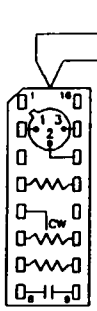
DRAWING NO. A13900P18 SHEET 4 OF 8 REV -

DESCRIPTION	VALUE	MFG.	PART NO.
DIP HEADER			
RESISTOR	10K, 1/4W, 5%	ALLEN-BRADLEY	RC07GF103J
RESISTOR	10K, 1/4W, 5%	ALLEN-BRADLEY	RC07GF103J
RESISTOR	10K, 1/4W, 5%	ALLEN-BRADLEY	RC07GF103J

MODULE: M29 AUXILIARY UTILITY

BOARD LOCATION: AC35

DRAWING NO. A13900P18 SHEET 3 OF 8 REV -

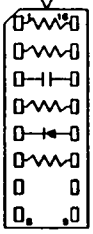


DESCRIPTION	VALUE	MFG.	PART NO.
DIP HEADER			
VOLTAGE REFERENCE	10.000V	ANALOG DEVICES	AD581LH
RESISTOR	4.99K,1/8W,1%	DALE	RN55D4991F
TRIM POT	500 OHM	BOURNS	3260W-1-501
RESISTOR	5.11K,1/8w,1%	DALE	RN55D5111F
CAPACITOR	0.1uF		

DRAWING NO. A13900P18 SHEET 6 OF 8 REV -

MODULE: M29 AUXILIARY UTILTIY

BOARD LOCATION: AG20

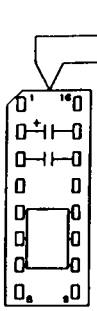


DESCRIPTION	VALUE	MFG.	PART NO.
DIP HEADER			
RESISTOR	8.2K, 18W, 5%	ALLEN-BRADLEY	RC07GF822J
RESISTOR	47K, 1/8W, 5%	ALLEN-BRADELY	RC07GF473J
CAPACITOR	.22uF		
RESISTOR	10K, 1/4W, 5%	ALLEN-BRADLEY	RC07GF103J
DIODE		PHILIPS	1N4148
RESISTOR	10K, 1/4W, 5%	ALLEN-BRADLEY	RC07GF103J

DRAWING NO. A13900P18 SHEET 5 OF 8 REV -

MODULE: M29 AUXILIARY UTILITY

BOARD LOCATION: AE04, AE16



DESCRIPTION	VALUE	MFG.	PART NO.
DIP HEADER			
CAPACITOR	10uF, 16V TANT	SPRAGUE	
CAPACITOR	01.uF		
VOLTAGE REGULATOR	-5V	NATIONAL	LM79M05CP

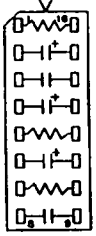
MODULE: M29 AUXILIARY UTILITY

BOARD LOCATION: AG43

DRAWING NO. A13900P18

SHEET 8 OF 8

REV -



DESCRIPTION	VALUE	MFG.	PART NO.
DIP HEADER			
RESISTOR	10,1/8W,5%	ALLEN-BRADLEY	RC07GF100J
CAPACITOR	10uF,35V TANT	MALLORY	TDC-106K035NSF
CAPACITOR	0.1uF		
CAPACITOR	10uF,35V TANT	MALLORY	TDC-106K035NSF
RESISTOR	1K,1/8W,5%	ALLEN-BRADLEY	RC07GF102J
CAPACITOR	10uF,35V TANT	MALLORY	TDC-106K035NSF
RESISTOR	10K,1/8W,5%	ALLEN-BRADLEY	RC07GF103J
CAPACITOR	1000pF	MALLORY	CK05BX102K

MODULE: M29 AUXILIARY UTILITY

BOARD LOCATION: AG34

DRAWING NO. A13900P18

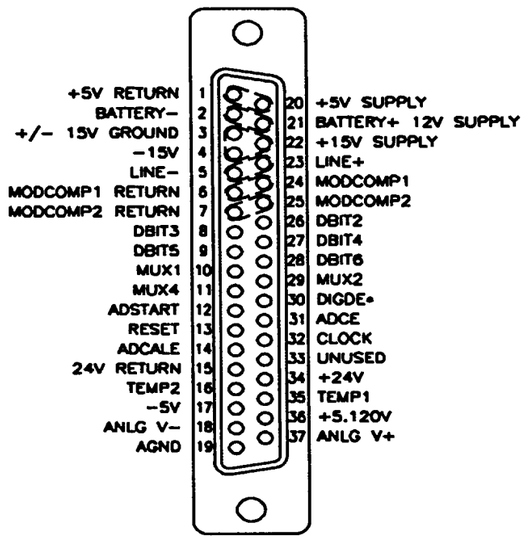
SHEET 7 OF 8

REV -

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

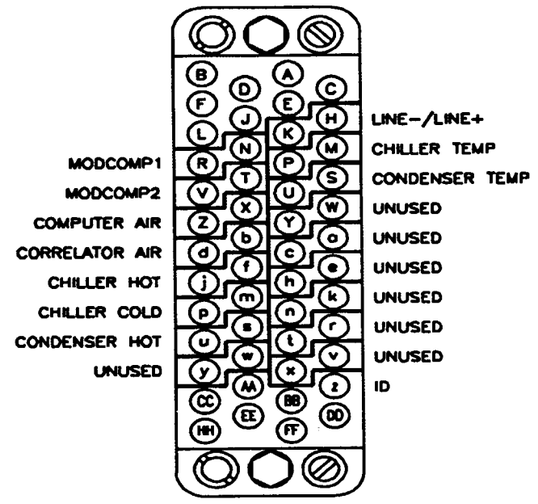
NOTE:

1. — — = GROUP SIGNALS



FRONT PANEL CONNECTOR — J1

VIEWED FROM MODULE FRONT



PIN	FUNCTION	PIN	FUNCTION
A		d	CORRELATOR AIR–
B	GND	e	
C		f	CHILLER HOT+
D	+12 VOLTS	h	
E		j	CHILLER HOT–
F	+24 VOLTS	k	
H	LINE+	m	CHILLER COLD+
J		n	
K	LINE–	p	CHILLER COLD–
L	24V RTN	r	
M	CHILLER TEMP+	s	CONDENSER HOT+
N	MODCOMP1+	t	
P	CHILLER TEMP–	u	CONDENSER HOT–
R	MODCOMP1–	v	
S	CONDENSER TEMP+	w	
T	MODCOMP2+	x	
U	CONDENSER TEMP–	y	
V	MODCOMP2–	z	ID4
W		AA	ID5
X	COMPUTER AIR+	BB	ID2
Y		CC	ID3
Z	COMPUTER AIR–	DD	ID0
a		EE	ID1
b	CORRELATOR AIR+	FF	ID GND
c		HH	ANALOG GND

REAR PANEL CONNECTOR — P1

VIEWED FROM MODULE REAR

ACAD : 13900W03

D13900S07	SCHEMATIC
A13900Z03	BOM
D13900P16	ASSEMBLY
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX) ±
2 PLACE DECIMALS (.XX) ±
1 PLACE DECIMALS (.X) ±

MATERIAL :

FINISH :

VLA

WYE MONITOR

TITLE: M29 AUXILIARY UTILITY MODULE CONNECTOR TEST POINTS WIRING DIAGRAM

SHEET NUMBER 1 OF 1 | DRAWING NUMBER C13900W03 | REV. — | SCALE 2/1

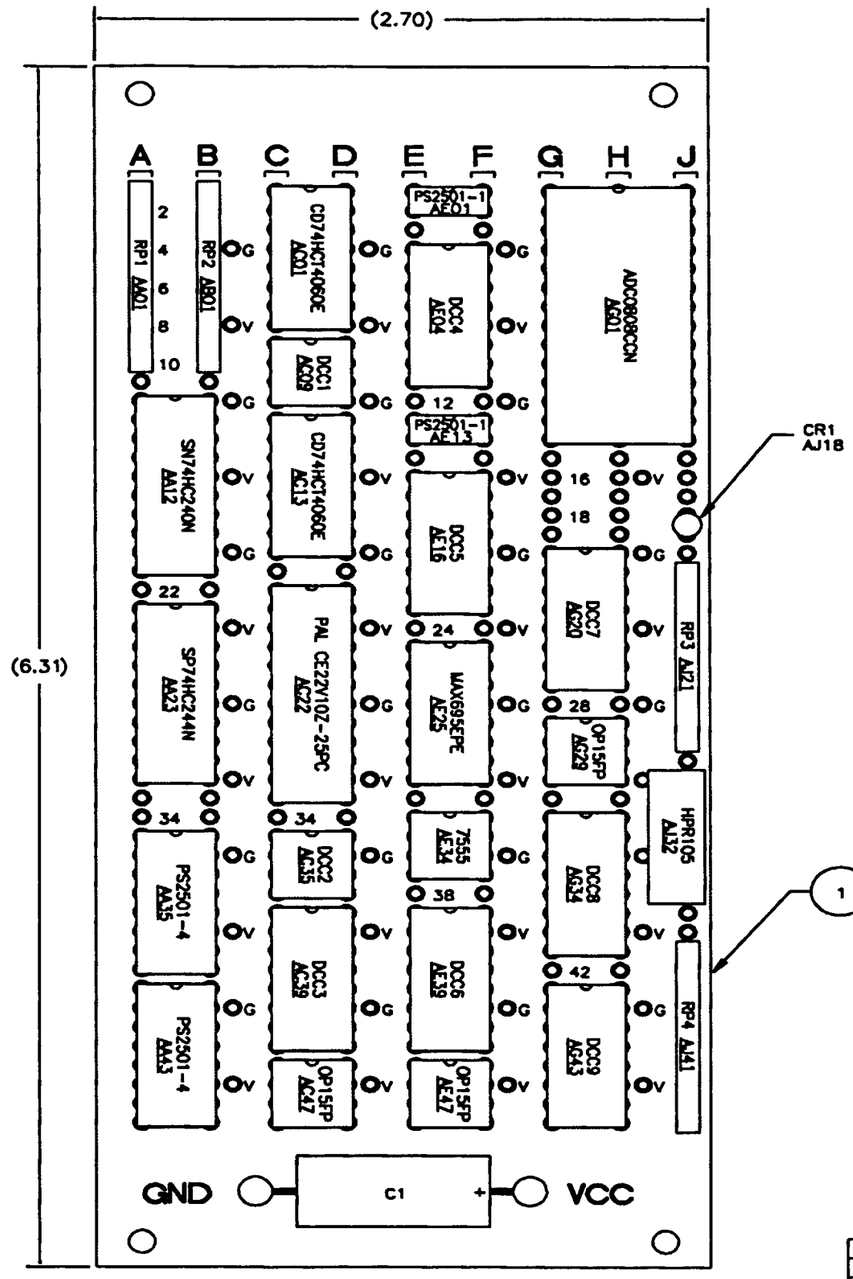
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 3-94
DESIGNED BY	DATE 3-94
APPROVED BY	DATE 3-94

NOTES:

1. INSTALLED ON AUGAT 616-CG1 DIP HEADER.
   REF: DIP HEADER ASSEMBLY, DWG. #A13900P18
2. INSTALLED ON AUGAT 608-CG1 DIP HEADER.
   REF: DIP HEADER ASSEMBLY, DWG. #A13900P18

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION



ACAD : 13900P17

DCC1 AC09 (2)

1	3.3K	8
	1N4148	
	1N4148	
4	3.3K	5

DCC2 AC35 (2)

1	10K	8
	10K	
	10K	
4		5

DCC3 AC39 (1)

1	22.6K	16
	1K	
	1K	
	48.7K	
	0.1uf	
8	16K	9

DCC4 AE04 (1)

1	8.2K	16
	47K	
	.22uf	
	10K	
	1N4148	
	10K	
8		9

DCC5 AE16 (1)

1	8.2K	16
	47K	
	.22uf	
	10K	
	1N4148	
	10K	
8		9

DCC6 AE39 (1)

1	22.6K	16
	1K	
	1K	
	48.7K	
	0.1uf	
8	16K	9

DCC7 AG20 (1)

1		16
	AD581	
	4.99K	
	500	
	5.11K	
8	0.1uf	9

DCC8 AG34 (1)

1	10	16
	10uf	
	0.1uf	
	10uf	
	1K	
	10uf	
	10K	
8	1000pf	9

DCC9 AG43 (1)

1		16
	10uf	
	0.1uf	
	-5V	
8		9

ITEM NO.	REF. DES.	MANUFACTURER	PART NUMBER	DESCRIPTION	QTY
16			HPR105	CONVERTER, POWER	1
15		TI	ADC0808CCN	CONVERTER, A/D	1
14		HARRIS	7555	CLOCK	1
13		MAXIM	MAX695EPE	WATCHDOG, A/D	1
12		PMI	OP15FP	AMPLIFIER, OPERATIONAL	3
11		AMD	PALCE22V10Z-25PC	PAL, CONTROL	1
10		RCA	CD74HCT4060E	COUNTER	2
9		NEC	PS2501-4	OPTOISOLATOR	2
8		NEC	PS2501-1	OPTOISOLATOR	2
7		SPI	SP74HC244N	OCTAL BUFFER/LINE DRIVER	1
6		TI	SN74HC240N	OCTAL BUFFER/LINE DRIVER	1
5	RP2-RP4	BOURNS	4310R-101-103	RESISTOR PACK, 10K	3
4	RP1	BOURNS	4310R-101-102	RESISTOR PACK, 1K	1
3	CR1			LED, RED	1
2	C1	SPRAGUE	TVA 1308	CAPACITOR, 50uf/50V	1
1				BOARD, WIRE-WRAP	1

D13900S07	SCHEMATIC
A13900P18	DIP HEADER
D13900P15	ASSEMBLY
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL :

FINISH :

VLA RADIO OBSERVATORY

WYE MONITOR

TITLE: M29 AUXILIARY UTILITY MODULE WIRE-WRAP BOARD COMPONENT LAYOUT

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

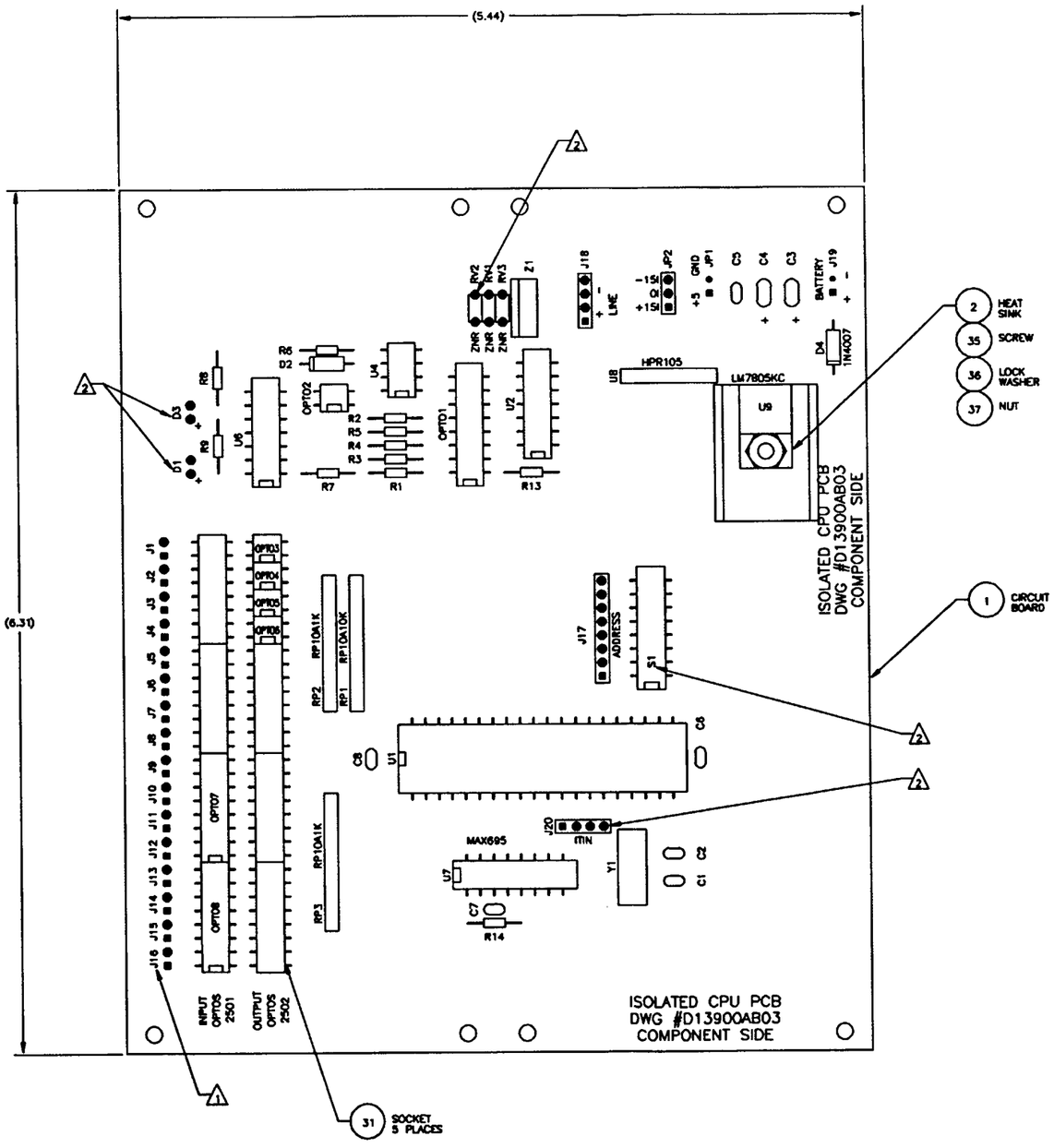
DRAWN BY	DATE 3-94
DESIGNED BY	DATE 3-94
APPROVED BY	DATE 3-94

SHEET NUMBER 1 OF 1 | DRAWING NUMBER C13900P17 | REV. — | SCALE 2/1

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	5-94			CHGD PS2501-1 TO OP15

NOTES:

1. REFERENCE DESIGNATORS JXX AND JPXX = WIRE-WRAP CONNECTIONS. MOUNT WIRE-WRAP PINS ON CIRCUIT SIDE OF PC BOARD
2. NOT INSTALLED



COMPONENT SIDE

ITEM NO.	REF. DES.	MANUFACTURER	PART NUMBER	DESCRIPTION	QTY
37				NUT, HEX-3/16 4-40UNC-2B	1
36				WASHER, LOCK #4	1
35				SCREW, FLAT HEAD, SS, 4-40UNC-2A x .25	1
34	J1-J20, JP1-JP2			PIN, WIRE WRAP	55
33	U1	AMP	2-640379-3	SOCKET, 40-PIN	1
32	U4	AMP	2-640463-3	SOCKET, 8-PIN	1
31	U2, OPT01, OPT04-OPT08	AMP	2-640358-3	SOCKET, 16-PIN	10
30	Z1	TECCOR	P1602	SURGE SUPPRESSOR	1
29	Y1	ECS	ECS-110.5-20-4	CRYSTAL, 11.0592 MHZ	1
28	U9	NATIONAL	LM7805KC	VOLTAGE REGULATOR	1
27	U8	BURR BROWN	HPR105	DC-DC CONVERTER	1
26	U7	MAXIM	MAX695	IC, 16-PIN	1
25	U6	SIGNETICS	74HCT32	IC, 14-PIN	1
24	U4	PMI	OP15	IC, 8-PIN	1
23	U2	SIGNETICS	74HCT00	IC, 14-PIN	1
22	U1	INTEL	87C51FA	IC, 40-PIN	1
21	S1		SW DIP-8	SWITCH	1
20	R14			RESISTOR, 10	1
19	R13			RESISTOR, 150	1
18	R8-R9			RESISTOR, 1K	2
17	R6-R7			RESISTOR, 10K	2
16	R3-R5			RESISTOR, 330K	3
15	R1-R2			RESISTOR, 51K	2
14	RV1-RV3	PANASONIC	ZNR 10K680	SURGE SUPPRESSOR	3
13	RP2-RP3		RP10A1K	RESISTOR PACK, 1K	2
12	RP1		RP10A10K	RESISTOR PACK, 10K	1
11	OPT03-OPT06	NEC	PS2502-1	OPTOISOLATOR	4
10	OPT02	PMI	OP15	OPTOISOLATOR	1
9	OPT01, OPT07-OPT08	NEC	PS2501-4	OPTOISOLATOR	3
8	D4		1N4007	DIODE	1
7	D2		1N914	DIODE	1
6	D1, D3			LED	2
5	C5-C8			CAPACITOR, 0.1uf	4
4	C3, C4			CAPACITOR, 10uf	2
3	C1, C2			CAPACITOR, 33pf	2
2		NRAO	B13720M25	HEAT SINK	1
1		NRAO	D13900AB03	CIRCUIT BOARD	1

D13900S07	SCHEMATIC
D13900M03	DRILL DWG
D13900AB06	SOLDER MASK
D13900AB05	SILKSCREEN
D13900P15	ASSEMBLY
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL :

FINISH :

VLA PROJECT: WYE MONITOR

TITLE: M29 AUXILIARY UTILITY ISOLATED CPU INTERFACE BOARD ASSY

NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801

DRAWN BY — DATE 3-94

DESIGNED BY — DATE 9-92

APPROVED BY — DATE 3-94

SHEET NUMBER 1 OF 1 | DRAWING NUMBER D13900P16 | REV. A | SCALE 2/1

ACAD : 13900P16

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

NOTES:
1. LOCATED UNDER OPERATOR ROOM FLOOR NEXT TO COMPUTER AIR FLOW SWITCH

BLUE STRIPED BELDEN 9501

SMALL JUNCTION BOX ABOVE HVAC CONTROLS IN MACHINE ROOM

BELDEN 9508

AD590
- RED
- BLACK
- N/C

AD590
- RED
- BLACK
- N/C

BELDEN 9501

TB4-1	PAIR #1 RED	CHILLER TEMPERATURE +	M
TB4-2	BLACK	–	P
TB4-3	PAIR #2 WHITE	CONDENSER TEMPERATURE +	S
TB4-4	BLACK	–	U
TB1-7	PAIR #3 GREEN	CHILLER HOT +28V	f
TB1-5	BLACK	RTN	j
TB1-4	PAIR #4 BLUE	CHILLER COLD +28V	m
TB1-2	BLACK	RTN	p
TB2-7	PAIR #5 YELLOW	CONDENSER HOT +28V	s
TB2-5	BLACK	RTN	u
TB4-9	PAIR #6 BROWN	SPARE	
TB4-10	BLACK		
TB4-11	PAIR #7 ORANGE	SPARE	
TB4-12	BLACK		
TB4-13	PAIR #8 WHITE	28VDC +	
TB4-14	RED	RTN	

9-J1
REAR OF BIN IN OPERATORS CONSOLE POSITION 9 AT M29B

B
D
F
L
X
Z
b
d

WHITE +28V
RED +28V RTN
BLACK GND
BLUE +12V

10-J1
REAR OF BIN IN OPERATORS CONSOLE POSITION 10 AT M28

F L B D

COMPUTER AIR FLOW

STRIPED BELDEN 9501
- RED
- BLACK
- SHIELD

CORRELATOR AIR FLOW

BELDEN 9501

1 RED
2 BLACK
3 SHIELD

1 MOLEX CONNECTOR 03-06-1032 WITH MALE (PINS) 02-06-2132

MOLEX CONNECTOR 1 03-06-2032 WITH FEMALE (SOCKETS) 02-06-1132

CHASSIS AT BIN IN OPERATOR CONSOLE

12-J2
REAR OF BIN IN OPERATORS CONSOLE POSITION 12 AT M28
MS3120A14S-1P

TO UPS UNDER FLOOR
- HOT
- NEUTRAL
- GND

A B C / A B C

MS3106A14S-1S

ACAD : 13900W08

C13900W03	WIRING DIAG
D13900S07	SCHEMATIC
D13900P15	ASSEMBLY
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES : ANGLES ±
3 PLACE DECIMALS (.XXX) ±
2 PLACE DECIMALS (.XX) ±
1 PLACE DECIMALS (.X) ±

MATERIAL :

FINISH :

VLA SOCORRO, NM

WYE MONITOR

TITLE
WYE MONITOR
M29 MODULE-CONTROL BLDG
HVAC INTERFACE
WIRING DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 7-94
DESIGNED BY	DATE 7-94
APPROVED BY	DATE 7-94

SHEET NUMBER 1 OF 1 | DRAWING NUMBER C13900W08 | REV. – | SCALE NONE

2.12 M28 Power Supply/Battery Module

M28 is a dual-voltage, DC power supply with backup batteries that is used to power the M27 and M29 modules. In normal operation, the power supply provides DC power to the M27 and M29 modules and maintains a charge on the batteries. In the event of an AC power failure, the batteries provide operating power to the M27's and M29.

The Panasonic LCR 12V1.3P batteries are lead-acid, have a long service life, are maintenance free, do not generate corrosive gases during normal use, are sealed and guaranteed not to leak, and can be used in any physical orientation.

The M28 drawings are listed below; for convenient reference, reduced-scale copies are found at the end of this text.

```
D13900P08       WYE Monitor M28 Power Supply/Battery Module Assembly
C13900S10       M28 Power Supply/Battery Schematic Diagram
A13900Z02       M28 Power Supply/Battery Module BOM
```

Refer to the schematic diagram. The M28 uses two Lambda VS10-15 switching power supplies cascade-connected to provide both 27 and 13.5 volt DC outputs. The 13.5 volt and 27 volt outputs have a common return. The 13.5 volt output powers the M27 and M29 modules and the 27 volt output is used to power DC relays in the M27 and remote equipment. 1N4007 diodes on the output of the power supplies isolate the batteries from the power supplies when the AC power is off. Internal 1 ampere fuses prevent damage to the power supplies in the event of a short-failure of the batteries.

A front panel LED indicates the presence of the 27 volt output and two front panel test jacks permit measurement of the 27 volt output.

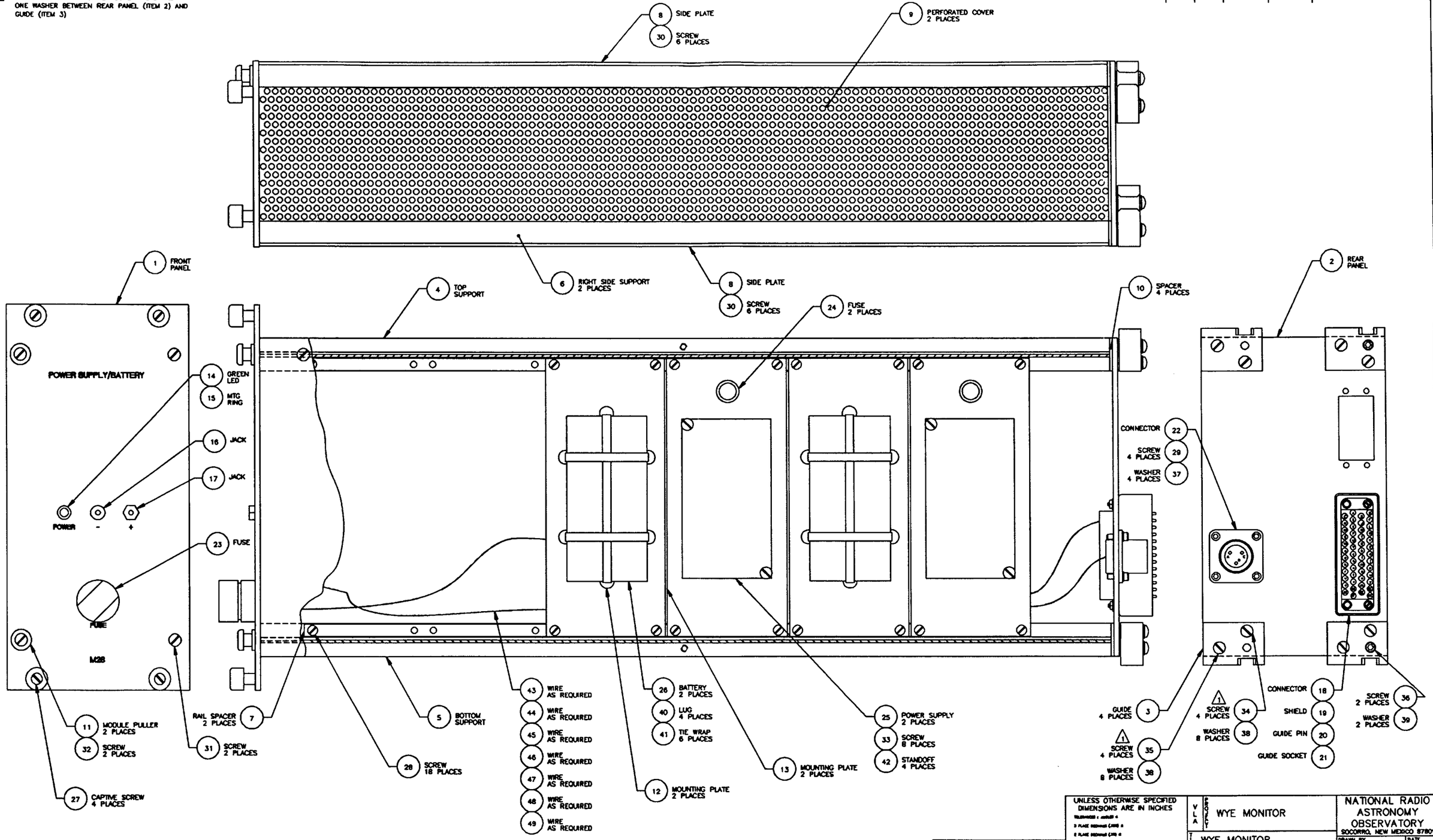
The Lambda VS10-15 output current capacity is 0.7 Amps at an output voltage of 15 volts. The DC output may be adjusted over 10 to 15 volts by an output voltage adjustment potentiometer; this is set to 13.7 VDC for M28. AC input and DC outputs are connected via Molex-type connectors. Line and load regulation are 0.4% and 0.8%, respectively. Peak-to-peak ripple and noise is rated at 150 mV. The output has current limit and overvoltage protection. Typical efficiency is 72%. Isolation of the DC outputs is 500 volts to frame ground. The power supplies are mounted on a metal component plate which serves as a heat sink. A VS10 power supply data sheet is included in Section 5.

The Panasonic LCR 12V1.3P has a 12 volt output and a 1.3 ampere-hour capacity. In the event of loss of AC power, the M28 will power one M29 for 3.5 hours, two M27s for 5.0 hours, and three M27s for 3.3 hours. These values are based upon measurements of power demand and take into account the transmission duty cyle of the M27 and M29 modules on the Auxiliary bus and a 60% discharge limit for the batteries. Refer to the Panasonic battery data sheets in Section 5. Note that the batterie's Cyclic life vs Depth of Discharge curves show a marked reduction in cycle life as the depth of discharge increases. A 60% discharge depth was chosen for these operating time calculations. While it is obviously difficult to set strict M28 battery check guidelines, maintenance personnel should periodically check the M28 batteries.

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

NOTES:

1. PLACE ONE WASHER UNDER SCREW HEAD AND ONE WASHER BETWEEN REAR PANEL (ITEM 2) AND GUIDE (ITEM 3)



ACAD : 13900P08

A13900Z02	BOM
C13900S10	SCHEMATIC
NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL :

FINISH :

PROJECT: VLA — WYE MONITOR

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

TITLE: WYE MONITOR
M28 POWER SUPPLY/ BATTERY MODULE ASSEMBLY

DRAWN BY	DATE 6-93
DESIGNED BY	DATE 6-93
APPROVED BY	DATE 6-93

SHEET NUMBER 1 OF 1 | DRAWING NUMBER D13900P08 | REV. – | SCALE 1/1

BILL OF MATERIAL
NATIONAL RADIO ASTRONOMY OBSERVATORY

X ELECTRICAL X MECHANICAL BOM # A13900Z02 REV - DATE 6-17-93 PAGE 2 OF 4

MODULE M28 NAME POWER SUPPLY/BATTERY DWG# D13900P08 SUB ASSY _____ DWG# _____

SCHEM. DWG# C13900S10 LOCATION WYE MON QUA/SYS. _____ PREPRD BY K. TATE APPRVD BY N. ATENCIO

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
1		NRAO	C13900M05	PANEL, FRONT	1
2		NRAO	C13900M09	PANEL, REAR	1
3		NRAO	C13050M04	GUIDE	4
4		NRAO	C13720M15-2	SUPPORT, TOP	1
5		NRAO	C13720M15-1	SUPPORT, BOTTOM	1
6		NRAO	B13050M23	SUPPORT, RIGHT SIDE	2
7		NRAO	C13720M17	SPACER, INSULATED RAIL	2
8		NRAO	B13050M18	PLATE, SIDE	2
9		NRAO	C13050M22-2	COVER, PERFORATED	2
10		NRAO	B13900M10	SPACER	4
11		NRAO	C13050M70	KNOB, MODULE PULLER	2
12		NRAO	C13900M11-1	PLATE, MOUNTING	2
13		NRAO	C13900M11-2	PLATE, MOUNTING	2
14				LED, GREEN	1
15		HEWLETT PACKARD	HLMP-0103	RING, LED MOUNTING	1
16				JACK, NEG	1
17				JACK, POS	1
18		AMP	201357-3	CONNECTOR, 37-PIN	1
19		AMP	202394-2	SHIELD, CONNECTOR	1
20		AMP	200833-4	PIN, GUIDE	2

REVISIONS
REV | DATE | DRAWN BY | APPRV'D BY | DESCRIPTION

USED ON
NEXT ASSY

DRAWN BY DATE 6-93
DESIGNED BY DATE 6-93
APPROVED BY DATE 6-93

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

V L A

PROJECT WYE MONITOR
TITLE M28 POWER SUPPLY/BATTERY MODULE BOM
DWG NO. A13900Z02
SHEET 1 OF 4

BILL OF MATERIAL
NATIONAL RADIO ASTRONOMY OBSERVATORY

X ELECTRICAL X MECHANICAL BOM # A13900Z02 REV - DATE 6-17-93 PAGE 4 OF 4

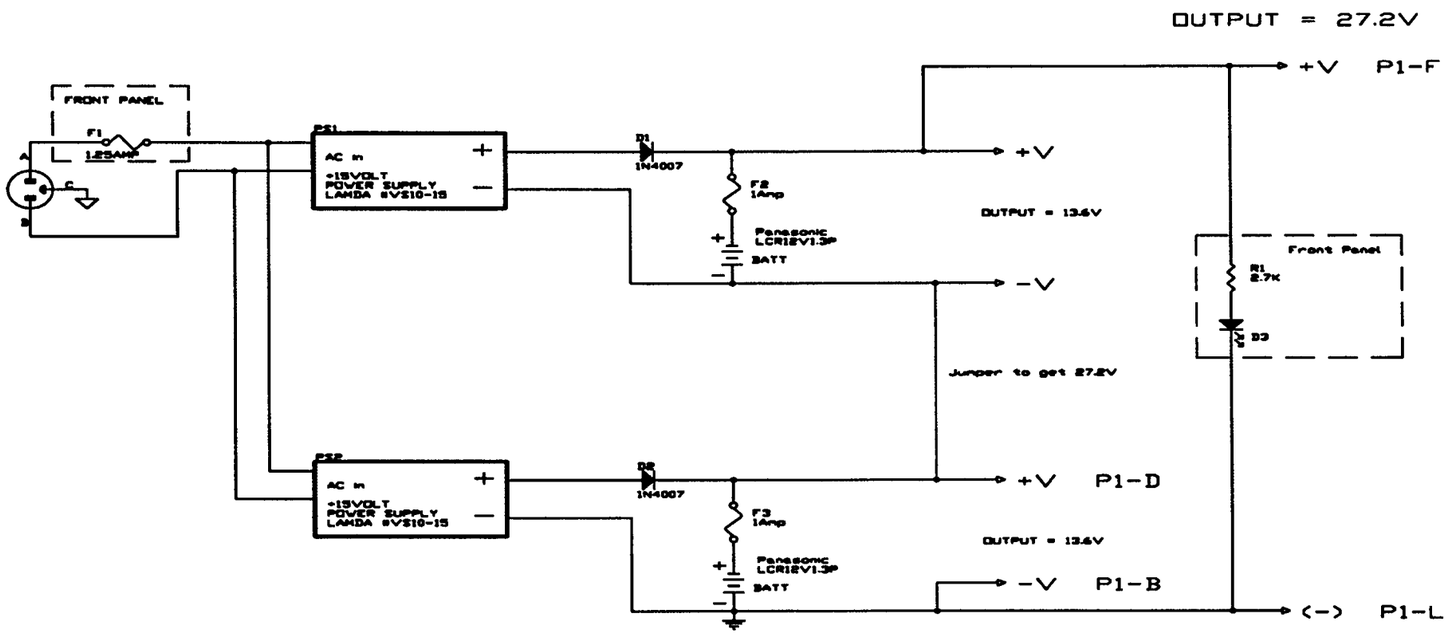
ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
38				WASHER, EXT. TOOTH, #6	16
39				WASHER, SPLIT RING LOCK, #6	2
40				LUG	4
41		T&B		WRAP, TIE	6
42				STANDOFF, 4-40UNC-2B x .50	4
43		ALPHA	7053	WIRE, RED #26 GA.	AR
44		ALPHA	7053	WIRE, BLK #26 GA.	AR
45		ALPHA	7055	WIRE, WHT #22 GA.	AR
46		ALPHA	7055	WIRE, RED #22 GA.	AR
47		ALPHA	7055	WIRE, BLK #22 GA.	AR
48		ALPHA	7055	WIRE, GRN #22 GA.	AR
49		ALPHA	7055	WIRE, GRY #22 GA.	AR
50		NRAO	D13900AB09	SILKSCREEN, FRONT PANEL	---
51		NRAO	D13900P08	ASSEMBLY, M28 MODULE	--
52		NRAO	C13900S10	SCHEMATIC, M28 MODULE	---
53		NRAO	A13900Z02	BOM	---
54					
55					
56					
57					
58					
59					

BILL OF MATERIAL
NATIONAL RADIO ASTRONOMY OBSERVATORY

X ELECTRICAL X MECHANICAL BOM # A13900Z02 REV - DATE 6-17-93 PAGE 3 OF 4

ITEM #	REF DES	MANUFACTURER	PART NUMBER	DESCRIPTION	TOTAL QTY.
21		AMP	203964-6	SOCKET, GUIDE	2
22		AMPHENOL	MS3102A-14S-01P	CONNECTOR	1
23		LITTLEFUSE	344125	FUSE, 20A, 125V	1
24				FUSE, 1A, 125V	2
25		NEMIC LAMBDA	SCB032A	SUPPLY, POWER	2
26		PANASONIC	LCR12V1.3P	BATTERY, RECHARGABLE	2
27		SOUTCHO	47-10-204-10	SCREW, CAPTIVE	3
28				SCREW, PAN HD, SS, 4-40UNC-2A x .25	18
29				SCREW, SOCKET HD, SS, 4-40UNC-2A x .38	4
30				SCREW, FLAT HD, SS, 6-32UNC-2A x .25	12
31				SCREW, FLAT HD, SS, 6-32UNC-2A x .38, HP GREY	2
32				SCREW, FLAT HD, SS, 6-32UNC-2A x .75	2
33				SCREW, PAN HD, SS 6-32UNC-2A x .25	8
34				SCREW, PAN HD, SS, 6-32UNC-2A x .75	4
35				SCREW, PAN, SS, 6-32UNC-2A x .88	4
36				SCREW, SOCKET HD, SS, 6-32UNC-2A x .38	2
37				WASHER, LOCK, #4	4

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	6-93			REMOVED GND FROM BATTERY



NEXT ASSEMBLY	DVG TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS <.XXX> ±
2 PLACE DECIMALS <.XX> ±
1 PLACE DECIMALS <.X> ±

MATERIAL:

FINISH:

PROJECT: WYE MONITOR

TITLE: M28 POWER SUPPLY/ BATTERY MODULE SCHEMATIC DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO,NEW MEXICO 87801

DRAWN BY	DATE 5-93
DESIGNED BY	DATE
APPROVED BY	DATE

SHEET NUMBER	DRAWING NUMBER	REV.	SCALE
1 OF 1	C13900S10	A	-

ORCAD : 13900S10

2.13 WYE-COMM Cable System

Four drawings describe the WYE-COMM system 25-pair cable routing, termination and signal assignments. These are: D13900B02, D13900B03, D13900B04 and D13900B05 — for the West, North, East Arms and Auxiliary cables, respectively. For convenience, reduced-scale copies of these drawings follow the text. The cable characteristics are specified by NRAO specification 91S00137, dated 25 September, 1977. The WYE Monitor system bus signals are distributed on these cables.

The implementation of the WYE Monitor system made five previous antenna-related cable functions obsolete which released many pairs of lines for other service. These obsolete functions are: NCP Reset, Emergency Stop, Antenna Stow Monitor, ACU Reset and Fire Alarm; therefore, they are not described in this manual. The Executone voice-communication equipment distributed on the WYE-COMM cables remains in service as the principal antenna-control room voice communication system. The Power Loss Alarm circuitry is also still in service.

During the WYE Monitor system implementation, the condition of the pairs formerly used for the above five functions were measured to determine line-to-line: DC and AC noise levels, resistance and capacitance. The DC and AC noise levels, resistance and capacitance to earth ground were not measured. The pairs selected for WYE Monitor signal distribution were based upon these measurements. The measurements were made at the control cable room punch-down terminal blocks except where noted. For documentation purposes, the measurement data are tabulated below.

West Arm Cable, 5/19/93

PAIR	DC mV	AC mV	Resistance Ω	Capacitance μF	CONDITION
BLU/WHT	350	190	open	1.16	OK
BLU/RED	12	20	open	1.17	OK
ORG/RED	60	16	open	1.17	OK
GRN/RED	1500	2	open	1.16	OK
BRN/RED	3300	1200	?	1.8 - 2.1?	Bad line, 180 Hz noise
SLATE/RED	70	250	open	1.17	
BLU/BLK	260	140	open	1.16	
ORG/BLK	150	2	open	1.17	
GRN/BLK	230	180	30 MΩ?	1.17 - 1.20	
BRN/BLK	60	2	open	1.15	
SLATE/BLK	60	540	open	0.27	
GRN/YEL	-	-	-	-	Used for WYE Monitor bus
BRN/YEL	2700	15	open	1.08	
SLATE/YEL	550	55	open	1.15	
SLATE/VIO	5500	1500	≈1 mΩ	1.7 - 2.0?	Bad line, 180 Hz noise

North Arm Cable, 3/18, 1993

BLU/WHT	-	-	-	1.07	
BLU/RED	-	-	-	1.06	
ORG/RED	10	≈1.9	open	1.06	
GRN/RED	28	≈2.0	open	1.07	
BRN/RED	60	≈2.0	open	1.06	
SLATE/RED	10	20	open	1.42	
BLU/BLK	3	<2	open	1.06	
ORG/BLK	20	<2	open	1.07	
GRN/BLK	11	<2	open	1.07	
BRN/BLK	<10	<2	open	1.06	
SLATE/BLK	20	<2	open	1.07	

GRN/YEL	<10	>150	open	1.06	Noisy
SLATE/YEL	40	>130	open?	0.4	Noisy
SLATE/VIO	200 to 500	900	open	1.4	Noisy

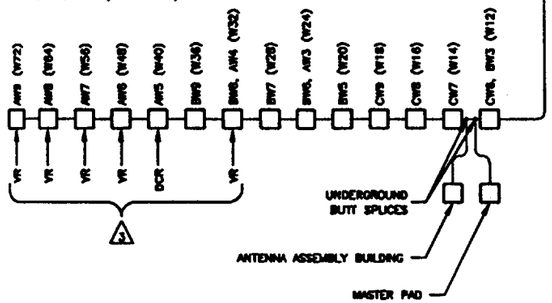
East Arm Cable, 5/18/93

BLU/WHT	200	<2	open	1.17	
BLU/RED	5500	500	open	1.8 - 2.0	
ORG/RED	150	<2	open	1.17	
GRN/RED	300	<2	open	1.17	
BRN/RED	270	<2	open	1.16	
SLATE/RED	20	<2	open	1.17	
BLU/BLK	1300	<2	open	1.15	
ORG/BLK	<10	<2	open	1.16	
GRN/BLK	2	2	open	1.17	
BRN/BLK	10	<2	open	1.15	
SLATE/BLK	10	<2	open	1.17	
GRN/YEL	<10	450	-	0.08 - 0.10	
BRN/YEL	-	-	-	-	Used for WYE Monitor bus
SLATE/YEL	60	2	open	1.15	
SLATE/VIO	5	35	open	1.07	
GRN/YEL	-10	52	open	0.192	At AE9, WYE Monitor bus

REV	DATE	DRAWN BY	APPR'V'D BY	DESCRIPTION
D	8-94			REVISED AND REDRAWN

NOTES:

1. REFERENCE: PUNCH-DOWN BOX LOCATION AND CABLE REPLACEMENT BLOCK DIAGRAM (NRAO DRAWING ∅C13900B13)
2. 25-PAIR ARMORED CABLE, SUPERIOR TYPE ASPWF, CONDUCTORS ∅22 AWG PER NRAO SPECIFICATION 91S00137, DATED SEPTEMBER 27, 1977. SEE NRAO DRAWING ∅C13900B13 FOR LOCATION OF PUNCH-DOWN BOX AND REPLACEMENT OF 18-PAIR CABLE
3. REFERENCE: PEDESTAL JUNCTION BOX DETAIL (NRAO DRAWING ∅D13900B06)
   REFERENCE: CABLE REPEATER BLOCK DIAGRAM (NRAO DRAWING ∅D13900B07)
   VR = VOICE FREQUENCY, 2-WAY REPEATER AMPLIFIER
   DCR = DC REPEATER FOR CONTROL CIRCUITS
4. REFERENCE: AWS/BW5 POWER MONITOR BLOCK DIAGRAM (NRAO DRAWING ∅C13900B09)
5. ALL JUNCTION BOXES ARE IDENTICAL
6. REFERENCE: TELEPHONE SYSTEM BLOCK DIAGRAM (NRAO DRAWING ∅D13900B01) OFFICE ROOM ∅1, SHEET 1
7. REFERENCE: WYE MONITOR A&B SWITCH BOX SCHEMATIC DIAGRAM (NRAO DRAWING ∅B13900W07)
8. APPROXIMATE LOOP RESISTANCE:
   CB TO DW1 (STATION 1) = 63 OHMS
   CB TO BW5 (STATION 20) = 400 OHMS
   CB TO AW5 (STATION 40) = 1170 OHMS



25-PAIR ARMORED CABLE

PD BLOCK #	WIRE COLOR	PAIR MATE	PD BLOCK #
1	BLUE	WHITE	2
3	ORANGE	WHITE	4
5	GREEN	WHITE	6
7	BROWN	WHITE	8
9	GRAY	WHITE	10
11	BLUE	RED	12
13	ORANGE	RED	14
15	GREEN	RED	16
17	BROWN	RED	18
19	GRAY	RED	20
21	BLUE	BLACK	22
23	ORANGE	BLACK	24
25	GREEN	BLACK	26
27	BROWN	BLACK	28
29	GRAY	BLACK	30
31	BLUE	YELLOW	32
33	ORANGE	YELLOW	34
35	GREEN	YELLOW	36
37	BROWN	YELLOW	38
39	GRAY	YELLOW	40
41	BLUE	VIOLET	45
42	ORANGE	VIOLET	46
43	GREEN	VIOLET	47
44	BROWN	VIOLET	48
49	GRAY	VIOLET	50

25-PAIR ARMORED CABLE

+28 VDC

MAINTENANCE PEDESTAL

25-PAIR ARMORED CABLE

PD BLOCK #	WIRE COLOR	PAIR MATE	PD BLOCK #	
1	BLUE	WHITE	2	SPARE1
3	ORANGE	WHITE	4	LINE ONE VOICE
5	GREEN	WHITE	6	LINE TWO VOICE
7	BROWN	WHITE	8	LINE ONE BUSY/PAGE
9	GRAY	WHITE	10	LINE TWO BUSY/PAGE
11	BLUE	RED	12	SPARE2
13	ORANGE	RED	14	WYE MONITOR
15	GREEN	RED	16	SPARE3
17	BROWN	RED	18	POWER LOSS ALARM
19	GRAY	RED	20	SPARE4
21	BLUE	BLACK	22	SPARE5
23	ORANGE	BLACK	24	SPARE6
25	GREEN	BLACK	26	SPARE7
27	BROWN	BLACK	28	SPARE8
29	GRAY	BLACK	30	SPARE9
31	BLUE	YELLOW	32	BWSAC POWER MONITOR
33	ORANGE	YELLOW	34	AWSAC POWER MONITOR
35	GREEN	YELLOW	36	SPARE10
37	BROWN	YELLOW	38	SPARE11
39	GRAY	YELLOW	40	SPARE12
41	BLUE	VIOLET	45	-28VDC
42	ORANGE	VIOLET	46	
43	GREEN	VIOLET	47	
44	BROWN	VIOLET	48	
49	GRAY	VIOLET	50	SPARE13

JUNCTION BOX 5
(BEHIND GENERATOR BUILDING)

CW5 (W10)
DW9 (W9)
DW8, CW4, BW2, AW1 (W8)
DW7 (W7)
DW6 (W6)
DW5 (W5)
DW4, CW2, BW1 (W4)
DW3 (W3)
DW2 (W2)
DW1 (W1)

25-PAIR ARMORED CABLE

W19VS EXECUTONE CABLE

PD BLOCK #	SHIELDED PAIR	WIRE COLOR	PAIR MATE	PD BLOCK #
1	SP	BLUE	WHITE	2
3	SP	ORANGE	WHITE	4
5	SP	GREEN	WHITE	6
7	SP	BROWN	WHITE	8
9	SP	GRAY	WHITE	10
11	SP	BLUE	RED	12
13	SP	ORANGE	RED	14
15	SP	GREEN	RED	16
17	SP	BROWN	RED	18
19	SP	GRAY	RED	20
21	SP	BLUE	BLACK	22
23	SP	ORANGE	BLACK	24
25	SP	GREEN	BLACK	26
27		BROWN	BLACK	28
29	SP	GRAY	BLACK	30
31		BLUE	YELLOW	32
33		ORANGE	YELLOW	34
35		GREEN	YELLOW	36
37		BROWN	YELLOW	38
39		GRAY	YELLOW	40
41		BLUE	VIOLET	45
42		ORANGE	VIOLET	46
43		GREEN	VIOLET	47
44		BROWN	VIOLET	48
49		GRAY	VIOLET	50

25-PAIR ARMORED CABLE

S.W. CORNER

MAINTENANCE BUILDING
SERVO SHOP

TO MAINTENANCE BUILDING AUXILIARY PD BLOCK

PD BLOCK #	SHIELDED PAIR	WIRE COLOR	PAIR MATE	PD BLOCK #	
1	SP	BLUE	WHITE	2	UNUSED
3	SP	ORANGE	WHITE	4	LINE ONE VOICE
5	SP	GREEN	WHITE	6	LINE ONE BUSY/PAGE CONTROL
7	SP	BROWN	WHITE	8	LINE TWO VOICE
9	SP	GRAY	WHITE	10	LINE TWO BUSY/PAGE CONTROL
11	SP	BLUE	RED	12	
13	SP	ORANGE	RED	14	
15	SP	GREEN	RED	16	
17	SP	BROWN	RED	18	
19	SP	GRAY	RED	20	
21	SP	BLUE	BLACK	22	RADIO CONTROL
23	SP	ORANGE	BLACK	24	RADIO TRANSMIT AUDIO 8
25	SP	GREEN	BLACK	26	RADIO RECEIVE AUDIO
27		BROWN	BLACK	28	
29	SP	GRAY	BLACK	30	
31		BLUE	YELLOW	32	
33		ORANGE	YELLOW	34	
35		GREEN	YELLOW	36	
37		BROWN	YELLOW	38	
39				40	
41		#16 RED		42	
43		#16 BLACK		44	
45				46	
47				48	
49				50	

TECH SERVICES BUILDING
MAIL ROOM EAST WALL
(IN CEILING)

TO EXECUTONE EQUIPMENT

TO EXECUTONE EQUIPMENT

#16 RED +28VDC

#16 BLACK -28VDC

25-PAIR ARMORED CABLE

PD BLOCK #	WIRE COLOR
1	BLUE
2	WHITE
3	ORANGE
4	WHITE
5	GREEN
6	WHITE
7	BROWN
8	WHITE
9	GRAY
10	WHITE
11	BLUE
12	RED
13	ORANGE
14	RED
15	GREEN
16	RED
17	BROWN
18	RED
19	GRAY
20	RED
21	BLUE
22	BLACK
23	ORANGE
24	BLACK
25	GREEN
26	BLACK
27	BROWN
28	BLACK
29	GRAY
30	BLACK
31	BLUE
32	YELLOW
33	ORANGE
34	YELLOW
35	GREEN
36	YELLOW
37	BROWN
38	YELLOW
39	GRAY
40	YELLOW
41	BLUE
42	VIOLET
43	ORANGE
44	VIOLET
45	GREEN
46	VIOLET
47	BROWN
48	VIOLET
49	GRAY
50	VIOLET

TERMINAL BLOCK # — TB1 (1-20), TB2 (1-20), TB3 (1-14 UNUSED)

TO 7 A&B SWITCH BOX — RED, GREEN

TO AC ALARM PANEL — ORANGE, BLUE, WHITE/ORANGE

4 BW5

WHITE/BLACK AW5 4

EAST ARM — NORTH ARM

PD BLOCK LOCATED ON BASE STATION PANEL ON CATWALK ABOVE ELECTRONICS LAB

TERMINAL BLOCKS FOR NORTH, EAST, AND WEST ARMS ARE LOCATED ON JUNCTION BOARD UNDER CONTROL ROOM FLOOR

JUNCTION BOARD

CONTROL BUILDING

ACAD : 13900B02

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL :

FINISH :

NEXT ASSEMBLY | DWG. TYPE

VLA — WYE COMMUNICATIONS SYSTEM

TITLE: WYE COMMUNICATIONS WEST ARM MAIN TELEPHONE CABLE BLOCK DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY | DATE 11-81
DESIGNED BY | DATE
APPROVED BY | DATE

SHEET NUMBER 1 OF 1 | DRAWING NUMBER D13900B02 | REV. D | SCALE NONE

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
D	8-94			REVISED AND REDRAWN

NOTES:

1. REFERENCE: PUNCH-DOWN BOX LOCATION AND CABLE REPLACEMENT BLOCK DIAGRAM (NRAO DRAWING #C13900B13)
2. 25-PAIR ARMORED CABLE, SUPERIOR TYPE ASPWF, CONDUCTORS #22 AWG PER NRAO SPECIFICATION 91S00137, DATED SEPTEMBER 27, 1977. SEE NRAO DRAWING #C13900B13 FOR LOCATION OF PUNCH-DOWN BOX AND REPLACEMENT OF 19-PAIR CABLE
3. REFERENCE: PEDESTAL JUNCTION BOX DETAIL (NRAO DRAWING #D13900B06)
   REFERENCE: CABLE REPEATER BLOCK DIAGRAM (NRAO DRAWING #D13900B07)
   VR = VOICE FREQUENCY, 2-WAY REPEATER AMPLIFIER
   DCR = DC REPEATER FOR CONTROL CIRCUITS
4. REFERENCE: AXS/BXS POWER MONITOR BLOCK DIAGRAM (NRAO DRAWING #C13900B09)
5. ALL JUNCTION BOXES ARE IDENTICAL
6. REFERENCE: TELEPHONE SYSTEM BLOCK DIAGRAM (NRAO DRAWING #D13900B01) OFFICE ROOM #1, SHEET 1
7. REFERENCE: WYE MONITOR A&B SWITCH BOX SCHEMATIC DIAGRAM (NRAO DRAWING #B13900W07)
8. APPROXIMATE LOOP RESISTANCE:
   CB TO DN1 (STATION 1) = 75 OHMS
   CB TO BN5 (STATION 20) = 330 OHMS
   CB TO AN5 (STATION 40) = 900 OHMS

PD BLOCK #	WIRE COLOR	PAIR MATE	PD BLOCK #	
1	BLUE	WHITE	2	SPARE1
3	ORANGE	WHITE	4	LINE ONE VOICE
5	GREEN	WHITE	6	LINE TWO VOICE
7	BROWN	WHITE	8	LINE ONE BUSY/PAGE
9	GRAY	WHITE	10	LINE TWO BUSY/PAGE
11	BLUE	RED	12	SPARE2
13	ORANGE	RED	14	WYE MONITOR
15	GREEN	RED	16	SPARE3
17	BROWN	RED	18	POWER LOSS ALARM
19	GRAY	RED	20	SPARE4
21	BLUE	BLACK	22	SPARE5
23	ORANGE	BLACK	24	SPARE6
25	GREEN	BLACK	26	SPARE7
27	BROWN	BLACK	28	SPARE8
29	GRAY	BLACK	30	SPARE9
31	BLUE	YELLOW	32	BN5AC POWER MONITOR
33	ORANGE	YELLOW	34	AN5AC POWER MONITOR
35	GREEN	YELLOW	36	SPARE10
37	BROWN	YELLOW	38	SPARE11
39	GRAY	YELLOW	40	SPARE12
41	BLUE	VIOLET	45	-28VDC
42	ORANGE	VIOLET	46	
43	GREEN	VIOLET	47	
44	BROWN	VIOLET	48	
49	GRAY	VIOLET	50	SPARE13

+28VDC

DN1 (N1) 5

1,2 25-PAIR ARMORED CABLE

25-PAIR ARMORED CABLE

PD BLOCK #	WIRE COLOR
1	BLUE
2	WHITE
3	ORANGE
4	WHITE
5	GREEN
6	WHITE
7	BROWN
8	WHITE
9	GRAY
10	WHITE
11	BLUE
12	RED
13	ORANGE
14	RED
15	GREEN
16	RED
17	BROWN
18	RED
19	GRAY
20	RED
21	BLUE
22	BLACK
23	ORANGE
24	BLACK
25	GREEN
26	BLACK
27	BROWN
28	BLACK
29	GRAY
30	BLACK
31	BLUE
32	YELLOW
33	ORANGE
34	YELLOW
35	GREEN
36	YELLOW
37	BROWN
38	YELLOW
39	GRAY
40	YELLOW
41	BLUE
42	VIOLET
43	ORANGE
44	VIOLET
45	GREEN
46	VIOLET
47	BROWN
48	VIOLET
49	GRAY
50	VIOLET

TERMINAL BLOCK # — TB1 (1–20), TB2 (1–20), TB3 (1–14)

TO 6 A&B SWITCH BOX — RED, GREEN

TO AC ALARM PANEL — ORANGE, BLUE, WHITE/BLACK, WHITE/BLUE

4 BN5

WHITE/BLACK

AN5

4

#16 RED — +28VDC

TO EXECUTONE EQUIPMENT

#16 BLACK

-28VDC

UNUSED (TB3 11–14)

PD BLOCK LOCATED ON BASE STATION PANEL ON CATWALK ABOVE ELECTRONICS LAB

TERMINAL BLOCKS FOR NORTH, EAST, AND WEST ARMS ARE LOCATED ON JUNCTION BOARD UNDER CONTROL ROOM FLOOR

JUNCTION BOARD

WEST ARM

EAST ARM

CONTROL BUILDING

ACAD : 13900B03

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL :

FINISH :

NEXT ASSEMBLY | DWG. TYPE

VLA

WYE COMMUNICATIONS SYSTEM

WYE COMMUNICATIONS NORTH ARM MAIN TELEPHONE CABLE BLOCK DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY | DATE 1-82

DESIGNED BY | DATE

APPROVED BY | DATE

SHEET NUMBER 1 OF 1 | DRAWING NUMBER D13900B03 | REV. D | SCALE NONE

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
D	8-94			REVISED AND REDRAWN

NOTES:

1. REFERENCE: PUNCH-DOWN BOX LOCATION AND CABLE REPLACEMENT BLOCK DIAGRAM (NRAO DRAWING #C13900813)
2. 25-PAIR ARMORED CABLE, SUPERIOR TYPE ASPWF, CONDUCTORS #22 AWG PER NRAO SPECIFICATION 91S00137, DATED SEPTEMBER 27, 1977. SEE NRAO DRAWING #C13900813 FOR LOCATION OF PUNCH-DOWN BOX AND REPLACEMENT OF 19-PAIR CABLE
3. REFERENCE: PEDESTAL JUNCTION BOX DETAIL (NRAO DRAWING #D13900806)
   REFERENCE: CABLE REPEATER BLOCK DIAGRAM (NRAO DRAWING #D13900807)
   VR = VOICE FREQUENCY, 2-WAY REPEATER AMPLIFIER
   DCR = DC REPEATER FOR CONTROL CIRCUITS
4. REFERENCE: AX5/BX5 POWER MONITOR BLOCK DIAGRAM (NRAO DRAWING #C13900809)
5. ALL JUNCTION BOXES ARE IDENTICAL
6. REFERENCE: TELEPHONE SYSTEM BLOCK DIAGRAM (NRAO DRAWING #D13900801) OFFICE ROOM #1, SHEET 1
7. REFERENCE: WYE MONITOR A&B SWITCH BOX SCHEMATIC DIAGRAM (NRAO DRAWING #B13900W07)
8. APPROXIMATE LOOP RESISTANCE:
   CB TO DE1 (STATION 1) = 60 OHMS
   CB TO BE5 (STATION 20) = 330 OHMS
   CB TO AE5 (STATION 40) = 960 OHMS

AE9 (E72) AE8 (E84) AE7 (E56) AE6 (E48) AE5 (E40) BE9 (E36) BE8, AE4 (E32) BE7 (E28) BE6, AE3 (E24) BE5 (E20) CE9 (E18) CE8, BE4, AE2 (E16) CE7 (E14) CE6, BE3 (E12) CE5 (E10) DE9 (E9) DE8, CE4, BE2, AE1, (E8) DE7 (E7) DE6, CE3 (E6) DE5 (E5) DE4, CE2, BE1 (E4) DE3 (E3) DE2, CE1 (E2)

VR VR VR VR DCR VR

△3

25-PAIR ARMORED CABLE

PD BLOCK #	WIRE COLOR	PAIR MATE	PD BLOCK #	
1	BLUE	WHITE	2	SPARE1
3	ORANGE	WHITE	4	LINE ONE VOICE
5	GREEN	WHITE	6	LINE TWO VOICE
7	BROWN	WHITE	8	LINE ONE BUSY/PAGE
9	GRAY	WHITE	10	LINE TWO BUSY/PAGE
11	BLUE	RED	12	SPARE2
13	ORANGE	RED	14	WYE MONITOR
15	GREEN	RED	16	SPARE3
17	BROWN	RED	18	POWER LOSS ALARM
19	GRAY	RED	20	SPARE4
21	BLUE	BLACK	22	SPARE5
23	ORANGE	BLACK	24	SPARE6
25	GREEN	BLACK	26	SPARE7
27	BROWN	BLACK	28	SPARE8
29	GRAY	BLACK	30	SPARE9
31	BLUE	YELLOW	32	BW5AC POWER MONITOR
33	ORANGE	YELLOW	34	AW5AC POWER MONITOR
35	GREEN	YELLOW	36	SPARE10
37	BROWN	YELLOW	38	SPARE11
39	GRAY	YELLOW	40	SPARE12
41	BLUE	VIOLET	45	
42	ORANGE	VIOLET	46	
43	GREEN	VIOLET	47	
44	BROWN	VIOLET	48	
49	GRAY	VIOLET	50	SPARE13

+28VDC

−28VDC

DE1 (E1) △5

△1 △2 25-PAIR ARMORED CABLE

25-PAIR ARMORED CABLE

PD BLOCK #	WIRE COLOR
1	BLUE
2	WHITE
3	ORANGE
4	WHITE
5	GREEN
6	WHITE
7	BROWN
8	WHITE
9	GRAY
10	WHITE
11	BLUE
12	RED
13	ORANGE
14	RED
15	GREEN
16	RED
17	BROWN
18	RED
19	GRAY
20	RED
21	BLUE
22	BLACK
23	ORANGE
24	BLACK
25	GREEN
26	BLACK
27	BROWN
28	BLACK
29	GRAY
30	BLACK
31	BLUE
32	YELLOW
33	ORANGE
34	YELLOW
35	GREEN
36	YELLOW
37	BROWN
38	YELLOW
39	GRAY
40	YELLOW
41	BLUE
42	VIOLET
43	ORANGE
44	VIOLET
45	GREEN
46	VIOLET
47	BROWN
48	VIOLET
49	GRAY
50	VIOLET

TO EXECUTONE EQUIPMENT

+28VDC #16 RED

#16 BLACK

−28VDC

PD BLOCK LOCATED ON BASE STATION PANEL ON CATWALK ABOVE ELECTRONICS LAB

TERMINAL BLOCK #				
1	TB1			
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				
17				
18				
19				
20				
1	TB2			
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				
17				
18				
19				
20				
1	TB3			
2				
3				
4				
5				
6				
7				
8				
9				
10				
11	UNUSED			
12	UNUSED			
13	UNUSED			
14	UNUSED			

TO △6 A&B SWITCH BOX — RED, GREEN

TO AC ALARM PANEL — ORANGE, BLUE, WHITE/VIOLET

△4 BE5

WHITE/BLACK

AE5 △4

WEST ARM

NORTH ARM

TERMINAL BLOCKS FOR NORTH, EAST, AND WEST ARMS ARE LOCATED ON JUNCTION BOARD UNDER CONTROL ROOM FLOOR

JUNCTION BOARD

CONTROL BUILDING

ACAD : 13900B04

NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL :

FINISH :

VLA — WYE COMMUNICATIONS SYSTEM

TITLE: WYE COMMUNICATIONS EAST ARM MAIN TELEPHONE CABLE BLOCK DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 1-82
DESIGNED BY	DATE
APPROVED BY	DATE

SHEET NUMBER 1 or 1 | DRAWING NUMBER D13900804 | REV. D | SCALE NONE

REV	DATE	DRAWN BY	APPR'D BY	DESCRIPTION
G	11-94			REVISED AND REDRAWN

NOTES:

1. 25-PAIR ARMORED CABLE, SUPERIOR TYPE ASPWF, CONDUCTORS #22 AWG PER NRAO SPECIFICATION 91S00137, DATED SEPTEMBER 27, 1977.
2. 19-PAIR ARMORED CABLE, EXECUTONE TYPE W19VS, 14 SHIELDED PAIRS #22 AWG: SINGLE CONDUCTORS #22 AWG; 1 PAIR #16 AWG. SP = SINGLE PAIR
3. #16 AWG RED: +28VDC
   #16 AWG BLACK: -28VDC AND GND (EXECUTONE)
4. REFERENCE: TELEPHONE SYSTEM BLOCK DIAGRAM (NRAO DRAWING #D13900801, SHEETS 2 & 3)
5. SPARE, 25-PAIR ARMORED CABLE ONLY
6. WIRES ARE TIED TOGETHER WITH WIRE NUTS
7. SEE NRAO DRAWINGS #C9390017

ANTENNA ASSEMBLY BUILDING

PD BLOCK #	WIRE COLOR	PAIR MATE	PD BLOCK #
1 SP	RED	WHITE	2
3 SP	ORANGE	WHITE	4
5 SP	GREEN	WHITE	6
7 SP	BROWN	WHITE	8
9 SP	GRAY	WHITE	10
11 SP	BLUE	RED	12
13 SP	ORANGE	RED	14
15 SP	GREEN	RED	16
17 SP	BROWN	RED	18
19 SP	GRAY	RED	20
21 SP	BLUE	BLACK	22
23 SP	ORANGE	BLACK	24
25 SP	GREEN	BLACK	26
27			28
29 SP	GRAY	BLACK	30
31	BLUE	WHITE	32
33	ORANGE	RED	34
35	GREEN	YELLOW	36
37	BROWN	VIOLET	38
39			40
41			42
43 SP	#16 RED	#16 BLACK	44
45			46
47			48
49			50

RAD CONTR
XMT AUD
RCV AUD

LOCATION: BASE OF LADDER

W19VS EXECUTONE CABLE (2)

TO AAB AND TRANSPORTER BUILDING (BLU/BLK) FIRE ALARM PULL STATIONS (BLU/RED)

CLOCK WIRE BLU/VIO

SP (5)

AUXILIARY CABLE BLU/RED

TO CLOCKS

PD BLOCK #	WIRE COLOR	PAIR MATE	PD BLOCK #
1	BLUE	WHITE	2
3	ORANGE	WHITE	4
5	GREEN	WHITE	6
7	BROWN	WHITE	8
9	GRAY	WHITE	10
11	BLUE	RED	12
13	ORANGE	RED	14
15	GREEN	RED	16
17	BROWN	RED	18
19	GRAY	RED	20
21	BLUE/BLUE	BLACK/RED	22
23	ORANGE	BLACK	24
25	GREEN	BLACK	26
27	BROWN	BLACK	28
29	GRAY	BLACK	30
31	BLUE	YELLOW	32
33	ORANGE	YELLOW	34
35	GREEN	YELLOW	36
37	BROWN	YELLOW	38
39	GRAY	YELLOW	40
41	BLUE	VIOLET	42
43	ORANGE	VIOLET	44
45	GREEN	VIOLET	46
47	BROWN	VIOLET	48
49	GRAY	VIOLET	50

LOCATION: NORTHEAST CORNER ABOVE OFFICE

(1) 25-PAIR ARMORED CABLE

CW6 BW3 W12

(2) W19VS EXECUTONE CABLE

JUNCTION BOX

PD BLOCK #	WIRE COLOR	PAIR MATE	PD BLOCK #
1	BLUE	WHITE	2
3	ORANGE	WHITE	4
5	GREEN	WHITE	6
7	BROWN	WHITE	8
9	GRAY	WHITE	10
11	BLUE	RED	12
13	ORANGE	RED	14
15	GREEN	RED	16
17	BROWN	RED	18
19	GRAY	RED	20
21	BLUE	BLACK	22
23	ORANGE	BLACK	24
25	GREEN	BLACK	26
27	BROWN	BLACK	28
29	GRAY	BLACK	30
31	BLUE	YELLOW	32
33	ORANGE	YELLOW	34
35	GREEN	YELLOW	36
37	BROWN	YELLOW	38
39	GRAY	YELLOW	40
41	BLUE	VIOLET	42
43	ORANGE	VIOLET	44
45	GREEN	VIOLET	46
47	BROWN	VIOLET	48
49	GRAY	VIOLET	50

LOCATION: BEHIND GENERATOR BUILDING

25-PAIR ARMORED CABLE (1)

MAINTENANCE PEDESTAL

PD BLOCK #	WIRE COLOR	PAIR MATE	PD BLOCK #
1	BLUE	WHITE	2
3	ORANGE	WHITE	4
5	GREEN	WHITE	6
7	BROWN	WHITE	8
9	GRAY	WHITE	10
11	BLUE	RED	12
13	ORANGE	RED	14
15	GREEN	RED	16
17	BROWN	RED	18
19	GRAY	RED	20
21	BLUE	BLACK	22
23	ORANGE	BLACK	24
25	GREEN	BLACK	26
27	BROWN	BLACK	28
29	GRAY	BLACK	30
31	BLUE	YELLOW	32
33	ORANGE	YELLOW	34
35	GREEN	YELLOW	36
37	BROWN	YELLOW	38
39	GRAY	YELLOW	40
41	BLUE	VIOLET	42
43	ORANGE	VIOLET	44
45	GREEN	VIOLET	46
47	BROWN	VIOLET	48
49	GRAY	VIOLET	50

25-PAIR ARMORED CABLE (1)

CW5 W10 — DW3 W8 — DW2 AW1 W8

SPLICE ABOVE GROUND INSIDE DW8, CW7, BW2, AND AW1 FENCE

25-PAIR ARMORED CABLE (1)

SERVO SHOP LINE PRINTER PORT 3 — BLK/RED GRN/WHT

SERVO SHOP CRT TERMINAL PORT 4 — BLK/RED GRN/WHT

PD BLOCK #	WIRE COLOR	PAIR MATE	PD BLOCK #
1 SP	BLUE	WHITE	2
3 SP	ORANGE	WHITE	4
5 SP	GREEN	WHITE	6
7 SP	BROWN	WHITE	8
9 SP	GRAY	WHITE	10
11 SP	BLUE	RED	12
13 SP	ORANGE	RED	14
15 SP	GREEN	RED	16
17 SP	BROWN	RED	18
19 SP	GRAY	RED	20
21 SP	BLUE	BLACK	22
23 SP	ORANGE	BLACK	24
25 SP	GREEN	BLACK	26
27	BROWN	BLACK	28
29 SP	GRAY	BLACK	30
31	BLUE	YELLOW	32
33	ORANGE	YELLOW	34
35	GREEN	YELLOW	36
37	BROWN	YELLOW	38
39	GRAY	YELLOW	40
41	BLUE	VIOLET	42
43	ORANGE	VIOLET	44
45	GREEN	VIOLET	46
47	BROWN	VIOLET	48
49	GRAY	VIOLET	50

BLU/BLK — TO OFFICE ROOM #1 IN TECH SERVICES BUILDING VIA 19-PAIR WEST ARM CABLE (REF: NRAO DWG #D13900802)

GRN/BLK

ORG/BLK

BLU/RED — CLOCK PULSE

LOCATION: SOUTHWEST CORNER

MAINTENANCE BUILDING SERVO SHOP

PD BLOCK #	WIRE COLOR	PAIR MATE	PD BLOCK #
1	BLUE	WHITE	2
3	ORANGE	WHITE	4
5	GREEN	WHITE	6
7	BROWN	WHITE	8
9	GRAY	WHITE	10
11	BLUE	RED	12
13	ORANGE	RED	14
15	GREEN	RED	16
17	BROWN	RED	18
19	GRAY	RED	20
21	BLUE	BLACK	22
23	ORANGE	BLACK	24
25	GREEN	BLACK	26
27	BROWN	BLACK	28
29	GRAY	BLACK	30
31	BLUE	YELLOW	32
33	ORANGE	YELLOW	34
35	GREEN	YELLOW	36
37	BROWN	YELLOW	38
39	GRAY	YELLOW	40
41	BLUE	VIOLET	42
43	ORANGE	VIOLET	44
45	GREEN	VIOLET	46
47	BROWN	VIOLET	48
49	GRAY	VIOLET	50

LOCATION: UNDER CONTROL ROOM FLOOR

WHT/VIO	RADIO PUSH TO TALK (4)
BLK/RED	SPARE
GRN/WHT	RADIO RECEIVE AUDIO (4)
BLK/RED	SERVO SHOP LINE PRINTER, PORT 3
GRN/WHT	SERVO SHOP LINE PRINTER, PORT 3
BLK/RED	SERVO SHOP CRT TERMINAL, PORT 4
GRN/WHT	SERVO SHOP CRT TERMINAL, PORT 4
ORG/WHT	RADIO TRANSMIT AUDIO (4)
BLK/WHT	SPARE
BLK/RED	CRYO LAB TERMINAL, PORT 1
WHT/GRN	AAB FIRE ALARM (N/C), PORT 1
GRN/WHT	CRYO LAB TERMINAL, PORT 1
BLK/RED	CRYO LAB LINE PRINTER, PORT 2
BLK/RED	SPARE, PORT 2 (5)
GRN/WHT	CRYO LAB LINE PRINTER, PORT 2
VIO/BLK	GENERATOR START KEY
GRY/BLK	SPARE

GRN/WHT

RED/GRN

WYE MONITOR A&B SWITCH BOX

M29 M28 — CONSOLE BIN

OPERATOR'S CONSOLE

BLK/RED

M28 M27 M27 — WYE MONITOR BIN

UPS ROOM

CONTROL BUILDING

TO FIRE SYSTEM PRESSURE SWITCH — RED/BLU

LOCATION: SE CORNER OF MAINTENANCE BLDG. SERVO SHOP

BLU/WHT
BLU/WHT
RED/WHT
ORG/WHT
GRN/WHT
RED/BLK
GRY/WHT
N/C
GRY/WHT
BLU/RED
ORG/RED
GRN/RED

TO FIRE SYSTEM J-BOX — TO CONTROL BUILDING FIRE ALARM ENUNCIATOR PANEL

PD BLOCK #	WIRE COLOR	PAIR MATE	PD BLOCK #
1 SP	RED	WHITE	2
3 SP	ORANGE	WHITE	4
5 SP	GREEN	WHITE	6
7 SP	BROWN	WHITE	8
9 SP	GRAY	WHITE	10
11 SP	BLUE	RED	12
13 SP	ORANGE	RED	14
15 SP	GREEN	RED	16
17 SP	BROWN	RED	18
19 SP	GRAY	RED	20
21 SP	BLUE	BLACK	22
23 SP	ORANGE	BLACK	24
25 SP	GREEN	BLACK	26
27			28
29 SP	GRAY	BLACK	30
31	BLUE	WHITE	32
33	ORANGE	RED	34
35	GREEN	YELLOW	36
37	BROWN	VIOLET	38
39			40
41			42
43 SP	#16 RED	#16 BLACK	44
45			46
47			48
49			50

LOCATION: ABOVE MAIL ROOM

MACHINE SHOP (ABOVE TELE. PANEL) — GENERATOR START — 752 TRIP

PLANS ELECTRIC

PD BLOCK #	WIRE COLOR	PAIR MATE	PD BLOCK #
1 SP	RED	WHITE	2
3 SP	ORANGE	WHITE	4
5 SP	GREEN	WHITE	6
7 SP	BROWN	WHITE	8
9 SP	GRAY	WHITE	10
11 SP	BLUE	RED	12
13 SP	ORANGE	RED	14
15 SP	GREEN	RED	16
17 SP	BROWN	RED	18
19 SP	GRAY	RED	20
21 SP	BLUE	BLACK	22
23 SP	ORANGE	BLACK	24
25 SP	GREEN	BLACK	26
27			28
29 SP	GRAY	BLACK	30
31	BLUE	WHITE	32
33	ORANGE	RED	34
35	GREEN	YELLOW	36
37	BROWN	VIOLET	38
39			40
41			42
43 SP	#16 RED	#16 BLACK	44
45			46
47			48
49			50

LOCATION: NORTH WALL

RED/BLK RED/BLK

SPLICE LOCATION: NORTH WALL

TECH SERVICES BUILDING

CRYO LAB

GRN/WHT BLK/RED — RCV XMT — LINE PRINTER PORT 2

GRN/WHT BLK/RED — RCV XMT — CRT TERMINAL PORT 1

RED/BLK RED/BLK

SPLICE LOCATION: SW CORNER OF SERVO SHOP

TWO (2) SHIELDED PAIRS #16 AWG

BLU/WHT BLU/BLK
RED/BLK ORG/BLK
RED/BLK RED/BRN

SPLICE

ELECTRIC SHOP J-BOX SPLICE BOX

W19VS EXECUTONE CABLE (2)

CONDUIT

GENERATOR START (7)

#16 AWG RED/BLK PAIR 752 TRIP, TO GENERATOR ROOM

RED/BRN RED/BLK

SPLICE

M28 M27 M27 M27

WYE MONITOR BIN

GENERATOR BUILDING

ACAD : 13900B05

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	VLA PROJECT	WYE COMMUNICATIONS SYSTEM	NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801
MATERIAL :	TITLE	WYE COMMUNICATIONS AUXILIARY TELEPHONE CABLE BLOCK DIAGRAM	DRAWN BY — DATE 12-81
FINISH :			DESIGNED BY — DATE
NEXT ASSEMBLY — DWG. TYPE			APPROVED BY — DATE
	SHEET NUMBER 1 OF 1	DRAWING NUMBER D13900B05	REV. G — SCALE NONE

2.14 Module Alignment

PC Interface Bin Modules

The most appropriate environment for testing the PC Interface Bin modules is a PC that is executing the control program and an off-line PC Interface bin equipped with the PC Transceiver, Watch-Dog Timer and Bin Power Supply Module. The modules can also be individually bench-tested with suitable test conditions.

PC Transceiver Module

The PC transceiver should be tested with an RS-232 level serial data stream using the WYECOM Cable Simulator C13900P03 for a load. The RS-232 data stream need not be formatted messages but must have a 300 Hz baud rate. The Transceiver output signal is 60 volts, p-p and the signal at the end of the load (AW9+ and AW9- terminals) should be an almost linear sawtooth signal with about a 37 volt, p-p amplitude. The signal character and amplitude should be measured using a two-channel oscilloscope in the differential mode.

Watch-Dog Timer Module

The Watch-Dog Timer module is typically tested in the PC Interface Bin with the PC turned off. The LEDs and audible alarm indicate the Watch-Dog Timer's response to the missing PC holdoff signal.

Bin Power Supply Module

The Bin Power Supply Module should be tested at full output power; the module's Lambda LVS-44-12-B power supply should provide 2.1 amperes at 12 volts DC, at an operating temperature of 25°C. After testing at full load, a test load that exceeds this current rating should be applied to the module to verify proper operation of the overload protection circuitry.

Control Interface Modules M26, M27 and M29

The control interface modules test environment consists of a WYE Monitor Bus Message Handler and a Device Interface Simulator. The WYE Monitor Bus Message Handler generates Command and Monitor Data Request messages and receives Command Acknowledge and Monitor Acknowledge messages. The Device Interface Simulator simulates the control and monitor interfaces of the devices serviced by M26, M27 and M29.

The M28 Power Supply/Battery Module is not tested by the Device Interface Simulator; it must be tested independently.

At present there are two sets of bus-driving test environments to test these modules: the AOC WYE Monitor Development System and the portable WYE Monitor Bus Message Handler D13900S11, described below.

The WYE Monitor Bus Message Handler D13900S11 is a portable test unit that generates Command and Monitor Request messages and displays Command Acknowledge and Monitor

Acknowledge messages. This unit simulates the operation of the Control PC and can be used at any bus node. All possible stimulus address and message arguments can be generated and all possible response message address and message arguments can be displayed. It can generate either Command or Monitor Request messages or passively monitor and display a bus line's activity by not outputting Command or Monitor Request messages. It can perform either single-cycle (output a single request message and display the response message) or operate continuously. It can also act as the bus Master or a Slave unit. Examination of the schematic diagram shows that the command discretes states are set by toggle switches and monitor states are displayed by discrete LEDs. A thumbwheel switch defines the stimulus message address and the response message address is displayed on a numeric display. Four control switches determine the operating modes. This test unit contains line driving and receiving circuitry identical to that contained in the control interfaces.

Setting a toggle switch in the up position causes the corresponding Command or Monitor Request message argument bits to be a 1. This commands the corresponding port bit in the receiving module's (M26, M27 or M29) Isolated CPU Interface Board to be active low - the 1 state. The monitor data bits of the received Command and Monitor Acknowledge messages are similarly displayed on the display LEDs. A 1 in the message, corresponding to a low-true input on the Isolated CPU Interface Board port, lights the associated LED. Since the address is displayed in a two-digit decimal format, there is no ambiguity of interpretation of address bits sense. For convenience, a reduced-scale copy of D13900S11 follows this text.

The Device Interface Simulator D13900S13 is a bench test unit used to test and align M26, M27 and M29. This unit has three 50 pin AMP connectors that are cabled to M26, M27 or M29. Three bus input ports route the bus line to the module type under test. Three dedicated sets of address toggle switches define the address of the module under test. Three dedicated sets of toggle switches define the monitor data discretes states and dedicated discrete LED's indicate the command states. Toggle switches and LED's are only provided for implemented command/monitor functions; switches and/or LED's for unimplemented functions are not provided. For example, M26 has four unimplemented Port 0 funcions; the circuitry for these functions cannot be implemented in the tester since it is not defined in M26. Front-panel test jacks permit measurement of the test unit's power supply voltages.

The Device Interface Simulator contains the power supplies required for M26, M27 and M29. They consist of a 24 volt psuedo-battery, a 28 volt relay supply, a 13.6 volt psuedo-battery, a +5 volts supply, a -10.000 volt supply and a ±15 volt power supply. The -10.000 volt supply is powered by the +5 volt supply.

The Device Interface Simulator contains two additional test stimulus features required by M29: two periodic psuedo-RS-232 signals to test the M29 watch-dog circuitry and current sources that simulate the AD590 currents at 0° C and 40° C temperatures. Port 1.0 and 1.1 toggle switches control the psuedo-RS-232 signals; the switches permit the psuedo-RS-232 to be periodically output or inhibited.

Note from the schematic diagram that the bus communications jacks on the simulator rear panel each have a circuit interrupt switch wired into the bus signal circuitry. If the WYE Monitor Message Handler is plugged into J5, J6 and J7 are also connected to this message handler so that M27 and M29 also receive the same signals. If, for example, this message handler is plugged into J6, J7 will also be driven by the message handler but J5 is disconnected. In this case, the WYE Monitor Development System could be connected to J5 and independently drive an M26. Similarly, if the message handler is connected to J7, M26 and M27 could be independently driven by the development system.

Since a detailed description of this unit is beyond the scope of this manual, it is not described but for convenience, a reduced-scale copy of the schematic diagram, D13900S13 follows this text.

The test environment should also have provisions to simulate the loading imposed by a WYE COM system cable pair. The WYECOM Cable Simulator Assembly C13900P03 can be used for this purpose.

When the WYE Monitor Message Handler is used to test M29, the user should remember that M29's output can be either discretes or a converted analog value; however, reference to the M29 schematics and the M29 description of Section 2.12 should enable all M29 modes and states to be evaluated.

Since a detailed description of this message handler is beyond the scope of this manual, refer to the schematic diagram and the unit's 87C51 firmware for details on this unit's operation.

The description above is focused upon the WYE Monitor bus environment.

M26 Antenna Interface Module

Since the Device Interface Simulator interface circuitry simulates the antenna systems, the first M26 test should exercise the M26 message address-detection function. This test would verify that the M26's address circuitry responds properly to all possible address states set into the WYE Monitor Bus message handler and does not spuriously respond when it is not addressed. The address is set by M26-peculiar toggle switches on the Device Interface Simulator.

Note that unless special M26 jumpering, etc. is done or an ACU Fault Board is connected to M26 (with appropriate voltage and logic state inputs), an ACU fault state should be read out.

The discretes monitor states set by the toggle switches should be displayed on the WYE Monitor Bus Message Handler's monitor data display.

Secondly, the three M26 commands should turn on and off the associated control state indicator LED's.

M27 Auxiliary Module

Since the Device Interface Simulator interface circuitry simulates the computer-correlator UPS's and the generator system interfaces, the first M27 test should exercise the M27 message address-detection function. This test verifies that the M27's address circuitry responds properly to all possible address states set into the WYE Monitor Bus message handler and M27 does not spuriously respond when it is not addressed. The address is set by M27-peculiar toggle switches on the Device Interface Simulator.

Since M27's monitor and monitor interfaces are simple and uniform, the monitor states set in the toggle switches should be displayed on the WYE Monitor Bus Message Handler's discretes display.

Similarly, the two M27 commands should turn on and off the command display LEDs.

M29 Auxiliary Utility Module

M29 is a more complicated module; both the discretes monitor data mode and the analog monitor data modes must be tested. M29 does not perform command functions. Refer to the M29 description in Section 2.11.

Since the Device Interface Simulator interface circuitry simulates the Control Building systems, the first M29 test should exercise the M29 message address-detection function. This test would verify that the M29's address circuitry responds properly to all possible address states set into the WYE Monitor Bus Message Handler and does not spuriously respond when it is not addressed. The address is set by M29-peculiar toggle switches on the Device Interface Simulator.

After the address tests are performed, the discretes monitor data mode should be tested first. Command bit 03 (P03) should be set to a 0; this selects the discretes monitor mode. Next, the Port 0 and Port 1 toggle switches should be exercised. The switch states should be displayed on the WYE Monitor Bus Message Handler discretes display. Note from the Device Interface Simulator schematic that this test also exercises the M29's RS-232 interface circuitry.

After verification of the discretes monitor circuitry, the AD590 interface circuitry should be aligned. This should be done before the analog data readout tests to permit verification of the converted analog data states.

AD590 Interface Circuits

The M29's +5.120 volt reference supply is adjusted first since the Analog-to-Digital Converter and the AD590 interface's offset current depend upon the accuracy of the +5.120 volt supply. The reference voltage may be measured on J1, the front panel test connector; pin 36 is the +5.120 supply output and pin 19 is analog ground. The 500 Ω trim potentiometer on dip header AG20 adjusts this voltage. The voltage should be set as close to +5.120 volts as possible. Bench tests have shown that this can be done with an error less than ± 1 mV.

Having set the +5.120 volt reference, the AD590 interface circuit's gain and offset trims can be set near the correct values by measuring the gain and zero path resistances with a digital multi-meter. This must be done for both AC47 and AE47 OP-15 operational amplifiers.

With power disconnected, measure the resistance from the OP-15's output pin (pin 6) to the inverting input pin (pin 2). Adjust the 2kΩ gain trim potentiometer (near the header's pin 6) until the total resistance is 50,000 Ω.

Measure the resistance from the +5.120 volt reference supply at J1-36 to the OP-15's inverting input (pin 2). Adjust the 1 kΩ trim potentiometer (near the header's pin 2) until the total resistance is 23,068 Ω.

After the initial settings described above, the circuits should be further adjusted using the calibration circuits built into the WYE Monitor Test Fixture. This fixture tests the AD590 interface circuits with precision current sinks. A switch near the bottom of the test fixture front panel selects 40° C or 0° C current sink values. Switch position labelled 0C (corresponding to an AD590 current at ° C) causes each channel to sink 273.15 μA. The other switch position, labelled 40C (corresponding to an AD590

current at +40° C), causes each channel to sink 313.15 μA. These current values are convenient reference points and are near those realized at the upper and lower points of the AD590's operational temperature environment.

With the current sinks set to 0C, adjust the offset trim potentiometers near pin 2 of the dip headers next to the temperature channel amplifliers so that the output voltages of the channel (measured on pin 6 of the amplifier or on the front panel test connector) is +2.560 volts. It should be possible to trim the voltage to within 1 or 2 mV.

With the current sinks set to 40C, adjust the gain trim potentiometers near pin 4 of the header next to the amplifiers so that the output voltage of the amplifiers are within 1 or 2 mV of +4.560 volts.

These two adjustments interact, so it may be necessary to repeat the adjustments two or more times before the voltages are correct within 1 or 2 mV.

Other than the +5.120 volt power supply voltage adjustment described above, there are no other adjustments required for the ADC0808 analog to digital converter.

After setting the AD590 interface amplifier's gain and offset adjustments, the analog data readout mode should be tested. To do so, set command bit P03 to 1 and bits PO0, PO1 and PO2 to 0. This sets the analog mode and selects analog multiplexer input IN0, the Chiller temperature probe channel. Set the Device Interface Simulator's Temperature Probes switch to 0° C. The output of both amplifiers should be +2.560 volts, mid-scale on the A/D converter's range. The corresponding value is $1000,0000_2$, (128_{10}) counts which should be displayed on the message handler discretes display.

Next, keeping command bit P03 a 1, set PO1 to 1, and PO2 and PO3 to 0. This selects analog multiplexer input IN1, the Condenser channel. The data readback should be identical to that read back from the Chiller channel.

Next, keeping command bit P03 a 1, set P01 and P02 to 1 and P03 to 0. This selects analog multiplexer input IN2, a floating input. The converted value should vary in a random manner.

Finally, keeping command bit P03 a 1, set PO0, PO1 and PO2 to 0; this selects analog multiplexer input IN0. Set the Temperature Probe switch to 40° C. The two amplifier outputs should be +4.560 volts and the corresponding digital value should be $1110,0100_2$. This value should be displayed on the message handler's discretes display. Finally, change the command bits to select IN1 and verify that the same value is displayed.

M28 Power Supply/Battery Module

Refer to the M28 schematic diagram C13900S10. M28 contains two Lambda VS10-15 modular power supplies. Adjust each supply's output to produce M28 output voltages of +13.6 and +27.2 volts.

The Panasonic LCR12V1.3P backup batteries have a capacity of 1.3 ampere-hours. Apply a 780 mA load to the 13.6 volt output and monitor the voltage for one hour. Record the results. Recharge the batteries and repeat the test using a 780 mA load on the 26.2 volt output. Again record the results. Recharge the batteries before the module is put into service.

REV.	DATE	DRAWN BY	APROV'D BY	DESCRIPTION
A	7-94			MINOR CORRECTIONS

NOTES:
1. # = ACTIVE LOW LEVEL
2. ALL RESISTORS ARE 1/4W, 5% UNLESS OTHERWISE INDICATED

ISOLATED COMMUNICATION INTERFACE

FRONT PANEL

LOW DATA

HIGH DATA

FUNCTION SELECT ROTARY SWITCHES

LCD DISPLAY CLOCK

LOW DATA LEDS

HIGH DATA LEDS

HIGH DIGIT

LOW DIGIT

ADDRESS

THUMB WHEELS

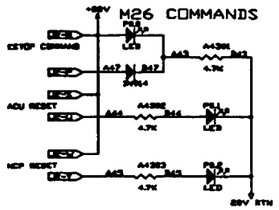
POWER CONDITIONING

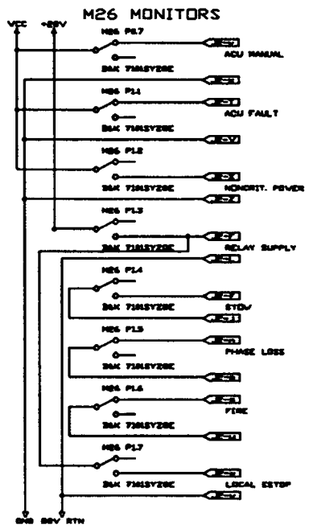
ORCAD : 13900S11

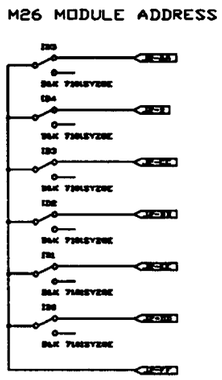
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ±		PRODUCT: WYE MONITOR	NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO,NEW MEXICO 87801
3 PLACE DECIMAL ±.XXX			
2 PLACE DECIMALS ±.XX			
1 PLACE DECIMALS ±.X			
MATERIAL:		TITLE: WYE MONITOR BUS MESSAGE HANDLER SCHEMATIC DIAGRAM	DRAWN BY / DATE
FINISH:			DESIGNED BY / DATE
			APPROVED BY / DATE
NEXT ASSEMBLY	SVG TYPE	SHEET NUMBER 1 OF 1	DRAWING NUMBER 13900S11 REV. A SCALE -

REV.	DATE	DRAWN BY	APPROV'D BY	DESCRIPTION

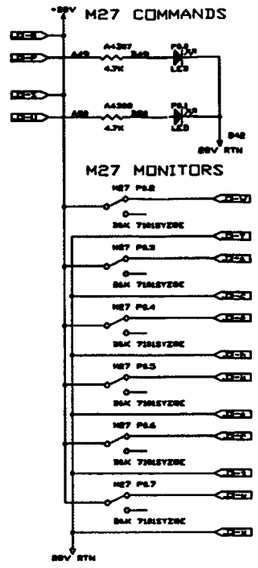
M26 TEST INTERFACE

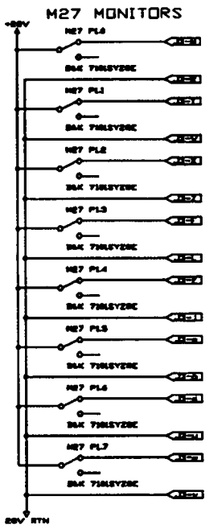


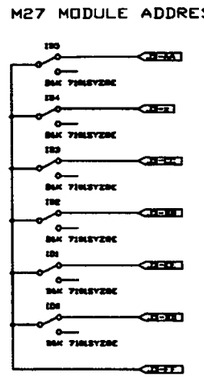




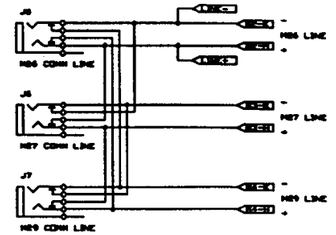
M27 TEST INTERFACE



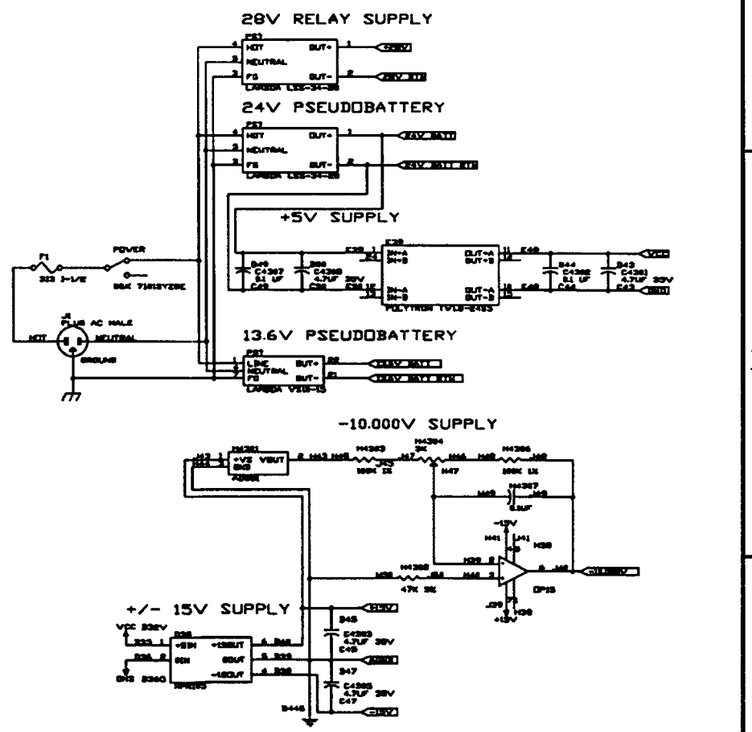




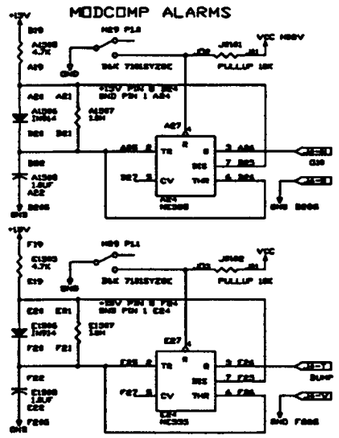
COMMUNICATIONS

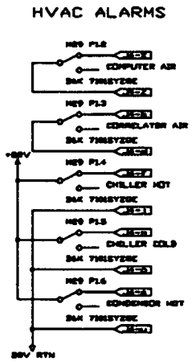


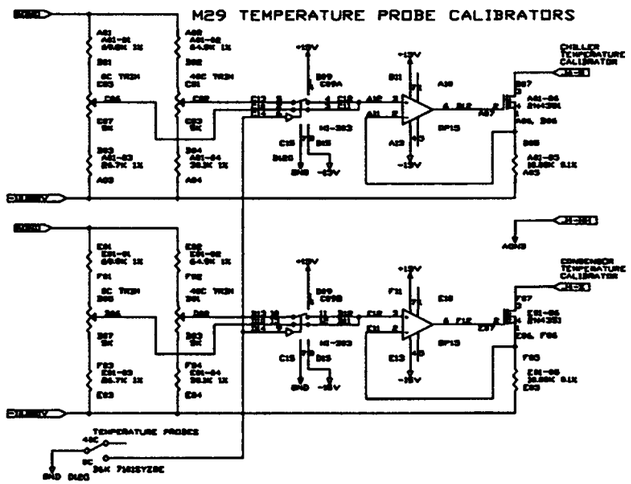
POWER SUPPLY

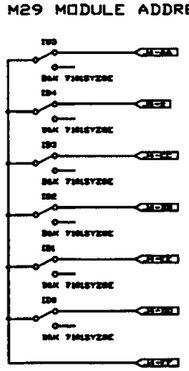


M29 TEST INTERFACE









ORCAD : 13900S13

PROPERTY OF NRAO

NEXT ASSEMBLY	SIZE TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCED ANGLES ±
3 PLACE DECIMAL ±.XXX
2 PLACE DECIMALS ±.XX
1 PLACE DECIMALS ±.X

MATERIAL:

FINISH:

VLBA PROJECT: WYE MONITOR

TITLE: WYE MONITOR DEVICE INTERFACE SIMULATOR SCHEMATIC DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO,NEW MEXICO 87801

DRAWN BY	DATE 6-94
DESIGNED BY	DATE 6-94
APPROVED BY	DATE 6-94

SHEET NUMBER 1 OF 1 | DRAWING NUMBER 13900S13 | REV. - | SCALE -

3.0 WYE MONITOR SYSTEM AND RELATED FUNCTIONAL DRAWINGS LIST

Note: asterisk-marked drawings are listed for reference, they are not included in this manual.

WYE Monitor System Drawings

C13900B12 WYE Monitor System Block Diagram
D13900B11 WYE Monitor Touch-Screen Control/Monitor Menu Structure Block Diagram

PC Interface Bin and Modules

D13900P09 WYE Monitor PC Interface Bin Assembly Drawing
C13900W04 WYE Monitor PC Interface Bin Wiring Diagram

C13900S02 WYE Monitor PC Transceiver PCB Schematic
C13900P13 WYE Monitor PC Transceiver Module Assembly
C13900P01 WYE Monitor PC Transceiver PCB Assembly

C13900S06 WYE Monitor PC Watchdog Circuit Board Schematic Diagram
C13900P10 WYE Monitor PC Watchdog Module Assembly
C13900P11 WYE Monitor PC Watchdog Circuit Board Assembly
C13900P12 WYE Monitor PC Watchdog Circiut Board Dip Header Assembly

C13900P14 WYE Monitor Power Supply Module Assembly

B13900W07 WYE Monitor A&B Switch Box Wiring Diagram

Isolated CPU Interface

D13900P02 WYE Monitor Isolated CPU Interface Board Assembly
C13900S03 WYE Monitor Isolated CPU Interface Board Schematic Diagram

M26 Antenna Interface Module and Related Drawings

D13900P06 WYE Monitor M26 Antenna Interface Module Assembly
D13900S04 WYE Monitor M26 Antenna Interface Module Schematic Diagram
A13900Z01 M26 Antenna Interface Module BOM
A13900P04 M26 Dip Header Assembly
C13900W02 M26 Antenna Interface Module Connector Test Points Wiring Diagram
C13900P07 M26 Antenna Interface Module Wire-Wrap Component Layout

C13900P05 ACU Fault Printed Circuit Board Assembly
C13900S09 ACU Fault Printed Circuit Board Schematic Diagram

D13900W01 WYE Monitor Wiring Diagram

M27 Auxiliary Monitor Module and Related Drawings

D13900P20 WYE Monitor M27 Auxiliary Monitor Module Assembly
A13900Z04 M27 Auxiliary Monitor Module BOM
D13900S08 WYE Monitor M27 Auxiliary Monitor Schematic Diagram
C13900P21 M27 Auxiliary Monitor Module Wire-Wrap Component Board
A13900P23 M27 Auxiliary Monitor Module Dip Header Assembly
C13900W05 M27 Auxiliary Module Connector Test Points Wiring Diagram
A13900W06* M27 Auxiliary Monitor Module Wire List
D13900P22 M27 Auxiliary Monitor Isolated CPU Interface Board Assembly

C9390028 Main Generator WYE COM Monitor Circuits
B13900S12 WYE Monitor Master Cubicle Relay and Header Schematic Diagram
D13900W09 M27-Generator System Interface

D13900W10 M27-Correlator and Computer UPS Interface

M29 Auxiliary Monitor Module and Related Drawings

D13900P15 WYE Monitor M29 Auxiliary Utility Module Assembly

A13900Z03 M29 Auxiliary Utility Module BOM
D13900S07 WYE Monitor Auxiliary Utility Module Schematic Diagram
A13900P18 M29 Auxiliary Utility Module Dip Header Assembly
C13900W03 M29 Auxiliary Utility Module Connector Test Points Wiring Diagram
C13900P17 M29 Auxiliary Utility Module Wire-Wrap Board Component Layout
D13900P16 M29 Auxiliary Utility Isolated CPU Interface Board Assembly
C13900W08 M29 Module Control Building HVAC Interface Wiring Diagram

M28 Power Supply/Battery Module

D13900P08 WYE Monitor M28 Power Supply/Battery Module Assembly
A13900Z02 M28 Power Supply/Battery Module BOM
C13900S10 M28 Power Supply/Battery Module Schematic Diagram

WYE-COMM Cable System Drawings

D13900B02 Main Telephone Cable West Arm
D13900B03 Main Telephone Cable North Arm
D13900B04 Main Telephone Cable East Arm
D13900B05 Auxiliary Telephone Cable

C13900P03 WYE COM Cable Simulator Assembly
C13900S05 WYE COM Cable Simulator Schematic Diagram

C13900B09* WYE-COMM System AX5/BX5 Power Monitor Block Diagram
C13900S01* WYE-COMM System Power Alarm Circuit Card Schematic Diagram
C13900B08* WYE-COMM System 25 Pair to 19 Pair Cable Splice Diagram

WYE Monitor System Test/Alignment Units

D13900S11 WYE Monitor Bus Message Handler
D13900S13 Device Interface Simulator Schematic Diagram

4.0 APPENDIX

CRC Algorithm Description

The Cyclic Redundancy Check (CRC) character was mentioned in Section 2.2. This byte is formulated over the four message bytes by the message generator and appended to the end of the message as it is being transmitted. Using the same algorithm, the message receiver formulates a CRC over the four message bytes and compares the message CRC with the CRC it just formulated. If they agree, the probability that the message is contaminated by errors is vanishingly small and it is considered to be error-free.

This section briefly describes some of the CRC generation principles and is not a rigorous mathematical treatment.

Digital error detection techniques include the use of parity bits and check sums. A parity bit is formulated over a set of bits (typically a byte) in accordance with an odd or even parity rule. When there is more than one byte in a set of data, for example a digital time-serial message, each byte will have an appended parity bit. In a similar manner, a numerical check sum can be formed over a set of bytes.

The techniques of parity bit formulation and usage are well known and widely used. Bit error evaluation techniques sometimes involve grouping data bytes and a parity-check byte into tables to determine bit errors by examination of the parity of the table rows and columns. While this technique can detect a single bit error, two or more bit errors can defeat this error detection technique.

A check sum is the summation of a group of bytes and is a rudimentary but useful data error check. The sum may overflow (typically the case) and the remainder is used as a measure of the check sum. In the old days when computer programs were read from paper tape, check sums were used to indicate that the computer had apparently read the program without error. Again, two or more bit errors can defeat this technique.

In a manner analogous to the parity and check sum techniques mentioned above, a CRC error detection scheme involves applying a set of mathematical rules to a set of data to develop a CRC which is transmitted with the data. Then upon reception, the data is evaluated by the receiver using the same rules to develop a CRC character; if the two CRC characters are identical, the received message is error free. Multiple-bit data errors in the data do not defeat CRC techniques. Since the error probability is so minute, the CRC techniques are not used for error correction.

In the CRC technique, the message serial data bits can be considered to be a polynomial, G(X)[1], of the form, $G(X) = a_nX^n + a_{n-1}X^{n-1} + \ldots a_0X^0$ where the a coefficients are either a 1 or 0 and X is 2. Thus $X^4 + X + 1$ can be represented by the binary value 10011 where the a_4, a_1, and a_0 coefficients are 1 and the a_3 and a_2 coefficients are 0. The CRC technique uses a message polynomial G(X), a generator polynomial P(X); and the objective is to construct a code message polynomial F(X) that is evenly divisible by P(X). The steps are as follows:

---

[1] P114, Technical Aspects of Data Communications, McNamara, second edition, 1982, Digital Equipment Corporation, Bedford, Mass.

1. The message G(X) is multiplied by X^{n-k} where n-k is the number of bits in the CRC.

2. Divide the resulting product $X^{n-k}[G(X)]$ by the generator polynomial, P(X).

3. Disregard the quotient and add the remainder, C(X) to the product to yield the code message polynomial F(X), which is represented as $X^{n-k}[G(X)] + C(X)$. C(X) is the CRC.

The division is performed in binary without carries or borrows and the remainder is always one bit less than the divisor. The remainder is the CRC and the divisor is the generator polynomial; therefore the CRC bit length is always one less than than the number of bits in the generator polynomial.

Note that the transmitted F(X) message data bits will resemble the original message data bits although they have been multiplied by X^{n-k}, which is a single factor. Although the multiplication raises each bit's polynomial value, the bits still represent their hardware equivalent before transmission.

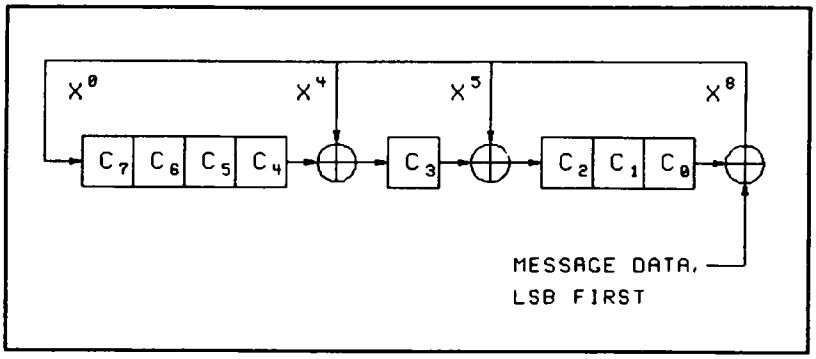


Figure 20 WYE Monitor CRC Generator Model

There are a number of CRC generation schemes; the VLA WYE Monitor scheme is described below. Remember that the WYE Monitor outputs the message address and data LSB first. This is important in the CRC formulation process.

Hardware implementations of CRC generators use a shift register with feedback to generate the CRC. Figure 20 shows a simplified representation of the hardware equivalent of the CRC generator used in the WYE Monitor system. The WYE Monitor system uses an 8051 software equivalent of this scheme, which is described in the 1990 Dallas Semiconductor Data Book. The CRC generator consists of a shift register and Exclusive-OR (XOR) gates. Shift counter and other logic details are not included in Figure 21. At the beginning of the message block, the CRC register is initialized to to a value of 0.

An XOR on the generator register output forms the XOR product of the data stream and the CRC generator register LSB output. This XOR output is fed back to XORs between stages 2 and 3, between stages 3 and 4 and is also input to the MSB-end of the generator register. The generator polynomial P(X) is thus $X^8 + X^5 + X^3 + 1$ or in binary representation, 10010101. The total number of message bits, which is n, is 40 and there are 32 data bits so k = 32. Thus n-k = 8, the number of CRC bits. Because there are 32 message bits in the WYE Monitor system message format, a CRC generation example is rather ponderous; therefore a simpler example follows.

1. Given:

Message polynomial G(X) = 110011 ($X^5 + X^4 + X + X^0$).
Generator polynomial P(X) = 11001 ($X^4 + X^3 + 1$).
G(X) contains 6 data bits.
P(X) contains 5 data bits and will yield a CRC with 4 bits; therefore n - k = 4.

2. Multiplying the message G(X) by X^{n-4} gives:

$X^{n-k}[G(X)] = X^4(X^5 + X^4 + X + X^0) = X^9 + X^8 + X^5 + X^4$. The binary equivalent of this product contains 10 bits and is 1100110000.

3. This product is divided by P(X).

```
                  100001      ← quotient
P(X) → 1001 ⟌1100110000       ← X^(n-k)[G(X)]
            11001
            -----
                10000
                11001
                -----
                 1001         ← remainder = C(X) = CRC
```

4. The remainder C(X) is added to $X^{n-k}[G(X)]$ to give F(X) = 1100111001.

The code message polynomial is transmitted. The receiver divides it by P(X). If there is no error, the division will produce no remainder and it is assumed that the message is error-free. A remainder indicates an error.

List of WYE Monitor System Commercial Hardware and Software Documentation

Covox Developer's Kit, Includes Sound Master II Owner's Manual and Software

Elographics:

Elographics Graphical User Interface.
Teletouch Touch Screen Controller, Model E281-4025
Elographics Touch-Screen Driver Program N1.5, Instruction and User's Manual

Autumn Hill Software: Menuet Software Manual. Two volumes: Library and Programming Guide

MetaWINDOW Reference Manual (This is the graphics interface between the control program C-language code and Menuet). These are the low-level graphics functions used in composing the C-language control program.

Willie's Computer Software Company: Comm-Drv Serial I/O driver used by the 4-port Serial I/O board.

TVGA Video Board - Model 8900C User's Manual

CTX Monitor - CVP-5468A Operating Manual

PC Generic Motherboard - 486SX-20 and DX-25/33 SC User's Manual, Rev D2, Oct 1991

5.0 Special-Purpose Components Data Sheets

The following special-purpose data sheets follow this page and are ordered as listed. Note that many of these components are widely used throughout the system.

PC Interface Bin

Intel 87C51FA Microcontroller
NEC PS2501-1 Photo Coupler
NEC PS2502-1 Photo Coupler
MAX233 RS-232 Driver/Receiver
MAX695 Microprocessor Supervisory Circuit
HPR105 DC/DC Converter
OP-15FP Operational Amplifier
Lambda LVS-44-12B Power Supply

Isolated CPU Interface Board

P1602 Surge Arrestor

M26 Antenna Interface

LTC1042 Window Comparator
LT1009 2.5 Volt Reference
Polytron TW1.8-24S5 DC/DC Converter

M29 Auxiliary Interface

ADC0808 Analog Multiplexer-A/D Converter
ICM7555 General Purpose Timer
AD590 Temperature Transducer
AD581 High Precision 10 V IC Reference
PALCE22V10Z-25 Programmable Array Logic
MC14060B 14-Bit Counter and Oscillator

M28 Power Supply/Battery Module

Lambda VS10-15 Power Supply
Panasonic LCR 12V1.3P Battery

HARRIS SEMICONDUCTOR

ICM7555/ICM7556
General Purpose Timer

GENERAL DESCRIPTION

The ICM7555/6 are CMOS RC timers providing significantly improved performance over the standard SE/NE555/6 and 355 timers, while at the same time being direct replacements for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, low THRESHOLD, TRIGGER and RESET currents, no crowbarring of the supply current during output transitions, higher frequency performance and no requirement to decouple CONTROL VOLTAGE for stable operation.

Specifically, the ICM7555/6 are stable controllers capable of producing accurate time delays or frequencies. The ICM7556 is a dual ICM7555, with the two timers operating independently of each other, sharing only V^+ and GND. In the one shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor. Unlike the regular bipolar 555/6 devices, the CONTROL VOLTAGE terminal need not be decoupled with a capacitor. The circuits are triggered and reset on falling (negative) waveforms, and the output inverter can source or sink currents large enough to drive TTL loads, or provide minimal offsets to drive CMOS loads.

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7555CBA	0°C to + 70°C	8 Lead SOIC
ICM7555IPA	25°C to + 85°C	8 Lead MiniDip
ICM7555ITV	− 25°C to + 85°C	TO-99 Can
ICM7555MTV*	− 55°C to + 125°C	TO-99 Can
ICM7556IPD	− 25°C to + 85°C	14 Lead Plastic DIP
ICM7556MJD*	− 55°C to + 125°C	14 Lead CERDIP

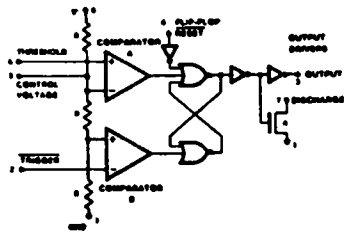
*Add /883B to part number if 883B processing is desired

FEATURES

- **Exact Equivalent in Most Cases for SE/NE555/556 or TLC555/556**
- **Low Supply Current — 60μA Typ. (ICM7555) 120μA Typ. (ICM7556)**
- **Extremely Low Trigger, Threshold and Reset Currents — 20pA Typical**
- **High Speed Operation — 1MHz Typical**
- **Wide Operation Supply Voltage Range Guaranteed 2 to 18 Volts**
- **Normal Reset Function – No Crowbarring of Supply During Output Transition**
- **Can Be Used With Higher Impedance Timing Elements Than Regular 555/6 for Longer RC Time Constants**
- **Timing From Microseconds Through Hours**
- **Operates in Both Astable and Monostable Modes**
- **Adjustable Duty Cycle**
- **High Output Source/Sink Driver Can Drive TTL/CMOS**
- **Typical Temperature Stability of 0.005% Per °C at 25°C**
- **Outputs Have Very Low Offsets, HI and LO**

APPLICATIONS

- **Precision Timing**
- **Pulse Generation**
- **Sequential Timing**
- **Time Delay Generation**
- **Pulse Width Modulation**
- **Pulse Position Modulation**
- **Missing Pulse Detector**



0363-1

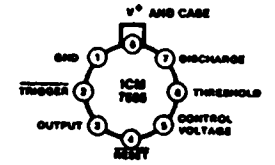
This Functional Diagram reduces the circuitry down to its simplest equivalent components. Tie down unused inputs. R = 100kΩ, ± 20% typ.

Figure 1: Functional Diagram

ABSOLUTE MAXIMUM RATINGS

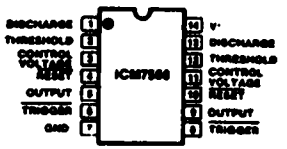
Supply Voltage ..... + 18 Volts
Input Voltage: Trigger, Control Voltage, Threshold, Reset[1] ..... V^+ + 0.3V to GND − 0.3V
Output Current 100mA
Power Dissipation[2] ICM7556 ..... 300mW
ICM7555 ..... 200mW
Storage Temperature ..... − 65°C to + 150°C
Lead Temperature (Soldering, 10sec) ..... + 300°C
Operating Temperature Range[2]
ICM7555/6 CX ..... 0°C to + 70°C
ICM7555/6 IX ..... − 25°C to + 85°C
ICM7555/6 MX ..... − 55°C to + 125°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



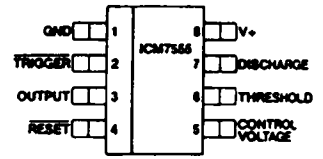
(OUTLINE DRAWING TV)

(OUTLINE DRAWING PA)



(OUTLINE DRAWING JD, PD)

0363-2



0363-3

(OUTLINE DRAWING BA)

Figure 2: Pin Configuration (Top View)

NOTES 1: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V^+ + 0.3V or less than V^- − 0.3V may cause destructive latchup. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power-supply is established. In multiple systems, the supply of the ICM7555/6 must be turned on first.

2: Junction temperatures should not exceed 135°C and the power dissipation must be limited to 20 mW at 125°C. Below 125°C power dissipation may be increased to 300 mW at 25°C. Derating factor is approximately 3 mW/°C (7556) or 2 mW/°C (7555).

NOTE: All typical values have been characterized but are not tested.

File Number 2867

NOTE: All typical values have been characterized but are not tested.

ICM7555
ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	ICM7555C,I,M T_A = 25°C			ICM7555M −55°C ≤ T_A ≤ +125°C			Units
			Min	Typ	Max	Min	Typ	Max	
I^+	Static Supply Current	V_{DD} = 5V V_{DD} = 15V		40 60	200 300			300 300	µA µA
	Monostable Timing Accuracy	RA = 10k, C = 0.1µF, V_{DD} = 5V		2		858		1161	% µs
	Drift with Temp*	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V					150 200 250		ppm/°C ppm/°C ppm/°C
	Drift with Supply*	V_{DD} = 5 to 15V		0.5			0.5		%/V
	Astable Timing Accuracy	RA = RB = 10k, C = 0.1µF, V_{DD} = 5V		2		1717		2323	% µs
	Drift with Temp*	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V					150 200 250		ppm/°C ppm/°C ppm/°C
	Drift with Supply*	V_{DD} = 5V to 15V		0.5			0.5		%/V
V_{TH}	Threshold Voltage	V_{DD} = 15V	62	67	71	61		72	% V_{DD}
V_{TRIG}	Trigger Voltage	V_{DD} = 15V	28	32	36	27		37	% V_{DD}
I_{TRIG}	Trigger Current	V_{DD} = 15V			10			50	nA
I_{TH}	Threshold Current	V_{DD} = 15V			10			50	nA
V_{CV}	Control Voltage	V_{DD} = 15V	62	67	71	61		72	% V_{DD}
V_{RST}	Reset Voltage	V_{DD} = 2 to 15V	0.4		1.0	0.2		1.2	V
I_{RST}	Reset Current	V_{DD} = 15V			10			50	nA
I_{DIS}	Discharge Leakage	V_{DD} = 15V			10			50	nA
V_{OL}	Output Voltage Drop	V_{DD} = 15V, I_{sink} = 20mA V_{DD} = 5V, I_{sink} = 3.2mA		0.4 0.2	1.0 0.4			1.25 0.5	V V
V_{OH}	Output Voltage Drop	V_{DD} = 15V, I_{source} = 0.8mA V_{DD} = 5V, I_{source} = 0.8mA	14.3 4.0	14.6 4.3		14.2 3.8			V V
V_{DIS}	Discharge Output Voltage Drop	V_{DD} = 5V, I_{SINK} = 15mA V_{DD} = 15V, I_{sink} = 15mA		0.2	0.4			0.6 0.4	V V
V^+	Supply Voltage*	Functional Oper.	2.0		18.0	3.0		16.0	V
t_R	Output Rise Time*	RL = 10M, CL = 10pF, V_{DD} = 5V		75					ns
t_F	Output Fall Time*	RL = 10M, CL = 10pF, V_{DD} = 5V		75					ns
f_{MAX}	Oscillator Frequency*	V_{DD} = 5V, RA = 470Ω, RB = 270Ω C = 200pF		1					MHz

*These parameters are based upon characterization data and are not tested.

NOTE: All typical values have been characterized but are not tested.

ICM7555/ICM7556

ICM7556
ELECTRICAL CHARACTERISTICS T_A = 25°C, unless otherwise specified.

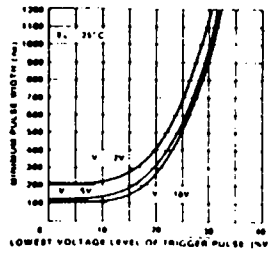
Symbol	Parameter	Test Conditions	ICM7556I,M T_A = 25°C			ICM7556M −55°C < T_A < +125°C			Units
			Min	Typ	Max	Min	Typ	Max	
I^+	Static Supply Current	V_{DD} = 5V V_{DD} = 15V		80 120	400 600			600 600	µA µA
	Monostable Timing Accuracy	RA = 10k, C = 0.1µF, V_{DD} = 5V		2		858		1161	% µs
	Drift with Temp*	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V					150 200 250		ppm/°C ppm/°C ppm/°C
	Drift with Supply*	V_{DD} = 5V to 15V		0.5			0.5		%/V
	Astable Timing Accuracy	RA = RB = 10k, C = 0.1µF, V_{DD} = 5V		2		1717		2323	% µs
	Drift with Temp*	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V					150 200 250		ppm/°C ppm/°C ppm/°C
	Drift with Supply*	V_{DD} = 5V to 15V		0.5			0.5		%/V
V_{TH}	Threshold Voltage	V_{DD} = 15V	62	67	71	61		72	% V_{DD}
V_{TRIG}	Trigger Voltage	V_{DD} = 15V	28	32	36	27		37	% V_{DD}
I_{TRIG}	Trigger Current	V_{DD} = 15V			10			50	nA
I_{TH}	Threshold Current	V_{DD} = 15V			10			50	nA
V_{CV}	Control Voltage	V_{DD} = 15V	62	67	71	61		72	% V_{DD}
V_{RST}	Reset Voltage	V_{DD} = 2V to 15V	0.4		1.0	0.2		1.2	V
I_{RST}	Reset Current	V_{DD} = 15V			10			50	nA
I_{DIS}	Discharge Leakage	V_{DD} = 15V			10			50	nA
V_{OL}	Output Voltage Drop	V_{DD} = 15V, I_{sink} = 20mA V_{DD} = 5V, I_{sink} = 3.2mA		0.4 0.2	1.0 0.4			1.25 0.5	V V
V_{OH}	Output Voltage Drop	V_{DD} = 15V, I_{source} = 0.8mA V_{DD} = 5V, I_{source} = 0.8mA	14.3 4.0	14.6 4.3		14.2 3.8			V V
V_{DIS}	Discharge Output Voltage Drop	V_{DD} = 5V, I_{sink} = 15mA V_{DD} = 15V, I_{sink} = 15mA		0.2	0.4			0.6 0.4	V V
V^+	Supply Voltage*	Functional Oper.	2.0		18.0	3.0		16.0	V
t_R	Output Rise Time*	RL = 10M, CL = 10pF, V_{DD} = 5V		75					ns
t_F	Output Fall Time*	RL = 10M, CL = 10pF, V_{DD} = 5V		75					ns
f_{MAX}	Oscillator Frequency*	V_{DD} = 5V, RA = 470Ω, RB = 270Ω, C = 200pF		1					MHz

*These parameters are based upon characterization data and are not tested.

NOTE: All typical values have been characterized but are not tested.

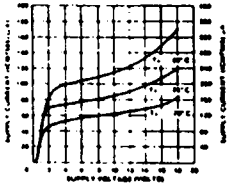
TYPICAL PERFORMANCE CHARACTERISTICS

MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



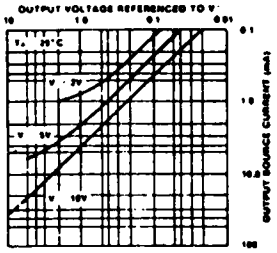
0363-4

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



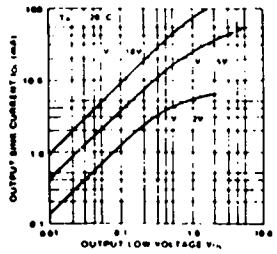
0363-5

OUTPUT SOURCE CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



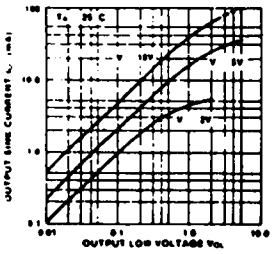
0363-6

OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



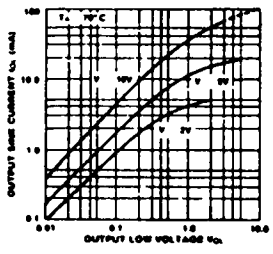
0363-7

OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



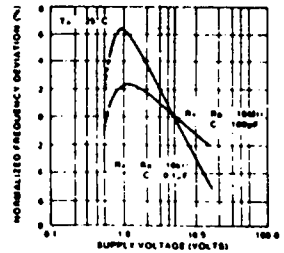
0363-8

OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



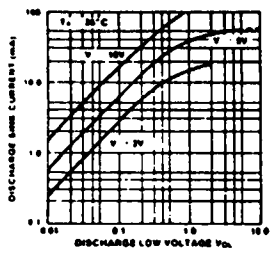
0363-9

NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE



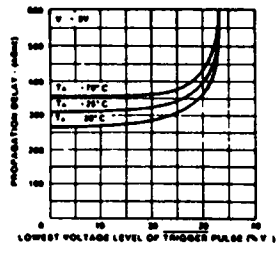
0363-10

DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



0363-11

PROPAGATION DELAY AS A FUNCTION OF VOLTAGE LEVEL OF TRIGGER PULSE



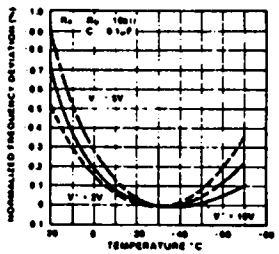
0363-12

NOTE: All typical values have been characterized but are not tested.

ICM7555/ICM7556

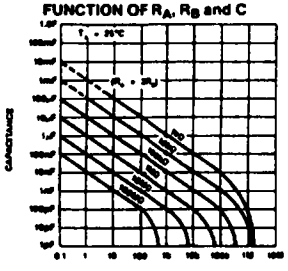
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE



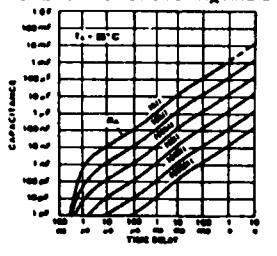
0363-13

FREE RUNNING FREQUENCY AS A FUNCTION OF R_A, R_B and C



0363-14

TIME DELAY IN THE MONOSTABLE MODE AS A FUNCTION OF R_A AND C

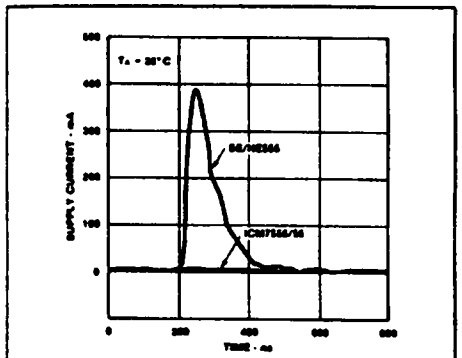


0363-15

APPLICATION NOTES

GENERAL

The ICM7555/6 devices are, in most instances, direct replacements for the NE/SE 555/6 devices. However, it is possible to effect economies in the external component count using the ICM7555/6. Because the bipolar 555/6 devices produce large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The 7555/6 devices produce no such transients. See Figure 3.



0363-16

Figure 3: Supply Current Transient Compared with a Standard Bipolar 555 During an Output Transition

The ICM7555/6 produces supply current spikes of only 2 - 3mA instead of 300 - 400mA and supply decoupling is normally not necessary. Secondly, in most instances, the CONTROL VOLTAGE decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high. Thus, for many applications 2 capacitors can be saved using an ICM7555, and 3 capacitors with an ICM7556.

POWER SUPPLY CONSIDERATIONS

Although the supply current consumed by the ICM7555/6 devices is very low, the total system supply can be high unless the timing components are high impedance. Therefore, use high values for R and low values for C in Figures 4 and 5.

OUTPUT DRIVE CAPABILITY

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5 volts or more the ICM7555/6 will drive at least 2 standard TTL loads.

ASTABLE OPERATION

The circuit can be connected to trigger itself and free run as a multivibrator, see Figure 4. The output swings from rail to rail, and is a true 50% duty cycle square wave. (Trip points and output swings are symmetrical). Less than a 1% frequency variation is observed, over a voltage range of + 5 to + 15V.

$$f = \frac{1.44}{RC}$$

The timer can also be connected as shown in Figure 4b. In this circuit, the frequency is:

$$f = 1.44/(R_A + 2R_B)C$$

The duty cycle is controlled by the values of R_A and R_B, by the equation:

$$D = R_B/(R_A + 2R_B)$$

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot. Initially the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative TRIGGER pulse to pin 2, the internal flip flop is set which releases the short circuit across the external capacitor and drives the OUTPUT high. The voltage across the capacitor now increases exponentially with a time constant $t = R_AC$. When the voltage across the capacitor equals $\frac{2}{3}$ V^+, the comparator resets the flip flop, which in turn discharges the capacitor rapidly and also drives the OUTPUT to its low state. TRIGGER must return to a high state before the OUTPUT can return to a low state.

$$t_{output} = -\ln(\tfrac{1}{3})\,R_AC = 1.1\,R_AC$$

NOTE: All typical values have been characterized but are not tested.

ICM7555/ICM7556

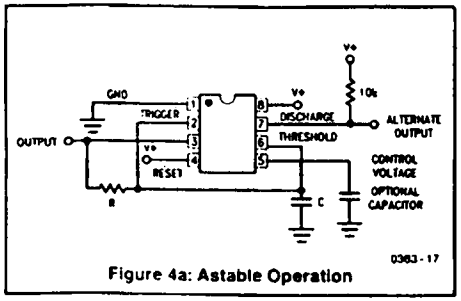


Figure 4a: Astable Operation

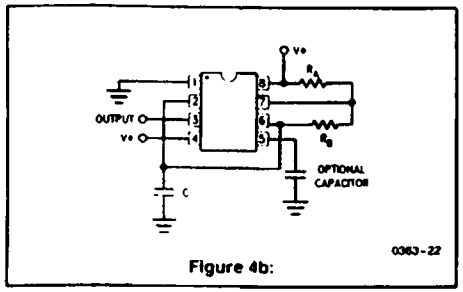


Figure 4b:

CONTROL VOLTAGE

The CONTROL VOLTAGE terminal permits the two trip voltages for the THRESHOLD and TRIGGER internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the astable mode or even inhibition of oscillation, depending on the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the CONTROL VOLTAGE pin.

RESET

The RESET terminal is designed to have essentially the same trip voltage as the standard bipolar 555/6, i.e. 0.6 to 0.7 volts. At all supply voltages it represents an extremely high input impedance. The mode of operation of the RESET function is, however, much improved over the standard bipolar 555/6 in that it controls only the internal flip flop, which in turn controls simultaneously the state of the OUTPUT and DISCHARGE pins. This avoids the multiple threshold problems sometimes encountered with slow falling edges in the bipolar devices.

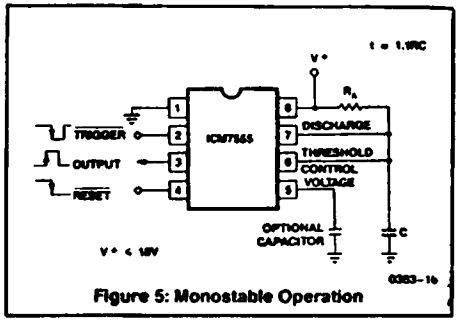


Figure 5: Monostable Operation

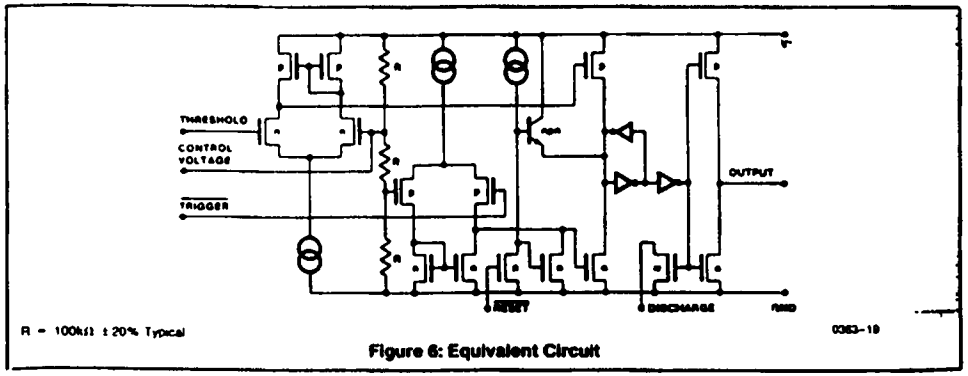


Figure 6: Equivalent Circuit

TRUTH TABLE

Threshold Voltage	Trigger Voltage	RESET	Output	Discharge Switch
DON'T CARE	DON'T CARE	LOW	LOW	ON
$> \frac{2}{3}(V^+)$	$> \frac{1}{3}(V^+)$	HIGH	LOW	ON
$< \frac{2}{3}(V^+)$	$> \frac{1}{3}(V^+)$	HIGH	STABLE	STABLE
DON'T CARE	$< \frac{1}{3}(V^+)$	HIGH	HIGH	OFF

NOTE: RESET will dominate all other inputs; TRIGGER will dominate over THRESHOLD.

NOTE: All typical values have been characterized but are not tested.

NOTE: All typical values have been characterized but are not tested.

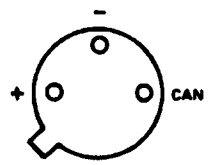
ANALOG DEVICES

Two-Terminal IC Temperature Transducer

AD590*

FEATURES
- Linear Current Output: 1μA/K
- Wide Range: -55°C to +150°C
- Probe Compatible Ceramic Sensor Package
- Two-Terminal Device: Voltage In/Current Out
- Laser Trimmed to ±0.5°C Calibration Accuracy (AD590M)
- Excellent Linearity: ±0.3°C Over Full Range (AD590M)
- Wide Power Supply Range: +4V to +30V
- Sensor Isolation from Case
- Low Cost

PIN DESIGNATIONS



BOTTOM VIEW

PRODUCT DESCRIPTION

The AD590 is a two-terminal integrated circuit temperature transducer which produces an output current proportional to absolute temperature. For supply voltages between +4V and +30V the device acts as a high impedance, constant current regulator passing 1μA/K. Laser trimming of the chip's thin film resistors is used to calibrate the device to 298.2μA output at 298.2K (+25°C).

The AD590 should be used in any temperature sensing application below +150°C in which conventional electrical temperature sensors are currently employed. The inherent low cost of a monolithic integrated circuit combined with the elimination of support circuitry makes the AD590 an attractive alternative for many temperature measurement situations. Linearization circuitry, precision voltage amplifiers, resistance measuring circuitry and cold junction compensation are not needed in applying the AD590.

In addition to temperature measurement, applications include temperature compensation or correction of discrete components, biasing proportional to absolute temperature, flow rate measurement, level detection of fluids and anemometry. The AD590 is available in chip form making it suitable for hybrid circuits and fast temperature measurements in protected environments.

The AD590 is particularly useful in remote sensing applications. The device is insensitive to voltage drops over long lines due to its high impedance current output. Any well-insulated twisted pair is sufficient for operation hundreds of feet from the receiving circuitry. The output characteristics also make the AD590 easy to multiplex: the current can be switched by a CMOS multiplexer or the supply voltage can be switched by a logic gate output.

*Covered by Patent No. 4,123,698.

PRODUCT HIGHLIGHTS

1. The AD590 is a calibrated two terminal temperature sensor requiring only a dc voltage supply (+4V to +30V). Costly transmitters, filters, lead wire compensation and linearization circuits are all unnecessary in applying the device.
2. State-of-the-art laser trimming at the wafer level in conjunction with extensive final testing insures that AD590 units are easily interchangeable.
3. Superior interference rejection results from the output being a current rather than a voltage. In addition, power requirements are low (1.5mW's @ 5V @ +25°C). These features make the AD590 easy to apply as a remote sensor.
4. The high output impedance (>10MΩ) provides excellent rejection of supply voltage drift and ripple. For instance, changing the power supply from 5V to 10V results in only a 1μA maximum current change, or 1°C equivalent error.
5. The AD590 is electrically durable: it will withstand a forward voltage up to 44V and a reverse voltage of 20V. Hence, supply irregularities or pin reversal will not damage the device.

AD590—SPECIFICATIONS (@ +25°C and V_S = +5V unless otherwise noted)

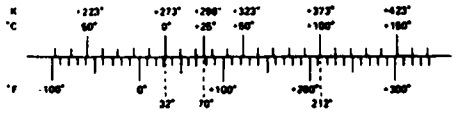
Model	AD590J Min	AD590J Typ	AD590J Max	AD590K Min	AD590K Typ	AD590K Max	Units
ABSOLUTE MAXIMUM RATINGS							
Forward Voltage (E+ to E−)			+44			+44	Volts
Reverse Voltage (E+ to E−)			−20			−20	Volts
Breakdown Voltage (Case to E+ or E−)			±200			±200	Volts
Rated Performance Temperature Range[1]	−55		+150	−55		+150	°C
Storage Temperature Range[1]	−65		+155	−65		+155	°C
Lead Temperature (Soldering, 10 sec)			+300			+300	°C
POWER SUPPLY							
Operating Voltage Range	+4		+30	+4		+30	Volts
OUTPUT							
Nominal Current Output @ +25°C (298.2K)		298.2			298.2		μA
Nominal Temperature Coefficient		1			1		μA/K
Calibration Error @ +25°C			±5.0			±2.5	°C
Absolute Error (over rated performance temperature range)							
Without External Calibration Adjustment			±10			±5.5	°C
With +25°C Calibration Error Set to Zero			±3.0			±2.0	°C
Nonlinearity			±1.5			±0.8	°C
Repeatability[2]			±0.1			±0.1	°C
Long Term Drift[3]			±0.1			±0.1	°C
Current Noise		40			40		pA/√Hz
Power Supply Rejection							
+4V≤V_S≤+5V		0.5			0.5		μA/V
+5V≤V_S≤+15V		0.2			0.2		μA/V
+15V≤V_S≤+30V		0.1			0.1		μA/V
Case Isolation to Either Lead		10^{10}			10^{10}		Ω
Effective Shunt Capacitance		100			100		pF
Electrical Turn-On Time		20			20		μs
Reverse Bias Leakage Current[4]							
(Reverse Voltage = 10V)		10			10		pA
PACKAGE OPTIONS[5]							
TO-52 (H-03A)		AD590JH			AD590KH		
Flat Pack (F-2A)		AD590JF			AD590KF		

NOTES
[1]The AD590 has been used at −100°C and +200°C for short periods of measurement with no physical damage to the device. However, the absolute errors specified apply to only the rated performance temperature range.
[2]Maximum deviation between +25°C readings after temperature cycling between −55°C and +150°C; guaranteed not tested.
[3]Conditions: constant +5V, constant +125°C; guaranteed, not tested.
[4]Leakage current doubles every 10°C.
[5]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Model	AD590L Min	AD590L Typ	AD590L Max	AD590M Min	AD590M Typ	AD590M Max	Units
ABSOLUTE MAXIMUM RATINGS							
Forward Voltage (E+ to E−)			+44			+44	Volts
Reverse Voltage (E+ to E−)			−20			−20	Volts
Breakdown Voltage (Case to E+ or E−)			±200			±200	Volts
Rated Performance Temperature Range[1]	−55		+150	−55		+150	°C
Storage Temperature Range[1]	−65		+155	−65		+155	°C
Lead Temperature (Soldering, 10 sec)			+300			+300	°C
POWER SUPPLY							
Operating Voltage Range	+4		+30	+4		+30	Volts
OUTPUT							
Nominal Current Output @ +25°C (298.2K)		298.2			298.2		μA
Nominal Temperature Coefficient		1			1		μA/K
Calibration Error @ +25°C			±1.0			±0.5	°C
Absolute Error (over rated performance temperature range)							
Without External Calibration Adjustment			±3.0			±1.7	°C
With +25°C Calibration Error Set to Zero			±1.6			±1.0	°C
Nonlinearity			±0.4			±0.3	°C
Repeatability[2]			±0.1			±0.1	°C
Long Term Drift[3]			±0.1			±0.1	°C
Current Noise		40			40		pA/√Hz
Power Supply Rejection							
+4V ≤ V_S ≤ +5V		0.5			0.5		μA/V
+5V ≤ V_S ≤ +15V		0.2			0.2		μA/V
+15V ≤ V_S ≤ +30V		0.1			0.1		μA/V
Case Isolation to Either Lead		10^{10}			10^{10}		Ω
Effective Shunt Capacitance		100			100		pF
Electrical Turn-On Time		20			20		μs
Reverse Bias Leakage Current[4] (Reverse Voltage −10V)		10			10		pA
PACKAGE OPTION[5]							
TO-52 (H-03A)		AD590LH			AD590MH		
Flat Pack (F-2A)		AD590LF			AD590MF		



TEMPERATURE SCALE CONVERSION EQUATIONS

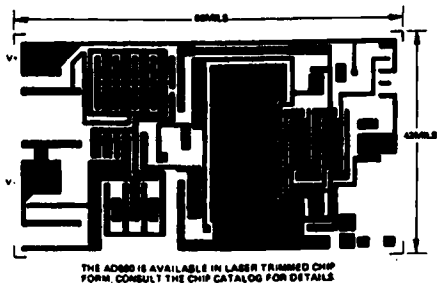
$$°C = \frac{5}{9}(°F - 32) \qquad K = °C + 273.15$$

$$°F = \frac{9}{5}°C + 32 \qquad °R = °F + 459.7$$

The 590H has 60μ inches of gold plating on its Kovar leads and Kovar header. A resistance welder is used to seal the nickel cap to the header. The AD590 chip is eutectically mounted to the header and ultrasonically bonded to with 1 MIL aluminum wire. Kovar composition: 53% iron nominal; 29% ±1% nickel; 17% ±1% cobalt; 0.65% manganese max; 0.20% silicon max; 0.10% aluminum max; 0.10% magnesium max; 0.10% zirconium max; 0.10% titanium max; 0.06% carbon max.

The 590F is a ceramic package with gold plating on its Kovar leads, Kovar lid, and chip cavity. Solder of 80/20 Au/Sn composition is used for the 1.5 mil thick solder ring under the lid. The chip cavity has a nickel underlay between the metalization and the gold plating. The AD590 chip is eutectically mounted in the chip cavity at 410°C and ultrasonically bonded to with 1 mil aluminum wire. Note that the chip is in direct contact with the ceramic base, not the metal lid. When using the AD590 in die form, the chip substrate must be kept electrically isolated, (floating), for correct circuit operation.

METALIZATION DIAGRAM



THE AD590 IS AVAILABLE IN LASER TRIMMED CHIP FORM. CONSULT THE CHIP CATALOG FOR DETAILS.

CIRCUIT DESCRIPTION[1]

The AD590 uses a fundamental property of the silicon transistors from which it is made to realize its temperature proportional characteristic: if two identical transistors are operated at a constant ratio of collector current densities, r, then the difference in their base-emitter voltages will be (kT/q)(ln r). Since both k, Boltzman's constant and q, the charge of an electron, are constant, the resulting voltage is directly porportional to absolute temperature (PTAT).

In the AD590, this PTAT voltage is converted to a PTAT current by low temperature coefficient thin film resistors. The total current of the device is then forced to be a multiple of this PTAT current. Referring to Figure 1, the schematic diagram of the AD590, Q8 and Q11 are the transistors that produce the PTAT voltage. R5 and R6 convert the voltage to current. Q10, whose collector current tracks the collector currents in Q9 and Q11, supplies all the bias and substrate leakage current for the rest of the circuit, forcing the total current to be PTAT. R5 and R6 are laser trimmed on the wafer to calibrate the device at +25°C.

Figure 2 shows the typical V–I characteristic of the circuit at +25°C and the temperature extremes.

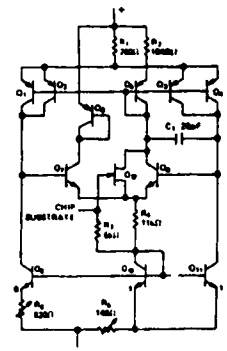


Figure 1. Schematic Diagram

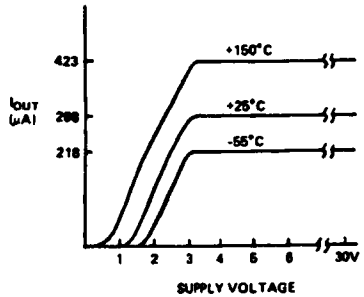


Figure 2. V–I Plot

[1] For a more detailed circuit description see M.P. Timko, "A Two-Terminal IC Temperature Transducer," IEEE J. Solid State Circuits, Vol. SC-11, p. 784-788, Dec. 1976.

EXPLANATION OF TEMPERATURE SENSOR SPECIFICATIONS

The way in which the AD590 is specified makes it easy to apply in a wide variety of different applications. It is important to understand the meaning of the various specifications and the effects of supply voltage and thermal environment on accuracy.

The AD590 is basically a PTAT (proportional to absolute temperature)[1] current regulator. That is, the output current is equal to a scale factor times the temperature of the sensor in degrees Kelvin. This scale factor is trimmed to 1μA/K at the factory, by adjusting the indicated temperature (i.e. the output current) to agree with the actual temperature. This is done with 5V across the device at a temperature within a few degrees of 25°C (298.2K). The device is then packaged and tested for accuracy over temperature.

CALIBRATION ERROR

At final factory test the difference between the indicated temperature and the actual temperature is called the calibration error. Since this is a scale factor error, its contribution to the total error of the device is PTAT. For example, the effect of the 1°C specified maximum error of the AD590L varies from 0.73°C at -55°C to 1.42°C at 150°C. Figure 3 shows how an exaggerated calibration error would vary from the ideal over temperature.

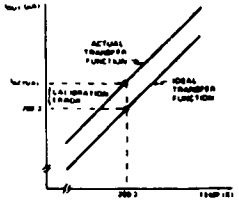


Figure 3. Calibration Error vs. Temperature

The calibration error is a primary contributor to maximum total error in all AD590 grades. However, since it is a scale factor error, it is particularly easy to trim. Figure 4 shows the most elementary way of accomplishing this. To trim this circuit the temperature of the AD590 is measured by a reference temperature sensor and R is trimmed so that V_T = 1mV/K at that temperature. Note that when this error is trimmed out at one temperature, its effect is zero over the entire temperature range. In most applications there is a current to voltage conversion resistor (or, as with a current input ADC, a reference) that can be trimmed for scale factor adjustment.

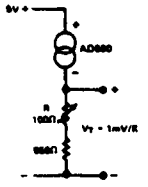


Figure 4. One Temperature Trim

[1] T(°C) = T(K) -273.2. Zero on the Kelvin scale is "absolute zero"; there is no lower temperature.

ERROR VERSUS TEMPERATURE: WITH CALIBRATION ERROR TRIMMED OUT

Each AD590 is also tested for error over the temperature range with the calibration error trimmed out. This specification could also be called the "variance from PTAT" since it is the maximum difference between the actual current over temperature and a PTAT multiplication of the actual current at 25°C. This error consists of a slope error and some curvature, mostly at the temperature extremes. Figure 5 shows a typical AD590K temperature curve before and after calibration error trimming.

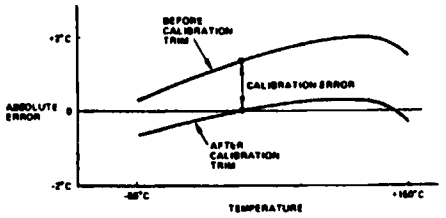


Figure 5. Effect of Scale Factor Trim on Accuracy

ERROR VERSUS TEMPERATURE: NO USER TRIMS

Using the AD590 by simply measuring the current, the total error is the "variance from PTAT" described above plus the effect of the calibration error over temperature. For example the AD590L maximum total error varies from 2.33°C at -55°C to 3.02°C at 150°C. For simplicity, only the larger figure is shown on the specification page.

NONLINEARITY

Nonlinearity as it applies to the AD590 is the maximum deviation of current over temperature from a best-fit straight line. The nonlinearity of the AD590 over the -55°C to +150°C range is superior to all conventional electrical temperature sensors such as thermocouples, RTD's and thermistors. Figure 6 shows the nonlinearity of the typical AD590K from Figure 5.

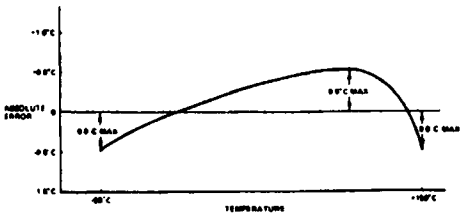


Figure 6. Nonlinearity

Figure 7A shows a circuit in which the nonlinearity is the major contributor to error over temperature. The circuit is trimmed by adjusting R_1 for a 0V output with the AD590 at 0°C. R_2 is then adjusted for 10V out with the sensor at 100°C. Other pairs of temperatures may be used with this procedure as long as they are measured accurately by a reference sensor. Note that for +15V output (150°C) the V+ of the op amp must be greater than 17V. Also note that V- should be at least -4V; if V- is ground there is no voltage applied across the device.

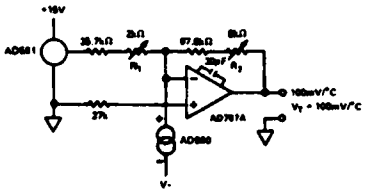


Figure 7A. Two Temperature Trim

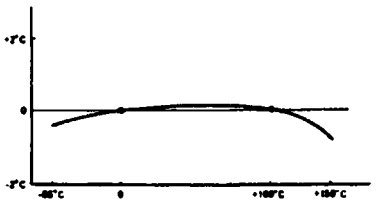


Figure 7B. Typical Two-Trim Accuracy

VOLTAGE AND THERMAL ENVIRONMENT EFFECTS

The power supply rejection specifications show the maximum expected change in output current versus input voltage changes. The insensitivity of the output to input voltage allows the use of unregulated supplies. It also means that hundreds of ohms of resistance (such as a CMOS multiplexer) can be tolerated in series with the device.

It is important to note that using a supply voltage other than 5V does not change the PTAT nature of the AD590. In other words, this change is equivalent to a calibration error and can be removed by the scale factor trim (see previous page).

The AD590 specifications are guaranteed for use in a low thermal resistance environment with 5V across the sensor. Large changes in the thermal resistance of the sensor's environment will change the amount of self-heating and result in changes in the output which are predictable but not necessarily desirable.

The thermal environment in which the AD590 is used determines two important characteristics: the effect of self heating and the response of the sensor with time.

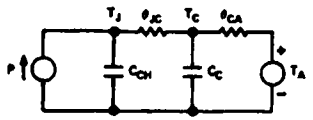


Figure 8. Thermal Circuit Model

Figure 8 is a model of the AD590 which demonstrates these characteristics. As an example, for the TO-52 package, θ_{JC} is the thermal resistance between the chip and the case, about 26°C/watt. θ_{CA} is the thermal resistance between the case and its surroundings and is determined by the characteristics of the thermal connection. Power source P represents the power dissipated on the chip. The rise of the junction temperature, T_J, above the ambient temperature T_A is:

$$T_J - T_A = P(\theta_{JC} + \theta_{CA}). \qquad \text{Eq. 1}$$

Table I gives the sum of θ_{JC} and θ_{CA} for several common thermal media for both the "H" and "F" packages. The heatsink used was a common clip-on. Using Equation 1, the temperature rise of an AD590 "H" package in a stirred bath at +25°C, when driven with a 5V supply, will be 0.06°C. However, for the same conditions in still air the temperature rise is 0.72°C. For a given supply voltage, the temperature rise varies with the current and is PTAT. Therefore, if an application circuit is trimmed with the sensor in the same thermal environment in which it will be used, the scale factor trim compensates for this effect over the entire temperature range.

MEDIUM	$\theta_{JC} + \theta_{CA}$ (°C/watt)		τ (sec) (Note 3)	
	H	F	H	F
Aluminum Block	30	10	0.6	0.1
Stirred Oil[1]	42	60	1.4	0.6
Moving Air[2]				
With Heat Sink	45	–	5.0	–
Without Heat Sink	115	190	13.5	10.0
Still Air				
With Heat Sink	191	–	108	–
Without Heat Sink	480	650	60	30

[1] Note: τ is dependent upon velocity of oil; average of several velocities listed above.
[2] Air velocity ≈ 9ft/sec.
[3] The time constant is defined as the time required to reach 63.2% of an instantaneous temperature change.

Table I. Thermal Resistances

The time response of the AD590 to a step change in temperature is determined by the thermal resistances and the thermal capacities of the chip, C_{CH}, and the case, C_C. C_{CH} is about 0.04 watt-sec/°C for the AD590. C_C varies with the measured medium since it includes anything that is in direct thermal contact with the case. In most cases, the single time constant exponential curve of Figure 9 is sufficient to describe the time response, T(t). Table I shows the effective time constant, τ, for several media.

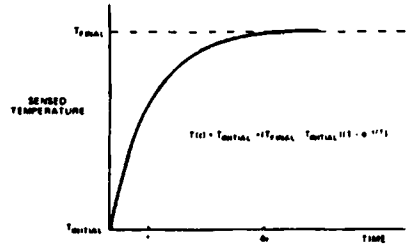


Figure 9. Time Response Curve

GENERAL APPLICATIONS

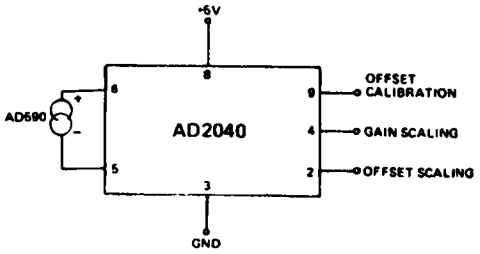


Figure 10 Variable Scale Display

Figure 10 demonstrates the use of a low-cost Digital Panel Meter for the display of temperature on either the Kelvin, Celsius or Fahrenheit scales. For Kelvin temperature Pins 9, 4 and 2 are grounded, and for Fahrenheit temperature Pins 4 and 2 are left open.

The above configuration yields a 3 digit display with 1°C or 1°F resolution, in addition to an absolute accuracy of ±2.0°C over the -55°C to +125°C temperature range if a one-temperature calibration is performed on an AD590K, L, or M.

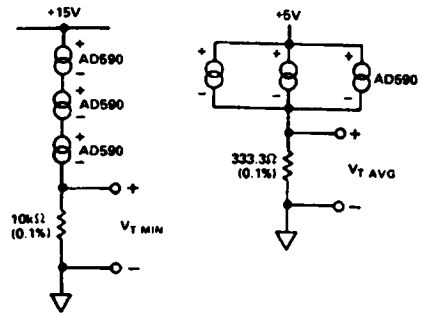


Figure 11. Series & Parallel Connection

Connecting several AD590 units in series as shown in Figure 11 allows the minimum of all the sensed temperatures to be indicated. In contrast, using the sensors in parallel yields the average of the sensed temperatures.

The circuit of Figure 12 demonstrates one method by which differential temperature measurements can be made. R_1 and R_2 can be used to trim the output of the op amp to indicate

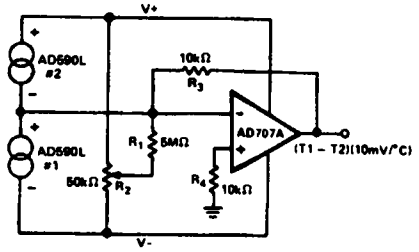


Figure 12. Differential Measurements

a desired temperature difference. For example, the inherent offset between the two devices can be trimmed in. If V+ and V- are radically different, then the difference in internal dissipation will cause a differential internal temperature rise. This effect can be used to measure the ambient thermal resistance seen by the sensors in applications such as fluid level detectors or anemometry.

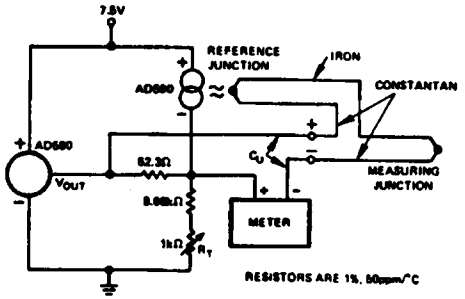


Figure 13. Cold Junction Compensation Circuit for Type J Thermocouple

Figure 13 is an example of a cold junction compensation circuit for a Type J Thermocouple using the AD590 to monitor the reference junction temperature. This circuit replaces an ice-bath as the thermocouple reference for ambient temperatures between +15°C and +35°C. The circuit is calibrated by adjusting R_T for a proper meter reading with the measuring junction at a known reference temperature and the circuit near +25°C. Using components with the T.C.'s as specified in Figure 13, compensation accuracy will be within ±0.5°C for circuit temperatures between +15°C and +35°C. Other thermocouple types can be accommodated with different resistor values. Note that the T.C.'s of the voltage reference and the resistors are the primary contributors to error.

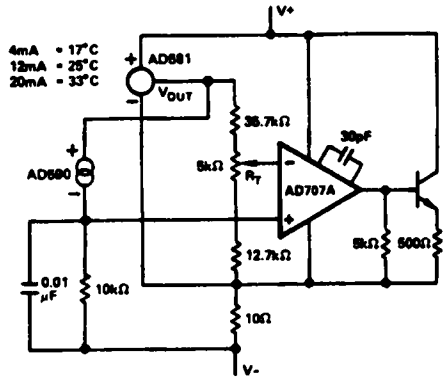


Figure 14. 4 to 20mA Current Transmitter

Figure 14 is an example of a current transmitter designed to be used with 40V, 1kΩ systems; it uses its full current range of 4mA to 20mA for a narrow span of measured temperatures. In this example the 1µA/K output of the AD590 is amplified to 1mA/°C and offset so that 4mA is equivalent to 17°C and 20mA is equivalent to 33°C. R_T is trimmed for proper reading at an intermediate reference temperature. With a suitable choice of resistors, any temperature range within the operating limits of the AD590 may be chosen.

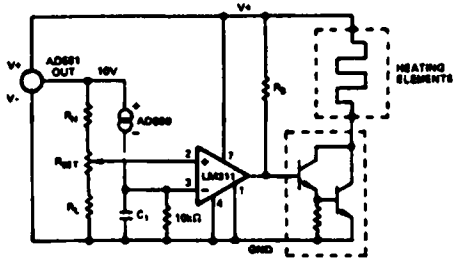


Figure 15. Simple Temperature Control Circuit

Figure 15 is an example of a variable temperature control circuit (thermostat) using the AD590. R_H and R_L are selected to set the high and low limits for R_{SET}. R_{SET} could be a simple pot, a calibrated multi-turn pot or a switched resistive divider. Powering the AD590 from the 10V reference isolates the AD590 from supply variations while maintaining a reasonable voltage (~7V) across it. Capacitor C_1 is often needed to filter extraneous noise from remote sensors. R_B is determined by the β of the power transistor and the current requirements of the load.

Figure 16 shows how the AD590 can be configured with an 8-bit DAC to produce a digitally controlled set point. This

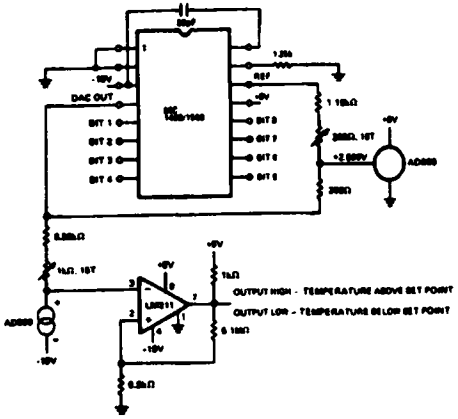


Figure 16. DAC Set Point

particular circuit operates from 0 (all inputs high) to +51°C (all inputs low) in 0.2°C steps. The comparator is shown with 1°C hysteresis which is usually necessary to guard-band for extraneous noise; omitting the 5.1MΩ resistor results in no hysteresis.

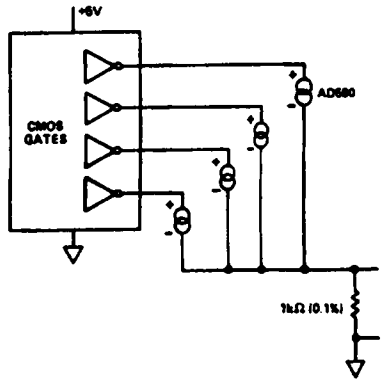


Figure 17. AD590 Driven from CMOS Logic

The voltage compliance and the reverse blocking characteristic of the AD590 allows it to be powered directly from +5V CMOS logic. This permits easy multiplexing, switching or pulsing for minimum internal heat dissipation. In Figure 17 any AD590 connected to a logic high will pass a signal current through the current measuring circuitry while those connected to a logic zero will pass insignificant current. The outputs used to drive the AD590's may be employed for other purposes, but the additional capacitance due to the AD590 should be taken into account.

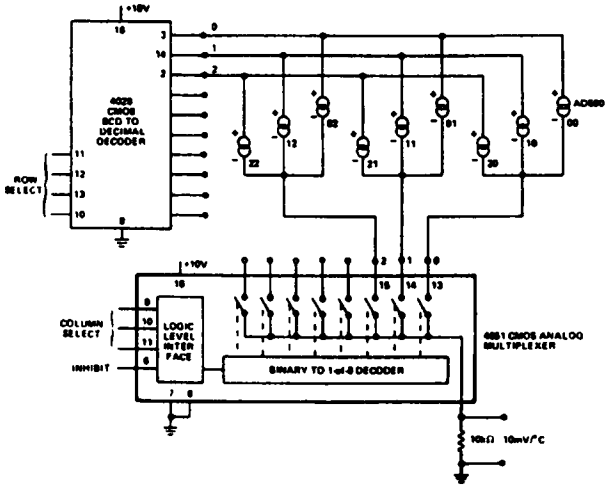


Figure 18. Matrix Multiplexer

CMOS Analog Multiplexers can also be used to switch AD590 current. Due to the AD590's current mode, the resistance of such switches is unimportant as long as 4V is maintained across the transducer. Figure 18 shows a circuit which combines the principal demonstrated in Figure 17 with an 8 channel CMOS Multiplexer. The resulting circuit can select one of eighty sensors over only 18 wires with a 7 bit binary word. The inhibit input on the multiplexer turns all sensors off for minimum dissipation while idling.

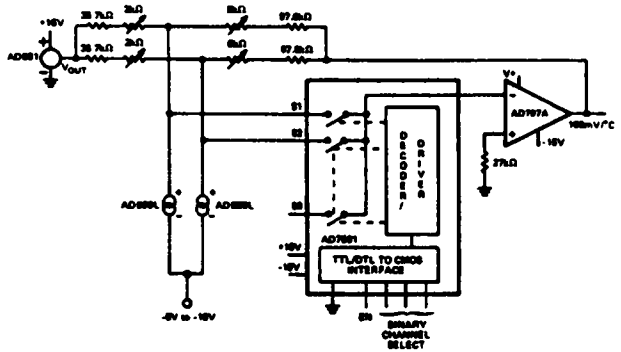


Figure 19. 8-Channel Multiplexer

Figure 19 demonstrates a method of multiplexing the AD590 in the two-trim mode (Figure 7). Additional AD590's and their associated resistors can be added to multiplex up to 8 channels of ±0.5°C absolute accuracy over the temperature range of −55°C to +125°C. The high temperature restriction of +125°C is due to the output range of the op amps; output to +150°C can be achieved by using a +20V supply for the op amp.

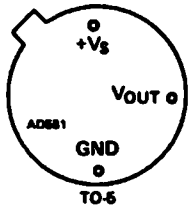
ANALOG DEVICES

High Precision 10V IC Reference

AD581*

FEATURES
- Laser-Trimmed to High Accuracy:
  - 10.000 Volts ±5mV (L and U)
- Trimmed Temperature Coefficient:
  - 5ppm/°C max, 0 to +70°C (L)
  - 10ppm/°C max, −55°C to +125°C (U)
- Excellent Long-Term Stability:
  - 25ppm/1000 hrs. (Noncumulative)
- Negative 10 Volt Reference Capability
- Low Quiescent Current: 1.0mA max
- 10mA Current Output Capability
- 3-Terminal TO-5 Package
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



TO-5

BOTTOM VIEW

PRODUCT DESCRIPTION

The AD581 is a three terminal, temperature compensated, monolithic band-gap voltage reference which provides a precise 10.00 volt output from an unregulated input level from 12 to 30 volts. Laser Wafer Trimming (LWT) is used to trim both the initial error at +25°C as well as the temperature coefficient, which results in high precision performance previously available only in expensive hybrids or oven-regulated modules. The 5mV initial error tolerance and 5ppm/°C guaranteed temperature coefficient of the AD581L represent the best performance combination available in a monolithic voltage reference.

The band-gap circuit design used in the AD581 offers several advantages over classical Zener breakdown diode techniques. Most important, no external components are required to achieve full accuracy and stability of significance to low power systems. In addition, total supply current to the device, including the output buffer amplifier (which can supply up to 10mA) is typically 750μA. The long-term stability of the band-gap design is equivalent or superior to selected Zener reference diodes.

The AD581 is recommended for use as a reference for 8-, 10- or 12-bit D/A converters which require an external precision reference. The device is also ideal for all types of A/D converters up to 14 bit accuracy, either successive approximation or integrating designs, and in general can offer better performance than that provided by standard self-contained references.

The AD581J, K, and L are specified for operation from 0 to +70°C, the AD581S, T, and U are specified for the −55°C to +125°C range. All grades are packaged in a hermetically-sealed three-terminal TO-5 metal can.

PRODUCT HIGHLIGHTS

1. Laser trimming of both initial accuracy and temperature coefficient results in very low errors over temperature without the use of external components. The AD581L has a maximum deviation from 10.000 volts of ±7.25mV from 0 to +70°C, while the AD581U guarantees ±15mV maximum total error without external trims from −55°C to +125°C.
2. Since the laser trimming is done on the wafer prior to separation into individual chips, the AD581 will be extremely valuable to hybrid designers for its ease of use, lack of required external trims, and inherent high performance.
3. The AD581 can also be operated in a two-terminal "Zener" mode to provide a precision negative 10 volt reference with just one external resistor to the unregulated supply. The performance in this mode is nearly equal to that of the standard three-terminal configuration.
4. Advanced circuit design using the band-gap concept allows the AD581 to give full performance with an unregulated input voltage down to 13 volts. With an external resistor, the device will operate with a supply as low as 11.4 volts.
5. The AD581 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD581/883B data sheet for detailed specifications.

AD581—SPECIFICATIONS (@ V_{IN} = +15V and 25°C)

Model	AD581J Min	AD581J Typ	AD581J Max	AD581K Min	AD581K Typ	AD581K Max	AD581L Min	AD581L Typ	AD581L Max	Units
OUTPUT VOLTAGE TOLERANCE (Error from nominal 10,000V output)			±30			±10			±5	mV
OUTPUT VOLTAGE CHANGE										
Maximum Deviation from +25°C			±13.5			±6.75			±2.25	mV
Value, T_{min} to T_{max} (Temperature Coefficient)			30			15			5	ppm/°C
LINE REGULATION										
15V≤V_{IN}≤30V			3.0 (0.002)			3.0 (0.002)			3.0 (0.002)	mV %/V
13V≤V_{IN}≤15V			1.0 (0.005)			1.0 (0.005)			1.0 (0.005)	mV %/V
LOAD REGULATION 0≤I_{OUT}≤5mA		200	500		200	500		200	500	μV/mA
QUIESCENT CURRENT		0.75	1.0		0.75	1.0		0.75	1.0	mA
TURN-ON SETTLING TIME TO 0.1%[1]		200			200			200		μs
NOISE (0.1 to 10Hz)		40			40			40		μV/p-p
LONG-TERM STABILITY		25			25			25		ppm/1000 hrs.
SHORT-CIRCUIT CURRENT		30			30			30		mA
OUTPUT CURRENT										
Source @ +25°C	10			10			10			mA
Source T_{min} to T_{max}	5			5			5			mA
Sink T_{min} to T_{max}	5			5			5			μA
Sink −55°C to +85°C	–			–			–			mA
TEMPERATURE RANGE										
Specified	0		+70	0		+70	0		+70	°C
Operating	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTION[2] TO-5 (H-03B)		AD581JH			AD581KH			AD581LH		

Model	AD581S Min	AD581S Typ	AD581S Max	AD581T Min	AD581T Typ	AD581T Max	AD581U Min	AD581U Typ	AD581U Max	Units
OUTPUT VOLTAGE TOLERANCE (Error from nominal 10,000V output)			±30			±10			±5	mV
OUTPUT VOLTAGE CHANGE										
Maximum Deviation from +25°C			±30			±15			±10	mV
Value, T_{min} to T_{max} (Temperature Coefficient)			30			15			10	ppm/°C
LINE REGULATION										
15V≤V_{IN}≤30V			3.0 (0.002)			3.0 (0.002)			3.0 (0.002)	mV %/V
13V≤V_{IN}≤15V			1.0 (0.005)			1.0 (0.005)			1.0 (0.005)	mV %/V
LOAD REGULATION 0≤I_{OUT}≤5mA		200	500		200	500		200	500	μV/mA
QUIESCENT CURRENT		0.75	1.0		0.75	1.0		0.75	1.0	mA
TURN-ON SETTLING TIME TO 0.1%[1]		200			200			200		μs
NOISE (0.1 to 10Hz)		40			40			40		μV/p-p
LONG-TERM STABILITY		25			25			25		ppm/1000 hrs.
SHORT-CIRCUIT CURRENT		30			30			30		mA
OUTPUT CURRENT										
Source @ +25°C	10			10			10			mA
Source T_{min} to T_{max}	5			5			5			mA
Sink T_{min} to T_{max}	200			200			200			μA
Sink −55°C to +85°C	5			5			5			mA
TEMPERATURE RANGE										
Specified	−55		+125	−55		+125	−55		+125	°C
Operating	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTION[2] TO-5 (H-03B)		AD581SH			AD581TH			AD581UH		

NOTES
[1]See Figure 7.
[2]H = Hermetic Metal Can. For outline information see Package Information section.
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Input Voltage V_{IN} to Ground	40V
Power Dissipation @ +25°C	600mW
Operating Junction Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C
Thermal Resistance	
Junction-to-Ambient	150°C/W

APPLYING THE AD581

The AD581 is easy to use in virtually all precision reference applications. The three terminals are simply primary supply, ground, and output, with the case grounded. No external components are required even for high precision applications; the degree of desired absolute accuracy is achieved simply by selecting the required device grade. The AD581 requires less than 1mA quiescent current from an operating supply range of 12 to 30 volts.

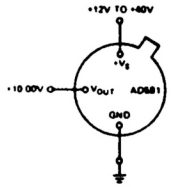


Figure 1. AD581 Pin Configuration (Top View)

An external fine trim may be desired to set the output level to exactly 10.000 volts within less than a millivolt (calibrated to a main system reference). System calibration may also require a reference slightly different from 10.00 volts. In either case, the optional trim circuit shown in Figure 2 can offset the output by up to ±30 millivolts (with the 22Ω resistor), if needed, with minimal effect on other device characteristics.

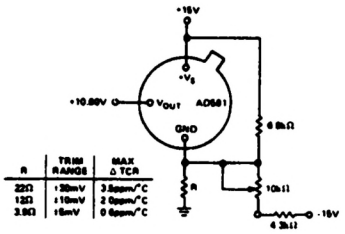


Figure 2. Optional Fine Trim Configuration

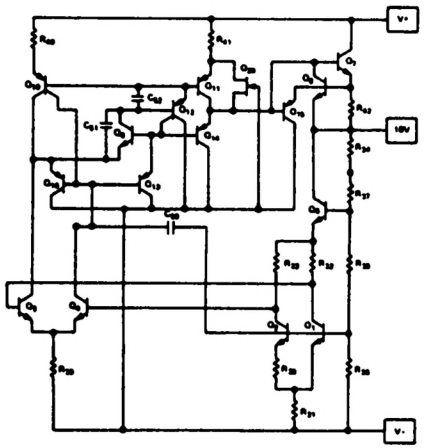


Figure 3. Simplified Schematic

VOLTAGE VARIATION vs. TEMPERATURE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references have been characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of nonlinearities in temperature characteristics, which originated in standard Zener references (such as "S" type characteristics) most manufacturers have begun to use a maximum limit error band approach to specify devices. This technique involves measurement of the output at 3, 5 or more different temperatures to guarantee that the output voltage will fall within the given error band. The temperature characteristic of the AD581 consistently follows the S-curve shown in Figure 4. Three-point measurement of each device guarantees the error band over the specified temperature range.

The error band which is guaranteed with the AD581 is the maximum deviation from the initial value at +25°C; this error band is of more use to a designer than one which simply guarantees the maximum total change over the entire range (i.e., in the latter definition, all of the changes could occur in the positive direction). Thus, with a given grade of the AD581, the designer can easily determine the maximum total error from initial tolerance plus temperature variation (e.g., for the AD581T, the initial tolerance is ±10mV, the temperature error band is ±15mV, thus the unit is guaranteed to be 10.000 volts ±25mV from -55°C to +125°C).

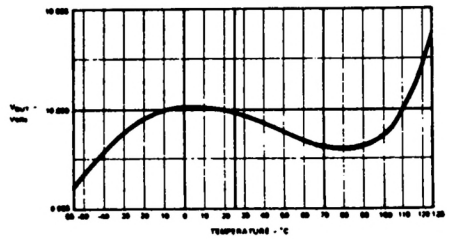


Figure 4. Typical Temperature Characteristic

OUTPUT CURRENT CHARACTERISTICS

The AD581 has the capability to either source or sink current and provide good load regulation in either direction, although it has better characteristics in the source mode (positive current into the load). The circuit is protected for shorts to either positive supply or ground. The output voltage vs. output current characteristics of the device are shown in Figure 5. Source current is displayed as negative current in the figure; sink current is positive. Note that the short circuit current (i.e., zero volts output) is about 28mA; when shorted to +15 volts, the sink current goes to about 20mA.

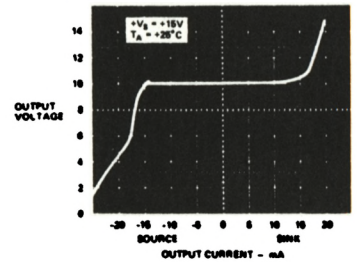


Figure 5. AD581 Output Voltage vs. Sink and Source Current

DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for operation. Figure 6 displays the turn-on characteristic of the AD581. This characteristic is generated from cold-start operation and represents the true turn-on waveform after an extended period with the supplies off. The figure shows both the coarse and fine transient characteristics of the device; the total settling time to within ±10 millivolt is about 180μs, and there is no long thermal tail appearing after the point.

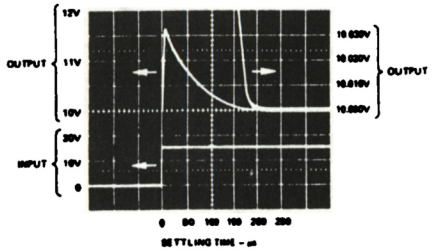


Figure 6. Output Settling Characteristic

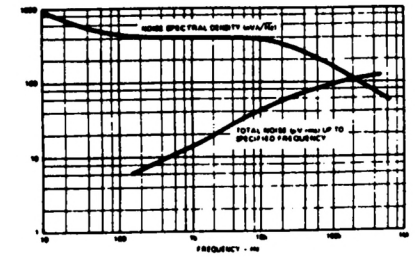


Figure 7. Spectral Noise Density and Total rms Noise vs. Frequency

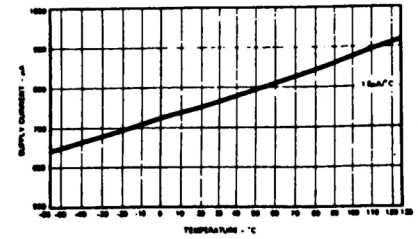


Figure 8. Quiescent Current vs. Temperature

PRECISION HIGH CURRENT SUPPLY

The AD581 can be easily connected with power pnp or power darlington pnp devices to provide much greater output current capability. The circuit shown in Figure 9 delivers a precision 10 volt output with up to 4 amperes supplied to the load. The 0.1μF capacitor is required only if the load has a significant capacitive component. If the load is purely resistive, improved high frequency supply rejection results from removing the capacitor.

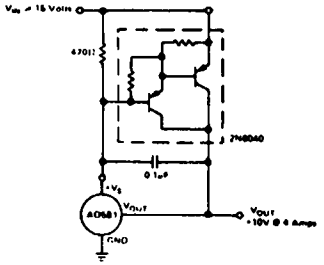


Figure 9. High Current Precision Supply

CONNECTION FOR REDUCED PRIMARY SUPPLY

While line regulation is specified down to 13 volts, the typical AD581 will work as specified down to 12 volts or below. The current sink capability allows even lower supply voltage capability such as operation from 12V ±5% as shown in Figure 10. The 560Ω resistor reduces the current supplied by the AD581 to a manageable level at full 5mA load. Note that the other bandgap references, without current sink capability, may be damaged by use in this circuit configuration.

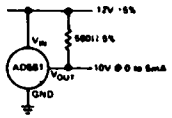


Figure 10. 12-Volt Supply Connection

THE AD581 AS A CURRENT LIMITER

The AD581 represents an alternative to current limiter diodes which require factory selection to achieve a desired current. This approach often results in temperature coefficients of 1%/°C. The AD581 approach is not limited to a defined set current limit; it can be programmed from 0.75 to 5mA with the insertion of a single external resistor. Of course, the minimum voltage required to drive the connection is 13 volts. The AD580, which is a 2.5 volt reference, can be used in this type of circuit with compliance voltage down to 4.5 volts.

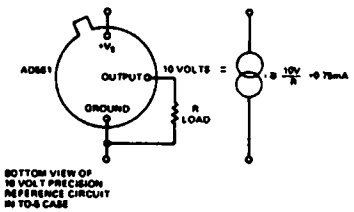


Figure 11. A Two-Component Precision Current Limiter

NEGATIVE 10-VOLT REFERENCE

The AD581 can also be used in a two-terminal "Zener" mode to provide a precision -10.00 volt reference. As shown in Figure 13, the V_{IN} and V_{OUT} terminals are connected together to the high supply (in this case, ground). The ground pin is connected through a resistor to the negative supply. The output is now taken from the ground pin instead of V_{OUT}. With 1mA flowing through the AD581 in this mode, a typical unit will show a 2mV increase in output level over that produced in the three-terminal mode. Note also that the effective output impedance in this connection increases from 0.2Ω typical to 2 ohms. It is essential to arrange the output load and the supply resistor, R_S, so that the net current through the AD581 is always between 1 and 5mA. For operation to +125°C, the net current should be between 2 and 5mA. The temperature characteristics and long-term stability of the device will be essentially the same as that of a unit used in the standard three-terminal mode.

The AD581 can also be used in a two-terminal mode to develop a positive reference. V_{IN} and V_{OUT} are tied together and to the positive supply through an appropriate supply resistor. The performance characteristics will be similar to those of the negative two-terminal connection. The only advantage of this connection over the standard three-terminal connection is that a lower primary supply can be used, as low as 10.5 volts. This type of operation will require considerable attention to load and primary supply regulation to be sure the AD581 always remains within its regulating range of 1 to 5mA (2 to 5mA for operation beyond +85°C).

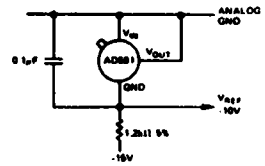


Figure 12. Two-Terminal – 10 Volt Reference

10 VOLT REFERENCE WITH MULTIPLYING CMOS D/A OR A/D CONVERTERS

The AD581 is ideal for application with the entire AD7533 series of 10- and 12-bit multiplying CMOS D/A converters, especially for low power applications. It is equally suitable for the AD7574 8-bit A/D converter. In the standard hook-up, as shown in Figure 14, the +10 volt reference is inverted by the amplifier/DAC configuration to produce a 0 to -10 volt range. If an AD308 amplifier is used, total quiescent supply current will typically be 2mA. If a 0 to +10 volt full scale range is desired, the AD581 can be connected to the CMOS DAC in its -10 volt "Zener" mode, as shown in Figure 12 (the $-10V_{REF}$ output is connected directly to the $V_{REF\,IN}$ of the CMOS DAC). The AD581 will normally be used in the -10 volt mode with the AD7574 to give a 0 to +10 volt ADC range. This is shown in Figure 14. Bipolar output applications and other operating details can be found in the data sheets for the CMOS products.

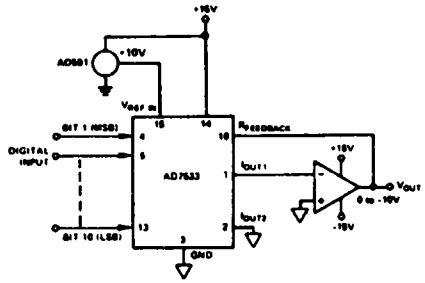


Figure 13. Low Power 10-Bit CMOS DAC Application

PRECISION 12-BIT D/A CONVERTER REFERENCE

The AD562, like most D/A converters, is designed to operate with a +10 volt reference element. In the AD562, this 10 volt reference voltage is converted into a reference current of approximately 0.5mA via the internal 19.95kΩ resistor (in series with the external 100Ω trimmer). The gain temperature coefficient of the AD562 is primarily governed by the temperature tracking of the 19.95kΩ resistor and the 5k/10k span resistors; this gain T.C. is guaranteed to 3ppm/°C. Thus, using the AD581L (at 5ppm/°C) as the 10 volt reference guarantees a maximum full scale temperature coefficient of 8ppm/°C over the commercial range. The 10 volt reference also supplies the normal 1mA bipolar offset current through the 9.95k bipolar offset resistor. The bipolar offset T.C. thus depends only on the T.C. matching of the bipolar offset resistor to the input reference resistor and is guaranteed to 3ppm/°C.

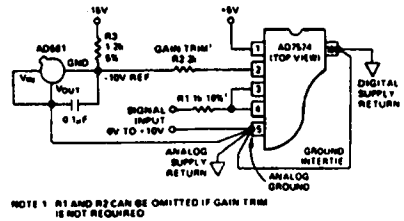


Figure 14. AD581 as Negative 10-Volt Reference for CMOS ADC

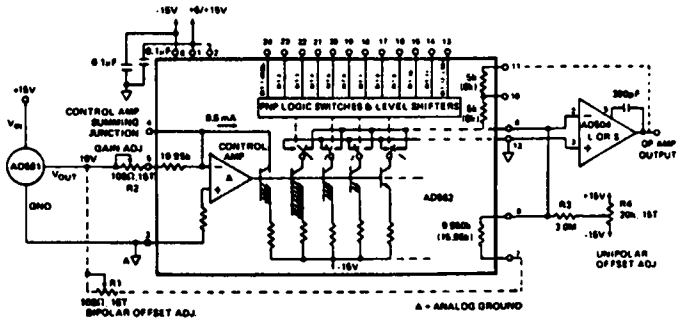


Figure 15. Precision 12-Bit D/A Converter

PRELIMINARY IND

PALCE22V10Z-25

Zero-Power 24-Pin EE CMOS Versatile PAL Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Zero-power CMOS technology
  - 15 µA standby current
  - 25 ns first-access propagation delay
- Unused product term disable for reduced power consumption
- Industrial Operating Range
  - T_C = –45°C to +85°C
  - V_{CC} = +4.5 V to +5.5 V
- HC- and HCT-compatible inputs and outputs
- Electrically-erasable technology provides reconfigurable logic and full testability
- 10 macrocells programmable as registered or combinatorial, and active high or active low to match application needs
- Varied product term distribution allows up to 16 product terms per output for complex functions
- Global asynchronous reset and synchronous preset for initialization
- Power-up reset for initialization and register preload for testability
- Extensive third-party software and programmer support through FusionPLD partners
- 24-pin SKINNYDIP and 28-pin PLCC packages save space

GENERAL DESCRIPTION

The PALCE22V10Z is an advanced PAL device built with zero-power, high-speed, electrically-erasable CMOS technology. It provides user-programmable logic for replacing conventional zero-power CMOS SSI/MSI gates and flip-flops at a reduced chip count.

The PALCE22V10Z provides zero standby power and high speed. At 15 µA maximum standby current, the PALCE22V10Z allows battery powered operation for an extended period.

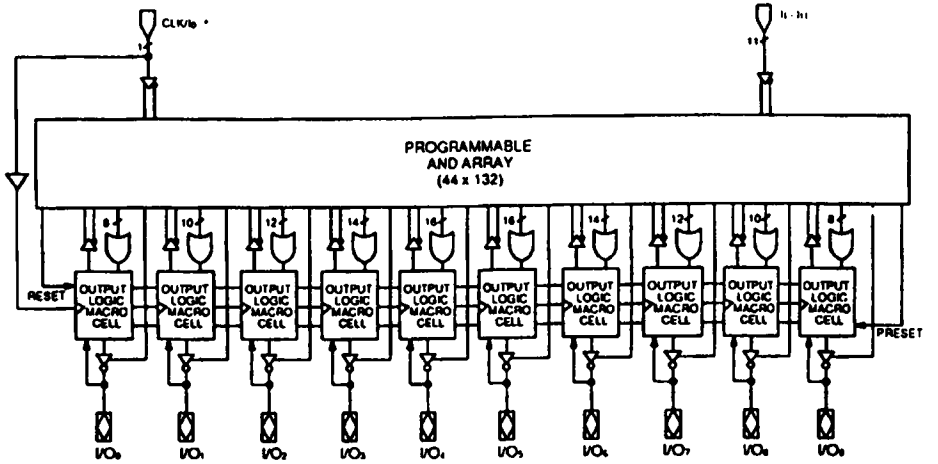
The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

The product terms are connected to the fixed OR array with a varied distribution from 8 to 16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, and active high or active low. The output configuration is determined by two bits controlling two multiplexers in each macrocell.

AMD's FusionPLD program allows PALCE22V10Z designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the PLD Software Reference Guide for certified development systems and the Programmer Reference Guide for approved programmers.

Publication# 15700 Rev. A Amendment/0
Issue Date: January 1992

BLOCK DIAGRAM

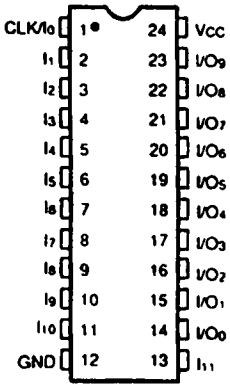


09849-001A

CONNECTION DIAGRAMS

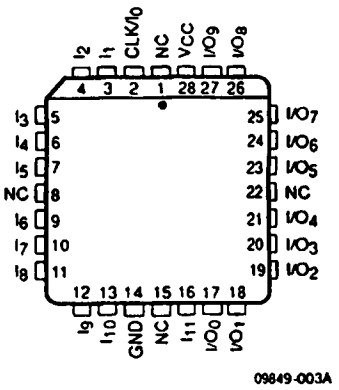
Top View

SKINNYDIP



09849-002A

PLCC



09849-003A

Note:

Pin 1 is marked for orientation.

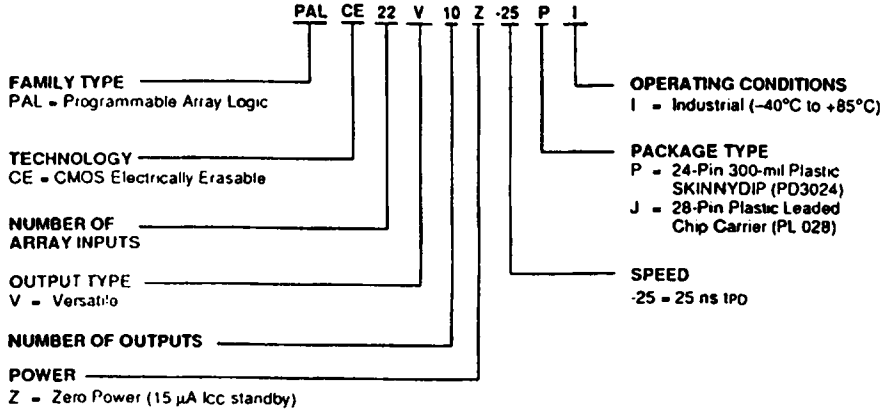
PIN DESCRIPTION

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
Vcc	=	Supply Voltage

ORDERING INFORMATION

Industrial Products

AMD programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of these elements:



Valid Combinations	
PALCE22V10Z-25	PI, JI

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The PALCE22V10Z is the zero-power version of the PALCE22V10. It has all the architectural features of the PALCE22V10. In addition, the PALCE22V10Z has zero standby power and unused product term disable.

The PALCE22V10Z allows the systems engineer to implement the design on-chip, by programming EE cells to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state.

The PALCE22V10Z has 12 inputs and 10 I/O macrocells. The macrocell (Figure 1) allows one of four potential output configurations: registered output or combinatorial I/O, active high or active low (see Figure 2). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits S_0 - S_1. Multiplexer controls are connected to ground (0) through a programmable bit, selecting the "0" path through the multiplexer. Erasing the bit disconnects the control line from GND and it floats to Vcc (1), selecting the "1" path.

The device is produced with a EE cell link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern.

Variable Input/Output Pin Ratio

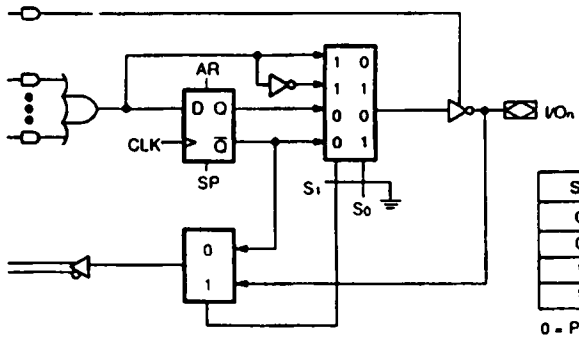
The PALCE22V10Z has twelve dedicated input lines, and each macrocell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to Vcc or GND.

Registered Output Configuration

Each macrocell of the PALCE22V10Z includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration (S_1 = 0), the array feedback is from $\overline{Q}$ of the flip-flop.

Combinatorial I/O Configuration

Any macrocell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop (S_1 = 1). In the combinatorial configuration the feedback is from the pin.



S_1	S_0	Output Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

0 = Programmed EE bit
1 = Erased (charged) EE bit

09849-004A

Figure 1. Output Logic Macrocell

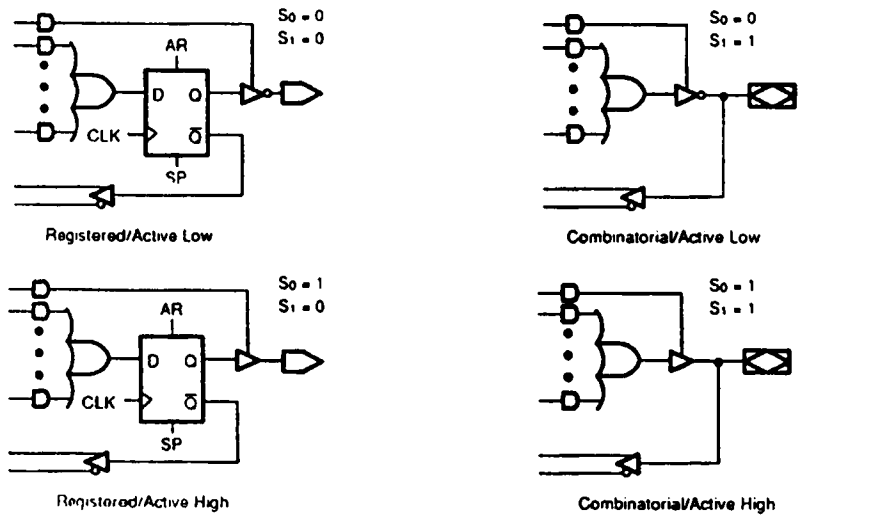


Figure 2. Macrocell Configuration Options

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be active high ($S_0 = 1$).

Preset/Reset

For initialization, the PALCE22V10Z has additional Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Zero-Standby Power Mode

The PALCE22V10Z features a zero-standby power mode. When none of the inputs switch for an extended period (typically 50 ns), the PALCE22V10Z will go into standby mode, shutting down most of its internal circuitry. The current will go to almost zero ($I_{CC} < 15\ \mu A$). The outputs will maintain the states held before the device went into the standby mode.

When any input switches, the internal circuitry is fully enabled and power consumption returns to normal. This feature results in considerable power savings for operation at low to medium frequencies. This savings is illustrated in the I_{CC} vs. frequency graphs.

Product-Term Disable

On a programmed PALCE22V10Z, any product terms that are not used are disabled. Power is cut off from these product terms so that they do not draw current. As shown in the I_{CC} vs. frequency graphs, product-term disabling results in considerable power savings. This savings is greater at the higher frequencies.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PALCE22V10Z will depend on the programmed output polarity. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The registers on the PALCE22V10Z can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

After programming and verification, a PALCE22V10Z design can be secured by programming the security EE bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security bit is programmed, the array will read as if every bit is erased, and preload will be disabled.

The bit can only be erased in conjunction with erasure of the entire pattern.

Programming and Erasing

The PALCE22V10Z can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

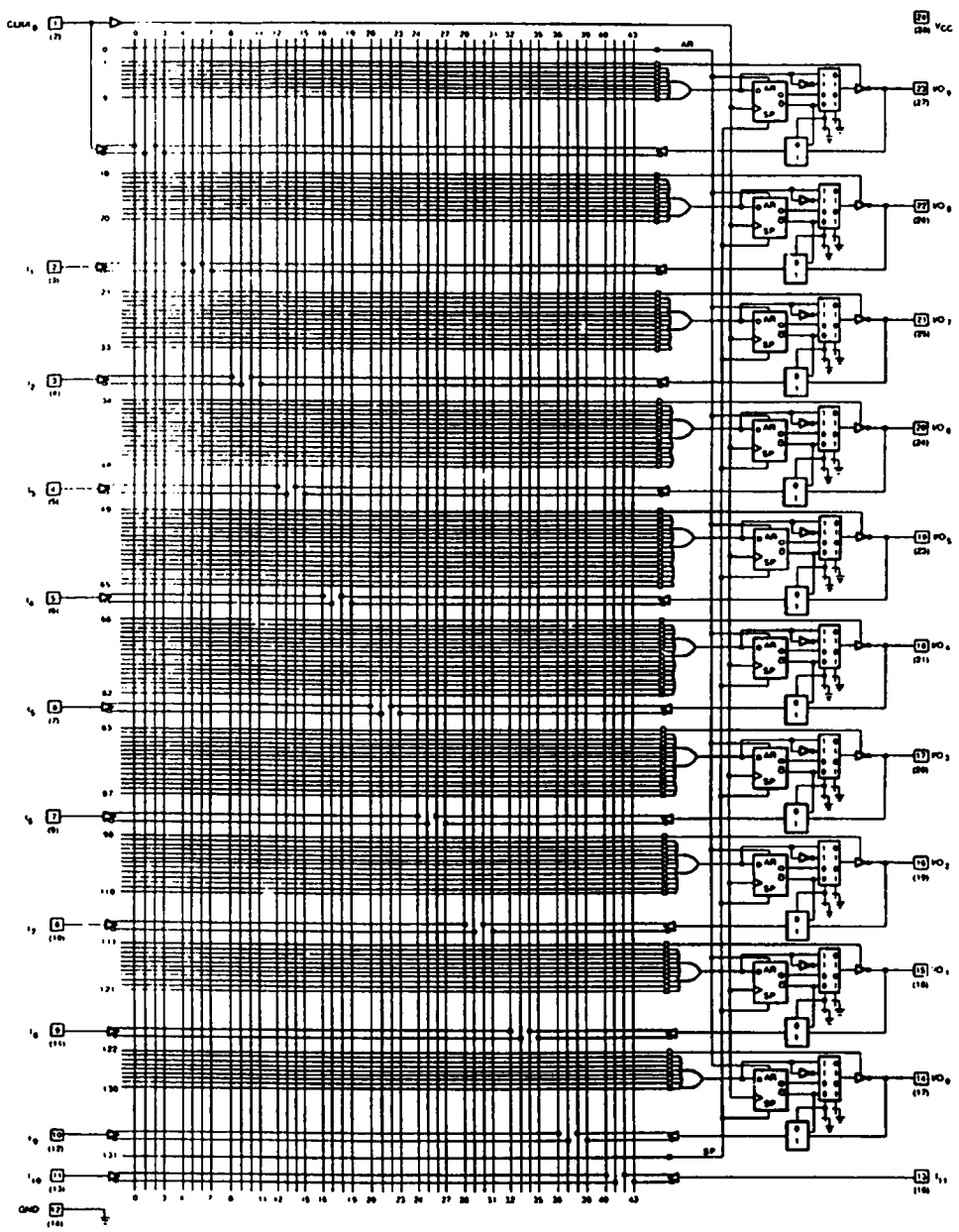
The PALCE22V10Z offers a very high level of built-in quality.

The erasability of the CMOS PALCE22V10Z allows direct testing of the device array to guarantee 100% programming and functional yields.

Technology

The high-speed PALCE22V10Z is fabricated with AMD's advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with HC and HCT devices. This technology provides strong input-clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM
SKINNYDIP (PLCC) Pinouts



09849-006A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to Vcc + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to Vcc + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (TA = 0°C to +75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Industrial (I) Devices

Operating Case Temperature (Tc)	−45°C to +85°C
Supply Voltage (Vcc) with Respect to Ground	+4.5 V to +5.5 V

Operating Ranges define those limits between which the functionality of the device is guaranteed

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

PRELIMINARY

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min.	I_{OH} = 6 mA	3.84		V
			I_{OH} = 20 µA	Vcc−0.1		V
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = Min.	I_{OL} = 16 mA		0.5	V
			I_{OL} = 6 mA		0.33	V
			I_{OL} = 20 µA		0.1	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Notes 1, 2)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Notes 1, 2)			0.9	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, Vcc = Max. (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, Vcc = Max. (Note 3)			−10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, Vcc = Max. $V_{IN} = V_{IH}$ or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, Vcc = Max. $V_{IN} = V_{IH}$ or V_{IL} (Note 3)			−10	µA
Isc	Output Short-Circuit Current	V_{OUT} = 0.5 V Vcc = Max. (Note 4)		−30	−150	mA
Icc	Supply Current	Outputs Open (I_{OUT} = 0 mA), Vcc = Max.	f = 0		15	µA
			f = 25 MHz		120	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Represents the worst case of HC and HCT standards, allowing compatibility with either.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

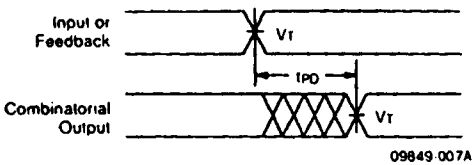
PRELIMINARY

Parameter Symbol	Parameter Description			Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output Input Switching when Device is in Standby Mode				25	ns
	Input Switching when Device is not in Standby Mode				20	ns
t_S	Setup Time from Input, Feedback or SP to Clock			15		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				15	ns
t_{AR}	Asynchronous Reset to Registered Output				25	ns
t_{ARW}	Asynchronous Reset Width			25		ns
t_{ARR}	Asynchronous Reset Recovery Time			25		ns
t_{SPR}	Synchronous Preset Recovery Time			25		ns
t_{WL}	Clock Width	LOW		13		ns
t_{WH}		HIGH		13		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	33.3		MHz
		Internal Feedback (f_{CNT})		35.7		MHz
t_{EA}	Input to Output Enable Using Product Term Control				25	ns
t_{ER}	Input to Output Disable Using Product Term Control				25	ns

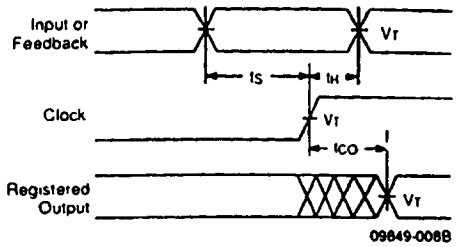
Notes:

2. See Switching Test Circuit for test conditions
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.

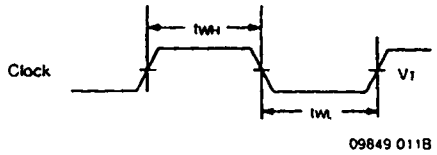
SWITCHING WAVEFORMS



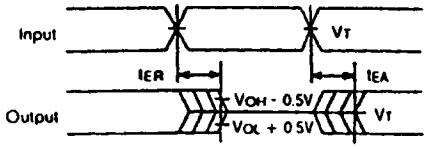
Combinatorial Output



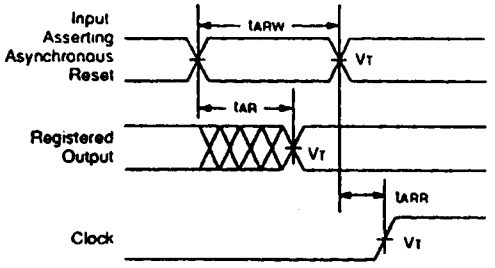
Registered Output



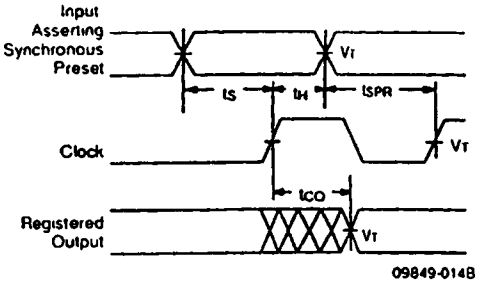
Clock Width



Input to Output Disable/Enable



Asynchronous Reset



Synchronous Preset

Notes:

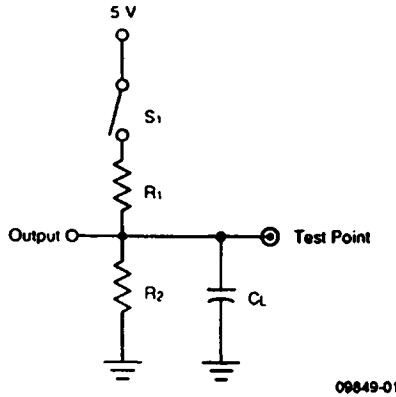
1. $V_T = V_{CC}/2$.
2. Input pulse amplitude 0 V to V_{CC}
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
———	Must be Steady	Will be Steady
———		
⟋⟋⟋	May Change from H to L	Will be Changing from H to L
⟋⟋⟋	May Change from L to H	Will be Changing from L to H
⟋⟍⟋⟍	Don't Care, Any Change Permitted	Changing, State Unknown
⟋⟍ ⟍⟋	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

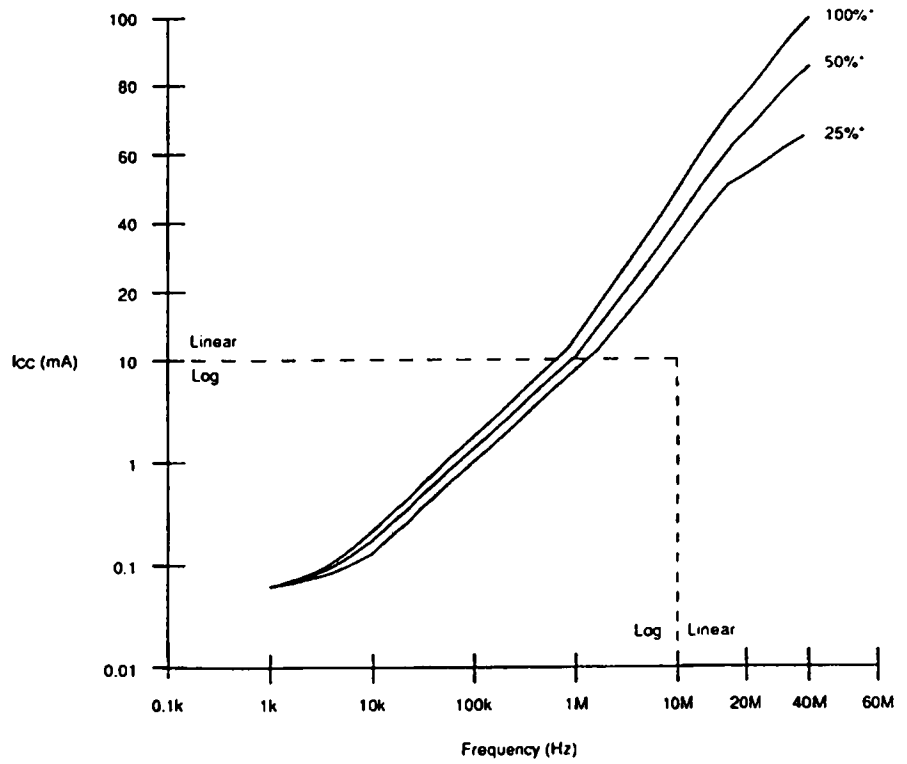
SWITCHING TEST CIRCUIT



09649-015A

Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	30 pF	820 Ω	820 Ω	Vcc/2
t_{EA}	Z → H: Open Z → L: Closed				Vcc/2
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

TYPICAL I_{CC} CHARACTERISTICS
V_{CC} = 5.0 V, T_A = 25°C



15700A-002B

*Percent of product terms used.

Icc vs. Frequency

ENDURANCE CHARACTERISTICS

The PALCE22V10Z is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

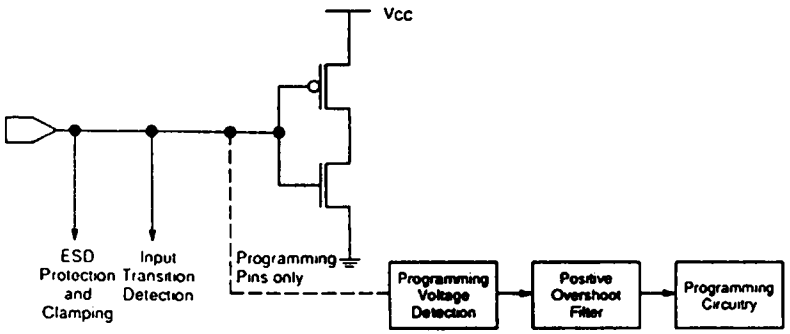
Endurance Characteristics

Symbol	Parameter	Min.	Units	Test Conditions
t_{DR}	Min Pattern Data Retention Time	20	Years	Max. Operating Temperature
N	Min Reprogramming Cycles	100	Cycles	Normal Programming Conditions

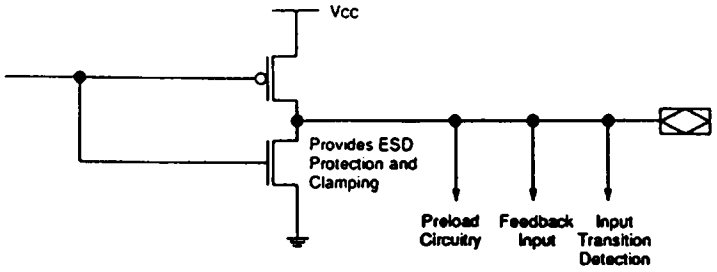
ROBUSTNESS FEATURES

The PALCE22V10Z-25 has some unique features that make it extremely robust, especially when operating in high speed design environments. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

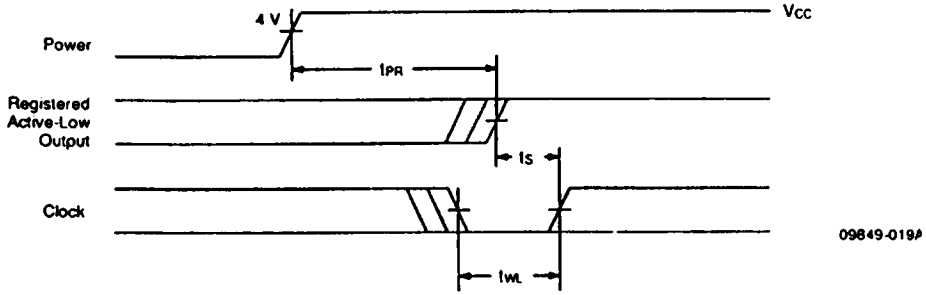
13061B-003A

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways Vcc can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The Vcc rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

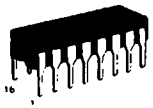
MOTOROLA

MC14060B

14-BIT BINARY COUNTER AND OSCILLATOR

The MC14060B is a 14-stage binary ripple counter with an on-chip oscillator buffer. The oscillator configuration allows design of either RC or crystal oscillator circuits. Also included on the chip is a reset function which places all outputs into the zero state and disables the oscillator. A negative transition on Clock will advance the counter to the next state. Schmitt trigger action on the input line permits very slow input rise and fall times. Applications include time delay circuits, counter controls, and frequency dividing circuits.

- Fully static operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Buffered Outputs Available from Stages 4 Through 10 and 12 Through 14
- Common Reset Line
- Pin for Pin Replacement for CD4060B



L SUFFIX
CERAMIC
CASE 620

P SUFFIX
PLASTIC
CASE 648

D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

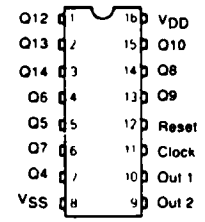
T_A = −55 to 125°C for all packages

TRUTH TABLE

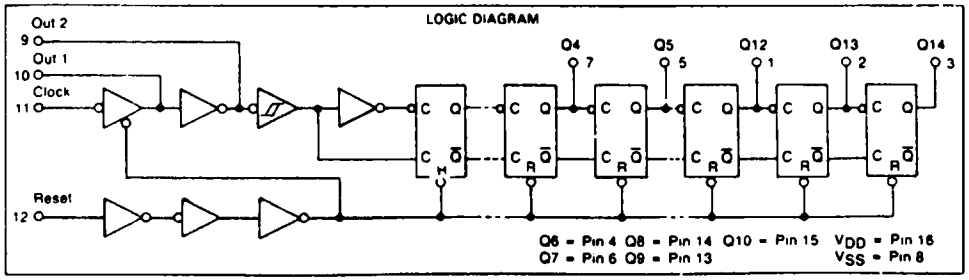
Clock	RESET	Output State
⌐⌐	L	No Change
⌐_	L	Advance to next state
x	H	All Outputs are low

x = Don't Care

PIN ASSIGNMENT



LOGIC DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: All Packages: 7.0 mW/°C from 65°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} V	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	V
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	V
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (V_O = 4.5 or 0.5 V)	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	V
(V_O = 9.0 or 1.0 V)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 V)		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level (V_O = 0.5 or 4.5 V)	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	V
(V_O = 1.0 or 9.0 V)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 V)		15	11.0	—	11.0	8.25	—	11.0	—	
Input Voltage "0" Level (V_O = 4.5 Vdc) (For Input 11	V_{IL}	5.0	—	1.0	—	2.25	1.0	—	1.0	Vdc
(V_O = 9.0 Vdc) and Output 10)		10	—	2.0	—	4.50	2.0	—	2.0	
(V_O = 13.5 Vdc)		15	—	2.5	—	6.75	2.5	—	2.5	
"1" Level (V_O = 0.5 Vdc)	V_{IH}	5.0	4.0	—	4.0	2.75	—	4.0	—	Vdc
(V_O = 1.0 Vdc)		10	8.0	—	8.0	5.50	—	8.0	—	
(V_O = 1.5 Vdc)		15	12.5	—	12.5	8.25	—	12.5	—	
Output Drive Current (V_{OH} = 2.5 V) (Except Source	I_{OH}	5.0	−3.0	—	−2.4	−4.2	—	−1.7	—	mA
(V_{OH} = 4.6 V) Pins 9 and 10)		5.0	−0.64	—	−0.51	−0.88	—	−0.36	—	
(V_{OH} = 9.5 V)		10	−1.6	—	−1.3	−2.25	—	−0.9	—	
(V_{OH} = 13.5 V)		15	−4.2	—	−3.4	−8.8	—	−2.4	—	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mA
(V_{OL} = 0.5 V)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 V)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μA
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current** (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.25 μA/kHz) f + I_{DD}							μA
		10	I_T = (0.54 μA/kHz) f + I_{DD}							
		15	I_T = (0.85 μA/kHz) f + I_{DD}							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time (Counter Outputs)	t_{TLH}	5.0	–	40	200	ns
		10	–	25	100	
		15	–	20	80	
Output Fall Time (Counter Outputs)	t_{THL}	5.0	–	50	200	ns
		10	–	30	100	
		15	–	20	80	
Propagation Delay Time Clock to Q4	t_{PLH} t_{PHL}	5.0	–	415	740	ns
		10	–	175	300	
		15	–	125	200	
Clock to Q14		5.0	–	1.5	2.7	μs
		10	–	0.7	1.3	
		15	–	0.4	1.0	
Clock Pulse Width	t_{WH}	5.0	100	65	–	ns
		10	40	30	–	
		15	30	20	–	
Clock Pulse Frequency	f_ϕ	5.0	–	5	3.5	MHz
		10	–	14	8	
		15	–	17	12	
Clock Rise and Fall Time	t_{TLH} t_{THL}	5.0 10 15	No Limit			ns
Reset Pulse Width	t_w	5.0	120	40	–	ns
		10	60	15	–	
		15	40	10	–	
Propagation Delay Time Reset to Qn	t_{PHL}	5.0	–	170	360	ns
		10	–	80	160	
		15	–	60	100	

#Data labelled Typ is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

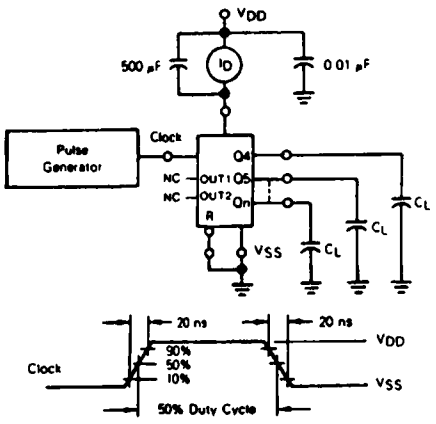


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

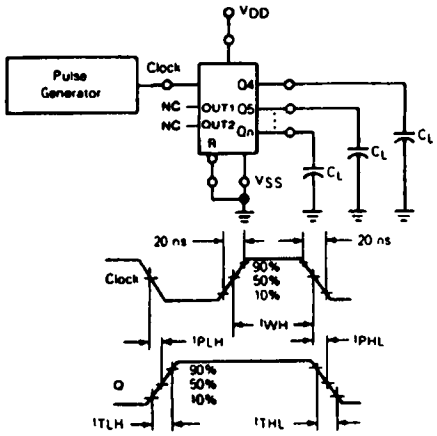
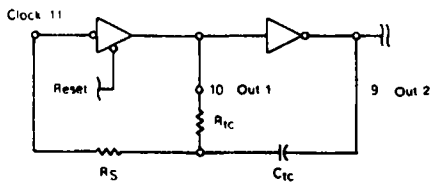


FIGURE 3 – OSCILLATOR CIRCUIT USING RC CONFIGURATION



$$f \approx \frac{1}{2.3\,R_{TC}C_{TC}}$$

for 1 kHz ≤ f ≤ 100 kHz
and $2R_{TC} < R_S < 10R_{TC}$
(f in Hz, R in ohms, C in farads)
The formula may vary for other frequencies. For maximum value for the resistors is 1 MΩ.

TYPICAL RC OSCILLATOR CHARACTERISTICS

FIGURE 4 – RC OSCILLATOR STABILITY

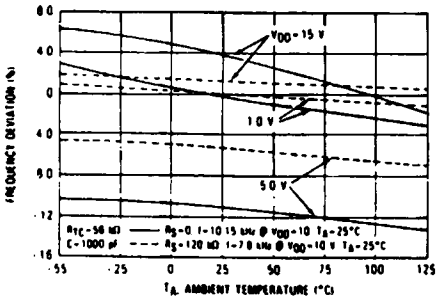


FIGURE 5 – RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{TC} AND C

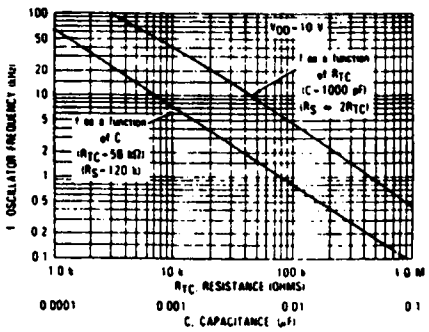


FIGURE 6 – TYPICAL CRYSTAL OSCILLATOR CIRCUIT

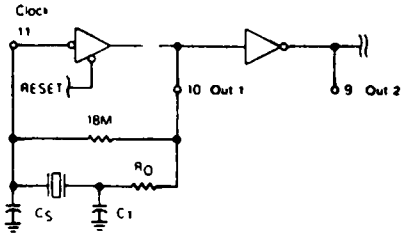


FIGURE 7 – TYPICAL DATA FOR CRYSTAL OSCILLATOR CIRCUIT

Characteristic	500 kHz Circuit	32 kHz Circuit	Unit
Crystal Characteristics			
Resonant Frequency	500	32	kHz
Equivalent Resistance, R_S	1.0	6.2	kΩ
External Resistor/Capacitor Values			
R_O	47	750	kΩ
C_T	82	82	pF
C_S	20	20	pF
Frequency Stability			
Frequency Changes as a Function of V_{DD} (T_A = 25°C)			
V_{DD} Change from 5.0 V to 10 V	+6.0	+2.0	ppm
V_{DD} Change from 10 V to 15 V	+2.0	+2.0	ppm
Frequency Change as a Function of Temperature (V_{DD} = 10 V)			
T_A Change from −55°C to +25°C Complete Oscillator*	+100	+120	ppm
T_A Change from +25°C to +125°C Complete Oscillator*	−160	−560	ppm

*Complete oscillator includes crystal, capacitors and resistors.

Panasonic

RECHARGEABLE SEALED LEAD-ACID BATTERIES

General Description

The LCR Series is a sealed lead acid rechargeable battery system. The lead calcium rechargeable (LCR) battery, will stand up to tough operating conditions such as overcharge and deep discharge. In field service, troubles due to abnormal, improper operation or misuse are reduced to a minimum.

Applications

- **Consumer Applications**
  Portable VTR VCR, TV, record players, tape recorders, vacuum cleaners and appliances, and as portable power supplies
- **Communication and Telephone Equipment**
  Cordlesss portable telephones, and transceivers
- **Office Equipment**
  Portable calculators, computers, electronic cash registers, printer, and typewriters
- **Memory Back up & UPS**
  UPS systems, electronic cash registers, computers, sequencers
- **Tools and Engine-start**
  Grass and hedge trimmers, cordless drills, screwdrivers, engine start, and electric saws
- **Instrument and Medical Equipment**
  Electronic instruments, measuring equipment, medical electronics, and heart defibrillators
- **Photography**
  Electronic cameras, strobe, VTR and movie lights
- **Toys and Hobby**
  Radio-controllers, motor driving, lights
- **Emergency Devices**
  Lights, fire and burglar alarms, communication systems, fire shutters

Features

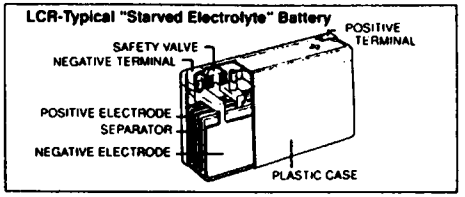
- Exceptional deep discharge recovery
- Long service life, float or cyclic
- Starved electrolyte
- Maintenance free operation
- Charge, discharge, or store in any position
- No corrosive gas generation
- Leakproof design
- No memory effect
- Approved as 'dry cell' for airshipment by Department of Transportation and IATA
- UL component recognized (all major models) File #MH13723(N)

● Temperature Range Summary

Discharge	5°~122°F	-15°~50°C
Charge	32°~104°F	0°~40°C
Storage	5°~104°F	-15°~40°

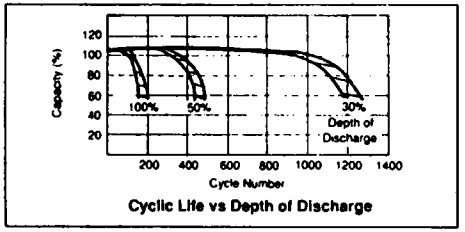
● Charging method and battery application

	Cyclic operation	Trickle operation	Float operation
Constant Voltage	Regulation range of controlled voltage 6 volt batteries: 7.3V to 7.5V 12 volt batteries: 14.6V to 15.0V	Regulation range of controlled voltage: 6 volt batteries: 6.8V to 6.9V 12 volt batteries: 13.6V to 13.8V	Regulation range of controlled voltage 6 volt batteries: 6.8V to 6.9V 12 volt batteries: 13.6V to 13.8V



● Cycle Life

Cycle life is very much dependent on the depth of the discharge which the battery encounters during each cycle.



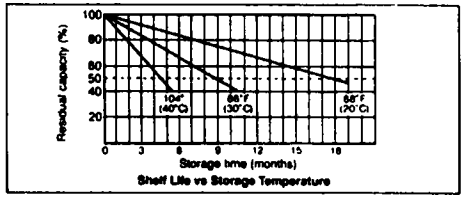
Cyclic Life vs Depth of Discharge

● Float or Back up Life

The expected float life at room temperature is approximately 8 years on the basis of accelerated tests.

●"Shelf Life"

Self-discharge rate is very much dependent on the storage temperature as shown in the graph. Lower temperatures allow the battery to be stored for longer periods. (Each ten degree drop results in a halving of self-discharge rate and doubles storage time.)



Shelf Life vs Storage Temperature

Model Number	Nominal Voltage (V)	Nominal Capacity 10 hour rate (Ah)	Nominal Capacity 20 hour rate (Ah)	Dimensions Length inch (mm)	Width inch (mm)	Height inch (mm)	Total Height (including terminals) inch (mm)	Weight (Approx.) lbs. (g)	Standard Terminals or Connectors
General Type									
LCR6V1.3P	6	1.2	1.3	3.82(97)	0.94(24)	1.97(50)	2.16(56)	0.66(300)	Faston Type 187
LCR12V1.3P	12	1.2	1.3	3.82(97)	1.87(47.5)	1.97(50)	2.16(56)	1.30(5.90)	"
LCR12V2.2P	12	2.0	2.2	6.97(177)	1.34(34)	2.36(60)	2.60(66)	1.76(800)	"
LCT-1912AP	12	1.8	1.9	0.94(23.8)	7.17(182)	2.33(61.5)	2.43(61.7)	1.40(635)	Pressure Contact
LCR6V2.4P	6	2.2	2.4	2.60(66)	1.30(33)	3.88(98.5)	4.11(104.5)	1.15(520)	Faston Type 187
LCR6V3.4P	6	3.0	3.4	5.28(134)	1.34(34)	2.36(60)	2.60(66)	1.36(620)	"
LCR12V3.4P	12	3.0	3.4	5.28(134)	2.64(67)	2.36(60)	2.60(66)	2.73(1240)	"
LCR6V3.2P	6	3.0	3.2	2.60(66)	1.30(33)	4.69(119)	4.92(125)	1.46(660)	"
LCR6V4P	6	3.7	4.0	2.76(70)	1.89(48)	4.02(102)	4.25(108)	1.83(830)	"
LCR6V4PL	6	3.7	4.0	2.76(70)	1.89(48)	4.02(102)	4.02(102)	1.83(830)	Lead wire Type
LCR12V4PF	12	3.7	4.0	2.76(70)	3.82(97)	4.02(102)	4.33(110)	3.66(1660)	Faston Type 187
LCR6V6.5P	6	6.0	6.5	5.95(151)	1.34(34)	3.70(94)	3.94(100)	2.54(1150)	Faston Type 187 or 250
LCR12V6.5P	12	6.0	6.5	5.95(151)	2.54(64.5)	3.70(94)	3.94(100)	4.85(2200)	"
LCR6V10PA	6	8.8	10.0	5.95(151)	1.97(50)	3.70(94)	3.94(100)	3.86(1750)	"
LCR12V10PF	12	9.3	10.0	5.95(151)	3.98(101)	3.70(94)	4.01(102)	7.72(3500)	"
LCR12V17P	12	15	17	7.13(181)	3.00(76)	6.58(167)	6.58(167)	13.7(6200)	M5 Bolt and Nut type
Large Capacity Type									
LCL12V20P	12	18	20	7.28(185)	4.92(125)	6.50(165)	6.50(165)	16.5(7.5)	M5 Bolt and Nut type
LCL12V24P	12	22	24	4.92(125)	6.50(165)	6.89(175)	6.89(175)	19.2(8.7)	"
LCL12V38P	12	35	38	7.76(197)	6.50(165)	6.89(175)	6.89(175)	28.7(13)	M6 Bolt and Nut type
LCL12V65P	12	57	65	13.8(350)	6.54(166)	6.85(174)	6.85(174)	41.9(19)	"
LCR12V80P	12	70	80	16.03(407)	6.82(173)	8.27(210)	9.69(246)	80.0(36)	M8 Bolt and Nut type
LCR12V100P	12	86	100	19.77(502)	7.09(180)	8.27(210)	10.04(255)	100.0(45)	"
LCR12V120P	12	104	120	19.89(505)	8.67(220)	8.27(210)	10.04(255)	115.0(52)	"
High Rate Type									
LCS-2.1P	4	2.1	2.2	1.90(48.3)	1.41(35.8)	2.48(63.1)	2.52(63.9)	0.57(260)	Pressure Contact
LCS-2.8P	8	2.1	2.2	1.89(48.0)	2.65(67.3)	2.48(63.1)	2.50(63.4)	1.15(520)	"
LCS-3.1P	8	3.1	3.2	1.89(48.0)	2.65(67.3)	3.56(90.3)	3.57(90.6)	1.59(720)	"
LCS-3.8P	4	3.8	4.0	1.88(47.8)	1.40(35.5)	4.6(118.7)	4.69(119)	1.08(490)	"
LCS-3.8P	6	3.8	4.0	2.03(51.5)	1.88(47.7)	4.67(118.7)	4.69(119)	1.52(690)	"
LCS-4.1P	4	4.1	4.3	1.88(47.8)	1.40(35.5)	4.67(118.7)	4.69(119)	1.12(510)	"
LCS-4.1P	6	4.1	4.3	1.88(47.8)	2.03(51.5)	4.67(118.7)	4.69(119)	1.63(740)	"
LCS-2.9P2PL	12	2.9	3.0	4.02(102)	2.19(55.5)	3.11(79)	3.14(79.8)	2.76(1250)	Leadwire Type
Compact/Speciality Type									
LCR-1812VBNC	12	1.8	1.9	7.89(200.5)	0.98(24.8)	2.38(60.5)	2.38(60.5)	1.54(700)	DC Plug
LCS-2012VBNC	12	2.0	2.1	7.90(200.7)	0.98(24.8)	2.43(61.8)	2.43(61.8)	1.54(700)	Pressure contact
LCS-2312AVBNC	12	2.3	2.4	7.17(182)	0.94(23.85)	2.42(61.5)	2.43(61.7)	1.40(635)	"
LCS-2012BVBN	12	2.0	2.2	1.14(29)	3.11(79)	6.02(153)	6.02(153)	1.58(715)	"

TW SERIES
1.8W-3W

REGULATED DC/DC CONVERTERS
24 PIN DIP

FEATURES:

- HIGH PERFORMANCE TT INPUT FILTER
- SINGLE AND DUAL OUTPUTS
- HIGHLY REGULATED ISOLATED OUTPUTS
- 100% BURN IN
- HIGH EFFICIENCY
- HIGH RELIABILITY
- NO EXTERNAL COMPONENTS

FROM STOCK

SPECIFICATIONS:

- OUTPUT VOLTAGE STABILITY 0.02%/°C Max
- OUTPUT VOLTAGE ACCURACY ± 5%
- REGULATION Line ±0.5% Max Load ±1% Max
- RIPPLE AND NOISE 50 mVP-P Max.
- INPUT-OUTPUT ISOLATION 500 VDC Min.
- OPERATING TEMPERATURE -25°C to + 71°C
- STORAGE TEMPERATURE -40°C to + 100°C
- EFFICIENCY 55% Min

SINGLE VOLTAGE UNITS

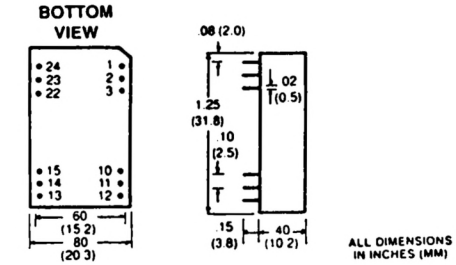
INPUT VOLTAGE (VDC)	OUTPUT VOLTAGE (VDC)	OUTPUT CURRENT (mA)	MODEL NUMBER	PRICE 1-9 QTY
5 (4.75-5.25)	5	360	TW1 8-5S5	23 00
	5	600	TW3-5S5	29 00
	9	250	TW1 8-5S9	23 00
	9	334	TW3-5S9	29 00
	12	150	TW1 8-5S12	23 00
	12	250	TW3-5S12	29 00
	15	120	TW1 8-5S15	23 00
	15	200	TW3-5S15	29 00
12 (11.40-12.60)	5	360	TW1 8-12S5	23 00
	5	600	TW3-12S5	29 00
	9	250	TW1 8-12S9	23 00
	9	334	TW3-12S9	29 00
	12	150	TW1 8-12S12	23 00
	12	250	TW3-12S12	29 00
	15	120	TW1 8-12S15	23 00
	15	200	TW3-12S15	29 00
24 (22.80-25.20)	5	360	TW1 8-24S5	23 00
	5	600	TW3-24S5	29 00
	9	250	TW1 8-24S9	23 00
	9	334	TW3-24S9	29 00
	12	150	TW1 8-24S12	23 00
	12	250	TW3-24S12	29 00
	15	120	TW1 8-24S15	23 00
	15	200	TW3-24S15	29 00
28 (26.60-29.40)	5	360	TW1 8-28S5	23 00
	5	400	TW2-28S5	25 00
	5	600	TW3-28S5	29 00
	9	250	TW1 8-28S9	23 00
	9	334	TW3-28S9	29 00
	12	150	TW1 8-28S12	23 00
	12	250	TW3-28S12	29 00
	15	120	TW1 8-28S15	23 00
	15	200	TW3-28S15	29.00
48 (45.60-50.40)	5	360	TW1 8-48S5	23 00
	5	600	TW3-48S5	29 00
	9	250	TW1 8-48S9	23.00
	9	334	TW3-48S9	29 00
	12	150	TW1 8-48S12	23 00
	12	250	TW3-48S12	29 00
	15	120	TW1 8-48S15	23 00
	15	200	TW3-48S15	29.00

POLYTRON DEVICES, INC.
P.O. BOX 398, PATERSON, N.J. 07544 (201) 345-5885 FAX: (201) 345-1264

24-PIN DIP DC/DC CONVERTERS (continued)

DUAL VOLTAGE UNITS

INPUT VOLTAGE (VDC)	OUTPUT VOLTAGE (VDC)	OUTPUT CURRENT (mA)	MODEL NUMBER	PRICE 1-9 QTY
5 (4.75-5.25)	± 5	± 180	TW1 8-5-5	29 00
	± 5	± 300	TW3-5-5	34 00
	± 9	± 100	TW1 8-5-9	29 00
	± 9	± 167	TW3-5-9	34 00
	± 12	± 75	TW1 8-5-12	29 00
	± 12	± 125	TW3-5-12	34 00
	± 15	± 60	TW1 8-5-15	29 00
	± 15	± 100	TW3-5-15	34 00
12 (11.40-12.60)	± 5	± 180	TW1 8-12-5	29 00
	± 5	± 300	TW3-12-5	34 00
	± 12	± 75	TW1 8-12-12	29 00
	± 12	± 125	TW3-12-12	34 00
	± 15	± 60	TW1 8-12-15	29 00
	± 15	± 100	TW3-12-15	34 00
24 (22.80-25.20)	± 5	± 180	TW1 8-24-5	29 00
	± 5	± 300	TW3-24-5	34 00
	± 12	± 75	TW1 8-24-12	29.00
	± 12	± 125	TW3-24-12	34 00
	± 15	± 60	TW1 8-24-15	29 00
	± 15	± 100	TW3-24-15	34 00
28 (26.60-29.40)	± 5	± 180	TW1 8-28-5	29 00
	± 5	± 300	TW3-28-5	34 00
	± 12	± 75	TW1 8-28-12	29 00
	± 12	± 125	TW3-28-12	34 00
	± 15	± 60	TW1 8-28-15	29 00
	± 15	± 100	TW3-28-15	34 00
48 (45.60-50.40)	± 5	± 180	TW1 8-48-5	29 00
	± 5	± 300	TW3-48-5	34 00
	± 12	± 75	TW1 8-48-12	29 00
	± 12	± 125	TW3-48-12	34 00
	± 15	± 60	TW1 8-48-15	29 00
	± 15	± 100	TW3-48-15	34 00



Pin Connections		
PIN	SINGLE OUTPUT	DUAL OUTPUT
1	+ V INPUT	+ V INPUT
2	N.C.	- V OUTPUT
3	N.C.	COMMON
10	- V OUTPUT	COMMON
11	+ V OUTPUT	+ V OUTPUT
12	- V INPUT	- V INPUT
13	- V INPUT	- V INPUT
14	+ V OUTPUT	+ V OUTPUT
15	- V OUTPUT	COMMON
22	N.C.	COMMON
23	N.C.	- V OUTPUT
24	+ V INPUT	+ V INPUT

POLYTRON DEVICES, INC.
P.O. BOX 398, PATERSON, N.J. 07544 (201) 345-5885 FAX: (201) 345-1264

National Semiconductor

ADC0808, ADC0809 8-Bit μP Compatible A/D Converters With 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

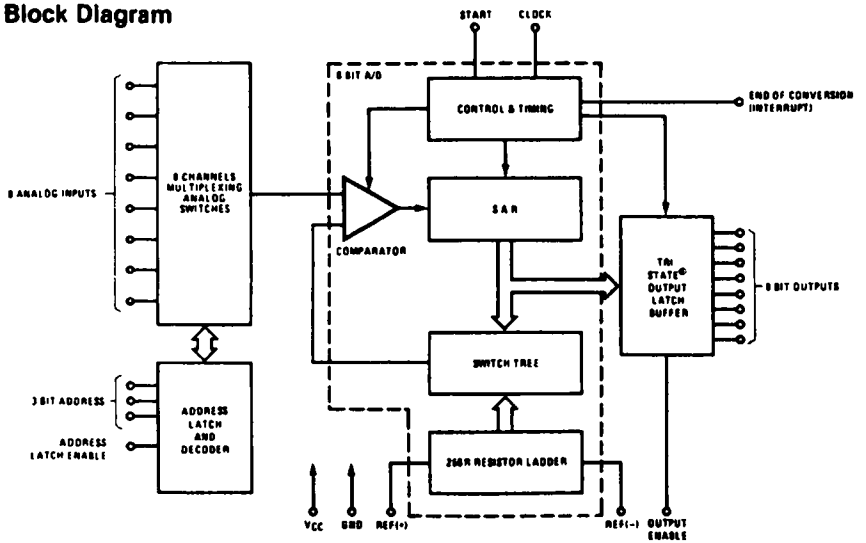
The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet. (See AN-247 for more information.)

Features

- Resolution — 8-bits
- Total unadjusted error — ± 1/2 LSB and ± 1 LSB
- No missing codes
- Conversion time — 100 μs
- Single supply — 5 V_{DC}
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- 8-channel multiplexer with latched control logic
- Easy interface to all microprocessors, or operates "stand alone"
- Outputs meet T^2L voltage level specifications
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Standard hermetic or molded 28-pin DIP package
- Temperature range −40°C to +85°C or −55°C to +125°C
- Low power consumption — 15 mW
- Latched TRI-STATE® output

Block Diagram



TRI-STATE® is a registered trademark of National Semiconductor Corp.

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin Except Control Inputs	−0.3V to (V_{CC} + 0.3V)
Voltage at Control Inputs (START, OE, CLOCK, ALE, ADD A, ADD B, ADD C)	−0.3V to +15V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 and 2)

Temperature Range (Note 1)	$T_{MIN} \le T_A \le T_{MAX}$
ADC0808CJ	−55°C ≤ T_A ≤ +125°C
ADC0808CCJ, ADC0808CCN, ADC0809CCN	−40°C ≤ T_A ≤ +85°C
Range of V_{CC} (Note 1)	4.5 V_{DC} to 8.0 V_{DC}

Electrical Characteristics

Converter Specifications: V_{CC} = 5 V_{DC} = $V_{REF(+)}$, $V_{REF(-)}$ = GND, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise stated.

	Parameter	Conditions	Min	Typ	Max	Units
	ADC0808					
	Total Unadjusted Error	25°C			± 1/2	LSB
	(Note 5)	T_{MIN} to T_{MAX}			± 3/4	LSB
	ADC0809					
	Total Unadjusted Error	0°C to 70°C			± 1	LSB
	(Note 5)	T_{MIN} to T_{MAX}			± 1 1/4	LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	2.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND-0.10		V_{CC}+0.10	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	V_{CC}+0.1	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		V_{CC}/2-0.1	V_{CC}/2	V_{CC}/2+0.1	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V
	Comparator Input Current	f_c = 640 kHz, (Note 6)	−2	±0.5	2	μA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0808CJ 4.5V ≤ V_{CC} ≤ 5.5V, −55°C ≤ T_A ≤ +125°C unless otherwise noted ADC0808CCJ, ADC0808CCN, and ADC0809CCN 4.75 ≤ V_{CC} ≤ 5.25V, −40°C ≤ T_A ≤ +85°C unless otherwise noted

	Parameter	Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
$I_{OFF(+)}$	OFF Channel Leakage Current	V_{CC} = 5V, V_{IN} = 5V,				
		T_A = 25°C		10	200	nA
		T_{MIN} to T_{MAX}			1.0	μA
$I_{OFF(-)}$	OFF Channel Leakage Current	V_{CC} = 5V, V_{IN} = 0,				
		T_A = 25°C	−200	−10		nA
		T_{MIN} to T_{MAX}	−1.0			μA
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		V_{CC}-1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	V_{IN} = 15V			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	V_{IN} = 0	−1.0			μA
I_{CC}	Supply Current	f_{CLK} = 640 kHz		0.3	3.0	mA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0808CJ $4.5V \le V_{CC} \le 5.5V$, $-55°C \le T_A \le +125°C$ unless otherwise noted ADC0808CCJ, ADC0808CCN, and ADC0809CCN $4.75 \le V_{CC} \le 5.25V$, $-40°C \le T_A \le +85°C$ unless otherwise noted

Parameter		Conditions	Min	Typ	Max	Units
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O = -360\ \mu A$	$V_{CC}-0.4$			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = 1.6$ mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	$I_O = 1.2$ mA			0.45	V
I_{OUT}	TRI-STATE® Output Current	$V_O = 5V$			3	μA
		$V_O = 0$	-3			μA

Electrical Characteristics

Timing Specifications: $V_{CC} = V_{REF(+)} = 5V$, $V_{REF(-)} = GND$, $t_r = t_f = 20$ ns and $T_A = 25°C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	*(Figure 5)*		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	*(Figure 5)*		100	200	ns
t_s	Minimum Address Set-Up Time	*(Figure 5)*		25	50	ns
t_H	Minimum Address Hold Time	*(Figure 5)*		25	50	ns
t_D	Analog MUX Delay Time From ALE	$R_S = 0\Omega$ *(Figure 5)*		1	2.5	μs
t_{H1}, t_{H0}	OE Control to Q Logic State	$C_L = 50$ pF, $R_L = 10k$ *(Figure 8)*		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	$C_L = 10$ pF, $R_L = 10k$ *(Figure 8)*		125	250	ns
t_c	Conversion Time	$f_c = 640$ kHz, *(Figure 5)* (Note 7)	90	100	116	μs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	*(Figure 5)*	0		8 + 2 μs	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE® Output Capacitance	At TRI-STATE® Outputs, (Note 12)		10	15	pF

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See *Figure 3*. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13*.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence *(Figure 6)*. See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Functional Description

Multiplexer: The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table I shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE I

SELECTED ANALOG CHANNEL	ADDRESS LINE C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach *(Figure 1)* was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +1/2 LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.

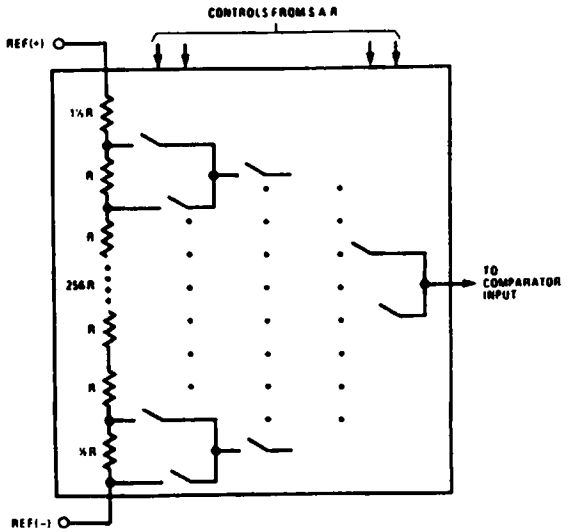


FIGURE 1. Resistor Ladder and Switch Tree

Functional Description (Continued)

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-179.

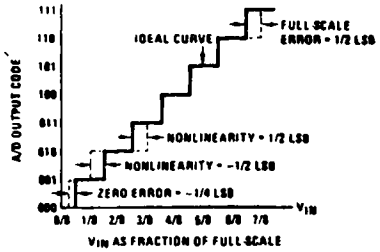


FIGURE 2. 3-Bit A/D Transfer Curve

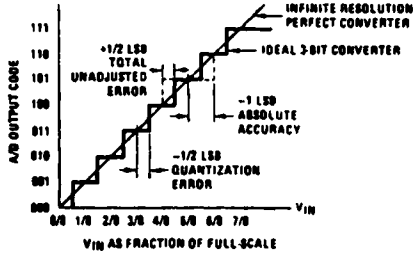
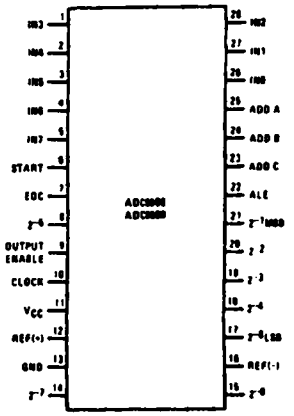


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

FIGURE 4. Typical Error Curve

Connection Diagram

Dual-In-Line Package



Timing Diagram

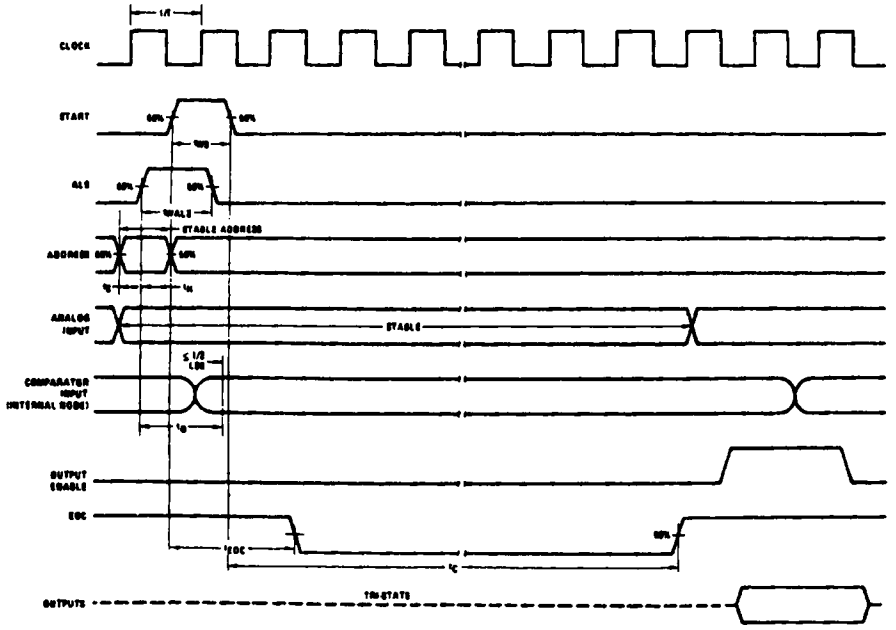


FIGURE 5

Typical Performance Characteristics

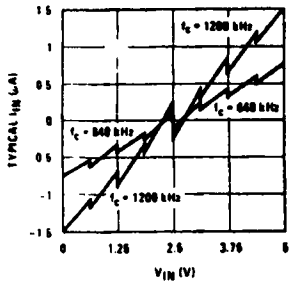


FIGURE 6. Comparator I_{IN} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

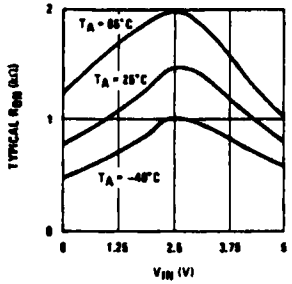


FIGURE 7. Multiplexer R_{ON} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

TRI-STATE® Test Circuits and Timing Diagrams

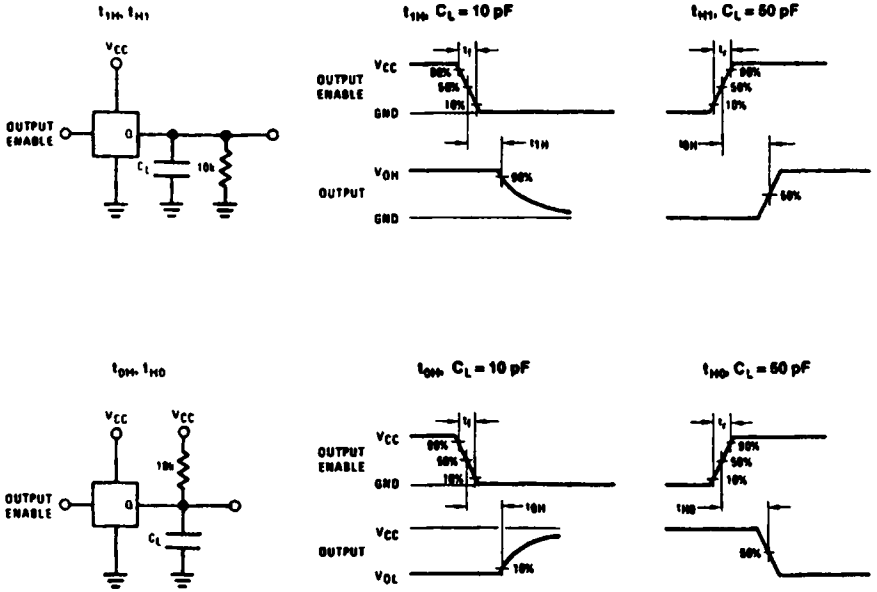


FIGURE 8

Applications Information

OPERATION

1.0 Ratiometric Conversion

The ADC0808, ADC0809 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0808 is expressed by the equation

$$\frac{V_{IN}}{V_{fs} - V_Z} = \frac{D_X}{D_{MAX} - D_{MIN}} \quad (1)$$

V_{IN} = Input voltage into the ADC0808
V_{fs} = Full-scale voltage
V_Z = Zero voltage
D_X = Data point being measured
D_{MAX} = Maximum data limit
D_{MIN} = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0808, ADC0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, *(Figure 9)*.

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC} = V_{REF} = 5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

2.0 Resistor Ladder Limitations

The voltages from the resistor ladder are compared to the selected input 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V is used, the supply should be adjusted to the same voltage within 0.1V.

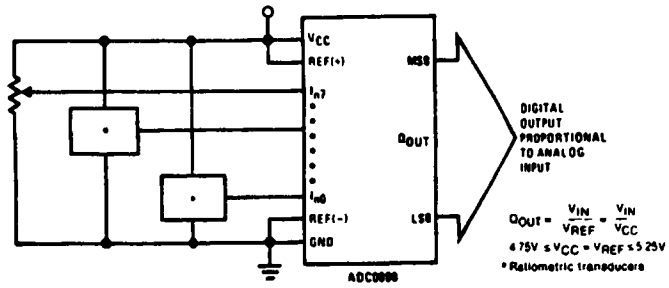


FIGURE 9. Ratiometric Conversion System

Applications Information (Continued)

The ADC0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 μF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.

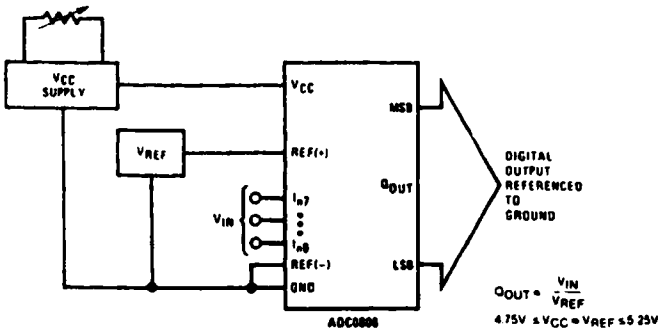


FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply

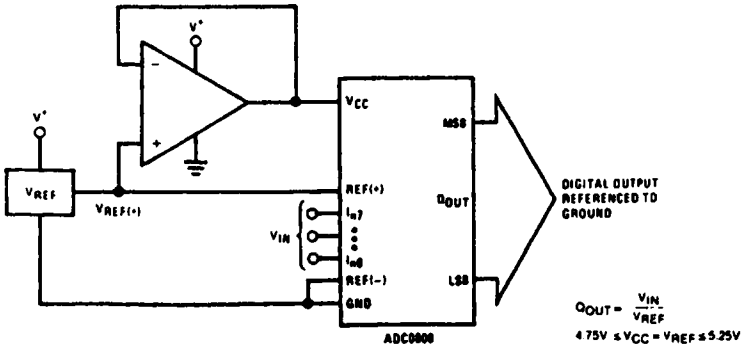


FIGURE 11. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

Applications Information (Continued)

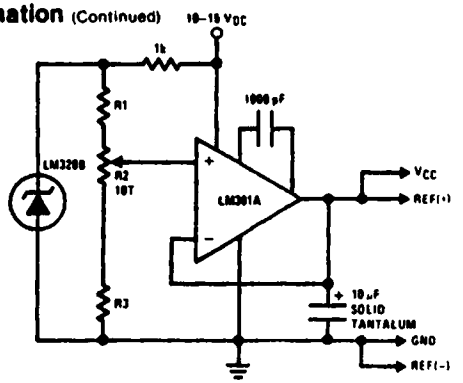


FIGURE 12. Typical Reference and Supply Circuit

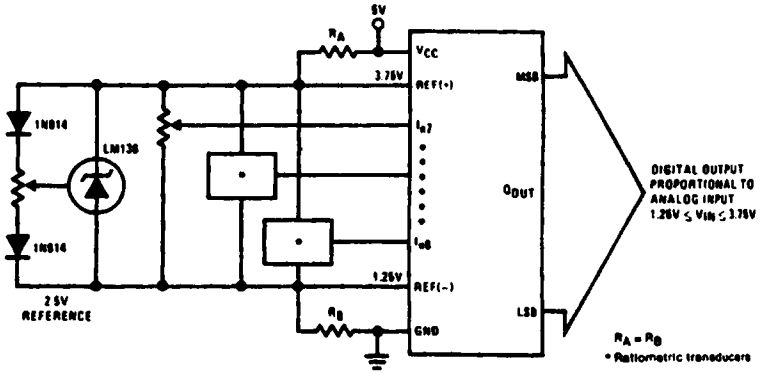


FIGURE 13. Symmetrically Centered Reference

3.0 Converter Equations

The transition between adjacent codes N and N+1 is given by:

$$V_{IN} = \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} + \frac{1}{512} \right] \pm V_{TUE} \right\} + V_{REF(-)} \quad (2)$$

The center of an output code N is given by:

$$V_{IN} = \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} \right] \pm V_{TUE} \right\} + V_{REF(-)} \quad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy} \quad (4)$$

where: V_{IN} = Voltage at comparator input
$V_{REF(+)}$ = Voltage at Ref(+)
$V_{REF(-)}$ = Voltage at Ref(−)
V_{TUE} = Total unadjusted error voltage (typically $V_{REF(+)} \div 512$)

4.0 Analog Comparator Inputs

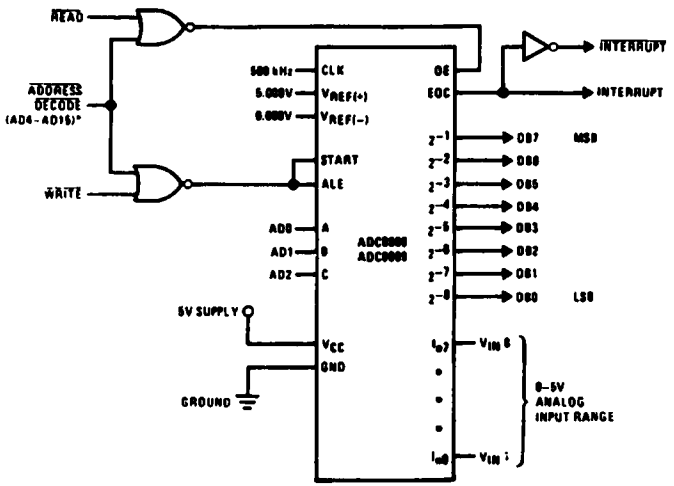
The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in *Figure 6*.

If no filter capacitors are used at the analog inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally.

Typical Application



* Address latches needed for 8085 and SC/MP interfacing the ADC0808 to a microprocessor

MICROPROCESSOR INTERFACE TABLE

PROCESSOR	READ	WRITE	INTERRUPT (COMMENT)
8080	MEMR	MEMW	INTR (Thru RST Circuit)
8085	RD	WR	INTR (Thru RST Circuit)
Z-80	RD	WR	INT (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA ∘ 2 R/W	VMA ∘ 2 R/W	IRQA or IRQB (Thru PIA)

Ordering Information

TEMPERATURE RANGE		−40°C to +85°C		−55°C to +125°C
Error	± 1/2 Bit Unadjusted	ADC0808CCN	ADC0808CCJ	ADC0808CJ
	± 1 Bit Unadjusted	ADC0809CCN		
Package Outline		N28A Molded DIP	J28A Hermetic DIP	J28A Hermetic DIP

5.0 Special-Purpose Components Data Sheets

The following special-purpose data sheets follow this page and are ordered as listed. Note that many of these components are widely used throughout the system.

PC Interface Bin

Intel 87C51FA Microcontroller
NEC PS2501-1 Photo Coupler
NEC PS2502-1 Photo Coupler
MAX233 RS-232 Driver/Receiver
MAX695 Microprocessor Supervisory Circuit
HPR105 DC/DC Converter
OP-15FP Operational Amplifier
Lambda LVS-44-12B Power Supply

Isolated CPU Interface Board

P1602 Surge Arrestor

M26 Antenna Interface

LTC1042 Window Comparator
LT1009 2.5 Volt Reference
Polytron TW1.8-24S5 DC/DC Converter

M29 Auxiliary Interface

ADC0808 Analog Multiplexer-A/D Converter
ICM7555 General Purpose Timer
AD590 Temperature Transducer
AD581 High Precision 10 V IC Reference
PALCE22V10Z-25 Programmable Array Logic
MC14060B 14-Bit Counter and Oscillator

M28 Power Supply/Battery Module

Lambda VS10-15 Power Supply
Panasonic LCR 12v1.3P Battery

Window Comparator

FEATURES

- Micropower 1.5μW (1 Sample/Second)
- Wide Supply Range — +2.8V to +16V
- High Accuracy
  - Center Error ±1mV Max
  - Width Error ±0.15% Max
- Wide Input Voltage Range
  - V⁺ to Ground
- TTL Outputs with 5V Supply
- Two Independent Ground-Referred Control Inputs
- Small Size 8-Pin MiniDIP

APPLICATIONS

- Fault Detectors
- Go/No-Go Testing
- Microprocessor Power Supply Monitor

DESCRIPTION

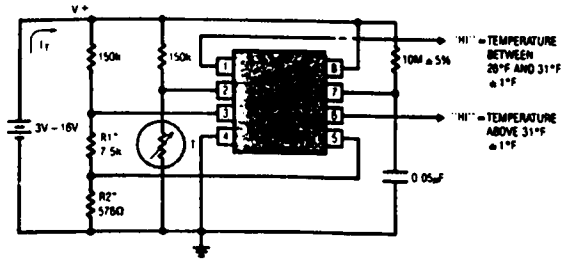
The LTC1042 is a monolithic CMOS window comparator manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process. Two high impedance voltage inputs, CENTER and WIDTH/2, define the middle and width of the comparison window. Whenever the input voltage, V_{IN}, is inside the window the WITHIN WINDOW output is high. The ABOVE WINDOW output is high whenever V_{IN} is above the window. By interchanging V_{IN} and CENTER the ABOVE WINDOW output becomes BELOW WINDOW and is high if V_{IN} is below the window.

Sampling techniques provide high impedance voltage inputs that can common-mode to both supply rails (V⁺ and GND). An important feature of the inputs is their non-interaction. Also the device is effectively "chopper stabilized", giving it extremely high accuracy over all conditions of temperature, power supply and input voltage range.

Another benefit of the sampling techniques used to design the LTC1042 is the extremely low power consumption. When the device is strobed, it internally turns on the power to the comparators, samples the inputs, stores the outputs in CMOS latches and then turns off power to the comparators. This all happens in about 80μs. Average power can be made small, almost arbitrarily, by lowering the strobe rate. The device can be self-strobed using an external RC network or strobed externally by driving the OSC pin with a CMOS gate.

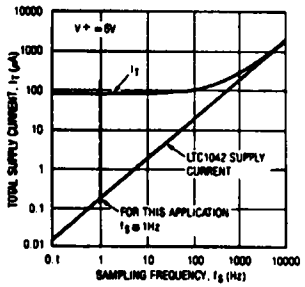
LTCMOS™ is a trademark of Linear Technology Corp

Battery Powered Remote Freezer Alarm



T = YELLOW SPRINGS INSTRUMENT CO., INC. P/N 44007
ALL RESISTORS ± 1% UNLESS OTHERWISE SPECIFIED
*OTHER TEMPERATURE BANDS MAY BE SELECTED BY CHOOSING APPROPRIATE VALUES FOR R1 AND R2

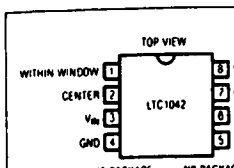
Total Supply Current vs Sampling Frequency



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V⁺ to GND) 18V
Input Voltage ..... V⁺ + 0.3V to – 0.3V
Operating Temperature Range
LTC1042C ..... – 40°C to 85°C
LTC1042M ..... – 55°C to 125°C
Storage Temperature Range ..... – 55°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Output Short Circuit Duration ..... Continuous

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC1042MJ8 LTC1042CN8

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
	Center Error (Note 2)	V⁺ = 2.8V to 6V (Note 1)	●		±0.3 + ±0.05	±1 + ±0.15	mV % WIDTH/2
		V⁺ = 6V to 15V (Note 1)	●		±1 + ±0.05	±3 + ±0.15	mV % WIDTH/2
	Width Error (Note 3)	V⁺ = 2.8V to 6V (Note 1)	●		±0.6 + ±0.1	±2 + ±0.3	mV % WIDTH/2
		V⁺ = 6V to 15V (Note 1)	●		±2 + ±0.1	±6 + ±0.3	mV % WIDTH/2
I_{BIAS}	Input Bias Current	V⁺ = 5V, T_A = 25°C, OSC = GND V_{IN}, CENTER and WIDTH/2 Inputs			±0.3		nA
R_{IN}	Average Input Resistance	f_S = 1kHz (Note 4)	●	10	15		MΩ
	Input Voltage Range		●	GND		V⁺	V
PSR	Power Supply Range		●	2.8		16	V
$I_{S(ON)}$	Power Supply ON Current (Note 5)	V⁺ = 5V	●		1.2	3	mA
$I_{S(OFF)}$	Power Supply OFF Current (Note 5)	V⁺ = 5V LTC1042C LTC1042M	● ●		0.001 0.001	0.5 5.0	μA μA
T_D	Response Time (Note 6)	V⁺ = 5V			80	100	μs
V_{OH} V_{OL}	Output Levels Logic 1 Output Logical 0 Output	V⁺ = 4.75V, I_{OUT} = – 360μA V⁺ = 4.75V, I_{OUT} = 1.6mA	● ●	2.4	4.4 0.25	0.45	V V
R_{EXT}	External Timing Resistor	Resistor Connected between V⁺ and OSC Pin	●	100		10,000	kΩ
f_S	Sampling Frequency	V⁺ = 5V, T_A = 25°C R_{EXT} = 1MΩ, C_{EXT} = 0.1μF			5		Hz

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Applies over input voltage range limit and includes gain uncertainty.

Note 2: Center error = [(V_U + V_L)/2 – CENTER] (where V_U = upper band limit and V_L = lower band limit).

Note 3: Width error = (V_U – V_L – 2 x WIDTH/2) (where V_U = upper band limit and V_L = lower band limit).

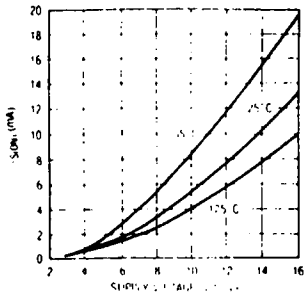
Note 4: R_{IN} is guaranteed by design and is not tested. R_{IN} = 1/(f_S x 66pF).

Note 5: Average supply current = $T_D \times I_{S(ON)} \times f_S + (1 - T_D f_S) I_{S(OFF)}$.

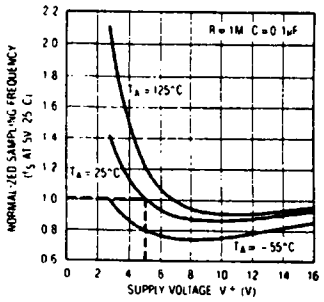
Note 6: Response time is set by an internal oscillator and is independent of overdrive voltage. T_D is guaranteed by correlation test and is not directly measured.

TYPICAL PERFORMANCE CHARACTERISTICS

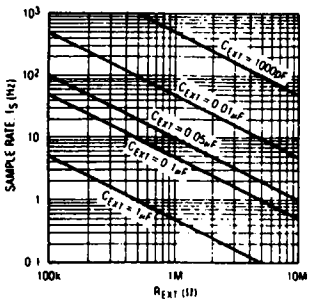
$I_{S(ON)}$ vs V^+



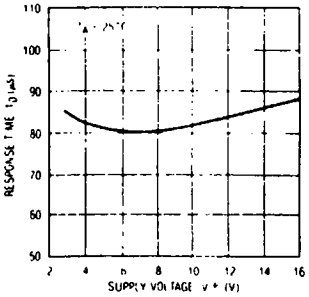
Normalized Sampling Frequency vs V^+, Temperature



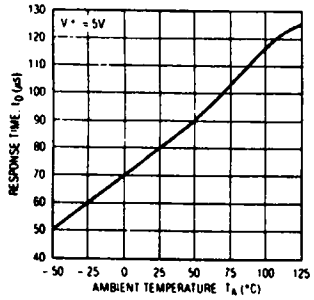
Sampling Rate vs R_{EXT}, C_{EXT}



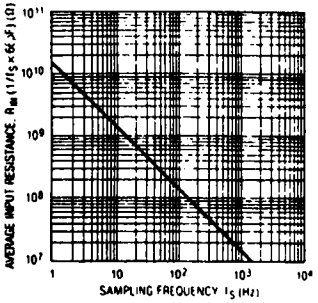
Response Time vs Supply Voltage



Response Time vs Temperature



R_{IN} vs Sampling Frequency

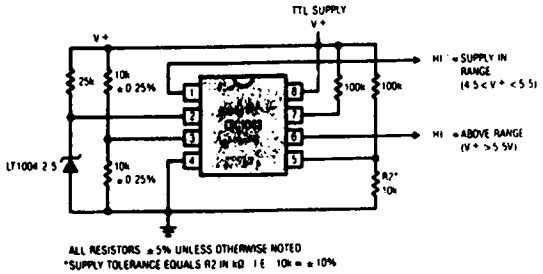


APPLICATIONS INFORMATION

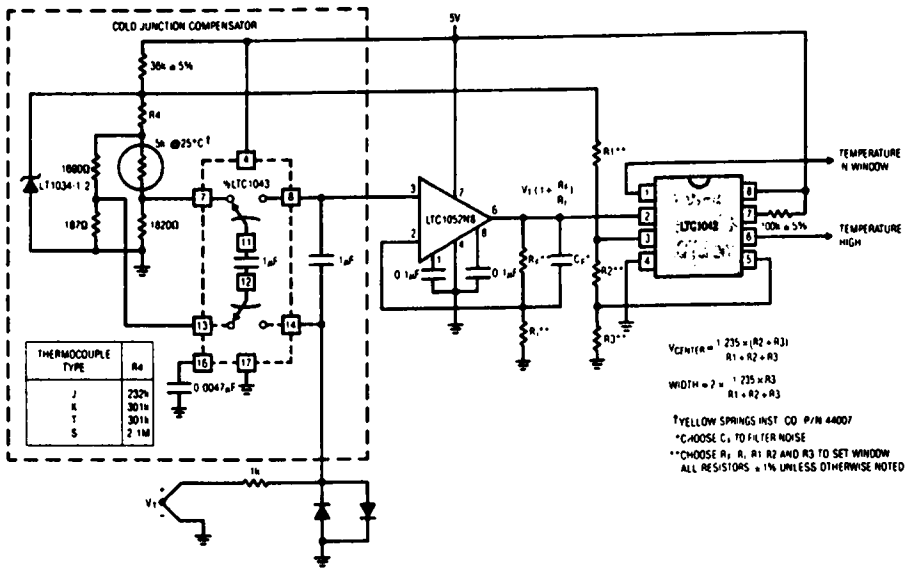
The LTC1042 uses sampled data techniques to achieve its unique characteristics. It consists of two comparators, each of which has two differential inputs (Figure 1). When the sum of the voltages on a comparator's inputs is positive, the output is high; when the sum is negative, the output is low. The inputs are interconnected such that when (CENTER – WIDTH/2) ≤ V_{IN} ≤ (CENTER + WIDTH/2) both comparator outputs are low. In this condition V_{IN} is within the window and the WITHIN WINDOW output is high. When V_{IN} > CENTER + WIDTH/2, V_{IN} is above the window and the ABOVE WINDOW output is high.

APPLICATIONS INFORMATION

TTL Power Supply Monitor



Single 5V Thermocouple Over Temperature Alarm



APPLICATIONS INFORMATION

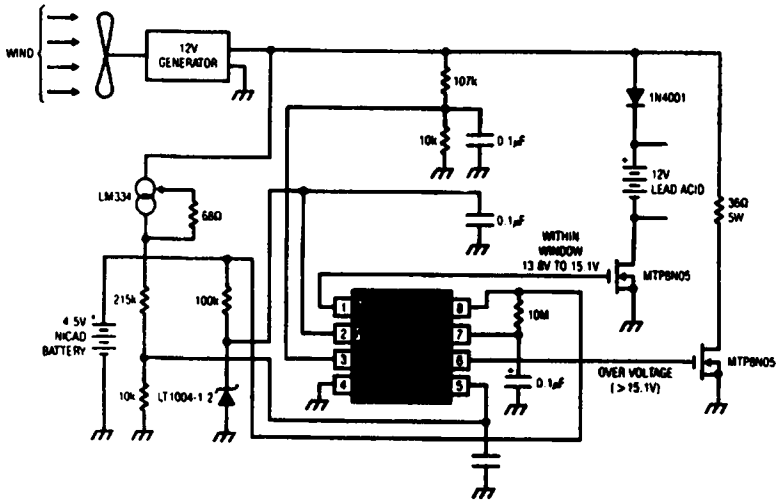
Wind Powered Battery Charger

A simple wind powered battery charger can be constructed using the new LTC1042, a 12V DC permanent magnet motor, and low cost power FET transistor.

The DC motor is used as a generator with the voltage output being proportional to its RPM. The LTC1042 monitors the voltage output and provides the following control functions.

1) If generator voltage output is below 13.8V, the control circuit is active and the NiCad battery is charging through the LM334 current source. The lead acid battery is not being charged.
2) If the generator voltage output is between 13.8V and 15.1V, the 12V lead acid battery is being charged at about a 1 amp/hour rate (limited by the power FET).
3) If generator voltage exceeds 15.1V (a condition caused by excessive wind speed or 12V battery being fully charged) then a fixed load is connected thus limiting the generator RPM to prevent damage.

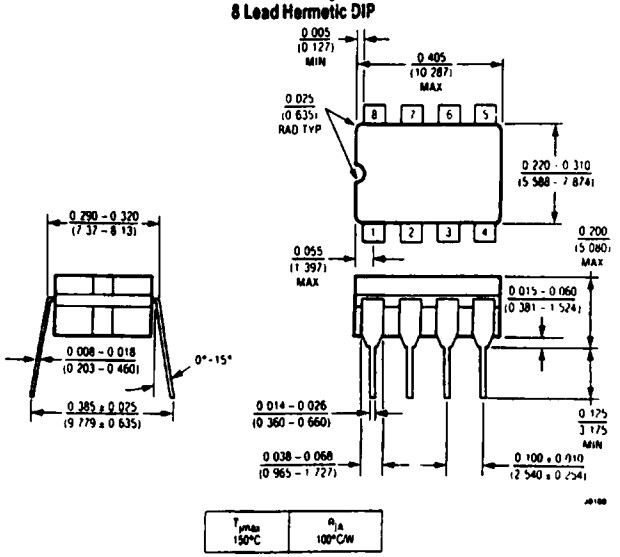
This charger can be used as a remote source of power where wind energy is plentiful such as on sailboats or remote radio repeater sites. Unlike solar powered panels, this system will function in bad weather and at night.



PACKAGE DESCRIPTION

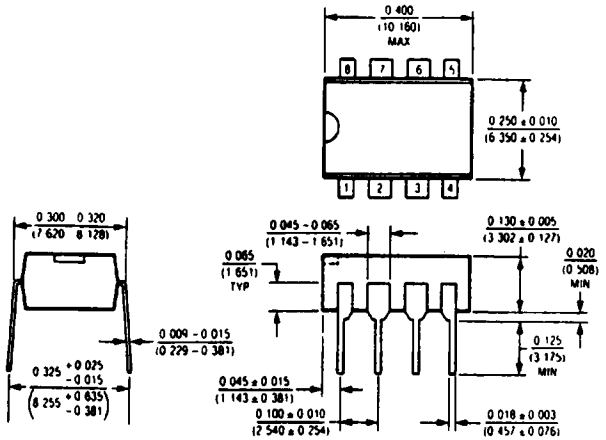
Dimensions in inches (millimeters) unless otherwise noted.

J8 Package
8 Lead Hermetic DIP



T_{jmax}	θ_{JA}
150°C	100°C/W

N8 Package
8 Lead Plastic



T_{jmax}	θ_{JA}
110°C	150°C/W

FEATURES

- 0.2% Initial Tolerance Max
- *Guaranteed* Temperature Stability
- Maximum 0.6Ω Dynamic Impedance
- Wide Operating Current Range
- Directly Interchangeable with LM136 for Improved Performance
- No Adjustments Needed for Minimum Temperature Coefficient

APPLICATIONS

- Reference for 5V Systems
- 8 Bit A/D and D/A Reference
- Digital Voltmeters
- Current Loop Measurement and Control Systems
- Power Supply Monitor

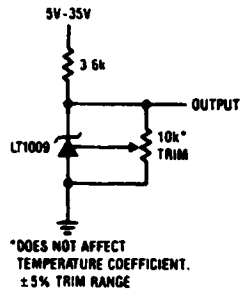
DESCRIPTION

The LT1009 is a precision trimmed 2.500 Volt shunt regulator diode featuring a maximum initial tolerance of only ±5mV. The low dynamic impedance and wide operating current range enhances its versatility. The 0.2% reference tolerance is achieved by on-chip trimming which not only minimizes the initial voltage tolerance but also minimizes the temperature drift.

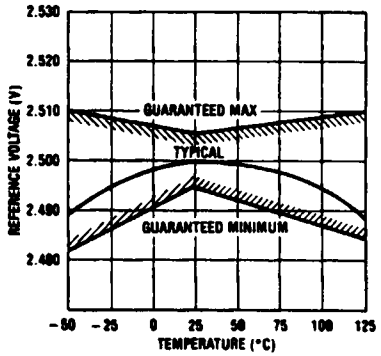
Even though no adjustments are needed with the LT1009, a third terminal allows the reference voltage to be adjusted ±5% to calibrate out system errors. In many applications, the LT1009 can be used as a pin-to-pin replacement of the LM136H-2.5 and the external trim network eliminated.

For a lower drift 2.5V reference, see the LT1019 data sheet.

2.5 Volt Reference



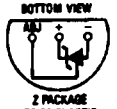
Output Voltage



ABSOLUTE MAXIMUM RATINGS

Reverse Current 20mA
Forward Current 10mA
Operating Temperature Range
LT1009M ..... −55°C to 125°C
LT1009C ..... 0°C to 70°C
Storage Temperature Range
LT1009M and C ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
	LT1009MH LT1009CH
	LT1009CZ

ELECTRICAL CHARACTERISTICS

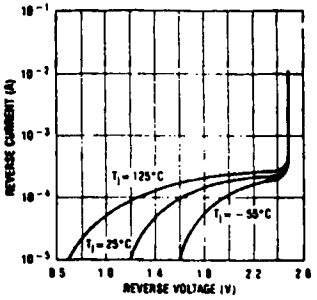
SYMBOL	PARAMETER	CONDITIONS		LT1009M MIN	LT1009M TYP	LT1009M MAX	LT1009C MIN	LT1009C TYP	LT1009C MAX	UNITS
V_Z	Reverse Breakdown Voltage	$T_A = 25°C$, $I_R = 1mA$		2.495	2.500	2.505	2.495	2.500	2.505	V
$\frac{\Delta V_Z}{\Delta I_R}$	Reverse Breakdown Change with Current	$400\mu A \le I_R \le 10mA$			2.6	6		2.6	10	mV
			●		3	10		3	12	mV
r_Z	Reverse Dynamic Impedance	$I_R = 1mA$			0.2	0.6		0.2	1.0	Ω
			●		0.4	1		0.4	1.4	Ω
$\frac{\Delta V_Z}{\Delta Temp}$	Temperature Stability	$T_{MIN} \le T_A \le T_{MAX}$	●			15		1.8	4	mV
	Average Temperature Coefficient	$0°C \le T_A \le 70°C$			15	25		15	25	ppm/°C
		$-55°C \le T_A \le 125°C$ (Note 1)			25	35				ppm/°C
$\frac{\Delta V_Z}{\Delta Time}$	Long Term Stability	$T_A = 25°C \pm 0.1°C$, $I_R = 1mA$			20			20		ppm/kHr

The ● denotes the specifications which apply over full operating temperature range.

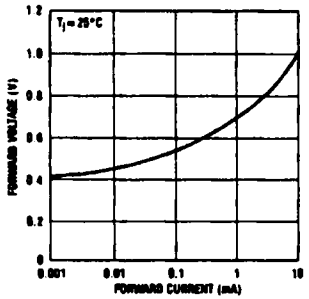
Note 1: Average temperature coefficient is defined as the total voltage change divided by the specified temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

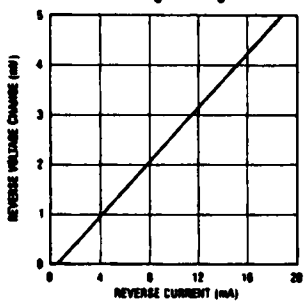
Reverse Characteristics



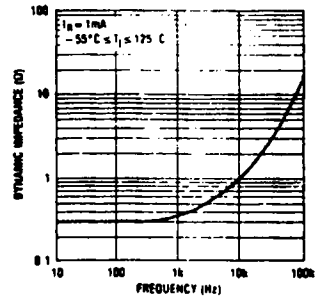
Forward Characteristics



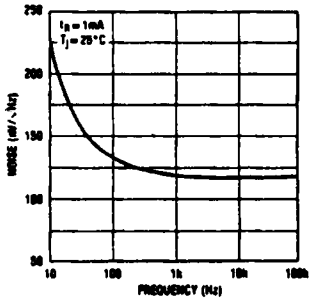
Reverse Voltage Change



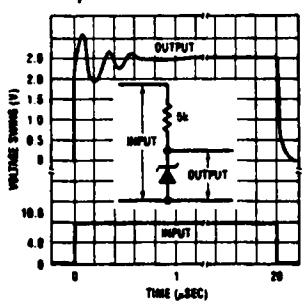
Dynamic Impedance



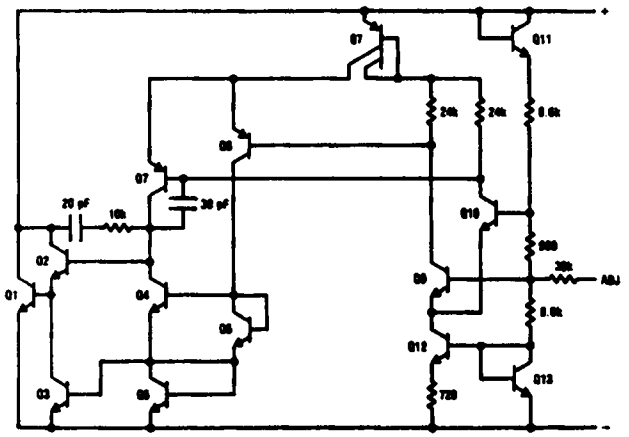
Zener Noise Voltage



Response Time

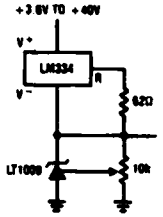


SCHEMATIC DIAGRAM

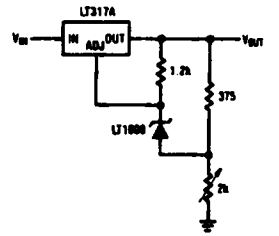


TYPICAL APPLICATIONS

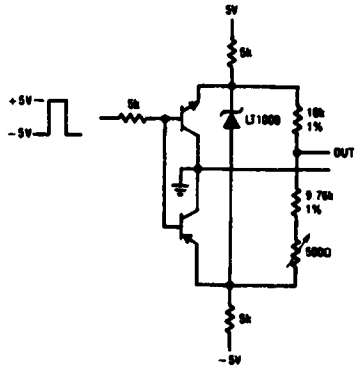
Wide Supply Range, Adjustable Reference



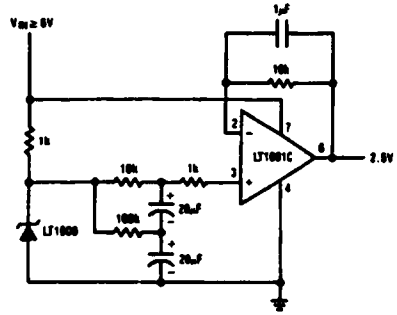
Low Temperature Coefficient Power Regulator



Switchable ±1.25V Bipolar Reference

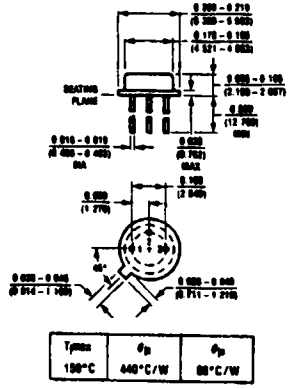


Low Noise 2.5V Buffered Reference



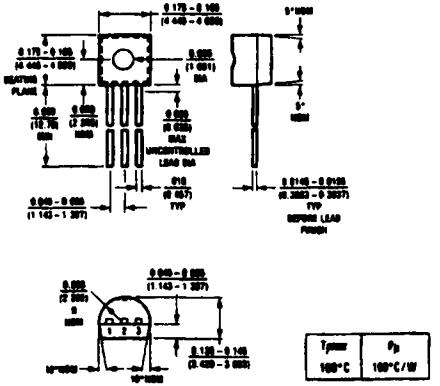
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

H Package
Metal Can



T_{jmax}	θ_{ja}	θ_{jc}
150°C	440°C/W	80°C/W

Z Package
Plastic



T_{jmax}	θ_{ja}
100°C	100°C/W