VLA Technical Report No. 75

VLBI MATRIX SWITCH SYSTEM

T8

T. COTTER

DECEMBER 1997

Table of Contents

I. General Description

The function of the VLBI Matrix Switch System is to provide computer control of the IF inputs to the VLBA Data Acquisition Rack. This system also provides equalization for the four analog sum IFs. The switch system has 24 IF inputs and has the capability of selecting any 4 of those 24 IF inputs. The 24 inputs are broken down as follows: 4 are the analog sums from the correlator, 4 are from an antenna on each arm for a total of 12, and the remaining 8 are auxiliary inputs to be used for special experiments, tests. etc. The antennas on each arm that provide the 12 IF inputs are selected by the NRAO scientific staff and can change. These IFs are connected at the T5 front panel IF monitor point. See Block Diagrams NRAO drawings D15000B01 and C80118Z01.

II. Submodule Description

The T8 module consists of five primary submodules. These submodules are the power supply, the square law detector, the analog sum buffer, the power splitter, and the modified Wandel Goltermann matrix switch.

II.1. The Power Supply

The power is provided by a triple output +15V @ 1.5A, -15V @ 1.5A, and +5V @ 8A linear supply. See NRAO drawing B80118S06.

II.2. The Square Law Detector

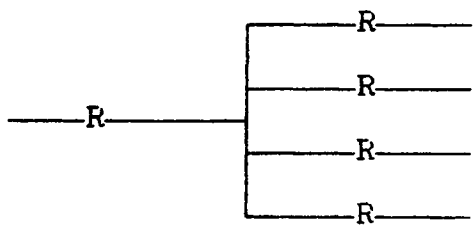
The square law detector submodule (see NRAO drawing C80118S05) consists of 8 two way power dividers, 4 Avantek 462 amplifiers, and 4 generic square law detector modules using BD4 back diodes. The square law detector schematic is show in NRAO drawing C13600S01, and a typical calibration curve is shown Table 1.

Table 1

input pwr dBm	voltage V		input pwr dBm	voltage V
-40	.100		-30	1.08
-39	.130		-29	1.370
-38	.170		-28	1.728
-37	.210		-27	2.144
-36	.260		-26	2.646
-35	.340		-25	3.368
-34	.430		-24	4.277
-33	.540		-23	5.410
-32	.690		-22	6.87
-31	.860		-21	8.44
			-20	10.57

II.3. The Power Splitter

The power splitter submodule consists of two large aluminum plates each with 12 4-way resistive power splitters attached. These plates are in the back of the rack behind the matrix switches. The resistors provide 50 ohm source and load impedances, andwere calculated as follows:



$$\frac{R+50}{4} + R = 50 \qquad R=30 \text{ Ohms}$$

Each power splitter was phase and amplitude matched on a network analyzer. The amplitude was matched within ±.2 dB and the phase was matched to ±.5 degree across a 50MHz bandwidth. Matching was achieved by carefully selecting resistors, and by varying the length and physical position of the resistors within the housings. See NRAO drawings C80117P01 and C80117P02.

II.4 The Analog Sum Buffer

The analog sum buffer submodule consists of 4 amplifier sub-submodules and 4 square law detector sub-submodules. The square law detector modules are the same as those used in II.2. See NRAO drawing C80118S04.

The amplifier sub-submodules are shown schematically in NRAO drawing C80118S01 and the assembly is shown in NRAO drawing C80118P02. These modules are designed to provide simultaneous outputs for both the VLBI and pulsar backends. These outputs are

electrically isolated as well as equalized. Components were chosen with tight tolerances to maintain a ± .5 degree phase match across the passband. The typical analog sum output is shown in Figure 1. The analog sum IFs each had their own passband shape but only one 2-pole filter design could be used to maintain the phase relationship. As the result of using only one design the equalized passband shapes vary in amplitude about ± 1 dB from 0 to 50 MHz. The equalizing filter was designed as follows:

$$C=\frac{1}{(2\pi f_r)^2 L} \qquad L=\frac{R_o(b^2-1)\sqrt{K}}{2\pi f_b b^2(K-1)}$$

$$R=R_o=(K-1) \qquad R_2=\frac{R_o}{K-1} \qquad A_{dB}=20\log K$$

f_r=frequency corresponding to A_{dB} $\quad b=f_b/f_r$

f_b=frequency corresponding to $A_{dB}/2$

R_o=50 ohms

See NRAO drawing C80118S01 for the values calculated for this equalizer. The poles where located at two different frequencies for optimum performance. A 10 dB attenuator was placed between the two poles because of load interactions.

The resultant response is shown in Figure 2.

II.5 The modified Wandel Goltermann Switch

The Wandel Goltermann switch is a 24x1 matrix switch. The original switch had to be modified is two ways. First, the input impedance had to be changed from 75 to 50 ohms. This was done by adding a 150 ohm resistor in parallel with the two parallel 150 ohm

resistors on the input. Second, the computer interface had to be changed so the switch could be operated remotely using the VLA online computing system. This was done by replacing the GPIB card within the switch with a new card. The new card is shown schematically in NRAO drawings C80110S03 and C80110S02. This card uses a programmable Xilinx chip. Along with this new board the address setup for the switch had to be modified. These modifications are shown in the Wandel Goltermann service manual in the back of this report. The new command and monitor protocol is shown in Appendix 1. The monitor and control address requirements for each switch are shown in Table 2.

TABLE 2

Switch	Position 4	Position 5	Address
IFA	down	down	224
IFB	down	up	225
IFC	up	down	226
IFD	up	up	227

III Test Procedure

III.1 Square Law Detector

A. Apply ± 15 and + 5 volts as shown in NRAO drawing C80118S05.

B. Using Table 3 below apply each RF power listed to each input shown in Table 4 and monitor the power at the corresponding output. The power difference between input and output should be 8.5 ± 1 dB. Monitor the voltage readings on the front panel meters and make sure that they correspond to the readings listed in Table 3.

Table 3

RF power dBm	Meter reading counts
-40	860
-36	2144
-33	4277
-30	8440

Table 4

Input	Output
J15	J14
J13	J16
J11	J8
J9	J10

III.2 Analog Sum Buffer

A. Setup

These tests require the use of an HP8407A Network analyzer, HP8601A Sweeper, HP11652-60009 Power divider or equivalents. These tests also require the use of a x-y plotter. Setup the network analyzer system as follows:

Power level -30 dBm @25 MHz

Sweep 1 to 50 MHz

Measurements will require use of the direct port on both the reference and test channels. Select cable lengths to produce a flat phase response with no UUT in place.

Setup and calibrate the x-y plotter to plot the phase.

B. Apply ± 15 and + 5 volts as shown in NRAO drawing C80118S04.

Note: Since the analog sum buffer module consists of two identical channels refer to Table 5 for I/O connections.

Table 5

	input	BB out	PP out	Meter
Channel 1	J15	J11	J13	Top
Channel 2	J16	J14	J12	Bottom

C. Connect the power divider output to the module input. Be sure to terminate unused ports on the channel under test. Connect the network analyzer (test channel) to BB out. The typical display of the magnitude is shown in Figure 3. Switch to phase. Plot the phase on graph paper.

D. Now connect the network analyzer to PP out (remember to terminate BB out with 50 ohms.) The typical magnitude display is shown in Figure 3. Switch to phase. Plot the phase on graph paper.

E. Check to see if the meter is reading something on the front panel.

F. Repeat steps C, D, and E for the other channel.

G. Compare the phase plots for each channel. Phase should be less than ± 1 degree from each other across the band.

III.3 Matrix Switch

A. Setup network analyzer per III.2A

B. Turn the switch on and set to local mode.

C. Connect the network analyzer to the output port.

D. Connect the power divider output to one of the input ports of the switch. Set the front panel selector switch to light the LED that corresponds to port that the power divider is connected to. Note: there are 24 ports.

E. With the network analyzer on magnitude display, measure the insertion loss of the switch. It should be ≤ 1.2 dB.

F. Switch the network analyzer to measure phase. Plot the phase.

G. Cycle through all 24 ports while repeating steps D, E and F. The phase should be the same for all ports within ±.5 degrees across the band.

III.4 Power Splitter

A. Setup network analyzer per III.2A

B. Connect the HP power divider output to the input of the power splitter under test.

C. Connect the network analyzer to one of the output ports of the power splitter. Be sure to terminate the remaining ports.

D. Measure the insertion loss. It should be 12 ±.5 dB.

E. Measure and plot the phase.

F. Repeat steps C, D, and E for each port. The Phase should be within ±.25 degrees between all ports across the band.

III.5 System tests

A. Setup network analyzer per III.2A

B. Connect the output of the HP power divider to the input of one of the system power splitters. Connect the network analyzer test channel to one of the switch outputs.

C. Put the switch in local and select the appropriate position for the system power splitter connected to in B.

D. Measure the insertion loss. It should be 10 ± 2 dB.

E. Measure and plot the phase. The phase variance for the system should be ±3 degrees.

F. Repeat steps B, C, D, and E for all power splitters and all switch outputs.

G. Make sure all switches are in remote.

H. Command each switch using the overlay. Make sure the LED on the front panel corresponds to the commanded position.

IV. APPENDIX 1

Monitor and control protocal uses DCS 0 Dataset 4

Commands

IF selected	Binary Command	LSB	HEX
No selection	0000 0000 0000 0000 0000	0000	000 000
analog sum A	0000 0000 0000 0000 0000	0001	000 001
analog sum B		0010	000 002
analog sum C		0011	000 003
analog sum D		0100	000 004
east arm A		0101	000 005
east arm B		0110	000 006
east arm C		0111	000 007
east arm D		1000	000 008
north arm A		1001	000 009
north arm B		1010	000 00A
north arm C		1011	000 00B
north arm D		1100	000 00C
west arm A		1101	000 00D
west arm B		1110	000 00E
west arm C		1111	000 00F
west arm D		0001 0000	000 010
aux 17		0001 0001	000 011
aux 18		0001 0010	000 012
aux 19		0001 0011	000 013
aux 20		0001 0100	000 014
aux 21		0001 0101	000 015

IF selected	Binary Command	LSB	HEX
aux 22	0001	0110	000 016
aux 23	0001	0111	000 017
aux 24	0001	1000	000 018
no selection	XXXX XXXX XXXX XXXX	XXX1 1XX1	

Monitor

The switch monitor read backs are the same except bit 23 monitors computer/local High=local and bits 16 to 20 monitor the baseband channel value.

Switch Addresses

Address of the top switch that is hard wired to IF A of the DAR is

´220 for command readback

´224 for monitor readback

´320 for command

Address of the second switch that is hard wired to IF B of the DAR is

´221 for command readback

´225 for monitor readback

´321 for command

Address of the third switch that is hard wired to IF C of the DAR is

´222 for command readback

´226 for monitor readback

´322 for command

Address of the fourth switch that is hard wired to IF D of the DAR is

´223 for command readback

´227 for monitor readback

´323 for command

V. FIGURES

Figure 1 Typical Analog Sum Output

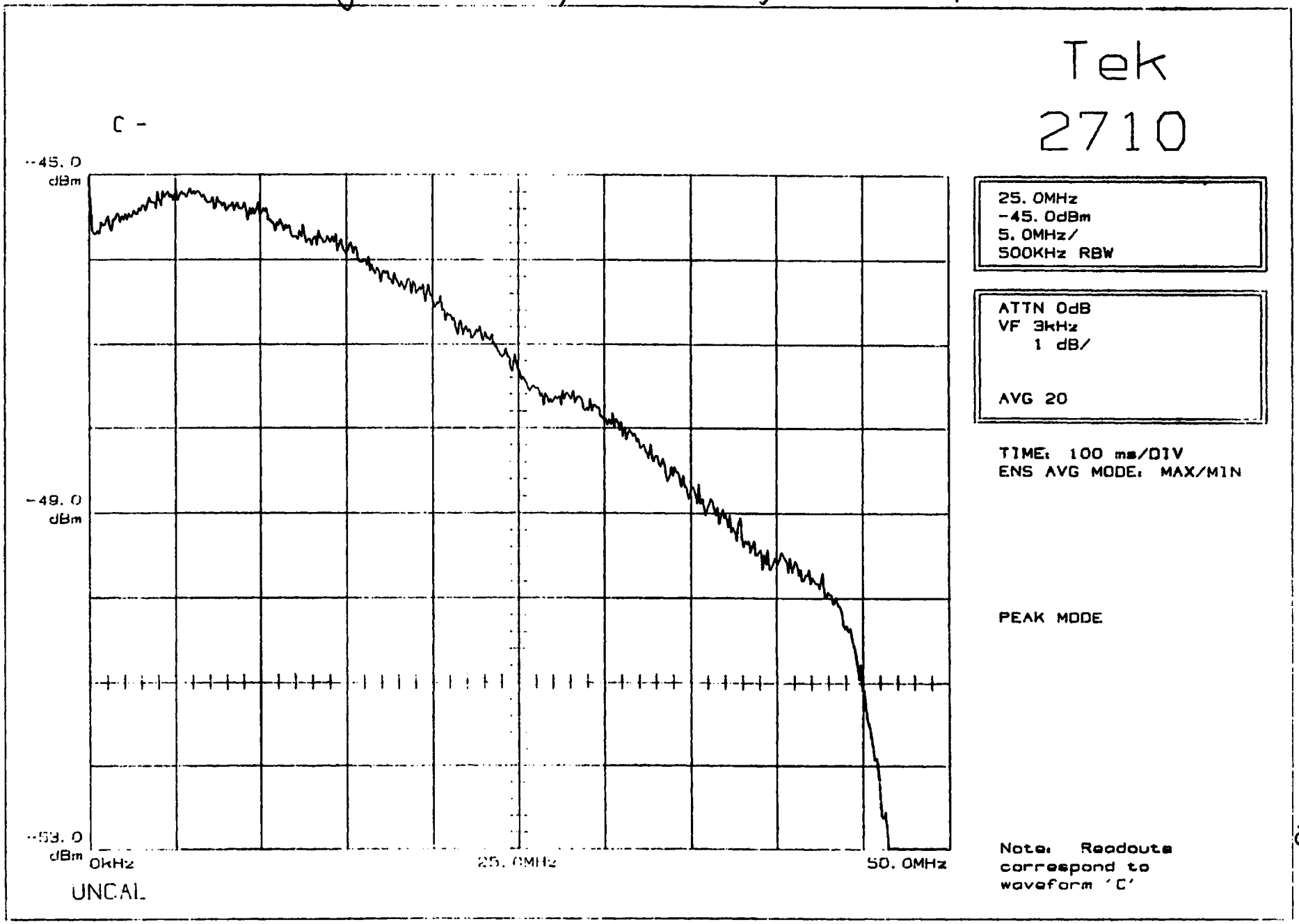
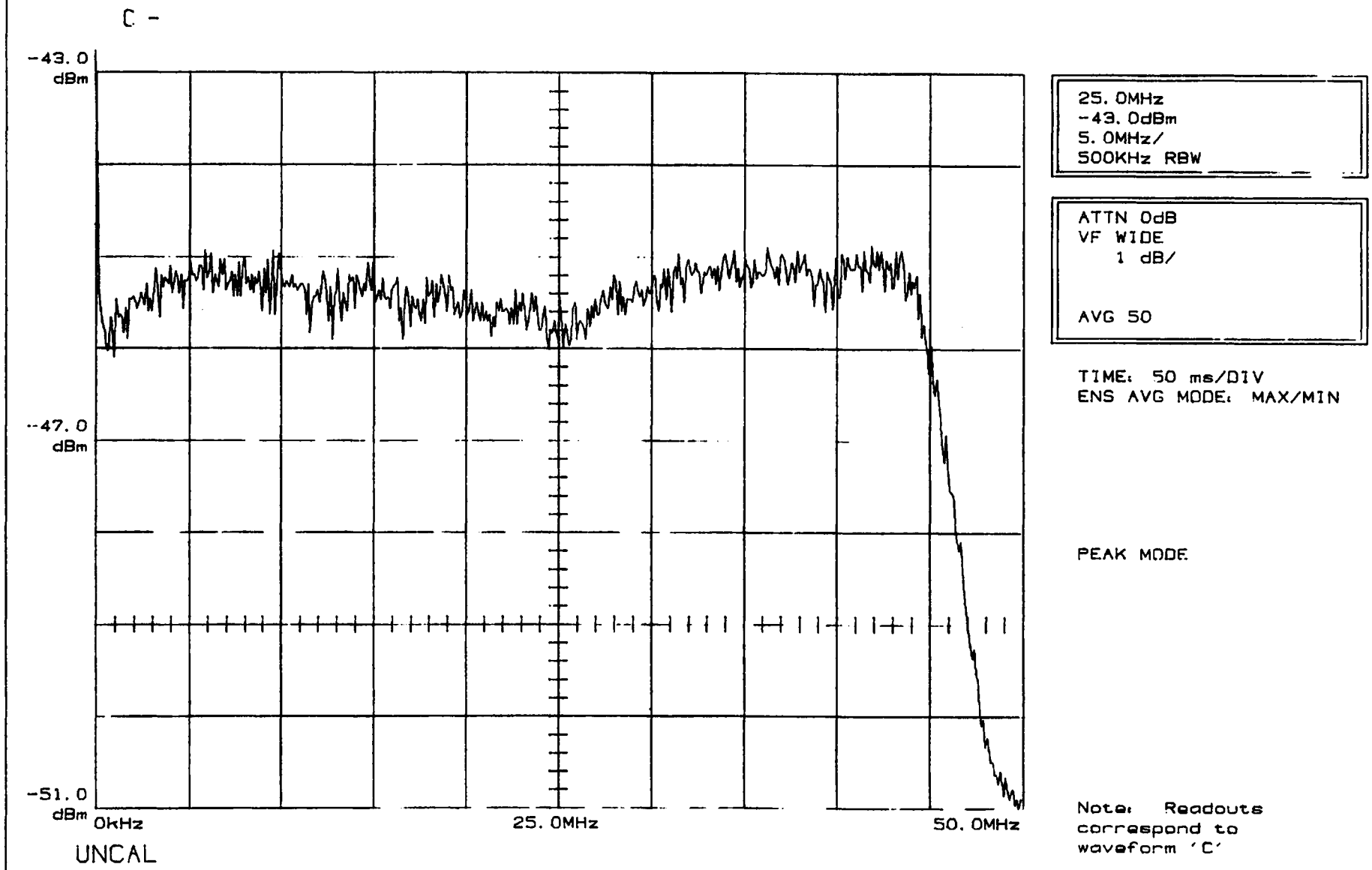
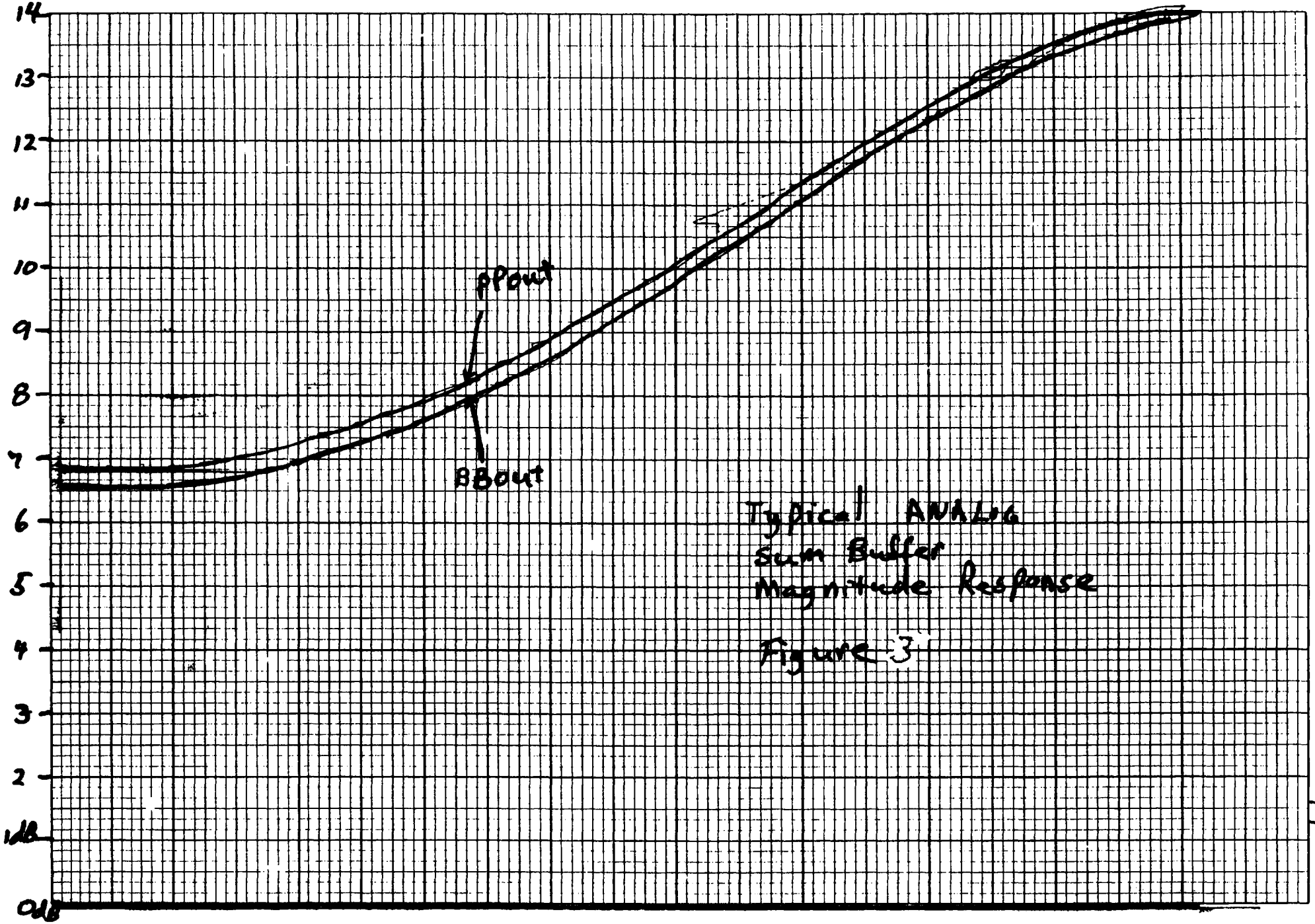


Figure 2 Analog Sum Equalized





Typical ANALOG
Sum Buffer
Magnitude Response

Figure 3

VI. DRAWING LIST

D80117M01 T8 Baseband Switch Module Splitter Box Mounting Plate

C80117M02 T8 Baseband Switch Module Connector Mounting Plate

C80117P01 T8 Baseband Switch Module Splitter Box Mounting Plate

D80117P02 T8 Baseband Switch Module Splitter Box Assembly

C80118AB01 T8 Baseband Switch Analog Sum Buffer Amplifier PCB Artwork

D80118AB02 T8 Baseband Switch Module IF Switch Rear Panel Silkscreen

D80118AB03 T8 Baseband Switch Module IF Switch Front Panel Silkscreen

A80118G01 T8 Baseband Switch Module IF Switch Firmware

C80118M01 T8 Baseband Switch Module Analog Sum Buffer PCB Amplifier Drill DWG

C80118M02 T8 Baseband Switch Module Analog Sum Buffer Amp.PCB Enclosure Box

C80118M03 T8 Baseband Switch Module Analog Sum Buffer Amp.PCB Enclosure Box Lid

D80118M04 T8 Baseband Switch Module IF Switch Rear Panel

D80118M05 T8 Baseband Switch Module IF Switch Front Panel

C80118P01 T8 Baseband Switch Module Analog Sum Buffer Amplifier PCB Assembly

C80118P02 T8 Baseband Switch Module Analog Sum Buffer Amplifier Assembly

C80118S01 T8 Baseband Switch Module Analog Sum Buffer Schematic Diagram

C80118S04 T8 Baseband Switch Module Analog Sum Buffer Module Schematic Diagram

C80118M06 T8 Module Square Law Detector Front Panel

C80118M07 T8 Module Analog Sum Buffer Front Panel

C80118M08 T8 Module 3-Wide Front Panel

C80118S05 T8 Module Square Law Detector Module Schematic Diagram

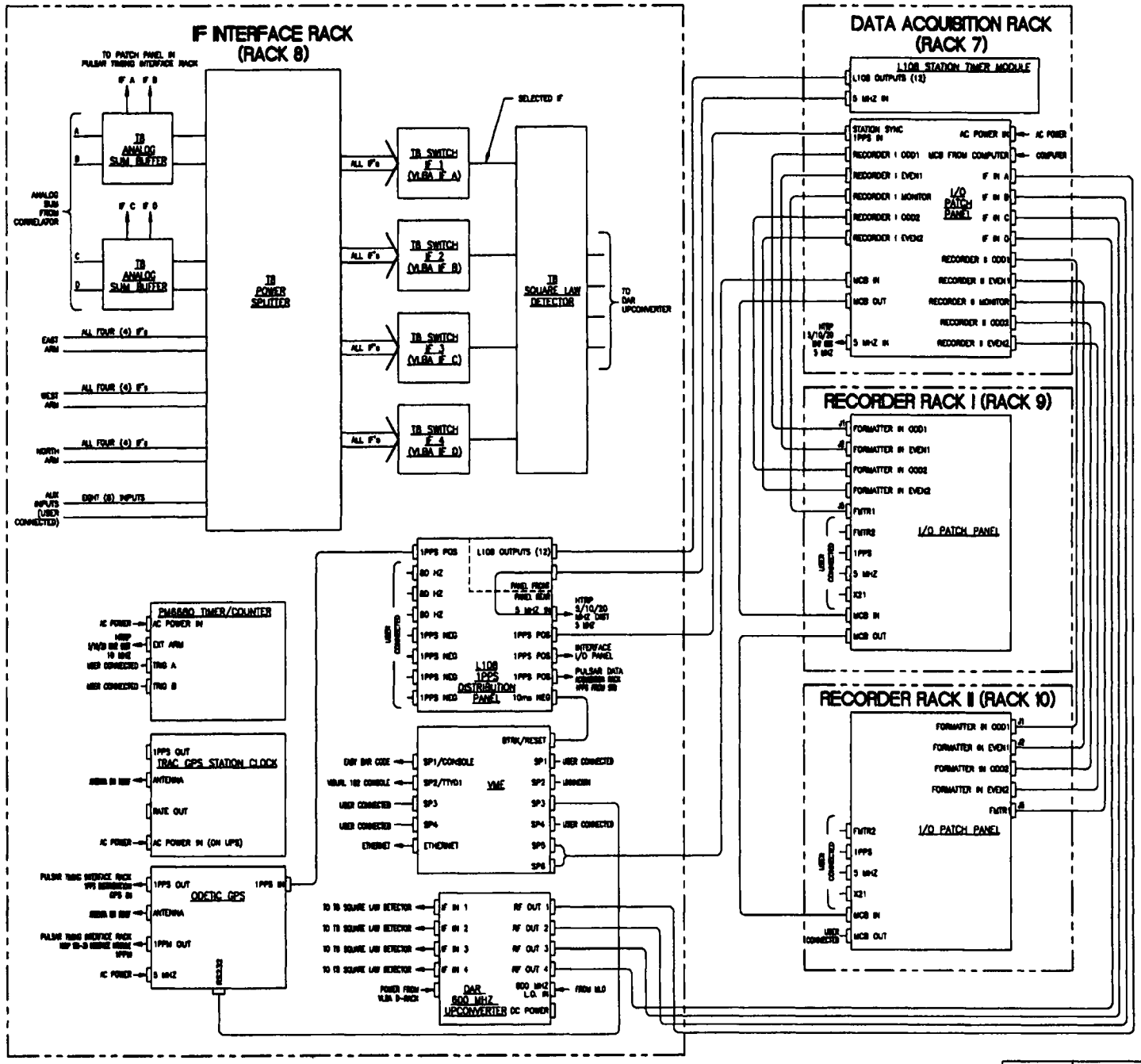
D15000B01 VLBI System Rack Interconnection Block Diagram

D15000P01 VLBI System Rack Layout

C80118Z01 VLBI/Pulsar Multiplex RF Switch Block Diagram Sketch

B80118S06 T8 Module Power Supply Module Schematic Diagram

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	1-95			REMOVED MKII RACK
B	6-95			ADDED RECORDER II
C	12/03/97			ADDED TB POWER SPLITTER



ACAD : 1500081A

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL :

FINISH :

D15000P01 NEXT ASSEMBLY | LAYOUT DWG. TYPE

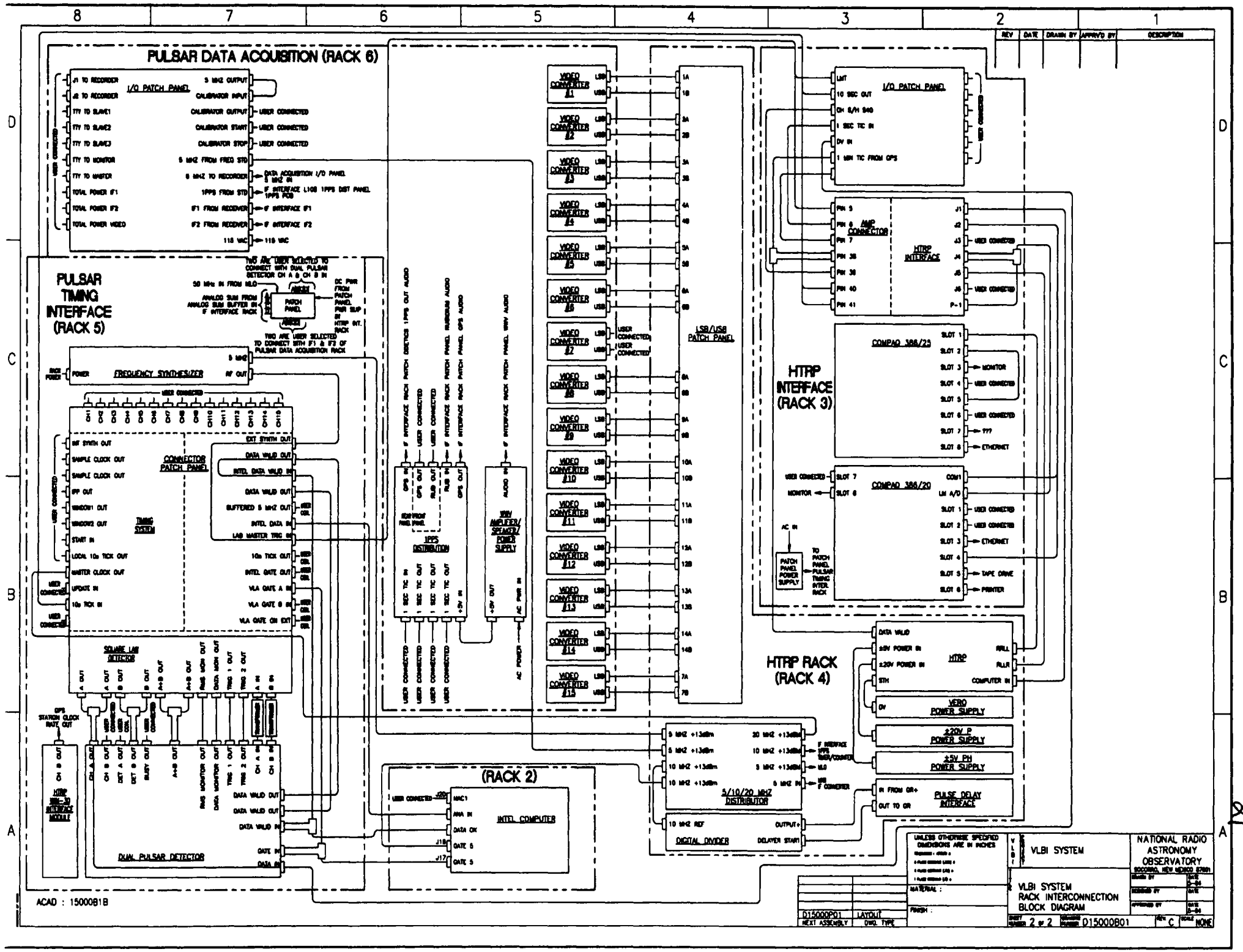
VLBI SYSTEM

VLBI SYSTEM
RACK INTERCONNECTION
BLOCK DIAGRAM

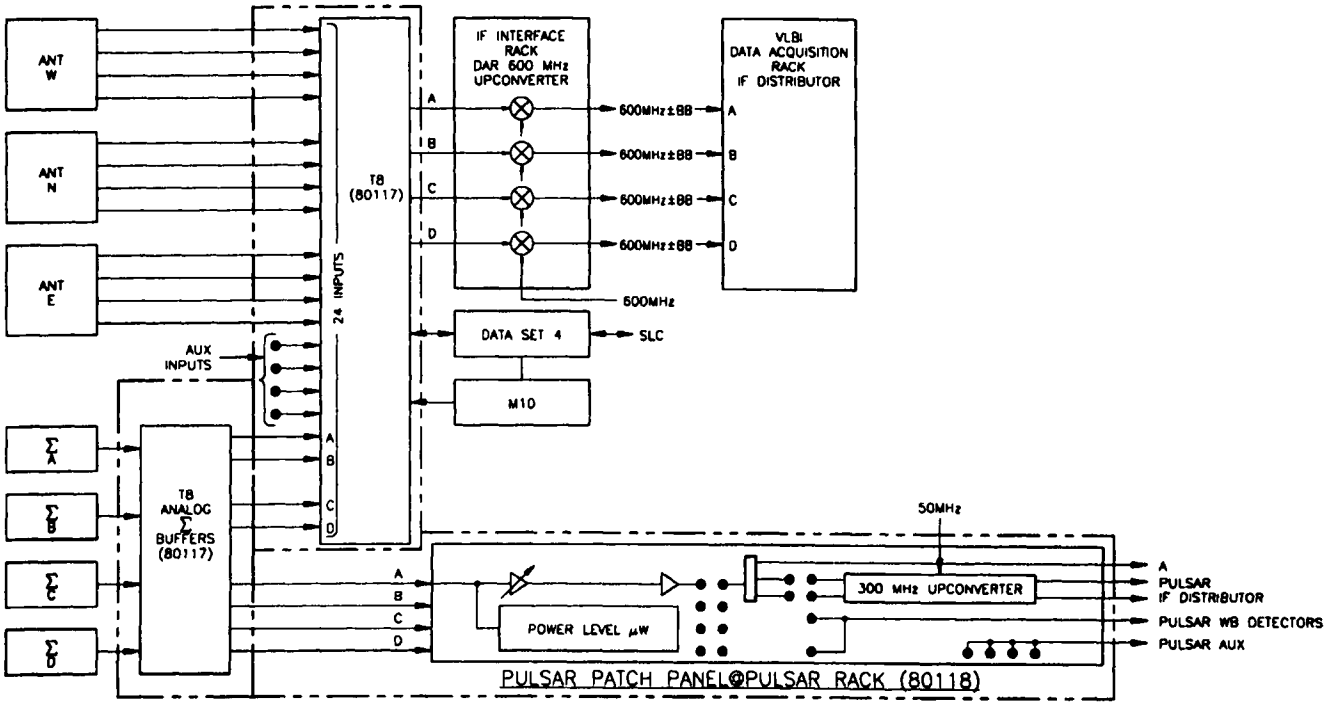
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY
DESIGNED BY
APPROVED BY

SHEET NUMBER 1 of 2 | DRAWING NUMBER D15000B01 | REV C | SCALE NONE


PULSAR DATA ACQUISITION (RACK 6)
I/O PATCH PANEL
PULSAR TIMING INTERFACE (RACK 5)
FREQUENCY SYNTHESIZER
CONNECTOR PATCH PANEL
TIMING SYSTEM
SQUARE LAW DETECTOR
DUAL PULSAR DETECTOR
HTRP 488-30 INTERFACE MODULE
VIDEO CONVERTER
LSB/USB PATCH PANEL
1PPS DISTRIBUTION
WW AMPLIFIER/ SPEAKER/ POWER SUPPLY
HTRP INTERFACE (RACK 3)
AMP CONNECTOR
HTRP INTERFACE
COMPAQ 386/25
COMPAQ 386/20
HTRP RACK (RACK 4)
HTRP
VERO POWER SUPPLY
±20V P POWER SUPPLY
±5V PH POWER SUPPLY
PULSE DELAY INTERFACE
5/10/20 MHZ DISTRIBUTOR
DIGITAL DIVIDER
(RACK 2)
INTEL COMPUTER
ACAD : 15000818
VLBI SYSTEM
NATIONAL RADIO ASTRONOMY OBSERVATORY
VLBI SYSTEM RACK INTERCONNECTION BLOCK DIAGRAM
D15000801
C
NONE

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	12/02/97			ADDED M10 AND AUX INPUT



ACAD : 80118Z1A

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL :

FINISH :

NEXT ASSEMBLY | DWG TYPE

VLBI PROJECT: PULSAR

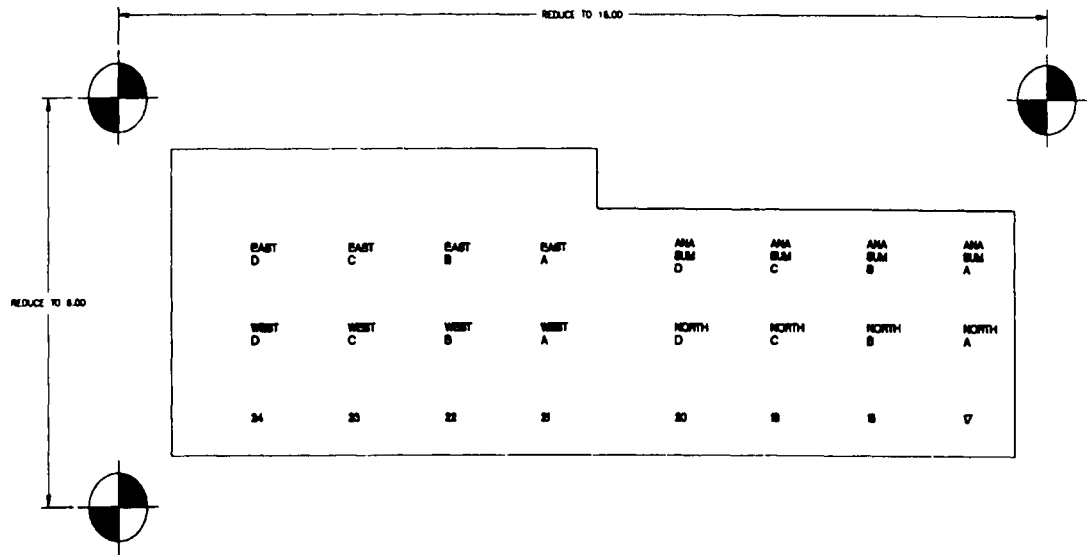
TITLE: PULSAR MULTIPLEX RF SWITCH BLOCK DIAGRAM SKETCH

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY | DATE 8-96
DESIGNED BY | DATE 8-96
APPROVED BY | DATE 8-96

SHEET NUMBER 1 OF 2 | DRAWING NUMBER C80118Z01 | REV A | SCALE NONE

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION



ACAD : 80118AB2

D80118M04	SILKSCREEN
NEXT ASSEMBLY	DWG TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

.005

MATERIAL

FINISH

VLA

T8 MODULE

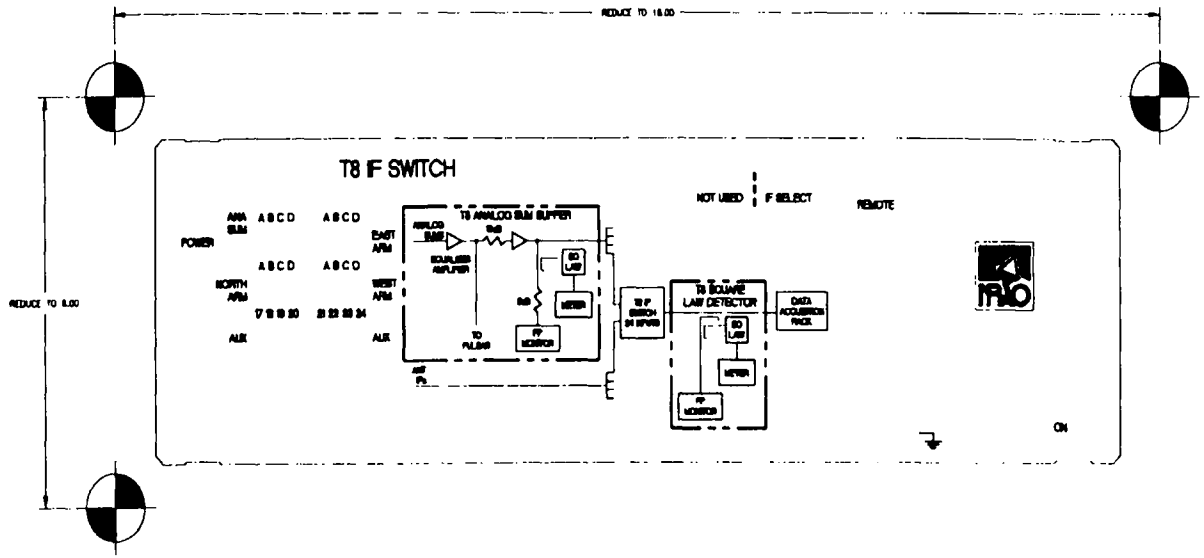
T8 MODULE
IF SWITCH
REAR PANEL
SILKSCREEN

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY — DATE 4/8/97
DESIGNED BY — DATE 4/8/97
APPROVED BY — DATE

SHEET NUMBER 1 of 1 | DRAWING NUMBER D80118AB02 | REV. – | SCALE 1/1

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION



ACAD 80118AB3

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

.005

MATERIAL

FINISH

DB01-18MOD NEXT ASSEMBLY

PANEL DWG

18 MODULE

18 MODULE
F SWITCH
FRONT PANEL
SILKSCREEN

SHEET NUMBER 1 OF 1

DRAWING NUMBER DB01-18A3C3

REV -

SCALE 1/1

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY DATE 4/8/91

DESIGNED BY DATE 4/8/91

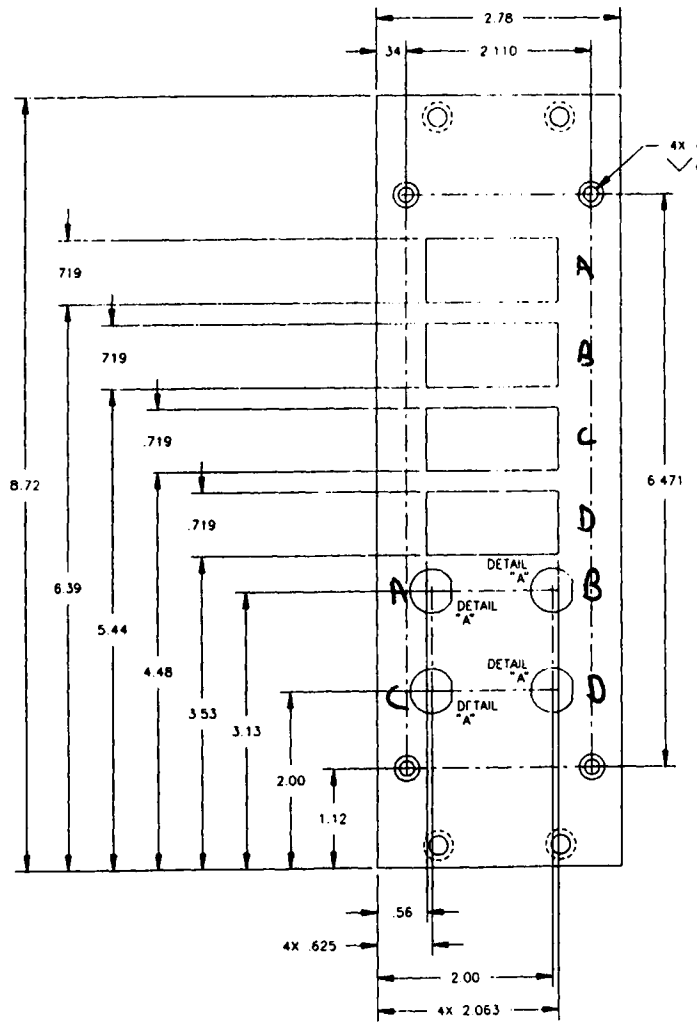
APPROVED BY DATE

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

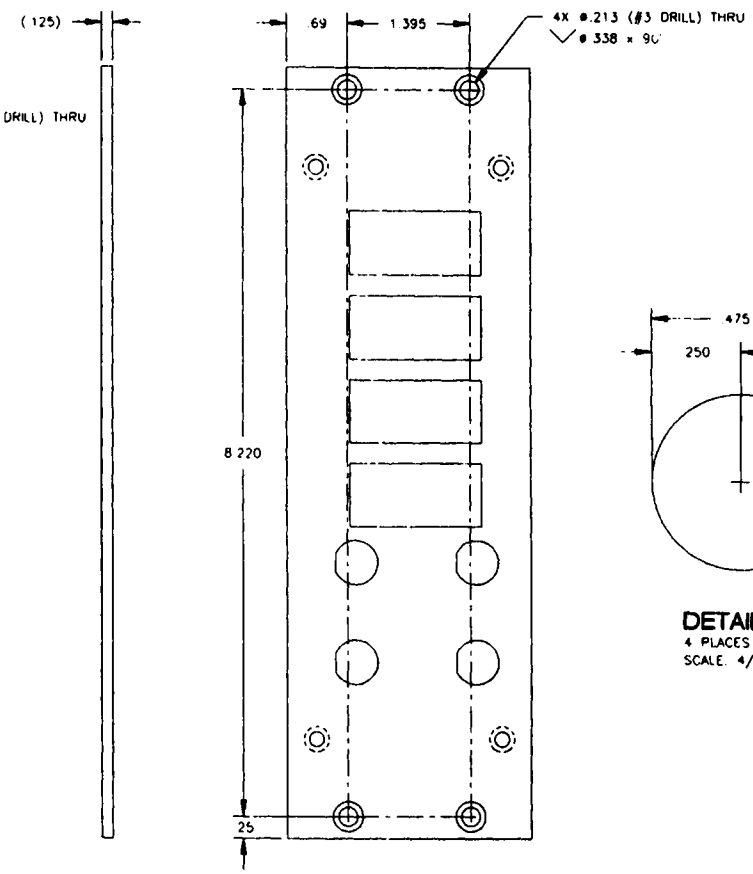
NOTES:

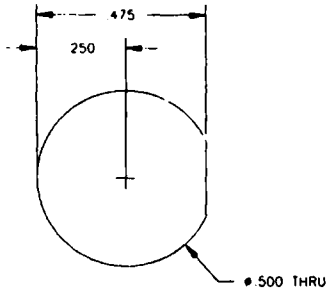
1. REMOVE ALL BURRS AND SHARP EDGES
2. A. FINISH:
   YELLOW CHROMATE CONVERSION ALL OVER

   B. PAINT:
   FRONT SURFACE AND ALL FOUR (4) EDGES
   USING HEWLETT PACKARD MINT GRAY
   PER NRAO SPECIFICATION A13030N01
3. REQUIRED PER ASSEMBLY: 1



FRONT VIEW





DETAIL A
4 PLACES
SCALE: 4/1

ACAD : 80118M06

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	
TOLERANCES ANGLES ±	1°
3 PLACE DECIMALS (.XXX) ±	.005
2 PLACE DECIMALS (.XX) ±	.01
1 PLACE DECIMALS (.X) ±	
MATERIAL :	AL PLATE, .125 THK
FINISH :	

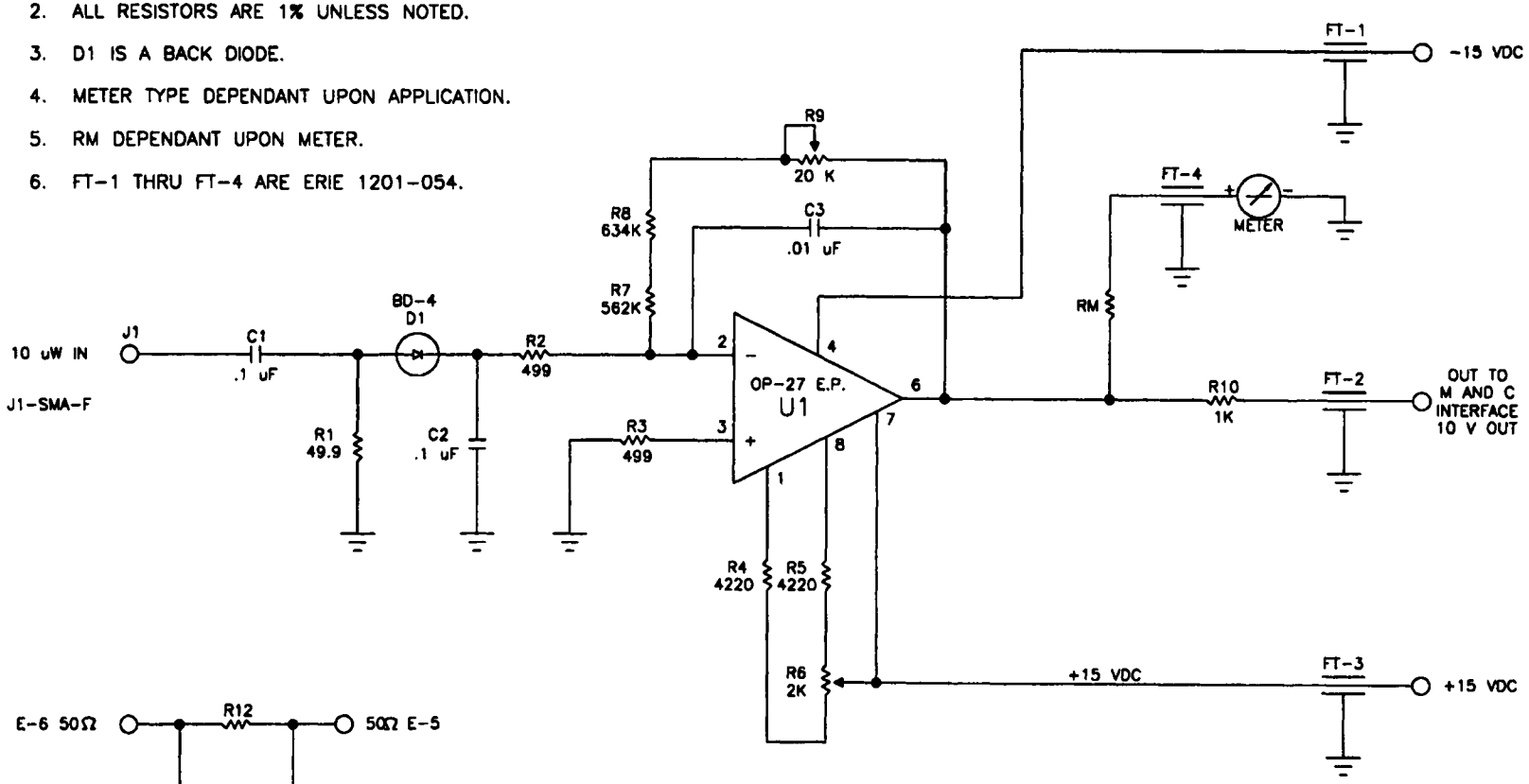
VLA PROJECT	TØ MODULE
TITLE	TØ MODULE SQUARE LAW DETECTOR FRONT PANEL
NATIONAL RADIO ASTRONOMY OBSERVATORY SOCORRO, NEW MEXICO 87801	
DRAWN BY	DATE 4/8/97
DESIGNED BY	DATE 4/8/97
APPROVED BY	DATE
SHEET NUMBER 1 OF 1	DRAWING NUMBER C80118M06
REV ..	SCALE 1/1

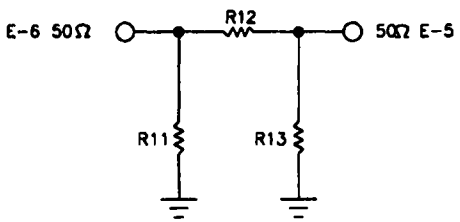
NEXT ASSEMBLY | DWG TYPE

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	2/88			CHANGED C2 VALUE FROM .01uf TO .1 uf
B	10/24/87			UPDATED TO NRAO STANDARDS

NOTES :

1. R7 AND R8 VALUES DEPENDANT UPON D1.
2. ALL RESISTORS ARE 1% UNLESS NOTED.
3. D1 IS A BACK DIODE.
4. METER TYPE DEPENDANT UPON APPLICATION.
5. RM DEPENDANT UPON METER.
6. FT-1 THRU FT-4 ARE ERIE 1201-054.





OPTIONAL INPUT ATTENUATOR

ACAD : 13600S01

NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL :

FINISH :

VLA PROJECT

D-RACK

VLA/JPL INTERFACE
SQUARE LAW
DETECTOR
SCHEMATIC DIAGRAM

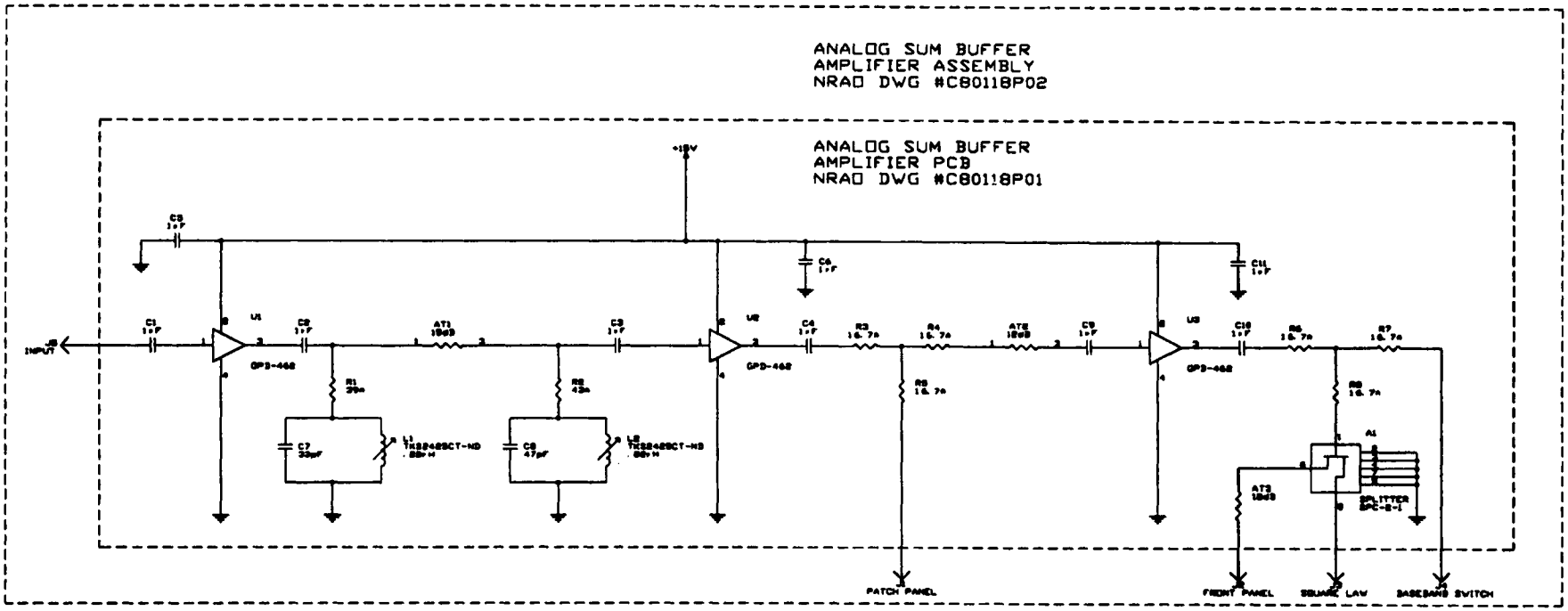
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY		DATE 12/87
DESIGNED BY		DATE 12/87
APPROVED BY		DATE 12/07/87

SHEET NUMBER 1 OF 1 | DRAWING NUMBER C13600S01 | REV. B | SCALE NONE

23

REV.	DATE	DRAWN BY	APPROV'D BY	DESCRIPTION
A	[illegible]/97			REMOVED ARROWS FROM AT1-3



ORCAD : 80118S01

C80118P02	ASSEMBLY
NEXT ASSEMBLY	SWG TYPE

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (X.XXX) ±
2 PLACE DECIMALS (X.XX) ±
1 PLACE DECIMALS (X.X) ±

MATERIAL:

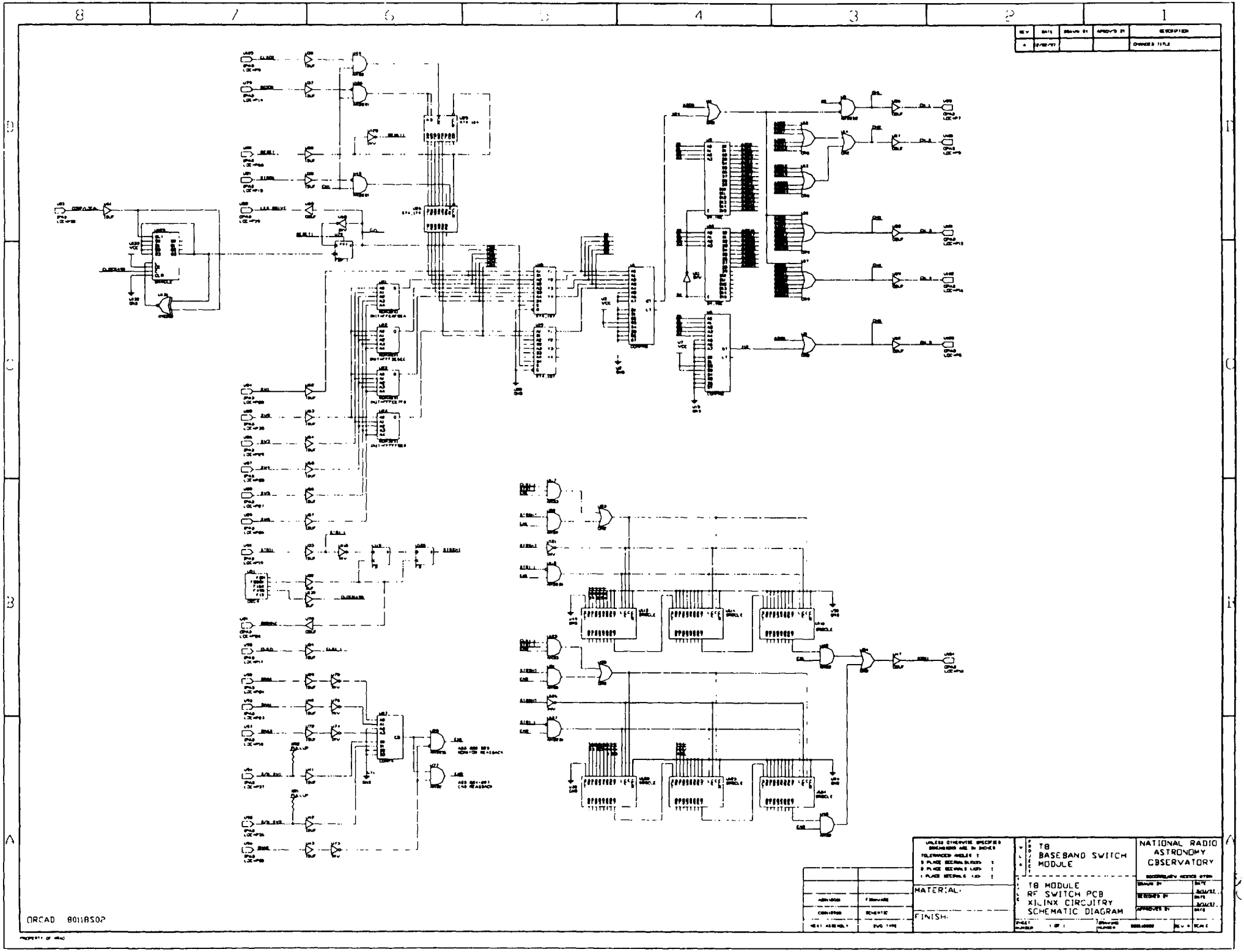
FINISH:

VLA PROJECT: T8 BASEBAND SWITCH MODULE

TITLE: T8 MODULE ANALOG SUM BUFFER AMPLIFIER ASSEMBLY SCHEMATIC DIAGRAM

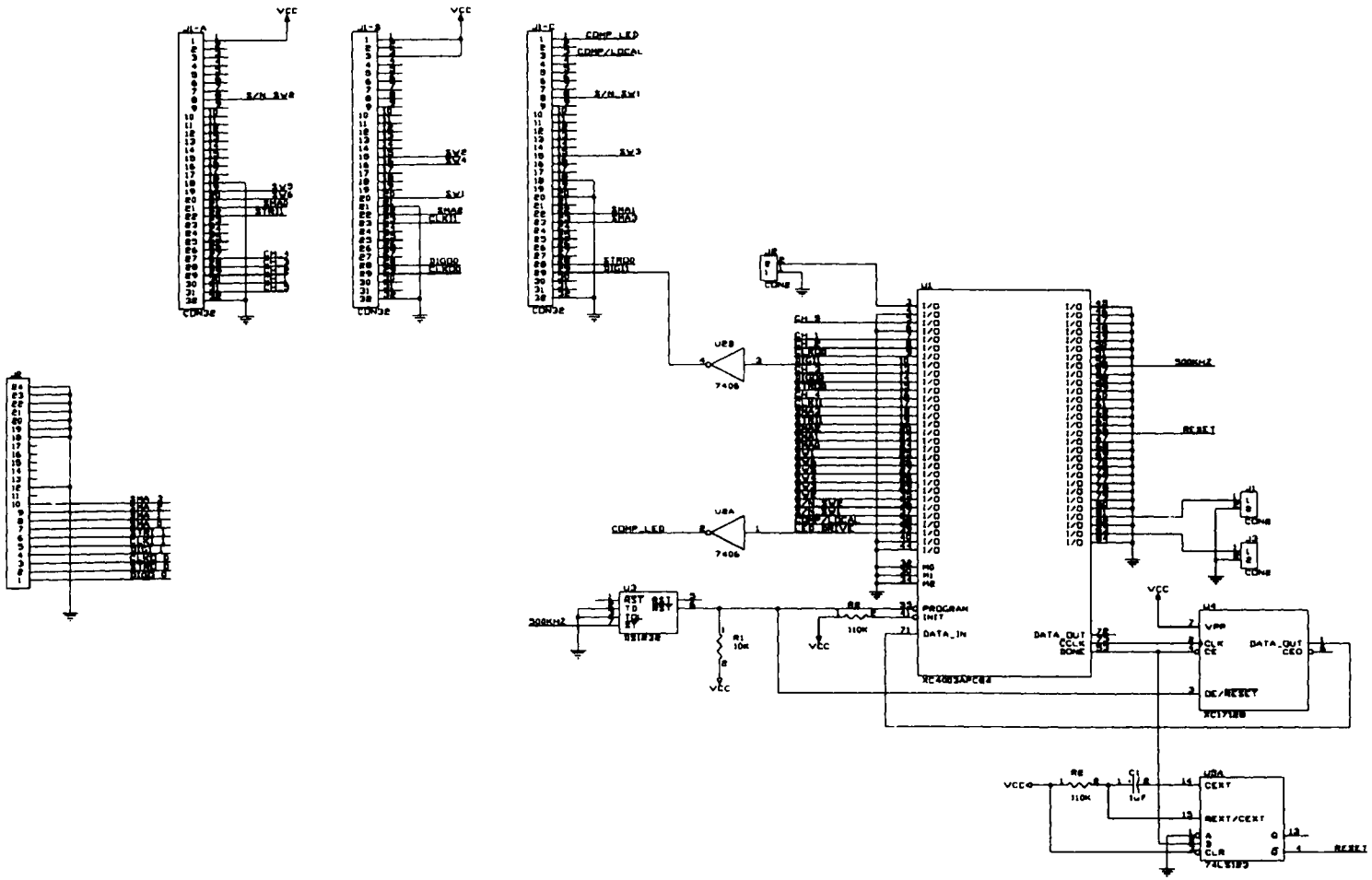
NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY		DATE 1-30-97
DESIGNED BY		DATE 1-30-97
APPROVED BY		DATE 1-30-97
SHEET NUMBER 1 OF 1	DRAWING NUMBER C80118S01	REV. A SCALE -


T8
BASEBAND SWITCH
MODULE
NATIONAL RADIO
ASTRONOMY
OBSERVATORY
T8 MODULE
RF SWITCH PCB
XILINX CIRCUITRY
SCHEMATIC DIAGRAM
MATERIAL:
FINISH:
ORCAD 8011BS02

NOTE: SELECTING SW 0, 25 THRU 29
SELECTS NOTHING

REV	DATE	DRAWN BY	APROV'D BY	DESCRIPTION
A	12/08/97			CHANGED TITLE



SW #	C/H 4-0	CH 9-1
1	00001	00000
2	00010	00001
3	00011	00010
4	00100	00011
5	00101	00100
6	00110	00101
7	00111	00110
8	01000	00111
9	01001	01000
10	01010	01001
11	01011	01010
12	01100	01011
13	01101	10000
14	01110	10001
15	01111	10010
16	10000	10011
17	10001	10100
18	10010	10101
19	10011	10110
20	10100	10111
21	10101	11000
22	10110	11001
23	10111	11010
24	11000	11011

A80118G01	FIRMWARE
D80118S02	SCHEMATIC
NEXT ASSEMBLY	DWG TYPE

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: ANGLES ±
3 PLACE DECIMALS (.XXX) ±
2 PLACE DECIMALS (.XX) ±
1 PLACE DECIMALS (.X) ±

MATERIAL:

FINISH:

VLA

PROJECT
T8
BASEBAND SWITCH
MODULE

TITLE
T8 MODULE
RF SWITCH PCB
SCHEMATIC DIAGRAM

NATIONAL RADIO
ASTRONOMY
OBSERVATORY
SOCORRO, NEW MEXICO 87801

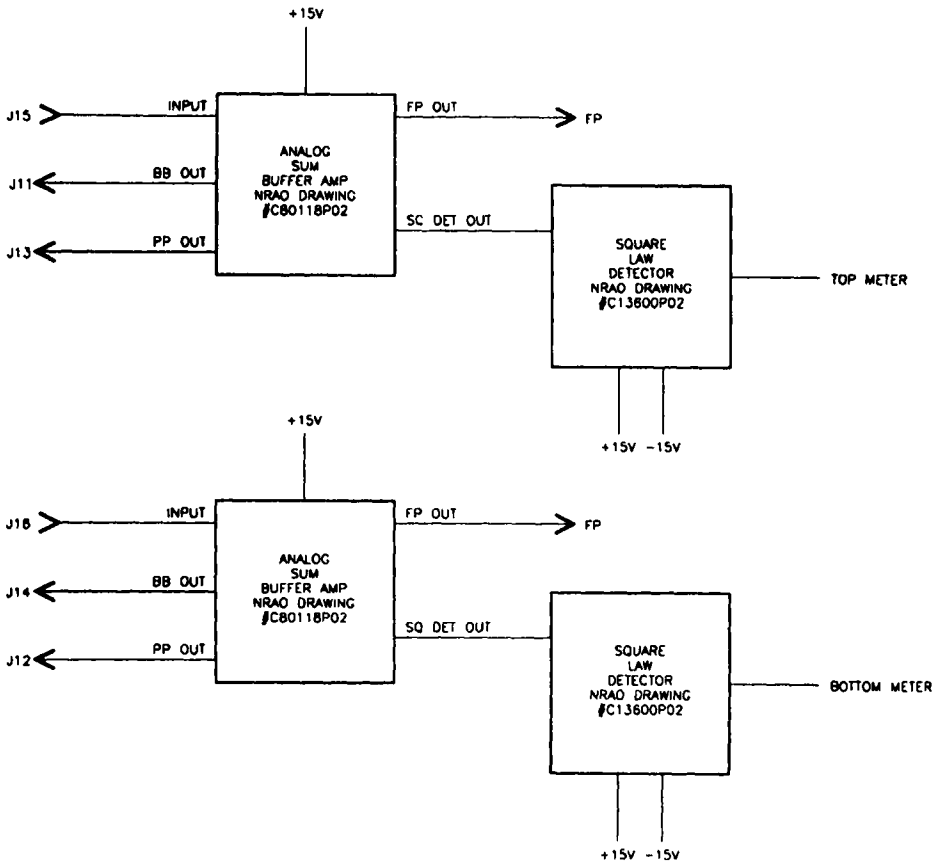
DRAWN BY	DATE 2/11/97
DESIGNED BY	DATE 2/11/97
APPROVED BY	DATE

SHEET NUMBER 1 OF 1
DRAWING NUMBER C80118S03
REV A
SCALE -

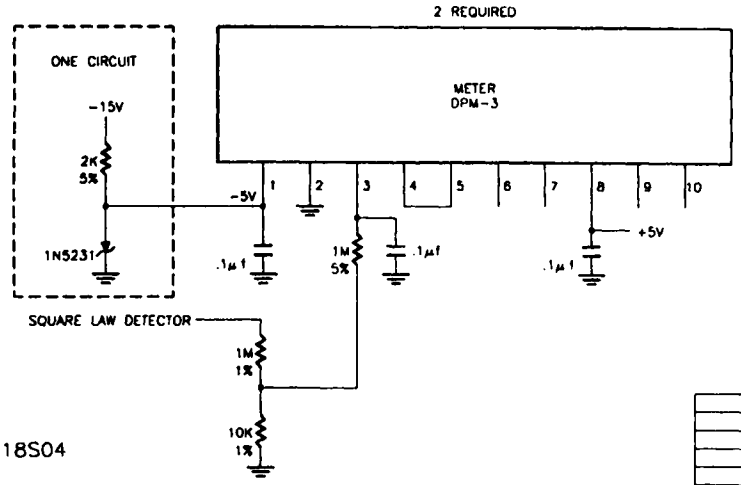
ORCAD : 80118S03

PROPERTY OF NRAO

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	12/02/87			CHANGED BB OUT AND PP OUT JACK NUMBERS



P1 CONNECTOR	
PIN #	FUNCTION
10	+5V
16	+15V
17	-15V
20	SQUARE LAW DETECTOR TOP METER
21	SQUARE LAW DETECTOR TOP METER GND
22	SQUARE LAW DETECTOR BOTTOM METER
23	SQUARE LAW DETECTOR BOTTOM METER GND
34	ANALOG GND (±15V)
42	DIGITAL GND (+5V)



ACAD : 80118S04

NEXT ASSEMBLY	DWG TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL :

FINISH :

VLA PROJECT

T8 BASEBAND SWITCH MODULE

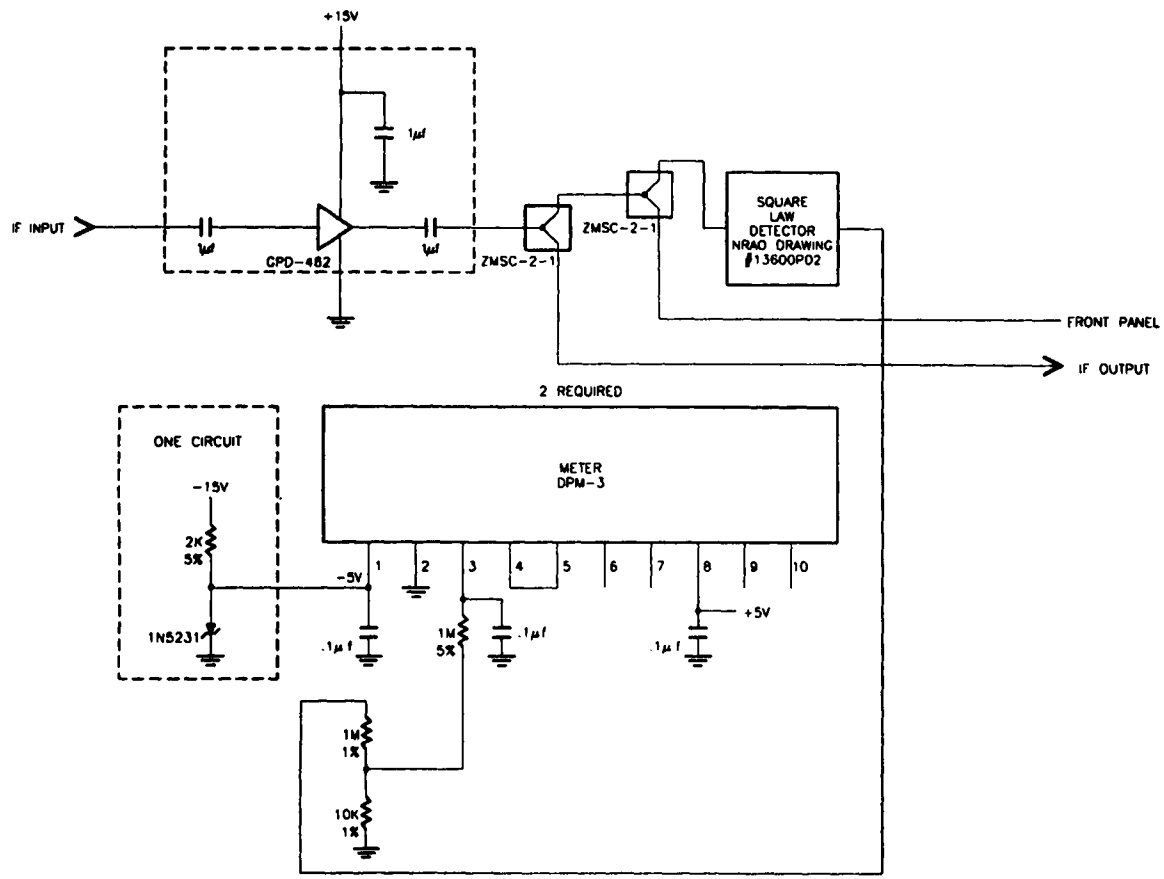
T8 MODULE ANALOG SUM BUFFER MODULE SCHEMATIC DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	DATE 8/20/97
DESIGNED BY	DATE 8/20/97
APPROVED BY	DATE 9/5/97

SHEET NUMBER 1 OF 1 | DRAWING NUMBER C80118S04 | REV A | SCALE NONE

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	12/02/97			REMOVED "D SQUARE LAW DETECTOR"



P1 CONNECTOR	
PIN #	FUNCTION
10	+5V
16	+15V
17	-15V
18	SQUARE LAW DETECTOR IF2
19	SQUARE LAW DETECTOR TOP IF2 GND
20	SQUARE LAW DETECTOR IF1
21	SQUARE LAW DETECTOR IF1 GND
22	SQUARE LAW DETECTOR IF4
23	SQUARE LAW DETECTOR TOP IF4 GND
24	SQUARE LAW DETECTOR IF3
25	SQUARE LAW DETECTOR IF3 GND
34	ANALOG GND (±15V)
42	DIGITAL GND (+5V)

IF INPUTS/OUTPUTS		
IF#	INPUT	INPUT
IF1	J15	J14
IF2	J13	J16
IF3	J11	J8
IF4	J9	J10

ACAD : 80118S05

NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL :

FINISH :

VLA

T8 MODULE

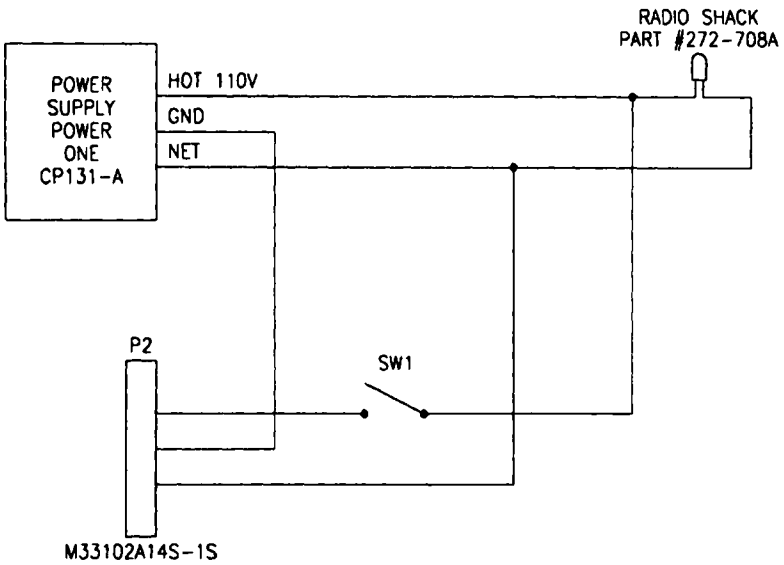
T8 MODULE
SQUARE LAW
DETECTOR MODULE
SCHEMATIC DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY		DATE 8/28/97
DESIGNED BY		DATE 8/28/97
APPROVED BY		DATE 9/8/97

SHEET NUMBER 1 OF 1 | DRAWING NUMBER C80118S05 | REV. A | SCALE NONE

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION



P1 CONNECTOR	
A	+15V
B	GND
C	+5V
D	-15V
E	+15V SEN
F	+15V SEN RTN
H	+5V SEN
J	+5V SEN RTN
K	-15V SEN
L	-15V SEN RTN
HH	GND

P2 CONNECTOR	
A	HOT 110V
B	GND
C	NEUTRAL

ACAD : 80118S06

NEXT ASSEMBLY	DWG. TYPE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES : ANGLES ±
3 PLACE DECIMALS (.XXX) ±
2 PLACE DECIMALS (.XX) ±
1 PLACE DECIMALS (.X) ±

MATERIAL :

FINISH :

VLA PROJECT: T8 BASEBAND SWITCH MODULE

TITLE: T8 MODULE POWER SUPPLY SCHEMATIC DIAGRAM

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

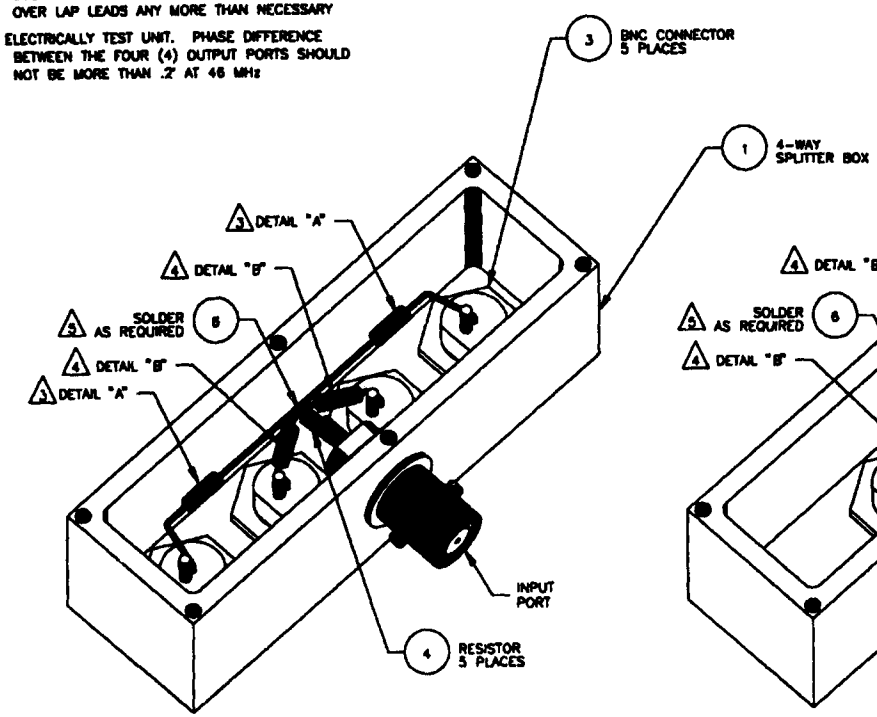
DRAWN BY	DATE 12/05/97
DESIGNED BY	DATE 10/22/97
APPROVED BY	DATE

SHEET NUMBER 1 OF 1 | DRAWING NUMBER B80118S06 | REV. – | SCALE NONE

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION
A	11-13-96			ADD NOTES 3-6; DETAILS A-B

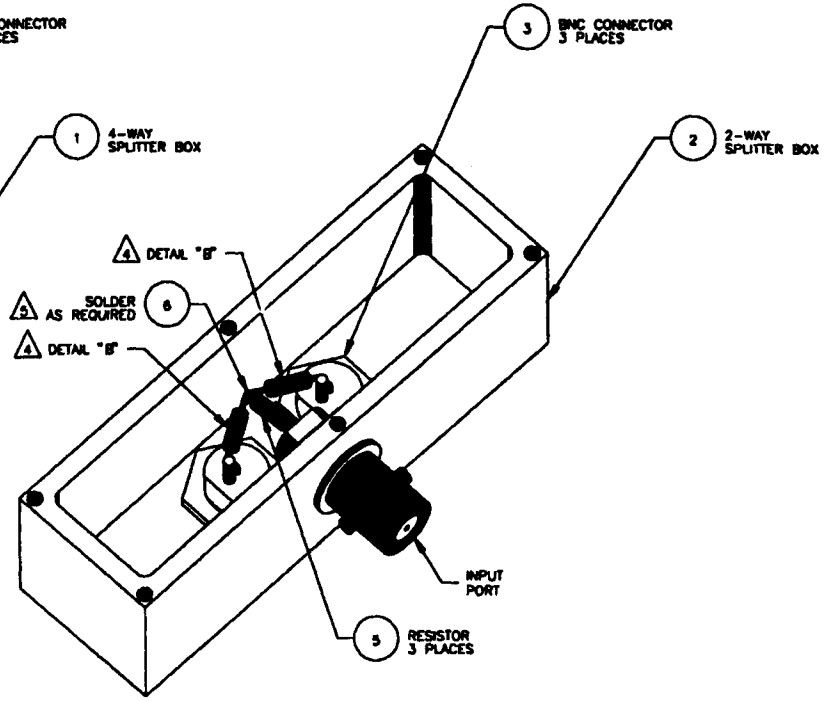
NOTES:

1. REMOVE ALL BURRS AND SHARP EDGES
2. MASK ALL THREADED HOLES BEFORE PLATING
3. TRIM RESISTOR LEADS AS SHOWN IN DETAIL "A"
4. TRIM RESISTOR LEADS AS SHOWN IN DETAIL "B"
5. SOLDER RESISTORS AT THIS POINT. DO NOT OVER LAP LEADS ANY MORE THAN NECESSARY
6. ELECTRICALLY TEST UNIT. PHASE DIFFERENCE BETWEEN THE FOUR (4) OUTPUT PORTS SHOULD NOT BE MORE THAN .2° AT 46 MHz



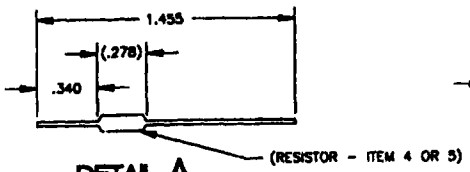
-10 ASSEMBLY

SCALE: 2/1
REQUIRED PER ASSEMBLY: 12



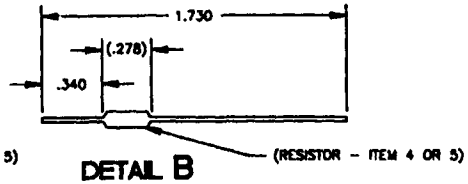
-20 ASSEMBLY

SCALE: 2/1
REQUIRED PER ASSEMBLY: 4



DETAIL A

2 PLACES PER ASSEMBLY
SCALE: 2/1



DETAIL B

2 PLACES PER ASSEMBLY
SCALE: 2/1

ITEM NO.	REF. DES.	MANUFACTURER	PART NUMBER	DESCRIPTION	QTY
6				SOLDER	AR
5		DALE	RN55D	RESISTOR,16.5,1/8W,1%	3
4		DALE	RN55D	RESISTOR,30.1,1/8W,1%	5
3		AMPHENOL	31-221	CONNECTOR, BNC PANEL	8
2		NRAO	C80117P01-2	BOX, 2-WAY SPLITTER	1
1		NRAO	C80117P01-1	BOX, 4-WAY SPLITTER	1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
2 PLACE DECIMALS (.XX) ± .005
3 PLACE DECIMALS (.XXX) ± .01
1 PLACE DECIMALS (.X) ±

MATERIAL :

FINISH :

VLA

T8 MODULE

T8 MODULE SPLITTER BOX ASSEMBLY

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY — DATE 8-96
DESIGNED BY — DATE 8-96
APPROVED BY — DATE 8-96

SHEET NUMBER 1 OF 2 | DRAWING NUMBER C80117P01 | REV. A | SCALE 1/1

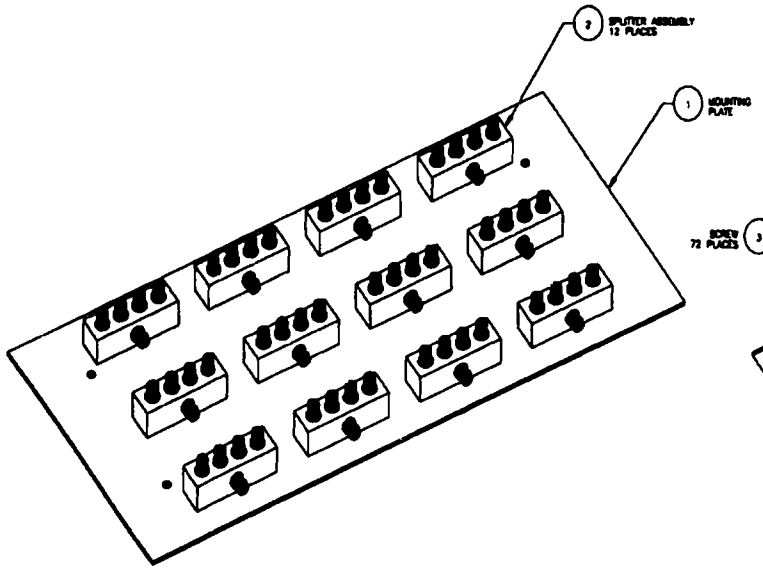
D80117P02	ASSEMBLY
NEXT ASSEMBLY	DWG. TYPE

ACAD : 80117P1A

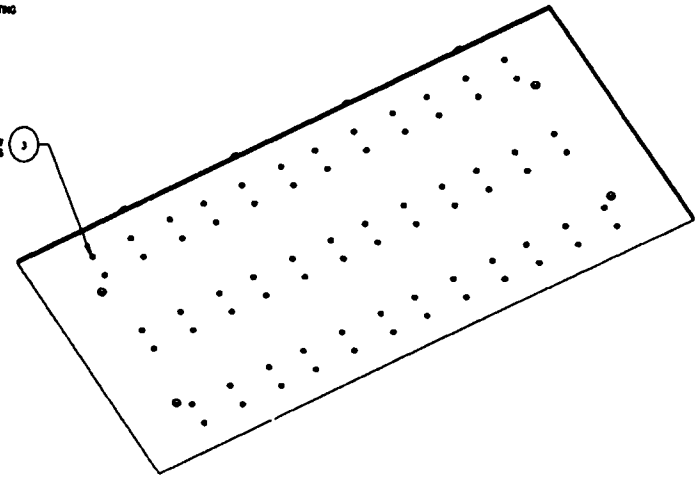
NOTES:

1. REMOVE ALL BURRS AND SHARP EDGES

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION



FRONT VIEW



REAR VIEW

ITEM NO.	REF. DES.	MANUFACTURER	PART NUMBER	DESCRIPTION	QTY
3				SCREW, 1/4-20 x .50	72
2		NRAO	D80117P01-10	ASSEMBLY, SPLITTER BOX	12
1		NRAO	D80117M01	PLATE, MOUNTING	1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMALS ± .XXX ± T
ANGLES ± .XXX ± .005
ANGLES ± .XX ± .01
MATERIAL :
FINISH :

NEXT ASSEMBLY | DWG. TYPE

VLA

TB MODULE

TB MODULE
SPLITTER BOX
MOUNTING PLATE
ASSEMBLY

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY K. SARE DATE 8-88
DESIGNED BY T. COTTON DATE 8-88
APPROVED BY DATE

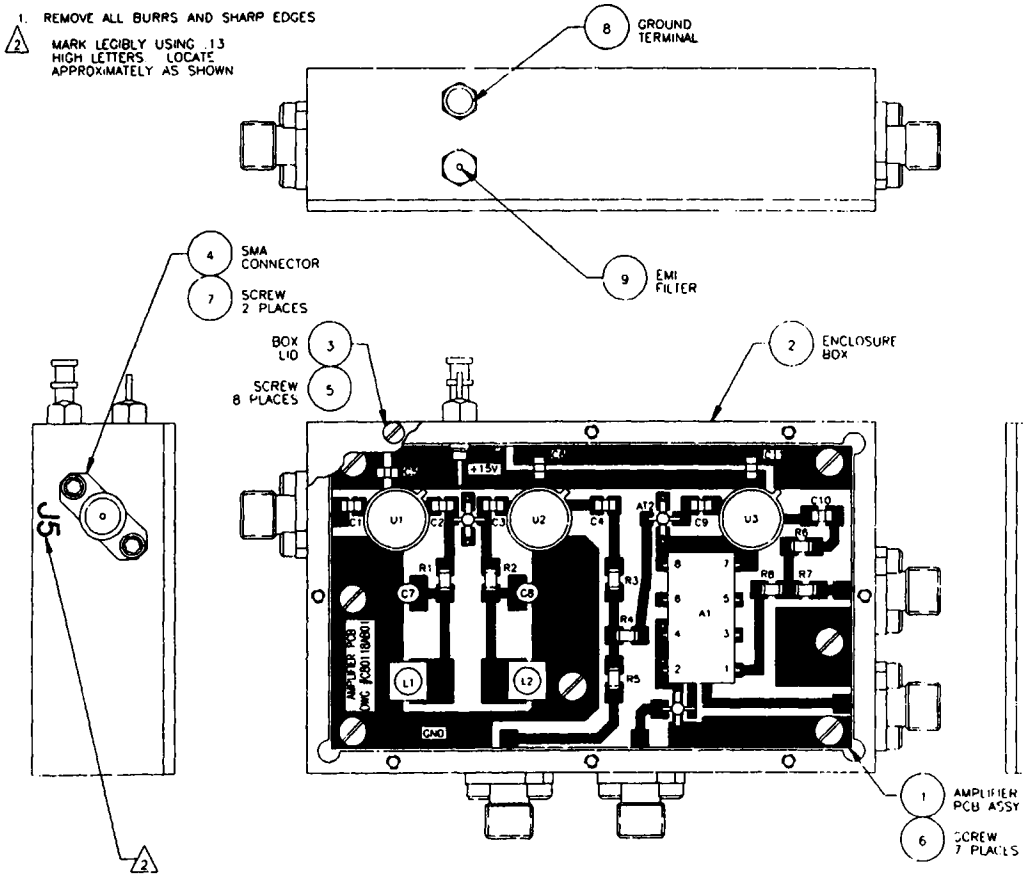
SHEET NUMBER 1 of 1 | DRAWING NUMBER D80117P02 | REV – | SCALE 1/2

ACAD : 80117P02

REV	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

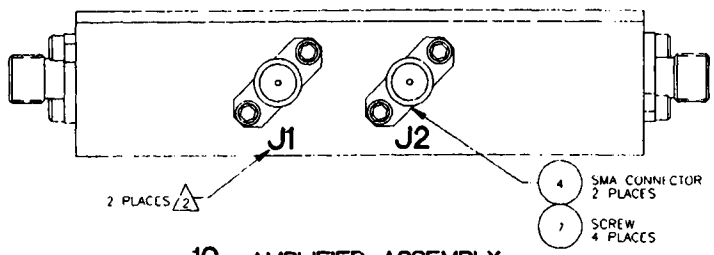
NOTES:

1. REMOVE ALL BURRS AND SHARP EDGES
2. MARK LEGIBLY USING .13 HIGH LETTERS LOCATE APPROXIMATELY AS SHOWN



WIRE LIST

DESIGNATOR	CONNECTED TO
J1	PATCH PANEL
J2	FRONT PANEL
J3	SQUARE LAW
J4	BASEBAND SWITCH
J5	INPUT



-10 AMPLIFIER ASSEMBLY

ITEM NO.	REF. DES	MANUFACTURER	PART NUMBER	DESCRIPTION	QTY
9		SPECTRUM	9900-381-6020	FILTER, EMI, 100pf	1
8		KEYSTONE	1587 1	TERMINAL, GROUND	1
7				SCREW, SOCKET HEAD, SS, #2-56UNC-2A x .125 LONG	10
6				SCREW, PAN HEAD, SS, #2-56UNC-2A x .25 LONG	7
5				SCREW, FLAT HEAD, SS, #0-80UNF-2A x .25 LONG	8
4	J1-J5	M/A COM	2052-5674-02	CONNECTOR, SMA	5
3		NRAO	C80118M03	BOX, LID	1
2		NRAO	C80118M02	BOX, ENCLOSURE	1
1		NRAO	C80118P01	ASSY, AMPLIFIER PCB	1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

MATERIAL

FINISH

PROJECT: T8 BASEBAND SWITCH MODULE

TITLE: T8 MODULE ANALOG SUM BUFFER AMPLIFIER ASSEMBLY

NATIONAL RADIO ASTRONOMY OBSERVATORY
SOCORRO, NEW MEXICO 87801

DRAWN BY	K TATE	DATE 11-7-96
DESIGNED BY	T COTTER	DATE 11-7-96
APPROVED BY		DATE

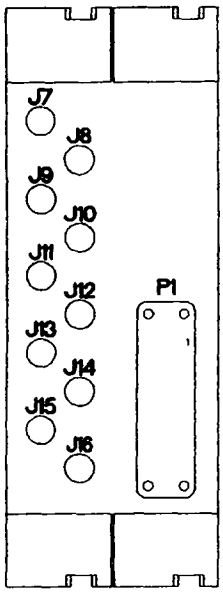
SHEET NUMBER 1 OF 1 | DRAWING NUMBER C80118P02 | REV – | SCALE 2/1

C80118S01 NEXT ASSEMBLY | SCHEMATIC DWG TYPE

ACAD : 80118P02

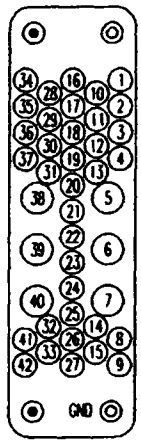
32

VII. MODULE CONNECTORS



DOUBLE WIDE MODULE
(REAR VIEW)

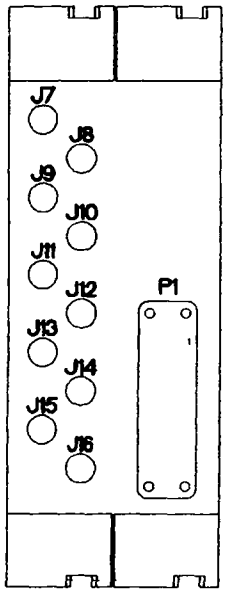
CONN.	FUNCTION
J7	
J8	IF3 Output
J9	IF4 Input
J10	
J11	IF3 Input
J12	
J13	IF2 Input
J14	IF1 Output
J15	IF1 Input
J16	IF2 Output



P1
(REAR VIEW OF CONNECTOR)

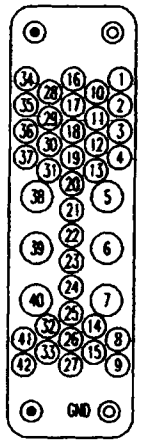
SQUARE LAW DETECTOR MODULE

P11 (42-PIN REAR)					
PIN	**FUNCTION**	**COMMENT**	**PIN**	**FUNCTION**	**COMMENT**
1			22	Detector IF4	
2			23	Detector IF4 Gnd	
3			24	Detector IF3	
4			25	Detector IF3 Gnd	
5			26		
6			27		
7			28		
8			29		
9			30		
10	+5 V		31		
11			32		
12			33		
13			34	Analog Gnd	+/- 15 V
14			35	Digital Gnd	+5 V
15			36		
16	+15 V		37		
17	-15 V		38		
18	Detector IF2		39		
19	Detector IF2 Gnd		40		
20	Detector IF1		41		
21	Detector IF1 Gnd		42		



DOUBLE WIDE MODULE
(REAR VIEW)

CONN.	FUNCTION	
J7		
J8		
J9		
J10		
J11	BB out	Top
J12	PP out	Bottom
J13	PP out	Top
J14	BB out	Bottom
J15	IF in	Top
J16	IF in	Bottom



P1
(REAR VIEW OF CONNECTOR)

ANALOG SUM BUFFER MODULE

P11 (42-PIN REAR)					
PIN	FUNCTION	COMMENT	PIN	FUNCTION	COMMENT
1			22	Detector	Bottom meter
2			23	Detector Gnd	Bottom meter
3			24		
4			25		
5			26		
6			27		
7			28		
8			29		
9			30		
10	+5 V		31		
11			32		
12			33		
13			34	Analog Gnd	+/-15 V
14			35	Digital Gnd	+5 V
15			36		
16	+15 V		37		
17	-15 V		38		
18			39		
19			40		
20	Detector	Top meter	41		
21	Detector Gnd	Top meter	42		

VIII. PARTS

XC17000 Family of Serial Configuration PROMs

Preliminary Product Specifications

Features

- Extended family of one-time programmable (OTP) bit-serial read-only memories used for storing the configuration bitstreams of Xilinx FPGAs
- On-chip address counter, incremented by each rising edge on the clock input
- Simple interface to the FPGA requires only one user I/O pin
- Cascadable for storing longer or multiple bitstreams
- Programmable reset polarity (active High or active Low) for compatibility with different FPGA solutions, (the older XC1736A has active-High reset only)
- XC17128 supports XC4000 fast configuration mode (10 MHz)
- Low-power CMOS EPROM process
- Available in 5 V and 3.3 V versions
- Available in plastic and ceramic packages, and commercial, industrial and military temperature ranges
- Space efficient 8-pin DIP, 8-pin SOIC or 20-pin surface-mount packages.
- Programming support by leading programmer manufacturers.

Description

The XC17000 family of serial configuration PROMs (SCPs) provides an easy-to-use, cost-effective method for storing Xilinx FPGA configuration bitstreams.

When the FPGA is in master serial mode, it generates a configuration clock that drives the SCP. A short access time after the rising clock edge, data appears on the SCP DATA output pin that is connected to the FPGA DIN pin. The FPGA generates the appropriate number of clock pulses to complete the configuration. Once configured, it disables the SCP. When the FPGA is in slave mode, the SCP and the FPGA must both be clocked by an incoming signal.

Multiple devices can be concatenated by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the following device. The clock inputs and the DATA outputs of all SCPs in this chain are interconnected. All devices are compatible and can be cascaded with other members of the family.

For device programming, the XACT development system compiles the LCA design file into a standard Hex format, which is then transferred to the programmer.

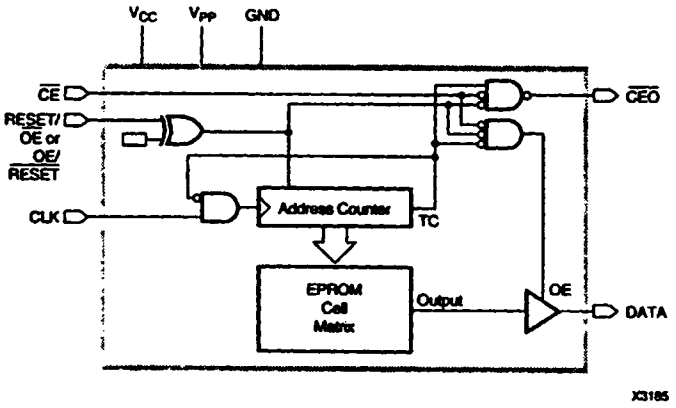


Figure 1. Simplified Block Diagram (does not show programming circuit)

Pin Assignments

DATA
Data output, 3-stated when either $\overline{CE}$ or $\overline{OE}$ are inactive. During programming, the DATA pin is I/O. Note that $\overline{OE}$ can be programmed to be either active High or active Low.

CLK
Each rising edge on the CLK input increments the internal address counter, if both $\overline{CE}$ and $\overline{OE}$ are active. Note that $\overline{OE}$ can be programmed to be either active High or active Low.

RESET/$\overline{OE}$
When High, this input holds the address counter reset and 3-states the DATA output. The polarity of this input pin is programmable as either RESET/$\overline{OE}$ or OE/$\overline{RESET}$. To avoid confusion, this document describes the pin as RESET/$\overline{OE}$, although the opposite polarity is possible on all devices except the older XC1736A.

$\overline{CE}$
When High, this pin disables the internal address counter, 3-states the DATA output, and forces the device into low-I_{CC} standby mode.

$\overline{CEO}$
Chip Enable output, to be connected to the CE input of the next SCP in the daisy chain. This output is Low when the $\overline{CE}$ and $\overline{OE}$ inputs are both active AND the internal address counter has been incremented beyond its Terminal Count (TC) value. In other words: when the PROM has been read, $\overline{CEO}$ will follow $\overline{CE}$ as long as $\overline{OE}$ is active. When $\overline{OE}$ goes inactive, $\overline{CEO}$ stays High until the PROM is reset. Note that $\overline{OE}$ can be programmed to be either active High or active Low.

V_{PP}
Programming voltage. No overshoot above the specified max voltage is permitted on this pin. For normal read operation, this pin *must* be connected to V_{CC}. Failure to do so may lead to unpredictable, temperature-dependent operation and severe problems in circuit debugging. *Do not leave V_{PP} floating!*

V_{CC}
Positive supply pin.

GND
Ground pin

Serial PROM Pinouts

Pin Name	8-Pin	20-Pin
DATA	1	2
CLK	2	4
RESET/$\overline{OE}$ (OE/$\overline{RESET}$)	3	6
CE	4	8
GND	5	10
CEO	6	14
V_{PP}	7	17
V_{CC}	8	20

Capacity

Device	Configuration Bits
XC1718D or L	18,144
XC1736D or L	36,288
XC1765D or L	65,536
XC17128	131,072

plus 32 bits for reset polarity control

Number of Configuration Bits, Including Header for all Xilinx FPGAs and Compatible SCP Type

Device	Configuration Bits	SCP
XC2064	12,038	XC1718
XC2018	17,878	XC1718
XC3020/3120	14,819	XC1718
XC3030/3130	22,216	XC1736
XC3042/3142	30,824	XC1736
XC3064/3164	46,104	XC1765
XC3090/3190	64,200	XC1765
XC3195	94,984	XC17128
XC4002A	31,668	XC1736
XC4003A	45,676	XC1765
XC4003H	53,967	XC1765
XC4004A	62,244	XC1765
XC4005A	81,372	XC17128
XC4005/4005H	95,000	XC17128
XC4006	119,832	XC17128
XC4008	147,544	XC17128 + XC1718
XC4010	178,136	XC17128 + XC1765
XC4013	247,960	XC17128 + XC17128
XC4025	422,168	XC17128 + XC17128 + XC17128 + XC1736

Controlling Serial PROMs

Most connections between the LCA device and the Serial PROM are simple and self-explanatory.

- The DATA output of the PROM drives DIN of the LCA devices.
- The master LCA CCLK output drives the CLK input of the Serial PROM.
- The $\overline{CEO}$ output of any Serial PROM can be used to drive the $\overline{CE}$ input of the next serial PROM in a cascade chain of PROMs.
- V_{PP} *must* be connected to V_{CC}. Leaving V_{PP} open can lead to unreliable, temperature-dependent operation.

There are, however, two different ways to use the inputs $\overline{CE}$ and $\overline{OE}$.

1. The LCA D/$\overline{P}$ or LDC output drives both $\overline{CE}$ and $\overline{OE}$ in parallel. This is the simplest connection, but it fails if a user applies $\overline{RESET}$ during the LCA configuration process. The LCA device aborts the configuration and then restarts a new configuration, as intended, but the Serial PROM does not reset its address counter, since it never saw a High level on its $\overline{OE}$ input. The new configuration, therefore, reads the remaining data in the PROM and interprets it as preamble, length count etc. Since the LCA device is the master, it issues the necessary number of CCLK pulses, up to 16 million (2^{24}) and D/$\overline{P}$ goes High. However, the LCA configuration will be completely wrong, with potential contentions inside the LCA device and on its output pins. *This method must, therefore, never be used when there is any chance of external reset during configuration.*

2. The LCA D/$\overline{P}$ or LDC output drives only the $\overline{CE}$ input of the Serial PROM while its $\overline{OE}$ input is driven by the LCA $\overline{RESET}$ input. This connection works under all normal circumstances, even when the user aborts a configuration before D/$\overline{P}$ has gone High. The Low level on the OE input during reset clears the PROM internal address pointer, so that the reconfiguration starts at the beginning. The reset polarity should be inverted for this mode to be used. It is strongly recommended that this method, shown in Figure 2, be used whenever possible.

LCA Master Serial Mode Summary

The I/O and logic functions of the Logic Cell Array and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three LCA mode pins. In Master Mode, the Logic Cell Array automatically loads the configuration program from an external memory. The Serial Configuration PROM has been designed for compatibility with the Master Serial Mode.

Upon power-up or reconfiguration, an LCA device enters the Master Serial Mode whenever all three of the LCA mode-select pins are Low (M0=0, M1=0, M2=0). Data is read from the Serial Configuration PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master Serial Mode provides a simple configuration interface. Only a serial data line and two control lines are required to configure an LCA device. Data from the Serial Configuration PROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK.

If the user-programmable, dual-function DIN pin on the LCA device is used only for configuration, it must still be held at a defined level during normal operation. The XC3000 and XC4000 families take care of this automatically with an on-chip default pull-up resistor. With XC2000-family devices, the user must either configure DIN as an active output, or provide a defined level, e.g., by using an external pull-up resistor, if DIN is configured as an input.

Programming the LCA With Counters Unchanged Upon Completion

When multiple LCA-configurations for a single LCA are stored in a Serial Configuration PROM, the $\overline{OE}$ pin should be tied Low as shown in Figure 3. Upon power-up, the internal address counters are reset and configuration begins with the first program stored in memory. Since the $\overline{OE}$ pin is held Low, the address counters are left unchanged after configuration is complete. Therefore, to reprogram the LCA with another program, the D/$\overline{P}$ line is pulled Low and configuration begins at the last value of the address counters.

Cascading Serial Configuration PROMs

For multiple LCAs configured as a daisy-chain, or for future LCAs requiring larger configuration memories, cascaded SCPs provide additional memory. After the last bit from the first SCP is read, the next clock signal to the SCP asserts its $\overline{CEO}$ output Low and disables its DATA line. The second SCP recognizes the Low level on its $\overline{CE}$ input and enables its DATA output. See Figure 2.

After configuration is complete, the address counters of all cascaded SCPs are reset if the LCA $\overline{RESET}$ pin goes Low, assuming the SCP reset polarity option has been inverted.

If the address counters are not to be reset upon completion, then the RESET/$\overline{OE}$ inputs can be tied to ground, as shown in Figure 3. To reprogram the LCA device with another program, the D/$\overline{P}$ line goes Low and configuration begins where the address counters had stopped. In this case, avoid contention between DATA and the configured I/O use of DIN.

When more than a few SCPs are daisy-chained, the designer must evaluate the worst-case CCLK-to-DATA delay resulting from the cascaded $\overline{CE}$-to-$\overline{CEO}$ delays. All Xilinx LCA devices require valid input data a set-up time before the next rising CCLK edge.

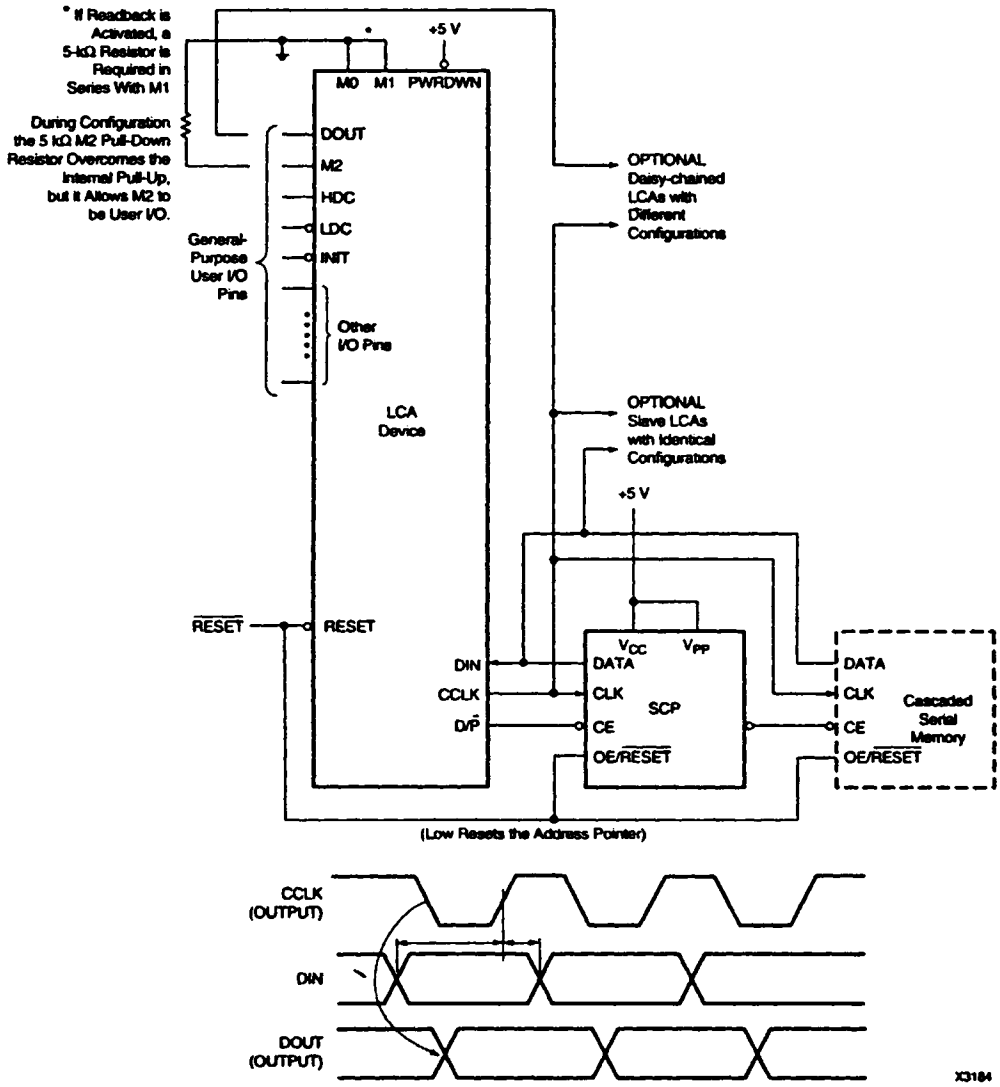
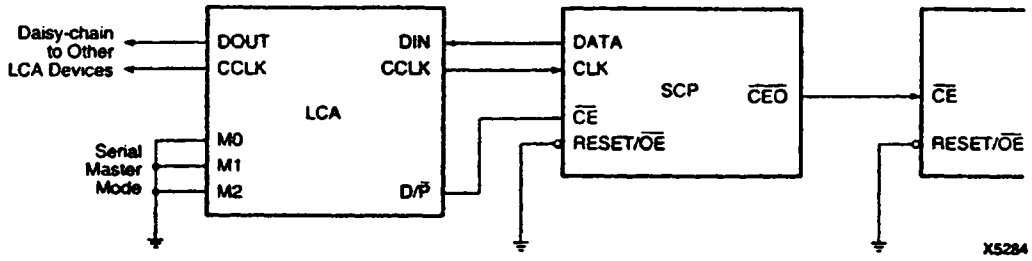


Figure 2. Master Serial Mode. The one-time-programmable Serial Configuration PROM supports automatic loading of configuration programs. Multiple devices can be cascaded to support additional LCA devices. An early D/P̄ inhibits the PROM data output one CCLK cycle before the LCA I/Os become active.



Notes: 1. If programmed for active High Reset, tie RESET to V_{CC}.
2. If M2 is tied directly to ground, it should be programmed as an input during operation.
3. If the LCA is reset during configuration, it will abort back to initialization state. An external signal is then required to reset the XC17XX counters.

Figure 3. Address Counters Not Reset at the End of Configuration

Standby Mode

The PROM enters a low-power standby mode whenever $\overline{CE}$ is asserted High. In this mode, the SCP consumes less than 0.5 mA of current. The output remains in a high-impedance state regardless of the state of the $\overline{OE}$ input.

Reducing Standby Current to Zero

The 0.5 mA of serial PROM standby current may be unacceptable in a low-current application. It is, however, possible to achieve zero standby current by disconnecting the PROM ground lead from system ground and connecting it to the $\overline{LDC}$ pin of the LCA, as shown in Figure 4.

As a result, the PROM powers up together with the LCA, since $\overline{LDC}$ goes Low immediately after power-up; the PROM then stays powered-up until the end of the configuration process. When the user outputs go active, $\overline{LDC}$ must go 3-state and thus cut off the PROM supply current. $\overline{LDC}$ must, therefore, be configurated as an input with pull-up resistor, not as an active High output.

The PROM operating current (typically <5 mA) causes a voltage drop of typically 100 mV on the $\overline{LDC}$ output, reducing the PROM supply voltage by that amount. This violates the specification, but is guaranteed to work, since all PROMs are factory-tested at 4.5 V V_{CC}. Multiple PROMs increase the $\overline{LDC}$ sink current by only 0.5 mA per additional PROM.

$\overline{LDC}$ must never be active High, because there might be a few more CCLK pulses at the end of configuration, which will pull the PROM's CLK input below the level of the PROM ground pin. In user mode, it is, therefore, important to avoid driving the PROM with any active High or Low levels. That means that the $\overline{LDC}$ and DIN pins cannot be used in user mode, they must both be configurated as inputs with a pull-up resistor. The $\overline{CE}$ input must be tied to the SCP ground pin. $\overline{RESET}$ (active Low) must be connected to the LCA $\overline{RESET}$ input.

This design assumes that only one configuration bitstream is stored in one or multiple PROMs. It is inherently impossible to use this design when multiple bitstreams are stored in one PROM or one daisy chain of PROMs.

Programming the XC17000 Family Serial PROMs

The devices can be programmed on programmers supplied by Xilinx or qualified third-party vendors. The user must ensure that the appropriate programming algorithm and voltage are used. Different product types use different algorithms and voltages, and the wrong choice can permanently damage the device.

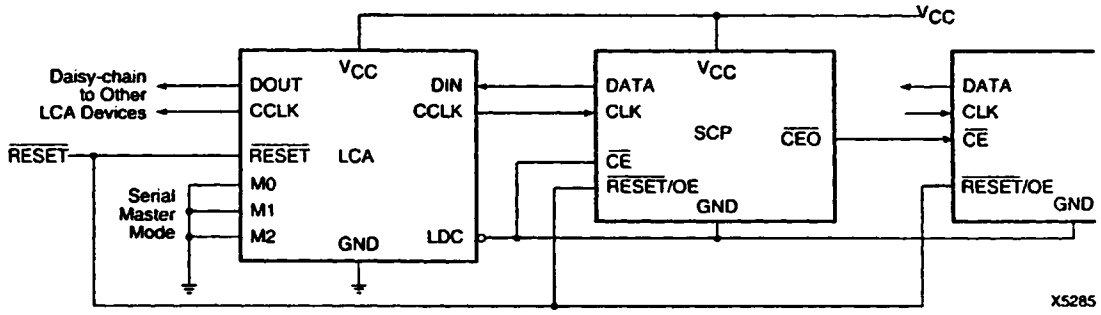


Figure 4. Zero-Standby Current Circuit

XC1718D, XC1736D, XC1765D, XC17128

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	-0.5 to +7.0	V
V_{PP}	Supply voltage relative to GND: XC1718D, XC1736D, XC1765D	-0.5 to +12.5	V
	Supply voltage relative to GND: XC17128	-0.5 to +15.5	V
V_{IN}	Input voltage relative to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	-65 to +125	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Commercial	Supply voltage relative to GND -0 °C to +70°C	4.75	5.25	V
	Industrial	Supply voltage relative to GND -40°C to +85°C	4.5	5.5	V
	Military	Supply voltage relative to GND -55°C to +125°C	4.5	5.5	V

DC Characteristics Over Operating Condition

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Commercial	3.86		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.32	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Industrial	3.76		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.37	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Military	3.7		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.4	V
I_{CCA}	Supply current, active mode			10	mA
I_{CCS}	Supply current, standby mode			0.5	mA
I_L	Input or output leakage current		-10	10	µA

Note: During normal read operation V_{PP} ***must*** be connected to V_{CC}

XC1718L and XC1765L

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	-0.5 to +6.0	V
V_{PP}	Supply voltage relative to GND	-0.5 to +12.5	V
V_{IN}	Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	-65 to +125	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

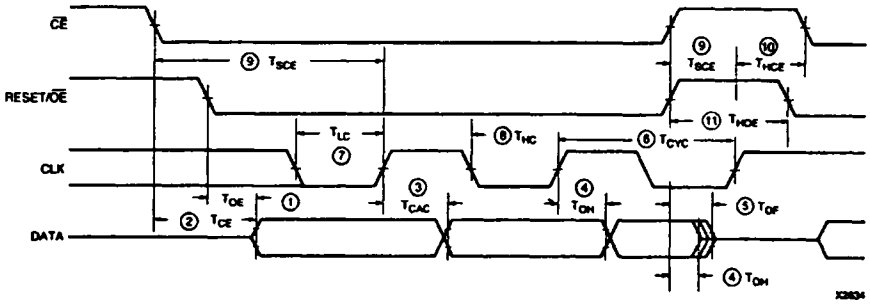
Symbol	Description		Min	Max	Units
V_{CC}	Commercial	Supply voltage relative to GND -0 °C to +70°C	3.0	3.6	V
	Industrial	Supply voltage relative to GND -40°C to +85°C	3.0	3.6	V
	Military	Supply voltage relative to GND -55°C to +125°C	3.0	3.6	V

DC Characteristics Over Operating Condition

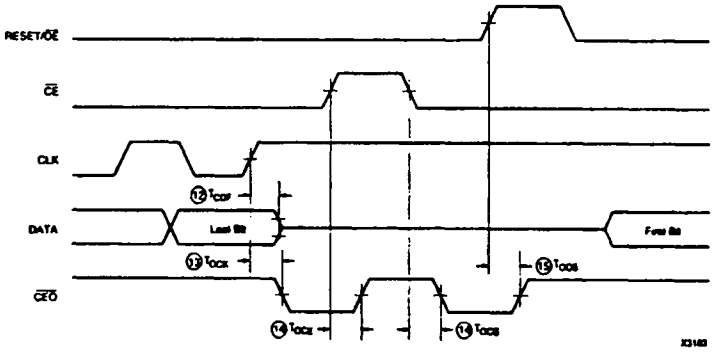
Symbol	Description	Min	Max	Units
V_{IH}	High-level input voltage	2.0	V_{CC}	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)		0.4	V
I_{CCA}	Supply current, active mode		5	mA
I_{CCS}	Supply current, standby mode		0.5	mA
I_L	Input or output leakage current	-10	10	µA

Note: During normal read operation V_{PP} *must* be connected to V_{CC}

AC Characteristics Over Operating Conditions



Symbol		Description	XC1718D, XC1736D, XC1765D		XC1718L, XC1765L		XC17128		Units
			Min	Max	Min	Max	Min	Max	
1	T_{HOE}	$\overline{OE}$ to Data Delay		45		45		50	ns
2	T_{CE}	$\overline{CE}$ to Data Delay		60		60		50	ns
3	T_{CAC}	CLK to Data Delay		150		200		60	ns
4	T_{OH}	Data Hold From $\overline{CE}$, $\overline{OE}$, or CLK	0		0		0		ns
5	T_{DF}	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay[2]		50		50		50	ns
6	T_{CYC}	Clock Periods	200		400		100		ns
7	T_{LC}	CLK Low Time[3]	100		100		25		ns
8	THC	CLK High Time[3]	100		100		25		ns
9	TSCE	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	25		40		25		ns
10	T_{HCE}	$\overline{CE}$ Hold Time to CLK (to guarantee proper counting)	0		0		0		ns
11	T_{HOE}	$\overline{OE}$ High Time (guarantees counters are reset)	100		100		20		n



Symbol		Description	XC1718D, XC1736D, XC1765D		XC1718L, XC1765L		XC17128		Units
			Min	Max	Min	Max	Min	Max	
12	T_{CDF}	CLK to Data Float Delay[2]		50		50		50	ns
13	T_{OCK}	CLK to $\overline{CEO}$ Delay		65		65		40	ns
14	T_{OCE}	CE to $\overline{CEO}$ Delay		45		45		40	ns
15	T_{OOE}	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay		40		40		45	ns

Notes: 1. AC test load = 50 pF
2. Float delays are measured with minimum tester ac load and maximum dc load.
3. Guaranteed by design, not tested.
4. All ac parameters are measured with V_{IL} = 0.0 V and V_{IH} = 3.0 V.

Ordering Information

XC17128 - PC20 C

Device Number

Operating Range/Processing
C = Commercial/Industrial (-40° to + 85°C)
M = Military (-55° to + 125°C)

Package Type
PD8 = 8-Pin Plastic DIP
DD8 = 8-Pin CerDIP
PC20 = 20-Pin Plastic Leaded Chip Carrier

Valid Ordering Combinations

XC17128PD8C
XC17128DD8M
XC17128PC20C

X3179

XC17XXX - PC20 C

Device Number
XC1718D
XC1718L
XC1736D
XC1765D
XC1765L

Operating Range/Processing
C = Commercial (0° to + 70°C)
I = Industrial (-40° to + 85°)
M = Military (-55° to + 125°C)
R = Military (-55° to + 125°C) with MIL-STD-883 Level B Equivalent Processing

Package Type
PD8 = 8-Pin Plastic DIP
DD8 = 8-Pin CerDIP
SO8 = 8-Pin Plastic Small-Outline Package
VO8 = 8-Pin Plastic Small-Outline Thin Package
PC20 = 20-Pin Plastic Leaded Chip Carrier

X3180

Valid Ordering Combinations

XC1718DPD8C	XC1736DPD8C	XC1765DPD8C	XC1718LPD8C	XC1765LPD8C
XC1718DPD8I	XC1736DPD8I	XC1765DPD8I	XC1718LSO8C	XC1765LSO8C
XC1718DSO8C	XC1736DSO8C	XC1765DSO8C	XC1718LVO8C	XC1765LVO8C
XC1718DVO8C	XC1736DVO8C	XC1765DVO8C	XC1718LPC20C	XC1765LPC20C
XC1718DSO8I	XC1736DSO8I	XC1765DSO8I		
XC1718DVO8I	XC1736DVO8I	XC1765DVO8I		
XC1718DPC20C	XC1736DPC20C	XC1765DPC20C		
XC1718DPC20I	XC1736DPC20I	XC1765DPC20I		
	XC1736DDD8M	XC1765DDD8M		
		XC1765DDD8R		

X3181

Marking Information

Due to the small size of the serial PROM package, the complete ordering part number cannot be marked on the package. The XC prefix is deleted and the package code is simplified. Device marking is as follows.

17XXX P C

Device Number
XC1718D
XC1718L
XC1736D
XC1765D
XC1765L

Operating Range/Processing
C = Commercial (0° to + 70°C)
I = Industrial (-40° to + 85°)
M = Military (-55° to + 125°C)

Package Type Code
P = 8-Pin Plastic DIP
D = 8-Pin CerDIP
S = 8-Pin Plastic Small-Outline Package
J = 20-Pin Plastic Leaded Chip Carrier

X3182

XILINX

XC4000A
Logic Cell Array Family

Product Specifications

Features

- Third Generation Field-Programmable Gate Arrays
  - Abundant flip-flops
  - Flexible function generators
  - On-chip ultra-fast RAM
  - Dedicated high-speed carry-propagation circuit
  - Wide edge decoders (two per edge)
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - Eight global low-skew clock or signal distribution network
- Flexible Array Architecture
  - Programmable logic blocks and I/O blocks
  - Programmable interconnects and wide decoders
- Sub-micron CMOS Process
  - High-speed logic and Interconnect
  - Low power consumption
- Systems-Oriented Features
  - IEEE 1149.1-compatible boundary-scan logic support
  - Programmable output slew rate (4 modes)
  - Programmable input pull-up or pull-down resistors
  - 24-mA sink current per output (48 per pair)
- Configured by Loading Binary File
  - Unlimited reprogrammability
  - Six programming modes
- XACT Development System runs on '386/'486-type PC, NEC PC, Apollo, Sun-4, and Hewlett-Packard 700 Series
  - Interfaces to popular design environments like Viewlogic, Mentor Graphics and OrCAD
  - Fully automatic partitioning, placement and routing
  - Interactive design editor for design optimization
  - 288 macros, 34 hard macros, RAM/ROM compiler

Description

The XC4000A family of FPGAs offers four devices at the low end of the XC4000 family complexity range. XC4000A differs from XC4000 in four areas: fewer routing resources, fewer wide-edge decoders, higher output sink current, and improved output slew-rate control.

- The XC4000 routing structure is optimized for smaller designs, naturally requiring fewer routing resources. The XC4000A devices have four Longlines and four single-length lines per row and column, while the XC4000 devices have six Longlines and eight single-length lines per row and column. This results in a smaller chip area and lower cost per device.
- XC4000A has two wide-edge decoders on every device edge, while the XC4000 has four. All other wide-decoder features are identical in XC4000 and XC4000A.
- XC4000A outputs are specified at 24 mA, sink current, while XC4000 outputs are specified at 12 mA. The source current is the same 4 mA for both families.
- The XC4000A family offers a more sophisticated output slew-rate control structure with four configurable options for each individual output driver: fast, medium fast, medium slow, and slow. Slew-rate control can alleviate ground-bounce problems when multiple outputs switch simultaneously, and it can reduce or eliminate crosstalk and transmission-line effects on printed circuit boards.

Note that the XC4003 and XC4005 devices are available in both flavors, the lower-priced XC4003A/XC4005A with reduced routing, and the higher-priced XC4003/XC4005 with more abundant routing resources. The XC4000A devices are intended for less demanding and more structured designs, and the XC4000 devices for more random designs requiring additional routing resources.

The equivalent devices are pin-compatible and are available in identical packages, but they are not bitstream compatible. In order to move from a XC4000A to a XC4000, or vice versa, the design must be recompiled.

Table 1. The XC4000A Family of Field-Programmable Gate Arrays

Device	XC4002A	XC4003A	XC4004A	XC4005A
Appr. Gate Count	2,000	3,000	4,000	5,000
CLB Matrix	8 x 8	10 x 10	12 x 12	14 x 14
Number of CLBs	64	100	144	196
Number of Flip-Flops	256	360	480	616
Max Decode Inputs (per side)	24	30	36	42
Max RAM Bits	2,048	3,200	4,608	6,272
Number of IOBs	64	80	96	112

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to 7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to 7	V
V_{TS}	Voltage applied to 3-state output	–0.5 to 7	V
T_{STG}	Storage temperature (ambient)	–65 to + 150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+ 260	°C
T_J	Junction temperature	+ 150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description			Min	Max	Units
V_{CC}	Supply voltage relative to GND	Commercial	0°C to 70°C	4.75	5.25	V
	Supply voltage relative to GND	Industrial	–40°C to 85°C	4.5	5.5	V
	Supply voltage relative to GND	Military	–55°C to 125°C	4.5	5.5	V
V_{IH}	High-level input voltage (XC4000 has TTL-like input thresholds)			2.0	V_{CC}	V
V_{IL}	Low-level input voltage (XC4000 has TTL-like input thresholds)			0	0.8	V
T_{IN}	Input signal transition time				250	ns

DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = –4.0 mA, V_{CC} min	2.4		V
V_{OL}	Low-level output voltage @ I_{OL} = 24 mA, V_{CC} max (Note 1)		0.4	V
I_{CCO}	Quiescent LCA supply current (Note 2)		10	mA
I_{IL}	Leakage current	–10	+10	µA
C_{IN}	Input capacitance (sample tested)		15	pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)	0.02	0.25	mA
I_{RLL}	Horizontal Long Line pull-up (when selected) @ logic Low	0.2	2.5	mA

Note: 1. With 50% of the outputs simultaneously sinking 24 mA.
2. With no output current loads, no active input or longline pull-up resistors, all package pins at V_{CC} or GND, and the LCA configured with a MakeBits tie option.

Wide Decoder Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, there derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

	Speed Grade		-6	-5	-4	
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Units**
Full length, both pull-ups, inputs from IOB I-pins	T_{WAF}	XC4002A	8.5	7.5	4.5	ns
		XC4003A	9.0	8.0	5.0	ns
		XC4004A	9.5	8.5	5.5	ns
		XC4005A	10.0	9.0	6.0	ns
Full length, both pull-ups inputs from internal logic	T_{WAFL}	XC4002A	11.5	10.5	6.5	ns
		XC4003A	12.0	11.0	7.0	ns
		XC4004A	12.5	11.5	7.5	ns
		XC4005A	13.0	12.0	8.0	ns
Half length, one pull-up inputs from IOB I-pins	T_{WAO}	XC4002A	8.5	7.5	5.5	ns
		XC4003A	9.0	8.0	6.0	ns
		XC4004A	9.5	8.5	6.5	ns
		XC4005A	10.0	9.0	7.0	ns
Half length, one pull-up inputs from internal logic	T_{WAOL}	XC4002A	11.5	10.5	7.5	ns
		XC4003A	12.0	11.0	8.0	ns
		XC4004A	12.5	11.5	8.5	ns
		XC4005A	13.0	12.0	9.0	ns

Note: These delays are specified from the decoder input to the decoder output. For pin-to-pin delays, add the input delay (T_{PID}) and output delay (one of 4 modes), as listed on page 2-70.

Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

	Speed Grade		-6	-5	-4	
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Units**
Global Signal Distribution						
From pad through **primary** buffer, to any clock k	T_{PG}	XC4002A	7.7	5.7	4.9	ns
		XC4003A	7.8	5.8	5.1	ns
		XC4004A	7.9	5.9	5.3	ns
		XC4005A	8.0	6.0	5.5	ns
From pad through **secondary** buffer, to any clock k	T_{SG}	XC4002A	8.7	6.7	6.1	ns
		XC4003A	8.8	6.8	6.3	ns
		XC4004A	8.9	6.9	6.5	ns
		XC4005A	9.0	7.0	6.7	ns

Horizontal Longline Switching Characteristic Guidelines

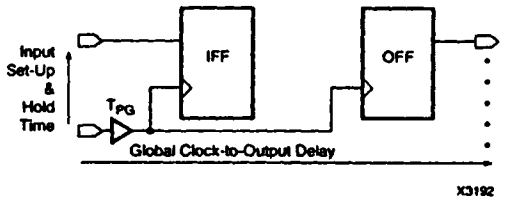
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

		Speed Grade	-6	-5	-4	
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Units**
TBUF driving a Horizontal Longline (L.L.) I going High or Low to L.L. going High or Low, while T is Low, i.e. buffer is constantly active	T_{IO1}	XC4002A	8.2	6.0	4.0	ns
		XC4003A	8.8	6.2	4.4	ns
		XC4004A	9.4	6.6	5.0	ns
		XC4005A	10.0	7.0	5.5	ns
I going Low to L.L. going from resistive pull-up High to active Low, (TBUF configured as open drain)	T_{IO2}	XC4002A	8.7	6.5	4.5	ns
		XC4003A	9.3	6.7	5.0	ns
		XC4004A	9.9	7.1	5.5	ns
		XC4005A	10.5	7.5	6.0	ns
T going Low to L.L. going from resistive pull-up or floating High to active Low, (TUBF configured as open drain)	T_{ON}	XC4002A	10.1	8.4	6.8	ns
		XC4003A	10.7	9.0	7.2	ns
		XC4004A	11.4	9.5	7.6	ns
		XC4005A	12.0	10.0	8.0	ns
T going High to TBUF going inactive, not driving L.L.	T_{OFF}	All devices	3.0	2.0	1.8	ns
T going High to L.L. going from Low to High, pulled up by a single resistor	T_{PUS}	XC4002A	23.0	19.0	13.0	ns
		XC4003A	24.0	20.0	14.0	ns
		XC4004A	25.0	21.0	15.0	ns
		XC4005A	26.0	22.0	16.0	ns
T going High to L.L. going from Low to High, pulled up by two resistors	T_{PUF}	XC4002A	10.5	8.5	6.5	ns
		XC4003A	11.0	9.0	7.0	ns
		XC4004A	11.5	9.5	7.5	ns
		XC4005A	12.0	10.0	8.0	ns

Guaranteed Input and Output Parameters (Pin-to-Pin)

All values listed below are tested directly, and guaranteed over the operating conditions. The same parameters can also be derived indirectly from the IOB and Global Buffer specifications. The XACT delay calculator uses this indirect method. When there is a discrepancy between these two methods, the directly tested values listed below should be used, and the derived values should be ignored.

		Speed Grade	-6	-5	-4	
Description	**Symbol**	**Device**				**Units**
Global Clock to Output (fast)	T_{ICKOF}	XC4002A	14.9	12.2	11.4	ns
		XC4003A	15.1	12.5	11.6	ns
	(Max)	XC4004A	15.3	12.8	11.8	ns
		XC4005A	15.5	13.0	12.0	ns
Global Clock to Output (slew limited)	T_{ICKO}	XC4002A	19.9	15.2	14.4	ns
		XC4003A	20.1	15.5	14.6	ns
	(Max)	XC4004A	20.3	15.8	14.8	ns
		XC4005A	20.5	16.0	15.0	ns
Input Set-up Time, using IFF (fast)	T_{PSUF}	XC4002A	2.6	2.3	1.8	ns
		XC4003A	2.4	2.0	1.6	ns
	(Min)	XC4004A	2.2	1.7	1.4	ns
		XC4005A	2.0	1.5	1.2	ns
Input Hold time, using IFF (fast)	T_{PHF}	XC4002A	4.9	3.7	3.7	ns
		XC4003A	5.1	4.0	4.0	ns
	(Min)	XC4004A	5.3	4.3	4.3	ns
		XC4005A	5.5	4.5	4.5	ns
Input Set-up Time, using IFF (with delay)	T_{PSU}	XC4002A	21.8	18.8	12.0	ns
		XC4003A	21.5	18.5	12.0	ns
	(Min)	XC4004A	21.2	18.2	12.0	ns
		XC4005A	21.0	18.0	12.0	ns
Input Hold Time, using IFF (with delay)	T_{PH}	XC4002A	0	0	0	ns
		XC4003A	0	0	0	ns
	(Min)	XC4004A	0	0	0	ns
		XC4005A	0	0	0	ns



Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). When testing fast outputs, only one output switches. When testing slew-rate limited outputs, half the number of outputs on one side of the device are switching. These parameter values are tested and guaranteed for worst-case conditions of supply voltage and temperature, and also with the most unfavorable clock polarity choice.

T_{PDLI} for -4 Speed Grade

Pad to I1, I2 via transparent latch, with delay	XC4002A	17.4 ns
	XC4003A	17.6 ns
	XC4004A	17.8 ns
	XC4005A	17.9 ns

T_{PICKD} for -4 Speed Grade

Input set-up time pad to clock (IK) with delay	XC4002A	15.4 ns
	XC4003A	15.6 ns
	XC4004A	15.8 ns
	XC4005A	15.9 ns

X5283

IOB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

		-6		-5		-4		
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
INPUT								
Propagation Delays								
Pad to I1, I2	T_{PID}		4.0		3.0		2.8	ns
Pad to I1, I2, via transparent latch (fast)	T_{PLI}		8.0		7.0		6.0	ns
Pad to I1, I2, via transparent latch (with delay)	T_{PDLI}		26.0		24.0		**	ns
Clock (IK) to I1, I2, (flip-flop)	T_{IKRI}		8.0		7.0		6.0	ns
Clock (IK) to I1, I2 (latch enable, active Low)	T_{IKLI}		8.0		7.0		6.0	ns
Set-up Time (Note 3)								
Pad to Clock (IK), fast	T_{PICK}	7.0		6.0		4.0		ns
Pad to Clock (IK) with delay	T_{PICKD}	25.0		24.0		**		ns
Hold Time (Note 3)								
Pad to Clock (IK), fast	T_{IKPI}	1.0		1.0		1.0		ns
Pad to Clock (IK) with delay	T_{IKPID}	neg		neg		neg		ns
OUTPUT								
Propagation Delays								
Clock (OK) to Pad (fast)	T_{OKPOF}		7.5		7.0		6.5	ns
Output (O) to Pad (fast)	T_{OPF}		9.0		7.0		5.5	ns
3-state to Pad begin hi-Z (slew-rate independent)	T_{TSHZ}		9.0		7.0		6.5	ns
3-state to Pad active and valid (fast)	T_{TSONF}		13.0		10.0		9.5	ns
Additional Delay								
For medium fast outputs			2.0		1.5		1.0	ns
For medium slow outputs			4.0		3.0		2.0	ns
For slow outputs			6.0		4.5		3.0	ns
Set-up and Hold Times								
Output (O) to clock (OK) set-up time	T_{OOK}	8.0		6.0		5.5		ns
Output (O) to clock (OK) hold time	T_{OKO}	0.0		0.0		0		ns
Clock								
Clock High or Low time	T_{CH}/T_{CL}	5.0		4.0		4.0		ns
Global Set/Reset								
Delay from GSR net through Q to I1, I2	T_{RRI}		14.5		13.5		13.5	ns
Delay from GSR net to Pad	T_{RPO}		18.0		17.0		14.6	ns
GSR width*	T_{MRW}	21.0		18.0		18.0		ns

* Timing is based on the XC4005. For other devices see XACT timing calculator.
** See preceding page.

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture).

2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up or pull-down resistor or alternatively configured as a driven output or be driven from an external source.

3. Input pad setup times and hold times are specified with respect to the internal clock (IK). To calculate system setup time, subtract clock delay (clock pad to IK) from the specified input pad setup time value, but do not subtract below zero. Negative hold time means that the delay in the input data is adequate for the **external system hold time** to be zero, provided the input clock uses the Global signal distribution from pad to IK.

CLB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

	Speed Grade	-6		-5		-4		
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Combinatorial Delays								
F/G inputs to X/Y outputs	T_{ILO}		6.0		4.5		4.0	ns
F/G inputs via H' to X/Y outputs	T_{IHO}		8.0		7.0		6.0	ns
C inputs via H' to X/Y outputs	T_{HHO}		7.0		5.0		4.5	ns
CLB Fast Carry Logic								
Operand inputs (F1,F2,G1,G4) to C_{OUT}	T_{OPCY}		7.0		5.5		5.0	ns
Add/Subtract input (F3) to C_{OUT}	T_{ASCY}		8.0		6.0		5.5	ns
Initialization inputs (F1,F3) to C_{OUT}	T_{INCY}		6.0		4.0		3.5	ns
C_{IN} through function generators to X/Y outputs	T_{SUM}		8.0		6.0		5.5	ns
C_{IN} to C_{OUT}, bypass function generators.	T_{BYP}		2.0		1.5		1.5	ns
Sequential Delays								
Clock K to outputs Q	T_{CKO}		5.0		3.0		3.0	ns
Set-up Time before Clock K								
F/G inputs	T_{ICK}	6.0		4.5		4.5		ns
F/G inputs via H'	T_{IHCK}	8.0		6.0		6.0		ns
C inputs via H1	T_{HHCK}	7.0		5.0		5.0		ns
C inputs via DIN	T_{DICK}	4.0		3.0		3.0		ns
C inputs via EC	T_{ECCK}	7.0		4.0		3.0		ns
C inputs via S/R, going Low (inactive)	T_{RCK}	6.0		4.5		4.0		ns
C_{IN} input via F'/G'		8.0		6.0		5.5		ns
C_{IN} input via F'/G' and H'		10.0		7.5		7.3		ns
Hold Time after Clock K								
F/G inputs	T_{CKI}	0		0		0		ns
F/G inputs via H'	T_{CKIH}	0		0		0		ns
C inputs via H1	T_{CKHH}	0		0		0		ns
C inputs via DIN	T_{CKDI}	0		0		0		ns
C inputs via EC	T_{CKEC}	0		0		0		ns
C inputs via S/R, going Low (inactive)	T_{CKR}	0		0		0		ns
Clock								
Clock High time	T_{CH}	5.0		4.0		4.0		ns
Clock Low time	T_{CL}	5.0		4.0		4.0		ns
Set/Reset Direct								
Width (High)	T_{RPW}	5.0		4.0		4.0		ns
Delay from C inputs via S/R, going High to Q	T_{RIO}		9.0		8.0		7.0	ns
Master Set/Reset*								
Width (High or Low)	T_{MRW}	21.0		18.0		18.0		ns
Delay from Global Set/Reset net to Q	T_{MRQ}		33.0		31.0		28.0	ns

* Timing is based on the XC4005. For other devices see XACT timing calculator.

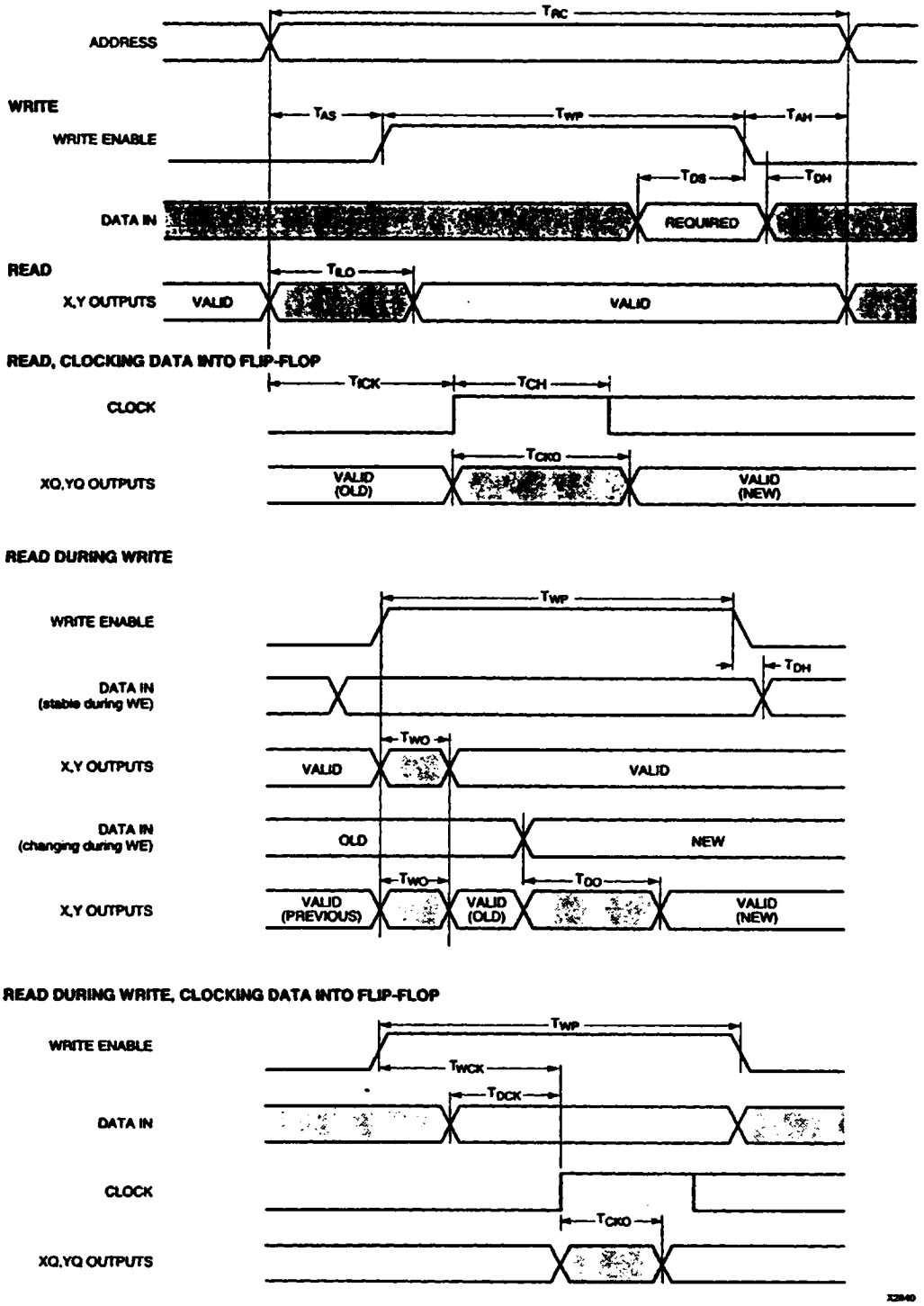
CLB Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

CLB RAM OPTION	Speed Grade		-6		-5		-4		
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Write Operation									
Address write cycle time	16 x 2	T_{WC}	9.0		8.0		8.0		ns
	32 x 1	T_{WCT}	9.0		8.0		8.0		ns
Write Enable pulse width (High)	16 x 2	T_{WP}	5.0		4.0		4.0		ns
	32 x 1	T_{WPT}	5.0		4.0		4.0		ns
Address set-up time before beginning of WE	16 x 2	T_{AS}	2.0		2.0		2.0		ns
	32 x 1	T_{AST}	2.0		2.0		2.0		ns
Address hold time after end of WE	16 x 2	T_{AH}	2.0		2.0		2.0		ns
	32 x 1	T_{AHT}	2.0		2.0		2.0		ns
DIN set-up time before end of WE	16 x 2	T_{DS}	4.0		4.0		4.0		ns
	32 x 1	T_{DST}	5.0		5.0		5.0		ns
DIN hold time after end of WE	both	T_{DHT}	2.0		2.0		2.0		ns
Read Operation									
Address read cycle time	16 x 2	T_{RC}	7.0		5.5		5.0		ns
	32 x 1	T_{RCT}	10.0		7.5		7.0		ns
Data valid after address change	16 x 2	T_{ILO}		6.0		4.5		4.0	ns
(no Write Enable)	32 x 1	T_{IHO}		8.0		7.0		6.0	ns
Read Operation, Clocking Data into Flip-Flop									
Address setup time before clock K	16 x 2	T_{ICK}	6.0		4.5		4.5		ns
	32 x 1	T_{IHCK}	8.0		6.0		6.0		ns
Read During Write									
Data valid after WE going active	16 x 2	T_{WO}		12.0		10.0		9.0	ns
(DIN stable before WE)	32 x 1	T_{WOT}		15.0		12.0		11.0	ns
Data valid after DIN	16 x 2	T_{DO}		11.0		9.0		8.5	ns
(DIN change during WE)	32 x 1	T_{DOT}		14.0		11.0		11.0	ns
Read During Write, Clocking Data into Flip-Flop									
WE setup time before clock K	16 x 2	T_{WCK}	12.0		10.0		9.5		ns
	32 x 1	T_{WCKT}	15.0		12.0		11.5		ns
Data setup time before clock K	16 x 2	T_{DCK}	11.0		9.0		9.0		ns
	32 x 1	T_{DCKT}	14.0		11.0		11.0		ns

Note: Timing for the 16 x 1 RAM option is identical to 16 x 2 RAM timing

CLB RAM Timing Characteristics



XC4002A Pinouts

Pin Description	PC 84	PQ100	VQ100	PG120	Bound Scan
VCC	2	92	89	G3	-
I/O (A8)	3	93	90	G1	26
I/O (A9)	4	94	91	F1	29
-	-	95*	92*	E1*	-
-	-	96*	93*	F2*	-
I/O (A10)	5	97	94	F3	32
I/O (A11)	6	98	95	D1	35
-	-	-	-	E2*	-
I/O (A12)	7	99	96	C1	38
I/O (A13)	8	100	97	D2	41
-	-	-	-	E3*	-
-	-	-	-	B1*	-
I/O (A14)	9	1	98	C2	44
SGCK1 (A15, I/O)	10	2	99	D3	47
VCC	11	3	100	C3	-
GND	12	4	1	C4	-
PGCK1 (A16, I/O)	13	5	2	B2	50
I/O (A17)	14	6	3	B3	53
-	-	-	-	A1*	-
-	-	-	-	A2*	-
I/O (TDI)	15	7	4	C5	56
I/O (TCK)	16	8	5	B4	59
-	-	-	-	A3*	-
I/O (TMS)	17	9	6	B5	62
I/O	18	10	7	A4	65
-	-	-	-	C6*	-
-	-	11*	8*	A5*	-
I/O	19	12	9	B6	68
I/O	20	13	10	A6	71
GND	21	14	11	B7	-
VCC	22	15	12	C7	-
I/O	23	16	13	A7	74
I/O	24	17	14	A8	77
-	-	18*	15*	A9*	-
-	-	-	-	B8*	-
I/O	25	19	16	C8	80
I/O	26	20	17	A10	83
I/O	27	21	18	B9	86
I/O	-	22	19	A11	89
-	-	-	-	B10*	-

Pin Description	PC 84	PQ100	VQ100	PG120	Bound Scan
I/O	28	23	20	C9	92
SGCK2 (I/O)	29	24	21	A12	95
O (M1)	30	25	22	B11	98
GND	31	26	23	C10	-
I (M0)	32	27	24	C11	101†
VCC	33	28	25	D11	-
I (M2)	34	29	26	B12	102†
PGCK2 (I/O)	35	30	27	C12	103
I/O (HDC)	36	31	28	A13	106
-	-	-	-	B13*	-
-	-	-	-	E11*	-
I/O	-	32	29	D12	109
I/O (LDC)	37	33	30	C13	112
I/O	38	34	31	E12	115
I/O	39	35	32	D13	118
-	-	36*	33*	F11*	-
-	-	37*	34*	E13*	-
I/O	40	38	35	F12	121
I/O (ERR, INIT)	41	39	36	F13	124
VCC	42	40	37	G12	-
GND	43	41	38	G11	-
I/O	44	42	39	G13	127
I/O	45	43	40	H13	130
-	-	44*	41*	J13*	-
-	-	45*	42*	H12*	-
I/O	46	46	43	H11	133
I/O	47	47	44	K13	136
I/O	48	48	45	J12	139
I/O	49	49	46	L13	142
-	-	-	-	K12*	-
-	-	-	-	J11*	-
I/O	50	50	47	M13	145
SGCK3 (I/O)	51	51	48	L12	148
GND	52	52	49	K11	-
DONE	53	53	50	L11	-
VCC	54	54	51	L10	-
PROG	55	55	52	M12	-
I/O (D7)	56	56	53	M11	151
PGCK3 (I/O)	57	57	54	N13	154
-	-	-	-	N12*	-

Pin Description	PC 84	PQ100	VQ100	PG120	Bound Scan
-	-	-	-	L9	-
I/O (D6)	58	58	55	M10	157
I/O	-	59	56	N11	160
I/O (D5)	59	60	57	M9	163
I/O (CS0)	60	61	58	N10	166
-	-	62*	59*	L8*	-
-	-	63*	60*	N9*	-
I/O (D4)	61	64	61	M8	169
I/O	62	65	62	N8	172
VCC	63	66	63	M7	-
GND	64	67	64	L7	-
I/O (D3)	65	68	65	N7	175
I/O (RS)	66	69	66	N6	178
-	-	70*	67*	N5*	-
-	-	-	-	M6*	-
I/O (D2)	67	71	68	L6	181
I/O	68	72	69	N4	184
I/O (D1)	69	73	70	M5	187
I/O (RCLK-BUSY/RDY)	70	74	71	N3	190
-	-	-	-	M4*	-
-	-	-	-	L5*	-
I/O (D0, DIN)	71	75	72	N2	193
SGCK4 (DOUT, I/O)	72	76	73	M3	196
CCLK	73	77	74	L4	-
VCC	74	78	75	L3	-
O (TDO)	75	79	76	M2	-
GND	76	80	77	K3	-
I/O (A0, WS)	77	81	78	L2	2
PGCK4 (I/O,A1)	78	82	79	N1	5
-	-	-	-	M1*	-
-	-	-	-	J3*	-
I/O (CS1, A2)	79	83	80	K2	8
I/O (A3)	80	84	81	L1	11
I/O (A4)	81	85	82	J2	14
I/O (A5)	82	86	83	K1	17
-	-	87*	84*	H3*	-
-	-	88*	85*	J1*	-
I/O (A6)	83	89	86	H2	20
I/O (A7)	84	90	87	H1	23
GND	1	91	88	G2	-

* Indicates unconnected package pins.
† Contributes only one bit (.I) to the boundary scan register.
Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 199 = BSCANT.UPD

XC4003A Pinouts

Pin Description	PC84	VQ100	PQ100	PG120	Bound Scan
VCC	2	89	92	G3	-
I/O (A8)	3	90	93	G1	32
I/O (A9)	4	91	94	F1	35
I/O	-	92	95	E1	38
I/O	-	93	96	F2	41
I/O (A10)	5	94	97	F3	44
I/O (A11)	6	95	98	D1	47
-	-	-	-	E2*	-
I/O (A12)	7	96	99	C1	50
I/O (A13)	8	97	100	D2	53
-	-	-	-	E3*	-
-	-	-	-	B1*	-
I/O (A14)	9	98	1	C2	56
SGCK1 (A15,I/O)	10	99	2	D3	59
VCC	11	100	3	C3	-
GND	12	1	4	C4	-
PGCK1 (A16, I/O)	13	2	5	B2	62
I/O (A17)	14	3	6	B3	65
-	-	-	-	A1*	-
-	-	-	-	A2*	-
I/O (TDI)	15	4	7	C5	68
I/O (TCK)	16	5	8	B4	71
-	-	-	-	A3*	-
I/O (TMS)	17	6	9	B5	74
I/O	18	7	10	A4	77
I/O	-	-	-	C6	80
I/O	-	8	11	A5	83
I/O	19	9	12	B6	86
I/O	20	10	13	A6	89
GND	21	11	14	B7	-
VCC	22	12	15	C7	-
I/O	23	13	16	A7	92
I/O	24	14	17	A8	95
I/O	-	15	18	A9	98
I/O	-	-	-	B8	101
I/O	25	16	19	C8	104
I/O	26	17	20	A10	107
I/O	27	18	21	B9	110
I/O	-	19	22	A11	113
-	-	-	-	B10*	-
I/O	28	20	23	C9	116
SGCK2 (I/O)	29	21	24	A12	119
O (M1)	30	22	25	B11	122
GND	31	23	26	C10	-
I (M0)	32	24	27	C11	125†
VCC	33	25	28	D11	-
I (M2)	34	26	29	B12	126†
PGCK2 (I/O)	35	27	30	C12	127
I/O (HDC)	36	28	31	A13	130
-	-	-	-	B13*	-
-	-	-	-	E11*	-
I/O	-	29	32	D12	133
I/O (LDC)	37	30	33	C13	136
I/O	38	31	34	E12	139
I/O	39	32	35	D13	142
I/O	-	33	36	F11	145
I/O	-	34	37	E13	148
I/O	40	35	38	F12	151
I/O (ERR, INIT)	41	36	39	F13	154
VCC	42	37	40	G12	-

Pin Description	PC84	VQ100	PQ100	PG120	Bound Scan
GND	43	38	41	G11	-
I/O	44	39	42	G13	157
I/O	45	40	43	H13	160
I/O	-	41	44	J13	163
I/O	-	42	45	H12	166
I/O	46	43	46	H11	169
I/O	47	44	47	K13	172
I/O	48	45	48	J12	175
I/O	49	46	49	L13	178
-	-	-	-	K12*	-
-	-	-	-	J11*	-
I/O	50	47	50	M13	181
SGCK3 (I/O)	51	48	51	L12	184
GND	52	49	52	K11	-
DONE	53	50	53	L11	-
VCC	54	51	54	L10	-
PROG	55	52	55	M12	-
I/O (D7)	56	53	56	M11	187
PGCK3 (I/O)	57	54	57	N13	190
-	-	-	-	N12*	-
-	-	-	-	L9*	-
I/O (D6)	58	55	58	M10	193
I/O	-	56	59	N11	196
I/O (D5)	59	57	60	M9	199
I/O ($\overline{CS0}$)	60	58	61	N10	202
I/O	-	59	62	L8	205
I/O	-	60	63	N9	208
I/O (D4)	61	61	64	M8	211
I/O	62	62	65	N8	214
VCC	63	63	66	M7	-
GND	64	64	67	L7	-
I/O (D3)	65	65	68	N7	217
I/O (RS)	66	66	69	N6	220
I/O	-	67	70	N5	223
I/O	-	-	-	M6	226
I/O (D2)	67	68	71	L6	229
I/O	68	69	72	N4	232
I/O (D1)	69	70	73	M5	235
I/O (RCLK-BUSY/RDY)	70	71	74	N3	238
-	-	-	-	M4*	-
-	-	-	-	L5*	-
I/O (D0, DIN)	71	72	75	N2	241
SGCK4 (DOUT, I/O)	72	73	76	M3	244
CCLK	73	74	77	L4	-
VCC	74	75	78	L3	-
O (TDO)	75	76	79	M2	-
GND	76	77	80	K3	-
I/O (A0, WS)	77	78	81	L2	2
PGCK4 (A1, I/O)	78	79	82	N1	5
-	-	-	-	M1*	-
-	-	-	-	J3*	-
I/O (CS1, A2)	79	80	83	K2	8
I/O (A3)	80	81	84	L1	11
I/O (A4)	81	82	85	J2	14
I/O (A5)	82	83	86	K1	17
I/O	-	84	87	H3	20
I/O	-	85	88	J1	23
I/O (A6)	83	86	89	H2	26
I/O (A7)	84	87	90	H1	29
GND	1	88	91	G2	-

* Indicates unconnected package pins.
† Contributes only one bit (.i) to the boundary scan register.
Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 247 = BSCANT.UPD

XC4004A Pinouts

Pin Description	PC84	TQ144	PQ160	PG120	Bound Scan
VCC	2	128	142	G3	-
I/O (A8)	3	129	143	G1	38
I/O (A9)	4	130	144	F1	41
I/O	-	131	145	E1	44
I/O	-	132	146	F2	47
I/O (A10)	5	133	147	F3	50
I/O (A11)	6	134	148	D1	53
-	-	135*	149*	-	-
-	-	136*	150*	-	-
GND	-	137	151	E2	-
-	-	-	152*	-	-
-	-	-	153*	-	-
I/O (A12)	7	138	154	C1	56
I/O (A13)	8	139	155	D2	59
I/O	-	140	156	E3	62
I/O	-	141	157	B1	65
I/O (A14)	9	142	158	C2	68
SGCK1 (A15, I/O)	10	143	159	D3	71
VCC	11	144	160	C3	-
GND	12	1	1	C4	-
PGCK1 (A16, I/O)	13	2	2	B2	74
I/O (A17)	14	3	3	B3	77
I/O	-	4	4	A1	80
I/O	-	5	5	A2	83
I/O (TDI)	15	6	6	C5	86
I/O (TCK)	16	7	7	B4	89
-	-	-	8*	-	-
-	-	-	9*	-	-
GND	-	8	10	A3	-
-	-	9*	11*	-	-
-	-	10*	12*	-	-
I/O (TMS)	17	11	13	B5	92
I/O	18	12	14	A4	95
I/O	-	13	15	C6	98
I/O	-	14	16	A5	101
I/O	19	15	17	B6	104
I/O	20	16	18	A6	107
GND	21	17	19	B7	-
VCC	22	18	20	C7	-
I/O	23	19	21	A7	110
I/O	24	20	22	A8	113
I/O	-	21	23	A9	116
I/O	-	22	24	B8	119
I/O	25	23	25	C8	122
I/O	26	24	26	A10	125
-	-	25*	27*	-	-
-	-	26*	28*	-	-
GND	-	27	29	-	-
-	-	-	30*	-	-
-	-	-	31*	-	-
I/O	27	28	32	B9	128
I/O	-	29	33	A11	131
I/O	-	30	34	B10	134
I/O	-	31	35	-	137

Pin Description	PC84	TQ144	PQ160	PG120	Bound Scan
I/O	28	32	36	C9	140
SGCK2 (I/O)	29	33	37	A12	143
O (M1)	30	34	38	B11	146
GND	31	35	39	C10	-
I (M0)	32	36	40	C11	149†
VCC	33	37	41	D11	-
I (M2)	34	38	42	B12	150†
PGCK2 (I/O)	35	39	43	C12	151
I/O (HDC)	36	40	44	A13	154
I/O	-	41	45	B13	157
I/O	-	42	46	E11	160
I/O	-	43	47	D12	163
I/O (LDC)	37	44	48	C13	166
-	-	-	49*	-	-
-	-	-	50*	-	-
GND	-	45	51	-	-
-	-	46*	52*	-	-
-	-	47*	53*	-	-
I/O	38	48	54	E12	169
I/O	39	49	55	D13	172
I/O	-	50	56	F11	175
I/O	-	51	57	E13	178
I/O	40	52	58	F12	181
I/O (ERR, INIT)	41	53	59	F13	184
VCC	42	54	60	G12	-
GND	43	55	61	G11	-
I/O	44	56	62	G13	187
I/O	45	57	63	H13	190
I/O	-	58	64	J13	193
I/O	-	59	65	H12	196
I/O	46	60	66	H11	199
I/O	47	61	67	K13	202
-	-	62*	68*	-	-
-	-	63*	69*	-	-
GND	-	64	70	-	-
-	-	-	71*	-	-
-	-	-	72*	-	-
I/O	48	65	73	J12	205
I/O	49	66	74	L13	201
I/O	-	67	75	K12	211
I/O	-	68	76	J11	214
I/O	50	69	77	M13	217
SGCK3 (I/O)	51	70	78	L12	220
GND	52	71	79	K11	-
DONE	53	72	80	L11	-
VCC	54	73	81	L10	-
PROG	55	74	82	M12	-
I/O (D7)	56	75	83	M11	223
PGCK3 (I/O)	57	76	84	N13	226
I/O	-	77	85	N12	229
I/O	-	78	86	L9	232
I/O (D6)	58	79	87	M10	235
I/O	-	80	88	N11	238
-	-	-	89*	-	-

Pin Description	PC84	TQ144	PQ160	PG120	Bound Scan
-	-	-	90*	-	-
GND	-	81	91	-	-
-	-	82*	92*	-	-
-	-	83*	93*	-	-
I/O (D5)	59	84	94	M9	241
I/O (CS0)	60	85	95	N10	244
I/O	-	86	96	L8	247
I/O	-	87	97	N9	250
I/O (D4)	61	88	98	M8	253
I/O	62	89	99	N8	256
VCC	63	90	100	M7	-
GND	64	91	101	L7	-
I/O (D3)	65	92	102	N7	259
I/O (RS)	66	93	103	N6	262
I/O	-	94	104	N5	265
I/O	-	95	105	M6	268
I/O (D2)	67	96	106	L6	271
I/O	68	97	107	N4	274
-	-	98*	108*	-	-
-	-	99*	109*	-	-
GND	-	100	110	-	-
-	-	-	111*	-	-
-	-	-	112*	-	-
I/O (D1)	69	101	113	M5	277
I/O (RCLK-BUSY/RDY)	70	102	114	N3	280
I/O	-	103	115	M4	283
I/O	-	104	116	L5	286
I/O (D0, DIN)	71	105	117	N2	289
SGCK4 (DOUT, I/O)	72	106	118	M3	292
CCLK	73	107	119	L4	-
VCC	74	108	120	L3	-
O (TDO)	75	109	121	M2	-
GND	76	110	122	K3	-
I/O (A0, WS)	77	111	123	L2	2
PGCK4 (I/O,A1)	78	112	124	N1	5
I/O	-	113	125	M1	8
I/O	-	114	126	J3	11
I/O (CS1, A2)	79	115	127	K2	14
I/O (A3)	80	116	128	L1	17
-	-	117*	129*	-	-
-	-	-	130*	-	-
GND	-	118	131	-	-
-	-	119*	132*	-	-
-	-	120*	133*	-	-
I/O (A4)	81	121	134	J2	20
I/O (A5)	82	122	135	K1	23
-	-	-	136*	-	-
I/O	-	123	137	H3	26
I/O	-	124	138	J1	29
I/O (A6)	83	125	139	H2	32
I/O (A7)	84	126	140	H1	35
GND	1	127	141	G2	-

* Indicates unconnected package pins.
† Contributes only one bit (.I) to the boundary scan register.
Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 295 = BSCANT.UPD

XC4005A Pinouts

Pin Description	PC84	TQ144	PQ160	PQ208	PG156	Bound Scan
VCC	2	128	142	183	H3	-
I/O (A8)	3	129	143	184	H1	44
I/O (A9)	4	130	144	185	G1	47
I/O	-	131	145	186	G2	50
I/O	-	132	146	187	G3	53
-	-	-	-	188*	-	-
-	-	-	-	189*	-	-
I/O (A10)	5	133	147	190	F1	56
I/O (A11)	6	134	148	191	F2	59
I/O	-	135	149	192	E1	62
I/O	-	136	150	193	E2	65
GND	-	137	151	194	F3	-
-	-	-	-	195*	-	-
-	-	-	-	196*	-	-
-	-	-	152*	197*	D1*	-
-	-	-	153*	198*	D2*	-
I/O (A12)	7	138	154	199	E3	68
I/O (A13)	8	139	155	200	C1	71
-	-	-	-	-	-	-
I/O	-	140	156	201	C2	74
I/O	-	141	157	202	D3	77
I/O (A14)	9	142	158	203	B1	80
SGCK1 (A15, I/O)	10	143	159	204	B2	83
VCC	11	144	160	205	C3	-
-	-	-	-	206*	-	-
-	-	-	-	207*	-	-
-	-	-	-	208*	-	-
-	-	-	-	1*	-	-
GND	12	1	1	2	C4	-
-	-	-	-	3*	-	-
PGCK1 (A18, I/O)	13	2	2	4	B3	86
I/O (A17)	14	3	3	5	A1	89
I/O	-	4	4	6	A2	92
I/O	-	5	5	7	C5	95
-	-	-	-	-	-	-
I/O (TDI)	15	6	6	8	B4	98
I/O (TCK)	16	7	7	9	A3	101
-	-	-	8*	10*	A4*	-
-	-	-	9*	11*	-	-
-	-	-	-	12*	-	-
-	-	-	-	13*	-	-
GND	-	8	10	14	C6	-
I/O	-	9	11	15	B5	104
I/O	-	10	12	16	B6	107
I/O (TMS)	17	11	13	17	A5	110
I/O	18	12	14	18	C7	113
-	-	-	-	19*	-	-
-	-	-	-	20*	-	-
I/O	-	13	15	21	B7	116
I/O	-	14	16	22	A6	119
I/O	19	15	17	23	A7	122
I/O	20	16	18	24	A8	125
GND	21	17	19	25	C8	-
VCC	22	18	20	26	B8	-
I/O	23	19	21	27	C9	128
I/O	24	20	22	28	B9	131
I/O	-	21	23	29	A9	134
I/O	-	22	24	30	B10	137
-	-	-	-	31*	-	-
-	-	-	-	32*	-	-
I/O	25	23	25	33	C10	140
I/O	26	24	26	34	A10	143
I/O	-	25	27	35	A11	146
I/O	-	26	28	36	B11	149
GND	-	27	29	37	C11	-
-	-	-	-	38*	-	-
-	-	-	-	39*	-	-
-	-	-	30*	40*	A12*	-
-	-	-	31*	41*	-	-
I/O	27	28	32	42	B12	152
I/O	-	29	33	43	A13	155
I/O	-	30	34	44	A14	158

Pin Description	PC84	TQ144	PQ160	PQ208	PG156	Bound Scan
I/O	-	31	35	45	C12	161
-	-	-	-	-	-	-
I/O	28	32	36	46	B13	164
SGCK2 (I/O)	29	33	37	47	B14	167
O (M1)	30	34	38	48	A15	170
GND	31	35	39	49	C13	-
(TM0)	32	36	40	50	A16	173†
-	-	-	-	51*	-	-
-	-	-	-	52*	-	-
-	-	-	-	53*	-	-
-	-	-	-	54*	-	-
VCC	33	37	41	55	C14	-
I (M2)	34	38	42	56	B15	174†
PGCK2 (I/O)	35	39	43	57	B16	175
I/O (HDC)	36	40	44	58	D14	178
I/O	-	41	45	59	C15	181
-	-	-	-	-	-	-
I/O	-	42	46	60	D15	184
I/O	-	43	47	61	E14	187
I/O (LDC)	37	44	48	62	C16	190
-	-	-	49*	63*	E15*	-
-	-	-	50*	64*	D16*	-
-	-	-	-	65*	-	-
-	-	-	-	66*	-	-
GND	-	45	51	67	F14	-
I/O	-	46	52	68	F15	193
I/O	-	47	53	69	E16	196
I/O	38	48	54	70	F16	199
I/O	39	49	55	71	G14	202
-	-	-	-	72*	-	-
-	-	-	-	73*	-	-
I/O	-	50	56	74	G15	205
I/O	-	51	57	75	G16	208
I/O	40	52	58	76	H16	211
I/O (ERR INIT)	41	53	59	77	H15	214
VCC	42	54	60	78	H14	-
GND	43	55	61	79	J14	-
I/O	44	56	62	80	J15	217
I/O	45	57	63	81	J16	220
I/O	-	58	64	82	K16	223
I/O	-	59	65	83	K15	226
-	-	-	-	84*	-	-
-	-	-	-	85*	-	-
I/O	46	60	66	86	K14	229
I/O	47	61	67	87	L16	232
I/O	-	62	68	88	M16	235
I/O	-	63	69	89	L15	238
GND	-	64	70	90	L14	-
-	-	-	-	91*	-	-
-	-	-	-	92*	-	-
-	-	-	71*	93*	N16*	-
-	-	-	72*	94*	M15*	-
I/O	48	65	73	95	P16	241
I/O	49	66	74	96	M14	244
I/O	-	67	75	97	N15	247
I/O	-	68	76	98	P15	250
I/O	50	69	77	99	N14	253
SGCK3 (I/O)	51	70	78	100	R16	256
GND	52	71	79	101	P14	-
-	-	-	-	102*	-	-
DONE	53	72	80	103	R15	-
-	-	-	-	104*	-	-
-	-	-	-	105*	-	-
VCC	54	73	81	106	P13	-
-	-	-	-	107*	-	-
PROG	55	74	82	108	R14	-
I/O (D7)	56	75	83	109	T16	259
PGCK3 (I/O)	57	76	84	110	T15	262
I/O	-	77	85	111	R13	265
-	-	-	-	-	-	-
I/O	-	78	86	112	P12	268
I/O(D6)	58	79	87	113	T14	271

* Indicates unconnected package pins.
† Contributes only one bit (.i) to the boundary scan register.

XC4005A Pinouts (continued)

Pin Descriptions	PC84	TQ144	PQ160	PQ208	PG156	Bound Scan
I/O	-	80	88	114	T13	274
-	-	-	89*	115*	R12*	-
-	-	-	90*	116*	T12*	-
-	-	-	-	117*	-	-
-	-	-	-	118*	-	-
GND	-	81	91	119	P11	-
I/O	-	82	92	120	R11	277
I/O	-	83	93	121	T11	280
I/O (D5)	59	84	94	122	T10	283
I/O (CS0)	60	85	95	123	P10	286
-	-	-	-	124*	-	-
-	-	-	-	125*	-	-
I/O	-	86	96	126	R10	289
I/O	-	87	97	127	T9	292
I/O (D4)	61	88	98	128	R9	295
I/O	62	89	99	129	P9	298
VCC	63	90	100	130	R8	-
GND	64	91	101	131	P8	-
I/O (D3)	65	92	102	132	T8	301
I/O (RS)	66	93	103	133	T7	304
I/O	-	94	104	134	T6	307
I/O	-	95	105	135	R7	310
-	-	-	-	136*	-	-
-	-	-	-	137*	-	-
I/O (D2)	67	96	106	138	P7	313
I/O	68	97	107	139	T5	316
I/O	-	98	108	140	R6	319
I/O	-	99	109	141	T4	322
GND	-	100	110	142	P6	-
-	-	-	-	143*	-	-
-	-	-	-	144*	-	-
-	-	-	111*	145*	R5*	-
-	-	-	112*	146*	-	-
I/O (D1)	69	101	113	147	T3	325
I/O (RCLK-BUSY/RDY)	70	102	114	148	P5	328
I/O	-	103	115	149	R4	331
-	-	-	-	-	-	-
I/O	-	104	116	150	R3	334
I/O (D0, DIN)	71	105	117	151	P4	337
SGCK4 (DOUT, I/O)	72	106	118	152	T2	340
CCLK	73	107	119	153	R2	-
VCC	74	108	120	154	P3	-
-	-	-	-	155*	-	-
-	-	-	-	156*	-	-
-	-	-	-	157*	-	-
-	-	-	-	158*	-	-
O (TDO)	75	109	121	159	T1	-
GND	76	110	122	160	N3	-
I/O (A0,WS)	77	111	123	161	R1	2
PGCK4 (A1,I/O)	78	112	124	162	P2	5
I/O	-	113	125	163	N2	8
-	-	-	-	-	-	-
I/O	-	114	126	164	M3	11
I/O (CS1,A2)	79	115	127	165	P1	14
I/O (A3)	80	116	128	166	N1	17
-	-	117*	129*	167*	M2*	-
-	-	-	130*	168*	M1*	-
-	-	-	-	169*	-	-
-	-	-	-	170*	-	-
GND	-	118	131	171	L3	-
I/O	-	119	132	172	L2	20
I/O	-	120	133	173	L1	23
I/O (A4)	81	121	134	174	K3	26
I/O (A5)	82	122	135	175	K2	29
-	-	-	-	176*	-	-
-	-	-	136*	177*	-	-
I/O	-	123	137	178	K1	32
I/O	-	124	138	179	J1	35
I/O (A6)	83	125	139	180		38
I/O (A7)	84	126	140	181	J3	41
GND	1	127	141	182	H2	-

* Indicates unconnected package pins.
Boundary Scan Bit 0 = TDO.T

Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 343 = BSCANT.UPD

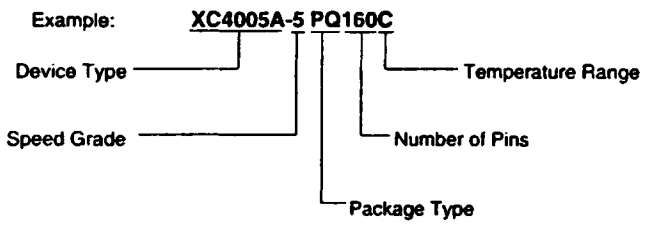
For a detailed description of the device architecture, see pages 2-9 through 2-31.

For a detailed description of the configuration modes and their timing, see pages 2-32 through 2-55.

For detailed lists of package pinouts, see pages 2-57 through 2-81 through 2-85.

For package physical dimensions and thermal data, see Section 4.

Ordering Information



Component Availability

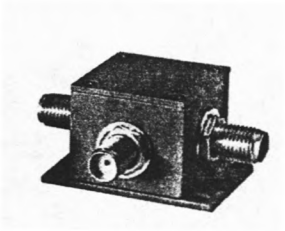
PINS		84	100			120	144	156	160	164	191	196	208		223	240
TYPE		PLAST. PLCC	PLAST. PQFP	PLAST. VQFP	TOP BRAZED CQFP	CERAM. PGA	PLAST TQFP	CERAM PGA	PLAST. PQFP	TOP BRAZED CQFP	CERAM. PGA	TOP BRAZED CQFP	PLAST PQFP	METAL PQFP	CERAM. PGA	METAL PQFP
CODE		PC84	PQ100	VQ100	CB100	PG120	TQ144	PG156	PQ160	CB164	PG191	CB196	PQ208	MQ208	PG223	MQ240
XC4002A	-6	C I	C I	C I		C I										
	-5	C	C	C		C										
	-4	C	C	C		C										
XC4003A	-10				M B	M B										
	-6	C I	C I	C I	M B	C I M B										
	-5	C	C	C		C										
	-4	C	C	C		C										
XC4004A	-6	C I				C I	C I		C I							
	-5	C				C	C		C							
	-4	C				C	C		C							
XC4005A	-6	C I					C I	C I	C I				C I			
	-5	C					C	C	C				C			
	-4	C					C	C	C				C			

C = Commercial = 0° to +70° C I = Industrial = -40° to +85° C M = Mil Temp = -55° to +125° C

B = MIL-STD-883C Class B Parentheses indicates future product plans

POWER SPLITTERS/COMBINERS 50 & 75Ω

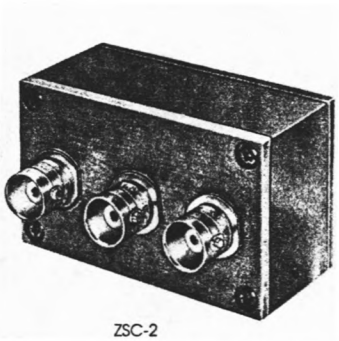
2 WAY-0° 2 kHz to 10 GHz



ZESC-2

ZFSC-2

ZMSC-2



ZSC-2

MODEL NO.	FREQ. RANGE MHz f_L-f_U	ISOLATION dB L Typ.	L Min.	M° Typ.	M° Min.	U Typ.	U Min.	INSERTION LOSS, dB Above 3dB L Typ.	L Max.	M° Typ.	M° Max.	U Typ.	U Max.	PHASE UNBALANCE Degrees L Max.	M° Max.	U Max.	AMPLITUDE UNBALANCE dB L Max.	M° Max.	U Max.	VSWR (:1) S Typ.	S Max.	OUT Typ.	OUT Max.	CAPD DATA (see RF/IF Designer's handbook) Page	CASE STYLE Note B	CONNECTION	PRICE $ Qty. (1-9)
ZESC-2-11	10-2000	19	10	18	13	20	11	0.5	0.9	0.5	1.0	0.6	1.2	1	3	6	0.20	0.30	0.50	see Performance Data and curves				2-94	V37	ar	71.95
ZFSC-2-1	5-500	30	25	28	20	25	20	0.2	0.5	0.3	0.6	0.6	0.8	2	4	4	0.15	0.15	0.30					2-91	K18	ar	44.95
■ ZFSC-2-1-75	0.25-300	20	15	30	25	25	20	0.4	0.75	0.4	0.75	0.4	1.0	2	3	5	0.15	0.20	0.30					2-91	K18	ar	45.95
■ ZFSC-2-1W-75	5-600	44	26	45	30	31	20	0.22	0.6	0.27	0.7	0.46	0.9	1	2	3	0.20	0.30	0.40					2-138	K18	ar	50.95
ZFSC-2-1W	1-750	30	20	28	20	25	20	0.2	0.5	0.4	0.8	0.8	1.0	2	4	4	0.15	0.15	0.30					2-163	K18	ar	48.95
ZFSC-2-2	10-1000	30	20	25	20	23	18	0.2	0.5	0.5	1.0	0.9	1.2	2	4	4	0.15	0.15	0.30					2-163	K18	ar	51.95
	GHz	L1	U1					L1		U1				L1	U1		L1	U1									
ZFSC-2-9G	3.5-9.0	18	12	20	12			0.5	1.5	0.6	1.2			7	10		0.30	0.50						2-93	JJJ142	as	59.95
ZFSC-2-10G	2.0-10.0	15	9	20	12			0.5	1.5	0.6	1.6			7	12		0.60	0.50						2-93	JJJ142	as	69.95
ZFSC-2-4	0.2-1000	20	15	25	20	23	18	0.2	0.5	0.5	1.0	0.9	1.2	2	4	4	0.15	0.15	0.30					2-164	K18	ar	55.95
ZFSC-2-5	10-1500	25	15	30	20	25	18	0.25	0.6	0.5	1.0	0.8	1.5	2	3	4	0.15	0.20	0.50					2-164	K18	ar	59.95
✣ ZFSC-2-6*	0.002-60	27	20	30	20	27	20	0.3	0.6	0.3	0.6*	0.6	1.0	2	3	4	0.15	0.20	0.30					2-165	K18	ar	49.95
✣■ ZFSC-2-6-75	0.004-60	30	20	35	20	25	20	0.5	0.8	0.4	0.8	0.7	1.0	1	2	3	0.15	0.20	0.30					2-165	K18	ar	51.95
ZFSC-2-11	10-2000	14	10	16	14	20	15	1.2	1.5	1.2	1.5	1.0	2.2	1	2	4	0.20	0.30	0.50					2-94	K18	ar	64.95
△ ZFSC-2-2500	10-2500	16	11	17	14	17	14	0.5	0.8	0.6	1.4	0.8	1.5	1	4	8	0.20	0.30	0.40					2-94	K18	ar	74.95
ZMSC-2-1	0.1-400	20	15	25	20	25	20	0.2	0.5	0.4	0.75	0.6	1.0	2	3	4	0.15	0.20	0.30					2-32	M21	at	49.95
ZMSC-2-1W	1-650	25	20	35	20	25	20	0.3	0.5	0.5	0.8	0.7	1.0	2	3	4	0.15	0.20	0.30					2-32	M21	at	54.95
✣ ZMSC-2-2*	0.002-60	27	20	30	20	27	20	0.3	0.6	0.3	0.6	0.6	1.0	2	3	4	0.15	0.25	0.30					2-43	M21	at	59.95
ZSC-2-1	0.1-400	20	15	25	20	25	20	0.2	0.5	0.4	0.75	0.6	1.0	2	3	4	0.15	0.20	0.30					2-32	M22	at	47.95
ZSC-2-1W	1-650	25	20	35	25	25	20	0.3	0.5	0.5	0.8	0.7	1.0	2	3	4	0.15	0.20	0.30					2-32	M22	at	49.95
✣ ZSC-2-2*	0.002-60	25	20	30	20	27	20	0.3	0.6	0.3	0.6	0.6	1.0	2	3	4	0.15	0.25	0.30					2-33	M22	at	52.95
✣■ ZSC-2-2-75*	0.002-60	25	20	30	20	27	20	0.3	0.6	0.3	0.6	0.6	1.0	2	3	4	0.15	0.25	0.30					2-96	M22	at	53.95
ZSC-2-4	10-1000	25	20	35	20	25	20	0.2	0.5	0.5	0.8	0.7	1.3	2	4	6	0.15	0.20	0.30					2-33	M22	at	52.95
■ ZSC-2375	55-85			35	25					0.3	0.5				1			0.10						2-166	M22	at	52.95
■ ZSC-2-1-75	0.25-300	20	15	30	20	20	15	0.4	0.75	0.4	0.75	0.4	1.0	2	3	5	0.15	0.20	0.30					2-166	M22	at	49.95

NOTES:

- * Isolation specified to 0.004 MHz
- o When only specification for M range given, specification applies to entire frequency range.
- ✣ At low range frequency band (fL to 10 fL), linearly derate maximum input power by 13 dB.
- ■ Denotes 75 Ohm model, for coax connector models 75 Ohm BNC connectors are standard.
- △ Available only with SMA connectors
- A. General Quality Control Procedures, Environmental Specifications, Hi-Rel and MIL description are given in section 0, see "Mini-Circuits Guarantees Quality" article.
- B. Connector types and case mounted options, case finishes are given in section 0, see "Case styles & Outline Drawings".
- C. Prices and specifications subject to change without notice.
- 1. Absolute maximum power, voltage and current ratings:
  - 1a. Matched power rating, models ZAPD, ZN2PD, ZC2PD 10 Watt ZAPD-900-5W, 5W (as a splitter), other models 1 Watt
  - 1b. Internal load dissipation 0.125 Watt, ZAPD-900-5W, 1W max ZN2PD-9G, 0.25W

coaxial connections

see case style outline drawing for pin locations

PORT	ar	as	at
SUM PORT	3	S	2
PORT 1	1	1	1
PORT 2	2	2	3
GND EXT.			
CASE GND			
NOT USED			

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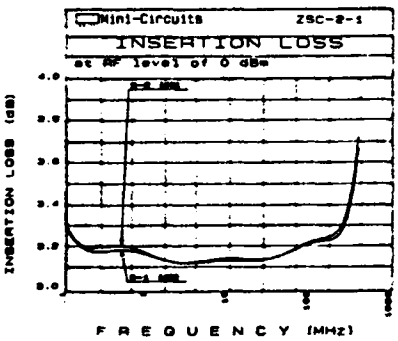
2WAY-0°

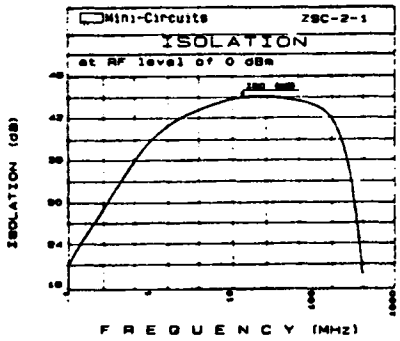
Power Splitter/Combiners

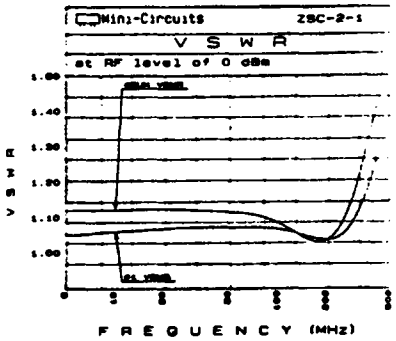
50 ohms

ZMSC-2-1, ZSC-2-1

0.1 to 400MHz





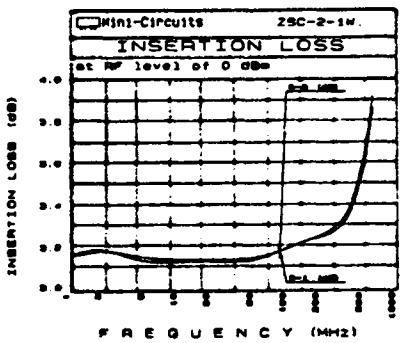


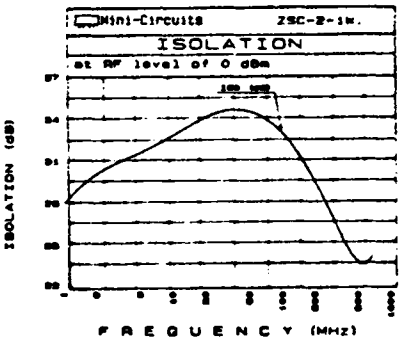
FREQUENCY (MHz)	INSERTION LOSS (dB) S-1	INSERTION LOSS (dB) S-2	AMPLITUDE UNBALANCE (dB) 1-2	ISOLATION (dB)
0.1	3.33	3.33	0.00	22.82
0.5	3.24	3.23	0.01	35.06
1.0	3.25	3.24	0.01	39.76
5.0	3.19	3.15	0.04	51.14
10.0	3.17	3.17	0.00	49.55
20.0	3.23	3.20	0.03	44.22
50.0	3.23	3.20	0.03	37.22
100.0	3.27	3.26	0.01	32.39
128.6	3.30	3.29	0.01	30.81
171.5	3.30	3.31	0.01	29.38
200.0	3.31	3.29	0.02	28.96
257.2	3.35	3.33	0.02	29.45
300.0	3.42	3.39	0.03	31.46
328.6	3.46	3.47	0.01	33.72
400.0	3.49	3.45	0.04	34.03

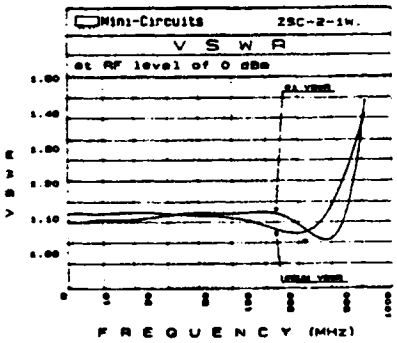
FREQUENCY (MHz)	VSWR S	VSWR 1	VSWR 2
0.1	1.49	1.96	1.97
0.5	1.14	1.20	1.20
1.0	1.14	1.16	1.16
5.0	1.15	1.11	1.11
10.0	1.15	1.11	1.11
20.0	1.16	1.11	1.11
50.0	1.15	1.10	1.10
100.0	1.13	1.08	1.08
128.6	1.12	1.07	1.08
171.5	1.08	1.07	1.07
200.0	1.06	1.07	1.07
257.2	1.05	1.10	1.11
300.0	1.10	1.15	1.16
328.6	1.15	1.18	1.20
400.0	1.25	1.24	1.26

ZMSC-2-1W, ZSC-2-1W

1 to 650MHz







FREQUENCY (MHz)	INSERTION LOSS (dB) S-1	INSERTION LOSS (dB) S-2	AMPLITUDE UNBALANCE (dB) 1-2	ISOLATION (dB)
1.0	3.31	3.28	0.03	27.72
5.0	3.18	3.21	0.03	37.92
10.0	3.19	3.21	0.02	45.09
20.0	3.22	3.24	0.02	46.45
50.0	3.21	3.24	0.03	37.51
100.0	3.29	3.29	0.00	31.91
152.4	3.35	3.34	0.01	28.72
200.0	3.33	3.35	0.02	26.74
260.6	3.38	3.40	0.02	24.91
300.0	3.40	3.46	0.06	24.02
390.4	3.47	3.49	0.02	22.64
455.3	3.59	3.61	0.02	22.15
500.0	3.62	3.65	0.03	22.04
563.5	3.68	3.71	0.03	22.33
650.0	3.86	3.89	0.03	23.85

FREQUENCY (MHz)	VSWR S	VSWR 1	VSWR 2
1.0	1.11	1.26	1.26
5.0	1.13	1.16	1.16
10.0	1.13	1.14	1.14
20.0	1.14	1.14	1.14
50.0	1.13	1.13	1.13
100.0	1.13	1.12	1.12
152.4	1.14	1.11	1.11
200.0	1.13	1.10	1.10
260.6	1.14	1.07	1.08
300.0	1.15	1.06	1.06
390.4	1.18	1.03	1.03
455.3	1.21	1.05	1.05
500.0	1.23	1.07	1.07
563.5	1.26	1.12	1.12
650.0	1.30	1.19	1.18

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case styles

outline dimensions (inch / mm)

case no.	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	wt. grams	NOTES*
A01	.770 19.56	.800 20.32	.385 9.78	.400 10.16	.370 9.40	.400 10.16	.200 5.08	.20 5.08	.14 3.56	.031 .79									5.2	A1,B3,E1,B7
A03	.480 12.19	.500 12.70	.390 9.91	.405 10.29	.210 5.33	.230 5.84	.100 2.54	.20 5.08	.14 3.56	.020 .51									2.3	A1,B4,E1,B7
A04	.770 19.56	.800 20.32	.200 5.08	.210 5.33	.370 9.40	.400 10.16	.200 5.08	.20 5.08	.14 3.56	.031 .79									3.7	A1,B3,E1,B7
A05	.770 19.56	.800 20.32	.240 6.10	.250 6.35	.370 9.40	.400 10.16	.200 5.08	.20 5.08	.14 3.56	.031 .79									3.7	A1,B3,E1,B7
A06	.770 19.56	.800 20.32	.285 7.24	.310 7.87	.370 9.40	.400 10.16	.200 5.08	.20 5.08	.14 3.56	.031 .79									5.2	A1,B3,E1,B7
A11	.480 12.19	.500 12.70	.240 6.10	.255 6.48	.210 5.33	.230 5.84	.100 2.54	.20 5.08	.14 3.56	.020 .51									1.9	A1,B4,E1,B7
B02	.480 12.19	.500 12.70	.240 6.10	.255 6.48	.210 5.33	.230 5.84	.16 4.06	.100 2.54	.14 3.56	.20 5.08	.020 .51								1.9	A1,B4,E1,B7
B13	.480 12.19	.500 12.70	.390 9.91	.405 10.29	.210 5.33	.230 5.84	.16 4.06	.100 2.54	.14 3.56	.20 5.08	.020 .51								2.3	A1,B4,E1,B7
C07	.770 19.56	.810 20.57	.380 9.65	.410 10.41	.030 .76	.200 5.08	.20 5.08	.14 3.56											11.0	A1,E1,B7
C145	.770 19.56	.810 20.57	.380 9.65	.410 10.41	.030 .76	.200 5.08	.20 5.08	.14 3.56											11.0	A1,E1,B7
D08	1.000 25.40	1.025 26.04	.390 9.91	.430 10.92	.500 12.70	.525 13.34	.025 .64	.300 7.62	.200 5.08	.09 2.29	.13 3.30	.150 3.81	.20 5.08	.14 3.56					8.5	A1,E1,B7
D09	1.000 25.40	1.025 26.04	.240 6.10	.280 7.11	.500 12.70	.525 13.34	.025 .64	.300 7.62	.200 5.08	.09 2.29	.13 3.30	.150 3.81	.20 5.08	.14 3.56					7.5	A1,E1,B7
E10	1.580 40.13	1.620 41.15	.380 9.65	.410 10.41	.770 19.56	.810 20.57	.030 .76	.200 5.08	.10 2.54	.20 5.08	.14 3.56								23.0	A1,E1,B7
F14	2.00 50.80	2.00 50.80	.75 19.05	1.00 25.40	.25 6.35	1.500 38.10	.125 3.18	.39 9.91	1.00 25.40	.50 12.70	1.00 25.40								170.0	A10, C1,D2
F53	2.00 50.80	2.0 50.80	.75 19.05	1.00 25.40	.13 3.30	1.750 44.45	.125 3.18	.39 9.91	1.00 25.40	.50 12.70	1.00 25.40								170.0	A10 C1,D2
F183	1.26 32.00	1.00 25.40	.70 17.78	.200 5.08	.200 5.08	.860 21.84	.125 3.18	.35 8.89	.63 16.00	.38 9.65	.50 12.70								24	A4,B1,D17
G15	1.25 31.75	1.25 31.75	.75 19.06	.63 16.00	.38 9.65	.61 15.49	— —	.80 20.32	.80 20.32	.76 19.30	.125 3.18	1.688 42.88	2.18 55.37	.75 19.05	.07 1.78				85.0	A10,A18,B1, D1,D7
G144	1.25 31.75	1.25 31.75	— —	.63 16.00	.38 9.65	.61 15.49	— —	— —	— —	.76 19.30	.125 3.18	1.688 42.88	2.18 55.37	.75 19.05	.07 1.78				85.0	A10,A18, B6,D6
H16	1.25 31.75	1.25 31.75	.75 19.05	.63 16.00	.38 9.65	1.000 25.40	.125 3.18	1.000 25.40	— —	— —	.125 3.18	1.688 42.88	2.18 55.37	.75 19.05	.07 1.78				70.00	A10,A18,B1, D2,D3,D4
J17	1.25 31.75	1.25 31.75	.75 19.05	.63 16.00	.38 9.65	1.000 25.40	.125 3.18	1.000 25.40	— —	— —	.125 3.18	1.688 42.88	2.18 55.37	.75 19.05	.07 1.78				75.0	A10,A18, B1,D2,D3
K18	1.25 31.75	1.25 31.75	.75 19.05	.63 16.00	.38 9.65	1.000 25.40	.125 3.18	1.000 25.40	— —	— —	.125 3.18	1.688 42.88	2.18 55.37	.75 19.05	.07 1.78				70.0	A10,A18,B1, C1,D2,D3
L19	1.50 38.10	1.13 28.70	1.00 25.40	.50 12.70	.155 3.94	2.345 59.56	.138 3.51	.987 25.07	2.50 63.50	.10 2.54	.31 7.87	1.19 30.23	— —	.66 16.76	— —	— —	.150 3.81		37.0	A6,A11,A18, B2,D6
L20	2.25 57.15	1.38 35.05	1.24 31.50	.50 12.70	.150 3.81	3.100 78.74	.138 3.51	1.238 31.45	3.25 82.55	.10 2.54	.40 10.16	1.86 47.24	— —	.64 16.26	— —	— —	.150 3.81		74.0	A6,A11,A18, B2,D5
M21	1.50 38.10	1.13 28.70	1.00 25.40	.50 12.70	.155 3.94	2.345 59.56	.138 3.51	.987 25.07	2.50 63.50	.10 2.54	.31 7.87	.75 19.05	1.19 30.23	.66 16.76	— —	— —	.150 3.81		40.0	A6,A11,A18, B2,C1,D6
M22	2.25 57.15	1.38 35.05	1.24 31.50	.50 12.70	.150 3.81	3.100 78.74	.138 3.51	1.238 31.45	3.25 82.55	.10 2.54	.40 10.16	1.15 29.21	1.86 47.24	.64 16.26	— —	— —	.150 3.81		74.0	A6,A11,A18, B2,C1,D5
M23	2.25 57.15	1.38 35.05	1.24 31.50	.50 12.70	.150 3.81	3.100 78.74	.138 3.51	1.238 31.45	3.25 82.55	.10 2.54	.63 16.00	1.06 26.92	1.63 41.40	.69 17.53	— —	— —	.150 3.81		70.0	A6,A11,A18, B2,C1,D6

tolerance .x±.1 .xx±.03 .xxx±.015 inch **oz. = grams x.0353**

* NOTES:

A. MATERIAL AND FINISH
- A1. Header material: C.R.S. Pin material: #52 alloy. Finish: electro tin, hot-oil flowed. Cover material: cupro-nickel.
- A4. Case material: aluminum alloy. Finish: iridite per MIL-C-5541
- A6. Case material: aluminum alloy. Finish: blue paint over iridite.
- A10. Case material: aluminum alloy. Finish: grey paint or yellow iridite.
- A11. Case material: aluminum alloy. Finish: blue anodized.
- A18. Mounting bracket finish: iridite or clear anodize.

B. MOUNTING
- B1. Mounting bracket available on request. Add suffix B to part number.
- B2. Mounting bracket available on request. For bracket mounted on connector end add suffix B to part number and $5.00 to unit cost. For bracket mounted on the rear, add suffix BR to part number and add $1.50 to unit cost.
- B3. Insulated spacer available. Request P/N B14-045-01.
- B4. Insulated spacer available. Request P/N B-14-047-01.
- B6. Bracket version only.
- B7. Pins meniscus (of header): 0.015" max.

C. MARKING
- C1. For port markings 1, 2, and 3 see specification data sheet.

D. CONNECTORS
- D1. Connectors: SMA Standard. BNC on request (no charge). Male SMA on request, consult factory.
- D2. Connectors: please specify, unless otherwise noted: BNC is standard. TNC, SMA and Type N, consult factory. (ZAPD -4 units not available with BNC).
- D3. For Bracket Version, Option B, this dimension, "C**", changes from 0.75 to 0.94 inches.
- D4. FTB Models available: *A15 female BNC/isolated female BNC. *C15 male BNC/isolated female BNC. FT Models available: *A16 female BNC/female BNC 75 ohms. *B16 female BNC/male BNC 75 ohms. *C16 male BNC/female BNC 75 ohms.
- D5. Connectors: BNC standard, TNC consult factory.
- D6. Connectors: Female SMA only. Male SMA available on request, consult factory.
- D7. For ZFSC-5 a fifth connector is offered as Port 5 in-line and opposite of sum(s) port.
- D17. Connectors: Female SMA only.

E. SPECIAL TOLERANCES
- E1. Pin diameter ±.005 inch.

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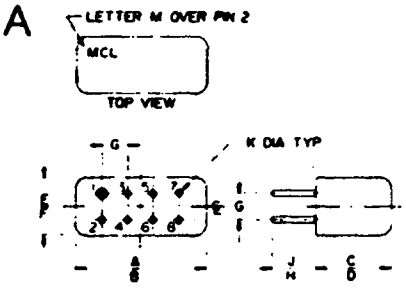
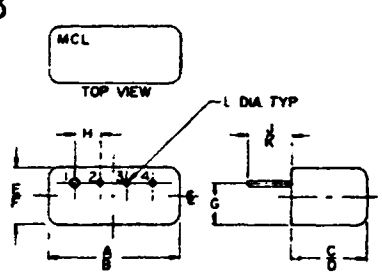
A



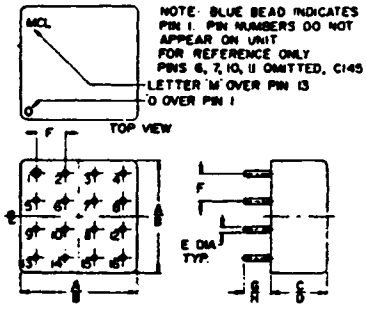
NOTE Blue Bead indicates pin 1
Pin numbers do not appear on unit
For reference only

B

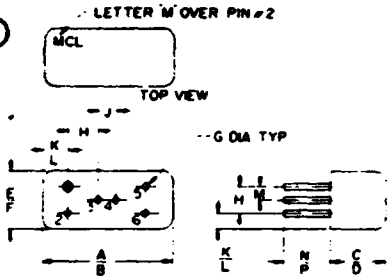


NOTE Blue Bead indicates pin 1
Pin numbers do not appear on unit
For reference only

C

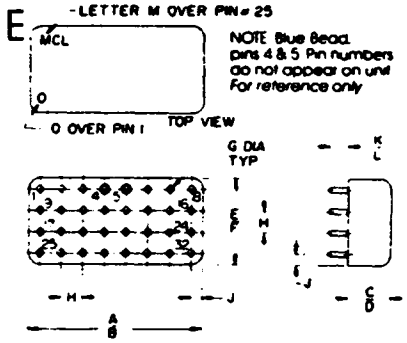


D



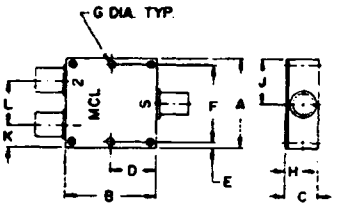
NOTE Blue Bead indicates pin 1
Pin numbers do not appear on unit
For reference only

E

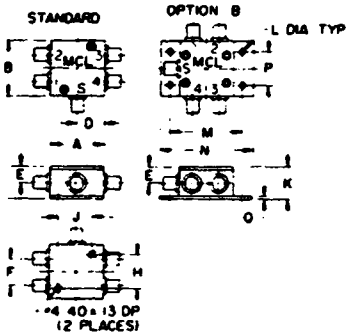


NOTE Blue Bead pins 4 & 5 Pin numbers do not appear on unit
For reference only

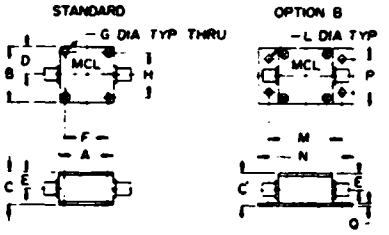
F



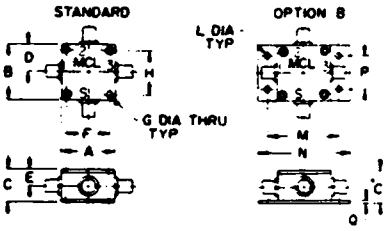
G



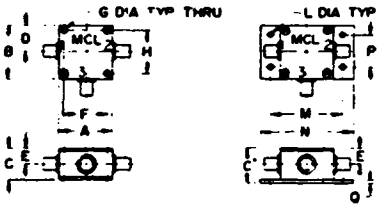
H



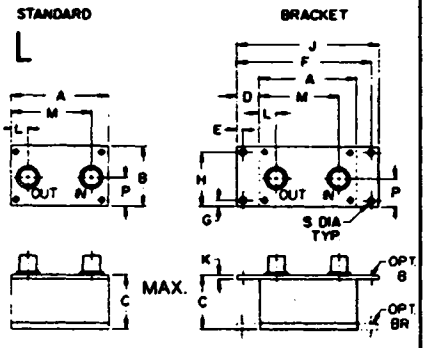
J



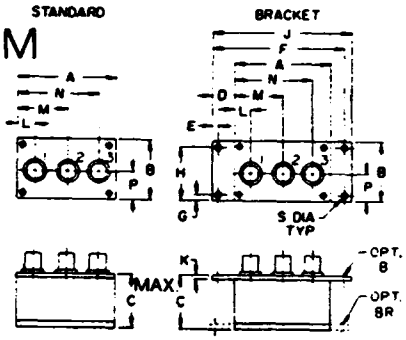
K



L



M



Surface Mount

BP2 JPS JYPS LRPS SCP SYPS

	MODEL NO.	FREQ. RANGE MHz f_L-f_U	ISOLATION dB L Typ.	ISOLATION dB L Min.	ISOLATION dB M° Typ.	ISOLATION dB M° Min.	ISOLATION dB U Typ.	ISOLATION dB U Min.	INSERTION LOSS, dB Above 3dB L Typ.	INSERTION LOSS, dB Above 3dB L Max.	INSERTION LOSS, dB Above 3dB M° Typ.	INSERTION LOSS, dB Above 3dB M° Max.	INSERTION LOSS, dB Above 3dB U Typ.	INSERTION LOSS, dB Above 3dB U Max.	PHASE UNBALANCE Degrees L Max.	PHASE UNBALANCE Degrees M° Max.	PHASE UNBALANCE Degrees U Max.	AMPLITUDE UNBALANCE dB L Max.	AMPLITUDE UNBALANCE dB M° Max.	AMPLITUDE UNBALANCE dB U Max.	CAPD DATA (see RF/IF Designer hand-book) Page	CASE STYLE Note B	CONNECTION	PRICE $ Qty. (1-9)
NEW	BP2C	810-960			25	18					0.6	0.9				3.0			0.2		—	XX211	jm	1.29***
NEW	BP2G	1420-1660			28	20					0.6	1.0				3.0			0.2		—	XX211	jm	0.99***
NEW	BP2P	1710-1990			30	20					0.7	1.0				3.0			0.2		—	XX211	jm	1.24***
	JPS-2-1N	350-550			30	20					0.25	0.5				3.0			0.3		2-129	BH292	hv	8.95
	JPS-2-1W	3-750	36	20	28	17	19	16	0.5	0.8	0.4	1.0	0.9	1.4	1.0	2.0	4.0	0.2	0.3	0.4	2-130	BH292	hv	8.95
	JPS-2-4	100-1000			22	16					0.5	1.4				5.0			0.4		2-130	BH292	hv	9.95
	JPS-2-900	400-900			24	18					0.5	1.2				3.0			0.4		2-131	BH292	hv	9.95
■	JYPS-2-4-75	5-1000	24	17	25	20	30	18	0.4	0.8	0.4	1.0	0.8	1.5	3.0	4.0	5.0	0.2	0.3	0.4	2-138	BJ293	jf	16.95
◆	LRPS-2-1	5-500	50	25	33	24	30	23	0.25	0.5	0.3	0.6	0.5	1.2	1.0	2.0	3.0	0.15	0.2	0.3	2-118	QQQ130	am	8.95
◆■	LRPS-2-1-75	2-500	35	18	35	25	27	20	0.30	0.8	0.35	0.6	0.5	1.0	1.0	2.0	3.0	0.15	0.2	0.3	2-139	QQQ130	am	8.95
◆■	LRPS-2-1W-75	10-650	28	22	29	24	30	20	0.5	1.0	0.6	0.75	0.6	1.2	1.0	2.0	3.0	0.15	0.2	0.3	2-139	QQQ130	am	9.95
◆	LRPS-2-4	10-1000	25	20	23	16	19	14	0.3	0.5	0.4	0.9	0.8	1.5	1.0	3.0	5.0	0.15	0.2	0.4	2-120	QQQ130	am	19.95
◆	LRPS-2-11	20-2000	19	15	21	15	30	15	0.6	0.8	0.7	1.0	0.8	1.5	2.0	3.0	5.0	0.2	0.3	0.7	2-132	QQQ130	gn	24.95
◆	LRPS-2-25	1700-2500			20	16					0.8	1.3				10.0			0.9		2-132	QQQ130	gn	21.95
◆	LRPS-2-980	800-980			30	18					0.5	1.0				3.0			0.5		2-133	QQQ130	am	8.95
	SCP-2-1	0.1-400	25	15	30	20	25	20	0.3	1.2	0.2	0.6	0.4	1.1	2.0	2.0	3.0	0.15	0.2	0.3	2-92	YY101	aq	10.45
	SCP-2-1A	1-550	25	20	25	20	25	20	0.3	0.6	0.3	0.6	0.7	1.3	2.0	2.0	3.0	0.15	0.2	0.4	2-92	YY101	aq	10.45
	SYPS-2-1	2-500	40	20	32	20	30	20	0.2	0.6	0.3	0.75	0.6	1.0	2.0	3.0	4.0	0.2	0.3	0.5	2-133	TTT167	hk	12.95

L = low range (f_L to 10 f_L) M = mid range (10 f_L to f_U/2) U = upper range (f_U/2 to f_U)

NSN GUIDE

MCL NO.	NSN	MIL-P-23971/15*
MSC-2-1	6625-01-124-8595	02
PSC-2-1	6625-00-548-0739	01
PSC-2-1W	5985-01-190-7701	
PSC-2-2	6625-01-143-2571	
PSC-2-4	6625-01-230-0492	
TSC-2-1	5895-01-332-8100	

* units are not QPL listed

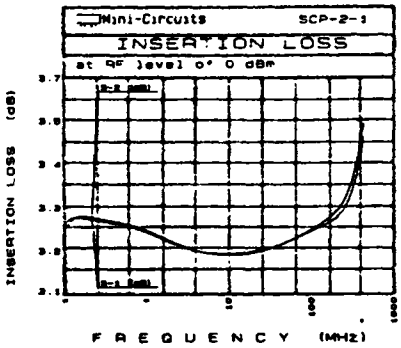
pin connections see case style outline drawing for pin locations

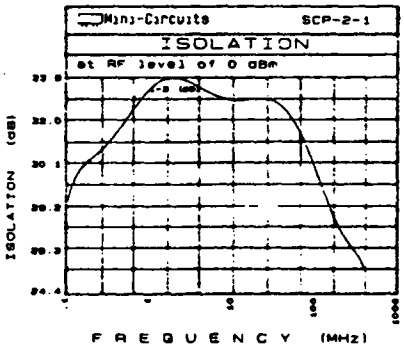
PORT	aj	ak	am	an	ap	aq	gn	he	hk	hv	jf	jm
SUM PORT	1	2	6	1	1	1	6	5	3	1	1	2
PORT 1	2	1	4	4	5	5	4	9	1	3	3	8
PORT 2	4	3	3	5	6	6	3	1	2	4	6	5
GND EXT.	3	4,5	1	2,3,6,7,8	2,3,4,7,8	2,3,4,7,8	1,2,5	all other pins	4,5,6	6	7,8	1,3,4,6,7
CASE GND	3	4,5	—	2,3,6,7,8	2,3,4,7,8	—	—	all other pins	—	—	—	—
NOT USED			2,5		—	—	—		—	2,5	2,4,5	—

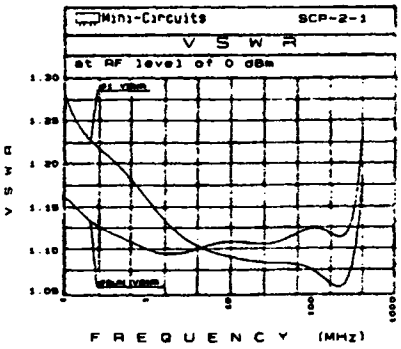
Power Splitter/Combiners 50 ohms

SCP-2-1

0.1 to 400 MHz





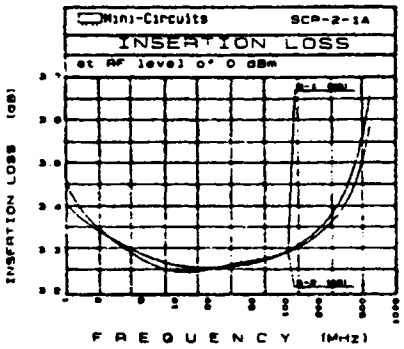


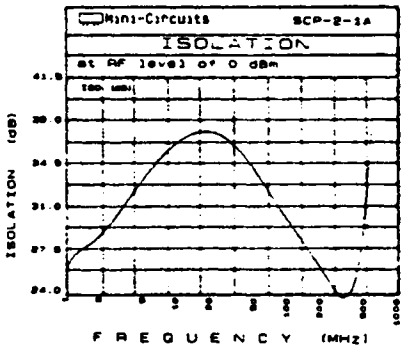
FREQUENCY (MHz)	INSERTION LOSS (dB) S-1	INSERTION LOSS (dB) S-2	AMPLITUDE UNBALANCE (dB) 1-2	ISOLATION (dB) 1-2
0.100	3.26	3.25	0.01	28.83
0.200	3.26	3.27	0.01	30.54
0.500	3.24	3.24	0.00	31.67
1.000	3.22	3.23	0.01	33.78
2.000	3.19	3.19	0.00	33.87
5.000	3.16	3.16	0.00	33.17
10.000	3.16	3.16	0.00	33.01
20.000	3.17	3.16	0.01	33.04
50.000	3.19	3.19	0.00	32.14
100.000	3.24	3.23	0.01	29.88
102.787	3.24	3.22	0.02	29.70
113.036	3.22	3.21	0.01	29.39
133.533	3.23	3.23	0.00	28.70
200.000	3.32	3.28	0.04	26.99
400.000	3.62	3.55	0.07	24.42

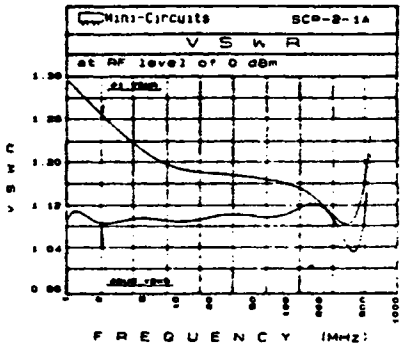
FREQUENCY (MHz)	VSWR S	VSWR 1	VSWR 2
0.100	1.16	1.27	1.28
0.200	1.13	1.22	1.22
0.500	1.12	1.20	1.20
1.000	1.10	1.15	1.15
2.000	1.10	1.13	1.13
5.000	1.10	1.10	1.10
10.000	1.11	1.09	1.09
20.000	1.11	1.09	1.09
50.000	1.11	1.08	1.09
100.000	1.12	1.08	1.08
102.787	1.12	1.08	1.08
113.036	1.12	1.07	1.08
133.533	1.12	1.07	1.07
200.000	1.12	1.06	1.06
400.000	1.27	1.19	1.16

SCP-2-1A

1 to 550 MHz







FREQUENCY (MHz)	INSERTION LOSS (dB) S-1	INSERTION LOSS (dB) S-2	AMPLITUDE UNBALANCE (dB) 1-2	ISOLATION (dB) 1-2
1.000	3.35	3.39	0.04	26.45
2.000	3.29	3.29	0.00	28.70
5.000	3.24	3.23	0.01	33.26
10.000	3.21	3.19	0.02	36.59
20.000	3.21	3.21	0.00	37.33
50.000	3.22	3.23	0.01	34.01
100.000	3.27	3.24	0.03	29.89
120.000	3.27	3.26	0.01	28.73
135.000	3.27	3.29	0.02	27.97
149.000	3.25	3.26	0.01	27.34
164.000	3.29	3.28	0.01	26.85
179.000	3.31	3.30	0.01	26.23
200.000	3.32	3.33	0.01	25.81
275.000	3.33	3.33	0.00	24.35
550.000	3.64	3.56	0.08	41.47

FREQUENCY (MHz)	VSWR S	VSWR 1	VSWR 2
1.000	1.11	1.35	1.35
2.000	1.09	1.29	1.29
5.000	1.09	1.22	1.22
10.000	1.10	1.19	1.19
20.000	1.10	1.18	1.18
50.000	1.10	1.17	1.17
100.000	1.11	1.16	1.16
120.000	1.11	1.16	1.16
135.000	1.11	1.15	1.15
149.000	1.12	1.14	1.15
164.000	1.11	1.14	1.14
179.000	1.11	1.13	1.13
200.000	1.12	1.12	1.13
275.000	1.10	1.10	1.10
550.000	1.23	1.25	1.21

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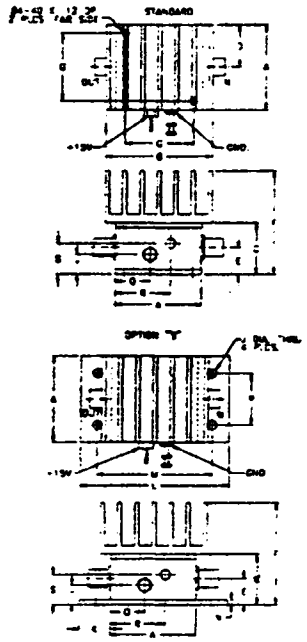
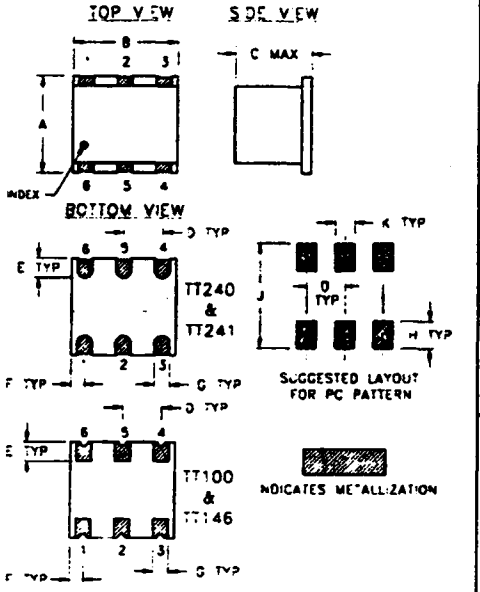
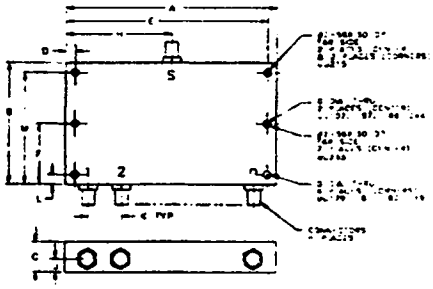
SS



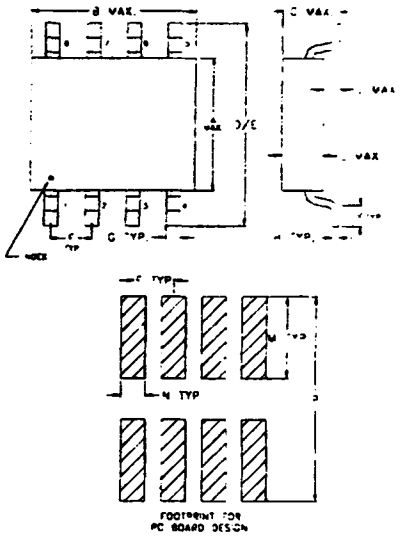
TT



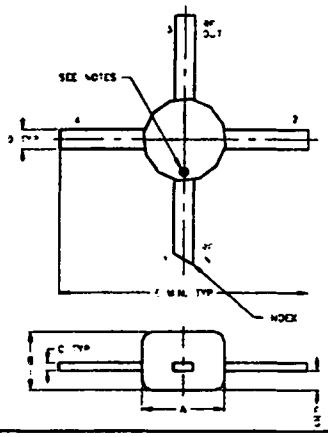
UU



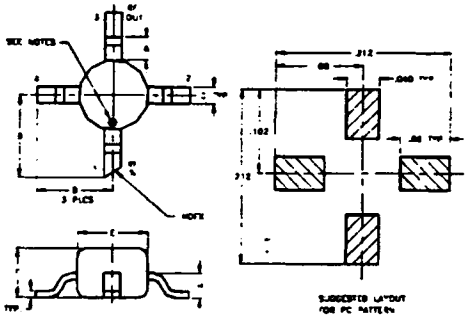
XX



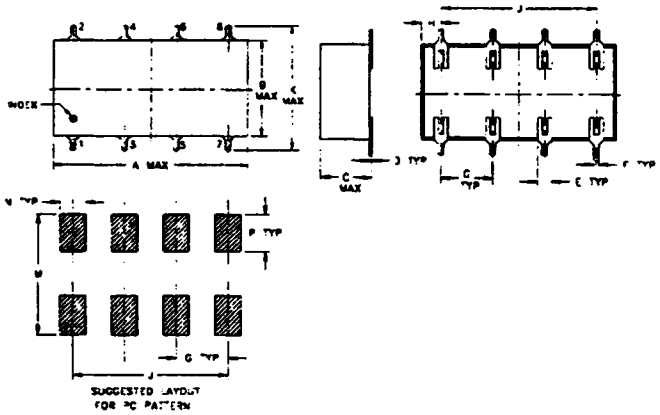
VV



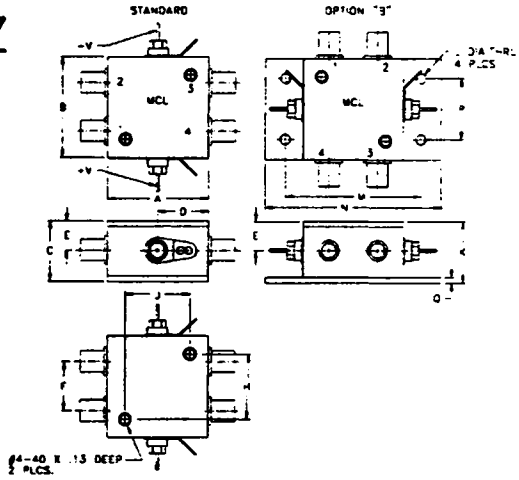
WW



YY



ZZ



In Stock... Immediate Delivery

For Custom Versions Of Standard Models Consult Our Applications Dept.

case styles

outline dimensions (inch / mm)

case no.	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	wt. grams.	NOTES*
SS98	1.25 31.75	1.56 39.62	.75 19.05	.63 16.00	.39 9.91	1.50 38.10	1.000 25.40	— —	.125 3.18	.46 11.68	2.18 55.37	1.688 42.88	.07 1.78	.750 19.05	.50 12.70	.80 20.32	.45 11.43	.29 7.37	85.0	A8, A18, B1, D6
TT100	.250 6.35	.310 7.87	.20 5.08	.100 2.54	.050 1.27	.055 1.40	.040 1.02	.070 1.78	.270 6.86	.050 1.27									.50	A14, F2
TT146	.250 6.35	.310 7.87	.275 6.99	.100 2.54	.050 1.27	.055 1.40	.040 1.02	.070 1.78	.270 6.86	.050 1.27									.50	A14, F0
TT240	.250 6.35	.310 7.87	.20 5.08	.100 2.54	.050 1.27	.055 1.40	.040 1.02	.070 1.78	.270 6.86	.050 1.27									.50	A20, F3
TT241	.250 6.35	.310 7.87	.275 6.99	.100 2.54	.050 1.27	.055 1.40	.040 1.02	.070 1.78	.270 6.86	.050 1.27									.50	A20, F0
UU102	3.50 88.90	2.00 50.80	.50 12.70	.150 3.81	3.350 85.09	1.00 25.40	.125 3.18	1.75 44.45	.20 5.08	.55 13.97									120.0	A10, C2, D17
UU179	8.50 215.90	3.95 100.33	.75 19.05	.250 6.35	8.250 209.55	— —	.187 4.75	4.250 107.95	.38 9.65	.500 12.70	.475 12.07	3.475 88.27							282	A4, D17
UU181	2.25 57.15	2.30 58.42	.63 16.00	.125 3.18	2.125 53.98	— —	.125 3.18	1.13 28.70	.31 7.87	.500 12.70	.125 3.18	2.175 55.24							51	A4, D17
UU182	2.75 69.85	2.80 71.12	.63 16.00	.125 3.18	2.625 66.68	— —	.125 3.18	1.38 35.05	.31 7.87	.500 12.70	.125 3.18	2.675 67.95							67	A4, D17
UU187	6.00 152.40	1.62 41.15	.88 22.35	.250 6.35	5.750 146.05	.810 20.57	.144 3.66	3.00 76.20	.44 11.18	1.00 25.40	— —	— —							274	A4, D23
UU188	3.50 88.90	2.13 54.10	.88 22.35	.150 3.81	3.350 85.09	1.06 26.92	.125 3.18	1.75 44.45	.44 11.18	.89 22.61	— —	— —							184	A4, D23
UU215	4.00 101.60	1.25 31.75	.38 9.65	.125 3.18	3.875 98.43	.500 12.70	#2-56 —	2.00 50.80	.19 4.83	.500 12.70	— —	1.125 28.58							77	A4, D17
UU233	1.50 38.10	1.00 25.40	.38 9.65	.125 3.18	1.375 34.93	.500 12.70	#2-56 —	.75 19.05	.19 4.83	.50 12.70									28.0	A8, B8, C2, D17
UU244	2.25 57.15	1.25 31.75	.50 12.70	.150 3.81	2.100 53.34	.62 15.75	.125 3.18	1.12 28.45	.19 4.83	.50 12.70									70	A4, C2, D17
UU449	9.78 248.41	3.13 79.50	.88 22.35	.200 5.08	9.580 243.33	— —	.144 3.66	4.89 124.21	.44 11.18	.89 22.61	.200 5.08	2.930 74.42							840	A4, D25
VV105	.085 2.16	.060 1.52	.008 .20	.020 .51	.256 6.50	.012 .30	.025 .64												.015	A13, C4, E2
WW107	.020 .51	.10 2.54	.020 .51	.092 2.34	.085 2.16	.060 1.52	.008 .20	.026 .66											.015	A13, C4, E2, F4
XX112	.18 4.57	.18 4.57	— —	.40 10.16	.36 9.14	.050 1.27	.015 .38	.005 .13	.005 .13	.07 1.78	.06 1.52	.100 2.54	.03 0.76	.420 10.69					.15	A15, E2, F19
XX211	.163 4.14	.202 5.13	.077 1.96	.25 6.35	.22 5.59	.050 1.27	.017 .43	.009 .23	.025 .63	.03 .76	— —	.050 1.27	.03 0.76	.270 6.86					.10	A13, E2, F16
YY101	.75 19.05	.38 9.65	.20 5.08	.010 .25	.050 1.27	.020 .51	.200 5.08	.075 1.91	.600 15.24	.450 11.43	— —	.47 11.94	.100 2.54	.150 3.81					1.6	A13, E2, E5, F5
YY109	.75 19.05	.38 9.65	.20 5.08	.010 .25	.050 1.27	.020 .51	.200 5.08	.075 1.91	.600 15.24	.72 18.29	— —	.74 18.80	.100 2.54	.150 3.81					1.6	A13, E2, E5, F0
YY161	.75 19.05	.38 9.65	.28 7.11	.010 .25	.050 1.27	.020 .51	.200 5.08	.075 1.91	.600 15.24	.450 11.43	— —	.47 11.94	.100 2.54	.150 3.81					1.6	A13, E2, F6
ZZ121	1.25 31.75	1.25 31.75	.75 19.05	.63 16.00	.38 9.65	.61 15.49	— —	.800 20.32	.800 20.32	.76 19.30	.125 3.18	1.688 42.88	2.18 55.37	.75 19.05	.07 1.78				85.0	A10, A18, B1, D6

tolerance .x±.1 .xx±.03 .xxx±.015 inch **oz. = grams x.0353**

* NOTES:

A. MATERIAL AND FINISH
- A1. Header material: C.R.S. Pin material: #52 alloy. Finish: electro tin, hot oil flowed. Cover material: cupro-nickel.
- A4. Case material: aluminum alloy. Finish: iridite per MIL-C-5541.
- A6. Case material: aluminum alloy. Finish: blue paint over iridite.
- A8. Case material: aluminum alloy. Finish: case iridite Heat sink, black anodize.
- A10. Case material: aluminum alloy. Finish: grey paint or yellow iridite.
- A11. Case material: aluminum alloy. Finish: blue anodized.
- A13. Case material: plastic. Lead finish: Tin or tin-lead plate.
- A14. Case material: ceramic or plastic, ceramic base. Terminations: palladium platinum silver.
- A15. Case material: kovar. Lead material: kovar. Finish: gold plate per MIL-G-45204.
- A18. Mounting bracket finish: iridite or clear anodize.
- A20. Case material: ceramic. Terminations: solder plate over nickel. Board edges straight.

B. MOUNTING
- B1. Mounting bracket available on request. Add suffix B to part number.
- B7. Pin's meniscus (of header) 0.015" max.
- B8. #2-56 UNC-2B mounting holes provided to .32" deep minimum.

C. MARKING
- C2. Consecutive marking n = no. of way power splitter.
- C4. RF input lead (1) identified by diagonally cut lead: the cut may be 45°(ref) in either direction. It may also have an additional orientation mark. Model dash number identified by color dot or alphanumeric code on case. See specification data sheet.
- C5. RF output is identified by index mark, model dash number by alphanumeric code.

D. CONNECTORS
- D6. Connectors: Female SMA only. Male SMA available on request, consult factory.
- D17. Connectors: Female SMA only.
- D23. Connectors: Please specify female type N or SMA.
- D25. Connectors: Female N standard. For other connectors consult factory.

E. SPECIAL TOLERANCES
- E1. Pin diameter ±.005 inch.
- E2. Lead width ±.010; lead thickness ±.005 inch.
- E5. For SCM mixers, long lead version (YY109) is available upon request, consult factory. To order short lead version (case YY101) add -NL suffix.

F. PACKAGING
- F0. Not available in Tape & Reel.
- F1-29. Tape and reel packaging available. See Tape and Reel Packaging Information for details. To order Tape & Reel version add -TR suffix to mode

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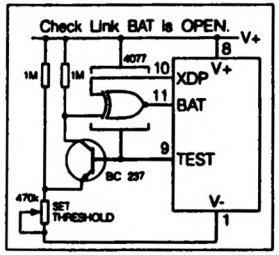
ANALOGUE INPUTS

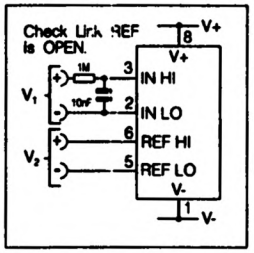
The analogue inputs IN HI, IN LO, REF HI and REF LO are differential inputs. They respond to the voltage across them and not their voltage with respect to the power supply. However, no input must be higher than 0.5V below the positive supply or lower than 1.0V above the negative supply (note that the DPM 3S generates its own negative supply of approximately 5V below GND). If there is any danger that an input may be taken beyond the power supply rails, a series resistor MUST be fitted to limit the input current to less than 100µA. For optimum performance use a floating supply and connect IN LO and REF LO to COM. This will eliminate the common mode voltage and any small errors that may occur.

APPLICATIONS

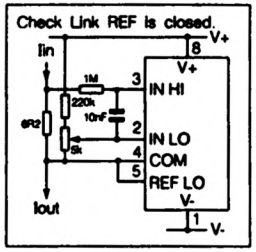
Do not connect more than one meter to the same power supply if the meters cannot use the same signal ground. Input filter should be as close as possible to the meter.



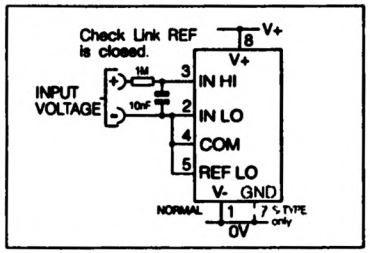
Driving battery annunciator with associated logic and low battery detection circuitry.



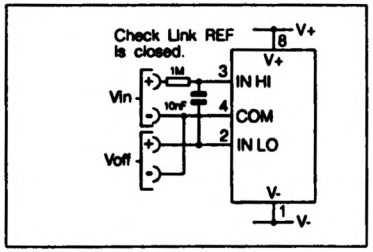
Measuring the ratio of two voltages. Reading = $1000V_1/V_2$
$50mV < V_2 < 200mV$.
$V_1 < 2V_2$.



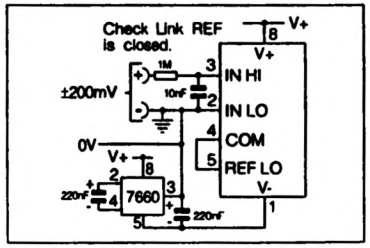
Measuring 4-20mA to read 0 - 999 (supply MUST be isolated).



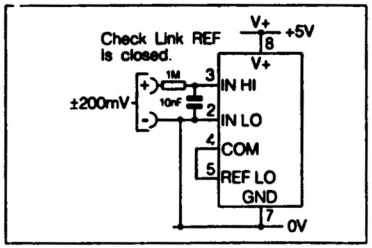
Measuring a floating voltage source of 200mV full scale. For DPM 3S leave V- (Pin 1) floating and connect 0V to GND (Pin 7).



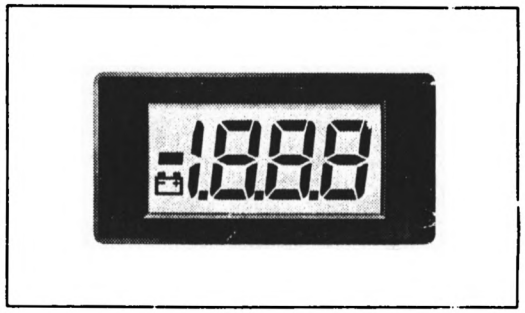
Zero display when applied input is not zero, the offset and input voltages should be applied as shown.



Measuring a single ended input referenced to supply (DPM 3).



Measuring a single ended input referenced to supply (DPM 3S).



- Ultra Compact
- 11mm Digits
- Ultra Low Power
- Snap-in Integral Bezel
- Single Rail Version (DPM 3S)

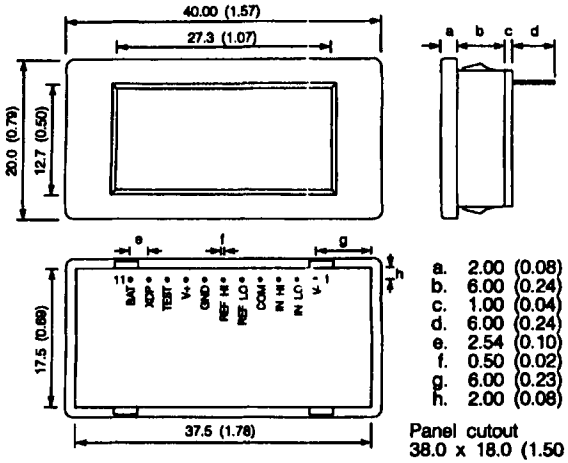
3½ Digit Subminiature LCD DPM 3

The DPM 3 uses advanced components and the latest miniaturisation techniques to produce a compact DPM module. Miniature size means the module can be integrated into the smallest of enclosures for local indication. Its low cost means it will suit high and low volume applications. The snap-in integral bezel makes mounting simple.

The DPM features auto-zero, auto-polarity, 200mV Full Scale Reading (F.S.R), 11mm digit height and programmable decimal points. Very low power consumption allows long battery life, making it useful in handheld equipment. For single rail use, the DPM 3S features a built in negative rail generator, enabling the meter to measure a signal referenced to its own power supply 0V.

SPECIFICATION		MIN.	TYP.	MAX.	UNIT
Accuracy (overall error)			0.1		% (±1 count)
Linearity				±1	count
Sample rate			3		per/sec
Temperature range		0		50	°C
Temperature stability	Normal		200		ppm/°C
	S-type		100		
Supply voltage	Normal (V+ to V-)	7	9	14	V
	S-type (V+ to GND)	3	5	7	
Supply current	Normal		150		µA
	S-type		250		
Maximum D.C. input voltage				±20	V
Input leakage current (Vin = 0V)			1	10	pA

DIMENSIONS All dimensions in mm (inches)



a. 2.00 (0.08)
b. 6.00 (0.24)
c. 1.00 (0.04)
d. 6.00 (0.24)
e. 2.54 (0.10)
f. 0.50 (0.02)
g. 6.00 (0.23)
h. 2.00 (0.08)

Panel cutout
38.0 x 18.0 (1.50 x 0.71)

Panel thickness
1.0 to 2.5 (0.04 to 0.1)

PIN FUNCTIONS

1. V-. DPM 3 - Negative power supply connection. DPM 3S - No connection.
2. IN LO. Negative measuring input.
3. IN HI. Positive measuring input.
4. COM. Ground for analogue section of A/D converter, it is actively held at 2.8V below V+ and must not be allowed to sink excessive current (>100μA) by, for instance, connecting to a higher voltage.
5. REF LO. Negative input for reference voltage.
6. REF HI. Positive input for reference voltage (connected via Link REF to internal reference).
7. GND. DPM 3 - No connection. DPM 3S 0V power supply connection.
8. V+. Positive power supply connection.
9. TEST. Connect to V+ to display segments "-1888". It should not be operated for more than a few seconds as the D.C. voltage applied to the LCD may "burn" the display. This pin is normally at 5V below V+ and is the ground for the digital section of the meter.
10. XDP. Annunciator Drive Waveform, this is an inversion of the LCD backplane signal.
11. BAT. (Pin not factory fitted.) Connecting this pin to XDP (pin 10) will turn the battery annunciator on (ensure Link BAT is open when driving annunciator). See Applications for low battery sensing circuit.

ON BOARD LINKS

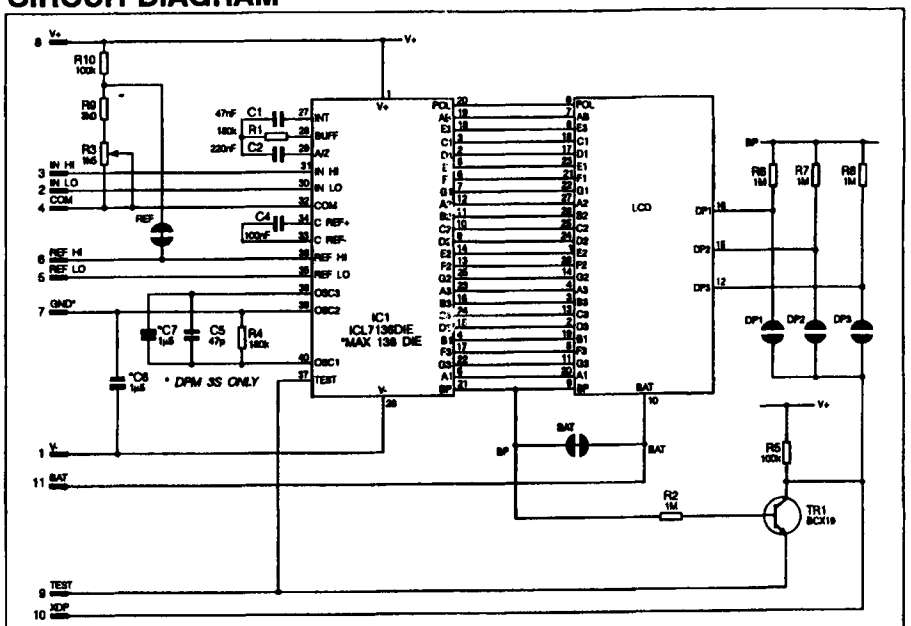
On board links can be made with a solder link to implement features.

DP1. Make to turn on DP1 (199.9).
DP2. Make to turn on DP2 (19.99).
DP3. Make to turn on DP3 (1.999).
REF. Factory made - Connects internal reference to REF HI. Should only be disconnected if using external reference.

PANEL FITTING

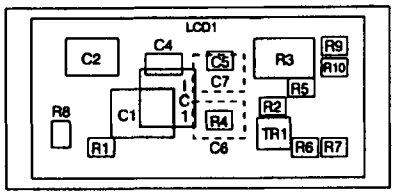
Locate the meter by passing it through the front of the panel cutout, (38.0mm x 18.0mm), gently pushing until the rear of the bezel is flush with the panel (DO NOT PUSH ON THE LCD). The snap-in lugs will now automatically hold the meter firmly in position.

CIRCUIT DIAGRAM



SOLDER PAD LINKS - Interconnections can be made by applying a solder link across the appropriate solder pad provided (see circuit diagram).

COMPONENT LAYOUT - FRONT VIEW



Component on underside of PCB.

S-type modules only.

SCALING

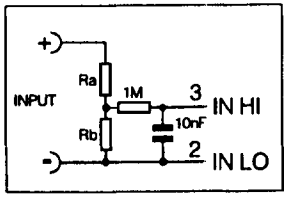
A potential divider may be used to alter the full scale reading of the meter - see table.

Note

The meter will have to be re-calibrated by adjusting the calibration pot R3 at the rear of the module.

*Input must not exceed ±250V.

If input is to exceed ±250V use Ra = 10M, Rb = 1k and ensure that Ra is rated for high voltage use.



REQUIRED F.S.R.	Ra	Rb
2V	910k	100k
20V	1M	10k
200V	1M	1k
2kV*	1M	100R
200μA	0R	1k
2mA	0R	100R
20mA	0R	10R
200mA	0R	1R

INTERNATIONAL SERIES DESCRIPTION

The INTERNATIONAL SERIES is a high reliability line of open-frame power supplies designed to operate from the wide range of AC power sources found worldwide.

This feature greatly simplifies your inventory and service considerations by allowing the use of one standard power supply regardless of destination.

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If you plan to distribute your products worldwide, obtaining necessary agency approvals can be greatly simplified by specifying POWER-ONE, INC. INTERNATIONAL SERIES.

Power-One
DC POWER SUPPLIES

INTERNATIONAL SERIES DC POWER SUPPLIES

DRAWING NO. 51281 REV. L

SPECIFICATIONS AND APPLICATION DATA

VOLTAGE/CURRENT RATING CHART

MODEL	+2V	+5V	+12V	+15V	+18-20V	+24V	+28V	-5V	-12V	-15V	-18-20V	-24V	CASE
SINGLE OUTPUT													
HA5-1.5/OVP-A		1.5											B
HA15-0.9-A			0.9 or 0.9										B
HA24-0.5-A						0.5 or 0.5							B
HB2-3-A	3.0												B
HB5-3/OVP-A		3.0											B
HB12-1.7-A			1.7										B
HB15-1.5-A				1.5									B
HB24-1.2-A						1.2							B
HB28-1-A							1.0						B
HC2-6-A	6.0												C
HC5-6/OVP-A		6.0											C
HC12-3.4-A			3.4										C
HC15-3-A				3.0									C
HC24-2.4-A						2.4							C
HC28-2-A							2.0						C
HD2-12-A	12.0												D
HD5-12/OVP-A		12.0											D
HD12-6.8-A			6.8										D
HD15-6-A				6.0									D
HD24-4.8-A						4.8							D
HD28-4-A							4.0						D
HE2-18-A	18.0												E
HE5-18/OVP-A		18.0											E
HE12-10.2-A			10.2										E
HE15-9-A				9.0									E
HE24-7.2-A						7.2							E
HE28-6-A							6.0						E
HN5-9/OVP-A		9.0											N
HN12-5.1-A			5.1										N
HN15-4.5-A				4.5									N
HN24-3.6-A						3.6							N
HN28-3-A							3.0						N
DUAL OUTPUTS													
HAA5-1.5/OVP-A		1.5						1.5					AA
HAA15-0.8-A			1.0 or 0.8					*0.4 or 1.0 or 0.8					AA
HAA24-0.6-A					0.4 or 0.6						0.4 or 0.6		AA
HAA512-A		2.0	▼0.5 or ▼0.5										AA
HAD12-0.4-A			0.4						0.4				B
HAD15-0.4-A				0.4						0.4			B
HBB5-3/OVP-A		3.0						3.0					BB
HBB15-1.5-A			1.7 or 1.5					*0.7 or 1.7 or 1.5					BB
HBB24-1.2-A					0.9 or 1.2						0.9	1.2	BB
HBB512-A		3.0	▼1.25 or ▼1.25										BB
HCC5-6/OVP-A		6.0						6.0					CC
HCC15-3-A	—		3.4 or 3.0						3.4 or 3.0				CC
HCC24-2.4-A					1.8 or 2.4						1.8 or 2.4		CC
HCC512-A		6.0	▼2.5 or ▼2.5										CC
HDD15-5-A			5.0 or 5.0						5.0 or 5.0				E
TRIPLE OUTPUTS													
HTAA-16W-A		2.0	0.4 or 0.4					*0.4 or ▼0.4 or ▼0.4					AA
HBAA-40W-A		3.0	1.0 or 0.8					*0.4 or 1.0 or 0.8					BAA
HCAA-60W-A		6.0	1.0 or 1.0					*0.4 or 1.0 or 1.0					D
HCBB-75W-A		6.0	1.7 or 1.5					*0.7 or 1.7 or 1.5					CBB
HDBB-105W-A		12.0	1.7 or 1.5					*0.7 or 1.7 or 1.5					DBB
CP131-A		8.0	1.7 or 1.5					*0.7 or 1.7 or 1.5					131

HIGH VOLTAGE

MODEL	+48V	+120V	+180V	+200V	+250V	CASE
HB48-0.5-A	0.5					B
HC48-1-A	1.0					C
HD48-3-A	3.0					D
HE48-4-A	4.0					E
HB120-0.2-A		0.2				B
HB200-0.12-A ø			0.12 or 0.12			B
HB250-0.1-A					0.1	B

* -12V(or -15V) requires jumper on PCB for -5V.
† for ±12V, refer to chassis silkscreen.
ø for 180V, refer to chassis silkscreen.
▼ 12V to 15V adjustable output
— indicates no remote sense.
Specifications subject to change without notice.

FEATURES

- VDE transformer construction
- ± .05% regulation.
- T.C. burned-in to MIL-883 Lev. B
- Chassis notched for AC input
- 100/120/220/230-240 VAC
- Industry standard size
- Full rated to 50°C
- Remote sense - most outputs
- UL recognized/CSA certified
- OVP on 5V outputs
- 2 hour burn-in period
- Foldback/current limit

SPECIFICATIONS

AC INPUT:	100/120/220/230-240 VAC+ +10% -13% 47-63Hz (Derate output current 10% for 50 Hz operation.) See AC connection table under APPLICATION NOTES for jumper information. Fuse information is next to outline and mounting drawings.
DC OUTPUT:	See Voltage/Current Rating Chart. Adjustment range ±5% minimum. (Voltage nonadjustable on HAD models.)
LINE REGULATION:	± .05% for a 10% line change. (±1% for HAD models.)
LOAD REGULATION:	± .05% for a 50% load change (±1% for HAD models.)
OUTPUT RIPPLE:	2V to 15V outputs: 5.0mV Pk-Pk maximum 24V to 250V outputs: 3.0mV+.02%Vout Pk-Pk maximum (HAD models: 0.1%Vout Pk-Pk maximum.)
TRANSIENT RESPONSE:	≤50us for a 50 to 100% load change
SHORT CIRCUIT AND OVERLOAD PROTECTION:	Automatic current limit/foldback.
OVERVOLTAGE PROTECTION:	Built-in on all 5V outputs. Set at 6.2VDC ±0.4V. Other outputs may use optional overvoltage protection.
REMOTE SENSING:	Provided on most models. Open sense lead protection built-in.
STABILITY:	±0.3% for 24 hour period after 1 hour warm-up
TEMPERATURE RATING:	0°C to 50°C full-rated, derated linearly to 40% at 70°C. 12 CFM forced air cooling required to meet IEC 380/950 above 80% of total rated output power.
TEMPERATURE COEFFICIENT:	± .03%/°C maximum
EFFICIENCY: (typical)	2V to 5V outputs: 45% 12V and 15V outputs: 55% 24V through 28V & 48V through 250V outputs: 60%
VIBRATION:	Per MIL-STD-810D, Method 514.3, Category 1, Procedure I
SHOCK:	Per MIL-STD-810D, Method 516.3, Procedure III

* Tolerance for 230VAC operation is +15% -10%.
Note: Specifications subject to change without notice.

WARRANTY

POWER-ONE, INC. warrants each power supply of its manufacture that does not perform to published specifications, as a result of defective materials or workmanship, for a period of two (2) full years from the date of original delivery.

POWER-ONE, INC. assumes no liabilities for the consequential damages of any kind through the use or misuse of its products by the purchaser or others. No other obligations or liabilities are expressed or implied.

PRODUCTS RETURNED FOR REPAIR

Please follow this procedure when returning products for servicing.

1. Contact Power-One's Customer Service Department for authorization to return products.

   POWER-ONE, INC.
   740 Calle Plano
   Camarillo, CA 93012
   USA

   PHONE: (805) 987-8741
   (800) 678-9445
   FAX: (805) 388-0476
   TWX: 910-336-1297

2. A Returned Material Authorization (RMA) will be issued and must appear on all shipping documents and containers.

3. Products must be returned freight pre-paid. Products returned freight collect or without an RMA number will be rejected and returned freight collect.

APPLICATION NOTES:

REMOTE SENSE

Remote sense terminals may be used to compensate for output line losses and provide for a remote point of regulation. Figure 1 shows the proper termination for a power supply with remote sensing.

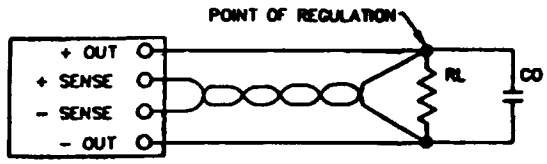


FIGURE 1

Load lines must be sized to prevent an excessive voltage drop from the output to the load. Since the point of regulation is at the load, the power supply must compensate for line losses. Excessive load line losses may affect current limiting, AC line dropout point and OVP margin (if applicable).

Leads should be sized to drop no more than 0.5V – the less the better. Use of a twisted pair or shielded pair for the sense lines is recommended for noise immunity. In problem applications, the use of a small AC decoupling capacitor (.1 to 10uF) across the sense terminals is highly recommended. In some applications there may be a tendency for the power supply to oscillate due to additional phase shift caused by the series resistance and inductance in the load leads. The addition of capacitor Co will reduce output impedance and provide stability. The recommended value of Co is 100uF per ampere of 50uF per foot and can be the sum of the distributed decoupling capacitors found in most systems.

All Power-One supplies have open sense lead protection to protect the load from an overvoltage condition if the sense leads are removed. There is no need to strap the sense terminals to the output terminals in the local sense mode.

OVERVOLTAGE PROTECTION (OVP)

An overvoltage protection circuit, commonly refered to as a crowbar, is used to prevent damage to voltage sensitive loads such as TTL logic. Trip point of the OVP is usually set at 115% – 135% of the output voltage. The OVP will short the output terminals upon sensing a fault condition. The primary fuse of the supply will blow if the supply is not foldback current limited. Nuisance tripping of the OVP is a common problem. Noise from input line spikes or load noise can cause an OVP to fire. The INTERNATIONAL SERIES has OVP noise filtering to prevent nuisance tripping and reduce transformer interwinding capacitance to minimize input line susceptibility.

COMMON-MODE LATCH UP

In certain instances dual power supplies can exhibit a problem known as common-mode latch up. This occurs when the positive supply comes up first and forces a reverse bias condition on the negative supply. The negative supply latches up in a current limit condition. Power-One has incorporated a unique anti-latch circuit into every dual power supply in the INTERNATIONAL SERIES which will minimize this problem.

EMI/RFI

These linear power supplies have inherently low conducted and radiated noise levels. For most system applications they will meet the requirements of FCC Docket 20780 for Class A equipment and VDE 0871 for Class A equipment without additional noise filtering.
For special applications consult factory.

COOLING

Convection cooling is adequate where non-restricted air flow is available. When operating in a confined area, moving air or conduction cooling is recommended.

SAFETY SPECIFICATIONS

The INTERNATIONAL SERIES power supplies were designed to meet or exceed requirements for the following specifications: IEC 380, IEC 435, VDE 0730 Part 2, VDE 0804, ECMA-57, CEE 10 Part 2P, UL 1012, CSA 22.2 No. 143, CSA 22.2 No. 154. Specifically field terminal to terminal spacing is 5.25 mm with 9.0 mm creepage to other metal, leakage current is less than 5.0uA and dielectric withstanding voltages are 3750 VAC input to chassis, 3750 VAC input to output and 300 VDC output to chassis.

GROUNDING

Grounding considerations in designing a power distribution system are often overlooked but can have a significant impact on overall system performance. A single point system ground should be employed where possible to eliminate ground loops and improve regulation.

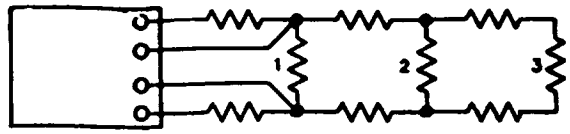


FIGURE 2

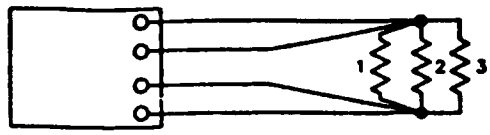


FIGURE 3

Figure 2 shows a simple but undesirable connection scheme. Regulation at loads 2 and 3 becomes progressively worse due to voltage drops in the finite wire resistance between loads. Figure 3 shows an improved connection system in which regulation is maintained at all three loads because wire losses are not cumulative.

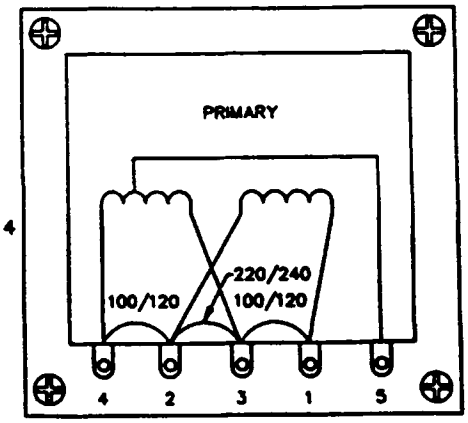
AC INPUT CONSIDERATIONS

Almost all power supplies use a capacitive input filter that draws current only at the peaks of the AC input voltage. The peak to RMS ratio can be very high, typically 3 to 1. When a supply is turned on, the input capacitor has a very low impedance and draws an initially high surge current until it charges to its nominal voltage. The input surge current can be as high as 20 times the rated input current and lasts for several cycles of the AC input.

AC CONNECTION AND FUSING*

The five wire input to the INTERNATIONAL SERIES provides four voltage ranges: 100/120/220/230–240** +10%, –13%. See chassis AC connection table (Figure 4) for the jumpering requirements. For convenience the jumper sequence from the Hi-Vol series is retained. Extended low line tolerance provides additional drop out margin in areas where line voltages are marginal. Inputs must be fused.

FIGURE 4

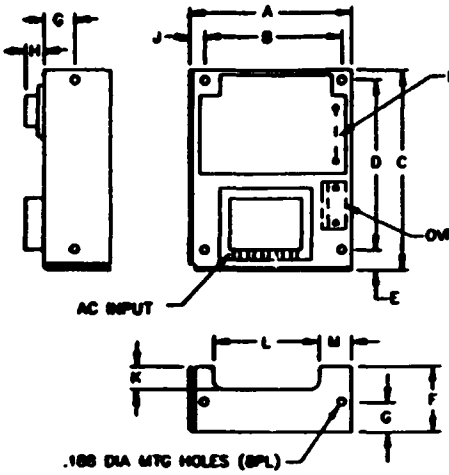


AC INPUT, 47–63 HZ				
FOR USE AT	100 VAC	120 VAC	220 VAC	230/240 VAC
JUMPER	1&3 2&4	1&3 2&4	2&3	2&3
APPLY AC	1&5	4&1	1&5	4&1

NOTE: This product is a Class 1 power supply and requires the chassis to be connected to earth ground at end application.
*NOTE: Use 700°C iron for soldering input connections. Varnish acts as flux and is solder strippable.
**NOTE: Tolerance for 230VAC operation is +15%, –10%.

OUTLINE AND MOUNTING DRAWINGS

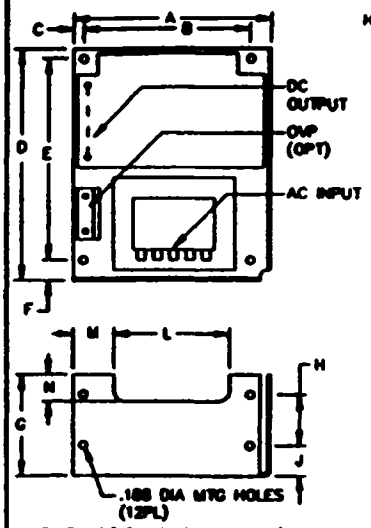
B CASE
WT. 2 LBS.



	INCH	mm.
A	4.00	101.60
B	3.375	85.73
C	4.87	123.70
D	4.125	104.78
E	0.50	12.70
F	1.62	41.15
G	0.75	19.05
H	0.450	11.43
J	0.38	9.65
K	0.57	14.48
L	0.260	66.04
M	0.794	20.17

FUSE AT: 0.5/0.25 AMPS FOR 100-120/220-240 VAC

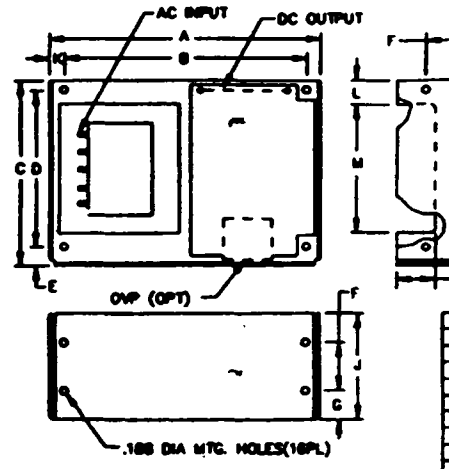
C CASE
WT. 4 LBS.



	INCH	mm.
A	4.87	123.70
B	4.125	104.78
C	0.25	6.35
D	5.62	142.75
E	4.875	123.83
F	0.50	12.70
G	2.50	63.50
H	1.250	31.75
J	0.75	19.05
K	0.450	11.43
L	2.85	72.39
M	1.025	26.04
N	0.665	16.89

FUSE AT: 1.0/0.5 AMPS FOR 100-120/220-240VAC

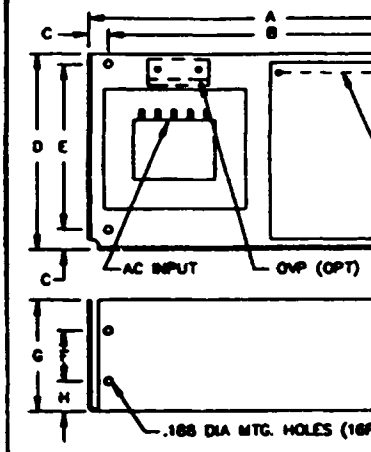
N CASE
WT. 6 LBS.



	INCH	mm.
A	7.00	177.80
B	6.250	158.75
C	4.87	123.70
D	4.125	104.78
E	0.50	12.70
F	1.250	31.75
G	0.75	19.05
H	0.525	13.34
J	2.75	69.85
K	0.38	9.65
L	0.640	16.26
M	3.35	85.09
N	1.00	25.40

FUSE AT: 2.0/1.0 AMPS FOR 100-120/220-240 VAC

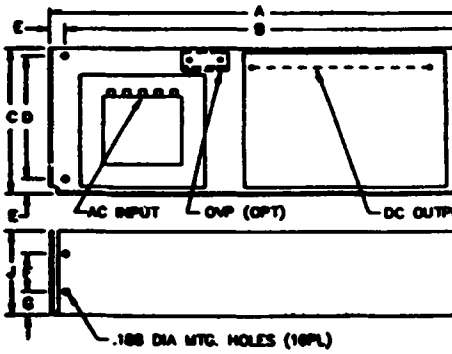
D CASE
WT. 7.5 LBS.



	INCH	mm.
A	9.00	228.60
B	8.000	203.20
C	0.50	12.70
D	4.87	123.70
E	4.125	104.78
F	1.250	31.75
G	2.75	69.85
H	0.75	19.05
J	0.525	13.34

FUSE AT: 2.0/1.0 AMPS FOR 100-120/220-240 VAC

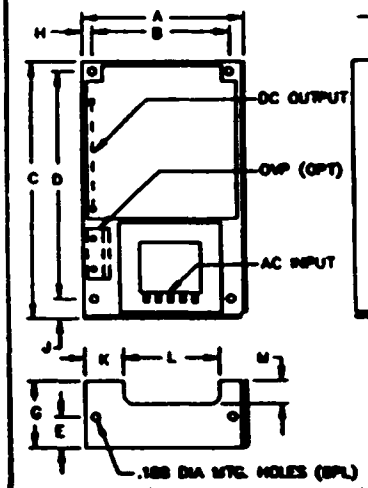
E CASE
WT. 10 LBS.



	INCH	mm.
A	14.00	355.60
B	13.000	330.20
C	4.87	123.70
D	4.125	104.78
E	0.50	12.70
F	1.250	31.75
G	0.75	19.05
H	0.650	16.51
J	2.75	69.85

FUSE AT: 3.0/1.5 AMPS FOR 100-120/220-240 VAC

AA CASE
WT. 2 LBS.

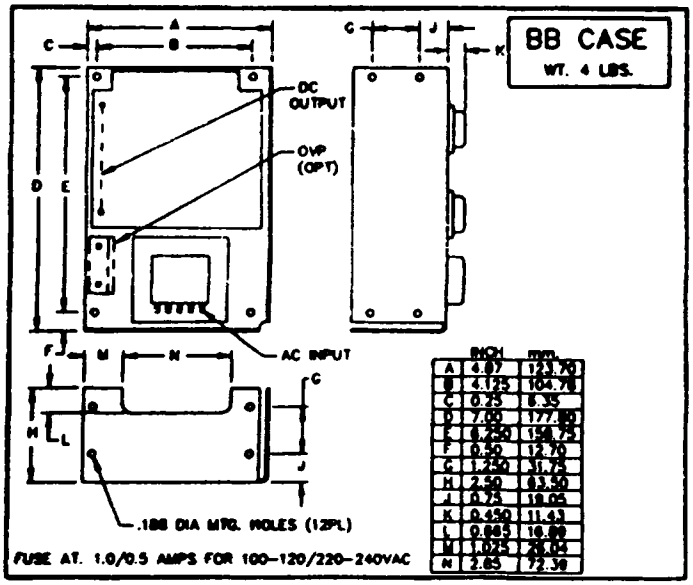


	INCH	mm.
A	4.00	101.60
B	3.375	85.73
C	6.50	165.10
D	5.750	146.05
E	0.75	19.05
F	0.450	11.43
G	1.62	41.15
H	0.25	6.35
J	0.50	12.70
K	0.945	24.26
L	2.37	60.20
M	0.57	14.48

FUSE AT: 0.5/0.25 AMPS FOR 100-120/220-240 VAC
MTAA: 0.75/0.375 AMPS FOR 100-120/220-240 VAC

OUTLINE AND MOUNTING DRAWINGS

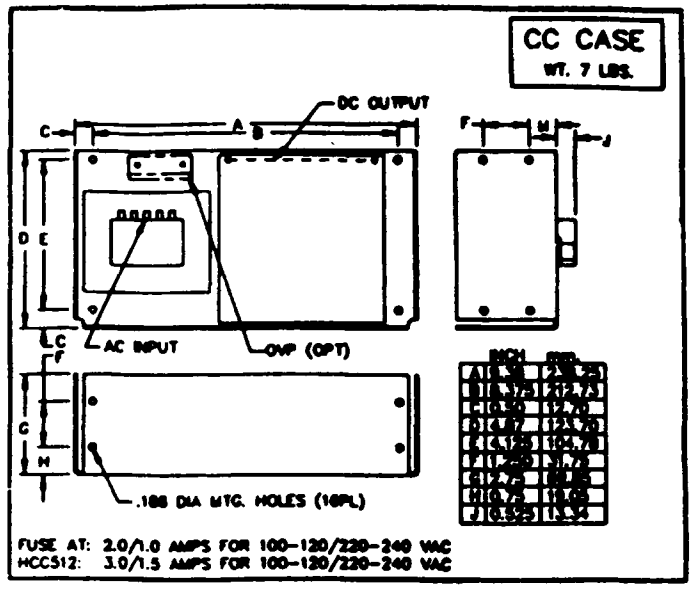
BB CASE
WT. 4 LBS.



	INCH	mm
A	4.87	123.70
B	4.125	104.78
C	0.25	6.35
D	7.00	177.80
E	6.250	158.75
F	0.50	12.70
G	1.250	31.75
H	2.50	63.50
J	0.75	19.05
K	0.450	11.43
L	0.625	15.88
M	1.025	26.04
N	2.85	72.39

FUSE AT. 1.0/0.5 AMPS FOR 100–120/220–240VAC

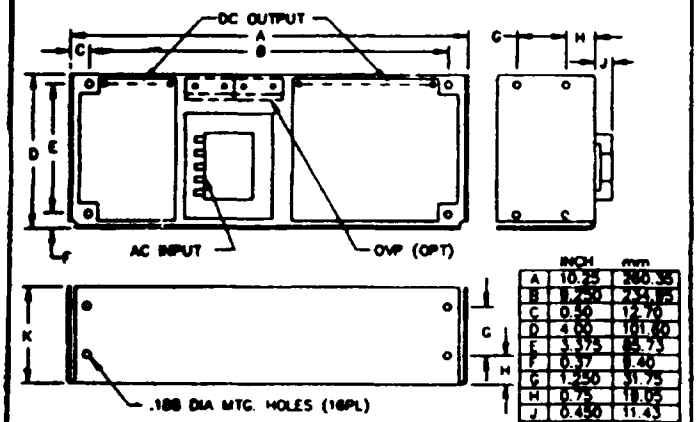
CC CASE
WT. 7 LBS.



	INCH	mm
A	9.25	235.00
B	7.375	187.33
C	0.50	12.70
D	4.87	123.70
E	4.125	104.78
F	1.250	31.75
G	2.50	63.50
H	0.75	19.05
J	0.525	13.34

FUSE AT: 2.0/1.0 AMPS FOR 100–120/220–240 VAC
HCC512: 3.0/1.5 AMPS FOR 100–120/220–240 VAC

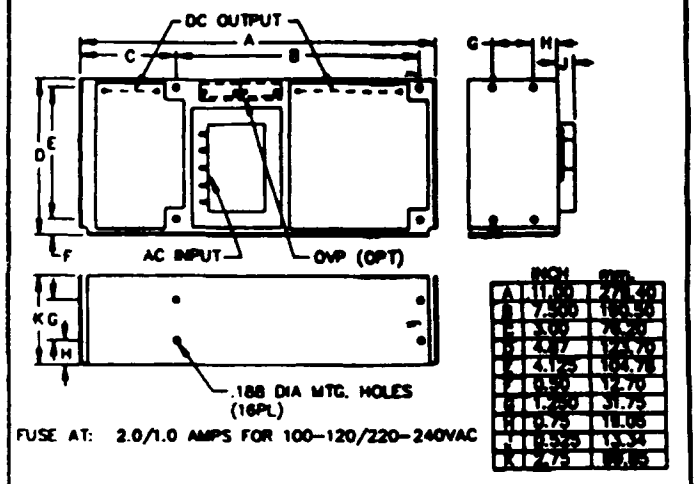
BAA CASE
WT. 5 LBS.



	INCH	mm
A	10.25	260.35
B	9.250	234.95
C	0.50	12.70
D	4.00	101.60
E	3.375	85.73
F	0.37	9.40
G	1.250	31.75
H	0.75	19.05
J	0.450	11.43
K	2.50	63.50

FUSE AT: 1.0/0.5 AMPS FOR 100–120/220–240 VAC

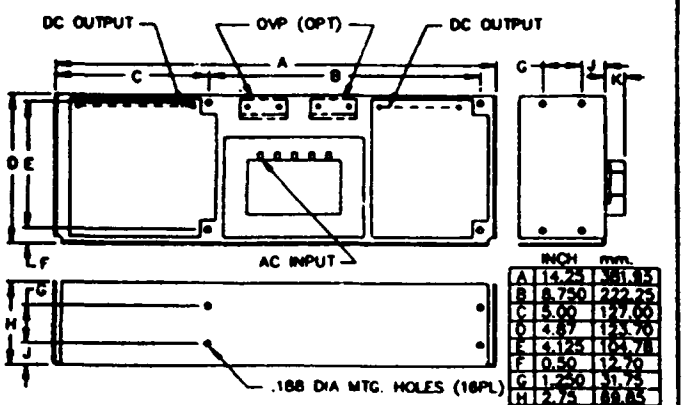
CBB CASE
WT. 8 LBS.



	INCH	mm
A	11.00	279.40
B	7.500	190.50
C	3.00	76.20
D	4.87	123.70
E	4.125	104.78
F	0.50	12.70
G	1.250	31.75
H	0.75	19.05
J	0.525	13.34
K	2.75	69.85

FUSE AT: 2.0/1.0 AMPS FOR 100–120/220–240VAC

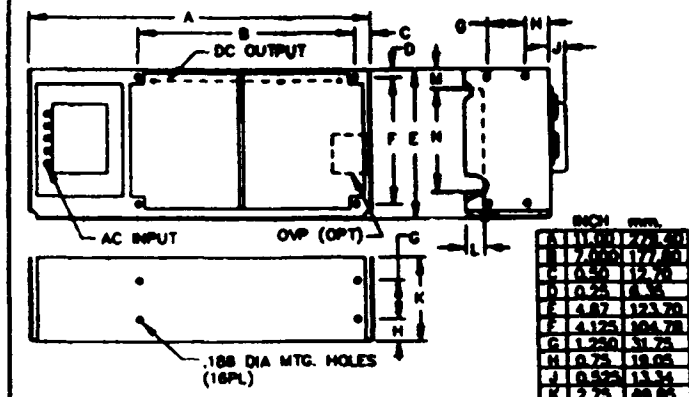
DBB CASE
WT. 11 LBS.



	INCH	mm
A	14.25	361.83
B	8.750	222.25
C	5.00	127.00
D	4.87	123.70
E	4.125	104.78
F	0.50	12.70
G	1.250	31.75
H	2.75	69.85
J	0.75	19.05
K	0.625	15.88

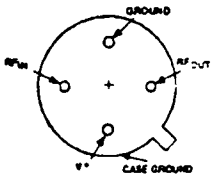
FUSE AT: 3.0/1.5 AMPS FOR 100–120/220–240 VAC

131 CASE
WT. 9 LBS.



	INCH	mm
A	11.00	279.40
B	7.000	177.80
C	0.50	12.70
D	0.25	6.35
E	4.87	123.70
F	4.125	104.78
G	1.250	31.75
H	0.75	19.05
J	0.525	13.34
K	2.75	69.85
L	0.600	15.24
M	0.640	16.26
N	3.35	85.09

FUSE AT: 3.0/1.5 AMPS FOR 100–120/220–240 VAC



TO-12, p 609

GPD SERIES LOW COST AMPLIFIERS, TO-12 PACKAGE

Guaranteed Specifications at 0° to 50°C Case Temperature

Model	Frequency Response (MHz) Minimum	Gain (dB) Minimum	Gain[2] (dB) Minimim	Noise Figure (dB) Typical	Power Output for 1 dB Gain Compression (dBm) Typical	Gain Flatness (±dB) Typical	3rd-Order Intercept Point (dBm) Typical	Input Power (±1% Reg.) Voltage (VDC)	Current (mA) Typical	Page Number
GPD-201	5-200	30	26	3 0	+5	1 0	+13	+15	30	254
GPD-202	5-200	25	23	5 5	+11	1 0	+18	+15	60	254
GPM-552	5-500	33	32	4 5	0	0 2	+14	+15	34	264
GPM-1052	5-1000	20	20	7 0	+8	0 3	+20	+15	60	268
GPD-251	5-200	25	23	4 0	+1	1 0	+10	+5	30	256
GPD-252	5-200	15	14	4.0	0	1 0	+12	+5	11	257
GPD-401/-461[1]	5-200	13	12	4 0	−2	1 0	+9	+15	10	258
GPD-411	5-400	12	11	3 0	−6	1.0	+4	+15	7	263
GPD-402/-462[1]	5-400	13	12	8 0	+8	1.0	+18	+15	24	259
GPD-403/-463[1]	5-400	9	8	7 5	+16	1 0	+25	+24	65	260
GPD-404/-464[1]	5-400	9	8	7 5	+17	1.0	+26	+15	70	261
GPD-405	10-400	13	12	5 0	+24	1 0	+36	+15	90	262
GPD-1001/-1061[1]	5-1000	12	11	6 0	0	1 0	+12	+15	15	265
GPD-1002/-1062[1]	5-1000	12	11	7 0	+6	1 0	+16	+15	27	266
GPD-1003/-1063[1]	5-1000	10	9	7 0	+14	1 0	+25	+15	55	267

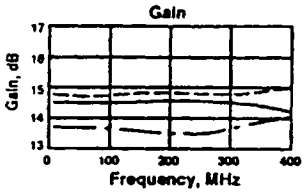
NOTES. 1. The 60 Series is the same as the standard series except that three external capacitors are required to establish low frequency roll-off
2. Military temperature conditions −55° to +85°C

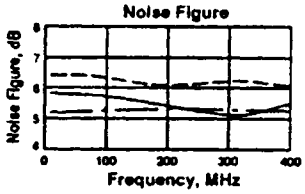
MAXIMUM RATINGS AND THERMAL CHARACTERISTICS TABLE

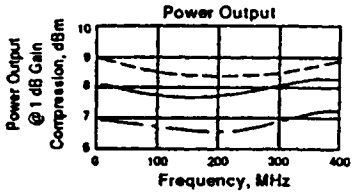
	Maximum Ratings					Thermal Characteristics[1]				
Model	DC Voltage (Volts)	Continuous RF Input Power (dBm)	Operating Case Temperature (°C)	Storage Temperature (°C)	"R" Series Burn-in Temperature (°C)	θ_{JC} (°C/W)	Active Transistor Power Dissipation (mW)	Junction Temperature Above Case Temperature (°C)	MTBF MIL-HDBK-217E, A_{UF} @ 90°C (Hrs)	Weight (Grams)
GPD-201	+17	+13	-55 to +125	-62 to +150	+125	105	33	3	1,678,671	1.5
GPD-202	+17	+13	-55 to +125	-62 to +150	+125	105	117	12	1,621,478	1.5
GPD-251	+12	+13	-55 to +125	-62 to +150	+125	105/105	23/43	2/5	1,678,323	1.5
GPD-252	+12	+13	-55 to +125	-62 to +150	+125	105	20	2	2,000,740	1.5
GPD-401/461	+17	+13	-55 to +125	-62 to +150	+125	90	14	2	2,045,316 (401) 2,388,527 (461)	1.5
GPD-402/-462	+17	+13	-55 to +125	-62 to +150	+125	90	82	7	2,325,901 (402) 2,640,329 (462)	1.5
GPD-403/-463	+25	+13	-55 to +125	-62 to +150	+125	85	275	23	3,058,127 (403) 3,602,215 (463)	1.5
GPD-404/-464	+17	+13	-55 to +115	-62 to +150	+115	85	330	28	2,435,672 (404) 2,512,908 (464)	1.5
GPD-405	+17	+13	-55 to +100	-62 to +150	+100	55	750	41	1,607,022	1.5
GPD-411	+17	+13	-55 to +125	-62 to +150	+125	105[2]	24[2]	3[2]	1,608,303	1.5
GPM-552	+17	+17	-55 to +100	-62 to +100	+100	135/135	85/85	12/12	—	1.5
GPD-1001/-1061	+17	+13	-55 to +125	-62 to +150	+125	105	37	4	1,639,228 (1001) 1,910,397 (1061)	1.5
GPD-1002/-1062	+17	+13	-55 to +125	-62 to +150	+125	105	81 6	9	1,639,228 (1002) 1,882,476 (1062)	1.5
GPD-1003/-1063	+17	+13	-55 to +125	-62 to +150	+125	75	185	14	869,341 (1003) 2,101,101 (1063)	1.5
GPM-1052	+17	+17	-55 to +71	-62 to +71	+71	130/130	125/175	16/23	—	1.5

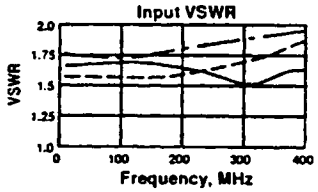
NOTES 1 Values refer to 1st and 2nd stage transistors respectively.
2. For further information, see High Reliability section.

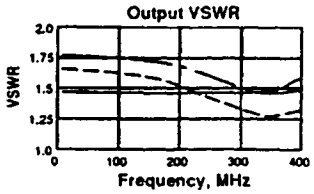
TYPICAL PERFORMANCE OVER TEMPERATURE (@ +15 VDC unless otherwise noted)



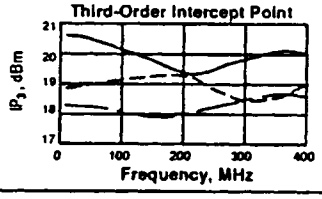


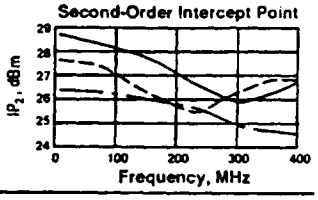






KEY: +25°C ———
+85°C – – – –
-55°C —·—





AUTOMATIC NETWORK ANALYZER MEASUREMENTS (Typical production unit @ +25°C ambient)

NUMERICAL READINGS

BIAS = 15.00 VOLTS

FREQ MHz	VSWR IN	GAIN dB	PHASE DEG	PHASE DEV	GPDEL ns	VSWR OUT	ISOL dB
100.0	1.63	14.33	174.29	.02	.00	1.45	23.70
150.0	1.60	14.23	170.90	.05	.18	1.46	23.27
200.0	1.56	14.24	167.76	.33	.20	1.45	22.92
250.0	1.53	14.17	163.59	-.40	.20	1.45	22.76
300.0	1.53	14.23	160.48	-.11	.19	1.45	22.49
350.0	1.55	14.22	156.84	-.32	.18	1.47	22.00
400.0	1.58	14.09	154.18	.43	.17	1.51	21.79
450.0	1.68	14.11	150.88		.21	1.54	21.28
500.0	1.83	13.97	146.56		.21	1.61	21.01
550.0	2.06	13.81	143.23		.22	1.70	20.54
600.0	2.33	13.76	138.65		.26	1.82	20.37
650.0	2.67	13.38	133.97		.24	1.97	20.05
700.0	3.08	13.05	130.10		.22	2.15	19.79
750.0	3.60	12.74	126.17		.24	2.35	19.62
800.0	4.17	12.36	121.50		.22	2.58	19.88

S-PARAMETERS, MAGNITUDES AND ANGLES

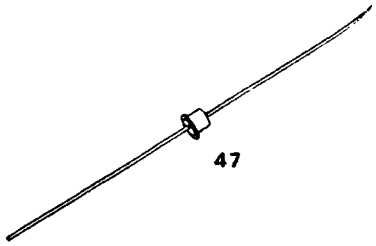
BIAS = 15.00 VOLTS

FREQ	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	Mag	Ang	dB	Ang	dB	Ang	Mag	Ang
100.00	.235	-179.6	14.333	174.0	-23.399	15.6	.183	3.2
150.00	.230	-178.7	14.267	170.8	-23.288	23.6	.181	8.7
200.00	.221	-177.6	14.297	167.9	-23.158	28.4	.183	11.3
250.00	.209	-173.3	14.225	163.6	-22.753	36.3	.181	14.4
300.00	.207	-168.0	14.267	160.7	-22.286	42.9	.185	18.2
350.00	.212	-160.8	14.253	156.9	-22.099	49.7	.187	24.2
400.00	.228	-154.2	14.179	154.0	-21.392	55.4	.196	29.4
450.00	.258	-148.9	14.178	150.5	-21.186	58.8	.209	34.4
500.00	.298	-146.4	13.985	146.4	-20.985	64.6	.231	38.2
550.00	.346	-145.8	13.839	142.9	-20.484	67.1	.259	41.0
600.00	.400	-147.2	13.746	138.4	-20.250	71.3	.292	41.7
650.00	.457	-150.1	13.382	133.7	-20.036	75.1	.329	41.1
700.00	.512	-154.7	13.047	130.0	-19.837	77.9	.366	39.4
750.00	.569	-159.7	12.735	126.1	-19.672	79.9	.406	36.7
800.00	.617	-164.5	12.341	121.4	-19.820	81.9	.441	32.8

Avantek, Inc. • 481 Cottonwood Drive, Milpitas, CA 95035 • General Office (408) 432-3080 • Component Sales (408) 943-4296 • TWX 910-338-2206 • FAX (408) 432-3243

Germanium Diodes

BD1-7

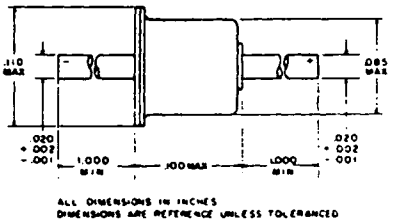


The General Electric types 4JFBD1-7 are germanium back diodes which make use of the quantum mechanical tunneling phenomenon, thereby attaining a very low forward voltage drop and eliminating charge storage effects. They feature closely controlled forward voltage characteristics with very small temperature coefficients. The very low forward voltage and low capacity of the back diode make it ideal for use in high frequency applications and in transistor and tunnel diode switching circuits. The germanium back diodes are characterized in seven types according to the forward current at a forward voltage of 90 millivolts and according to the maximum reverse leakage current.

absolute maximum ratings: (25°C) (unless otherwise specified)

Part Number	1	2	3	4	5	6	7	units
Forward Current (-55 to + 100°C)	30	15	10	5	5	5	5	ma
Reverse Current (-55 to + 100°C)	10	5	5	5	5	5	5	ma
Lead Temperature, from case for 10 seconds	1/16" + 1/32" 260°C							

AXIAL DIODE OUTLINE



electrical characteristics: (25°C) (unless otherwise specified)

	Sym.	BD1	BD2	BD3	BD4	BD5	BD6	BD7	Units
Forward Voltage, V_{F1} =90 MV ± 10 mv at I_{F1} =		10	5	2	1	.5	.2	.1 ma	
Forward Voltage at I_{F2} ($I_{F2} = 3I_{F1}$)	V_{F2}	120	130	170	170	170	160	160 mv	typ.
Reverse Voltage, $I_R = I_p$ max	V_{R1}	440	420	400	380	350	330	330 mv	min.
Reverse Voltage, I_R =1 ma	V_{R2}	440	465	465	465	465	465	465 mv	min.
Reverse Peak Point Current	I_P	1	.5	.2	.1	.05	.02	.01 ma	max.
Series Inductance (Measured at case)	L_S	1.5	1.5	1.5	1.5	1.5	1.5	1.5 nh	typ.
Total Terminal Capacity	C	8	6	4	3	3	3	3 pf	typ.
(V_R =350 mv)		20	10	10	10	10	10	10 pf	max.
Recovery Time*	t_r	1.0	0.7	0.5	0.4	0.4	0.4	0.4 ns	typ.

*The recovery time is measured to a reverse current of 1 ma. when switching from 0.1 volt forward to 0.4 volt reverse from a 50 ohm source. Since the back diode does not exhibit charge storage, the recovery time is determined by the charging time of the total device capacity.

AVX

How to Order

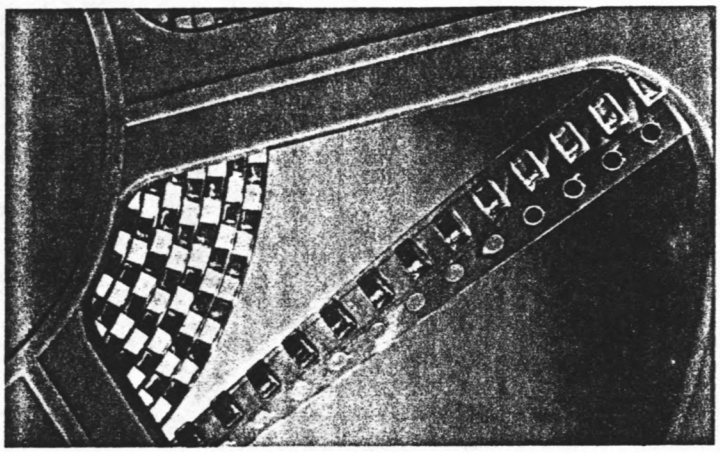
Part Number Explanation

EXAMPLE: 08051A101JATMA

0805	1	A	101	J	A	T	M	A
Size (L" x W")	**Voltage**	**Dielectric**	**Capacitance Code**	**Capacitance Tolerance**	**Failure Rate**	**Terminations**	**Marking Packaging**	**Special Code**
0504	16V = Y	NPO = A	(2 significant digits + no. of zeros)**	C = ±.25 pF‡	A = Not Applicable	NiGuard®	M = 7" Reel Embossed Tape/Marked	A = Standard
0603	25V = 3	X7R = C	Examples:	D = ±.50 pF‡		Standard:	N = 7" Reel Paper Tape/Marked	T = .026" Max. Thk
0805	50V = 5	Z5U = E	10 pF = 100	F = ±1%		T = Plated Ni and Solder	R = 13" Reel Embossed Tape/Marked	S = .022" Max. Thk
0508	100V = 1	Y5V = G	100 pF = 101	G = ±2%		Specials:	S = 13" Reel Paper Tape/Marked	R = .018" Max. Thk
1005	200V = 2	Special = T	1,000 pF = 102	J = ±5%		7 = Plated Ni Gold Plated	1 = 7" Reel Embossed Tape/Unmarked	P = .015" Max. Thk
0907	500V = 7		22,000 pF = 223	K = ±10%		Pd/Ag	2 = 7" Reel Paper Tape/Unmarked	
0612	600V = C		220,000 pF = 224	M = ±20%		Standard:	3 = 13" Reel Embossed Tape/Unmarked	
1206	1000V = A		1 μF = 105	Z = [+80, -20]%		1 = Pd/Ag	4 = 13" Reel Paper Tape/Unmarked	
1505	1500V = S			P = +100%, -0%		Others	B = Bulk/Marked	
1210	2000V = G					Consult AVX	9 = Bulk/Unmarked	
1510	2500V = W							
1805	3000V = H							
1808	4000V = J							
1812	5000V = K							
1825								
2321								
2225								
3640								

‡ C&D tolerances from 1.0 pF to 9.1 pF
** For values below 10 pfd, use "R" in place of decimal point, e.g., 9.1 pfd = 9R1.

NPO Dielectric
General Specifications



NPO (C0G) chip components meet long term capacitance stability characteristics of critical applications.

For special designs, consult AVX/Kyocera.

NPO is the most popular formulation of the "temperature-compensating," EIA Class I ceramic materials. Modern NPO formulations contain neodymium, samarium and other rare earth oxides and have dielectric constants between 30 and 80.

NPO ceramics offer one of the most stable capacitor dielectrics available. Capacitance change with temperature is 0 ±30ppm/°C which offers considerably less change at ±0.3% Δ C from -55°C to +125°C than other types of dielectrics at ±2%. Capacitance drift or hysteresis for NPO ceramics is negligible at less than ±0.05% versus up to ±2% for films. Typical capacitance change with life is less than ±0.1% for NPOs, one-fifth that shown by most other dielectrics. NPO formulations show no aging characteristics.

The NPO formulation usually has "Qs" in excess of 1000 and show little capacitance or "Q" changes with frequency. Their dielectric absorption is typically less than 0.6% which is similar to mica and most films.

Capacitance Range
0.5 pF to .027 μF (1.0 Vrms, 1kHz, for ≦ 100 pF use 1 MHz)

Capacitance Tolerances
±.25 pF, ±.5 pF, ±1%, ±2%, ±5%, ±10%, ±20%
For values less than 10 pF, tightest tolerance available is ±0.25 pF ("C").

Operating Temperature Range
-55°C to +125°C

Temperature Characteristic
0 ± 30 ppm/°C

Voltage Ratings
200, 100 & 50 VDC (+125°C)

Dissipation Factor
0.1% max. (+25°C and +125°C); 1.0 Vrms, 1 MHz for values ≦ 100 pF, and 1kHz for values > 100 pF

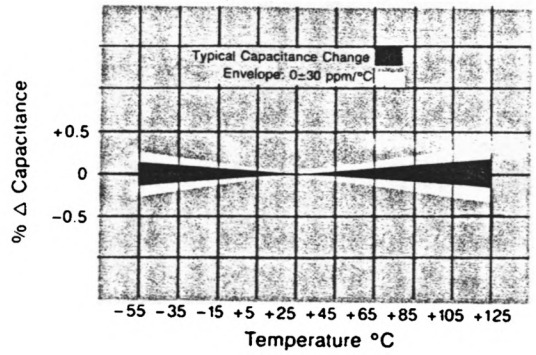
Insulation Resistance (+25°C, RVDC)
100,000 megohms min. or 1000 ohm-Farads min., whichever is less

Insulation Resistance (+125°C, RVDC)
10,000 megohms min. or 100 ohm-Farads min., whichever is less

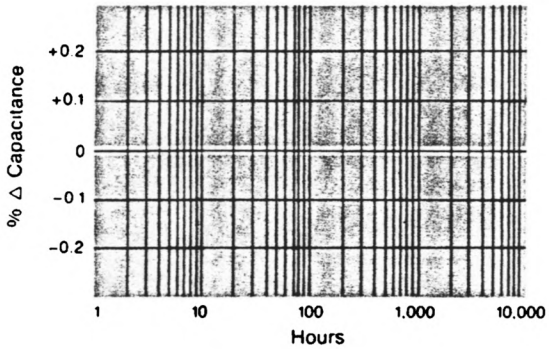
Dielectric Strength
250% of rated voltage

NPO Dielectric
Typical Characteristic Curves

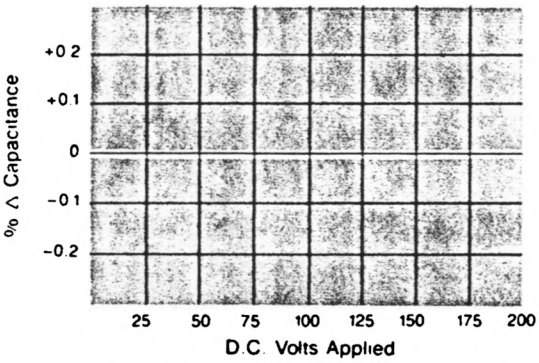
Temperature Coefficient



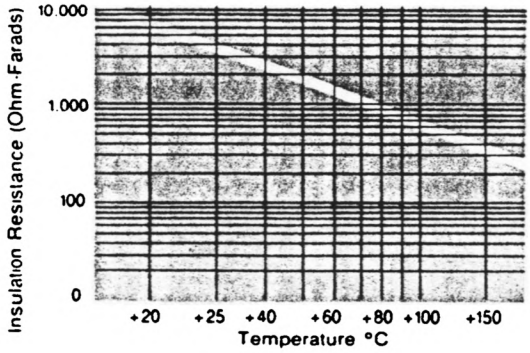
Aging Rate



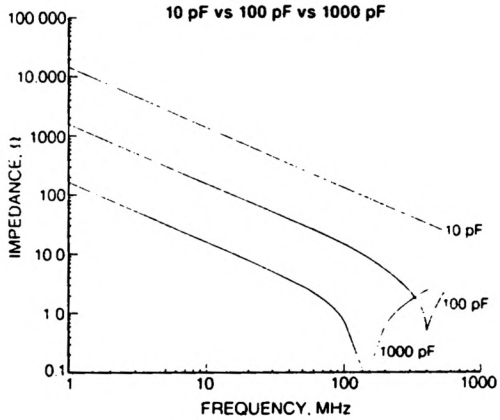
Voltage Coefficient



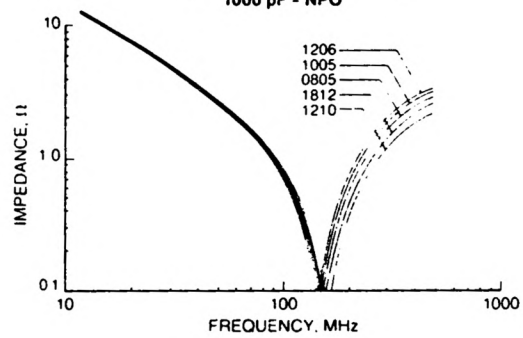
Insulation Resistance vs. Temperature



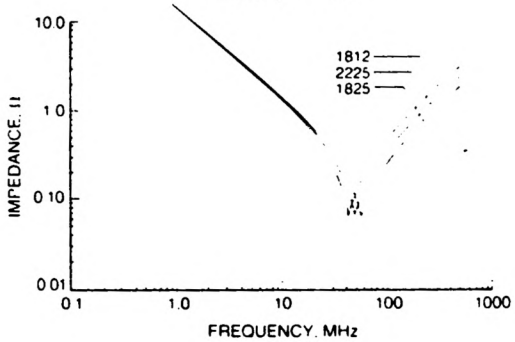
Impedance vs Frequency
0805 - NPO
10 pF vs 100 pF vs 1000 pF



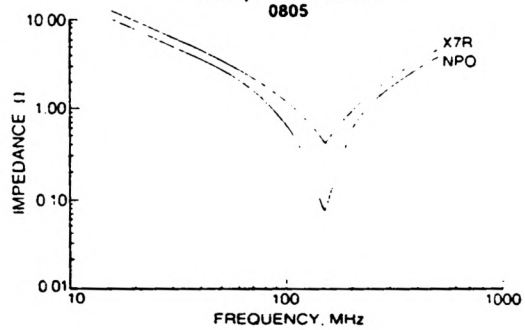
Impedance vs Frequency
1000 pF - NPO



Impedance vs Frequency
10,000 pF - NPO



Impedance vs Frequency
1,000 pF - NPO vs X7R
0805



AVX

NPO Dielectric

Preferred Sizes are Shaded

SIZE		0504**			0603**		0805			1005			0907		1206			1505		
(L) Length	MM (in.)	1.27 ± .25 (.050 ± .010)			1.60 ± .15 (.063 ± .006)		2.01 ± 0.2 (.079 ± .008)			2.41 ± .25 (.095 ± .010)			2.29 ± .25 (.090 ± .010)		3.20 ± 0.2 (.126 ± .008)			3.81 ± .25 (.150 ± .010)		
(W) Width	MM (in.)	1.02 ± .25 (.040 ± .010)			.81 ± .15 (.032 ± .006)		1.25 ± 0.2 (.049 ± .008)			1.27 ± .25 (.050 ± .010)			1.78 ± .25 (.070 ± .010)		1.60 ± 0.2 (.063 ± .008)			1.27 ± .25 (.050 ± .010)		
(T) Thickness	MM (in.)	1.02 (.040)			1.02 (.040)		1.27 (.050)			1.27 (.050)			1.27 (.050)		1.27 (.050)			1.27 (.050)		
(t) Terminal	MIN. MAX.	.12 (.005) .38 (.015)			.25 (.010) .51 (.020)		.25 (.010) .71 (.028)			.25 (.010) .76 (.030)			.25 (.010) .76 (.030)		.25 (.010) .71 (.028)			.25 (.010) .76 (.030)		
WVDC		50	100	200	50	100	50	100	200	50	100	200	50	100	50	100	200	50	100	200
Cap. (pF)	0.5																			
	1.0																			
	1.2																			
	1.5																			
	1.8																			
	2.2																			
	2.7																			
	3.3																			
	3.9																			
	4.7																			
	5.6																			
	6.8																			
	8.2																			
	10																			
	12																			
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	56																			
	68																			
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	120																			
	150																			
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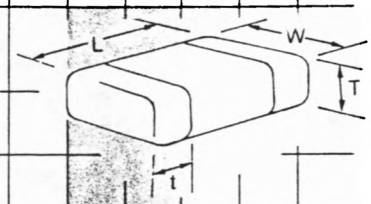
	220																			
	270																			
	330																			
	390																			
	470																			
	560																			
	680																			
	820																			
	1000																			
	1200																			
	1500																			
	1800																			
	2200																			
	2700																			
	3300																			
	3900																			
	4700																			
	5600																			
	6800																			
	8200																			
Cap (μF)	.010																			
	.012																			
	.015																			
	.018																			
	.022																			
	.027																			
	.033																			
	.039																			



NOTES:
- Dimensions are in millimeters, dimensions in parenthesis are in inches.
- **For higher voltage chips, see pages 22-25.**

**** IR and Vapor phase soldering only recommended.**

RAS-2
Meßstellenumschalter
Remote Access Switch System

Anhang zur Serviceanleitung
Service Manual Appendix

BN 9510/00.87

Wandel & Goltermann
Elektronische Meßtechnik

MESSSTELLENUMSCHALTER RAS-2

für die Zusammenfassung von koaxialen Meßpunkten

REMOTE ACCESS SWITCH SYSTEM RAS-2

for selecting coaxial test points

COMMUTATEUR DE POINTS DE MESURE RAS-2

pour la concentration des points de mesure coaxiaux

Anhang/Appendix/Annexe BN 9510/03/04/05

Serie/Series/Série A...

Best.-Nr. Order No. / Numero de commande BN 9510/03/04/05

Ausgabe / Edition 3287/5.85 ersetzt / replaces / remplace

I.5.85 kg/Se
0.12.5.85

Wandel & Goltermann Elektronische Meßtechnik

Anschriften

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Tel. 8-88 04 80, tlx. 17 783 wgab s

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Wandel & Goltermann (Schweiz) AG
Postfach 254, CH-3000 Bern 25
Tel. 31-42 66 44, tlx. 912 350 wgoch

USA
Wandel & Goltermann, Inc.
P.O.B. 13 585, Imperial Center
Research Triangle Park, NC 27 709-3585
Tel. 919-544-57 30, tlx. 810-621-0 002

Inhaltsverzeichnis des Anhangs — RAS-2

Contents of Appendix — RAS-2

Sommaire d l'annexe — RAS-2

Anmerkungen zu den Stromlaufplänen und den Schaltteillisten

Abkürzungsbeispiele

(4) = Stromlaufplan 4

[B20-8] = Leiterplatte 8

Pkt. 6 = Anschlußpunkt 6

TP 203 = Testpunkt 203

Farbkennzeichnung

bl - blau
blank - blank
br = braun
fl = farblos
ge = gelb
gn = grün
gr = grau
rs = rosa
rt = rot
Schirm = Schirm
sw = schwarz
vio = violett
ws = weiß

grrt = grau/rot

geschirmte Leitung
blanker Draht

BS = Bestückungsseite
NBS = nicht bestückte Seite

Alle angegebenen Spannungen sind mit einem Instrument 100 kΩ/V gegen 0 V gemessen.

Relais in Ruhestellung dargestellt

Sollten die Werte bestimmter Bauelemente in den Stromlaufplänen und Schaltteillisten differieren, so sind stets die Angaben in den Schaltteillisten als verbindlich anzusehen.

Bestellangaben

Be: Ersatzteilbestellungen unbedingt beachten:

Die genaue Bezeichnung ist der Schaltteilliste zu entnehmen.

Bauelemente mit BV bzw. WN sind im Werk anzufordern.

Neben der Bestellnummer (BN) ist die Gerätenummer mit Serienindex, die Positionsnummer des Bauelements und die Sachnummer anzugeben.

Beispiel: PM-20 BN 881/01
Nr. 0001 A

2 T 2

Schaltbild-Nr. Positions-Nr.
Sach-Nr. 0001-0015.836

Baugruppenverbindungen

Da die Stromlaufpläne für jede Baugruppe getrennt gezeichnet sind, müssen alle Zuleitungen zu anderen Baugruppen deutlich erkennbar sein. Die nachstehende Skizze erläutert die hier angewandten Verfahren zur Kennzeichnung.

Verfahren 1

Beim Anschlußpunkt einer Baugruppe steht die Adresse der anderen Anschlußpunkte, mit denen er verbunden ist.

Verfahren 2

Beim Anschlußpunkt steht nur eine Signalbezeichnung ohne Adresse. Dann sind alle Anschlußpunkte anderer Baugruppen mit der gleichen Signalbezeichnung untereinander verbunden.

Notes for Circuit Diagram and the Parts Lists

Abbreviations examples

Circuit diagram 4

Circuit board 8

Connection point 6

Test point 203

Colour coding

blue
bare wire
brown
transparent
yellow
green
grey
pink
red
screening
black
violet
white

grey/red

Screened lead
Bare wire

Component side
Soldering side

All voltage ratings measured with respect to 0 V with 100 kΩ/V meter.

Relays shown in rest position

If the values of individual components listed in the circuit diagrams and component lists should differ from another, these values given in the component lists are valid.

Ordering Information

When ordering spare parts, the following instructions must be followed without fail:

The exact designation of the component shall be taken from the "Parts Lists".
Components prefixed with BV or WN should be ordered from the manufacturer, W&G.
Next to the order number (BN) the serial number of that particular instrument along with the position number of the component and the item number shall be given.

Example: PM-20 BN 881/01
No. 0001 A

2 T 2

Circuit diagram Position No.
Item number 0001-0015.836

Connections between subassemblies

Because of each subassembly having been drawn separately, all the interconnections with the other subassemblies must be clearly identifiable. The following sketch explains the method used here for identifying the connections.

Method 1

At a connection point of a subassembly, there are located the addresses of the other connection points with which it is connected.

Method 2

At the connection point, there is only located a signal designation without address. Then, all similarly designated connection points of other subassemblies are interconnected.

Notes sur les schémas de principe et les listes de composants

Exemples d'abréviations

Schéma 4

Platine 8

Point de raccordement 6

Point test 203

Code des couleurs

bleu
nu
brun
transparent
jaune
vert
gris
rose
rouge
blindage
noir
violet
blanc

gris/rouge

Conducteur blindé
Fil nu

Côté composants
Côté soudure

Toutes les tensions données sont mesurées par rapport à 0 V avec un instrument de 100 kΩ/V.

Les relais sont représentés en position repos

Lorsque les valeurs de certains composants diffèrent entre les schémas de principes et les listes de composants, les valeurs des listes de composants sont seules valables.

Données pour la commande

Pour la commande de composants de rechange il faut absolument observer

La désignation exacte du composant qui est à prendre dans la liste des composants.
Les composants BV ou WN sont à réclamer à l'usine.

Outre le numéro de commande (BN) le numéro de l'appareil avec son index de série et le numéro de position du composant et numéro d'objet sont à donner.

Exemple: PM-20 BN 881/01
N° 0001 A

2 T 2

N° de schéma N° de position
N° d'objet 0001-0015.836

Raccordement des modules

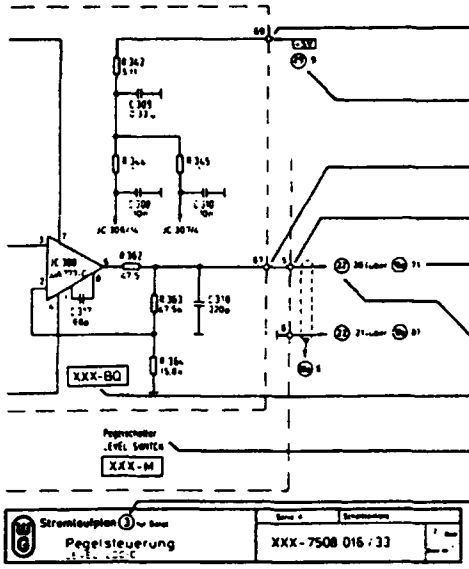
Les schémas de principe des modules étant représentés séparément les liaisons entre les différents modules doivent être facilement reconnues.
Le schéma suivant indique le système d'identification utilisé.

Système 1

Le point de raccordement du module comporte l'adresse de l'autre point de raccordement auquel il est relié.

Système 2

Le point de raccordement ne comporte qu'une indication de signal sans adresse. Tous les points de raccordement des autres modules comportant la même indication de signal sont alors reliés ensemble.



Anschlußpunkt 69 der Leiterplatte 697-BQ	Connection point 69 of printed circuit board (p.c.b.) 697-BQ	Point 69 du circuit imprimé 697-BQ
+ 5 V kommt von Stromlaufplan (29) Anschlußpunkt 9	+5 V coming from circuit diagram (29), connection point 9	le +5 V arrive du schéma (29), point 9
Anschlußpunkt 67 der Leiterplatte XXX-BQ geht auf Anschlußpunkt 5 der Trägerkarte XXX-M, von hier aus zu Stromlaufplan (18a) Anschlußpunkt 7 und schließl. zu Punkt 20 des Stromlaufplanes (22)	Connection point 67 of the p.c.b. XXX-BQ going to connection point 5 of mother board XXX-M, and from this point, to circuit diagram (18a), connection point 7, finally going to point 20 of circuit diagram (22)	le point 67 du circuit imprimé XXX-BQ va au point 5 de la carte support XXX-M, de là au schéma (18a) point 7 et pour terminer au point 20 du schéma (22)
Bezeichnung der Leiterplatte (Sandwichkarte)	Designation of p.c.b. (sandwich card)	Désignation du circuit imprimé (carte sandwich)
Bezeichnung der Trägerkarte	Designation of mother board	Désignation de carte support
Stromlaufplan Nr.	Circuit diagram No.	N° du schéma de principe

Bezeichnung der Anschlußpunkte

(30) 21: Anschlußpunkt 21 von Schaltbild (30)

(30) S 3010/a/5: Kontakt a/5 von Schalter 10 in Schaltbild (30)

Beispiel: Der Anschlußpunkt M des Schaltbildes (29) mit der Signalbezeichnung "Null-Verschiebung (0,4)" ist mit 2 weiteren Anschlußpunkten der gleichen Signalbezeichnung verbunden.

1) Kontakt a/5 von Schalter 10 in Schaltbild (30) (Verbindung läuft ganz oder teilweise außerhalb des Steckkartenträgers)

2) bBW/7 von Schaltbild (31) (Verbindung läuft innerhalb des Steckkartenträgers)

Bei Steckkartentechnik mit einem Steckkartenträger gibt eine Liste Auskunft über die Anschlußpunkte mit gleicher Signalbezeichnung.

Designation of connection points

(30) 21: connection point 21 from circuit diagram (30)

(30) S 3010/a/5: contact a/5 from switch 10 in circuit diagram (30).

Example: Connection point M of circuit diagram (29) having the signal designation "zero offset (0,4)" is connected to two other connection points of the same signal designation.

1) Contact a/5 from switch 10 in circuit diagram (30) (connection passes completely, or partially, outside of the mother board)

2) bBW/7 from circuit diagram (31) (connection stays within the mother board)

With plug-in p.c.b. technology using plug-in mother boards, a list provides information concerning the connection points having the same signal designation.

Désignation des points de raccordement

(30) 21: point de raccordement 21 du schéma (30)

(30) S 3010/a/5: contact a 5 du commutateur 10 du schéma (30)

Exemple: Le point de raccordement M du schéma (29) avec l'indication de signal "décalage du zéro (0,4)" est relié à deux autres points de raccordement avec la même indication de signal.

1) Contact a/5 du commutateur 10 du schéma (30) (la liaison passe entièrement ou en partie hors de la carte support)

2) bBW/7 du schéma (31) (la liaison passe dans la carte support)

Système de cartes enfichables sur une carte support. Une liste informe des points de raccordement avec la même indication de signal.

Buchsenleisten - Kontaktbezeichnung ≙ Anschlußpunkt-Bezeichnung } von Schaltbild (29)

Edge connectors - contact designation ≙ connection point designation } from Circuit diagram (29)

Prise - désignation du contact ≙ désignation du point de raccordement } du schéma (29)

Signalbezeichnung	außerhalb Prüfbereich	Anschlußpunkte	innerhalb Prüfbereich	I	II			II	I	innerhalb Prüfbereich	Anschlußpunkte	außerhalb Prüfbereich	Signalbezeichnung	Leiste
- 12 V		Stromversorgung siehe 81.16			20	V	18	18		Stromversorgung siehe 81.16			- 12 V	29
		frei			21	U	17	17	2	(30) Bo 3001 / 4			0 v 13 -2	376 GG
0 v 13 -2			(31) Bo 3001 / 3	2	22	T	16	16	2	(30) 00 / 6	sss	(30) 19	2³ x 0,01 A	81.33
2³ x 0,01 A		(30) 18 sss	(31) bBW / 4	2	23	S	15	15	2	(31) bBW / 2	sss	(30) 17	2¹ x 0,01 A	
2¹ x 0,01 A		(30) 16 sss	(31) bBW / 2	2	24	R	14	14	5	(18) 8 / 8, (19) 6 / 8, (20) 6 / 8, (22) 8 / 8			Reglak (Reglak)	
1 v 10 -2			(31) Bo 3001 / 1	2	25	P	13	13	2	(31) Bo 3001 / 2			2 v 13 -2	
Null - Verschiebung (0,2)		(30) S 3010 / a / 3	(31) bBW / 6	2	26	N	12	12	2	(31) bBW / 5	sss	(30) S 3010 / a / 2	Null - Verschiebung (0,1)	
Null - Verschiebung (0,4)		(30) S 3010 / a / 5	(31) bBW / 7	2	27	M	11	11	2	(31) bBW / 4	sss	(30) S 3010 / a / 4	Null - Verschiebung (0,3)	
Null - Verschiebung (0,6)		(30) S 3010 / a / 7	(31) bBW / 8	2	28	L	10	10	2	(31) bBW / 3	sss	(30) S 3010 / a / 6	Null - Verschiebung (0,5)	
Null - Verschiebung (0,8)		(30) S 3010 / a / 9	(31) bBW / 9	2	29	K	9	9	2	(31) bBW / 2	sss	(30) S 3010 / a / 8	Null - Verschiebung (0,7)	
Masse (boden)		Stromversorgung siehe 81.16			30	J	8	8		Stromversorgung siehe 81.16			Masse (boden)	
Verschiebung 2³		(19) C / 6, (22) 8 / 2, (23) 8 / 2		6	31	H	7	7	2	(31) bBW / 1	sss	(30) S 3010 / a / 10	Null - Verschiebung (0,9)	
Verschiebung 2²		(19) C / 5		2	32	F	6	6	2	(19) C / 4			Verschiebung 2³	
Verschiebung 2¹		(22) 8 / 4		2	33	E	5	5	2	(19) C / 10			Verschiebung 2¹	
Verschiebung 2⁰		(30) 21 sss	(31) bBW/11, (19) D/9	3	34	D	4	4	2	(22) 8 / 6			Verschiebung 2⁰	
Verschiebung 2⁻¹		(22) 8 / C		2	35	C	3	3	3	(20) 6 / 5, (21) 6 / 5			2⁻¹ x 0,01 A	
2⁻² x 0,01 A		(20) 6 / 6, (21) 6 / 6		3	36	B	2	2	3	(20) 6 / 6, (21) 6 / 6			2⁻² x 0,01 A	
- 6 v		Stromversorgung siehe 81.16			37	A	1	1	3	(20) 6 / 8, (21) 6 / 8			2⁻³ x 0,01 A	

Anschlußpunkte mit gleicher Signalbezeichnung für diese Buchsenreihe

Connection points with the same signal designation for this connector row of contacts

Points de raccordement avec même indication de signal pour cette rangée de prises

außerhalb Prüfbereich xxx innerhalb Prüfbereich

außerhalb Prüfbereich ≙ diese Anschlußpunkte sind durch Leitungen verbunden, die teilweise oder ganz außerhalb des Steckkartenträgers verlaufen

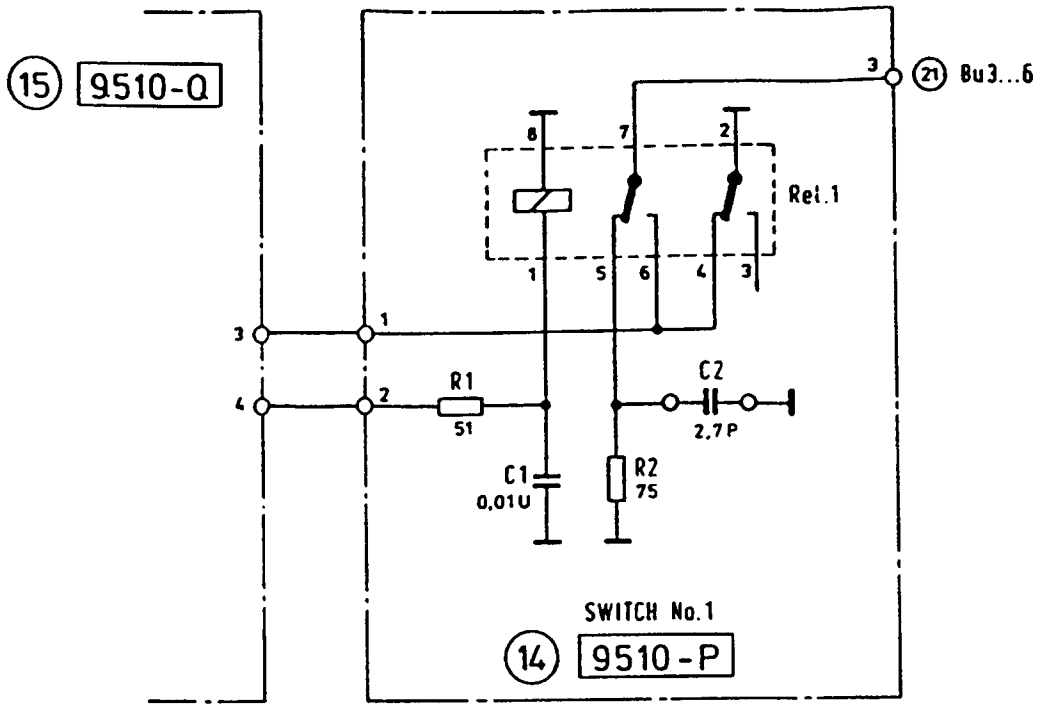
outside of test region xxx within test region

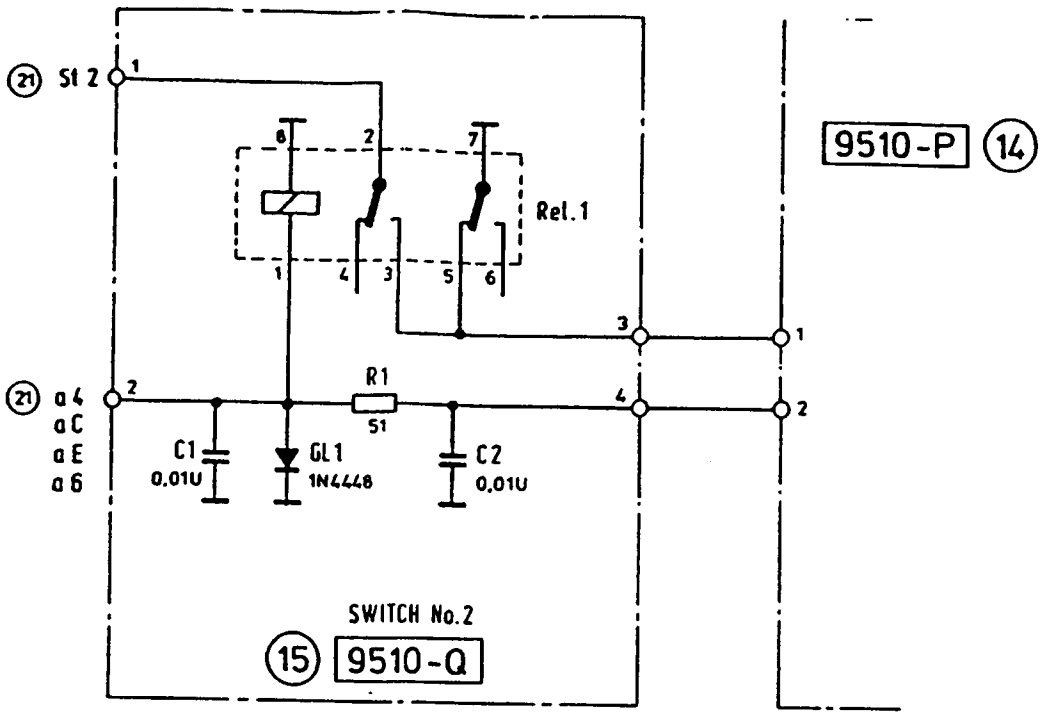
outside of test region ≙ these connection points are connected by lines which partially, or completely, pass outside of the mother board.

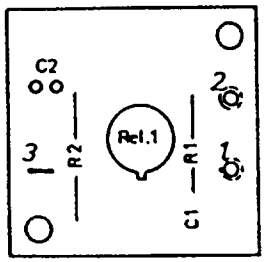
hors gamme de contrôle xxx dans la gamme de contrôle

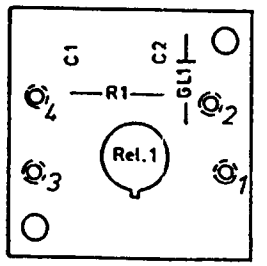
hors gamme de contrôle ≙ ces points de raccordement sont reliés par des conducteurs qui passent en partie ou entièrement hors de la carte support.

1	Meßstellenumschalter	BN 9510/03/04/05
1	Remote Access Switch System	BN 9510/03/04/05
1	Commutateur de points de mesure	BN 9510/03/04/05









14 9510-P

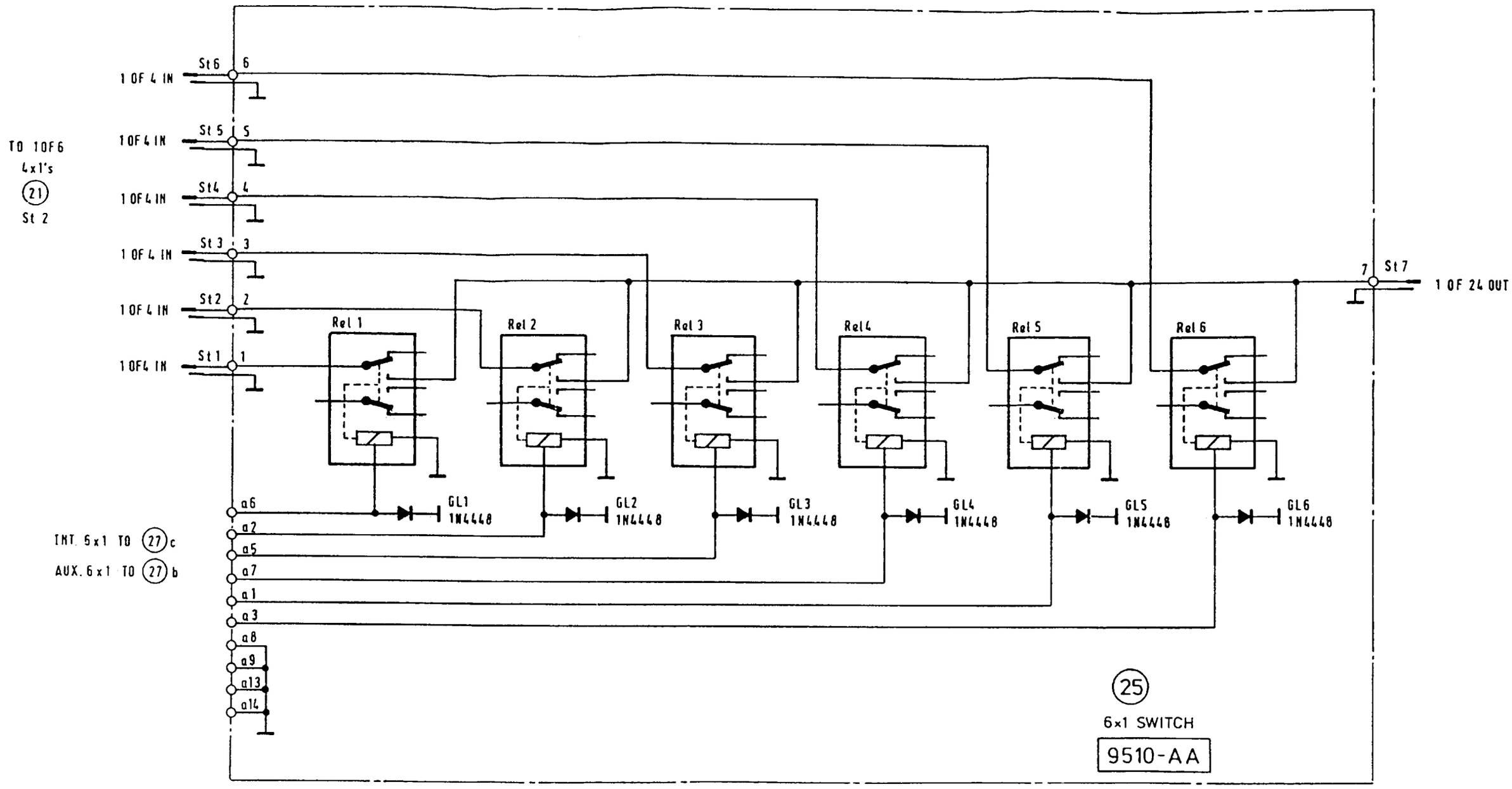
Benennung RAS-2 BN9510
Switch No.1 ASSEMBLED
9510-7014.00/4 2

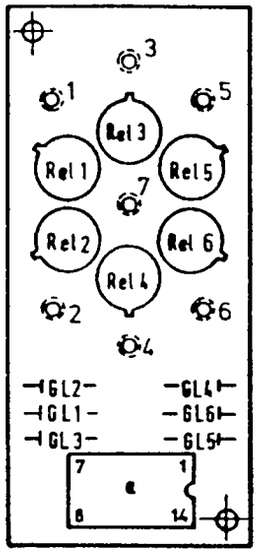
15 9510-Q

Benennung RAS-2 BN9510
Switch No.2 ASSEMBLED
9510-7015.00/4 2

Stromlaufplan für Gerät RAS-2 9510/03/04	Serie	Schaltanlage	
SWITCH No. 1	9510-7514.01/4 2		1 Blatt Blatt-Nr 1

Stromlaufplan 15 für Gerät RAS-2 9510/03/04	Serie	Schaltanlage	
SWITCH No. 2	9510-7515.01/4 2		1 Blatt Blatt-Nr 1





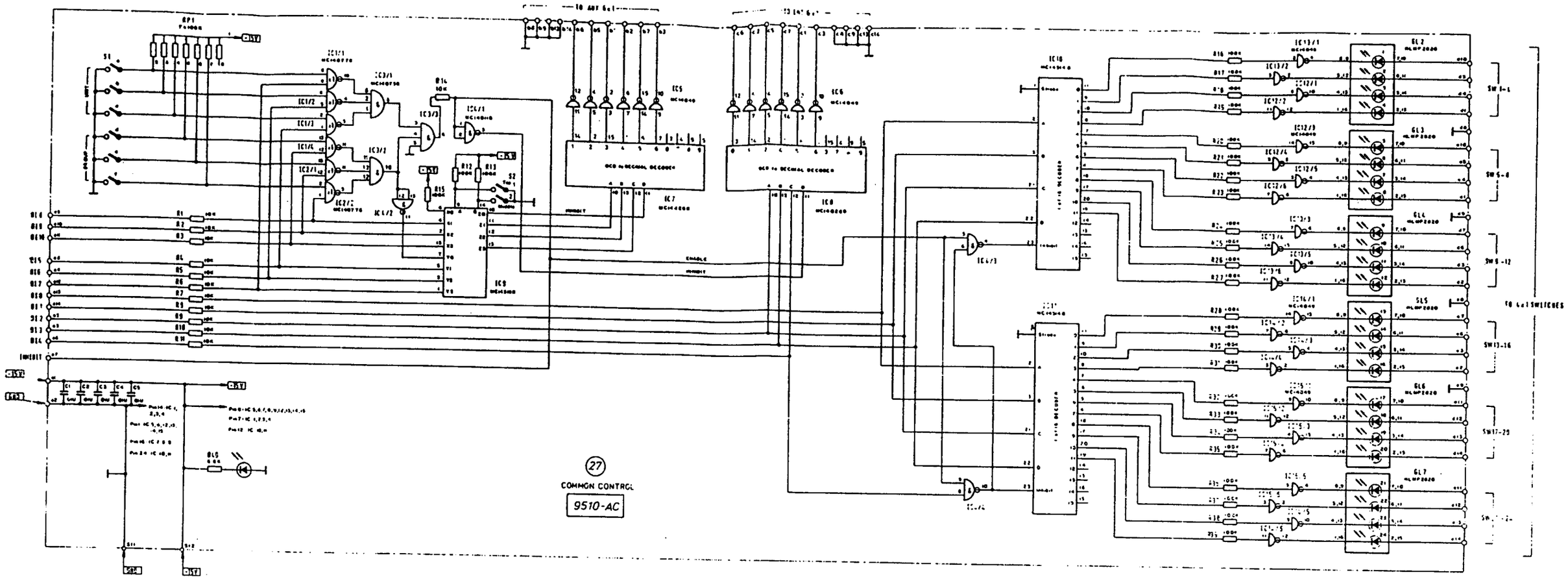
25

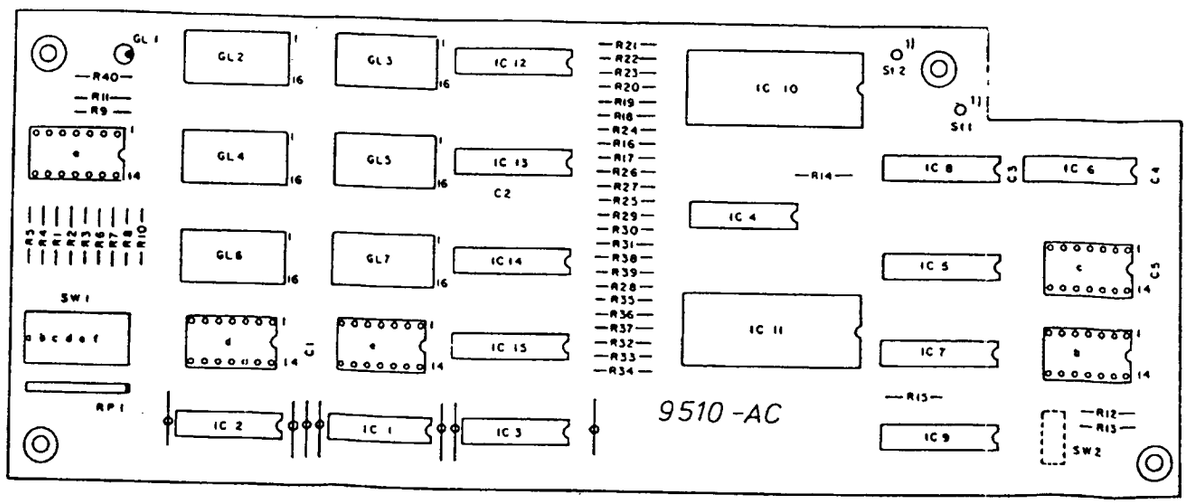
9510-AA

Benennung: 6x1 Switch	BN9510/03/04/05
ASSEMBLED	Series A...
9510-7025.00/4	0

6 x 1 switch — 1 aus 6 Schalter — Commutateur 1 de 6

WG Stromlaufplan für Berät.: BN9510/03/04	Serie A	Schaltliste 9510-7025.00	
6x1 Switch	9510-7525.01/3	1	Blatt 1 / Blatt-Nr. 1





27 9510-AC

Benennung	BN9510 /03/04/05
Common Control Board	
ASSEMBLED	Series A
9510-7027.00/3	

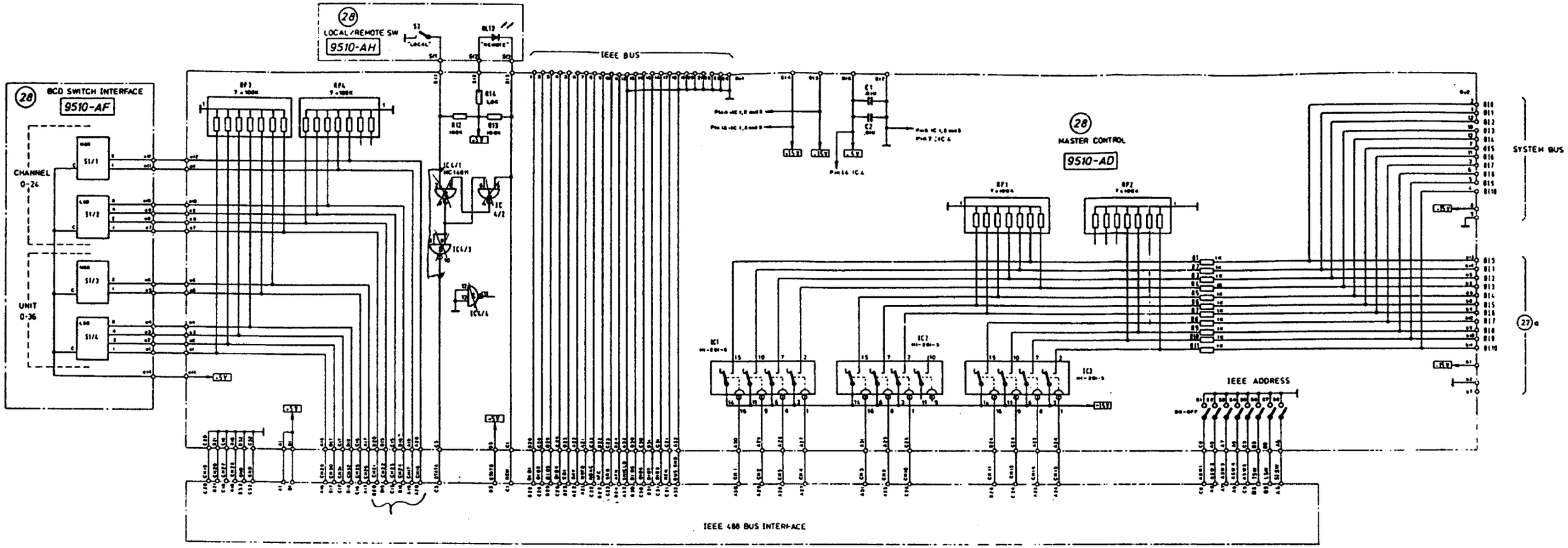
Common control
BCD to decimal decoder
To aux 6 x 1

Gemeinsames Steuerteil
BCD-Dezimal-Dekoder
Zum Sammelumschalter

Commande commune
Décodeur BCD-décimal
Vers auxiliaire 1 de 6

Überspannung gegen Masse: Instrument - 100 kΩ/V
ALL VOLTAGE RATINGS MEASURED WITH RESPECT TO 0 V WITH 100 kΩ/V METER
Toutes les tensions données sont mesurées par rapport à 0 V avec un instrument de 100 kΩ/V

RAS-2	Serie A	BN9510/03/04	
COMMON CONTROL (27)	9510-7527.01/33	1	



for modification

1. Remove IC4
2. ADD Jumper from where pin 2 of IC4 To pin 10 of IC4 was

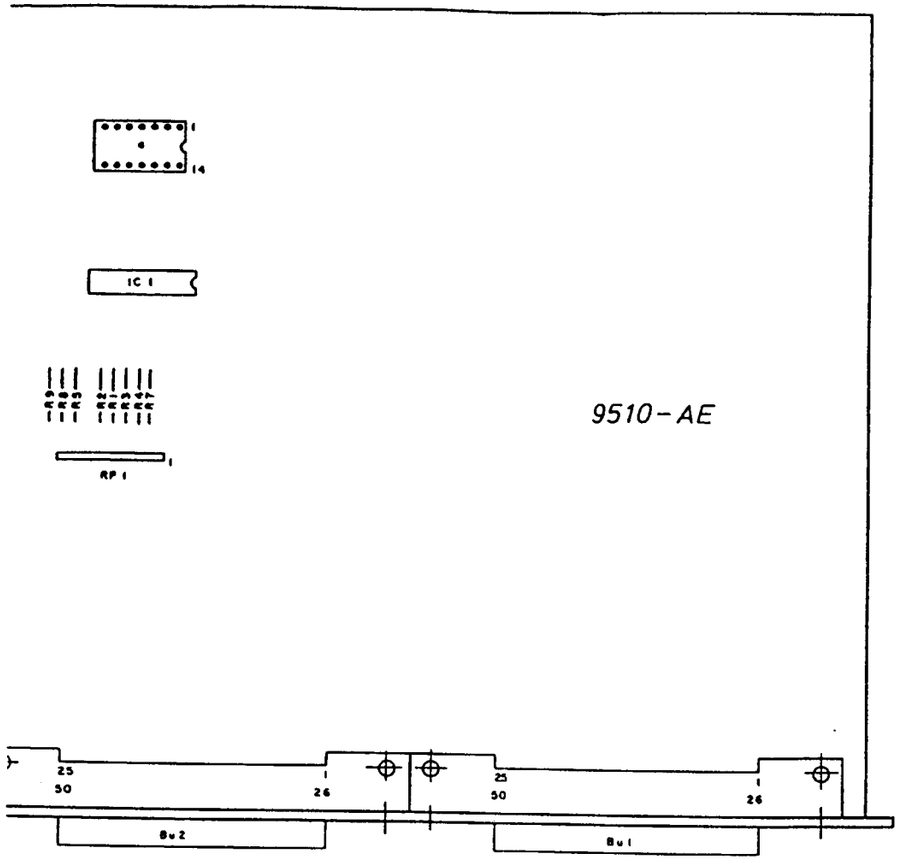
Master control	Hautpsteuerteil	Commande maître
and	und	et
BCD-switch	BCD-Schalter	Commutateur BCD
Channel	Kanal	Voie
Local	Handbetrieb	Local
Remote	Ferngesteuert	Télécommande
Unit	Gerät	Unité

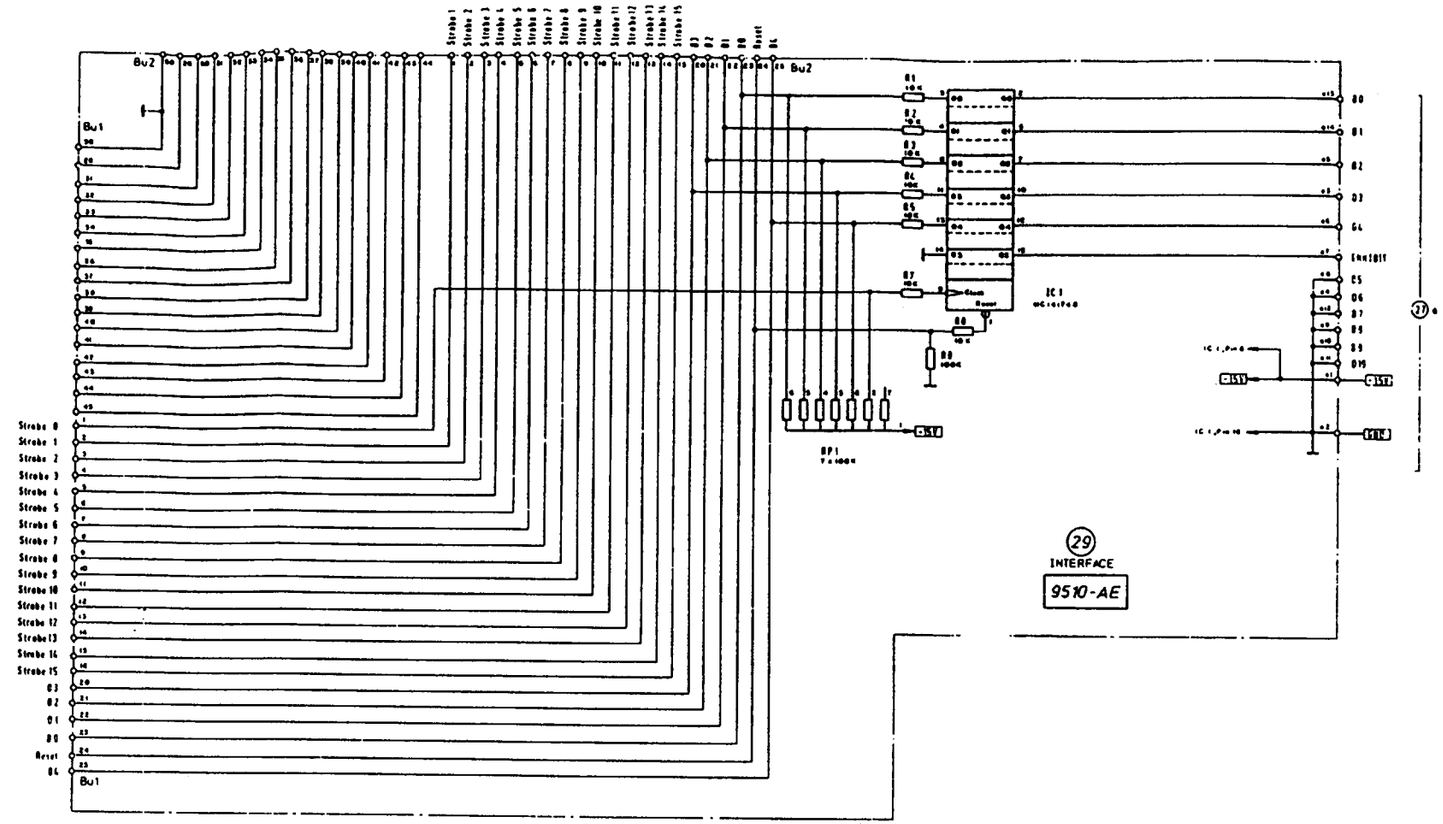
Stromlaufplan 28 für Gerät: 9510/03
Master Control

Serie A

9510-7528.01/33

1 Blatt
Blatt-Nr. 1





9510-AE

Benennung	BN9510/05
Interface, RAS-2 to RAS-1	
ASSEMBLED	Series A...
9510-7029.00/3	1

Stromlaufplan 29 für Gerät 9510/	Serie A	Schaltzeichnung 9510-7029.00
INTERFACE, RAS-2 to RAS-1	9510-7529.01/34	1 Blatt / Blatt-Nr. 1