CALIFORNIA INSTITUTE OF TECHNOLOGY

TO VLBA Correlator People

DATE October 24, 1983

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VLBA CORRELATOR MEMO
VC 003

SUBJECT VLSI Project Status

(This memo was prepared from materials used in a presentation of the JPL VLSI Chip Design work given on 9/29/83.)

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VLSI CORRELATOR CHIP

INTRODUCTION

MAJOR ISSUES

THE VLSI ADVANTAGE IN LARGE SYSTEMS LIKE THE VLBI CORRELATION PROCESSOR FOR THE VLBA:

* 50% ELIMINATION IN INTEGRATED CIRCUIT COUNT
* LIFE COST SAVINGS OF ~ $720 K

REVIEW THE CORRELATOR CHIP REQUIREMENTS

YIELD AND FAULT COVERAGE

DESIGN METHODOLOGY

COST SUMMARY OF THE CORRELATOR CHIP
$/CHIP

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VLSI CORRELATOR CHIP

VLBI SYSTEM STATISTICS

10 STATION - 32 SUBCHANNELS

	with VLSI	without VLSI
# of I/c's	66 K	128 K
# of p.c. boards	440	735
power	29 kw	65 kw
reliability	340 hrs	165 hrs
H/w $	$1,010 K	$1,445 K
mp $	790 K	895 K
Operational $/yr.	25 K	55 K
Life cost $ 6 yrs.	1,950 K	2,670 K
		(Δ+720 K)

# of microprocessors in system - 155
Algorithms demand a throughput of 775 million instructions/sec.
3K correlator chips are required (I/C reduction of 20 to 1)

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VLSI CORRELATOR CHIP
CORRELATOR CHIP REQUIREMENTS

The chip will contain two 8-lag complex correlators.

Quantization is either 2-level, 3-level, or 4-level.

Oversampling of 1x none, 2x, or 4x is available.

Multiplier products are pre-scaled (÷8) producing two data streams per lag. (complex)

Data correlation of up to 16 mega-samples per sec.

16 computational elements (CE) per chip.

NMOS technology

One watt of power.

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VLSI CORRELATOR CHIP
CHARACTERISTICS

Dual 8-stage shift register.

Input multiplexer logic for oversampling.

3-multiplier circuits for each computational element (CE) 48 million multiplications/ sec per CE

2-prescalers with overflow carries produces a complex data stream.

Each CE requires 625 gates (2,187 transistors)

occupies an area of 1.5 x .95 mm
3-micrometer minimum features

Correlator chip implementation requires 10.0 K gates (35 K transistors)

occupies an area of 6 x 3.8 mm

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VLSI CORRELATOR CHIP
YIELD PROSPECT

Reduction in a wafer yield (y)

Existence of area defects (y_o)

Whole portions of wafer provide no good devices

Existence of fatal point defects - defect density (D)

Defects are randomly distributed over wafer area

$y = y_o e^{-DA}$ A = chip active area

D = 5 defects/cm² A = 22.8 mm² y_o = .980

yield $y = .980e^{-1.14} = 31\%$ for a very large number of wafers

VLSI CORRELATOR CHIP

TESTING and FAULT ANALYSIS

$$F = 1 + \frac{1}{DA} \ln \frac{y_t}{y_p}$$

y_p = yield at probe y_t = true yield at 100% fault coverage

F = fractional fault coverage for a given set of test vectors

assume $y_t/y_p = 0.9$

$$F = 1 + \frac{1}{1.14} \ln .9 = .91$$

The fault coverage should be 91%

For high reliability test vectors should guarantee a fault coverage which cover the device's functions, and also the structures used for the circuit implementations ∿ 9000 vectors.

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VLSI CORRELATOR CHIP

CORRELATOR CHIP DESIGN METHODOLOGY

THREE DESIGN OPTIONS . . .

* GATE ARRAYS
* STANDARD CELLS
* FULLY CUSTOMIZED CHIPS

First two methods attain a high level of automation, speed design time and require little silicon savvy.

Fully customized approach requires the artistry of an IC expert.

STRUCTURED CUSTOM CHIP DESIGN -

Custom ICs by silicon compilers software

* Optimized circuit elements from user-specified inputs
* Without limited flexibility and inefficient layout

SMALL PROGRAMMABLE LOGIC ARRAYS (PLA) < 30 GATES EACH

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VLSI CORRELATOR CHIP
CORRELATOR CHIP DESIGN METHODOLOGY
STRUCTURED CUSTOM CHIP DESIGN

PRO	CON
* Reduces the design problem by 2/3 -- saved $240 K	Not as optimized as a full custom chip ∿0.67·A
* Cost is predictable	Yield can be improved 31% to 60% cost $50 K
* Bottom-up hierarchical design	
* Flexibility & efficient layouts	
* Optimized circuit elements (see CON)	

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VLSI CORRELATOR CHIP
COST SUMMARY OF CHIP

200 4 in.-wafer @ $500.00/wafer - $100 K & 20 K chips

Assume 30% usable chips = 6 K chips

fab cost	$100 K
package cost $10.00/chip	$60 K
testing	$50 K
Total	$210 K
$/chip =	$35.00

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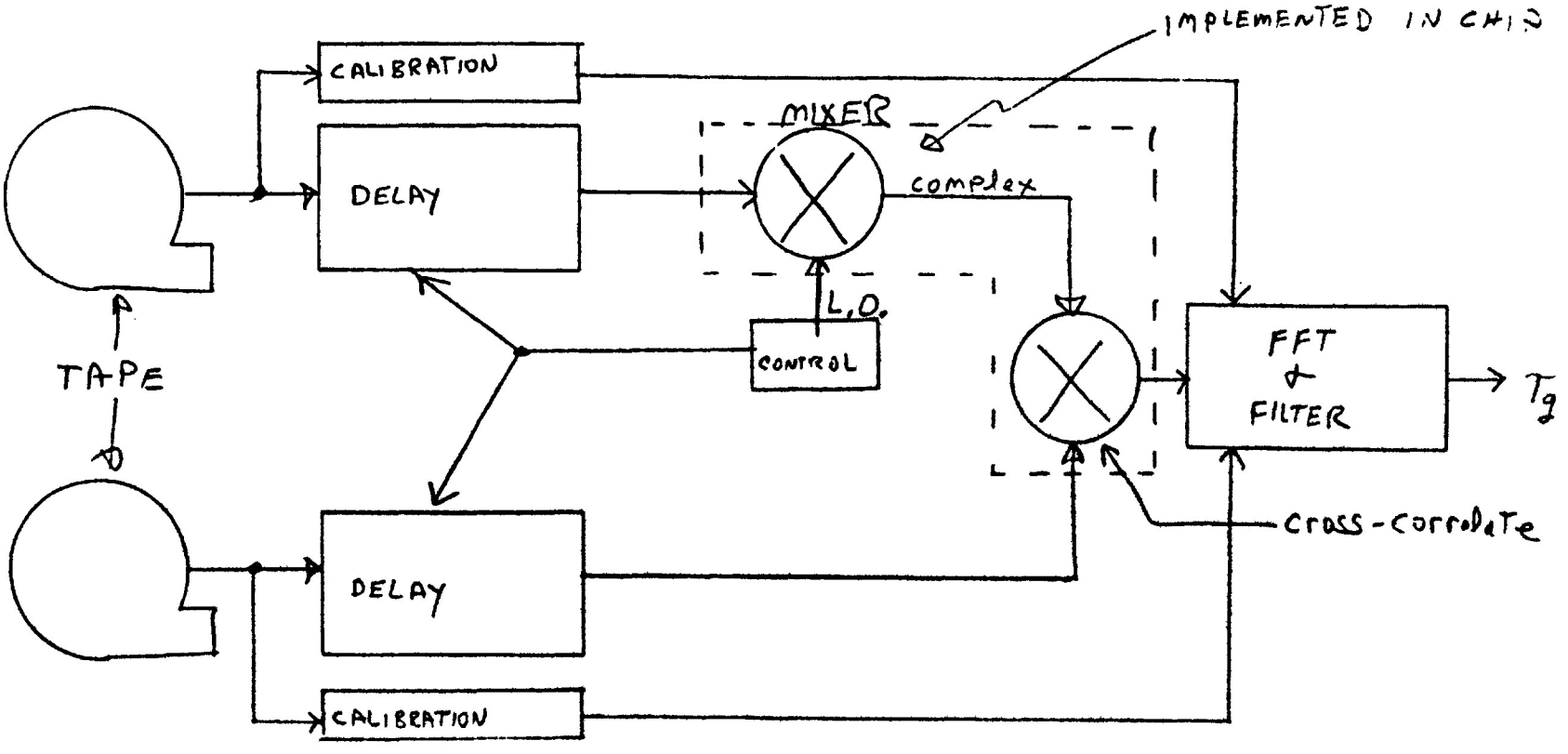
VLSI CORRELATOR CHIP
SUMMARY

* VLSI ADVANTAGE FOR THE VLBI PROCESSOR
  - SAVING OF $350 K - fewer ICs
  - $190 K - design methodology
  - $180 K - system reliability
* CORRELATOR CHIP REQUIREMENTS
* CHIP CHARACTERISTICS
* YIELD and FAULT COVERAGE
* DESIGN METHODOLOGY
* CHIP COST

VLSI CORRELATOR CHIP
CROSS-CORRELATION PROCESSOR

[28N] 28N(N-1)/2

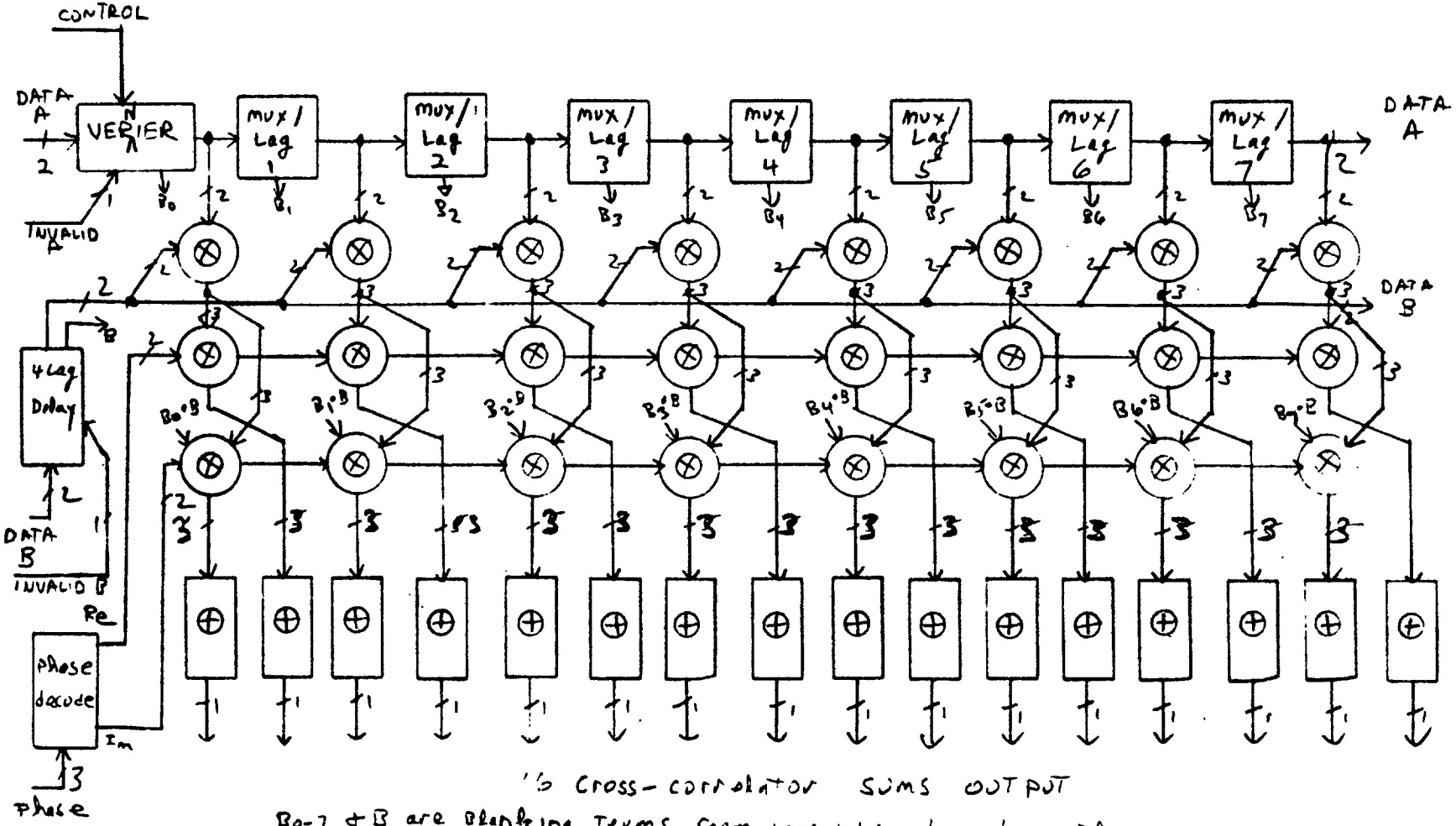


VLBI DATA PROCESSING (SIMPLIFIED) JCP 3-15

VLSI CORRELATOR CHIP

CORRELATOR BLOCK DIAGRAM

ONE OF TWO 8-Lag correlator circuits per chip



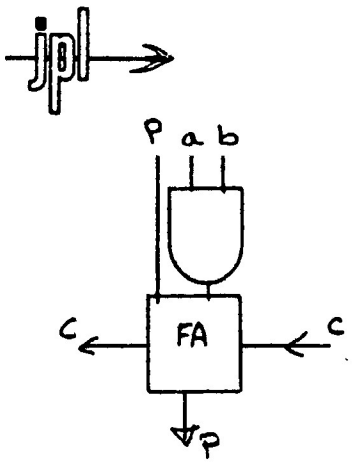
'6 Cross-correlator sums output

B0-7 & B are blanking terms from lags & delay 'or'ed' together

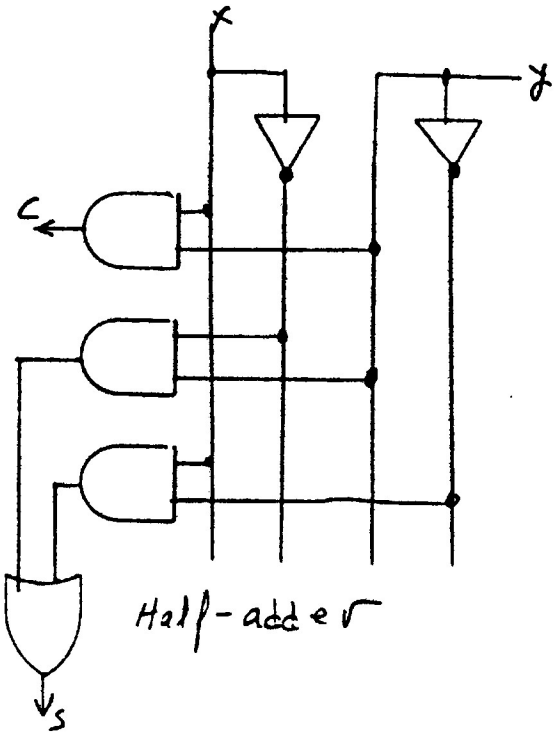
VLSI CORRELATOR CHIP

ARITHMETIC ALGORITHMS

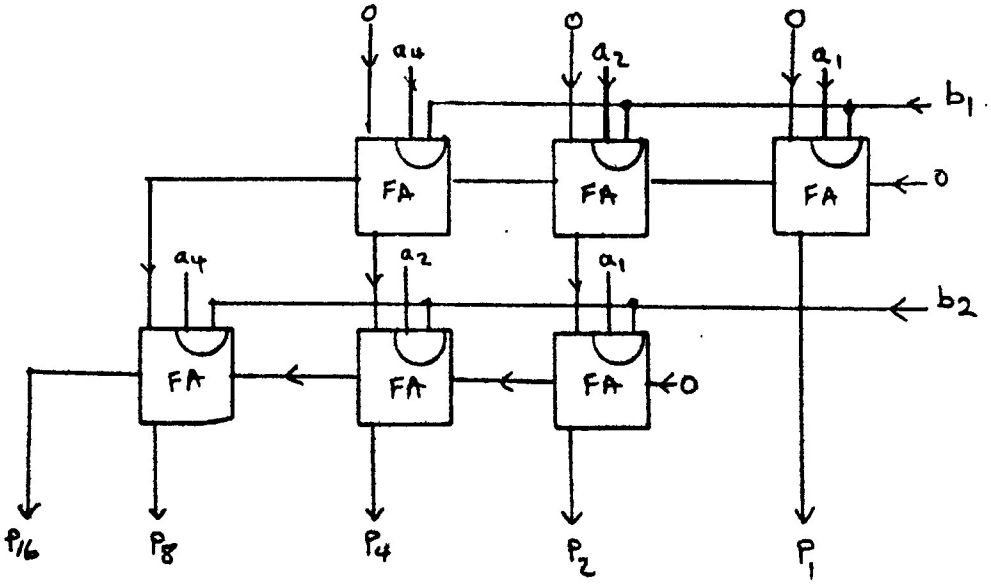
multiplication of binary numbers



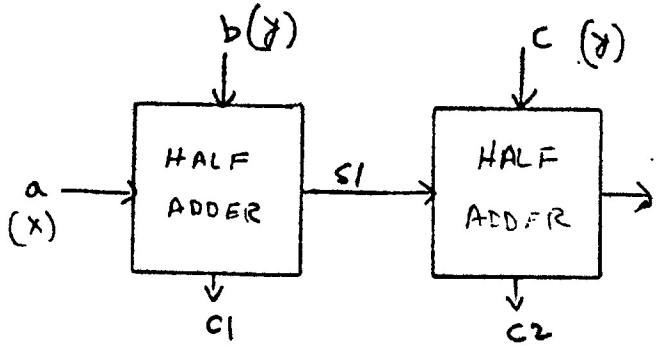
Iterative block



Half-adder



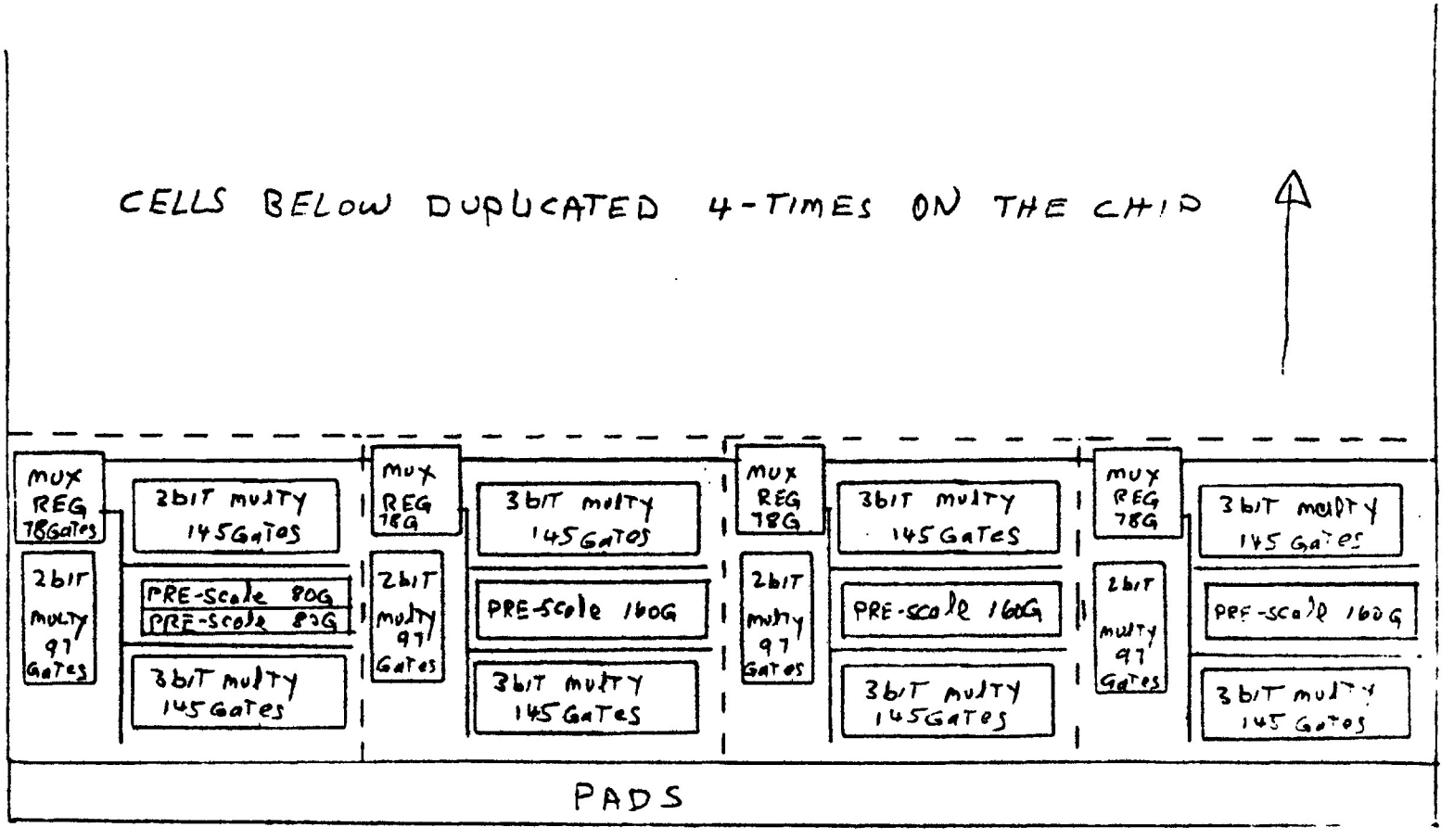
ITERATIVE ALGORITHM



Full-adder from Two half-adder

JCP 7-15

VLSI CORRELATOR CHIP
FLOOR PLAN



JCP 8-15

VLSI CORRELATOR CHIP

FULL CUSTOM OR STRUCTURED CUSTOM

FULL-CUSTOM
DESIGN COST - $360K
$/CHIP $27.00

STRUCTURED CUSTOM
DESIGN COST - $120K
$/CHIP - $35.00

DESIGN Δ = $240K
CHIP Δ = $8.00