JET PROPULSION LAB.   DEC. 12, 1983
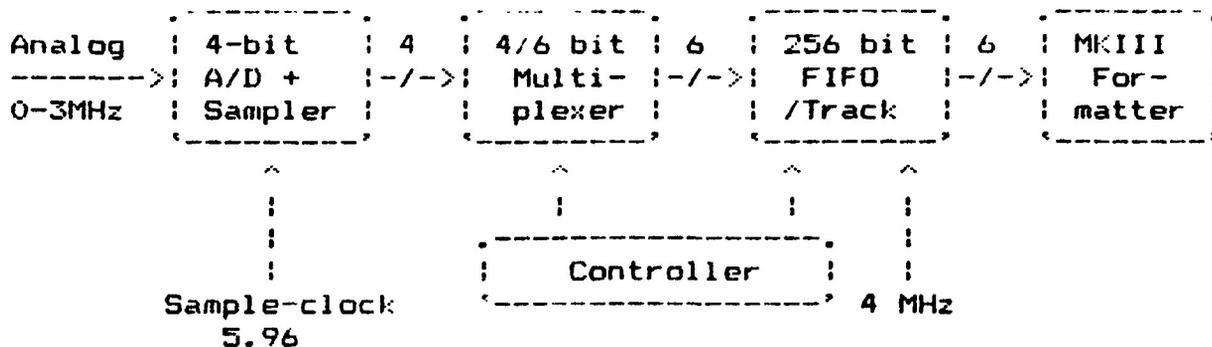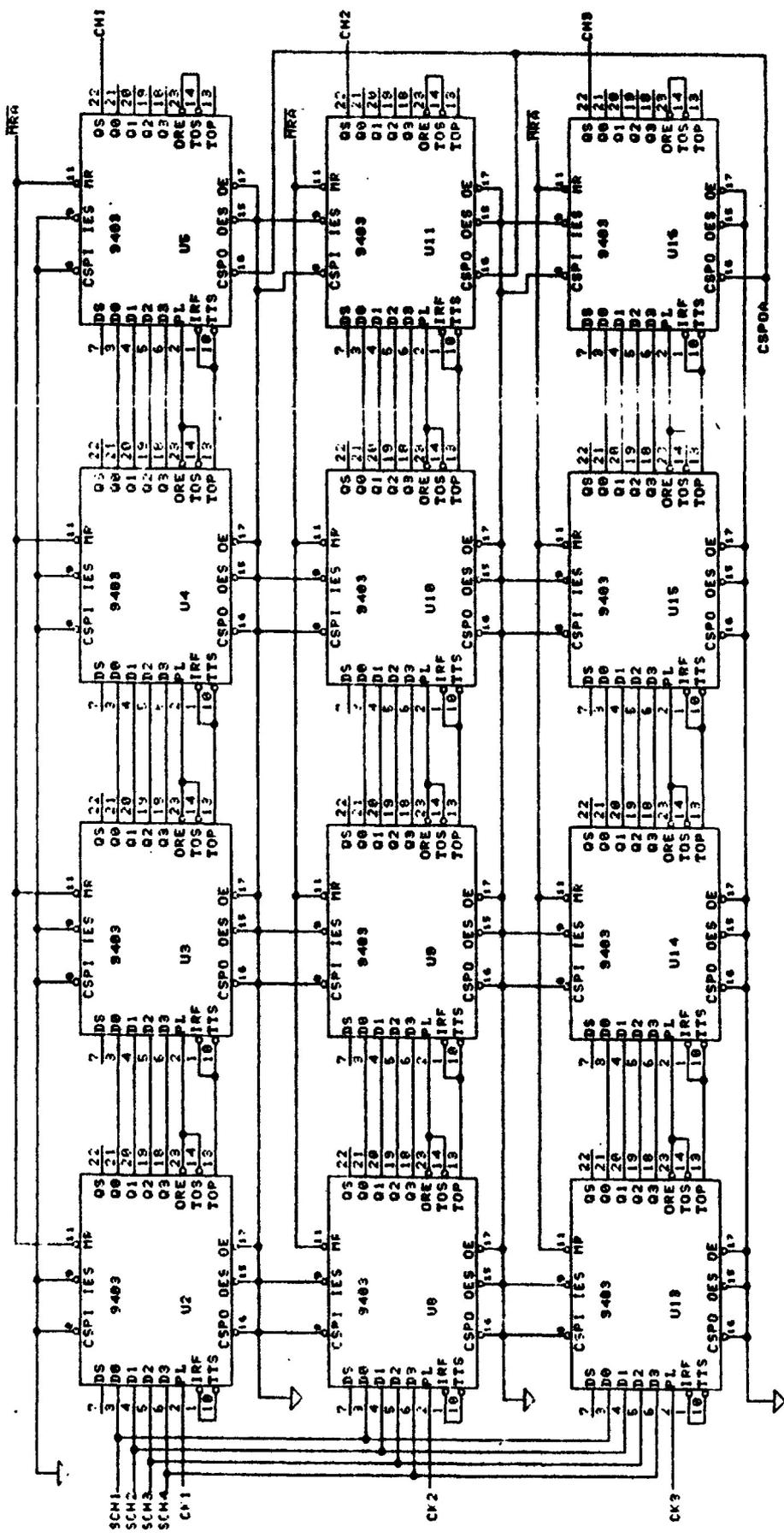VLBA MEMORANDUM

To: M. Ewing

From: B. Rayhrer, Les White

Subject: Recording with/without Data-gaps.

JLP has designed a circuit for recording on a MKIII terminal
without data-gaps for recording of telemetry data. This
circuit is designed for a 4-bit sampler with a sample-rate
of 5.96 MHz. 4 bits are then multiplexed on 6 tracks.
FIFO-storage of 256 bits per track is provided for storing
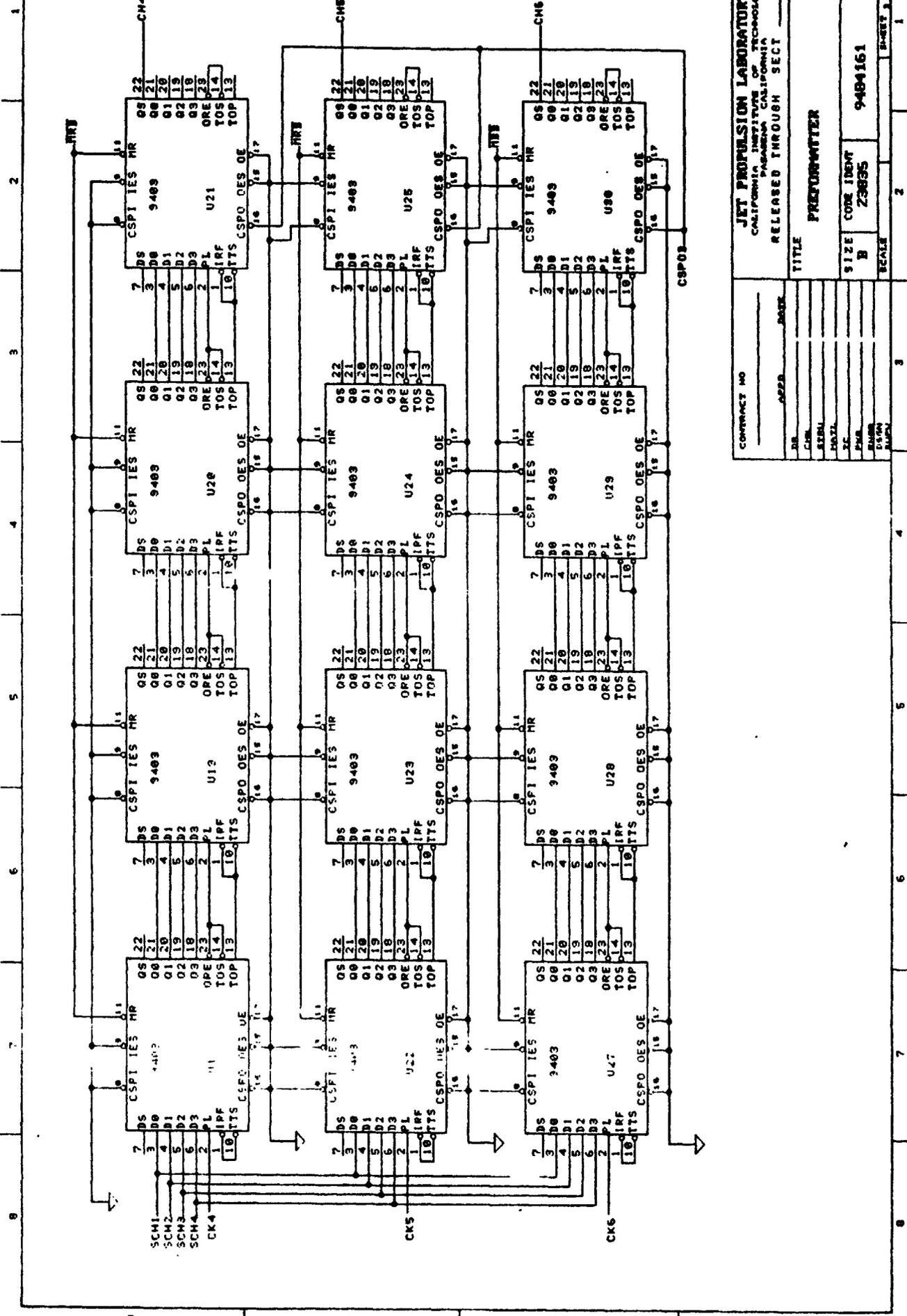data while the MKIII header is written on tape.

```
Analog    .- ------- .     .- ---- ----.      . ---------.     .------- - .
          : 4-bit    : 4  : 4/6 bit  : 6   : 256 bit  : 6  : MKIII    :
--------->: A/D +    :-/->:  Multi-  :-/->:   FIFO    :-/->: For-     :
0-3MHz    : Sampler  :    :  plexer  :     :  /Track   :     : matter   :
          '----------'     '----------'      '---------'     '----------'
               ^                 ^                ^         ^
               :                 :                :         :
               :            .-----------------.   :         :
               :            : Controller      :   :         :
          Sample-clock      '-----------------'  4 MHz
            5.96
```

As can be seen from the circuit diagrams, 11 chips per
track are needed. The VLBA requires no 4/6-multiplexer and
only a 160 bit FIFO simplifyng the circuit to only 5 1/2
chips per track.

SEQUENCE CONTROLLER

STATE CONTROLLER

MULTIPLEXER &
FIFO MEMORY
MATRIX
[SH 2]

FIFO MEMORY CONTROL

OUTPUT CLOCK POLARITY AND DELAY CONTROL

74974 — U44

27541 — U45

74LS157

74LS42 — U36

74LS163 — U52
74LS163 — U46
74LS163 — U47
74LS163 — U48
74LS163 — U49

26LS32B — U6
26LS32B — U26

7402 — U37A
7402 — U37B
7402 — U37C
7402 — U37D
7402 — U36A
7402 — U36B
7402 — U36C
7402 — U42C
7402 — U42A
7402 — U42B
7408 — U41A

74200 — U51

7404 — U33A

P2
P1

TEST IN

DELAY

CH1 CH2 CH3 CH4 CH5 CH6
CK1 CK2 CK3 CK4 CK5 CK6
CKO

SCH1 SCH2 SCH3 SCH4
MEWFR
TPCK
1PPS

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REV A

SCALE   SHEET 3 OF 4

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