NORTHEAST RADIO OBSERVATORY CORPORATION
HAYSTACK OBSERVATORY

10 April 1984

To: VLBA Correlator Group
From: Haystack Group
Subject: Notes on the "Haystack" fractional-bit correction algorithm

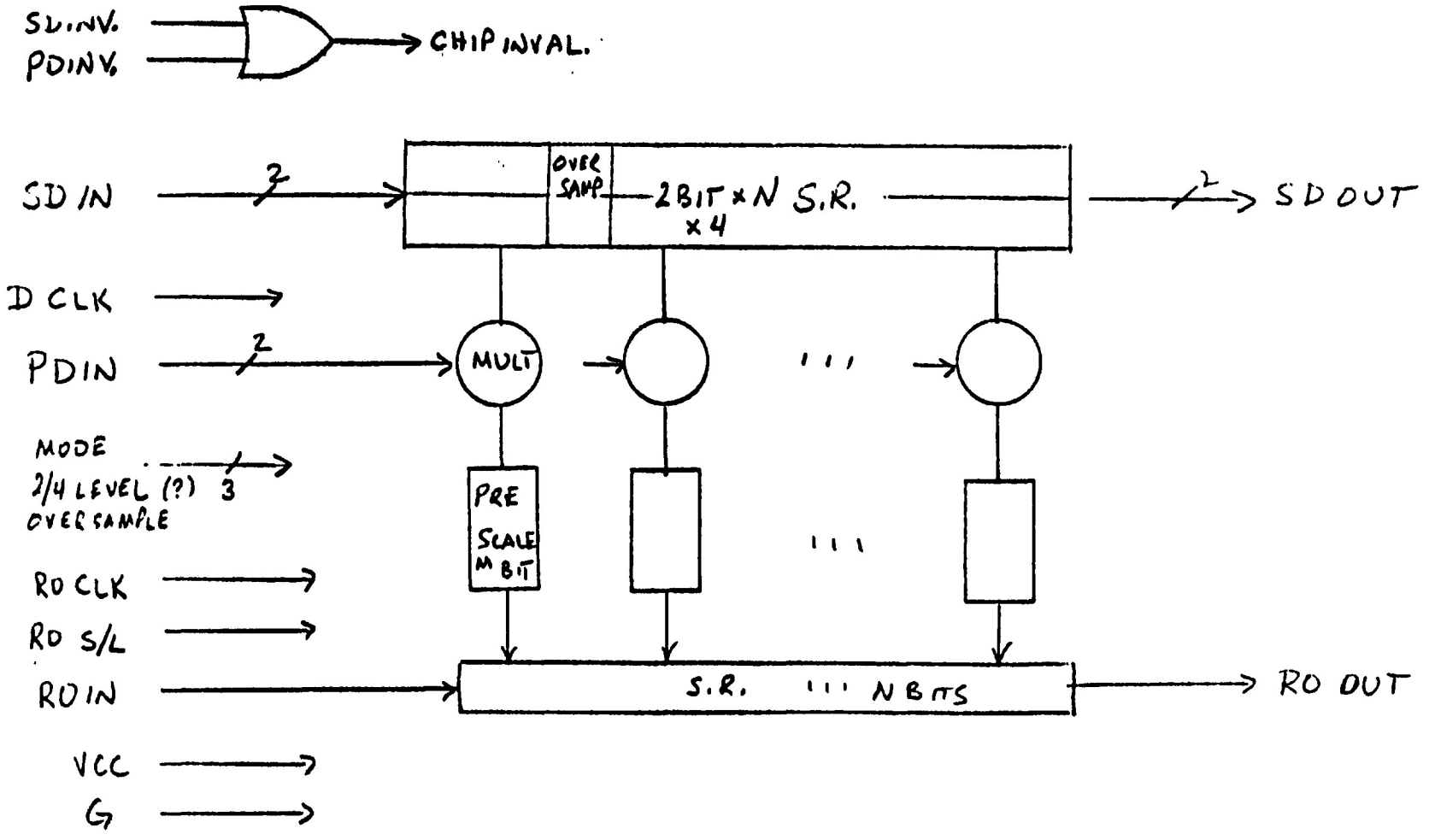
The question of the losses and benefits of various methods of dealing with the so-called "fractional-bit delay" has been discussed in several memos (see VLBA memos 112,270,326,333), but there still seems to be some confusion regarding the method and applicability of the fractional-bit correction as implemented on the Haystack correlator. The purpose of the memo is to clarify these points.

The "Haystack" algorithm corrects for the changing data delay by instantaneously adding +-90 degrees to the rotator phase at the same instant that the delay is changed by one bit. This adjustment may take place several times per second on long terrestrial baselines. The effect of this adjustment is to keep the phase of the rotator proper for the center of the recorded band, while allowing the phase error to build up to +-45 degrees at the bandedges. The only significant effect of this algorithm, if properly applied, if to reduce the SNR by approximately 3.5%. The algorithm is free of any systematic effects, regardless of the accumulation time, when a simple post-accumulation correction is applied (see VLBA memos 112,270).

The main benefit of the algorithm is to simplify the correlation processing of uniformly-sampled data with high bit-delay rates by allowing a simple method to extend accumlation times from milliseconds to seconds. Alternatively, in order to avoid the 3.5% SNR loss, the data must be broken into short segments, rapidly Fourier-transformed, then rotated to correct for the fractional-bit delay before accumulation into longer time segments. Furthermore, any such process of rapid Fourier transforms is unsuitable for spectral-line observations unless all lags are present at the time of the Fourier transform. In a correlator system which is designed to provide flexibility by trading number of channels (continuum) for number of lags (spectral), the complication in correlator architecture to provide this capability is considerable. When processing spectral-line data using the "Haystack" algorithm, lags can be combined in software following the correlation, avoiding complicated interconnections between modules processing only 8 or 16 lags each. Spectral-line data processed with the "Haystack" algorithm have been shown to be quite satisfactory.

It is true that variable-phase sampling would avoid the 3.5% SNR loss due to the "Haystack" algorithm, but new hardware, software, and operational complications are introduced, particularly in the acquisition systems. Furthermore, the coordination of the a priori models betweens the data acquisition and correlator systems must be precise down to the bit level at all times, otherwise the resulting data is subject to systematic errors at correlation time.

One further comment regarding the "Haystack" algorithm -- in order to process over-sampled data and, in some cases, phase-calibration signals, the same basic algorithm can be used provided that the phase-rotator increment applied at bit-shift time is a specifiable parameter, not simply fixed at +-90 degrees. This capability is easy to implement in hardware/firmware in the correlator.



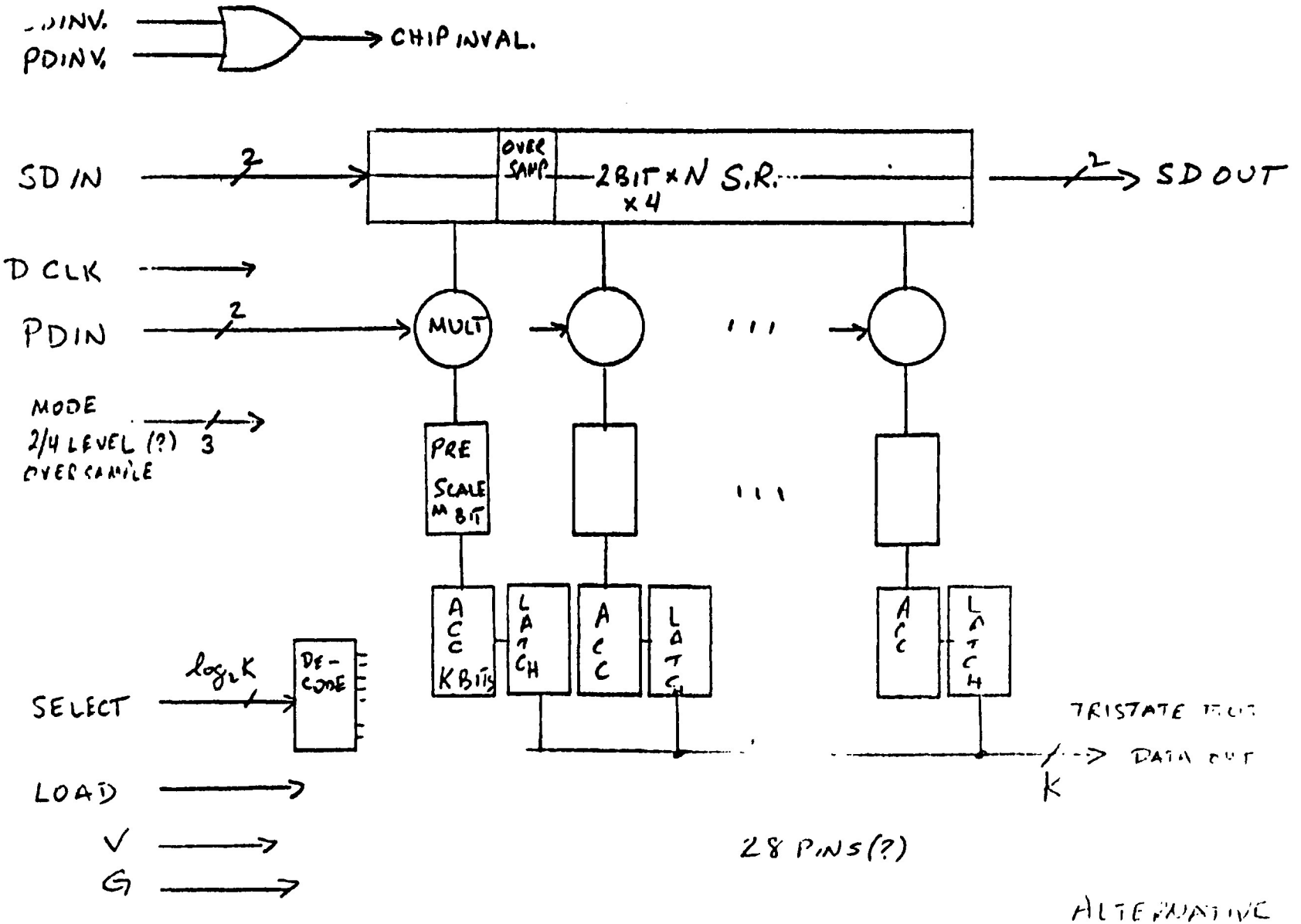
OFF CHIP: PHASE ROTN
VERN. DELAY
(INVALIDATE TIMING)

18 PINS

ISSUES: PRESCALER SIZE (M)
WHOLE CHIP INVALIDATE
NO READOUT OF LSB
N. LAGS (N)
HOW TO HANDLE OUTPUT DATA?

ALTERNATIVE
VLSI LAYOUT

7/20/84 MSE



OFFCHIP: PHASE POTN
VERN. DEL.
(INVALIDATE TIMING)

ISSUES: TRADE OFF N VS M VS K
ACCUMULATE TIME, ETC.

ALTERNATIVE
VLSI DESIGN
1/20/84 MSE