VLBA CORRELATOR SERIES
VC 025
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CSIRO

Division of Radiophysics
Vimiera and Pembroke Roads, Epping NSW

A Division of The Institute of Physical Sciences

Chief of Division
R H Frater, DScEng FTS

PO Box 76, Epping, NSW, Australia 2121
Telephone (02) 868 0222 Telex ASTRO 26230

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30 July 1984.

Dr M.S. Ewing,
California Institute of Technology
MS 105-24
Pasadena, CA 91125 USA.

Dear Marty,

Bob Frater, through John Brookes, has asked me to send you some details of our correlator chip for the Australia Telescope. I am also enclosing the latest P.R. sheet on the AT.

The chip we are building is an 8x8 array of correlators, with 8 X inputs and 8 Y inputs. i.e. 64 correlators per chip. Each correlator consists of an input section, a 1 or 2 bit multiplier section, a 4 bit prescaler, a serial adder/subtractor, a 16 bit accumulator register and a 16 bit result register. Data is output serially by connecting all 64 output registers in series. The multiplier is full 2 bit, i.e. counts of 1, 4 or 16, plus or minus. In 2 bit mode the data enters serially, magnitude then sign. The clock rate is 10 MHz, which for 2 bit operation gives 5 megacorrelations/sec.

The present status of the design is that we received prototypes of a 2x2 correlator array in mid June. This was an MPC fabrication using 4 micron SG-NMOS. It contains about 2400 transistors. Tests on these have been very encouraging. They function correctly up to about 14 MHz, although we have the feeling that this is limited at the moment by the external clock driver.

At the moment we are preparing a purchase document for the full production run. We require 4000 chips first up, with a possible extension to 10000. We hope to be able to use a 3 micron process, improving yield and speed. Simulations show that they could work up to near 20 MHz. Our plan is to have these delivered in the next 15 months.

Ihope this is of some use to you and I'd be glad to hear any comments you might have.

Regards,

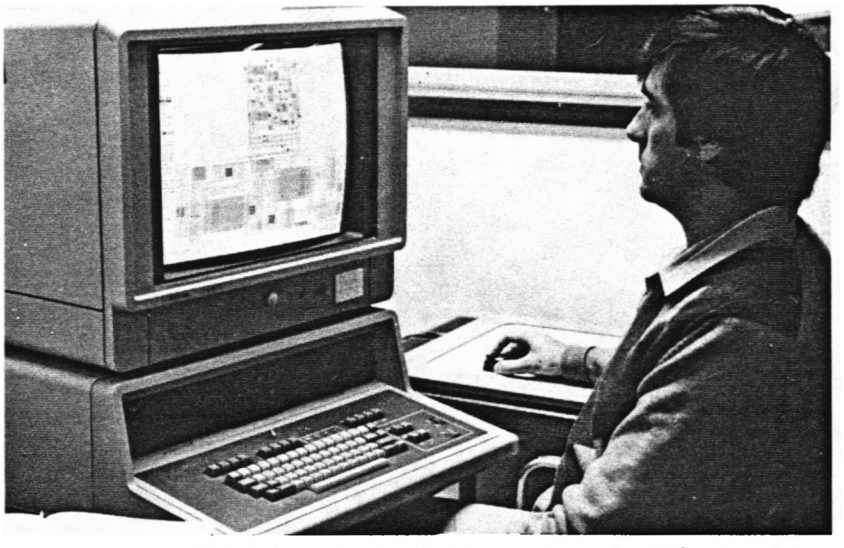
Warwick Wilson,
Section Leader,
AT Correlator Group.

VLSI TECHNOLOGY FOR THE AUSTRALIA TELESCOPE

The Digital Correlator

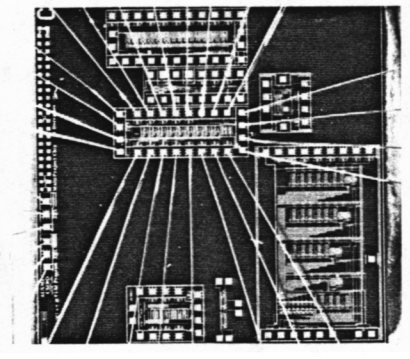
The Australia Telescope is not just a single telescope but rather an array of telescopes, or antennas, which can operate as one to simulate a telescope as large as the distance between the furthest antennas. The machine which lies at the heart of this type of telescope is called a correlator.

In this issue of A.T. Countdown, the workings of the correlator and the technology for its design and construction are described.



David Brown at the VLSI design workstation checking a portion of the AT Correlator design.

The signals received at each antenna in the AT arrays, after initial processing at the antenna, are sent via microwave links or fibre optic cables, to a building located near the centre of the 3 km railway track at Culgoora. Here they are fed into the Digital Correlator, a special purpose computer which carries out the first step of the processing required to produce a map of the area of sky being observed.



The AT Correlator chip on the multiproject wafer is seen bonded to the "outside world". The size of the actual chip is approximately one fiftieth of that shown.

In the correlator, the signal from each antenna, which by this stage is in digital (i.e. quantised) form, is multiplied by the signals from every other antenna and the products are accumulated for up to 10 seconds. For the 6 km Compact Array, with 6 antennas, there are 15 possible products, i.e. pairs. In fact, the number of products required is many more, particularly if spectral-line observations are in progress. In this case many extra products are formed by delaying one of the inputs to the multipliers by varying amounts. This provides the information necessary to produce maps at a set of contiguous frequencies as required for spectral-line studies. To provide the required number of frequencies for the entire array the correlator must perform over 6000 simultaneous multiplications for each set of signal samples from all antennas.

Up to 320 million sets of samples are sent from the antennas to the correlator every second. Even in terms of current and projected high density, high speed communications networks, this represents an exceptionally high data rate, and calls for the application of special techniques. For example, as it is not practical to build a multiplier capable of performing 320 million multiplications per second, we must revert to a technique called parallel processing. For each product, 32 multipliers are provided, each operating at 10 million multiplications per second. This gives a grand total of about 200,000 multipliers within the correlator.

The construction of a machine of these proportions has been made feasible by the use of Very Large Scale Integration (VLSI) techniques. Members of the Correlator Group within the AT Project are working on a design aimed at placing 64 multiplier/accumulators on a chip of silicon about 5 mm square. This chip will contain of the order of 30,000 transistors connected by conductors only 3 thousandths of a mm wide. The AUSMPC (Australian Multi Project Chip) program of the CSIRO Division of Computing Research's VLSI Program in Adelaide is providing a facility for the fabrication of prototypes. Encouraging results have already been obtained with test structures, the designs of which were submitted to AUSMPC in December 1983 and returned as working chips in February 1984. The next batch of chips, expected in June, include a full multiplier/accumulator implementation.

The Digital Correlator of the Australia Telescope represents a major advance in the use of state-of-the-art high speed digital electronics technology in Australia.

PROJECT PERSONNEL (CONT.)

Mr M.W. (Mal) Sinclair – section leader for the receivers. Mal has been a leading member of the Division's receiver group over the last 20 years including a period in the U.S.A. where he was responsible for the installation of the cooled microwave amplifiers on the 27 antennas of the Very Large Array radio telescope built by the NRAO in New Mexico and commissioned in 1979.

Dr W.E. (Warwick) Wilson - section leader for the correlator. Warwick recently returned to the Division following his secondment to Interscan Australia Pty. Ltd. in their joint venture with Wilcox Electric in the U.S.A. to develop the Interscan technology.

Dr R.H. (Ron) Wand – section leader for computing. Ron has returned to Australia for the AT Project after spending some 12 years in the U.S.A. including periods at the MIT Haystack Observatory where he was engaged in ionospheric and propagation studies.

Dr A.C. (Alan) Young is the leader for the signal distribution and monitoring section of the project. Alan returned to Australia to join the project after a stint at the Owens Valley Radio Observatory where he played a major part in the development of the mm telescope project.