VLBA CORRELATOR SERIES
VC 026
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NATIONAL RADIO ASTRONOMY OBSERVATORY
Charlottesville, Virginia 22903

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MEMORANDUM

TO: VLBA Correlator Group

FROM: R. Escoffier

SUBJECT: My Favorite Correlator Architecture

I have recently been studying correlator architecture for a possible VLA upgrade and for a possible millimeter array correlator.

The following attachments are the result of that study so far. While intended for a correlator where no fringe rotation, etc., need be done at the correlator, they still may have some application to a possible VLBA architecture. Note that the study considered only the correlators and ignored any integration.

The most important result applicable to the VLBA is the matrix structure of the correlator. This structure allows minimization of the lag generating shift register. The M by N gate array correlator chip allows maximizing the gate array utilization by not forcing N = M. System data interfaces are minimized by making N = M while lag generating shift registers are minimized by making N as large as possible. The optimum values of N and M thus depend on at least three factors: specific gate array, minimizing redundant lag generating flip/flops, and minimizing data interfaces. Note that lead channels, lag channels and auto products are all obtained in the simple system geometry.

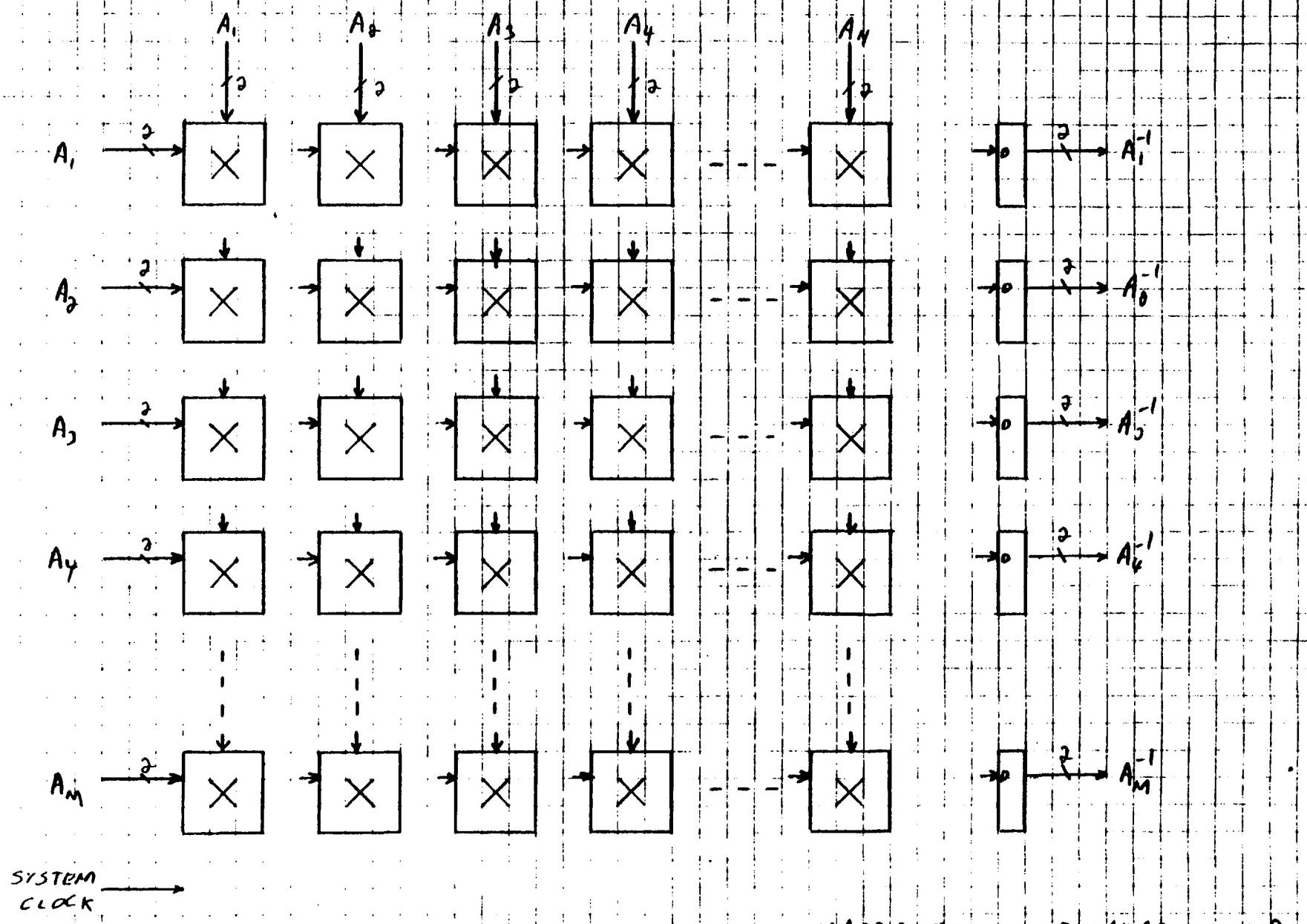
The big shortcoming of the study so far is, of course, the failure to include any information on integrators. My only thought on integrators as of now is that it would be nice for the correlators and a small pre-scaler to be on one gate-array chip and integrators on a second. I have two reasons for this approach: 1) the wastefullness of using the same technology to make both the high speed correlators and the lower speed integrators, and 2) an integrator chip has more universal applicability than a correlator chip since correlator structure (number of levels per sample, fringe rotation, etc.) varies with application while integrators do not.

7/13/84 RPE

IC	# MACROCELLS	$ DEVL.	$ IC	# CORR/IC	@ FREQ	P DISS (PER CORR) WATTS	COST FOR 10^7 MULT/SEC	# FCS TO MAKE VLAC	EST COS TO BUILD VLAC
(1) MCA 600 ECL	24	20K	29.00	8	128 MHZ	0.9 (.072)	$28.3	1458	$180K
(1) MCA 1200 ECL	48	27K	57.00	20	128 MHZ	1.8 (.072)	$22.3	584	105K
(1) MCA 2500 ECL	110	52K	280.00	48	256 MHZ	3.8 (.074)	$22.8	122	76K
(1) MCA 500 ALS	24	14K	9.50	8	32 MHZ	?	$37.1	4374	371K
(1) MCA 1300 ALS	60	19K	20.25	24	32 MHZ	?	$26.4	1458	155K
(1) MCA 2800 ALS	130	37K	225.00	56	100 MHZ	1.0 (.019)	$40.2	209	108K
VLA-1	—	43.4K (4)	8.50 (4)	2	100 MHZ	0.6 (0.3)	$49.0	5832	490K (
(2) QH1500 A	136	40K	85.00	32	80 MHZ	1.5 (.044)	$33.2		
(3) CALMOS 250	10	12.5K	2.25	4 (est)	25 MHZ	.02	$22.5	11664	822K
(3) CALMOS 1200	48	26K	10.50	20 (est)	25 MHZ	0.14	$21.0	2333	203K
(1) HCA 6306 CMOS	216	20K	4.00	18	25 MHZ	SMALL	$8.9	2592	192K
(1) HCA 6312 CMOS	400	27K	10.00	36	25 MHZ	"	$11.1	1296	111K
(1) HCA 6324 CMOS	765	35K	18.00	64	25 MHZ	"	$11.25	729	74K
(1) HCA 6348 CMOS	1620	50K	75.00	156	25 MHZ	"	$19.2	300	65K

(1) MOTOROLA, (2) AMCC, (3) CALMOS, (4) 1984 DOLLARS,

(6) COST EQ IS
$N(F+2C)$, N-#
F = 66.0, C = cos



MACROCELL CORRELATOR CHIP

RAL
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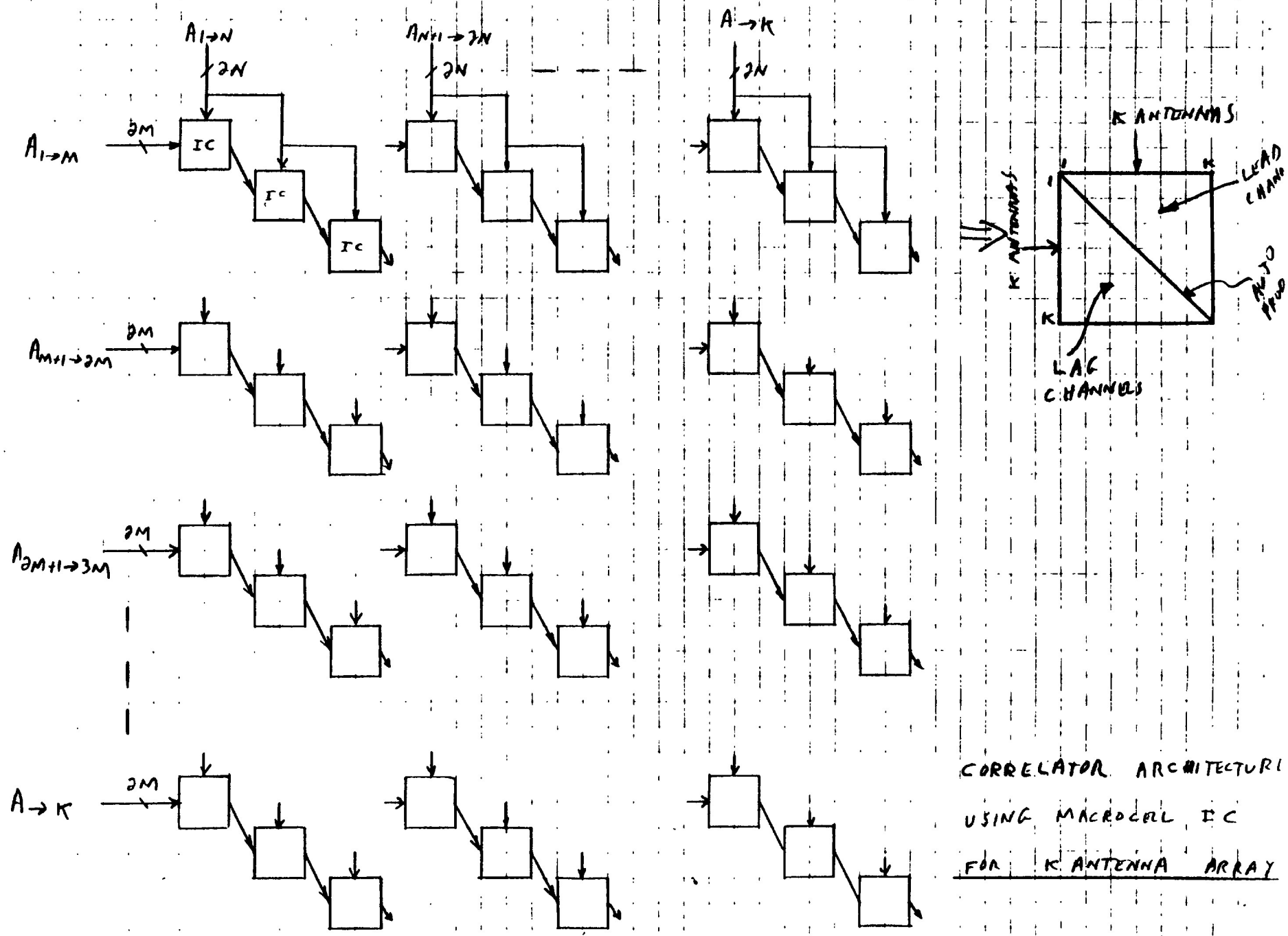

CORRELATOR ARCHITECTURE
USING MACROCELL IC
FOR K ANTENNA ARRAY

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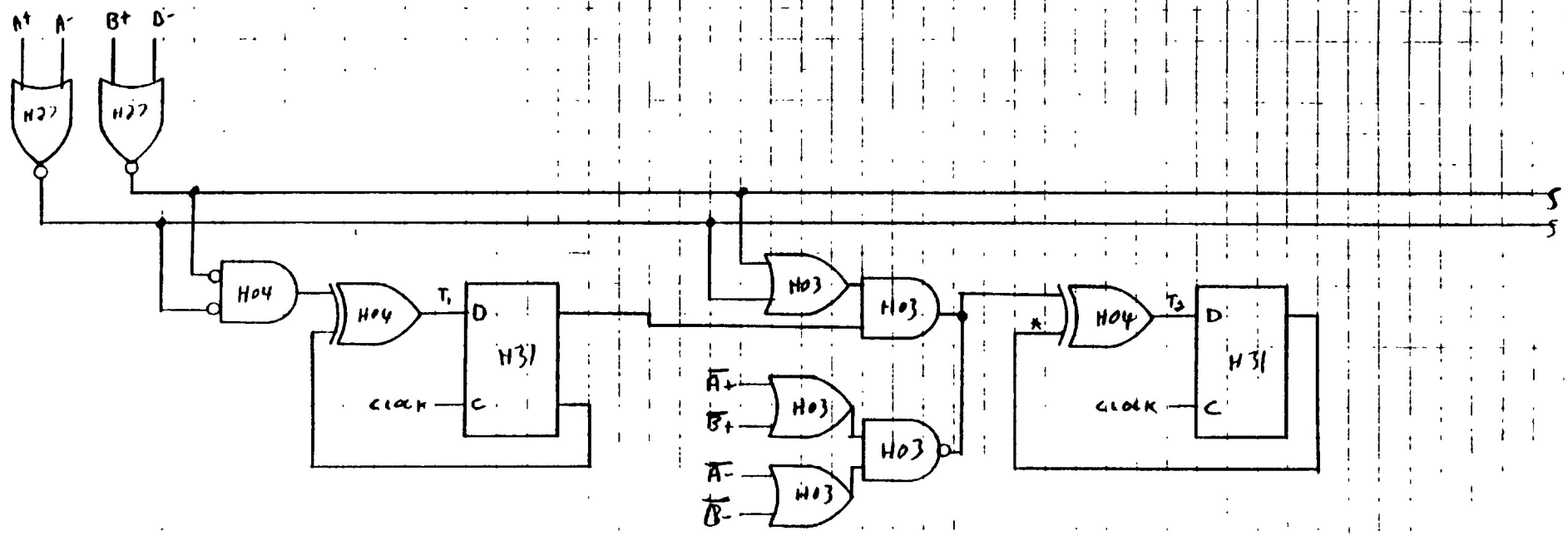

H27: 1.1 ns

H04: 1.4 ns (*)
1.05 ns

H03: 1.4 ns (*)
1.1 ns

H31: 1.5 ns PROP
1.5 ns T_{su}

2 CELLS

MCA 600, MCA 1200
CORRELATOR

$T_1 = 1.5 + 1.1 + 1.4 + 1.5 = 5.5$ MSEC

$T_2 = 1.5 + 1.1 + 1.4 + 1.05 + 1.5 = 6.55$ MSEC

$F_{CLOCK} = 128$ MHZ

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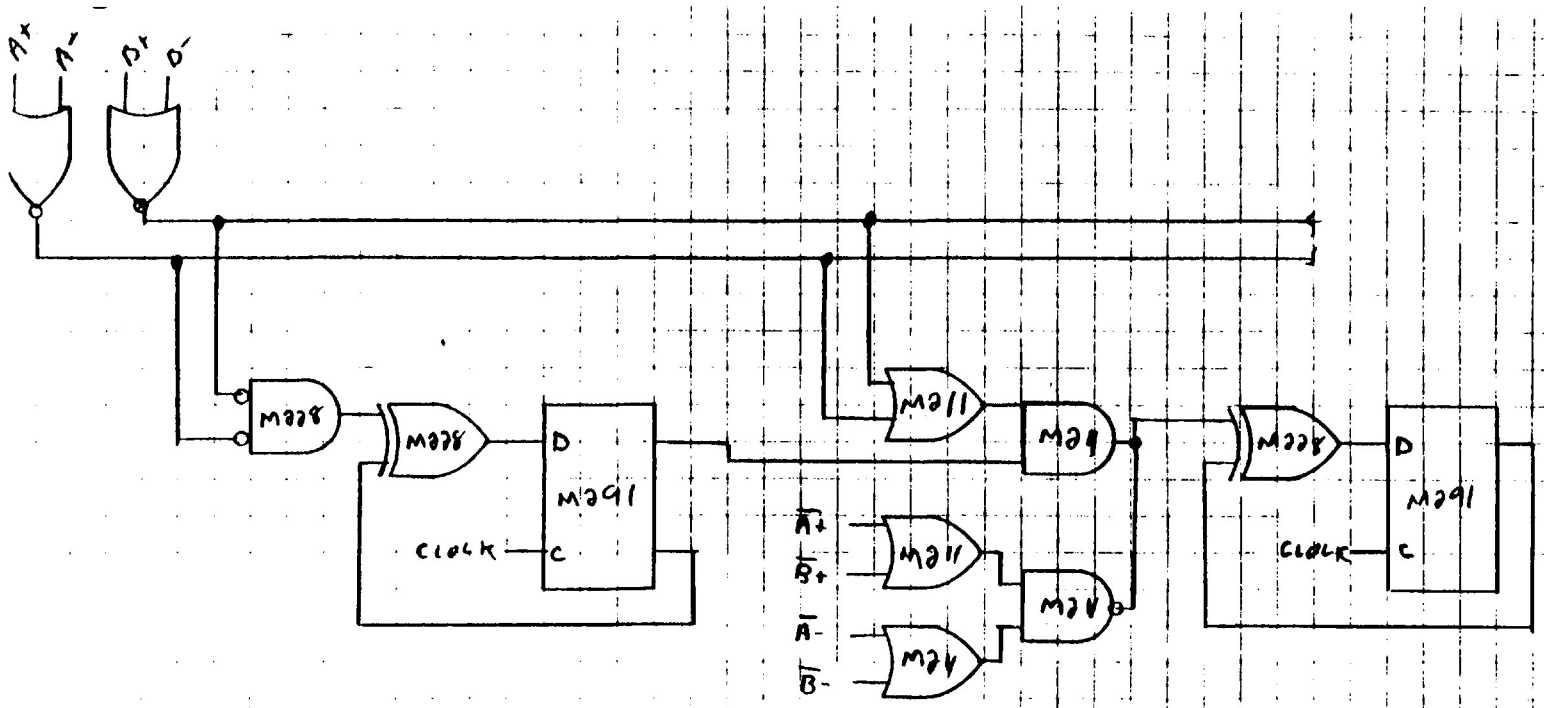

	ECL	ALS
M228:	0.575 nSEC	1.55 nSEC
M291:	0.750 nSEC T_{SU}	2.25
	0.60 nSEC T_{PPOP}	1.7 nSEC
M211:	0.55 nSEC	1.65 nSEC

$\boxed{2 \text{ CELLS}}$

$F_{CLOCK} = 256$ MHZ

$F_{CLOCK} = 100$ MHZ

MCA2500 CORRELATOR

OR MCA2800 CORRELATOR

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