VLBA Acquisition Memo # 19

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VLBA CORRELATOR SERIES
VC 027
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To: VLBA Correlator and Recorder groups
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Subject: Suggested DPS/Correlator Interface

DPS/Correlator Interface

The DPS/Correlator interface carries the following signals :

Timing Interface:
- 1 pps and 16 MHz provided to both correlator and DPS's from a master clock. Signals provided on differential ECL lines.

Signal Interface (DPS to Correlator):
- 16 channels of data, originating from up to 2 transports. Each channel contains sign, magnitude, and validity data as separate signals. These signals are all continuous (full transparency) and synchronized to the 1 pps and 16 MHz time signals, and are delay-offset according to commands from the control computer. Each channel may be independently offset within the constraints of decoder memory. All signals shall be differential ECL with data rates of 16,8,4,2, or 1 Mbits/sec. The DPS signal output will consist of 3 17-pair flat-ribbon cables with standard 34-pin connectors (one cable each for sign, magnitude, and validity data).
- 16 MHz clock synchronous with data to allow reclocking at correlator - on one cable pair along with data on each ribbon cable.
- Divided clock synchronous with data and 1 pps to allow optional checking at correlator - on one cable pair along with data on each ribbon cable.

Control Interface (Control computer to DPS):
- VLBA command/control interface multi-dropped to all DPS's.

Channel switching:
- Full matrix switching flexibility will be provided in the DPS so that any DPS output can be connected to any playback channel.

Details of the interface timing and electrical specifications will be supplied in a later memo.

Comments on DPS Control Interface

Only a single VLBA monitor/control interface is specified for all functions of the DPS's, including control of data-stream delay offsets.

Low-speed DPS functions such as gross tape manipulation (i.e. load, start, stop, set selectors, etc.) fall naturally within the realm of the VLBA monitor/control bus, and the implementation is straightforward. Control of the data delay offset is also easily managed by the VLBA monitor/control bus provided certain rules are adhered to by both the DPS and the correlator.

The maximum delay rate which must be handled by the DPS/Correlator system is set by the proposal of a dedicated VLBI earth-orbit satellite (dubbed QUASAT), where delay rates to ground-based stations may be as high as approximately 25 microsec/sec, which corresponds to a 1-bit change in delay every 40,000 samples. With a 16 Msample/sec data stream playing back at 16 Ms/s, this translates to a 1-bit change in delay every 2.5 msec of correlator real-time. Commanding individual delay changes to 10 DPS's, each with potentially 16 independent channels, using the monitor/control bus is clearly impossible. However, if a set of polynomial coefficients of a model delay are transmitted to the DPS's at a much more leisurely rate (say every few seconds), the monitor control bus can easily manage the data flow rate. Provided that the correlator/rotator units use exactly the same polynomial model in their delay calculations, everyone is happy. In order for the proposed method of delay update to work, each DPS must have the following capabilites:

1. Each DPS keeps "wall clock" time by observing the 1 pps and periodic (~once/hour) time-critical setting checks with the correlator control computer.
2. Each Track Decoder Module (see Figure 4) has the computational capability to evaluate once/~100msec a 4-term polynomial and its first derivative to determine the initial delay and delay-shift points within a 100 msec window of data. One set of polynomial coefficients is easily able to accurately model the delay over several seconds.
3. The DPS may be commanded to take actions wrt either to wall-clock time or decoded tape time. Specifically, the DPS may be commanded to provide a particular decoded tape time at a specified wall-clock time. Furthermore, a particular delay polynomial may be pre-loaded to become active at a particular decoded tape time.

The method for updating the delay offset from the DPS is then quite straightforward:

1. On correlation initialization, the control computer requests a particular tape time at a specified (future) wall-clock time, and also speicifed a set of polynomial coefficients for the delay for each channel of the DPS. It is the responsibility of the DPS to manipulate the tape in order to honor this request.
2. Once every few seconds, the control computer sends a new set of delay polynomial coefficients to be used starting at a specified wall-clock time or tape time.

Note that the delay update process is asynchronous wrt DPS/Correlator communications, but is completely synchronous and deterministic wrt the delay offsets applied to the data.

The basic method of delay update using a polynomial series is currently being used in the updated Haystack Mark III correlator design and is entirely workable. In the Haystack design, multi-order polynomials for delay, delay rate, and rotator phase are recomputed with 64-bit precision every 2.5 msec using an 80C86 microprocessor.

Details of the DPS control/monitor protocols will be specified in a later memo.