Interoffice Memorandum

CALIFORNIA INSTITUTE OF TECHNOLOGY

To: VLBA Correlator Memo Series   Date: 5 September 1984

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Subject: Microprocessor accumulators

We recognize the problem of how to provide medium- to long-term integration following the correlator's multipliers and short-term integrators and/or prescalers. High-density RAMs are very cheap per bit but are poorly matched in terms of size and access time to our application.

At least two high-speed single chip microprocessors are available that provide a possible compromise. These are the NEC uPD7720 and the TI TMS320 chips. (A higher performance chip, the Fujitsu MB8764, is also becoming available at higher cost.) A brief comparison is given in the following table:

	NEC uPD7720	TI TMS320
cycle time (ns)	250	200
RAM (N x width)	128 x 16	144 x 16
Program ROM	510 x 23	1536 x 16
Data ROM	510 x 13	- -
EPROM version	yes	no (use off-chip memory)
ALU width (bits)	16	32
Multiplier	16 x 16	16 x 16
Parallel I/O width	8	16
Serial I/O channels	1 in, 1 out	- -
Package	28 pin DIP	40 pin DIP
Power (mw)	900 typ.	900 max.
Pricing (Qty)	$210 (100) - 77P20	$83 (100)
	$44 (1000) - 7720	
Mask Charge	$3500 (7720)	?

These chips offer the following features for the correlator application:

A.   They offer 128 (or more) 16-bit accumulators, or 64 32-bit accumulators. Inputs (and outputs) can be multiplexed onto 8 or 16 bit buses, and there is a serial input (e.g.,

for prescaler carry inputs) on the NEC part.

B.   Programmability offers application flexibility and reduces the number of support chips required.

C.   On-chip arithmetic power may be used to implement various signal processing functions, such as up to 64-point FFT or other filtering.

D.   Density is 25 times greater than the best "dumb" accumulator chip (9513), but at a lower input clock rate.

BACK OF THE ENVELOPE DESIGN WITH THE 7720

Many design approaches are possible with the single-chip microprocessors. For the sake of concreteness, I will work out one. This is not meant to be at all optimal; it just shows some possibilities.

Correlator/pre-scaler assumptions:

16 MHz sample rate, 4 levels
Np bits of prescaler
prescaler carries are latched and shifted out bit-serially
every Tl msec

Microprocessor parameters:

Takes input from Nc counters
Accumulates 32-bit sums
Maximum dump rate Fd Hz.
Overflow period Po.

Schematically, we have

```
                                  +----------------------------+
                                  |         \                  |
                          +---+   |          \                 |
   +----------------------+ CRY |SH.|   |                      V
   | Np Prescaler bits |------|   |   |         +---------+
   +----------------------+   |REG|   |         |             |
                          +---+   |         |NEC          |
   +----------------------+ CRY |SH.|   |         |             |
   | Np Prescaler bits |------|   |   |         | 7720 or |
   +----------------------+   |REG|   |         |             |
                          +---+   |         | 77P20       |
                            o     Nc Counters |             |
                            o               |             |
                          +---+   |         +---------+
   +----------------------+ CRY |SH.|   |              |
   | Np Prescaler bits |------|   |   |         8 bits -> |
   +----------------------+   |REG|   |              V
                          +---+   /
                              /                Fringe Proc.
```

The number of counters Nc may not exceed 64, but the actual number depends on Np, the length of the prescaler, and the speed of the 7720. The operations to be performed by the 7720 include

    1. Shift in carries (in groups of 8 or 16) into SI register.
    2. Load DP register (RAM pointer).
    3. If data bit = 0, jump to 6.
    4. Increment RAM(DP), increment DP.
    5. Add carry to RAM(DP), increment DP.
    6. shift accumulator
    7. repeat steps 3-6 for 8 or 16 bit groups
    8. repeat steps 1-7 for all groups

Without a detailed programming analysis, I estimate that each of steps 2-6 is one program cycle, 250 ns. Thus a 16-channel group would take about 80 cycles, 20 us, in the worst case. Step 1 can probably be overlapped with other processing. Allowing for time to read out data and other overheads, perhaps 3 us per counter channel is a conservative time estimate.

If we want to process 64 counters, the overall scanning time would be Tl = 192 us, which requires corresponding accumulation, 3072 counts or Np = 12 bits. This is rather a long "prescaler"; we can reduce the time by reducing the number of counters scanned. (There are other benefits to this approach, since multiple time bins and double buffered I/O become possible.) The possibilities are as follow

Nc No. counters per 7720	Np Required correlator "prescaler", bits
64	12
32	11
16	10

A factor of 2 increase in performance may be possible by avoiding the serial input and using the parallel I/O bus strictly synchronized to the counter shift out. There are problems of handling input and output through the same port. (Correlation may have to be blanked occasionally.) On the other hand, it is possible to read out as many as the 8 high order bits of the counters in parallel. (The required prescaler bits are then reduced to 2 - 4 in the table above.) These are some of the many design options that would have to be considered.

In conclusion, the NEC 7720, TI TMS320, or like processors offer a possible solution to the correlator intermediate and long-term accumulation problem. They may be somewhat slower than we would desire, but they are very adaptable and relatively easy to use.