VLBA CORRELATOR SERIES
VC 029
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VLBA MEMORANDUM

To: M. Ewing

From: B. Rayhrer

On my recent trip to Haystack August 30,84 a lifely discussion took place about DPS/Correlator interface (VLBA MEMO #19) and I like to point to several areas of concern.

1. Time:
   Each DPS will be keeping its own current (wall) time-of-day clock and no tape-time will be available to the host computer. Tape slew is controlled by a command from the host which specifies what tape-time will be at a specified (future) wall-time (2 time time data words to be transferred to each DPS). All of this is done in the interest of releaving the host from as many real-time restriction as possible. It seems unnecessary complicated. What if proper tape-time cannot be reached at the specified wall-time? How early does the host have to issue the command? At what time will the tape leave its last position? If tape-time is not send to the host how does one read tape-time? A command has to exist which sets wall-time at each DPS upon initialization. It seems less complicated if tape-time is send to the host and the host computes an offset (+-xxx millisec. for example) and sends one offset word to each DPS.

2. Interface bit-rate:
   Presently peoposed is a constant 16Mbit/sec. There is disagreement on how lower bitrates for spectral line observations are handled. Options are:

   Oversampling at correlator with recirculation at correlator. Interface rate is constant at 16Mbit/sec.

   Oversampling at DPS with recirculation at correlator. Interface rate is either 16Mbit/sec bursts requiring framing of interface data or variable requiring no framing.

   Oversampling at DPS with recirculation at DPS. Interface rate is constant with framing.

   Oversampling at DPS with no recirculation. Interface rate is either 16Mbit/sec bursts with framing or variable without framing. The correlator would be operated inefficiently for < 16Mbit/sec.

3. Signal interface (DPS to Correlator). Haystack believes that ECL logic levels works well and other means need not be investigated. I'm not convinced as we have experianced serious problems in a MKIII DAT recently. Typical problems can occur from imperfect grounds. ECL provides some protection from common mode signals however my experience shows that even within one rack ground problems can cause this interface to fail. To make matters worse: H.H. proposes to run this interface at 32 Mbits/sec and send magnitude and sign over the same wires. This requires line-receivers with less common mode rejection. If this ECL interface is implemented we need to take extra care in providing proper ground connection to all racks.

4. Control interface (Host to DPS):
   Needs to be defined.

5. Size of decoder memory:
   Needs to be defined.