ACCUMULATORS AND PRESCALERS: REQUIRED NUMBER OF BITS

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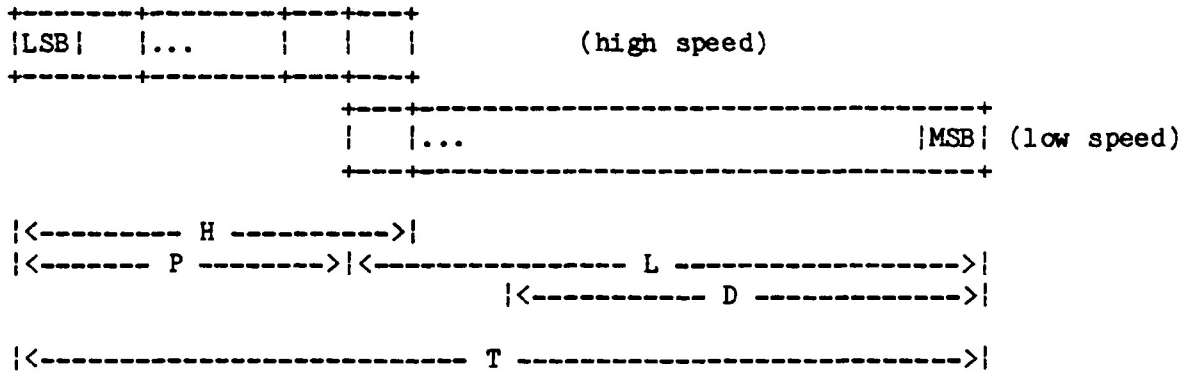
Recent memos (Correlator Memos Nos. 23, 24 and 28) have suggested various possible lengths for an accumulator to be implemented on a VLSI correlator chip, with additional accumulation to be accomplished off-chip in slower circuitry. It is the purpose of this note to point out that there are, in general, three register lengths to be chosen in such a scheme, and that these choices are well determined by specifying the minimum and maximum accumulation times. They are not subject to arbitrary choices by the designer. The relevent formulas are given.

Consider the following figure.



This represents an accumulator of total length T bits, divided into a high-speed part of length H and a low-speed part of length L = T - H + 1. It operates as follows. Every sample time, a multiplier product (generally 3 bits long) is computed and added to (LSB,LSB+1,LSB+2). Periodically, say every k samples, the most significant bit of the high speed accumulator is read, cleared and added to the low speed accumulator. Finally, every n samples or n/k high speed readouts, the most significant D bits of the accumulator are read out for further processing and the entire accumulator is cleared.

This arrangement can be described by three parameters; we shall use T, D, and H.

Total Length, T

The total length T must be sufficient to accomodate the longest allowed accumulation time at the highest sampling rate with a correlation coefficient of unity (it might be argued that, for a cross-correlator, the correlation coefficient will rarely exceed 0.5 or 0.25, and in such cases we could use shorter accumulation times; but here we assume that unity must be accomodated). Then

$$T \geq \text{gif}[\log_2(A_q\ n_{max})] + 1 \qquad (1)$$

where gif[x] is the largest integer not exceeding x; n_{max} is the maximum accumulation time, in sample periods; and A_q depends on the quantization used, as follows:

Quantization Levels, q	A_q	Assumptions
2	0.5	Scale=0.5, offset=0.5 (count = 0,1)
3	0.5407	Threshold=.612, scale=1, offset=1 (0,1,2)
4	1.1044	Thres=.90, wt=3, scale=1/3, offset=3 (0,2,3,4,6)

The multiplier products are scaled and offset as shown in order to allow up-only counting (the usual practice). Actually, the offset does not affect this result; although it will cause the minimum-length accumulator to overflow at high correlation coefficients, no information will be lost.

Output Word Length, D

The number of bits that are retained for further processing, D, is determined by the minimum allowed accumulation time. The roundoff error caused by neglecting the lower T-D bits has a standard deviation of

$$\sigma_r = \frac{2^{T-D}}{\sqrt{12}} \tag{2}$$

This assumes proper rounding of bit $P + 1$; for truncating, σ_r is worse by a factor of 2. The standard deviation due to noise in the original signals (assuming small correlation coefficients) is

$$\sigma_s = C_q \sqrt{n} \tag{3}$$

where $C_2 = 0.5$, $C_3 = .5407$, $C_4 = 1.143$ for 2-, 3-, and 4-level quantization, respectively (same assumptions as earlier). If we insist that $\sigma_r/\sigma_s < .01$ (i.e., 1% extra noise due to roundoff), we find

$$T - D < 0.5 \log_2(n) + \log_2(C_q) - 4.85. \tag{4}$$

The worst case is when $n = n_{min}$, the shortest allowed accumulation time.

High Speed Accumulator Length, H

While the addition of products to the LSBs must proceed at the full sampling rate, the more significant bits of the accumulator change more slowly. Therefore, as is well known, significant economies can be achieved in a large correlator by splitting the accumulator into high-speed and low-speed parts, and implementing

the low speed part in a random access memory shared by many multipliers. This is the main reason for the arrangement described above.

The length of the high speed accumulator is determined by its dump period k:

$$H \geq \text{gif}[\log_2(B_q\ k)] + 1 \qquad (5)$$

where $B_q = A_q$ + offset (1, 1.5407, 4.4044 for our three quantizations). The choice of k is an economic one. Smaller values of k save high speed accumulator bits, which are expensive; but they reduce the number of low speed accumulators which can share a given RAM, increasing the low speed accumulator cost. Evaluation of several trial designs will probably be needed in order to find a reasonable tradeoff.

The choice of k has one other effect. If a recirculating correlator is contemplated (a future option for VLBA), then the recirculator must hold at least k samples, and the minimum accumulation time is at least rk samples, for recirculation factor r. If k is too large, then the recirculator might be too expensive.

The design now separates into two cases: In Case I, which is illustrated in the figure, we have $D \leq L$; this is, the D bits that will finally be dumped are all in the low speed accumulator. In Case II, which arises for sufficiently small minimum accumulation times, we have $D > L$; then some of the output bits must come from the high speed accumulator. Thus, Case II requires that more than the MSB of the high speed accumulator be available for readout. The portion of the high speed accumulator that never needs to be read may be called a "prescaler"; its length is $P = \min(H - 1, T - D)$.

In Case I, another design option might be considered. Clearing the MSB of the high speed accumulator at each readout can be avoided if it is read every k/2 samples and the low speed accumulator is lengthened by one bit. Also, in principle, we should clear all bits of both accumulators after the final readout and before starting the next accumulation period. But if L - D is at least a few bits, the error made by not clearing the high speed accumulator may be neglected.

Implementation Notes

As discussed above, the full accumulator breaks down naturally into three stages: prescaler, high speed counter, and low speed counter. The break between the high speed and low speed counters has been defined here as the point where the dump rate is slow enough to allow many low speed counters to be implemented in a single RAM, thus achieving large cost savings. Each high speed counter must be "hard wired" to its prescaler and multiplier. In some cases, the high speed counter is only one bit long, so it may as well be on the same chip as the prescaler; and since the early stages of the prescaler must work at the same rate as the multiplier, they should be on the same chip as the multiplier. However, since the counter and the later stages of prescaler (if any) run more slowly than the multiplier, consideration should be given to placing them on a separate chip, especially if the speed difference implies that a different logic family should be chosen. In this regard, consideration must be given to whether it is acceptable to stop accumulating briefly in order for each high speed readout to occur. If not, so that the readout must occur in one sample period, then all stages of the high speed counter must be as fast as the multiplier.

Possible VLBA Values

It has been suggested (Benson, VLBA Memo No. 384) that accumulation times as low as 0.1 sec. may be used. We can reasonably assume that a maximum accumulation time of 10 sec. will be adequate. In the worst case, the minimum time is required at the minimum sampling rate (0.5 MHz, assuming 4 times Nyguist sampling of .0625 MHz bandwidth) and the maximum time at the maximum rate (16 MHz); then

$$n_{min} = 5 \times 10^4 \quad \rightarrow \text{(eqn. 4)} \quad T - D \leq 2 \text{ bits}$$

$$n_{max} = 1.6 \times 10^6 \quad \rightarrow \text{(eqn. 1)} \quad T \geq 28 \text{ bits}$$

The first result above implies that essentially no prescaling is allowed (even one of the three bits associated with the multiplier must be saved!). Therefore, it seems that this minimum time specification is too stringent; consider instead letting it be 1 sec. at 0.5 MHz, and shorter at faster sampling rates. Then 0.125 sec. is available at $\geq$ 4 MHz and .03125 at 16 MHz. This leads to

$$n_{min} = 5 \times 10^5 \quad \rightarrow \quad T - D \leq 3.6 \text{ bits.}$$

If we accept slightly more roundoff noise, then a 4-bit prescaler (1 bit beyond the multiplier register) is allowed.

Now consider the high speed dump period k and the corresponding high speed accumulator length H. It is reasonable to assume that the low speed accumulators will use an adder, RAM, and controller which can achieve a cycle time (read-add-write) of 250 nsec. Since 2048 x 8 chips are common and convenient, we assume a 2048 word RAM. (Fortunately, this corresponds to one baseline for the VLBA.) Then each accumulator can be updated every 512 μsec, which becomes the minimum high speed dump period; this is 8192 samples at 16 MHz, or H = 14 bits. With $P = 4$, we must be able to read out 10 of these bits. This also

gives a reasonable recirculator size (8192 samples) and does not constrain the minimum accumulation time for reasonable recirculation factors.

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