Interoffice Memorandum
CALIFORNIA INSTITUTE OF TECHNOLOGY

TO: VLBA correlator group DATE: 30 April 1985

FROM: Dave Fort and Steve Kator SUBJECT: ECA input connections

The Architecture Report shows each ECA receiving A and B bundles of 20 stations (pages 22-23). This note is the result of thinking about how to route these 160 signals to the VLSI correlator chips to acheive 10/14/20 station operation in a reasonable way at a reasonable cost. An efficient method of making these connections will influence the design of the correlator chip and hence, should be decided early on.

The fewest number of VLSI correlator chips in the system is acheived by organizing the correlator as a square array of 8-lag chips. The saving results because no chips are wasted in obtaining the negative lags of the autocorrelation function. For example, a 20 station square system requires 400 chips while a 20 station triangular array requires 440 chips. The total VLSI cost difference is $40K. For purposes of comparison the square array will be assummed and EC (elementary correlator) will mean one 8-lag chip.

Because the ECA contains 400 or more 68 pin VLSI packages plus adders and filters, it will probably have to be composed of at least a dozen boards (hopefully in one chassis) with about 40 ECs per board. If each EC is individually connected to 3 A stations and 3 B stations (for 10/14/20 modes) then the board will need 760 signal inputs and the backplane will need over 9000 individual wires to be connected. Neither of these possibilities is reasonable and therefore a method to reduce the number of different signals going to each board must be found.

The only way of reducing the number of different input signals is to have a number of ECs being fed the same signal. The natural way to do this in a correlator is to divide the ECA into a number of MXN blocks so that only M+N stations need to be fed to the block for each mode (each column gets one A station and each row gets one B station). The main restrictions on M and N are that 10/14/20 station modes must be accommodated and that 4/2/1 ECs respectively must be concatenated for the spectral line mode.

If the block size were chosen to be 4X5, two blocks to a board, then each board would need 216 signal inputs and the backplane would need 2400 wires. Actually, because the 10 and 20 station modes could use the same inputs if they are arranged properly the numbers are 144 signal inputs/board and 1600 backplane wires. A scheme of this sort requires 420 ECs on 11 boards (with one block unpopulated) adding $20K to the total VLSI cost. The number of inputs and backplane wires is still uncomfortably large.

More improvement could be obtained if the block size were chosen to be 4X4, two blocks to a board, and the 14 station mode were changed to a 15 station mode. This can be done by adding two ECs to each block

so that it can be converted to a 3X3 double lag arrangement. Now 10, 15 and 20 station modes can use the same 8 stations per block. This scheme requires 64 signal inputs and 800 backplane wires. Unfortunately, it also requires 450 ECs on 13 boards (with one block unpopulated) adding $50K to the total VLSI cost (minus the value of a 15 instead of 14 station mode).

Although the number of signal inputs to each card in the above schemes is not too large, the number of discrete backplane connections (13000 for 16 ECAs) is still very worrying. This has prompted us to consider a system where the A and B signals are bussed along the backplane (a PC board) and each board is capable of selecting any M stations from the A bus and any N stations from the B bus. If the block size is taken to be 4X4, two per board, then there will be 64 input signals per block and no individual backplane wires. All station modes can be done with 400 ECs, on 13 boards (with one block unpopulated), saving $50K over the non-switched 4X4 scheme.

To realize this arrangement will probably require the design of another VLSI gate array chip (unless a suitable commercial chip is found). A preliminary design shows that an 8 of 24 switch will fit on an 880 gate array and in a 68 pin PLCC package. The design cost would be about $21K plus in-house design time and the production cost would be $10 per chip (we need 1664). Therefore, the additional cost of this approach would be about $40K. Although $40K is only marginally cheaper than the hard-wired approach, it does save the cost and complexity of 13000 individual wires.

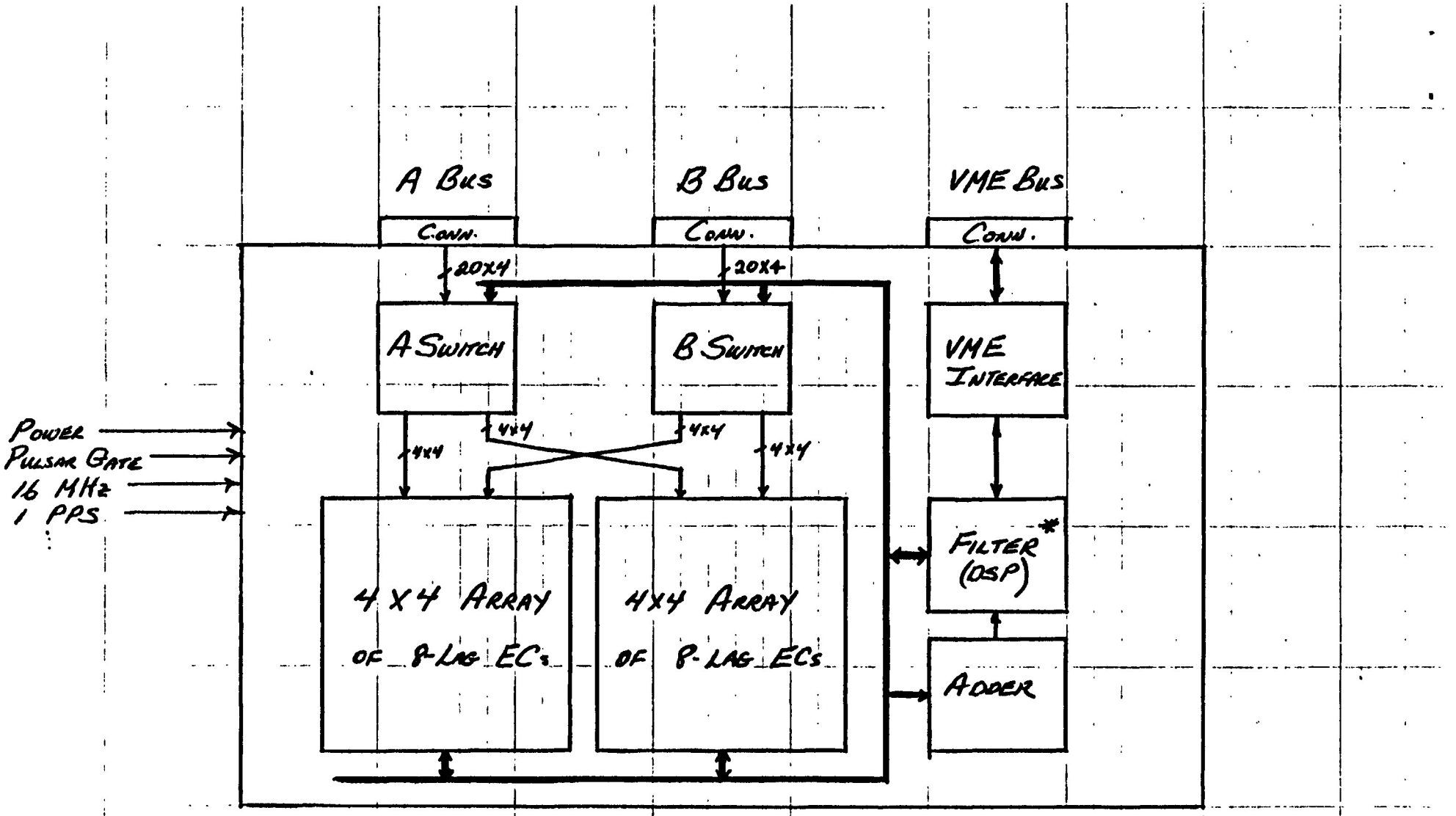
There are a number of other advantages to this approach:

(a) Allows self-test and self-heal on the fly if one populates the unpopulated block and switches it in parallel with the other 25 blocks in some sequence.

(b) Gains gate array design experience on a relatively simple chip.

(c) The chip can be used to advantage elsewhere, i.e. in the station crossbar and perhaps in the channel crossbar.

In summary, we recommend that an electronic switch be employed in distributing the ECA input data.



CORRELATOR CARD (13 per ECA)

* The Filter may reside on other boards