California Institute of Technology
VLBA Correlator Memorandum

To: VLBA Correlator Group 6 June 1985
From: Martin Ewing
Subject: Meeting with Austek, 6 June

Attending: Rob Clarke, Manager Product Development, Bruce Nelson, VP Software Technology, and Craig Forest (all from Austek), with Ewing, Fort, Kator, Pearson, and Seling.

Austek presented their company and its technical capabilities. They are interested in upper-scale "value added" applications for VLSI. This is our case - we are interested in providing a high-performance system rather than trimming off a few cents of the production cost of a commercial product. They see their particular contribution to be their ability to understand their clients' systems needs and to interact at the system architecture level. This is to be contrasted to the typical gate-array houses, who are really only able to turn a (very elegant) crank given a very specific design.

Austek's processes are 2μ HMOS (nMOS) or 2.5μ CMOS; their technique is based on "macrocells" which may be laid out arbitrarily across the die. Effective density is between that of "standard cell" and "full custom" approaches. They own a part interest in VTI, a US silicon foundry, which guarantees them rapid turnaround. They routinely go from "data" to prototypes in two months. Most of their business is in the US. They are accessible through electronic mail, e.g., ARPAnet.

Clarke presented a proposal to upgrade the AT "XCELL" design to operate at a 16 MHz clock rate with parallel (not serial) 2-bit sample input and with input "validity" (blanking) bits. This might make the chip "twice" as good for the VLBA compared with our earlier estimates of how we would have to operate the chip (e.g., at a 8 Msample/s rate). However the matrix input connections of the AT chip are maintained. A copy of the proposal will be available from the VLBA Project Office.

A long discussion ensued concerning the most desireable chip design from the VLBA viewpoint. It became clear that the bulk of the AT chip, which is in the multiplier/accumulators, would be readily transferred to a

new VLBA design. VLBA, however, needs a more convenient input connection scheme, along with vernier delay, fringe rotation, and "P bit" decoding at the front end. Austek will think about this and probably will come back with a revised technical proposal for this new chip. Off-hand estimates indicated that the total Austek price would likely be lower than our current estimates based on LSI Logic's 2μ CMOS gate arrays. They base this on achieving 32 complex lags on a chip with 8-bit prescaling and 16-bit accumulation, more than twice what we expect from the gate array.