California Institute of Technology
VLBA Correlator Memorandum

To: VLBA Correlator Group 10 July 1985
From: Martin Ewing MSE
Subject: Pulsar Window Generator (revised)

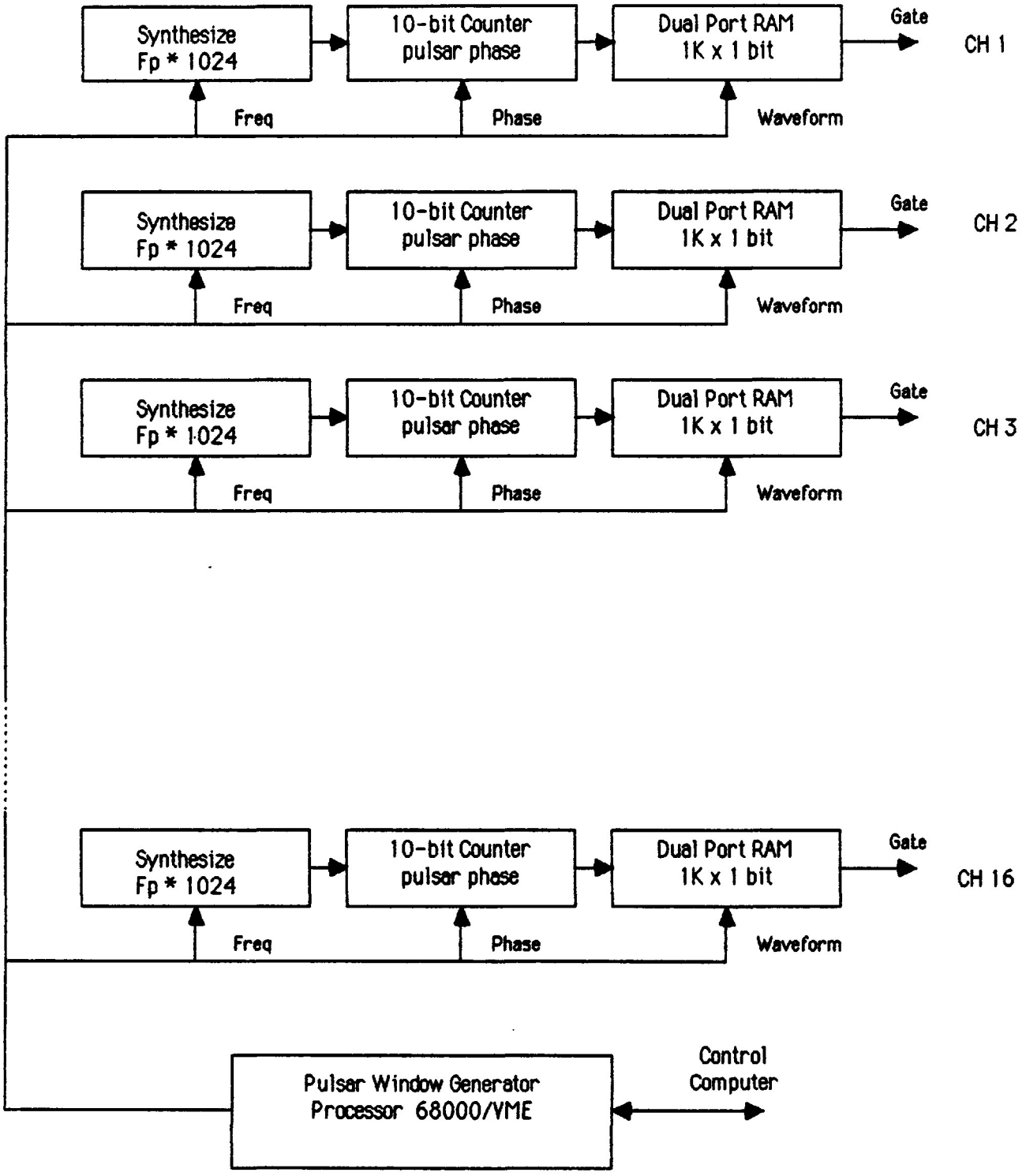
Attached is a preliminary design for the Pulsar Window Generator (PWG). It is based on a Fringe Rate Generator (FRG) chip. It is very likely that any chip used for VLBA fringe rotation will be suitable in the pulsar application. For concreteness, I employ the JPL FRG gate array design in the following.

It meets the specs of the Architecture report with the exception of the size of the window for high frequency pulsars. The report specifies windows as small as 0.1% of the pulse period all the way down to a period of 100 μs, implying a 10 MHz clock. This is rather impractical for the present approach, since the FRG clock is 2 MHz. It would provide 1K bins (~0.1%) across any pulse period ≥ 1 ms. The bins are represented in a 1Kx1 RAM, each bit representing on/off for a particular bin. Thus, arbitrary pulse "waveforms" may be accomodated to 0.1% resolution.

It is a simple matter to look at a 125 μs pulsar with 1% bins – just replicate the desired waveform 8 times in RAM. The tradeoff between period and resolution is flexible.

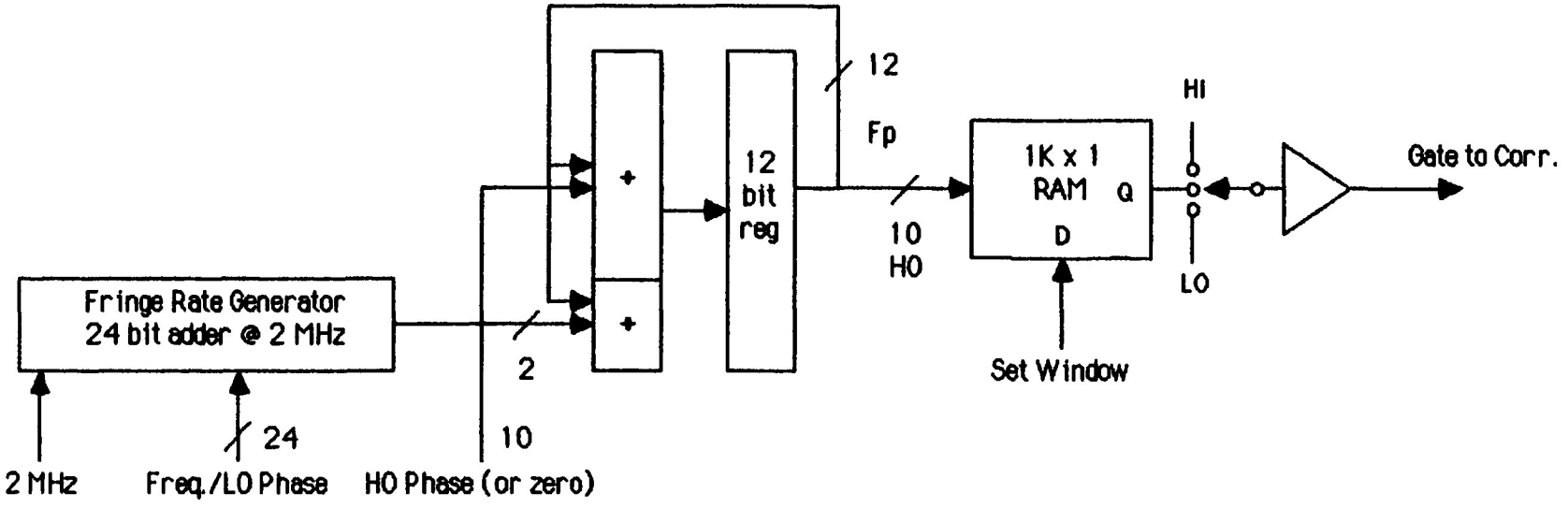
The JPL FRG chip has 24 bits of setting precision. At a 1 kHz maximum rate, the pulse phase might slip one bin in 16.7 seconds. The 68000 controller could update the FRGs and the phase registers every 1-10 seconds with parameters supplied by the control computer no more often than once every 30 sec–the specified interval. The PWG controller would be only lightly loaded at such a rate.

The preliminary cost estimate shows a hardware cost of under $10K, but about 7 work-months of labor, bringing the total effective (burdened) cost up to ~$50K.



Pulsar Window Generator

MSE 5/85



Pulsar Window Generator
One Channel Detail

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Pulsar Window Generator

7/10/85 mse	Qty/ch	Quant. Total	Price each	Total Price
Fringe Rate Generator	1	16	65	1040
Parameter Latch	3	48	2	96
12-bit adder	3	48	1	48
12-bit register	2	32	1	32
1K x 1 RAM	1	16	1	16
2:1 MUX	0.25	4	1	4
Line Driver	0.25	4	1	4
		=====		========
Subtotal Number, ICs		168		
Subtotal Price, ICs				1240
Ctrl logic, addr decode		6	1	6
Bus Interface		10	1	10
		=====		========
Total Number, ICs		184		
Total Price, ICs				1256
Wire wrapping		1000	0.15	150
Wire wrap board		8	150	1200
68000 Single Board Comp		1	2000	2000
VME Backplane & Power Supply		1	1500	1500
				========
Total Price, non-IC				4850
Total Price, Materials & Services				6106

LABOR (work-months)	ENGR	TECH
Design	1.0	
Wire Lists	0.7	0.7
Chassis Fabrication		0.4
Checkout	1.0	0.5
Software	1.5	
Documentation	0.7	0.7
	=======	=======
TOTAL	4.9	2.3