VLBA Correlator Memo No. 57

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To: Correlator Group
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Subject: XCELL Tricks - 4 bit multiplication

For some proposed LBA/VLBI correlator schemes it would be very useful to have more than 2-bit correlation, even though data is only sampled and recorded with 2-bit resolution. In particular, losses due to fringe rotation or DFT operations in the correlator can be significantly reduced by using more than two bits.

At first glance we might say that since XCELL has a 2-bit mode, we need only split samples into high- and low-order parts and multiply them separately in four multipliers. Unfortunately, things are not quite so simple, since the XCELL treats 2-bit data as an "unnatural" code, optimised for 2-bit sampling of gaussian data. From the Austek Chip Specification AU85401, AU85402, the multiplication table is

2-bit Multiplication in XCELL

		X Input			
		11	10	00	01
Y Input	11	+16	+4	-4	-16
	10	+4	+1	-1	-4
	00	-4	-1	+1	+4
	01	-16	-4	+4	+16

We see that the bits are interpreted in the following manner:

MSB	LSB
Sign	Magnitude (high/low)

Interpretation of Sample Bits

"High" Magnitude = 4
"Low" Magnitude = 1

There are many ways of combining such peculiarly weighted values to represent a higher precision sample. Natural weighting (1,2,4,...) is not possible, however. I have worked out a few simple schemes. Note that any scheme is useable in principle; the question is how to use the available hardware to achieve the best signal-to-noise ratio.

Scheme 1. Note that two 2-bit XCELL samples u and v can take the values

$$u = \pm(4,1)$$
$$v = \pm(4,1)$$

We can form a higher precision quantity w by combining u and v:

$$w = u\times 4 + v$$

This variable can take on the values

$$w = \pm(16,4)\pm(4,1) = \pm(20,17,15,12,8,5,3,0)$$

and the product of

$$w = u\times 4 + v$$

and

$$w' = u'\times 4 + v'$$

is

$$w\times w' = u\times u'-16 + (u\times v' + v\times u')\times 4 + v\times v'$$

The products can be formed in four XCELL multipliers (of the 64 on chip) with the accumulations added together in firmware or software with the indicated weighting.

This multiplication scheme has the useful advantage of including a zero state. (In fact there are two.) This provides a natural way to inhibit correlation due to invalid data arising from tape errors or pulsar gating.

Scheme 2. The relative weighting of u and v can be adjusted in various ways. We may take

$$w = u\times 2 + v$$

for example. Then w takes the values

$$w = \pm(12,9,7,6,4,3,2,1)$$

This scheme might have some value if the distribution of states should be uniform in the sense of naturally weighted 4-bit samples. It does not include a zero, however.

Scheme 3. Another possible weighting is

$$w = u\times 8 + v$$

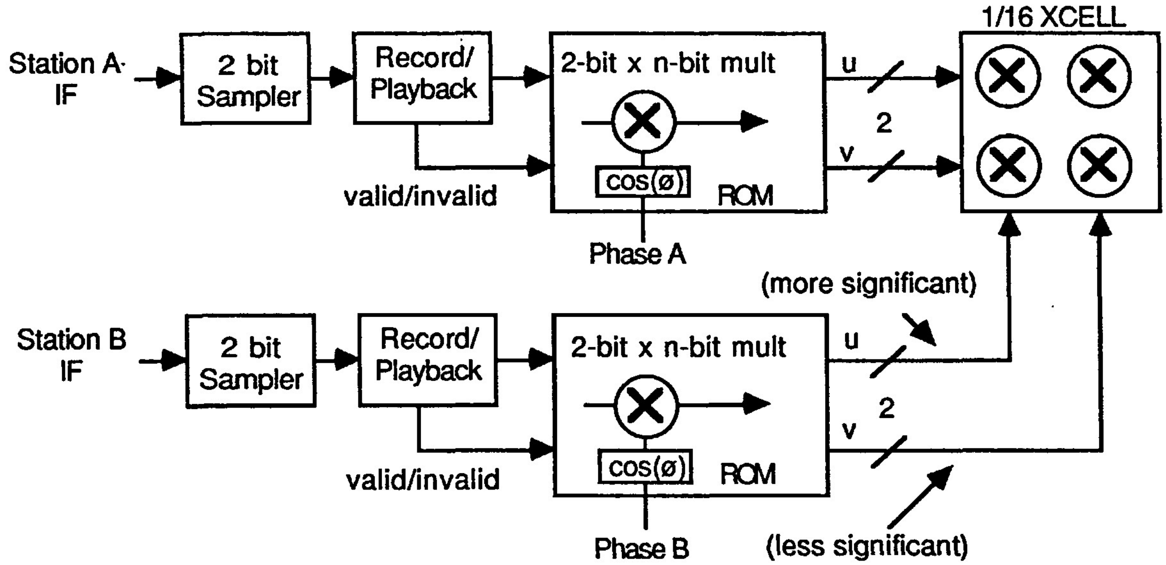
yielding the values

$$w = \pm(36,33,31,28,12,9,7,4)$$

The states are bunched at high and low magnitudes and do not include zero. Higher weighting of u vs v will increase the bunching.

Fractional weightings are also possible, but have not been investigated. It is possible that an optimum weighting would be non-integral, but it would not include the zero, which may be quite valuable for VLBI applications.

Typical Application. A correlator with digital (post-sampling) phase rotation in both data streams is the typical case in which a high-precision multiplication is desired. Consider the following figure:



Typical Application

The figure shows two VLBI IF channels sampled at 2-bit resolution, recorded and played back, and then transformed by multiplication against a "digital LO" controlled by an external phase generator. The cosine table and multiplication are conveniently implemented in ROM, allowing any of the multiple precision schemes described above. The u and v outputs are each 2-bit sample streams as far as the XCELL multiplier inputs are concerned.

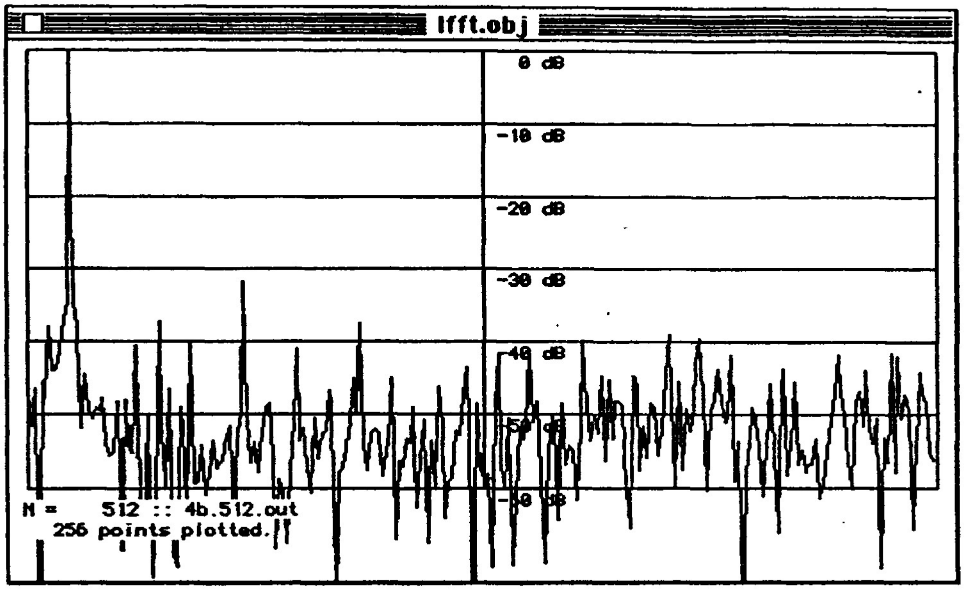
In a practical case, we note that the 2 bits of each XCELL input must be read in serially. Also, there would be both cosine and sine multipliers for each channel, and a complex correlation; these refinements do not alter the present analysis.

SNR Losses and Spurious Products. The primary reason for seeking to implement 4-bit multiplication is to avoid the losses and other problems associated with low-precision digital lobe rotation. A "standard" 3-level lobe rotation incurrs approximately 4% SNR loss, and two such rotators, one in each signal path, would be expected to double the loss. In addition, one must worry about the many possible intermodulation products between harmonics of the two digital LOs, especially when there may be strong monochromatic signals in the passband, e.g., phase calibrator signals.

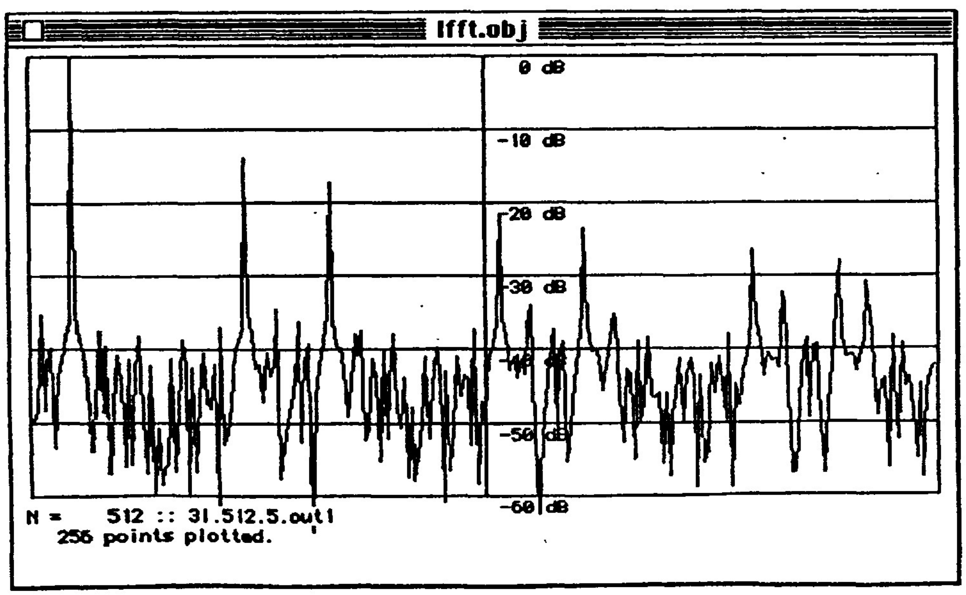
A complete analysis of the best achievable SNR in an application like that described above seems difficult. There are many adjustable parameters, including the sampler thresholds, the LO (sin/cos) quantisation, and the relative weightings of the partial multiplication products.

As a simple verification that 4-bit sampling can be quite good, I have quantised a "typical" sine wave according to the levels of "Scheme 1" above. This is used as input to an FFT routine calculating the log power spectrum (a). The result is presented below along with the same analysis for a 3-level waveform (b) where the quantisation threshold was set at 0.5 times the peak value.

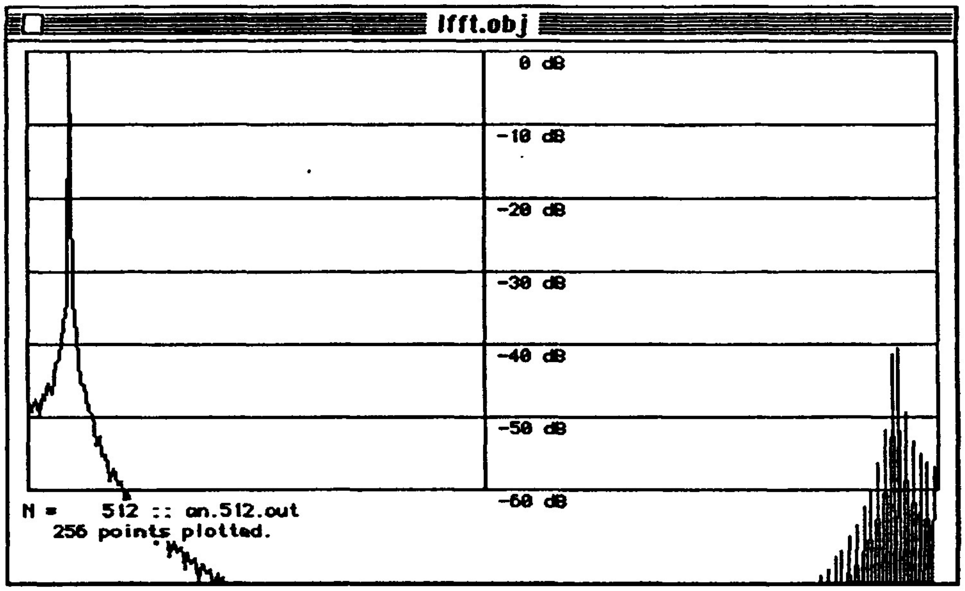
The 512-point FFT was performed with 80-bit IEEE floating point. Results of "80-bit" quantisation (essentially analog) data are shown in (c). The fact that the highest spurious peak in (a) is below -30 dB suggests that losses due to a single "Scheme 1" quantisation may be less than approximately 0.1%. More careful study is needed.



(a) Spectrum of 4-bit quantised sine wave.



(b) Spectrum of 3-level quantised sine wave.



(c) Spectrum of IEEE floating point sine wave.