VLBA Correlator Memo No. 75

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CSIRO Division of Radiophysics
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To: VLBA Correlator Memo Series

From: Martin Ewing

Subj: CSIRO/Austek FFT Chip

Attached are two memos by John O'Sullivan of CSIRO Radiophysics describing the new FFT chip. which is now in the final design stage at CSIRO. It is expected that this chip and a companion general microprocessor-oriented interface chip would be produced by Austek.

The memo of 1 April gives the general specifications. For VLBA use. the most relevant features are the 256 point FFT length with a 1.25 MHz sample rate. With a suitable front end (e.g., a 32 point FFT or a set of FIFOs), 32 of these chips could handle a VLBA data stream. yielding up to 8K frequency channels. The FFT is largely self-contained (RAM included), and the word length (16 - 24 bits) is certainly great enough. Depending on the market, one might guess that the chips would cost around $200 each.

John's second memo (2 May) indicates various additional applications that could make use of multiple chips in parallel or tandem. I estimate that the 2D FFT speed quoted is roughly three times the Convex C-1.

Serial FFT Chip
J. O'Sullivan
1-4-86

1.0 SPECIFICATIONS

A chip capable of performing a Fast Fourier Transform at sufficient rate would find many applicationsin the areas of speech and image processing or indeed any area where Fourier transforms or convolutions of two sequences are required. The original specifications are based on the requirements of high quality speech processing. The current specifications are determined in part by the need to demonstrate a clear advantage over signal processing chips such as the TMS32020. in part by the limitations of a3μ HMOS process and in part by applications in image and signal processing.

The chip will perform FFTs on complex or real data and input to the chip is in bit and word serial form continuously. The Fourier transformed data will appear also in bit and word serial form after a delay corresponding to a number of samples or words yet to be determined, but approximately equal to the transform length. Successive transforms are performed repetitively.

The basic parameters are;

1. Maximum Sample rate (16 bit) = 1.25 MHz, (complex samples)
2. Maximum Bit rate = 20 MHz
3. Maximum FFT length for single chip = 256. FFT lengths of 128, 64, ..., 2 selectable (for a 3μ HMOS process).
4. 256 point transform time = 0.2 msec
5. 16 or 24 bit arithmetic (selectable).
6. Control of scaling after every two radix-2 passes.
7. The following types of FFT are to be performed
    1. Complex - complex
    2. Real - complex

3. Complex - real

In addition the desire is that the chips will be cascadable to achieve longer lengths, or to produce outputs in normal order. These requirements for great flexibility in length and FFT type may prove too difficult to implement in practice and are to be viewed at present as a goal.

Properties such as transform length are directly influenced by the process available. Extension to longer transforms or greater arithmetic precision is trivial.

Possible applications lie at the high speed end of the capabilities of existing or projected DSP chips. The FFT chip outperforms the recently anounced Motorola DSP56000 by a factor of four. Specific applications include;

1. High speed spectral analyser for bandwidths up to 625 KHz.

2. High speed convolver for radar signal processing.

3. Add on image enhancement processor for Sun-type work stations aimed at remote sensing and astronomical users.

Serial FFT Chip
J. O'Sullivan
2-5-86

1.0 MULTIPLE CHIP APPLICATIONS

A number of demanding processing applications in radar, astronomical signal processing, sonar signal processing will require far higher processing rates than can be achieved by a single chip. In particular, high bandwidth radar applications and image processing at or near television frame rates might be named. For such applications it is necessary to provide the capability to cascade or to parallel multiple FFT chips.

It is anticipated that many the necessary hooks and algorithms can be placed on chip (some concessions have been made in the basic architecture with this in mind).

Given evidence of a market, auxilliary chips could be developed to aid the combination of multiple chips. The aim would be to produce a chip set capable of, for example, high speed two 2D Fast Fourier Transforms with perhaps only external image memory chips. A 256x256 point transform could be executed at 50 ms throughput rate with a pair of chips. Proportional reductions in processing time would be achieved with an increase in the number of transform chips.