VLBA Correlator Memo No. 90

(870929)

Correlator Operational Cycles Including the Integration Cycle and Self Test

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I) Introduction

This memo will describe the major operational cycles of the VLBA correlator. The cycles discussed include the FFT cycle, the fractional sample error correction update cycle, the delay update cycle, the fringe rate update cycle, the integration cycle and the self test cycle.

II) The FFT Cycle

The shortest operational cycle to be applied in the VLBA correlator will be the FFT cycle which will be 1028 32-Mhz clock periods in duration and consists of 1024 clock periods to fill the RAMs onboard the butterfly chips with 1024 samples and a 4 clock period pause.

In operation, the FX correlator will perform Fourier transforms of from 64 points to 2048 points in length. The transform length, however, will not effect the FFT cycle duration. The plan for the FX correlator is to always load 1024 samples into the input buffers of the FFT engines and to perform as many transforms as can be done on these samples. The transform length will be determined by how many butterfly stages are active in each FFT engine. (Transforms of 2048 points in length will be performed by using two FFT engines, each processing 1024 of the 2048 total points, with a point shuffle at the input to the last butterfly stage.)

The four bit pause after each FFT engine buffer has been filled will provide time for bank switching in the butterfly chip (two 1K buffers exist on each butterfly chip and they will be used to double buffer input samples to be transformed). No samples will be discarded as a result of this pause since the delay system RAMs can buffer the data through the pause interval. After the 4-bit pause, the system will start loading the FFT engine with samples that are contiguous to the samples loaded during the previous FFT cycle.

The FFT cycle will also be used for the update time for the fractional sample error correction parameters. The fractional sample phase is tracked using the delay model generator. Periodically, the sample time error of a given sampler will be down loaded to the fractional sample error correction circuitry

at the output of the FFT logic. The error parameter that is to be used by the correction logic will have 8-bit accuracy. Since the maximum delay change rate that the VLBA correlator must follow is set at 50 samples per second, the fractional sample error parameter must be updated at a rate of at least 256 times this maximum delay rate to have LSB accuracy. An update rate of at least once every 2500 samples is thus required.

III) The Fringe Model/Delay Change Cycle

The next operational cycle in the FX correlator to be considered is the 4-msec fringe model update cycle. The short term station fringe tracking will use a two coefficient Taylor series expansion, the two coefficients used being an initial fringe phase and the rate of change of the fringe phase. This simple station fringe tracker will track fringe phases to the required accuracy for about 4-msec and after that time must be updated with new coefficients by the fringe model generator.

The actual period of this cycle will be 126 FFT cycles which will include 125 active FFT cycles in which station samples are transformed and one FFT cycle duration pause to accomplish any reconfiguration required by the fringe update. Again, the pause will not introduce any observational inefficiency and the buffering action of the delay line will allow adjacent transforms across fringe cycle boundaries to be performed on contiguous samples in the playback data.

The delay programmed by the delay line will be updated at the start of each fringe model cycle. This update rate is higher that needed to meet the 50 bit per second delay change requirement but the fringe model cycle is a natural time in which to change the delay.

IV) Accumulator Cycle

The next cycle of the FX correlator to be considered here is the accumulator cycle. This cycle will be 3152 FFT cycles in length (25 fringe model cycles) and will include 3125 active Fourier transform cycles. A pause of two 1028 clock cycles will occur at the end of each accumulator cycle. The 3125 active Fourier transform cycles executed during one accumulation cycle will establish the minimum integration time of the correlator as being 100 msec (for 32 Mbs sampling).

Short term accumulation of cross- and auto-spectra will be done in the RAM storage of the butterfly chip. The complex multiply portion of this ASIC (Application Specific Integrated Circuit) will be used as the FX cross multiplier and the butterfly adder stages will be used as the floating point accumulator. The idea is to use the 1024 X 36 RAM onboard the butterfly chip to keep intermediate partial sums in a complex,

floating point format. The 36-bit wide RAM and the ASIC adder and scaling stages can permit operation with complex numbers having 15-bit real and imaginary mantissa resolutions with a common 6-bit exponent field.

The short term accumulator cycle described above will require that the accumulator support integrations of 3125 active FFT cycles before being dumped. This requirement implies that each term will be the sum of up to 3125 cross products. The numbers input to the cross multiplier will be 4-bit fractional numbers (actually they will be complex floating point numbers with 4-bit real and 4-bit imaginary components of the form S.XXX with a common 4-bit negative exponent). Thus the largest resulting complex cross product component that need be accumulated will be

$$(+.111)*(+.111) + (+.000)*(+.000) = (+.110001).$$

Cases where the FFT output can assume larger magnitudes such as the maximum value of .111 + j.111 need not be considered. If the scaling in the FFT engine were such that a complex output with this magnitude would be allowed, peak clipping would occur for points of this same magnitude but with phase angles like zero degrees (the exact form would have to be 1.10 + j.000, which cannot be expressed with a negative exponent).

Taken 3125 times, a cross multiplier output of .110001 would result in an accumulated value of (to 15 bits)

+ 1001 0101 1000.10

which represents an overflow condition in the sense that the last +.110001 term added to this result would have its 4 least significant bits shifted out of the 15-bit field of the adder and hence it would be truncated. If this level of overflow is not acceptable, a shorter accumulator cycle time will have to be used.

As noted above, the accumulator dump cycle will consist of 3150 FFT cycles followed by a pause the duration of two FFT cycles (2056 clock periods). This long pause will allow for the accumulator bank switch and for a self test integration to be made. Again, however, the delay buffer will ride the input data through the processing pause and no data will be lost.

V) Self Test

The pause at the end of each accumulator cycle will be used to perform self test integrations. At the start of each accumulator cycle pause, a pseudo-random data pattern 1024 samples in length will be loaded into all FFT engines and transformed. The resulting transform outputs will be cross

multiplied and stored in an empty accumulator buffer (since accumulator bank switch takes place at the end of an accumulation cycle, one of the two short term accumulator RAM banks will be free).

The idea is to allow the system to test itself every 100 msec on a non-interfere basis, i.e., the self test will be transparent to normal signal processing and will result in no loss of sensitivity. Self test at this level will occur automatically with no action required by the observer or the computer system other than to be aware of self test failures.

Each 100 msec, self test will test the entire FFT system, the cross-multipliers and 1/512th of the accumulator. By reading, and testing against a predicted value, one of the 512 terms in each baseline cross (or auto) product that results from the self test integration, it will take 51.2 seconds to test the entire cross multiplier/short term accumulator system (actually twice that to test both banks of the short term accumulator storage RAM).

An additional stage of self test will occur during otherwise dead intervals such as at the end of a tape pass or during source changes. This test would verify the entire system by using a pseudo-random data generator to supply input drive to the correlator at the playback interface input to the system and would be run upon command from the computer. The test will consist of a full 100 msec integration on the data generator output with the results of the integration being tested against predicted results. This more comprehensive albeit less frequent test will verify all of the interface, delay, FFT, cross multiplier, and short term accumulator. In addition, the mode setup will be tested since the pseudo random test signal will flow through the system as configured for the observation being processed.

VI) Timing

The data playback system will supply digital information to the correlator system at a constant bit rate of slightly above 9.0 Mbs. After the parity and frame header bits have been stripped from the recorder output, the bit rate of the astronomical data that is to be processed by the correlator should be exactly 8.000 Mbs. The correlator system clock rate that is required to keep up with this data rate and to provide for all of the pause intervals to be programmed into the correlator operation is;

$$(8 * 4)*(3152 * 1028) / (3125 * 1024)$$

since in each accumulator cycle there will be 3125 FFT cycles that process 1024 bits of astronomical data each within 3152 FFT

cycles of 1028 clock intervals each. The 8 * 4 term in the equation above is the 8 Mbs track bit rate, after overhead, times the maximum factor of one sampler bit stream being dispersed into 4 recorder tracks. A correlator system clock of 32.402556 Mhz is thus required.

It should be kept in mind that the FX correlator is a pipelined system. Thus an operation described above as if it were discrete and system wide is in actuality a distributed event. For example, the self test transform performed every accumulation cycle does not occur during a single 1028 clock interval. Instead the elapsed time between the initial 1024 clock interval when pseudo random data is loaded into the first butterfly stage input buffer until the transform and cross multiplication is complete and ready to be read and checked will be a number of FFT cycles.