VLBA Acquisition Memo # 20

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To: VLBA Correlator and Recorder Group
From: Haystack Group
Subject: Update on suggested DPS/Correlator Interface

This memo reflects a slight revision of the interface proposed in VLBA Acquisition Memo #19. The areas of change are in boldface. Usage of the word "channel" conforms to the definition stated in VLBA Acquisition Memo #11.

DPS/Correlator Interface
The DPS/Correlator interface carries the following signals:

Timing Interface:
- 1 pps and 16 MHz provided to both correlator and DPS's from a master clock. Signals provided on differential ECL lines.

Signal Interface (DPS to Correlator):
- **16 output channels, where each channel contains sign, magnitude, and validity data as separate signals.** These signals are all continuous (full transparency) and synchronized to the 1 pps and 16 MHz time signals, and are delay-offset according to commands from the control computer. Each channel may be independently offset within the constraints of decoder memory. All signals shall be differential ECL with **a data rate of 16 Mbits/sec** on each signal line. The DPS signal output will consist of 3 17-pair flat-ribbon cables with standard 34-pin connectors (one cable each for sign, magnitude, and validity data).
- 16 MHz clock synchoronous with data to allow reclocking at correlator - on one cable pair along with data on each ribbon cable.
- Divided clock synchronous with data and 1 pps to allow optional checking at correlator - on one cable pair along with data on each ribbon cable.

Control Interface (Control computer to DPS):
- VLBA command/control interface multi-dropped to all DPS's (see VLBA Acquisition Memo #19 for further discussion.)

Channel switching:
- Full 16x16 matrix switching will be provided in the DPS so that any of the 16 DPS output channels can be connected to any recorded channel.

Details of the interface timing and electrical specifications will be supplied in a later memo.