ACROSS TRACK PARITY

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VLBA data formats using along track CRCC codes for error detection will require fairly good raw recorder performance to guarantee that the VLBA fraction of data flagged invalid spec be met, e.g. for a (172,160) CRCC code the bit error rate per track must be < 6.E-5.

In the interest of increasing the operating range of these codes along track error correction was considered. However, the bursty nature of along track errors makes this form of error correction ineffective unless implemented along with high order interleaving.

Since across track errors are expected to be independent, across track error correction was considered next. An across track Reed-Solomon code was described and analysed by G.S. Wilson in VLBA Acquisition Memo #26. It was rejected as a possibility for the VLBA on four grounds:

1. Loss of track modularity.

2. Complexity.

3. Unknown impact on the rest of the system.

4. Loss of efficiency when 16 or fewer data tracks are recorded per pass.

Another simpler form of error correction using a synthesis of across track parity and along track CRCC error detection is proposed here. It maintains many of the advantages of the across track Reed-Solomon code but has fewer disadvantages. For example:

1. LOSS OF TRACK MODULARITY. In retrospect track modularity should perhaps receive less emphasis than previously thought in the VLBA DAS/DPS design since it has already been partially sacrificed to allow dynamic channel to track assignment.

2. COMPLEXITY. Since data must alread be brought together and synchronized for the channel-track matrix it is a simple matter to generate and detect across track parity at the same time.

3. IMPACT ON REST OF SYSTEM. Extra signal paths and switching will be required to handle the across track parity bits. However the generation and detection of along track CRCC code words is no more difficult for these extra signals than for the data tracks used in simple along track CRCC error detection. As in CRCC along track error detection FIFO's will be required to store data while syndromes are generated and ROM's will be required to decode data and generate flag bits. Since decoding will now require the calculation of the

number of syndrome failures and the number of parity errors per block, larger capacity ROM's will be required. It is expected that one 256 x 2 ROM per track will be adequate. As in CRCC error detection, counters will be required for monitoring purposes to determine the number of CRCC failures per track. Additional counters will be required to count across track parity errors.

4. LOSS OF EFFICIENCY. The VLBA recorder design includes 32 data tracks plus 3 system tracks. Up to 3 passes can be recorded without loss of data tracks if the 3 system tracks are used to record across track parity. An inspection of the observing mode examples presented by A.E.E. Rogers shows that with the exception of medium spectral observations all other recording will require 16, 32 or 64 tracks per pass, all of which can be recorded with less than 3 passes per head position. Medium spectral observations will only be taken infrequently and their tape volume requirements are already low.

DESCRIPTION

Consider an across track parity scheme in which the 32 VLBA data tracks are split into two groups of 16, each group of 16 possessing its own parity generator. To increase flexibility for multiple pass recording any subset of the data signals can be input to the parity generators. The parity bits can be recorded either on one of the three system tracks or on one of the data tracks not being used to record data. CRCC codes will be used for along track error detection.

In order to achieve maximum security in meeting spec the following four decoding rules can be used:

i) If there are no parity errors and no non-zero syndromes then all data will be passed unaltered to the correlator.

ii) If there are parity errors but no non-zero syndromes all data will be flagged invalid.

iii) If there is one and only one non-zero syndrome then the data from that track will be corrected using across track parity.

iv) If there are more than one non-zero syndromes then the appropriate along track CRCC code words will be flagged invalid.

Although these decoding rules optimize security, other decoding rules could be considered which significantly increase the operating range of the recorders. The worst case model used to constrain recorder operating range considers errors to occur as independent pairs. As it happens, across track parity can be used rather effectively to determine whether errors occur independently or in bursts, e.g. when the number of parity errors is high then one of the tracks with non-zero

syndrome contains either a burst error or a sync error while if the number of parity errors is low then all errors are likely to be nearly independent. Different decoding algorithms can be used when either type of error is suspected. For suspected burst errors, entire CRCC code words should be flagged invalid. However when errors are suspected to be independent, data could be flagged invalid only at points where parity errors and along track CRCC syndrome error detections intersect. For the case driving worst case estimates, i.e. when errors occur as independent pairs, the fraction of data flagged invalid can be reduced significantly if the modified decoding rule is used.

PERFORMANCE

In order to determine the performance of across track parity assume a system with 16 data tracks and one parity track. Along track error detection using both an (88,80) and (176,160) CRCC code will be considered. Decoding will use the rules suggested for maximum security.

The probability that x of the n=17 along track CRCC code words will have at least one error can be written

$$P(n,x) = \frac{n!}{(n-x)!\ x!}\ p^{x}(1-p)^{n-x}$$

where p ~ probability that any one of the along track code words will be in error.

Data is flagged invalid when more than one of the along track CRCC syndromes is non-zero. The probability that this will occur can be represented by the expression

$$\sum_{x=2}^{n} P(n,x)$$

Whenever data is flagged invalid only x/n of the tracks are effected. The fraction of data flagged invalid can then be written as

$$PD = \sum_{x=2}^{n} \frac{x}{n}\ P(n,x)$$

$$= \frac{1}{n}\ (\bar{x} - P(n,1))$$

$$\sim (n-1)\ p^{**2}$$

Data is also flagged invalid when there are parity errors and no non-zero along track syndromes. In this case the error cannot be localized to a track so all data is flagged invalid. This condition only occurs when a CRCC syndrome

fails to detect an error. The probability that an error will not be detected by CRCC error detection is

$$1/2^{**}(N-K)$$

where (N-K) is the number of CRCC check bits. The fraction of data flagged invalid due to this cause can be represented by

$$\sum_{x=1}^{n} \frac{n!}{(n-x)!\,x!} \left(p/2^{**}(N-K)\right)^{x} \left(1-p/2^{**}(N-K)\right)^{n-x}$$

$$\sim np/2^{**}(N-K)$$

The total fraction of data flagged invalid can then be written to good approximation as

$$PD = np/2^{**}(N-K) + (n-1)*p^{**}2$$

Values of PD have been calculated for p=0.01, p=0.015 and p=0.02 and summarized in Table 1.

	PD	
p	N-K=8	N-K=16
0.01	2.0E-3	1.5E-3
0.015	4.0E-3	3.2E-3
0.02	6.4E-3	5.4E-3

TABLE 1

This table can be used to interpolate to pmax, the maximum value of p at which the VLBA fraction of data flagged invalid spec is guaranteed to be met, i.e. the value of p at which PD=0.005. For N-K=8, pmax=0.017 and for N-K=16, pmax=0.019. Of more significance, a maximum along track bit error rate can be calculated. A worst case value will result if it is assumed that along track errors occur as independent pairs. In this case p can be related to BER, the along track bit error rate according to

$$p = n*BER/2$$

For an (88,80) CRCC code the maximum along track bit error rate guaranteed to meet the VLBA fraction of data flagged invalid spec is 3.9E-4. For a (176,160) CRCC code it is 2.2E-4.

Using the decode rules sugested for maximum security, decode errors occur only when along track CRCC error detection fails.

Worst case analysis is attained by assuming that all errors occur in bursts. When an error is detected, half the bits in the code word are on average incorrect. The fraction of data which are in error but not flagged invalid can then be written

$$PDE = \sum_{x=2}^{n} \frac{n!}{(n-x)!\,x!}\, p^{x}(1-p)^{n-x}\left(\frac{x}{2n}\right)\left[x\left(1/2^{**}(N-K)\right)^{x-1}\left(1 - 1/2^{**}(N-K)\right)\right]$$

$$+ \sum_{x=3}^{n} \frac{n!}{(n-x)!\,x!}\, p^{x}(1-p)^{n-x} \sum_{y=1}^{x-2} \left(\frac{y}{2n}\right) \frac{x!}{(x-y)!\,y!} \left(1/2^{**}(N-K)\right)^{y}$$

$$*\left(1 - 1/2^{**}(N-K)\right)^{**}(x-y)$$

For N-K=8 and p=0.017, PDE ~ 1.5E-5.
For N-K=16 and p=0.019, PDE ~ 7.1E-8.

Worst case sync error analysis can be attained by assuming that all errors are sync errors. When a non-zero syndrome is detected, all bits in the corresponding code word are assumed to be out of sync. In order to enhance sync error detection capability, the CRCC code words will be modified by adding an arbitrary bit pattern to the CRCC check bits and subtracting the same bit pattern at decode. The sync error detection capability of the codes after modification should be equivalent to the random error detection capability of unmodified CRCC codes.

For N-K=8 and p=0.017, PDSE ~ 3.0E-5, where PDSE is the fraction of out of sync data not flagged invalid. For N-K=16 and p=0.019, PDSE=1.4E-7. The sync error detect capability of an (88,80) modified CRCC code is marginal in terms of the appropriate VLBA spec. This code should be used in conjunction with another form of sync error detection. The sync error detection capability of a modified (176,160) CRCC code is however more than adequate.

ADVANTAGES

1. The requirement on minimum raw recorder performance has been relaxed by more than a factor of 3 over single track CRCC error detection if across track parity is added, e.g. for a (176,160) CRCC code the maximum average BER required to guarantee that the fraction of data flagged invalid spec be met is now 2.2E-4. Recall that this figure is the result of worst case analysis. If errors tend to come in bursts it will increase. If a more favourable decoding algorithm is used it will increase further. Finally, if dynamic channel to track switching is used this figure actually represents minimum OVERALL system performance. It is conceivable that some tracks could perform considerably worse providing others perform considerably better.

2. The maximum fraction of data in error but not flagged invalid is guaranteed to be well within spec, e.g. assuming a (176,160) along track CRCC code the maximum decoded BER is 7.0E-8.

3. The maximum fraction of data out of sync but not flagged invalid is guaranteed to be well within spec, e.g. for a modified (176,160) along track CRCC code the maximum decoded sync BER is 1.4E-7.

4. A very good estimate of average system BER can be determined from the number of across track parity errors.

5. Complete recovery from single track malfunctions is possible if the average BER for the remaining 16 tracks is < 2.9E-5 and dynamic channel to track switching is used.

6. Recovery from multiple track malfunctions is possible if the misbehaving tracks are in different across track parity groups.

7. Due to the recovery of malfunctioning tracks the minimum channel to track permutation rate can be decreased. This in turn implies an increase in the maximum frame length. A (176,160) CRCC code can then be used with 8000 bit frames to achieve a 9:8 (i.e. same as Mark III) ratio between formatted and unformatted data rates.

8. Given that data must already be brought together and synchronized for the channel to track permutation switch this error correction scheme is very simple to implement.

9. Flagging of data on resynchronization or missed detection of the sync word is not required.

10. Only one criterion is required to decide whether the system is "up" or "down", i.e. the fraction of data flagged invalid.

11. For the most commonly used recorder configurations there will be no apparent loss in efficiency over straight along track error detection. The observing modes where parity bits must be recorded on data tracks are infrequently used modes which already have low data volume requirements.

DISADVANTAGES

1. There will be some loss of efficiency for low data volume observing modes.

2. There will be an increase in system complexity, i.e. an extra module probably needs to be designed.