

VLBA Data Acquisition and Playback Systems
Design and Cost Estimate

Final Report for Phase I - Design Phase

for the period

1 January 1984 through 30 April 1985

ABSTRACT

This report describes work on the design phase (phase I) of the VLBA Data Acquisition and Playback Systems carried out at Haystack Observatory from 1 January 1984 through 30 April 1985. The system design is carried through the functional block diagram level for all modules of the system and is based on the latest design decisions. Major design decisions made with The National Radio Astronomy Observatory's (NRAO) approval during Phase I were the choice of the longitudinal recorder and the selection of a flexible data formatter which can accommodate a number of formats including MkIII.

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1. INTRODUCTION - OVERALL BLOCK DIAGRAM

1.1 Introduction

The Very Long Baseline Array (VLBA) is the next major radio telescope to be constructed as a National Facility for astronomy. The array will consist of ten fully steerable parabolic antennas distributed across the United States including an antenna in Hawaii and one in Puerto Rico. Each antenna will be 25 meters in diameter and will be outfitted with a complement of low noise receivers covering ten radio astronomy bands from 300 MHz to 89 GHz. Data will be recorded on magnetic tape and processed at a Very Long Baseline Interferometry (VLBI) correlation facility to be built by the California Institute of Technology for the VLBA. The array will act as an equivalent aperture of 79 meters with a resolution given approximately by the wavelength divided by the longest baseline length. The contribution that the MIT Haystack Observatory is making to this project is to provide the data digitization and recording system (see Figure 1-1) along with the playback system (see Figure 1-2) for the processor.

The design of the data recording and playback is based on the use of the longitudinal recorder using narrow track (20 micron) headstacks. The choice of the longitudinal recorders over a system using video cassette recorders was made at a design review meeting held at Haystack on 30 August 1984.

1.2 Overall Block Diagram

The overall block diagram of the data acquisition system is shown in Figure 1-3. The system accepts four I.F. signals in the range of 500-1000 MHz from the receivers in the vertex room. The I.F. signals are converted to baseband video signals by image separation mixers. The resulting upper and lower sideband video signals are digitized, formatted and sent to the tracks of a longitudinal recorder. Timing signals are received from the station frequency and time standards and control signals via the monitor and control bus. The system has complete signal switching capability allowing a selected bandwidth from any I.F. channel to be formatted on any recorded track. Further, the digitization electronics is split into two separate racks to allow operation in most modes to continue in the event of failure of any single major subsystem. In addition one rack can be taken "off-line" for maintenance while the other continues to acquire data. Each station will have two recorders each of which is connected to both digitization racks. Two recorders are needed for redundancy and to support 24 hours of continuous operation at an average rate of 100 Mbits/second. The acquisition system is extremely flexible and will support many types of experiments in an efficient manner within the constraints of the recording technology and processor capabilities. For example, in addition to supporting the normal continuum observations the system is compatible with the bandwidth synthesis observations at S and X band now being used for astrometry and geophysics. The system provides up to 32 video channels to aid in the de-dispersion of pulsar signals. Spectral line observations can be made with four level sampling to optimise the sensitivity. Millimeter and other coherence limited observations can record up to 512 Mbits/second for short periods so long as the average rate for 24 hours is maintained at 100 Mbits/second.

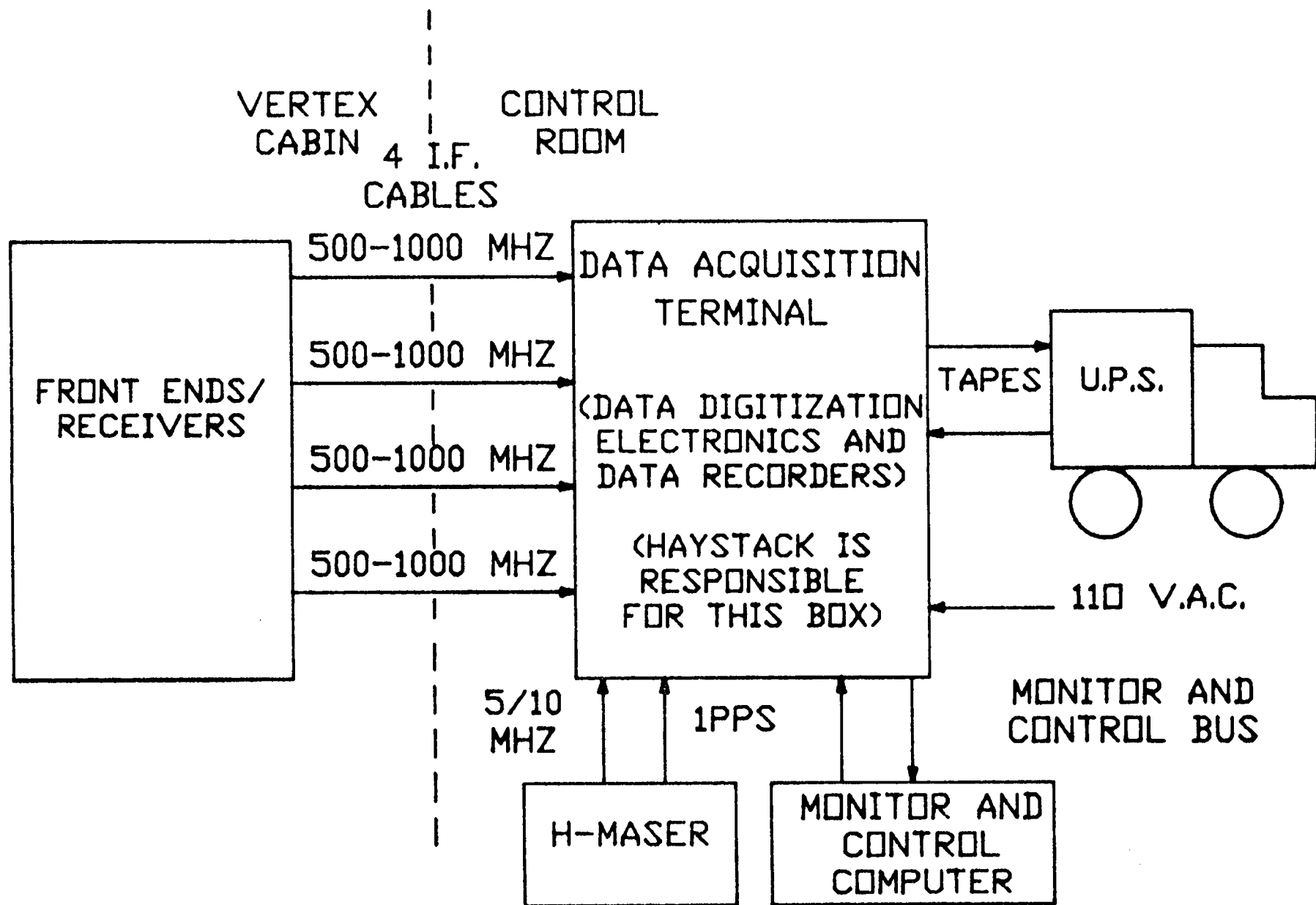


FIGURE 1-1 INTERFACES BETWEEN DATA ACQUISITION TERMINAL AND OTHER SYSTEMS AT EACH ANTENNA.

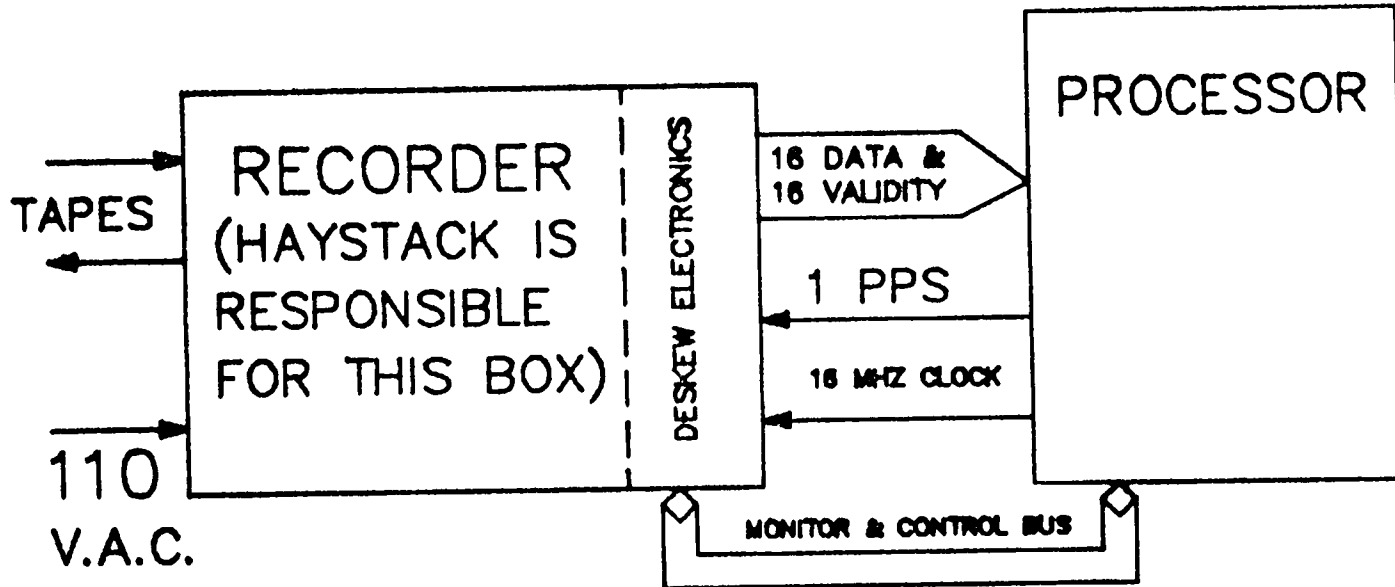


FIGURE 1-2 INTERFACES BETWEEN THE PLAYBACK RECORDER FOR EACH STATION AND THE PROCESSOR.

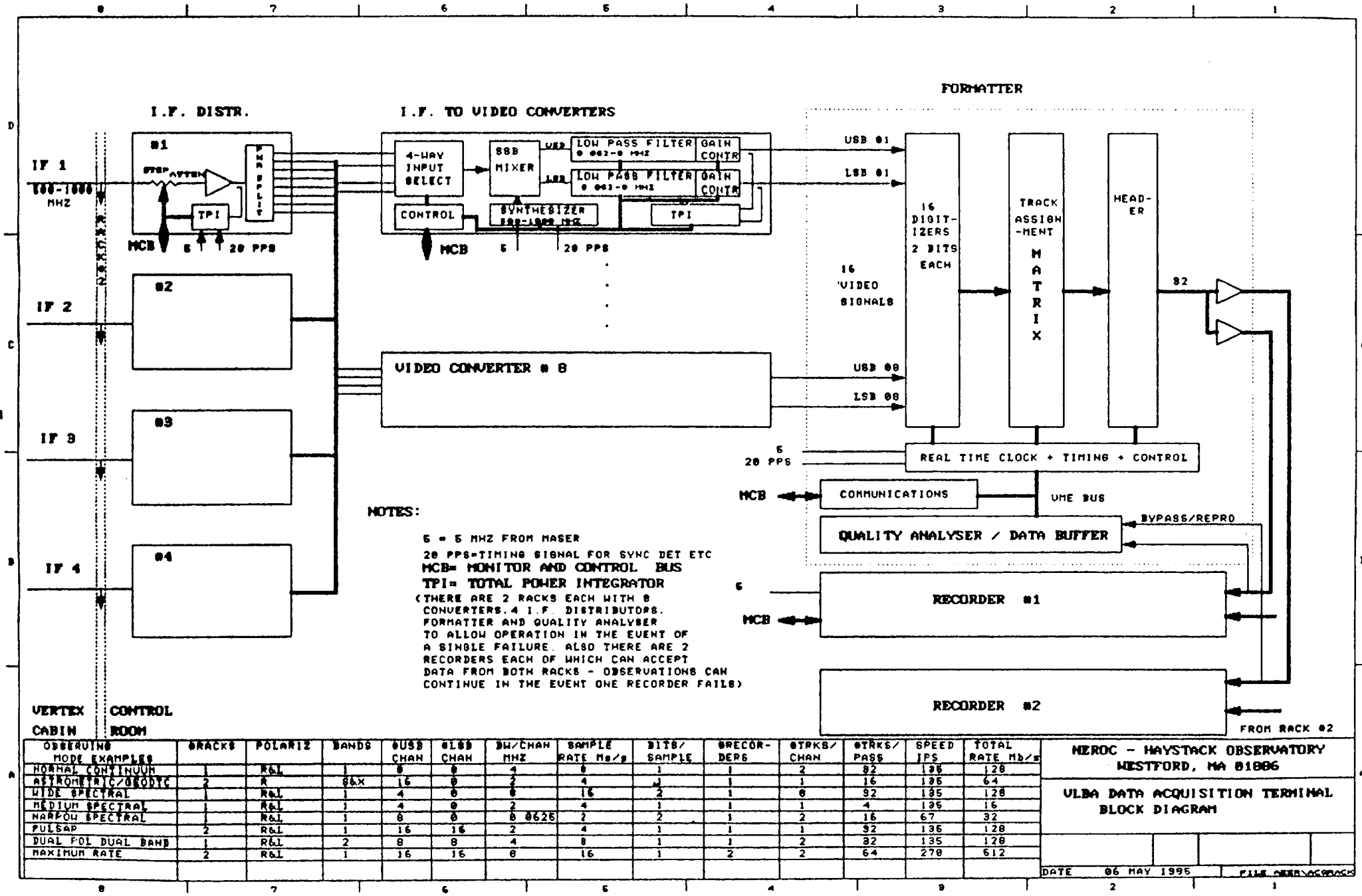


Figure 1-3

2. MODULES - DESIGN

2.1 I.F. Distributor

In each digitization rack four I.F. distributors are provided to distribute the I.F. signals to the eight video (or baseband) converters. Each distributor will contain a level setting attenuator and total power detector/integrator followed by an eight-way power divider.

2.2 Baseband (I.F. to video) Converter

The conversion to video or baseband is done in sixteen (eight per rack) identical video converters. These converters have a four-way input switch so that each can be connected to any one of the four I.F. signals in a completely flexible manner. Each converter contains a 500-1000 MHz synthesizer with ten KHz resolution, an image rejection mixer which separates the sidebands, low pass filter amplifiers, automatic gain control, and square law detectors. A block diagram of the converter is shown in Appendix 9.4.

2.3 Formatter

The video signals are digitized, sampled and formatted into frames. The formatting of each data frame includes the insertion of a header with time of day and other identifying information and the generation of parity and CRC bits. The actual format is flexible and under software control. A MkIII format can be generated as one of the simplest and least sophisticated or more complex formats can be used to make error detection more robust. Multiplexing and mode selection is also provided in the formatter.

2.4 Quality Analyser/Data Buffer

Two selectable channels from the recorder in either reproduce or bypass (direct feedthrough) mode can be decoded as a means of verification of the digitization and recording process. Up to four megabits of this decoded data can be stored by a data buffer for subsequent transmission via the monitor and control bus to the station computer.

2.5 Recorder

A VLBA recorder will consist of a basic longitudinal tape transport, a rack-mounted controller, and one or two head assemblies with associated signal electronics.

The transport will be a revision of the basic Honeywell Model 96 machine, upgraded to 10,000 MTBF to achieve the reliability needed for nearly continuous unattended operation. Improvements are to include more stable reel servos, a cleaner capstan servo, a more reliable vacuum supply, and low-wear replaceable tape-edge bearing surfaces. It is expected that these modifications will permit use of the thinnest available tapes on large reels, minimize maintenance expenses, and maximize component and tape lifetimes. While the VLBA requirement for

24-hour unattended operation at 100 Mbps average data rate can be met with two transports and presently available tape on sixteen inch reels, the intention is to push toward meeting this requirement with a single reel of tape per day.

For purposes of increased reliability, compatibility with other VLBA systems, and flexibility, the transport will be equipped with a new, modular controller. It will replace the extended chain of control presently used in Mark III recorders as much as possible with direct "single-link" control. All monitor and control functions governing tape transport, signal switching, and head block motion will be supervised by a microprocessor or PC core. A block diagram of this system is shown in Figure 2.5-1.

The head assemblies (each capable of mounting two headblocks) will be the same as those now being implemented for Mark IIIA, except that the track width will be reduced to 20 microns and that all 36 (32 data and 4 system) heads per stack will be interfaced. Control of stack position will be by means of an Inchworm actuator and LVDT sensor. If it proves technically feasible, the heads will be interfaced using a single-wire-per-head read-or-write interface for increased reliability, redundancy, and minimization of costs. Each transport will be equipped with two independent head blocks, unless the read/write interface is satisfactory in which case one head-block may be sufficient. Since raw tape channel performance is the most critical parameter of the recording system, every effort will be made to optimize it by reducing interference and choosing tape and head characteristics to take advantage of the latest technology. In particular, the exciting possibility of using the digital video tape now being developed will be fully explored.

The signal electronics include write modules which convert formatter outputs to head currents and read modules which amplify, equalize, and clip head outputs. These are functionally equivalent to similarly designated modules in Mark III recorders. Improved shielding and packaging for the read modules and single-ended head drivers for the write modules to support the read/write interface are being investigated. Also included in the recorder signal electronics are bit synchronizers (one for each simultaneously accessible head) and some signal routing functions.

2.6 Data Playback

The bit synchronized signals from the recorder are aligned with an external clock using buffer RAM and gross tape movement commands sent to the recorder. The decoding of each frame includes sync detection, CRCC syndrome detection, parity detection, control of the data valid flag and header and time code extraction. Multiplexing and mode selection are also provided. To match the capability of the formatter, the decoding algorithm is flexible and under computer control. (Block diagrams are given in Appendix 9.3.)

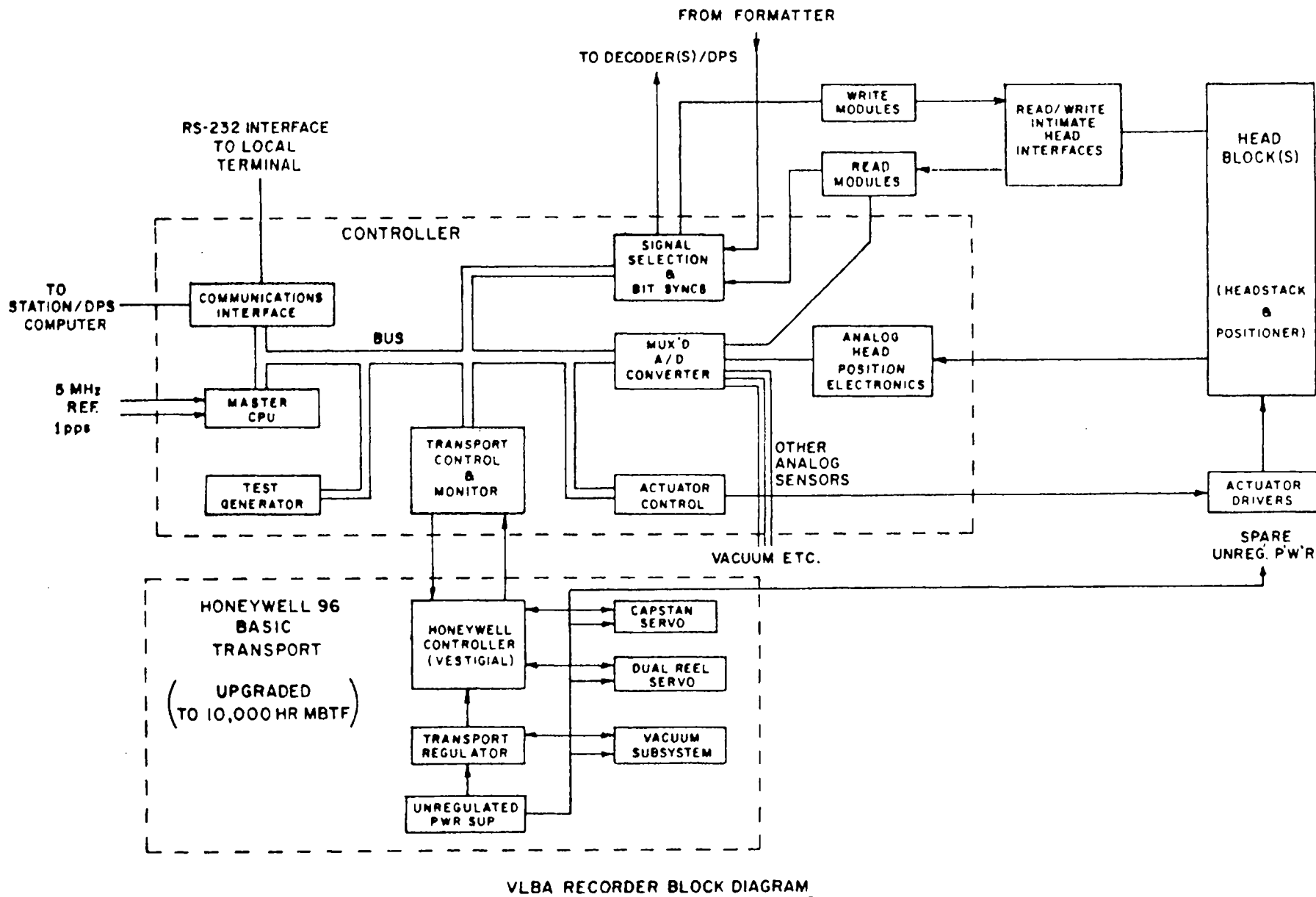


Figure 2.5-1

3. INTERFACES

3.1 Receiver to Data Acquisition System (DAS)

Signals: 4 I.F.s in the range 500 - 1000 MHz
Levels: -42 dBm nominal in 500 MHz bandwidth
Cables: RG-9 or equivalent
Connectors: Type N (male on cable ends from receivers)

3.2 Station Timing to DAS

FREQ:
Signals: 5 MHz at +13 dBm (nominal)
Cable: RG-9 or RG-142 or equiv
Connector: Type N or SMA
TIME:
Signal: 20 Hz square wave -0.5 to +0.5 volt
plus 1 pps to allow for the possibility of manually
synchronizing the formatter
Cable: RG-142 or equiv
Connector: SMA or BNC

3.3 Station Computer to DAS via VLBA Standard Monitor and Control Bus

3.4 Data Playback System (DPS) to Correlator

The DPS/Correlator interface carries the following signals:

Timing Interface:

- 1 pps and a "bit clock" provided to both correlator and DPS's from a master clock. Signals provided on differential ECL lines. Rise time of the 1-pps signal shall be sufficient to resolve a single "bit clock" cycle.

Each "bit clock" transition will advance all DPS channel outputs by one bit.

Signal Interface (DPS to Correlator):

- The agreed-upon DPS-to-Correlator interface will actually reside in the DPS. At that point, the correlator group is free to reformat the signals in any way desired before actually transmitting the data to the correlator proper.

The signals provided by the DPS at this interface are:

- 16 output channels, where each channel contains sign, magnitude, and validity data as separate signals. These signals are clocked

out by the "bit clock" at 16M samples/s repeating samples for data being reproduced at lower rates. A constant delay offset (which can be specified to within one sample interval) can be applied to all DPS output channels. This delay which is common to all DPS output channels can be used to augment the delay offset capabilities of the processor.

- A clock synchronous with data and a 1-pps clock, to allow unambiguous reclocking of the data.
- All signals shall be differential ECL with a maximum data rate of 25 Mbits/sec on each signal line.

Control Interface (Control computer to DPS):

- VLBA command/control interface multi-dropped to all DPS's

Channel switching:

- Any of the 16 DPS output channels can be connected to any recorded baseband channel.

Nominal record speeds: 67,135,270 inches/sec

Playback speed: 270 inches/sec (additional playback speed of 135 being studied as option)

4. SPECIFICATIONS

4.1 I.F. Distributor

Input frequency range: 500-1000 MHz
Gain: 0 dB at 750 MHz (including cable compensation network to correct for cable loss slope)
Input atten range: 0, -15 +/-1 dB, -30 +/-1.5 dB, infinity
Max phase change with gain: < 4 deg peak to peak
Square law linearity: < 1% from 5% to full scale
Isolation between outputs: > 20 dB

4.2 Baseband Converter

BASEBAND CONVERTER

Input range: 492-1008 MHz
Gain through conv(2 MHz BW): 64 +/- 1 dB maximum gain
Level control max atten: 30 dB
Level control phase shift: < 0.5 deg over full range of atten
Gain for other bandwidths: -3 dB/ octave increase in bandwidth
Image rejection: >26 dB over video range 10 kHz to 8 MHz
Output power: 0 +/-0.5 dBm
L.O. range: 500-1000 MHz in 10 KHz steps
Energy in 10 KHz sidebands: < -40 dBc
L.O. phase noise: < 2 deg. rms
L.O. leakage into video < -50 dB
Gain compression: < 0.05 dB (1%)
SNR(noise from converter): > 25 dB
Dynamic range: > 30 dB
Temperature coeff of phase: < 10 deg/ deg C/ GHz
L.O. settling time: < 1 sec
L.O. leakage into input: < -60 dBm
Temperature coeff. of gain: < 0.1 dB/ deg C
4-way input switch isolation:> 60 dB
Bandpass response:
1) >10 dB down at bandedge x 1.08
2) <0.5 dB ripple across lower 80%
3) <1 dB between units across upper 20%
4) <5 deg phase ripple between units across lower 80% of band
5) <20 deg between units across upper 20%
6) <0.2 deg/deg C temperature coefficient of phase over 80% of band
7) <0.1 dB/deg C temperature coefficient of amplitude over 80% of band
(The above should ensure that closure errors are < 0.5 degrees)

Bandwidths: 8,4,2,1,0.5,0.25,0.125,0.0625 MHz and external filter

Data processing: 1) Total power integration and synchronous detection with periods of an integral number of 20 Hz half-cycles or 25 msec
2) Auto-leveling of output power

Monitor and control:

FUNCTION	#bits	control	monitor
IF input select	2	Y	Y
L.O. frequency	16	Y	Y
L.O. unlock	1	N	Y
USB bandwidth	4	Y	Y
LSB bandwidth	4	Y	Y
USB gain	8	Y	Y
LSB gain	8	Y	Y
USB TPI input select	3	Y	Y
LSB TPI input select	3	Y	Y
USB TPI for last ref period	16	N	Y
LSB TPI for last ref period	16	N	Y
USB TPI(sig-ref)	16	N	Y
LSB TPI(sig-ref)	16	N	Y
#cycles to be averaged	16	Y	Y
USB auto-level on/off	1	Y	Y
LSB auto-level on/off	1	Y	Y
serial number	16	N	Y

4.3 Formatter

Number of video inputs: 16 (8 USB plus 8 LSB) in each of 2 identical formatters (one per rack)

Number of formatter outputs: 32 (64 for both units)

Sample rates: 16,8,4,2 MHz

Output format: Serial data format with time code, auxillary data, CRC error detection, (if needed to meet playback error rate specs), sync word, parity and programmable data block and frame length.

Video input level: 0+-0.5 dBm
-4+-0.5 dBm for 4-level processing

Input impedance: 50 ohms unbalanced

Threshold equivalent DC offset and hysteresis: < 5 mv

Threshold level: 600 mv (for magnitude) 0 mv (for sign)

Sampling epoch precision and jitter: < 2 nsec

Sampling modes: 2-level (1 bit) and 4-level (2 bits)
 (4-level coding -w=00,-l=01,+l=10,+w=11
 with MSB (sign) bit and LSB bit on
 separate tracks)

Formatter modes: 1X (output rate/track = sample rate)
 2X (output rate/track = sample rate/2)
 4X (output rate/track = sample rate/4)

Notes: In 1X mode adjacent time samples
 are on the same track
 In 2X mode odd and even samples
 are on separate tracks
 In 4X mode there is a 4-way split
 i.e. 1st. sample to trk w, 2nd. to
 trk x, 3rd. to trk y, 4th. to trk z

tracks/video signal:

I-----I		FORMATTER MODE				I-----I	
I	I	1X	I	2X	I	4X	I
ISAMPLINGI							
I	2-LEVELI	1	I	2	I	4	I
I	4-LEVELI	2	I	4	I	8	I
I-----I						I-----I	

Track switch: 32x32 switch to allow an arbitrary
 reassignment of data samples
 to recorder tracks - This assignment
 can be changed dynamically every frame

Output

Signals: 2 independently buffered sets of
 32 balanced ECL signals from formatter in each rack
 (32 balanced ECL from each of 2 formatters to each of 2 recorders)

4.4 Data Quality Analyser/Data Buffer

Data Memory: 4 Mbits

4.5 Recorders

Average recording rate: 100 Mb/s for 24 hours unattended
 High data rate (HDR): 200 Mb/s or greater
 For each channel and for an averaging time of 1 minute (real time)

Fraction of bits out of sync but flagged valid: $<10^{*-5}$
 Fraction of incorrect bits flagged valid(excluding bits out of sync): $<3 \times 10^{*-4}$
 Fraction of bits flagged invalid: $<10^{*-2}$
 If the above specs are met for the prescribed averaging time of 1 minute then there can be no loss of data (dropout) longer than 600 msec.
 (In no circumstances even when performance degrades should data which fail to meet error specs 1 (fraction of bits out of sync but flagged valid) or 2 (fraction of incorrect bits flagged valid) be passed to the correlator)
 *** see spec. A54001N001
 Weight of tape/day/station < 50 lbs at average rate
 Redundancy: The system will continue to ensure that observations can continue without maintenance in the event of single failures, provided unrecorded tape is available on at least one working transport

 Phase switching: The DPS should be able to unscramble any phase swithing that might be applied in the L0 system. This unscrambling can be accomplished by reversing the sign of the data being fed to the correlator using a deterministic algorithm.

5. MODES OF OPERATION

This subject has been extensively studied by Jon Romney who separates the system parameters into "user-designated" and system-determined as follows:

User-designated parameters:

a) Number of baseband channels

An upper/lower sideband pair of channels can be programmed to any I.F. frequency (in steps of 10 KHz) and connected to any of the four receiver I.F. channels. With both DAS racks up to 32 channels can be recorded. While any number of channels up to 32 could be recorded the number will most likely be a power to two.

b) Channel Bandwidth

8, 4, 2, 1, 0.5, 0.250, 0.125, 0.0625 MHz can be independently selected for each baseband channel.

c) Channel Sample Rate

16, 8, 4, 2 Msamples/sec. must be the same for all baseband channels. Lower sample rates are achieved by selecting every nth bit upon playback (as in MkII spectral line).

d) Sample Precision

2-level or 4-level

System-determined parameters

e) Number of Tracks

Each recorder will be able to record 32 data tracks (extra tracks may be used for redundancy and/or error correction) per pass of the tape although not all heads in the headstack need be enabled. The number of tracks recorded per pass will be the total data rate to be recorded divided by the bit rate per track.

f) Track Fanout

The number of tracks used to record a baseband (video) channel depends on the formatter mode which in turn will have to be selected so that the bit rate per track is set to 8 Mb/s at full tape speed (270 inches/sec nominal), 4 Mb/s at normal speed (135 inches/sec nominal), and 2 Mb/s at half speed (67 inches/sec nominal).

g) Recorded Bit Rate Per Track

Always set to be commensurate with tape speed. At present the nominal longitudinal bit density is 33,000 bits per inch, but may be increased to 50,000 bits per inch.

h) Speedup Factor

In order to optimise the playback performance tapes will always be played back at full speed (although a normal playback speed option is being studied) Note that tapes recorded at full speed will not be speeded up while tapes recorded at normal and half speed will be speeded up by factors of two and four respectively.

i) Playback Rate

This will always be at full speed or eight Mbits/sec/track. If a normal playback speed is not implemented as an option, two-level data cannot have a fanout of more than two tracks/channel and four-level data cannot have a fanout of more than four tracks/channel because the correlator will not be able to accept data at a higher rate than 16 Ms/s.

Recommended NORMAL Continuum Mode

2-level	16	4 MHz channels, 12 hr/tape, 2 x speedup
4-level	8	4 MHz channels, 12 hr/tape, 2 x speedup

This recommendation is given for the following reasons:

a) If most observations have a 2x speedup upon processing there will be time for some special multiple pass processing and maintenance activities.

b) While the amount of data that has to be archived for a given field of view depends only on the total bandwidth and not on the number of channels there may be some advantage in minimizing the number of channels.

6. COST ESTIMATE

We now update our fabrication cost estimates in the light of revised specifications and a better knowledge of the design details. All estimates are in 1985 dollars and are based on subcontracts for services (like p.c. board manufacture, wire-wrapping, etc.). If VLBA electronics were to be built by industry these cost estimates should be at least doubled (our experience with MkIII is that industry prices are at least double our cost to fabricate).

The most significant cost increase over previous estimates is the increased cost of the Honeywell Model 96 tape transport which is now estimated at 24K, based on recent purchase experience, compared with the previous estimate of 15K based on 1983 experience.

The revised specifications involve the following:

- 1) A great desire to have a maximum record rate of 512 Mb/s.
- b) Full flexibility in formatter to maintain options of format choice and error detection.
- c) Corresponding flexibility in the de-formatting function of the DPS.

Our better knowledge in the design detail has also affected the cost particularly in the areas of the headblock assembly, recorder electronics and DPS electronics.

6.1 Data Acquisition System (DAS) (two needed per site)

4	I.F. Distributors	\$ 3,000	
8	Baseband Converters	20,000	
	Formatter		
	Quality Analyser/Data Buffer	17,400	
	Digitization Rack and Power		
	Supplies	5,000	
	Labor for Digitization Rack	6,000	
	Subtotal for Digitization Rack		\$51,400
	Honeywell Recorder	24,000	
	Recorder Electronics	8,000	
	Headblock Assembly	8,000	
	Labor for Recorder Rack	6,000	
	Subtotal for Recorder Rack		\$46,000
	TOTAL	\$97,400	per DAS

6.2 Data Playback System (DPS)

Deskew Electronics	\$30,000
Honeywell Recorder	24,000
Recorder Electronics	8,000
Headblock Assembly	8,000
Assembly Checkout and Labor	6,000

TOTAL \$76,000 per DPS

Thus the total fabrication cost estimates are now as follows:

# UNIT	# REQUIRED	UNIT COST	TOTAL
DAS	20	97.4	1948
DPS	22	76.	<u>1672</u>
			3620

6.3 Options for Lower Cost

We suggest the following cost reduction options in the order we would recommend adoption if needed to reduce cost.

1] Put all 16 converters in one rack with a single formatter as originally proposed. This would make a major saving in formatter cost and a minor saving in the cost of I.F. distribution and rack hardware.

Savings in I.F. distribution and rack hardware	\$ 20,000
Saving in formatter cost (see appendix - uses type 2)	<u>\$155,640</u>
	\$175,640

2] Eliminate the LSB outputs in the video converters. This would reduce the cost of the video converters somewhat, and make for additional savings in the formatter assuming Option 1 is already exercised.

Video converter cost reduction (\$500 per converter)	\$ 80,000
Formatter cost reduction (uses type 1)	<u>18,180</u>
	\$ 98,180

3] Reduce the number of recorder tracks from 32 to 16. (Without reducing the number of formatter outputs - i.e. uses type 2.) This would result in some savings in the recorder and major savings in the DPS costs.

Savings in recorders approximately 2,000 per recorder for simpler headblock assembly	\$ 84,000
Savings in DPS electronics (which now has half the number of track modules)	<u>\$200,000</u>
	\$284,000

Comments and Recommendations

Adoption of option 1 would have an impact on the maintenance of the system and the rather convenient modularity which would allow initial implementation at the first VLBA antennas using only one digitization rack per station. In addition since only 32 formatter outputs are available the maximum attainable record rate is reduced from 512 Mb/s to 256 Mb/s. We recommend this revision to our original plans if funds are not available to support full redundancy of two racks per site and the 512 Mb/s capability (which exceeds the VLBA HDR specification).

If Option 2 is adopted there is a factor of 2 reduction in the de-dispersion capability for pulsars which is only a minor reduction of capability. If this option is chosen we recommend that space be left to allow LSB channels to be added.

Adoption of option 3 will require both transports for the high data rate mode (256 Mb/s). In addition, the normal observing mode will be to record at close to maximum speed allowing only a small (say 15%) speed-up upon processing. If this cost reducing option is exercised we recommend that space be left in the recorders and DPS to add additional track electronics when funds become available.

If all three cost reducing options are exercised the new cost estimate will be reduced by 558K\$ and will be within ten percent of the original estimate which was made in 1983 dollars while our new estimate is in 1985 dollars. While we do not anticipate further increases in our estimates, as the design progresses final fabrication cost estimates should be based on the actual prototypes. The most uncertain quantity is the cost of the Honeywell recorder which has already undergone a substantial increase. Further cost increases might be offset by reducing the number of transports needed to do the job - but this is too large an extrapolation on the longitudinal recording technology to be certain at this stage. A summary of the original costs, updated costs and options for lower cost are shown in the Table 6-1 which follows. (See Appendix for more details of the cost estimate.)

Module/Task	ORIGINAL PROPOSAL			ESTIMATE IN THIS REPORT			ALL BASEBAND CONV IN 1 RACK			16 TRACK RECORDER		
	Number Required	Unit Cost	Total Cost	Number Required	Unit Cost	Total Cost	Number Required	Unit Cost	Total Cost	Number Required	Unit Cost	Total Cost
I.F.Distributor	40	1	40	80	0.75	60	40	1	40	40	1	40
Baseband Conv.	160	2.5	400	160	2.5	400	160	2	320	160	2	320
Formatter/Decoder	10	23	230	20	17.4	348	10	17.4	174	10	17.4	174
DAS Racks	10	10	100	20	5	100	10	10	100	10	10	100
Honeywell Recorders	52	15	780	42	24	1008	42	24	1008	42	24	1008
Recorder Electronics	52	6	312	42	8	336	42	8	336	42	8	336
Headblock Assembly	52	4	208	42	8	336	42	8	336	42	6	252
DPS Electronics	22	16	352	22	30	660	22	30	660	22	20.9	460
Labor & Overhead	-	-	372	-	-	372	-	-	372	-	-	372
TOTALS			2794			3620			3346			3062

Complete Redundancy in Electronics 512 Mb/s maximum rate

Only partial redundancy in electronics 256 Mb/s maximum rate no LSB channels

256 Mb/s maximum rate + reduced speed-up at processor

OPTION 1 + 2

OPTION 1 + 2 + 3

FABRICATION PLAN - DATA ACQUISITION AND PLAYBACK (AEER 30 APR 85)

I---PHASE 1-----I---PHASE 2----I---FABRICATION PHASE----
 I---1984---I---1985----I---1986----I-1987-I-1988-I-1989
 JFMAMJJASONDJFMAMJJASONDJFMAMJJASON

MAJOR DESIGN DECISIONS
LONGITUDINAL RECORDER:
OPERATIONAL TESTS -----I
VCR RECORDER: OR--prototype--I
OPERATIONAL TESTS -----I	.	I-test---I
RECORDER CHOICE * (Done in favor of longitudinal)
FORMATTER CHOICE . * (Done)
DATA ACQUISITION SYSTEM --design----I
(DAS)
(I.F. distr.,baseband conv,Formatter etc.)	Iproto DAS
FABRICATION SCHEDULE:	.	-test---I
	.	.	3DAS. 10DAS. 7 DAS.	.	.	.
DATA PLAYBACK SYSTEM --design-----I
(DPS)	Iproto DPS
FABRICATION SCHEDULE:	.	-test---I
	.	.	.	6 DPS.16DPS	.	.
DESIGN REVIEWS *(recorder.type)
	*(telecon +viewgraphs)
	*(Socorro mtg)
	.	*(test results)
	.	*(fabr. reports)
	.	*(fabr. repts)
	.	*(fabr.)
COST (1985 k\$)	277	320	378	974	.1138	.1216

8. GLOSSARY

Baseband Channel: Data channel derived from one video output of a baseband converter.

Baseband Converter: Image separation mixer with synthesized local oscillator which converts a portion of the I.F. spectrum to separate upper and lower sideband video signals. Also known as video converter.

Data Acquisition System (DAS): System to record I.F. outputs of the receivers.

Data Playback System (DPS): Recorder with deskew and decoding electronics to present astronomical data input to the correlator.

Data quality Analyser: Decoder which allows the evaluation of performance of each recorder track either prior to recording (bypass) or upon playback.

Deformatter: Strips out synchronization bits, CRC codes, auxiliary data etc., and presents astronomical data to the processor, i.e., output is equivalent to digitizer output.

Headblock Assembly: Assembly of headstack with lateral positioning device.

Header: Information in format pertaining to time-of-day, mode, auxiliary data, etc.

Headstack: Stack of recorder heads.

I.F. Channel: Intermediate frequency signal from front end.

I.F. Distributor: Split an I.F. signal power into eight outputs which the input to the baseband converters.

Track: Recorder channel connected to a specific head. Also means one of the physical "tracks" of magnetized data on tape.

9. APPENDIX

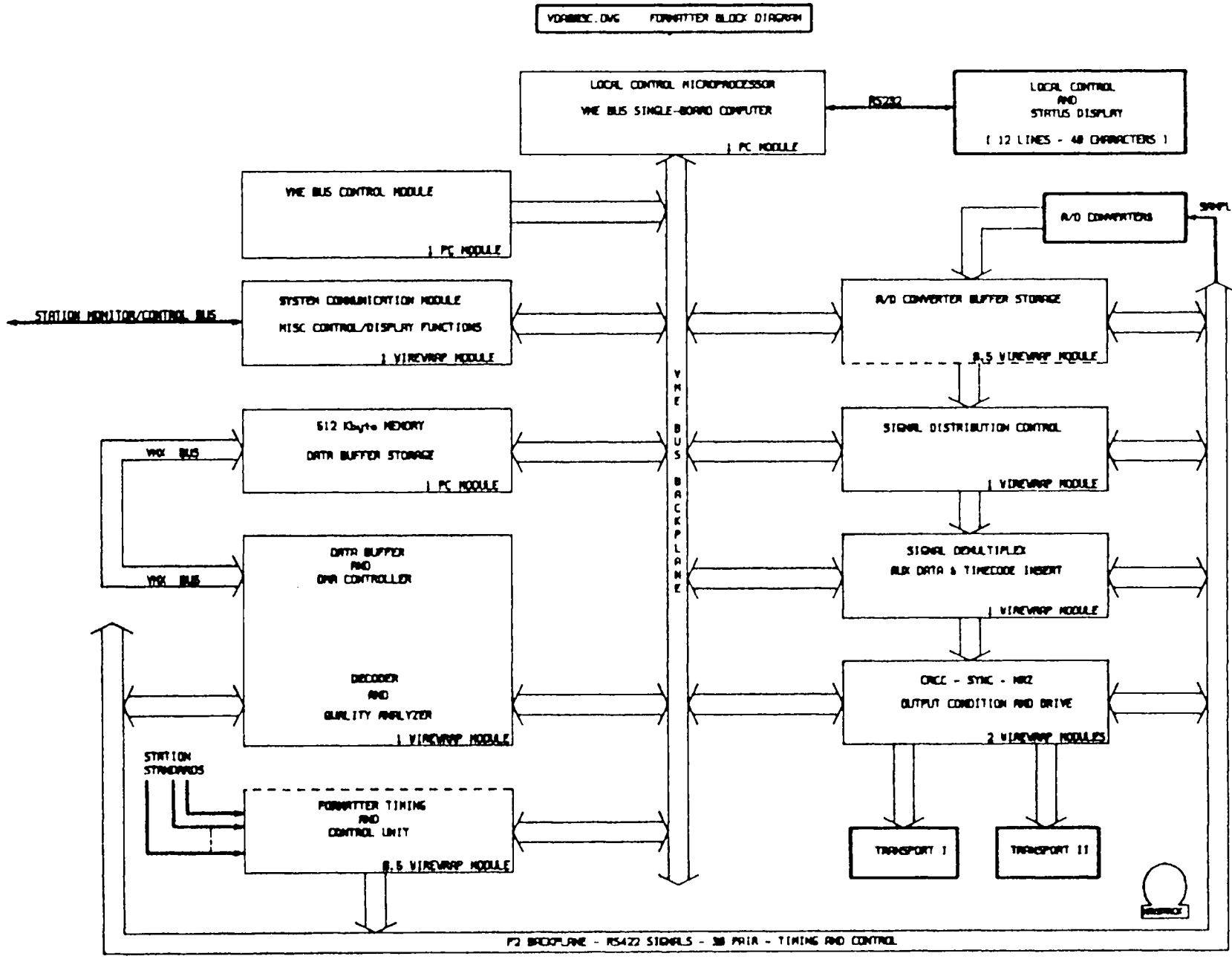


Figure 9.1-1

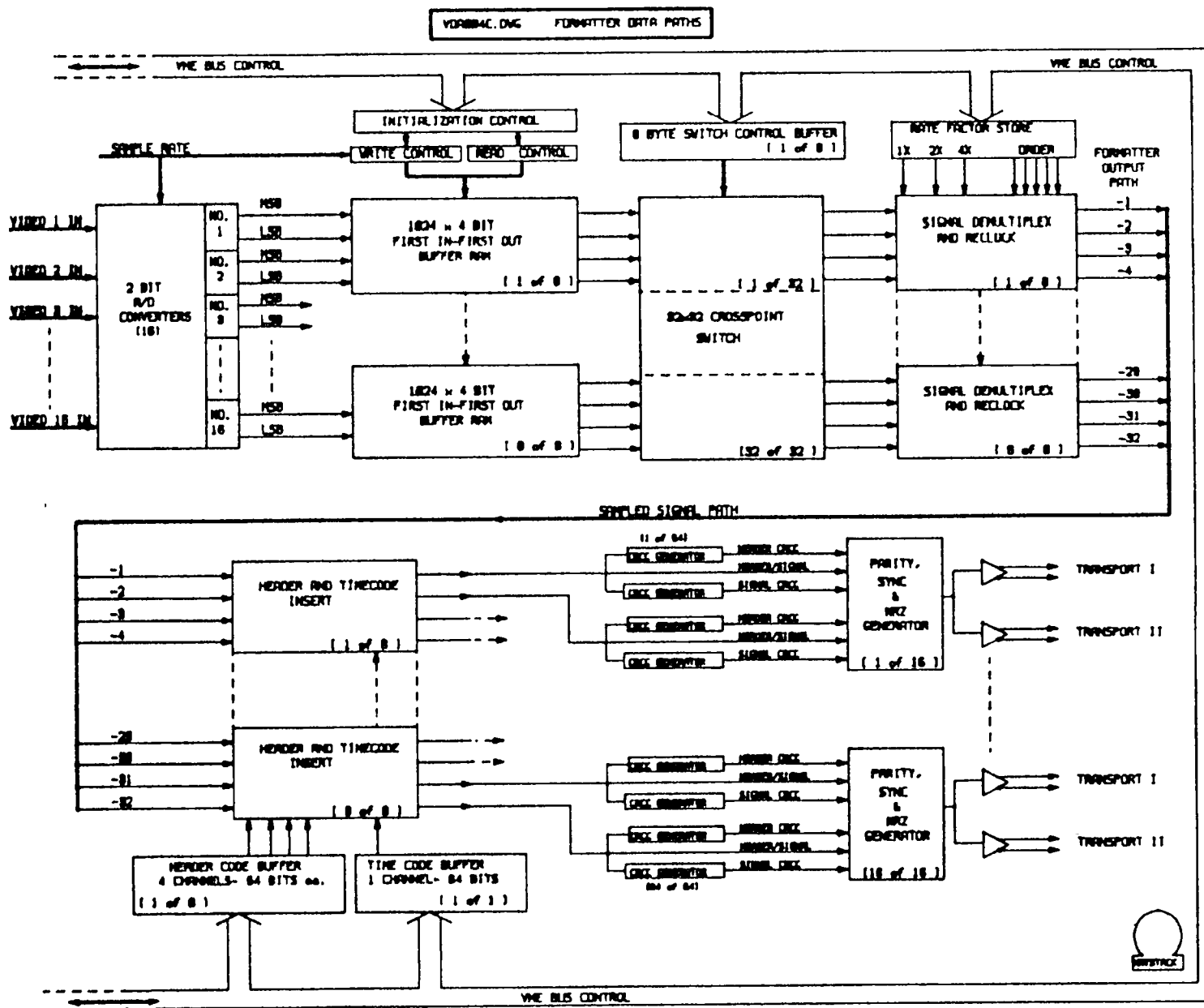


Figure 9.1-2

VORBISSIC FORMATTER TIMING AND CONTROL MODULE

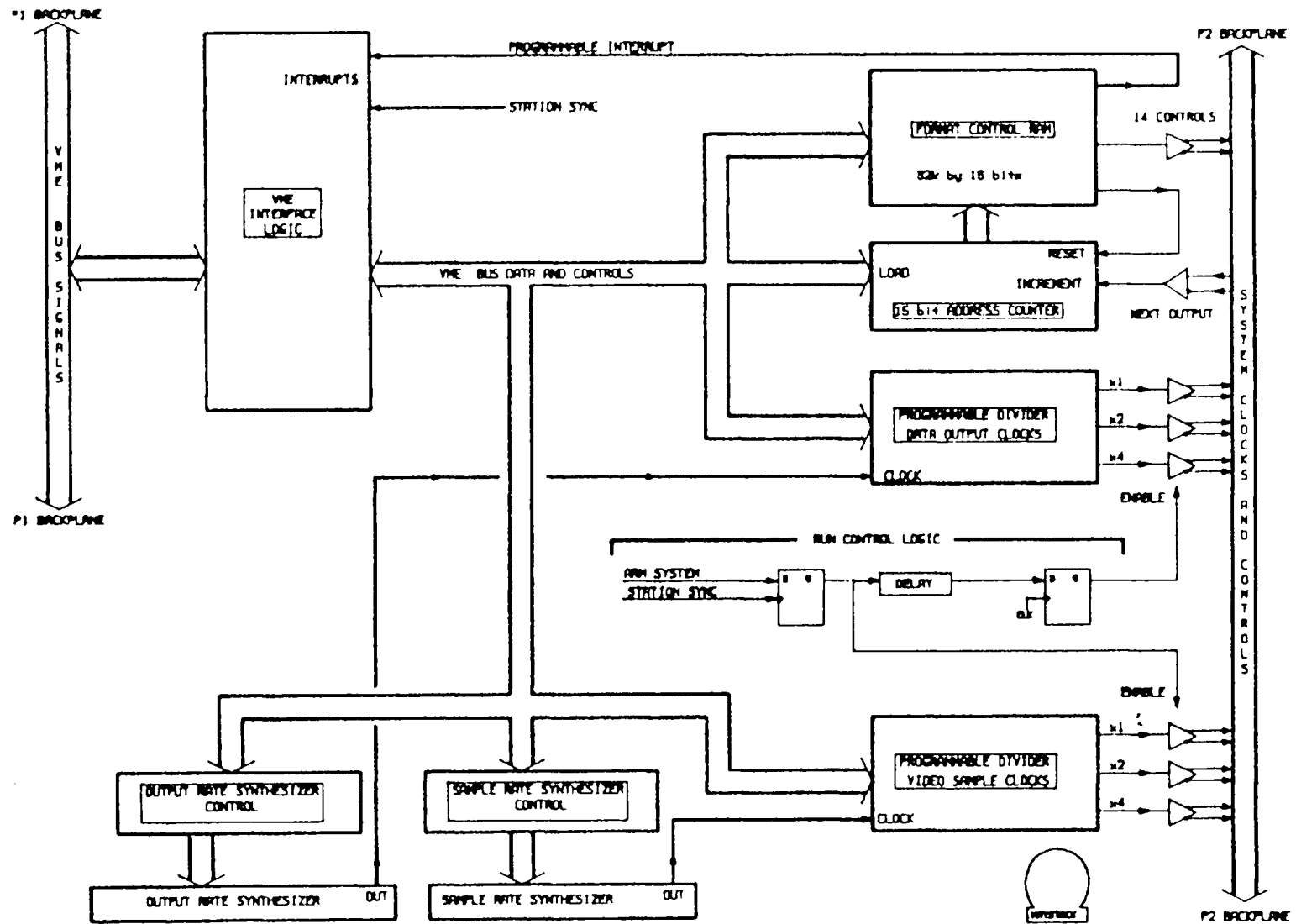


Figure 9.1-3

VERBILAC FORMAT CONTROL ASM SIGNALS

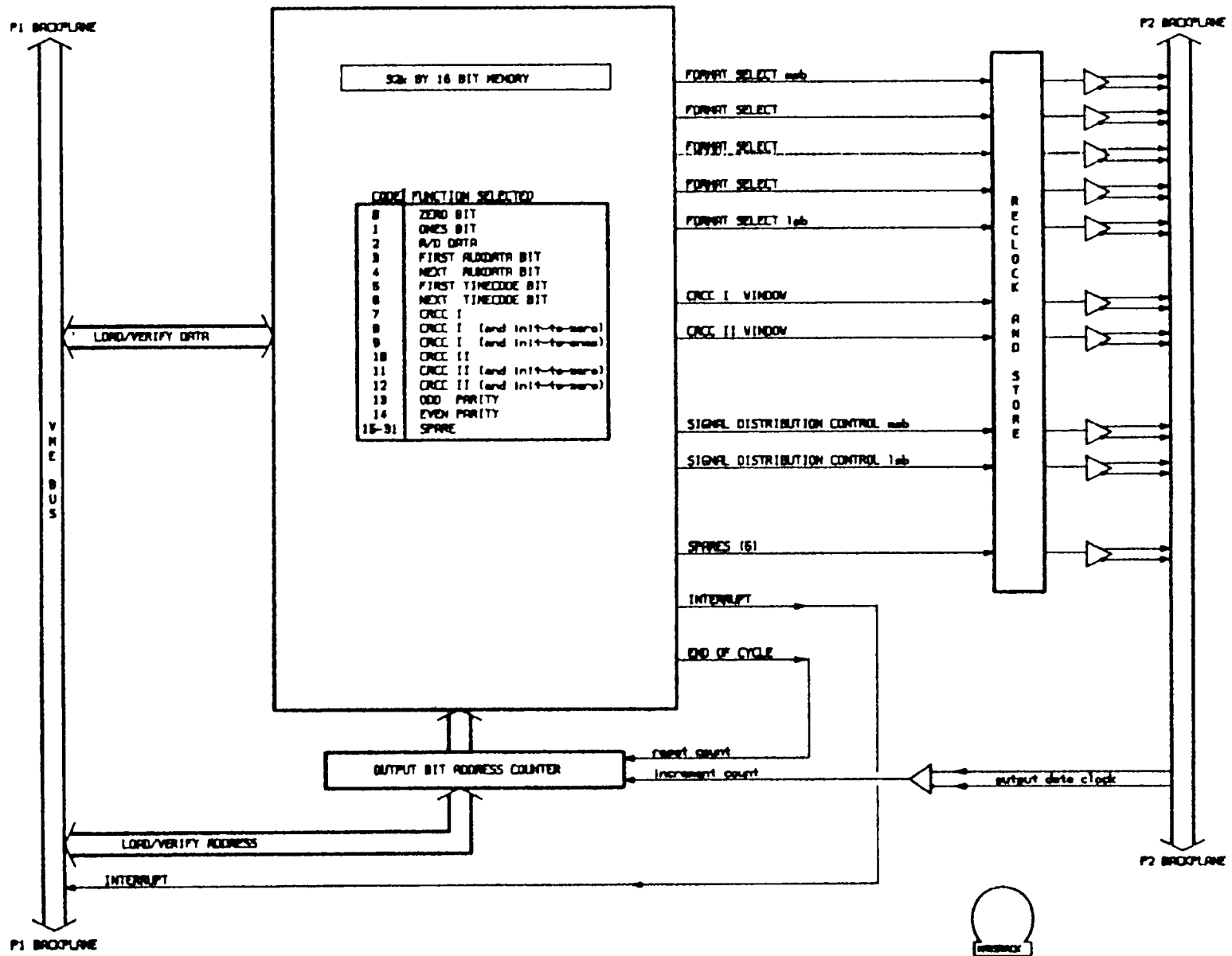


Figure 9.1-4

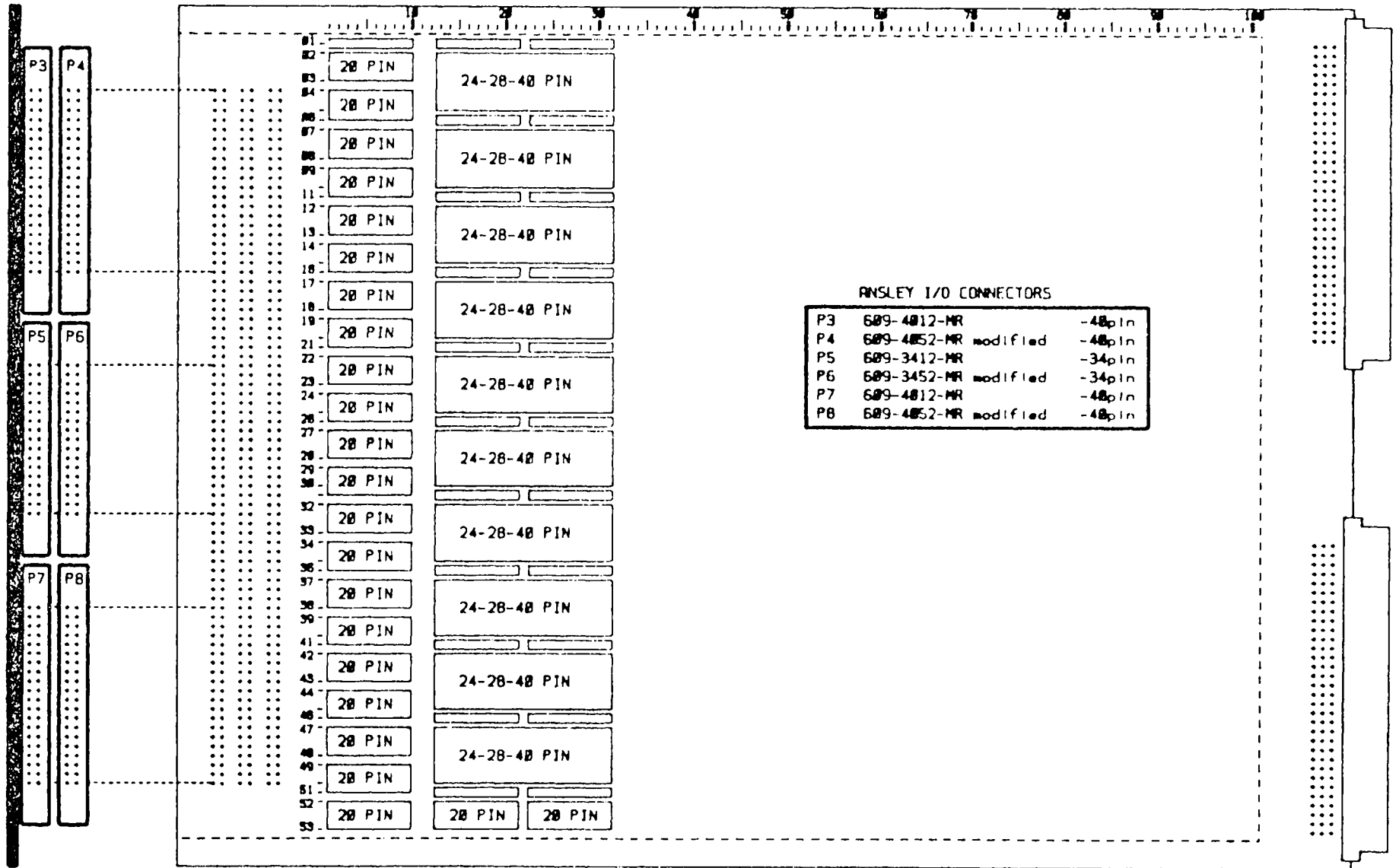


Figure 9.1-5

VOP012C.DWG FORMATTER SYSTEM CHASSIS LAYOUT

19 INCH VME BUS CHASSIS • 2.0 (0.8") SPACING

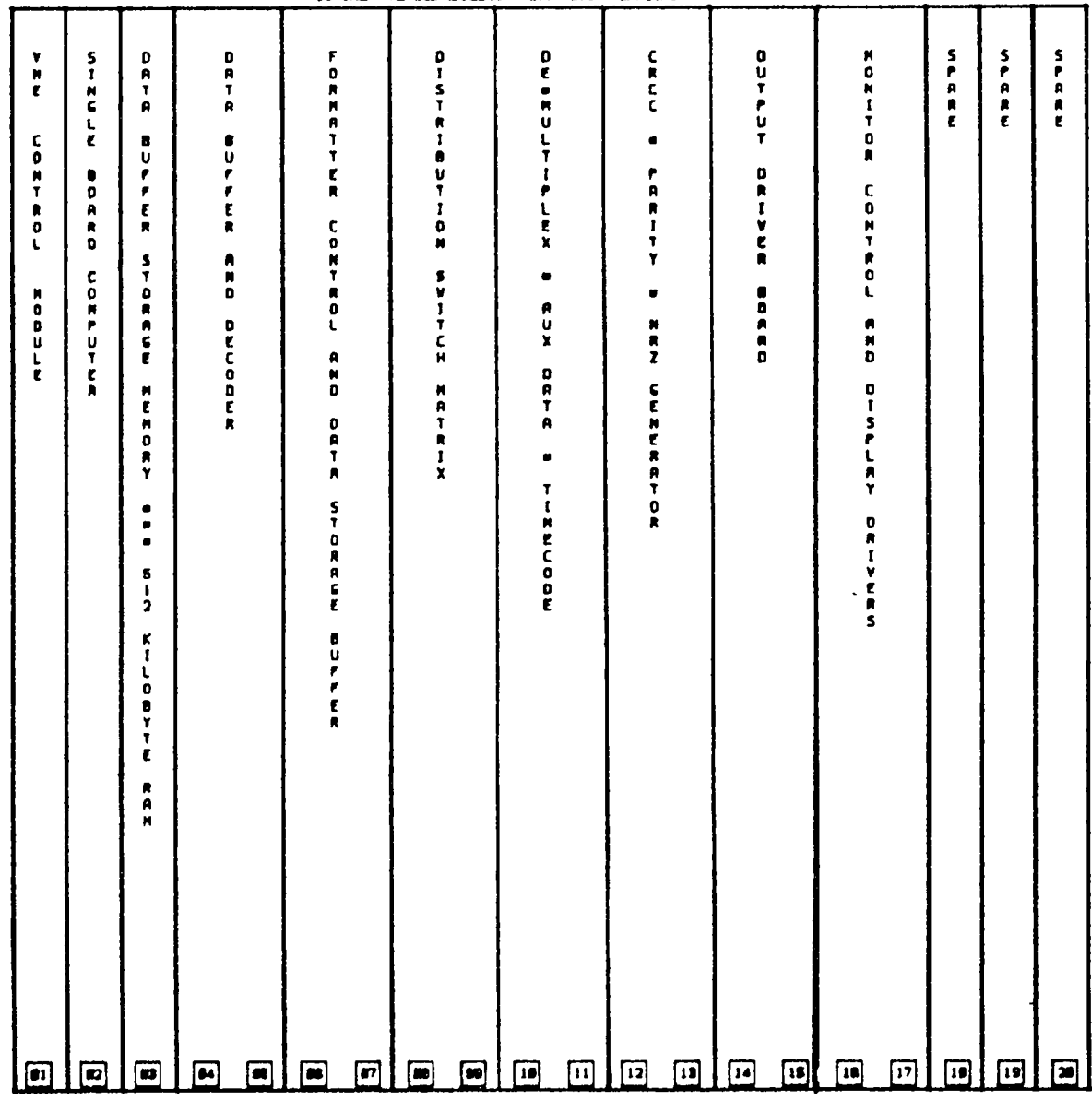


Figure 9.1-6

VLBA FORMATTER COST ESTIMATE SUMMARY -- 29APRIL85 -- file FORCOST

	cost each	total system cost
	-----	-----
CURRENT DESIGN.. TYPE 1	\$17382.00	\$347640.00
16 A/D's & 32 TRACKS per CHASSIS		
2 CHASSIS per STATION		
REDUCED DESIGN.. TYPE 2	\$19200.00	\$192000.00
32 A/D's & 32 TRACKS per CHASSIS		
1 CHASSIS per STATION		
REDUCED DESIGN.. TYPE 3	\$13696.00	\$273920.00
16 A/D's & 16 TRACKS per CHASSIS		
2 CHASSIS per STATION		
REDUCED DESIGN.. TYPE 4	\$16360.00	\$163600.00
32 A/D's & 16 TRACKS per CHASSIS		
1 CHASSIS per STATION		

9.2 Formatter Costs

9.2-1

TYPE 1: 16 A/D's, 32 TRACKS, 2 per STATION - CURRENT DESIGN

COMMERCIAL MODULES

1 ea 68010 CPU BOARD	\$1500.00
512 Kbyte DATA BUFFER RAM	\$3000.00
UME BUS CONTROL MODULE	\$750.00

total commercial modules.....	\$5250.00

WIRE-WRAP MODULES

7 WIREWRAP PANELS at 500.00	\$3500.00
20,000 WIRES at 0.10	\$2000.00
36 SWITCH MATRIX IC'S	\$432.00
10 ECL RAMS	\$250.00
1000 IC'S at 4.00	\$4000.00

total custom modules.....	\$10182.00

MECHANICAL / PACKAGING

UME RACK AND BACKPLANE	\$1000.00
CUSTOM P2 BACKPLANE	\$500.00
30 RIBBON CONNECTOR SETS	\$450.00

total mechanical.....	\$1950.00
	=====
total cost per formatter	\$17382.00
(2 required per site)	

ONE TIME SETUP COSTS

WIRE-WRAP PANEL TOOLING	\$2500.00
WIRE-WRAP SETUP	\$2000.00
WIRE-WRAP REWORK	\$1500.00
BACKPLANE LAYOUT	\$1500.00

total 'one time' setup cost...	\$7500.00

*** NOTE *** NOT INCLUDED IN COST ESTIMATES.....

POWER SUPPLIES
A/D CONVERTERS
FREQUENCY SYNTHESIZERS
PANEL DISPLAYS

9.2-2

TYPE 2: 32 A/D's, 32 TRACKS, 1 per STATION

 COMMERCIAL MODULES

1 ea 68010 CPU BOARD	\$1500.00
512 Kbyte DATA BUFFER RAM	\$3000.00
UME BUS CONTROL MODULE	\$750.00
total commercial modules.....	\$5250.00

 WIRE-WRAP MODULES

8 WIREWRAP PANELS at 500.00	\$4000.00
24,000 WIRES at 0.10	\$2400.00
100 SWITCH MATRIX IC'S	\$1200.00
10 ECL RAMS	\$250.00
1000 IC'S at 4.00	\$4000.00
total custom modules.....	\$11850.00

 MECHANICAL / PACKAGING

UME RACK AND BACKPLANE	\$1000.00
CUSTOM P2 BACKPLANE	\$500.00
40 RIBBON CONNECTOR SETS	\$600.00
total mechanical.....	\$2100.00
total cost per formatter	\$19200.00
(1 required per site)	

 ONE TIME SETUP COSTS

WIRE-WRAP PANEL TOOLING	\$2500.00
WIRE-WRAP SETUP	\$2000.00
WIRE-WRAP REWORK	\$1500.00
BACKPLANE LAYOUT	\$1500.00
total 'one time' setup cost...	\$7500.00

*** NOTE *** NOT INCLUDED IN COST ESTIMATES.....

POWER SUPPLIES
 A/D CONVERTERS
 FREQUENCY SYNTHESIZERS
 PANEL DISPLAYS

9.2-3

ULBA FORMATTER COST ESTIMATES -- 29APRIL85 -- file FORCOST3

TYPE 3: 16 A/D's, 16 TRACKS, 2 per STATION

COMMERCIAL MODULES

1 ea 68010 CPU BOARD	\$1500.00
512 Kbyte DATA BUFFER RAM	\$3000.00
UME BUS CONTROL MODULE	\$750.00

total commercial modules.....	\$5250.00

WIRE-WRAP MODULES

4 WIREWRAP PANELS at 500.00	\$2000.00
12,000 WIRES at 0.10	\$1200.00
16 SWITCH MATRIX IC'S	\$196.00
10 ECL RAMS	\$250.00
750 IC'S at 4.00	\$3000.00

total custom modules.....	\$6646.00

MECHANICAL / PACKAGING

UME RACK AND BACKPLANE	\$1000.00
CUSTOM P2 BACKPLANE	\$500.00
20 RIBBON CONNECTOR SETS	\$300.00

total mechanical.....	\$1800.00

total cost per formatter\$13696.00
 (2 required per site)

ONE TIME SETUP COSTS

WIRE-WRAP PANEL TOOLING	\$2500.00
WIRE-WRAP SETUP	\$2000.00
WIRE-WRAP REWORK	\$1500.00
BACKPLANE LAYOUT	\$1500.00

total 'one time' setup cost... \$7500.00

*** NOTE *** NOT INCLUDED IN COST ESTIMATES.....

POWER SUPPLIES
 A/D CONVERTERS
 FREQUENCY SYNTHESIZERS
 PANEL DISPLAYS

9.2-1-6

TYPE 4: 32 A/D's, 16 TRACKS, 1 per STATION

COMMERCIAL MODULES

1 ea 68010 CPU BOARD	\$1500.00
512 kbyte DATA BUFFER RAM	\$3000.00
VME BUS CONTROL MODULE	\$750.00
<hr/>	
total commercial modules.....	\$5250.00

WIRE-WRAP MODULES

6 WIREWRAP PANELS at 500.00	\$3000.00
10,000 WIRES at 0.10	\$1000.00
64 SWITCH MATRIX IC'S	\$768.00
10 ECL RAMS	\$250.00
800 IC'S at 4.00	\$3200.00
<hr/>	
total custom modules.....	\$9018.00

MECHANICAL / PACKAGING

VME RACK AND BACKPLANE	\$1000.00
CUSTOM P2 BACKPLANE	\$500.00
40 RIBBON CONNECTOR SETS	\$600.00
<hr/>	
total mechanical.....	\$2100.00
<hr/>	
total cost per formatter	\$16368.00
(1 required per site)	

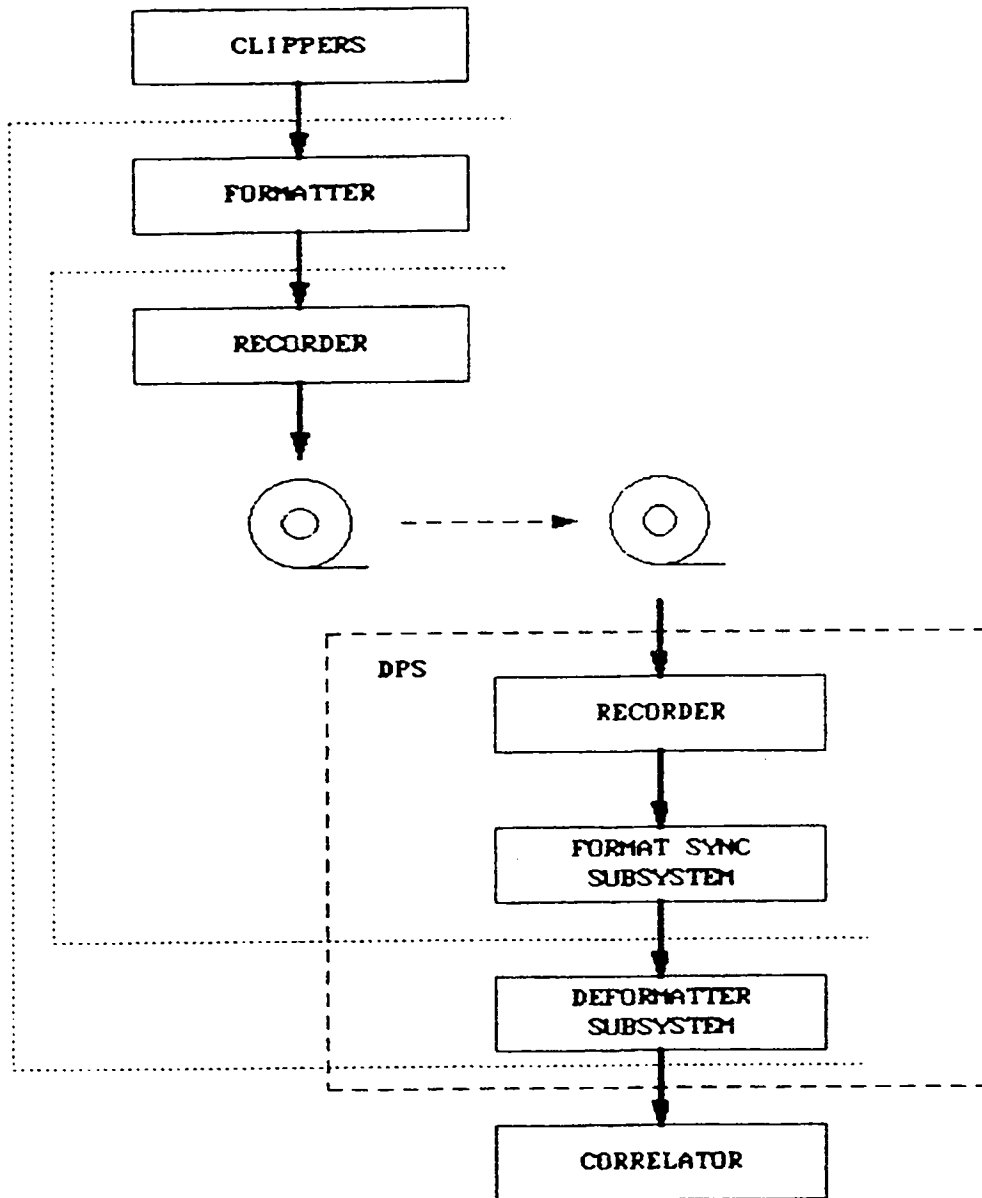
ONE TIME SETUP COSTS

WIRE-WRAP PANEL TOOLING	\$2500.00
WIRE-WRAP SETUP	\$2000.00
WIRE-WRAP REWORK	\$1500.00
BACKPLANE LAYOUT	\$1500.00
<hr/>	
total 'one time' setup cost...	\$7500.00

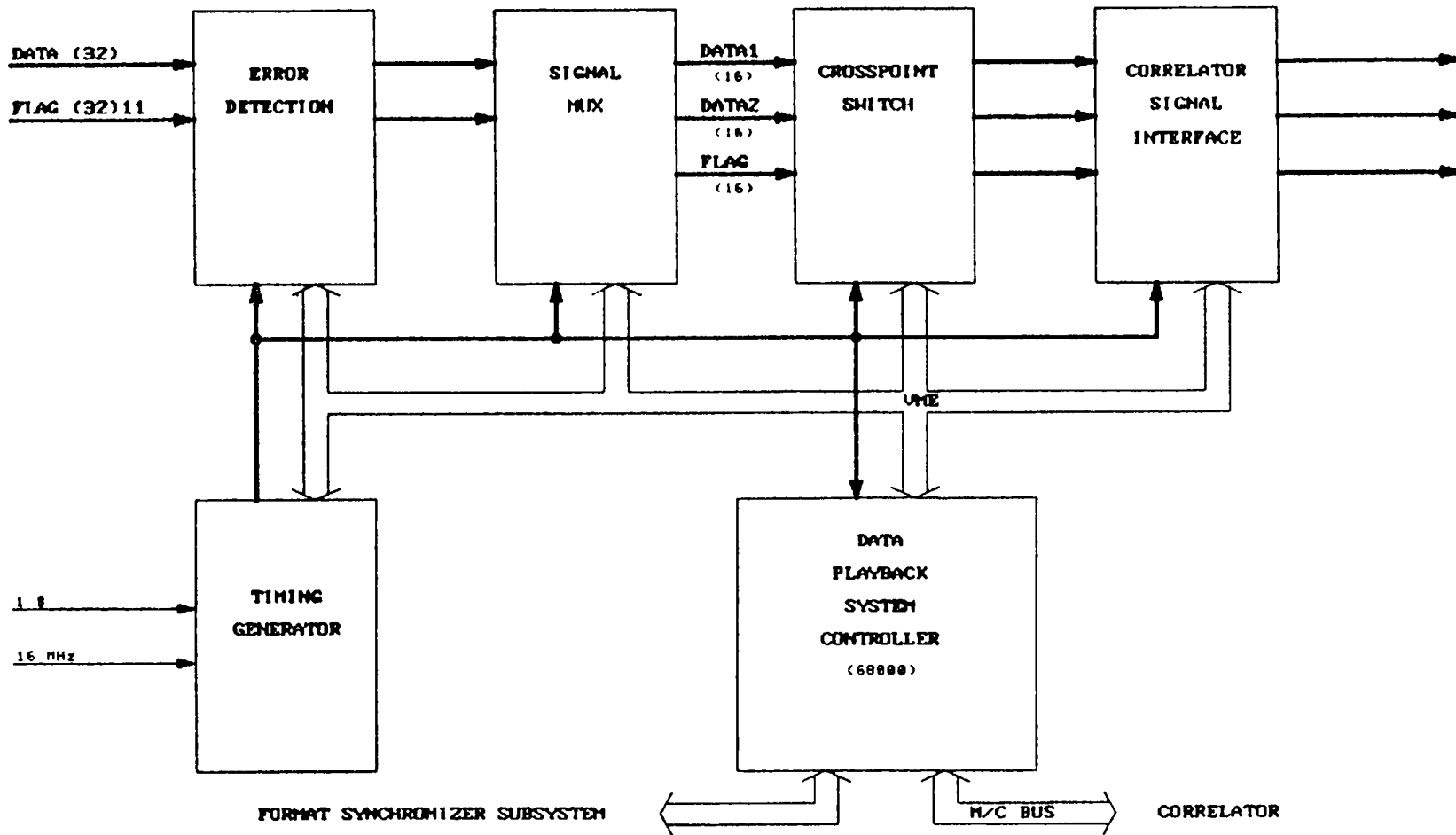
*** NOTE *** NOT INCLUDED IN COST ESTIMATES.....

POWER SUPPLIES
A/D CONVERTERS
FREQUENCY SYNTHESIZERS
PANEL DISPLAYS

9.3 DPS Block Diagrams

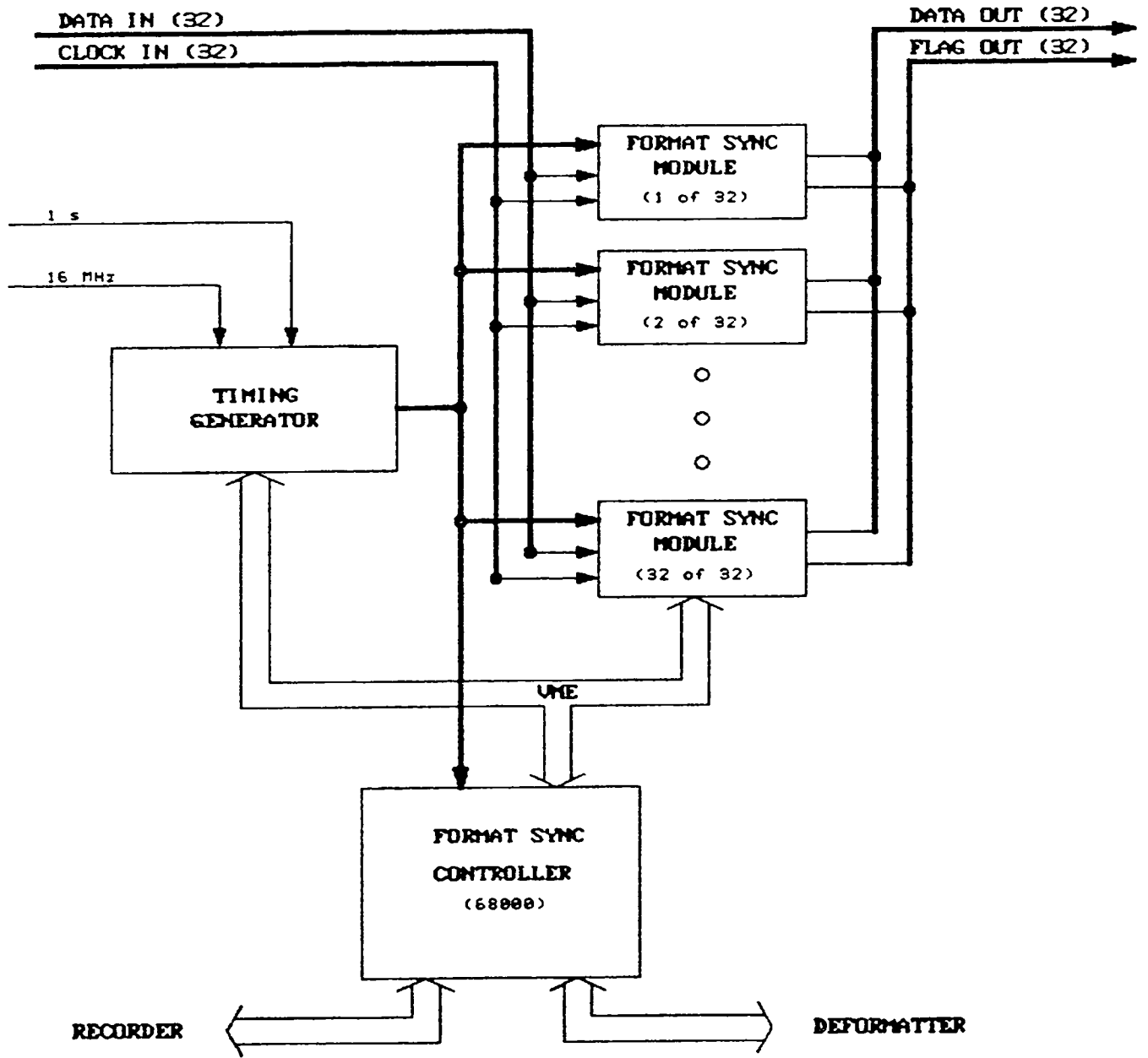


DATA PLAYBACK SYSTEM (DPS) FUNCTIONAL OVERVIEW



DEFORMATTER SUBSYSTEM

Figure 9.3-2



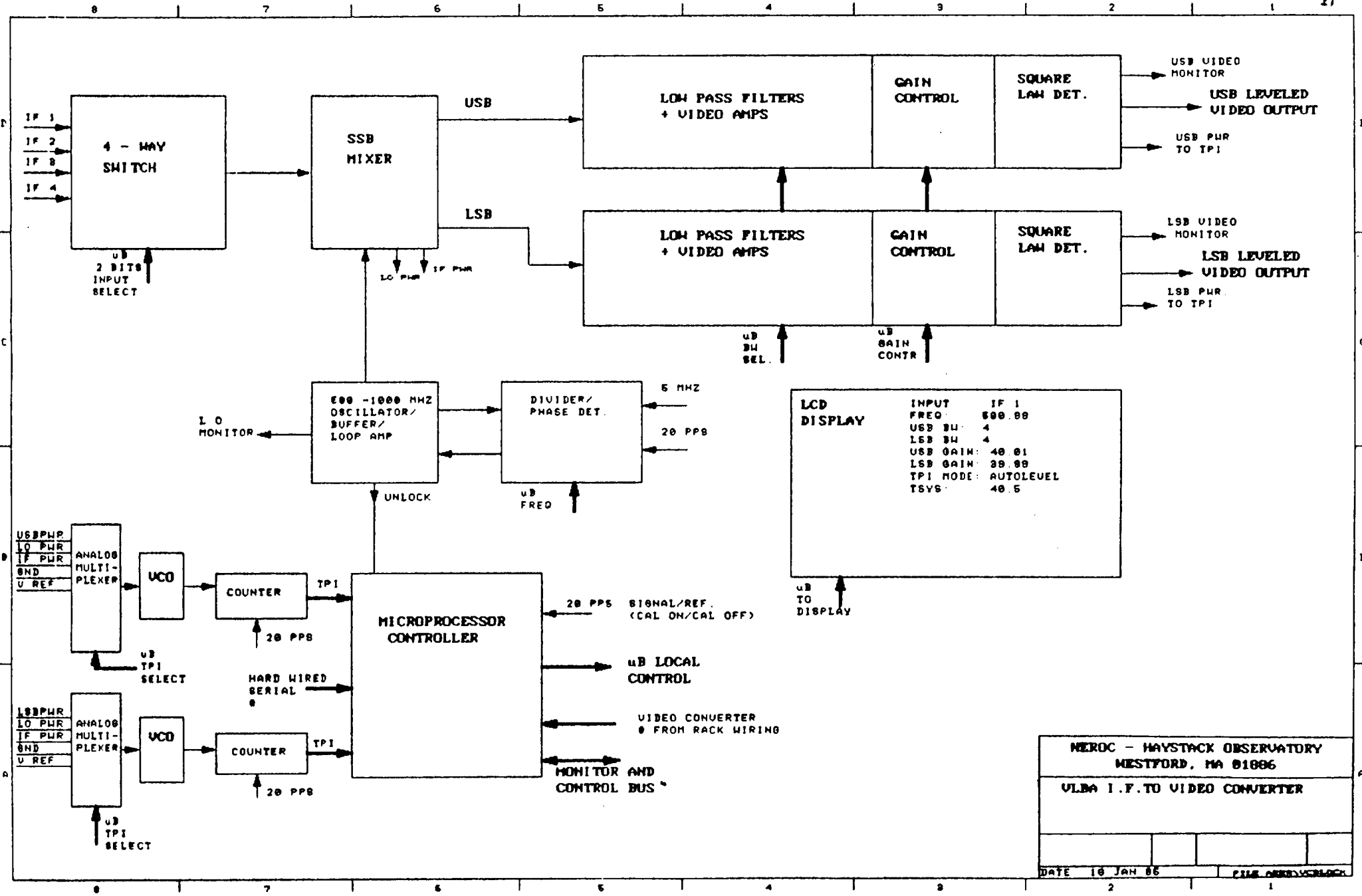
FORMAT SYNCHRONIZATION SUBSYSTEM

Figure 9.3-3

DPS COST BREAKDOWN

Format Sync 100 ICS/trk = 500/trk = \$16,000*	
Memory	1,500
up	1,500
Error Detection	1,500
Signal Mux	1,300
Cross-point switch	3,000
Correlator Interface	1,300
Timing Generator	1,400
Communications	1,000
Miscellaneous	<u>1,500</u>
	\$30,000
With only 16 tracks	~\$20,900

*Based on cost of equivalent function in new MkIII correlator



NEROC - HAYSTACK OBSERVATORY
 WESTFORD, MA 01886

VLBA I.F. TO VIDEO CONVERTER

DATE 10 JAN 86		FILE	00000000

Figure 9.4-1

9.5 I.F. Distributor and Baseband Converter Cost Breakdown

I.F. Distributor:

8-way Splitter	100
Amplifiers	100
Precision Attenuator	400
Power Detector	50
Misc	100
Total	750

Baseband Converter:

4-way Input	200
SSB Mixer	300
Local Oscillator	100
ECL Logic IC's (10)	200
Low Pass Filters (16)	800
Video Amps	200
Voltage Controlled	
Attenuator	100
Counters	100
uP	300
Misc	200
Total	2,500 (Elimination of LSB Channel would reduce cost by ~500)

Digitization Rack:

Rack	1,000
Power Supplies	2,000
Bins, Cable, Etc.	2,000
Total	5,000