

MASSACHUSETTS INSTITUTE OF TECHNOLOGY  
 HAYSTACK OBSERVATORY  
 WESTFORD, MASSACHUSETTS 01886

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Area Code 617  
 692-4765

TO: VLBA Data Acquisition Group  
 FROM: A. E. E. Rogers  
 SUBJECT: Proposed VLBA Format

The longitudinal format on each track I propose for the VLBA is the MkIII format (shown in the attached figure) with the following changes:

1) Add 20 data bytes to make the total frame length of 2520 bytes or 22680 bits (including parity) so that the tape clock rate is 9.072 MHz compared with 9.000 MHz for the MkIII format. This change makes the VLBA format a non-data replacement format with 2.5 ms between the sample time of the first data bit in each frame at the 9.072 MHz tape clock rate.

2) Assign the first 6 bytes (12 digits) of BCD auxiliary data (assigned to ASCII transceiver in MkIII) as follows:

BCD digit	Function
0 (first digit)	Mode (Barrel roll, etc.)
1	Sideband and bit type (sign or magn)
2,3	Baseband Conv. #
4,5	Record head #
6,7	Pass # (as per memo from ARW & JCW)
8,9,10,11	Head offset in microns (as per memo)

3) The formatter error code (7th byte of Aux data) although assigned in MkIII is not really used and therefore I propose that this byte be designated as a "spare" for VLBA format to allow for future addition.

#### A) Barrel Roll

The barrel roll feature in the VLBA is a cyclic reassignment of baseband channels and only affects the proposed longitudinal format in that the roll bit is on and the baseband channel will be cycling.

#### B) Modulation

In the VLBA format the data bits are multiplied by a frame synchronized pseudo-random code and will have to be demodulated

following decoding. Like the barrel roll this feature only affects the interpretation of the longitudinal data.

#### C) Cross-Track Parity

The data on a system track can be recorded as the cross-track parity bits from the data on other tracks. Like the features above this feature only affects the interpretation of the longitudinal data.

#### D) Frame Editing Criteria Proposed to Meet VLBA Specifications

I propose that a frame be the smallest "data packet" that can be edited and that each frame be examined and flagged invalid under any of the following conditions:

- 1) The trailing (beginning of next frame) sync word is detected at the wrong place.
- 2) The following 28 bytes are compared with their "expected value":

The leading (beginning of current frame) and trailing sync words

The leading and trailing BCD time

The leading and trailing pass numbers

The leading and trailing baseband channels

and found to contain more than 2 bit errors (2 error threshold).

- 3) The parity error count for the frame exceeds five.

Initialization of the time (needed to compute the expected time and other quantities) occurs with positive (no errors) leading and trailing sync plus a valid CRC on leading and trailing sync block plus the expected difference between the leading and trailing BCD times.

This proposed editing procedure should ensure that virtually no out of sync data is passed to the processor and that the average number of incorrect bits be maintained under  $3E-4$ .

The editing is not so stringent that all data will be flagged invalid since only 28 bytes have to be within error threshold for a frame to pass editing condition 2.

#### E) Proposed Error Monitoring

- 1) Parity error count on all data.
  - 2) Parity error count on data flagged valid.
  - 3) Number of resyncs (sync word detected at wrong place)
  - 4) Number of missing syncs in all data.
  - 5) Number of missing syncs in data flagged valid.
  - 6) Number of CRC errors in all data.
  - 7) Number of CRC errors in data flagged valid.
  - 8) Number of frames flagged invalid
- F) Proposed Criteria for Transport Fault - Shutdown for Repair
- 1) Fraction of data flagged invalid exceeds 1%.
- G) More details on errors etc.

- 1) Probability that out of sync data is flagged valid

For a frame with out of sync data to be flagged valid the data within the frame has to lose and recover sync within 5 data bytes (since out of sync data produces parity errors - unless out of sync by an integral number of bytes and the frame will be flagged invalid by editing condition 3) or the 14 bytes of trailing "sync" block data tested under editing condition 2 has to appear valid (within 2 bits) even though it is out of sync. For the 36 bit sync word alone this event has a probability of  $9E-9$  per frame and when the additional 90 bits checked are added the probability must be essentially zero. The loss and recovery of sync within 5 bytes is unlikely and even if we assume that it happens in 0.1% of the frames the net effect is that only  $2E-6$  bits out of sync incorrectly flagged valid. In other words the editing conditions are stringent enough to make sure less than  $1E-5$  bits with errors are flagged valid.

- 2) Recorder bit error rate (BER) needed to ensure that less than 1% data are flagged invalid

Since one tape error (which produces 2 bit errors owing to NRZM encoding) is allowed the probability that editing condition 2 will cause data to be flagged invalid is

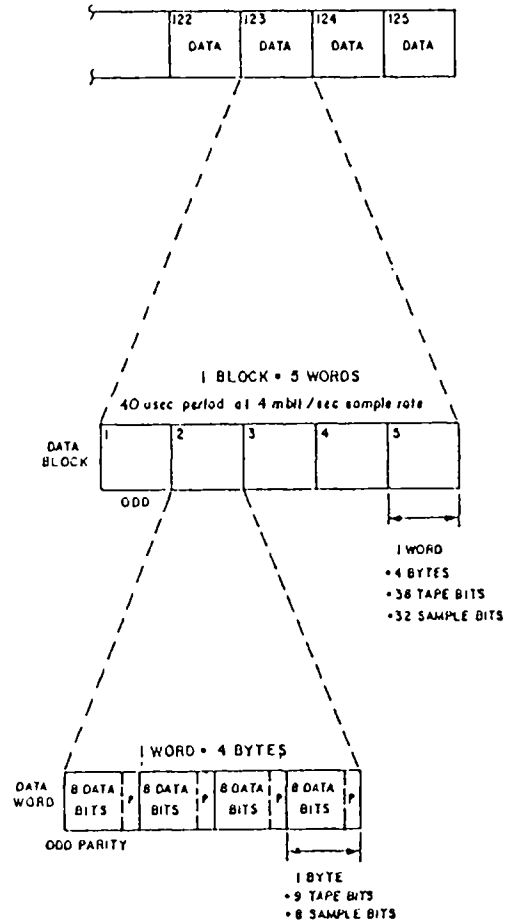
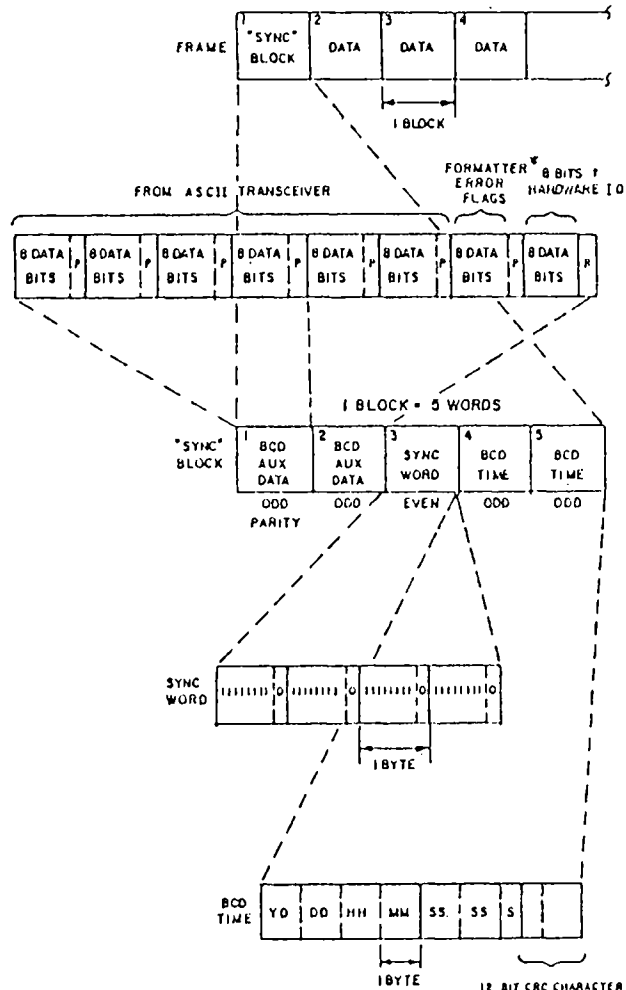
$$28 \times 9 \times 28 \times 9 \times \text{BER} \times \text{BER}$$

so that a BER of  $4E-4$  or better is needed to ensure that less than 1% of the frames fail editing condition 2. Since the editing condition 3 will flag data invalid at about the same BER a BER of better than  $3E-4$  is needed for more than 99% of the data to be flagged valid. If errors actually occur in bursts of several hundred bits as tests indicate the raw BER need not be as good by about an order of magnitude.

### 3) Implementation of frame editing

The calculation of the data validity could be accomplished by a microprocessor that is passed the 28 bytes and parity count from the decoder one frame in advance so that there is 2.5 ms to do the calculations.

1 FRAME = 125 BLOCKS (5 msec period at 4 Mbit/sec sample rate)



- FORMATTED ERROR FLAGS (00 DURING NORMAL OPERATION)
- BIT 0(SB) MODE (LSB)
- 1 — MODE (MSB)
  - 2 — DATA W (LSB)
  - 3 — DATA IN (MSB)
  - 4 — TIMING ERROR
  - 5 — FRAME ERROR
  - 6 — POWER FAIL
  - 7(MSB) SYNC TEST FAIL

- MODE DATA IN
- 0 - 'A'
  - 1 - 'B'
  - 2 - 'C'
  - 3 - 'D'
  - 0 - VIDEO
  - 1 - EXTERNAL
  - 2 - TEST
  - 3 - OFF
- T HARDWARE ID CODE SHOULD HAVE AT LEAST ONE BIT SET TO ZERO

### NOTES

THE 'SYNC BLOCK' REPLACES DATA.  
FIRST BIT OF 'SYNC BLOCK' CORRESPONDS TO THE TIME INDICATED BY 'SYNC BLOCK'.

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