VLBA ACQUISITION MEMO #169

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

HAYSTACK OBSERVATORY

WESTFORD, MASSACHUSETTS 01886

14 September 1989 *Area Code 508*

692-4764

To: VLBA Data Acquisition Group

From: Alan E.E. Rogers

Subject: Optimization of equalizer for playback of D1 tapes at 56 Kb/in

A] Equalizer circuit

An equalizer has been built and tested for playback of D1 tape at 160 IPS and 8 Mb/s per track (56K flux transitions/in). Figure 1 shows the equalizer circuit and Figure 2 shows the resulting "eye" pattern.

B] Equalizer phase and delay response

The amplitude and delay response is shown in Figure 3. Two sets of curves are shown giving the response with and without the 470 pf capacitor which provides low pass filtering of the high frequencies above the bandedge. In the new parallel playback electronics this low pass will probably be performed with a separate circuit.

C] SNR

The spectral signal to noise ratio (which is independent of the equalizer) is shown in Figure 2. The broadband signal to noise ratio is about 18 dB. The broadband SNR is dependent on the equalizer and is optimized by having an equalizer which weights the spectral SNR in proportion to the SNR - at least when the noise is only the random (thermal) portion. The bit error rate (BER) is dependent on a modified SNR which includes the intersymbol interference, due to imperfect waveform equalization, as a reduction of the available signal which competes with the noise in the decision process.

D] Optimization by manual adjustment

The equalizer was first optimized by substituting potentiometers for some of the resistors and a variable capacitor for the series resonant adjustment of C1,L. To the first order

C1	adjusts the peak frequency to bandedge
R1	adjusts the Q of the resonance
R2,C3	adjusts the mid frequency response
R3	adjusts the phasing between bandedge and midband
R4	adjusts the low frequency cut-off

Ideally the BER should be optimized but in practice it is convenient to watch a spectrum analyzer and "eye" pattern display.

E] Checking optimization by circuit simulation

A complete circuit simulation provides some useful added insight into the optimization. The following model was adopted

1] Generate pseudo random square wave with 8 MHz sample rate
2] FFT to frequency domain
3] Filter signal with
   a) Current source into parallel L=23 μH, C=8pf to simulate inductive pick-up of head and its resonance.
   b) Gap loss of 0.35 microns (see Acquisition Memo #150).
   c) Spacing of 0.35 microns.
4] Add noise filtered with head resonant circuit
5] Equalize signal plus noise
6] FFT to time domain
7] Develop an "eye" pattern
8] Measure signal from the opening of eye
9] Repeat with signal turned off to measure noise level and hence the SNR

Figure 4 shows some examples of the input signal, reconstructed waveform and "eye" patterns from the computer simulation. Noted are cases where the eye pattern is degraded by low frequency baseline wander and high frequency noise present without low pass filter.

Figure 5 gives the modified SNR from which the BER can be calculated as a function of various parameters.

F] The need for "DC restoration"

The need for "DC restoration" was described in a Haystack memo of 8 June 1988 (attached). A circuit for the DC restoration was tested and found to substantially improve the MKIIIA performance (by a factor of 10-100 in PER). However, owing to its complexity, the circuit has not yet been retrofitted into MKIIIA. An alternate and somewhat simpler circuit by W.D. Huber has been found (by Dan Smythe) in the IEEE Transactions on Magnetics, MAG-17, No.6, pg. 3352, 1981) and DC restoration is planned for the VLBA parallel reproduce electronics. The computer simulation confirms the advantage of DC restoration even for a random signal without long runs of zeroes.

G] The need for a low pass filter

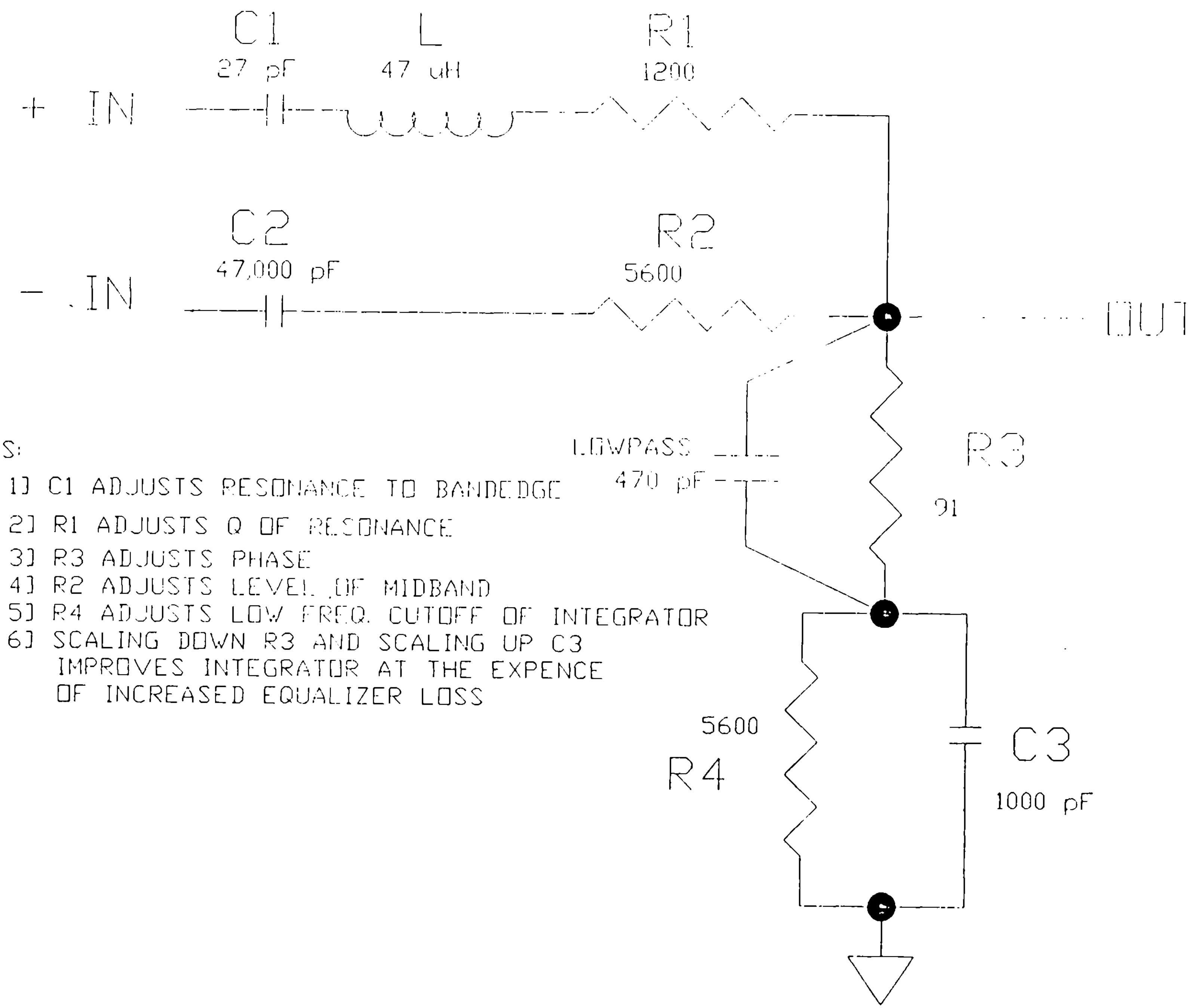
The high frequency noise (especially around head resonance) has to be more adequately filtered than it is in the present MKIIIA electronics. Adding one additional high frequency pole (with the 470 pf in the equalizer) may be adequate for the acquisition recorders - but even better performance can be achieved with an even better filter.

H] Equalizer dispersion

Ideally the equalizer should be non-dispersive. The delay characteristic has some ripple and increases rapidly below 70 KHz. The computer simulation shows that there are two problems with not allowing the integrator to go sufficiently low in frequency:

1] There is baseline wander.
2] Dispersion increases the intersymbol interference and degrades the eye pattern.

In order to optimize performance with DC restoration to reduce the effect of low frequency noise, it is advantageous to first extend the integrator to the lowest possible frequency to reduce dispersion. This can be accomplished by increasing C3 (and decreasing R3 to preserve the C3 R3 time constant) as much as possible while still maintaining acceptable loss in the equalizer.



NOTES:

1] C1 ADJUSTS RESONANCE TO BANDEDGE
2] R1 ADJUSTS Q OF RESONANCE
3] R3 ADJUSTS PHASE
4] R2 ADJUSTS LEVEL OF MIDBAND
5] R4 ADJUSTS LOW FREQ. CUTOFF OF INTEGRATOR
6] SCALING DOWN R3 AND SCALING UP C3 IMPROVES INTEGRATOR AT THE EXPENCE OF INCREASED EQUALIZER LOSS

FIG 1 DI 160 IPS EQUALIZER

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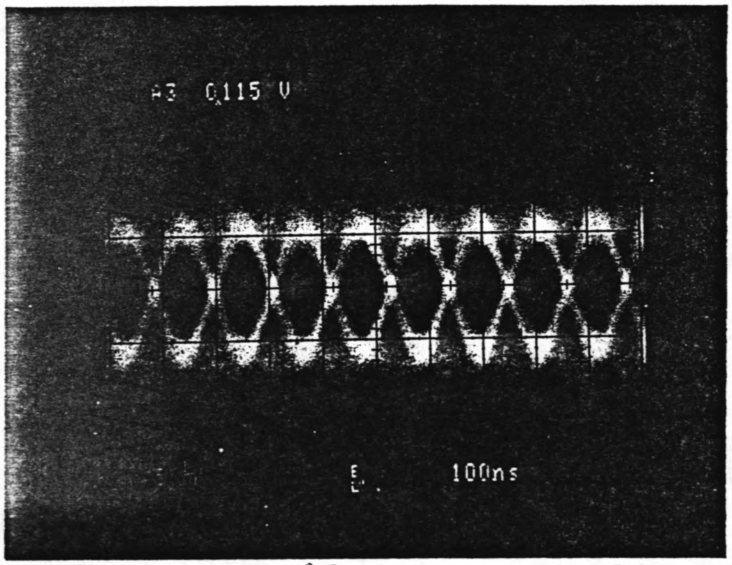
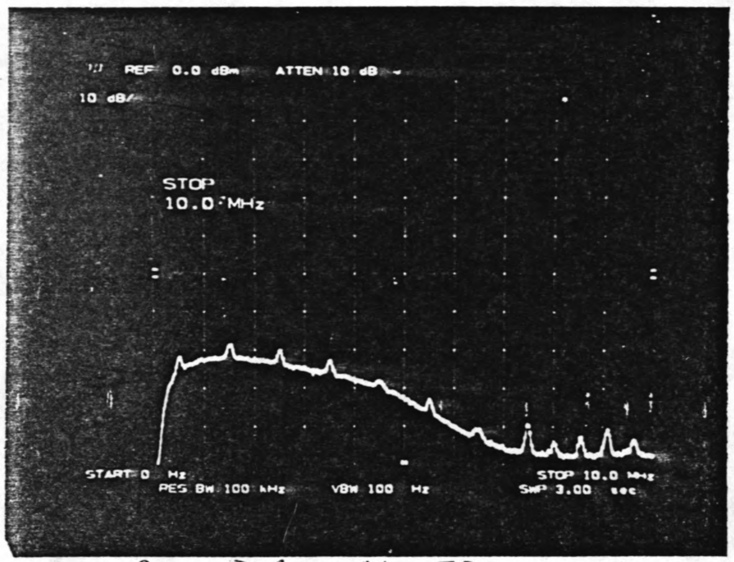
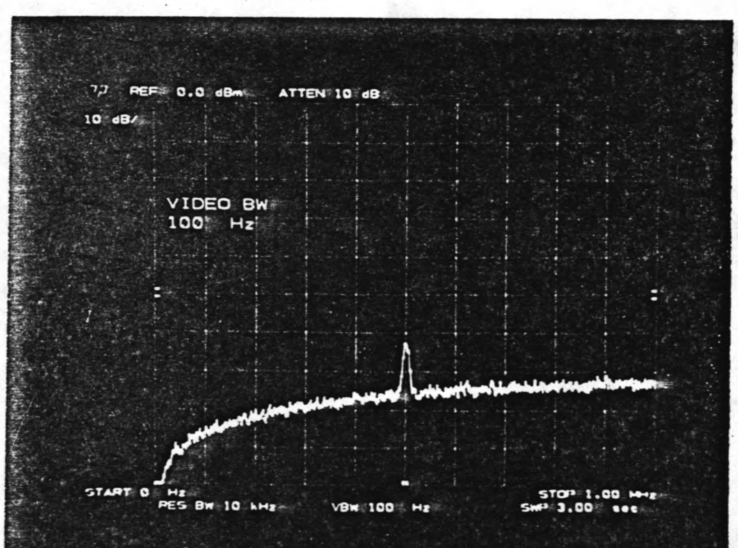


D1 160 IPS 12 SEPT 89



SNR D1 160 IPS 12 SEPT 89



SNR 160 IPS D1 12 SEPT 89

Figure 2
"EYE" Pattern
and spectral SNR
for D1 at 160 IPS
8 MHz sample rate

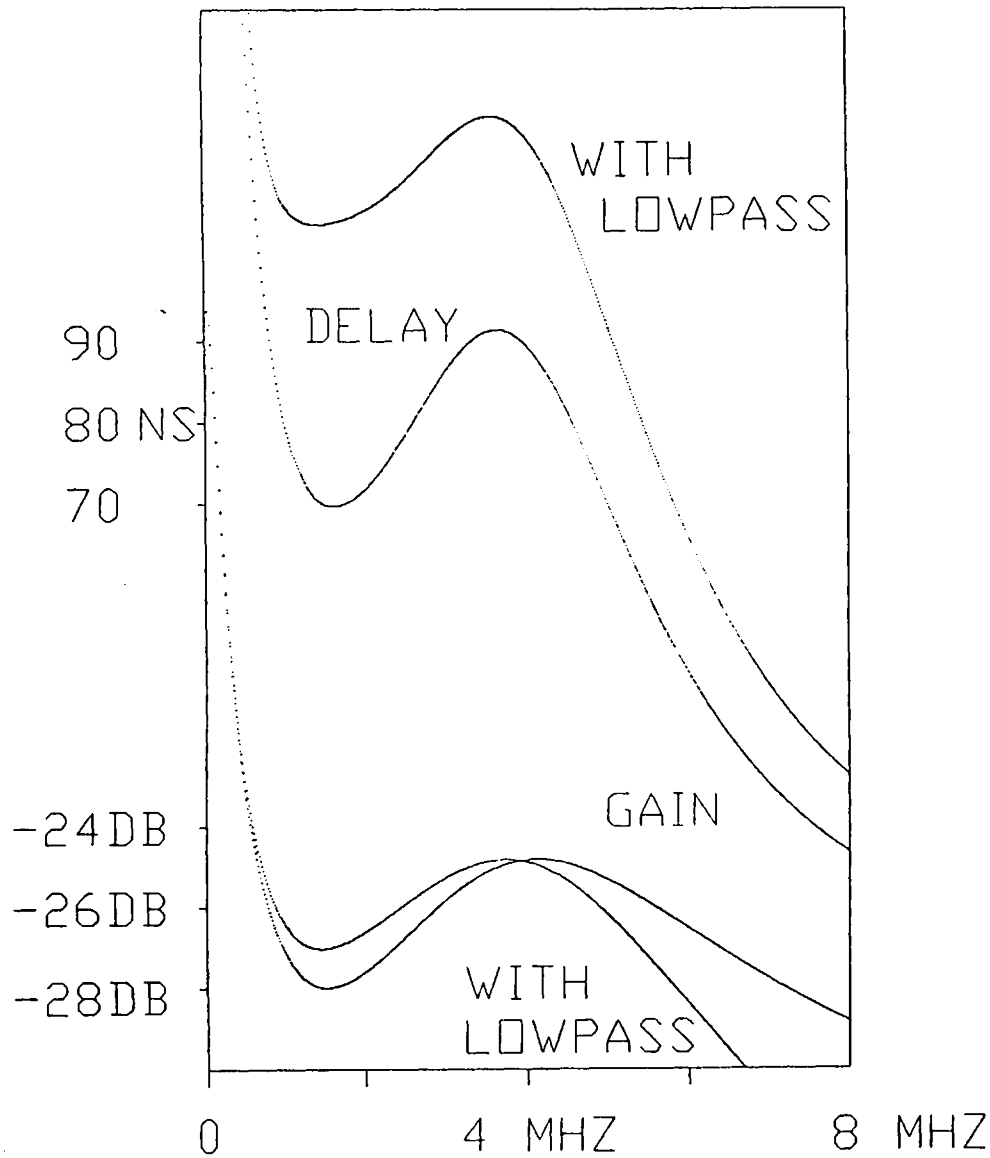


FIG 3 EQUALIZER AMPLITUDE AND DELAY RESPONSE WITH AND WITHOUT LOWPASS

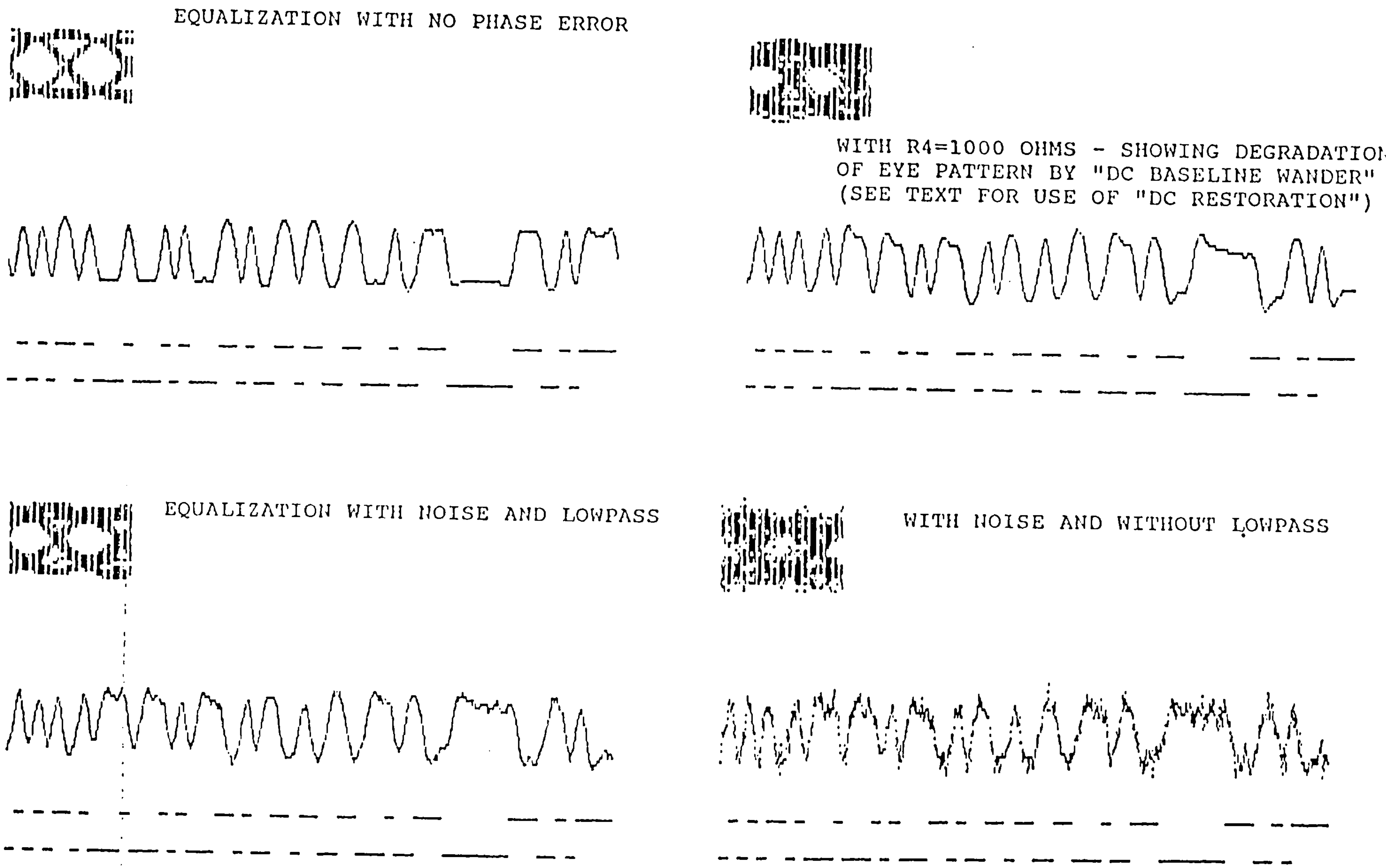


FIG 4 SOME SAMPLE "EYE" PATTERNS FROM COMPUTER SIMULATION

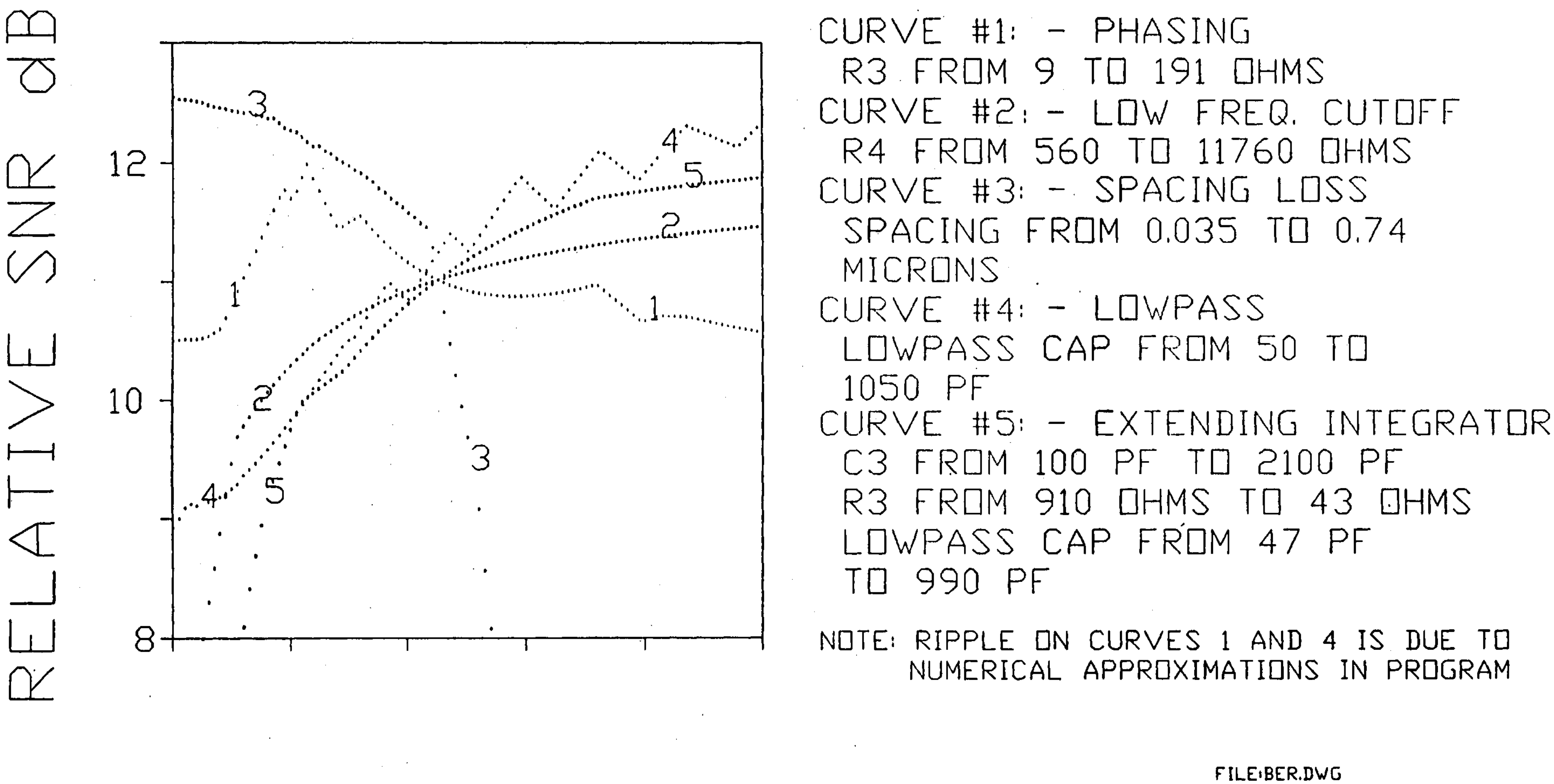


FIG 5 OPTIMIZATION CURVES

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

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WESTFORD, MASSACHUSETTS 01886

8 June 1988 *Area Code 508*
692-4764

To: VLBI Group

From: Alan E.E. Rogers
Hans F. Hinteregger

Subject: Narrow Track SNR Margin Equalization Improvements and the Use of D.C. Restoration

Introduction

We are studying the present MKIIA system in the hope that a few minor changes might lead to a substantial improvement in the margin over which the system will operate. So far we have found two areas which might yield some improvment as follows:

a) Limiting the analog response to 4 MHz (at 135 IPS playback) so that the noise from the head resonance at 12 MHz and high frequency noise pick-up doesn't degrade the broadband SNR.

b) Dynamic adjustment of the comparator threshold to reduce the errors produced by the inability of equalized signal to follow low frequency components.

Present Equalizer Limitations

The present equalizer whose transfer function is shown in Figure 1 has the low frequency roll-off of the equalizer set at about 40 KHz and as a result low frequency signals are poorly reproduced as illustrated by the "D.C." shifts shown in Figure 2. This problem is especially bad during the time code and auxilliary data portions of the frame and results in CRC errors. We recommend that more ones be encoded into the auxilliary data field when tapes are recorded. However the problem is not limited to the auxilliary data and additional measures are probably needed. Simply reducing the low frequency roll-off actually degrades the broadband SNR as the spectral SNR (shown in Figure 6) is degrading by 6 dB/octave at low frequencies.

D.C. Restoration

The effect of the D.C. shifts can be greatly reduced by adding positive and negative peak level detectors and using their mean to steer the reference on the comparator. Figure 3 shows both the equalized signal and the voltage mid-way between the positive and negative peaks.

Improved Equalizer

With a D.C. restoration circuit the low frequency response can actually be extended since the comparator reference now tracks low frequency components. In addition an additional high frequency cut-off has been added as illustrated in Figure 5.

Comparison Tests

The improved equalizer with D.C. restoration circuit was tested on the Westford acquisition recorder using a tape recorded at Hat Creek during the 3 mm experiment (which reproduced poorly on the processor). The results are shown in Figure 6.

The improved equalizer alone gives about a factor of two improvement in error rate while the combination of better equalizer plus D.C. restoration gives about 10-100 fold improvement in error rate.

Conclusions

Unfortunately the circuit changes needed to implement D.C. restoration are fairly extensive. The next step is to test the prototype on the processor and if the improvement is dramatic look for simpler ways of achieving the same result. This study indicates that the present margin (to 0.1% error rate) on the Hat Creek tapes is about 3 dB and increases to about 5 dB with improved equalization and D.C. restoration.

Attachments (5 Figures)

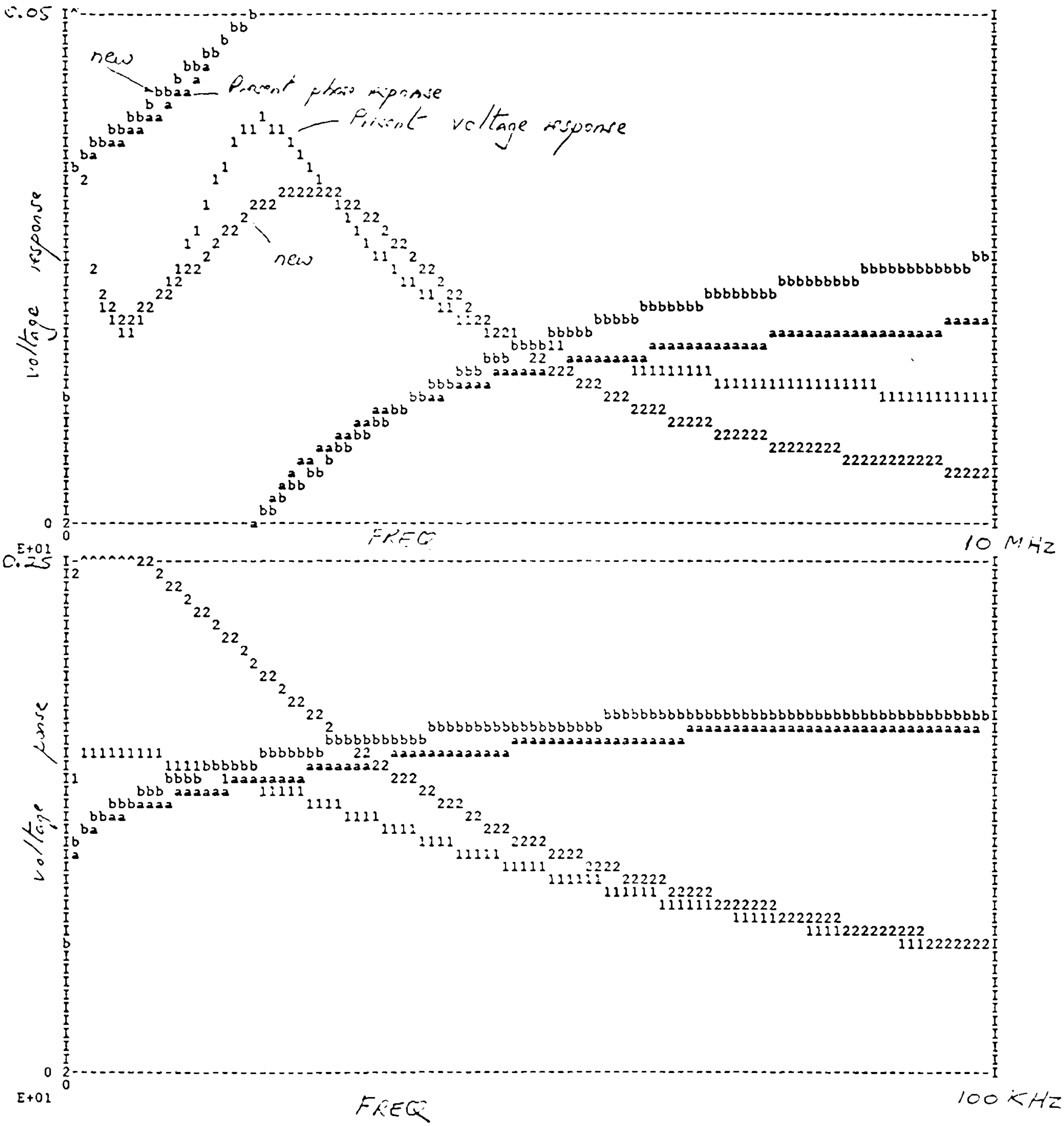
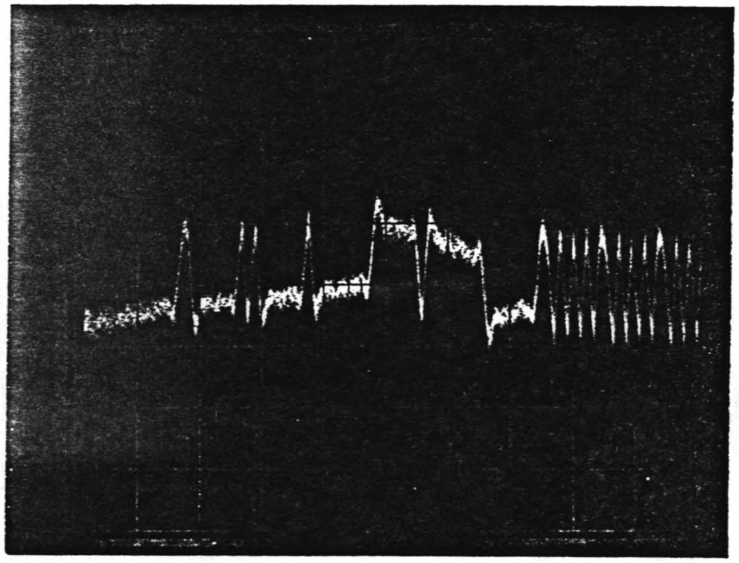
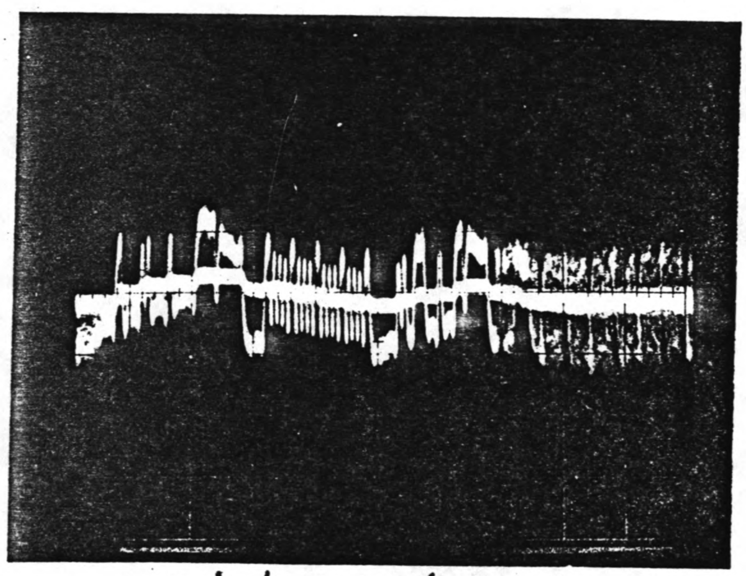


Figure 1. Equalizer response



ORIGINAL EQ.

Figure 2. Equalized signal going to comparator (scope sync. on frame sync.) showing significant "D.C." shifts which result from equalizer integration failing to extend low enough in frequency.



≃ factor 10. redn. in PE & SYNC.

Figure 3. Equalized signal along with $(V^{+}_{peak} + V^{-}_{peak})/2$ used to restore D.C. component the comparator.

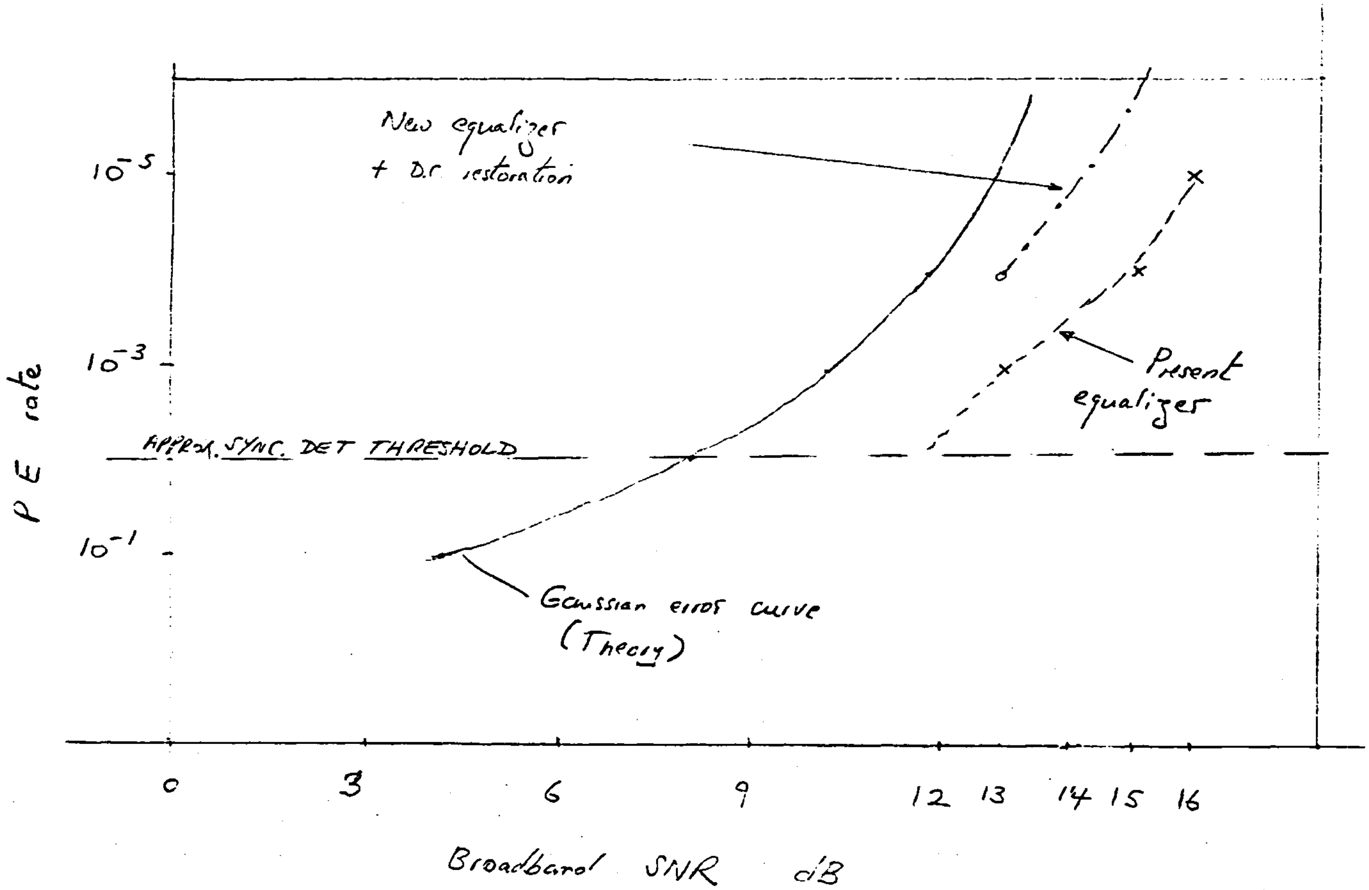
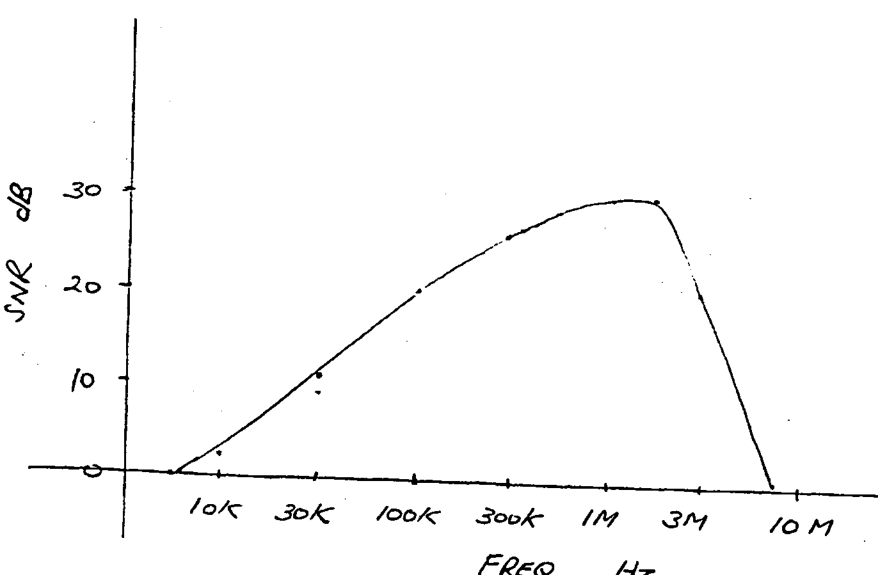


Figure 4. New equalizer plus D.C. restoration offers an improvement in parity error rate of about 10 – 100, a reduction in CRC error rate (probably by ≈ 10 – 100) and a reduction in sync. loss by approx 2. [The equivalent SNR improvement approx. 2 - 3 dB]



6 MHz	3 dB
4 MHz	5 dB
2 MHz	30 dB
1 MHz	30 dB
500 KHz	30 dB
250 KHz	26 dB
100 KHz	20 dB
50 KHz	15 dB
25 KHz	9 dB
10 KHz	3 dB

Figure 5. SNR vs frequency

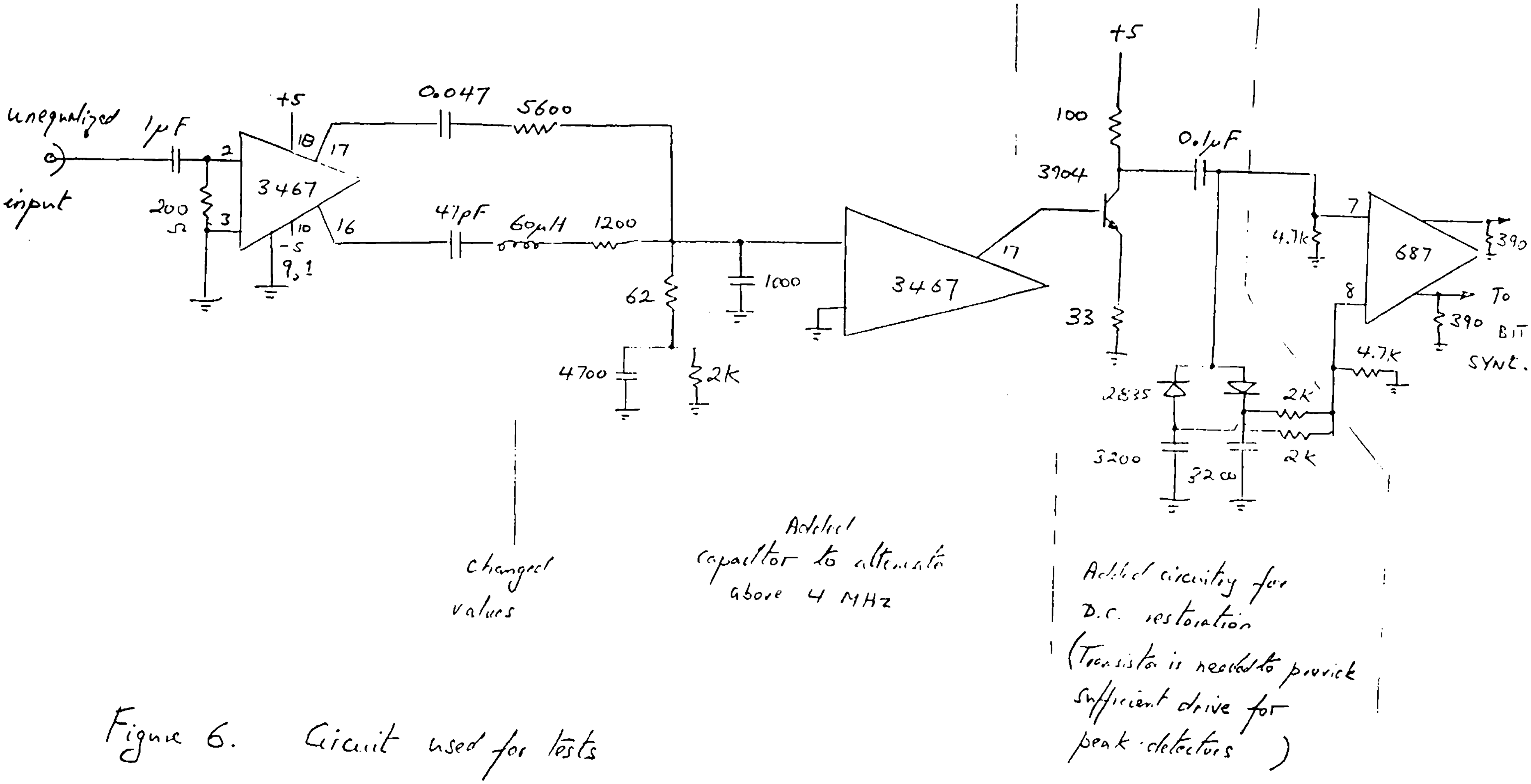


Figure 6. Circuit used for tests