VLBA ACQUISITION MEMO #249

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

HAYSTACK OBSERVATORY

WESTFORD, MASSACHUSETTS 01886

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Telephone: 508-692-4764
Fax: 617-981-0590

To: VLBA Data Acquisition Group

From: Alan E.E. Rogers
Edwin F. Nesman

Subject: Proposed redesign of the formatter A/D buffer module

Introduction

The present A/D buffer module includes a 32x32 cross-point switch for the sampler to recorder track assignments. It also contains the multi- and demulti-plex logic for fan-in and fan-out. The block diagram is shown in drawing #54202-K-1/3. The cross-point switch uses analog chips as large digital cross-point switches were not available when the formatter was designed in 1987/88. The analog switch does have some limitations due to the high capacitance of the elements (see VLBA Acquisition Memo #235). A redesigned module would use a digital switch to remove all restrictions on the track assignments as well as including added capabilities, like phase calibration tone extraction.

We suggest that a new A/D board design is better than separate A/D and Pcal extractor boards for the following reasons:

1] Present cabling arrangement to the front of the module can be preserved.
2] You do not have to have an expanded system. Only one A/D/Pcal board is required for the support of one recorder.
3] In an expanded system there is the redundancy of two identical boards.
4] Only one new board need be designed.

Proposed new block diagram

The new block diagram shown in preliminary drawing 54202-K, Rev. 2 would perform all the same tasks as the original module as well as including phase calibration extraction (see VLBA Acquisition Memo #248 for details) with the following performance specifications:

Tone frequencies:	D.C. to 16 MHz in 10 KHz steps (D.C. used for sampler threshold measurements)
Number of tones: (simultaneously)	4 with 4-bit sine/cosine table 8 with 2-bit sine/cosine table 16 with 1-bit sine/cosine table or any combination requiring no more than 32 (32-bit) accumulating counters.

Input switch to tone extractions:	32x16 cross-point switch so that any tone extractor input can be connected to any sampler output. Also tone extractors can be connected to a fixed 0 or 1 for test and table loading.
Maximum time to change input selection:	1 millisecond
Maximim time to load tables with new frequencies:	1 second
Maximum accumulation period:	120 seconds
Dead time between accumulation periods:	< 10 ms

Flexibility examples:

1] 8 tone extractors (in 1-bit sine/cosine table mode) looking at 4010 KHz in USB sign bit ouputs + 8 tone extractors looking at 3990 KHz in LSB sign bit outputs. This could extract the central phase cal tones in all the 8 MHz bandwidth outputs for 8 BBCs.

2] 4 tone extractors (in 4-bit mode) looking at 10, 1010, 2010, 3990 KHz sine and magnitude bits from a single 4 MHz USB output.

3] 4 tone extractors (in 2-bit mode) looking at 10 KHz from 4 USB sign and magnitude bit outputs + 4 tone extractors looking at threshold levels of the sine and magnitude bits of the same 4 USB outputs.

Major parts/board

Part	Number Required	Approx. Board Area Sq. Inch	Cost
SRAM (16K x 4)	8	6	120
32 x 32 Cross-point	2	5	200
32-bit counters	32	6/22[1]	550/225[1]
Microcontrollers	1	1	100
Miscellaneous	100	20	500
TOTALS		38/54[1]	1470/1145[1]

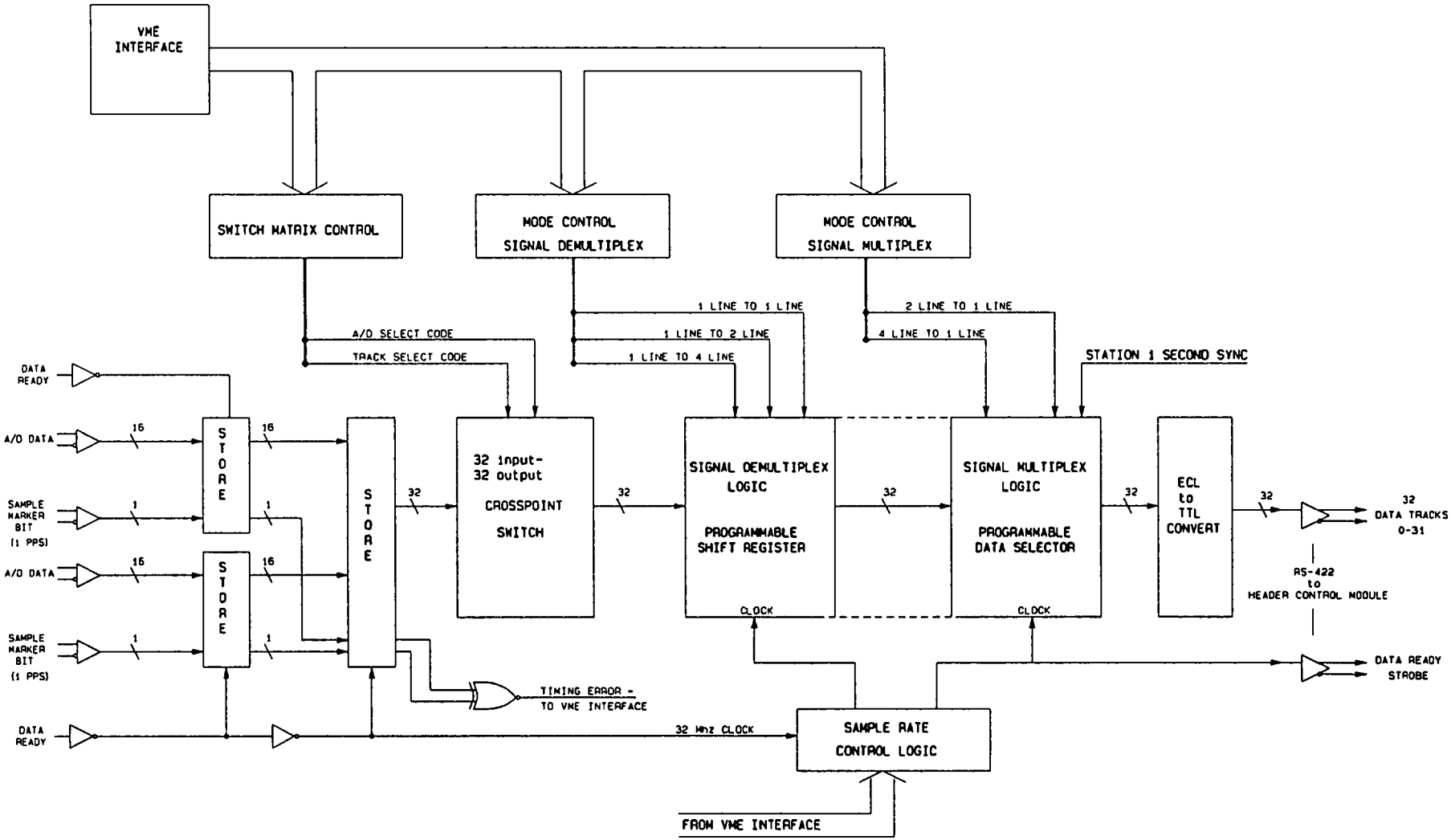
Engineering design time and replication cost

We estimate 6 man-months for engineering (including firmware), a prototype materials and services cost of about $5000, and a replication cost of about $3500, per board It would probably take nine months to one year from now until we have a fully tested prototype.

[1]Using LSI counters instead of one Xilinx chip for 16 counters.

file: 54202K01.DWG

A/D BUFFER MODULE - BLOCK DIAGRAM



21-NOV-88 CONVERT TO DASH-4 FORMAT JJL

PROTOTYPE 21-JAN-88

DR	J.I Levine	21-JAN-88
CHK	J.I Levine	21-JAN-88
ENGR		
PROJ		
PROD		

NEROC - HAYSTACK OBSERVATORY
WESTFORD, MA 01886

BLOCK DIAGRAM - VLBA
A/D BUFFER MODULE

MODULE	SIZE	DWG. NO.	REV.
A/D	C	C-54202-K	1

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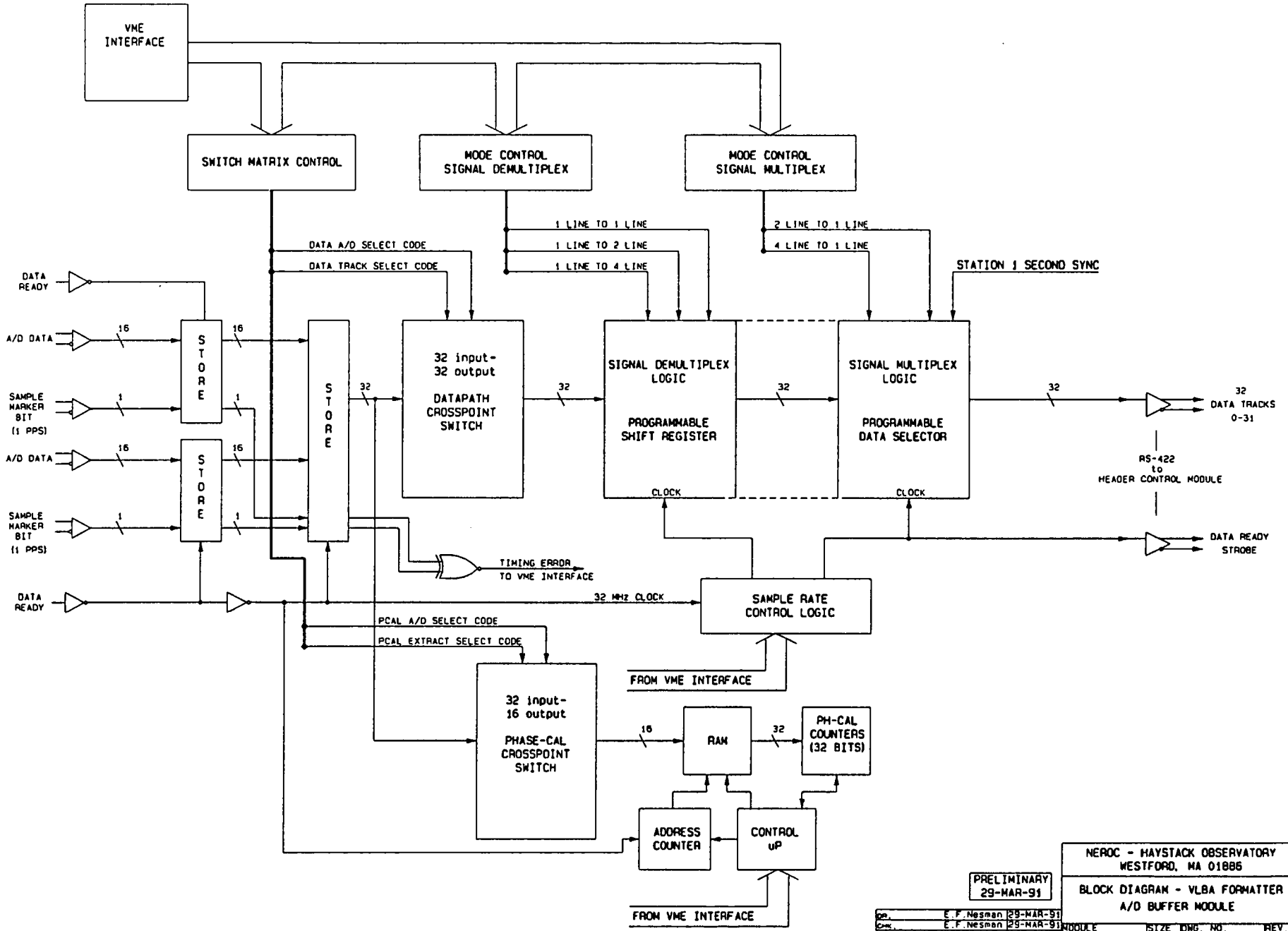
file: 54202K01.DWG

A/D BUFFER MODULE - BLOCK DIAGRAM



PRELIMINARY
29-MAR-91

DR.	E.F.Nesman	29-MAR-91
CHK.	E.F.Nesman	29-MAR-91
ENGR.		
PROJ.		
PROD.		

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BLOCK DIAGRAM - VLBA FORMATTER
A/D BUFFER MODULE

MODULE	SIZE	DWG. NO.	REV.
A/D	C	C-54202-K	2

DATE 21-JAN-88 SHEET 01 OF 03