VLBA ACQUISITION MEMO # 311

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

HAYSTACK OBSERVATORY

WESTFORD, MASSACHUSETTS 01886

28 May 1992

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To: Distribution

From: E. Nesman, V. Tran, K. Wilson

Subject: Recorder Controller Monitor Board Changes

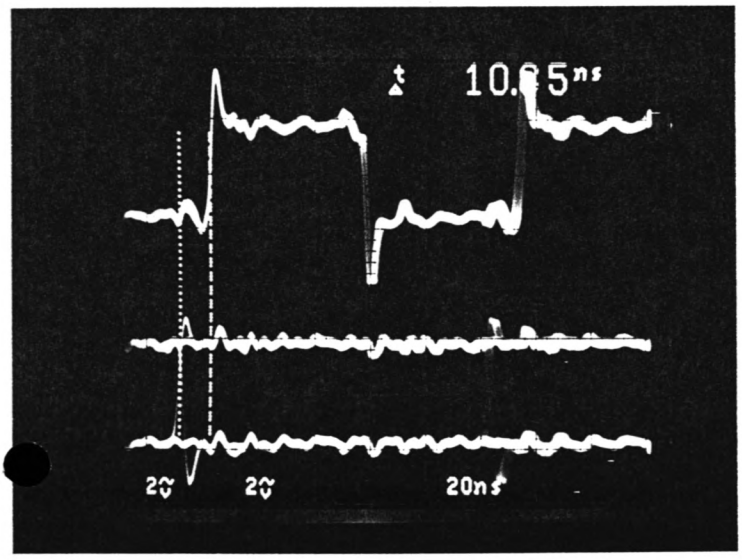
Problems have been identified in two different areas of the recorder controller monitor board--monitor input signal termination resistor wiring and malfuntion of the data extractor logic. These problems are addressed in the following sections, with information on engineering changes, field modifications, and production documention changes given for each area.

Engineering Changes

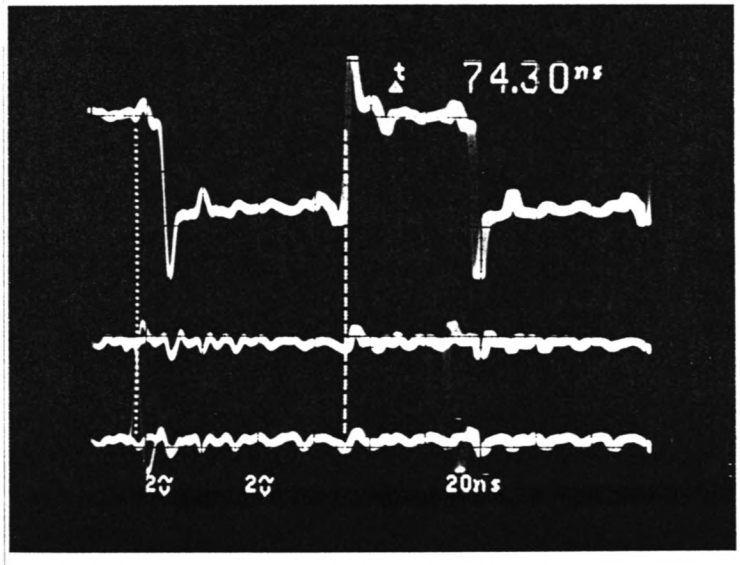
1. Monitor Input Terminations: A symbol pinout error exists on drawing C54328L004, wherein pins 2 And 3 are reversed on the SIP resistors at locations 1261 and 3161. This drawing has been corrected and re-released as Rev. A.

2. Data Extractor Malfunctions: The primary reason for the large number of faulty production boards was determined to be bad TI 74ALS86 IC's at location 5709. The bad IC's bear 1986 production date codes. This investigation also brought to light a marginal "data set-up time" situation at the NRZM decoder (74ALS175 at location 5720); this problem is corrected by inverting the clock as supplied to the clock distributor (74AS244 at location 6020). The inversion is implemented with a spare section of the 74ALS86 previously referenced. The set-up time is improved from a marginal 11 ns to about 74 ns. (See oscilloscope photos below.) Drawing C54328L006 has been revised to reflect this change and re-released as Rev. A.

Original



With Inverter



Field Modifications

1. Monitor Input Terminations: This error can be corrected by performing the wire-wrap changes listed below.

Remove List

From	To	Wrap Level
1163	1262	2
1061	1263	2
1263	J1-04	1
3463	3162	2
3261	3163	2
3163	J2-04	1

Add List

From	To	Wrap Level
J1-04	1262	1
1262	1061	2
1263	1163	2
J2-04	3162	1
3162	3261	2
3163	3463	2

2. Data Extractor Malfunctions: All monitor panels should be inspected for the presence of TI 74ALS86's with 1986 production date codes. All such devices should be replaced. The clock inverter can be added by performing the wire-wrap changes listed below.

Remove List

From	To	Wrap Level
6027	6140	1

Add List

From	To	Wrap Level
5720	5713	2
6140	5712	1
6027	5714	1

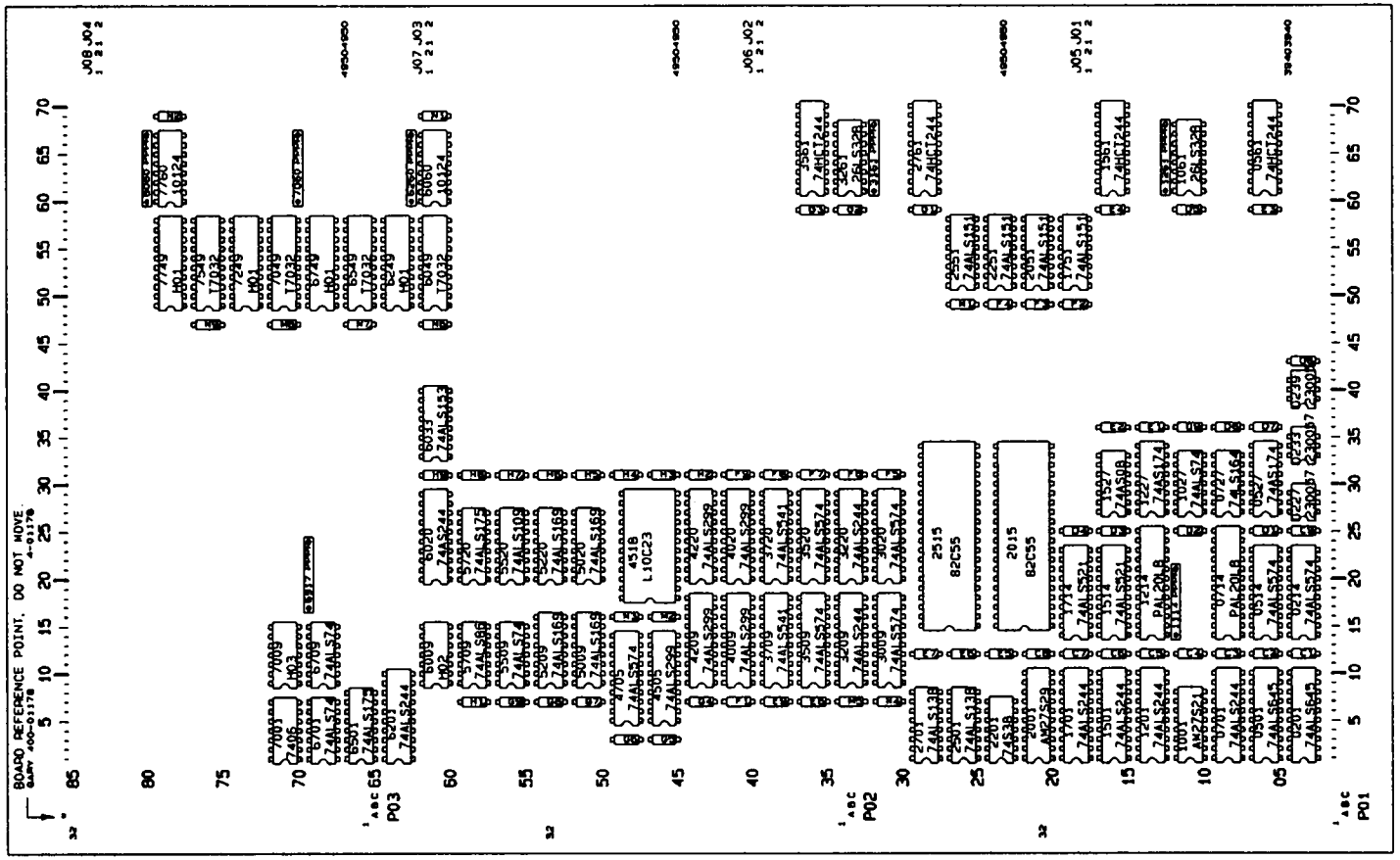
Production Documentation Changes

As mentioned above, logic diagrams C54328L004 and C54328L006 have been changed and re-released as Rev. A. A revised netlist has been generated and a "WRAPID" format wirelist (54328.wrp, rev. 2) has been recompiled for use on the next production run.

Timing diagram C54328V003 has been revised to reflect the use of the AT&T clock recovery IC and re-released as Rev. A. Also, assembly drawings C54328A001 and C54328A002 have been changed to show AT&T T7032 IC's instead of T7033 and re-released as Rev. A. Either type is acceptable in this application; however, the T7033 is no longer available. Block diagram C54328K001 has been revised to show the correct drawing number in the title block and re-released as Rev. A.

file: C328A001.DWG dwg: MONITOR MODULE - WRAPID BOARD LAYOUT

REV: A ENGR. E.F.Nesman 22-MAY-92



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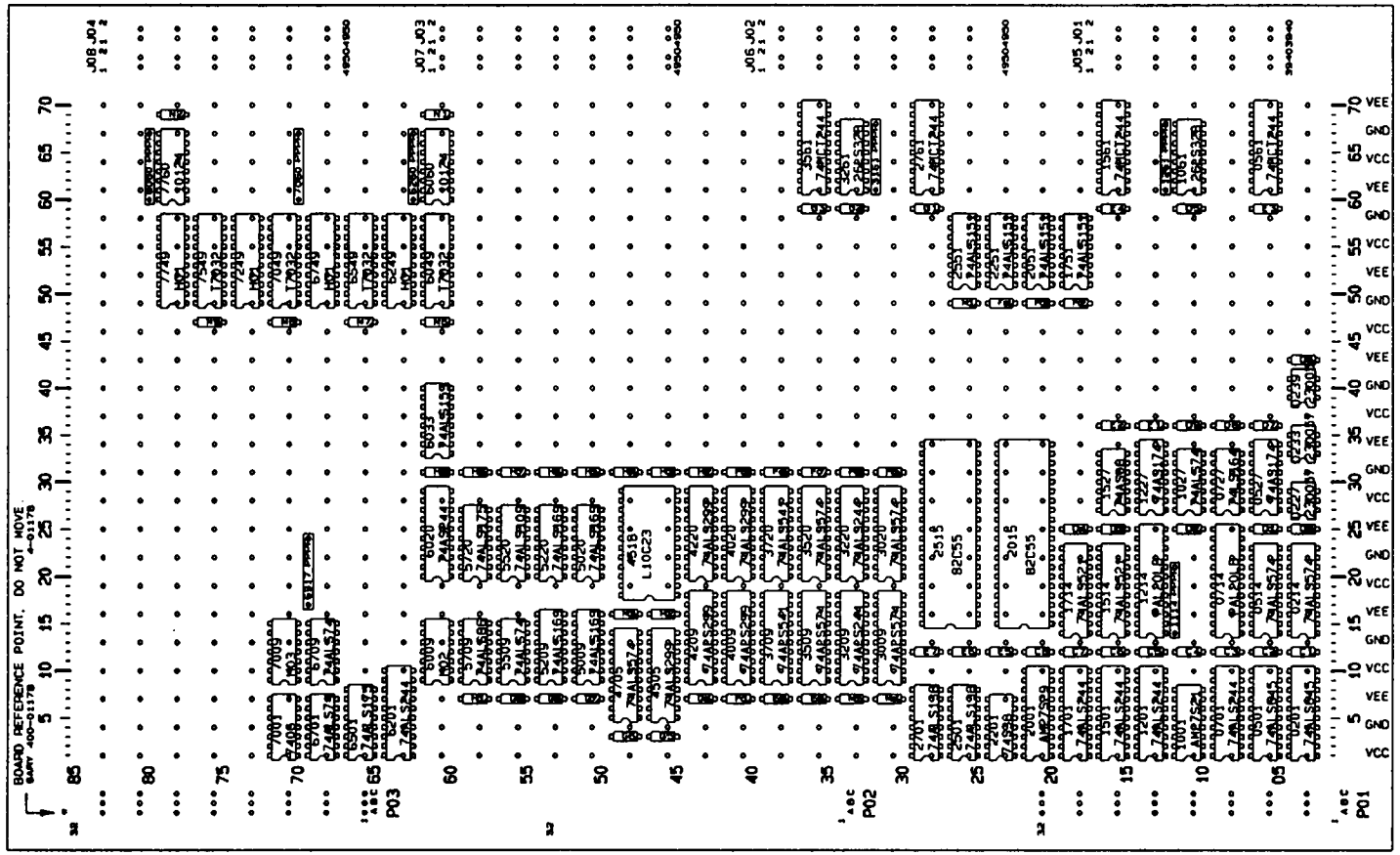
WESTFORD, MA 01886

VLBA RECORDER - BOARD ASSEMBLY
VME CONTROLLER - MONITOR MODULE
WRAPID BOARD LAYOUT

DR	E.F.Nesman 21-NOV-90			
CHK	E.F.Nesman 30-MAY-91			
ENGR	E.F.Nesman 21-OCT-91	MODULE	SIZE	DWG NO	REV
PROJ	A E E Rogers 21-OCT-91	MONITOR	C	C54328A001	A
PROD		DATE 21-OCT-91	SHEET 01 OF 08		

file: C328A002.DWG | dwg: MONITOR MOD. COMPONENT PANEL - PWR PIN LOCATIONS

REV: A ENGR. E.F.Nesman 22-MAY-92



MAY 27 1992

DR.	E.F.Nesman	21-NOV-90
CHK.	E.F.Nesman	30-MAY-91
ENGR	E.F.Nesman	21-OCT-91
PROJ.	A.E.E. Rogers	21-OCT-91
PROD.		

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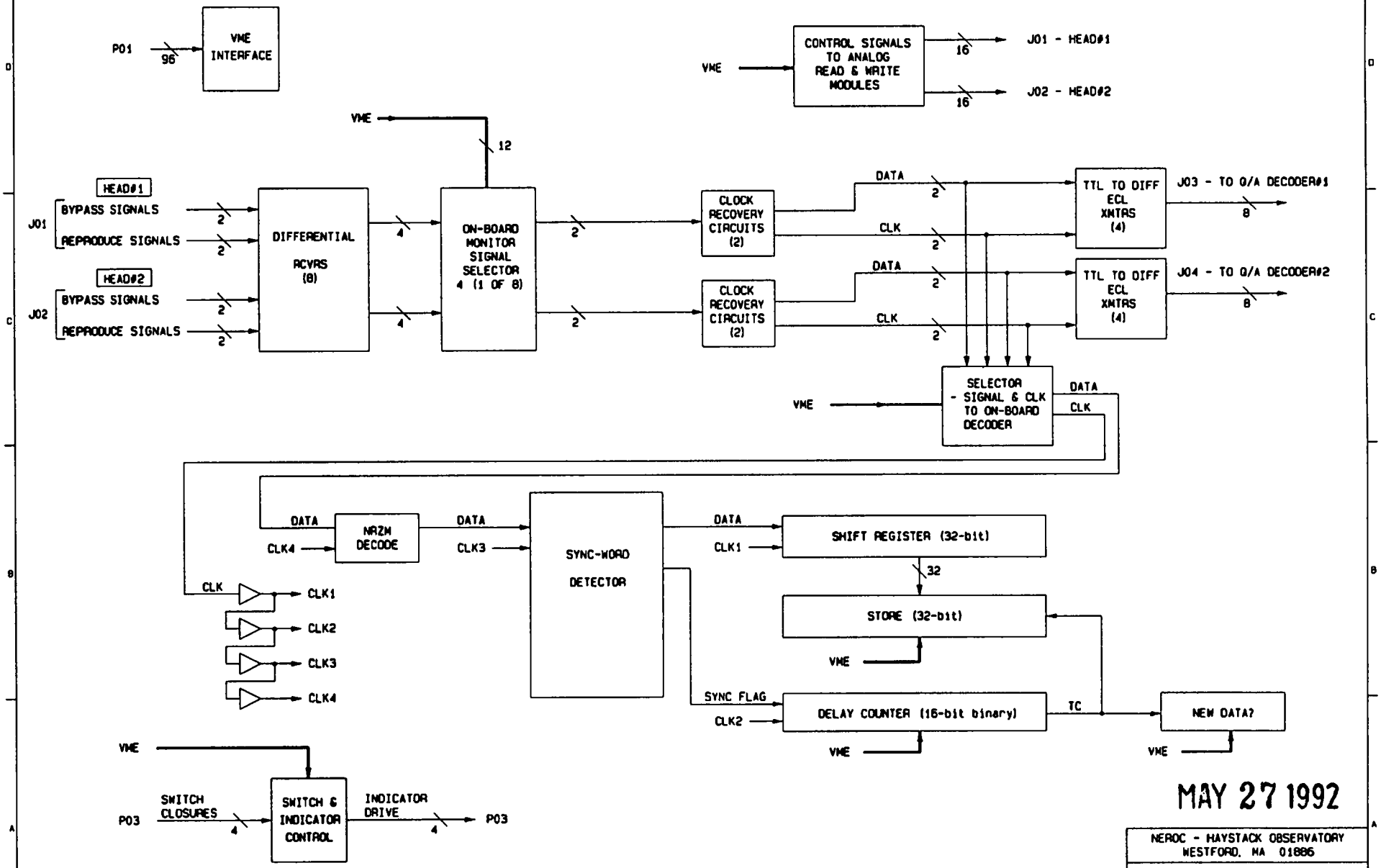
VLBA RECORDER - BOARD ASSEMBLY
VME CONTROLLER - MONITOR MODULE
COMPONENT PANEL PWR PIN LOCATIONS

MODULE	SIZE	DWG. NO	REV
MONITOR	C	C54328A002	A
DATE 21-OCT-91		SHEET 02 OF 06	

File: C328K001.DWG Dwg: MONITOR MODULE - BLOCK DIAGRAM

REV A Engr. E.F.Nesman 22-MAY-92



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VLBA RECORDER - BLOCK DIAGRAM
VME CONTROLLER - MONITOR MODULE

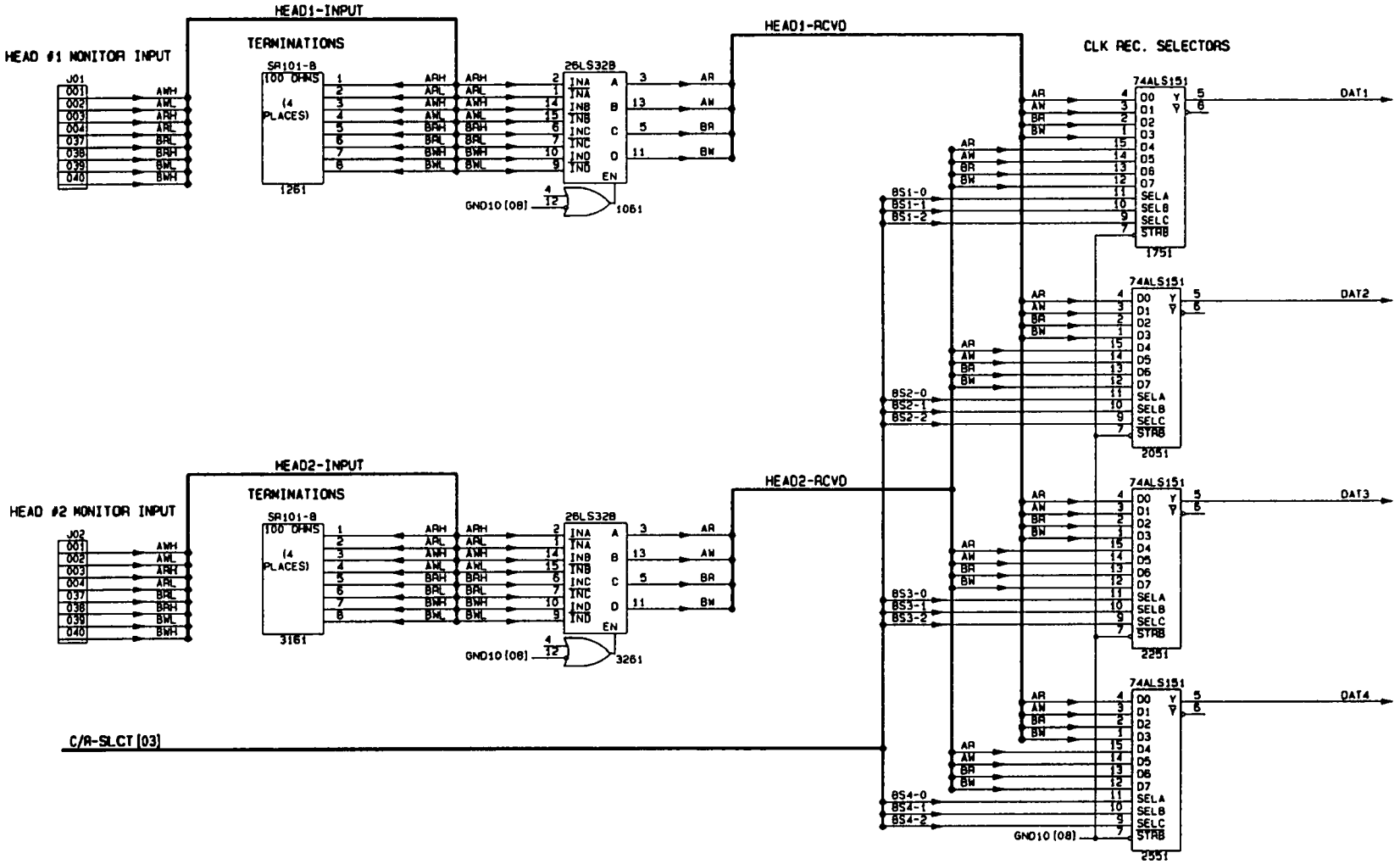
Dr.	E.F. Nesman	05-DEC-90
Chk.	E.F. Nesman	05-JUN-91
Engr.	E.F. Nesman	21-OCT-91
Proj.	A.E.E. Rogers	21-OCT-91
Prog.		

MODULE	SIZE	DWG NO.	REV
MONITOR	C	C54328K001	A

DATE 21-OCT-91 SHEET 01 OF 01

File: C328L004.DWG | Dwg: MONITOR MODULE - RECEIVERS & CLK REC. SELECTORS

REV: A | ENGR. E.F.Nesman 22-MAY-92



MAY 27 1992

DR.	E.F. Nesman	26-OCT-90	
CHK.	E.F. Nesman	28-MAY-91	
ENGR.	E.F. Nesman	21-OCT-91	
PROJ.	A.E.E. Rogers	21-OCT-91	
PROG.			

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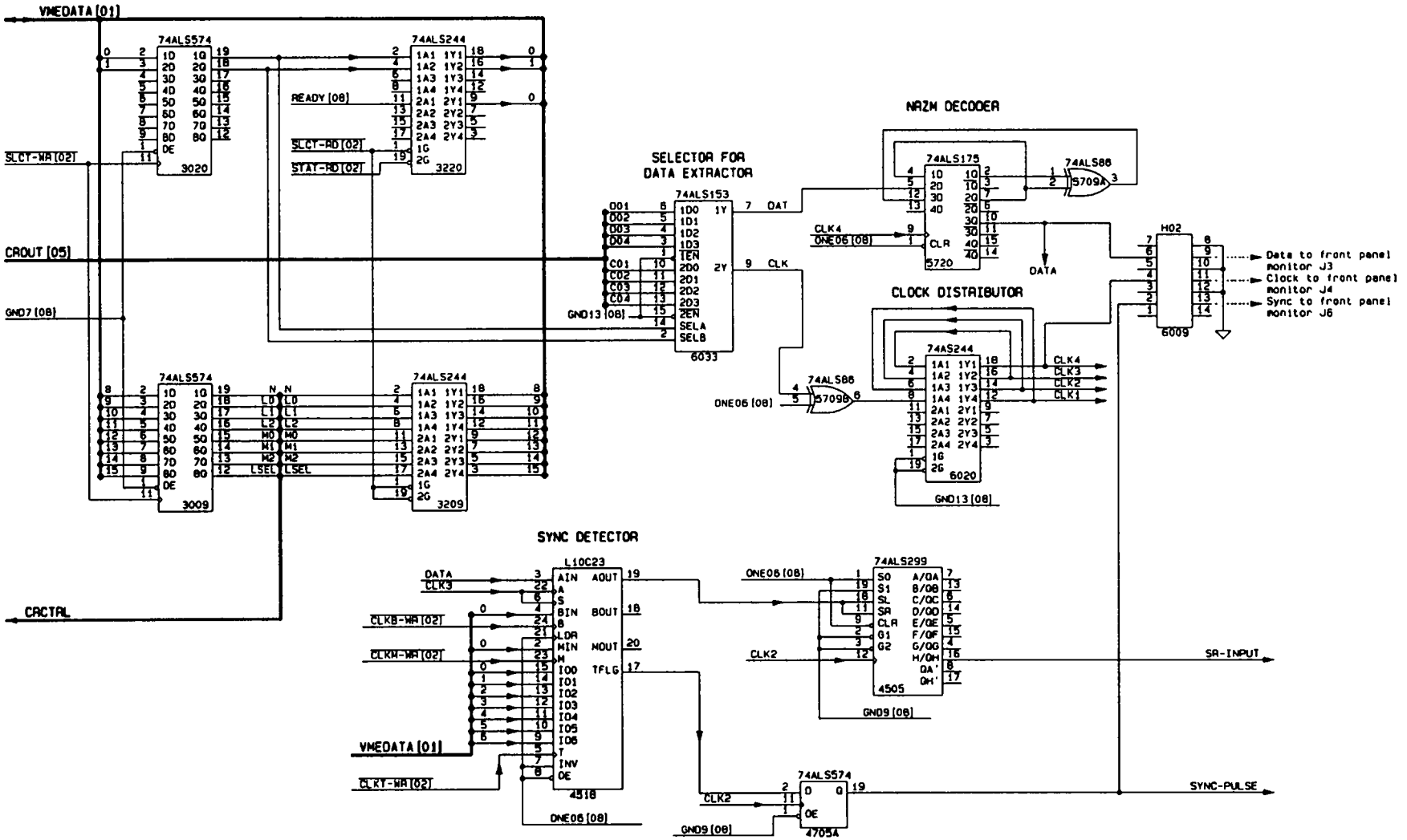
VLBA RECORDER - LOGIC DIAGRAM
VME CONTROLLER - MONITOR MODULE
RECEIVERS & CLK REC. SELECTORS

MODULE	SIZE	DWG NO	REV
MONITOR	C	C5432BL004	A

DATE 21-OCT-91 SHEET 04 OF 09

File: C328L006.DWG | Dwg: MONITOR MODULE - DATA SELECTOR & SYNC DETECTOR

REV: A ENGR. E.F.Nesman 22-MAY-92



MAY 27 1992

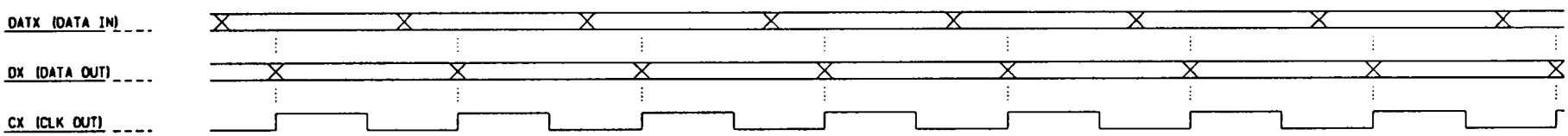
NERDC - HAYSTACK OBSERVATORY WESTFORD, MA 01886		
VLBA RECORDER - LOGIC DIAGRAM VME CONTROLLER - MONITOR MODULE DATA SELECTOR AND SYNC DETECTOR		
MODULE: MONITOR	SIZE: C	DWG NO: C54328L006 REV: A
DATE: 21-OCT-91		SHEET 06 OF 09

DR.	E.F. Nesman	16-OCT-90
CHK.	E.F. Nesman	28-MAY-91
A ENGR.	E.F. Nesman	21-OCT-91
B PROJ.	A.E.E. Rogers	21-OCT-91
C PROD.		

File: C328V003.DWG | Dwg: MONITOR MODULE - CLOCK RECOVERY TIMING

REV: A ENGR. E.F.Nesman 22-MAY-92

CLOCK RECOVERY TIMING



TIMING RELATIONSHIPS:
1. DELAY OF DATA OUT WITH RESPECT TO DATA IN - UNSPECIFIED
2. DELAY OF CLK OUT WITH RESPECT TO DATA OUT - 0 TO 3 NS

MAY 27 1992

DR	N.T. Petrachenko	21-JAN-87
CHK	A.E.E. Rogers	05-JAN-89
ENGR	V.A. Tran	01-MAY-89
PROJ	A.E.E. Rogers	10-MAY-89
PROD		

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VLBA RECORDER - TIMING DIAGRAM
VME CONTROLLER - MONITOR MODULE
CLOCK RECOVERY TIMING

MODULE:	SIZE	DWG NO.	REV
MONITOR	C	C54328V003	A

DATE 21-OCT-91 SHEET 03 OF 04