VLBA Data Acquisition Memorandum No. 401

Formatter Upgrade 512 Mbps

Version 7

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August 2, 2001

Formatter Modification Introduction

This procedure outlines the steps required to implement the VLBA formatter Modification. This modification upgrades the VLBA recorders from an aggregate record data rate of 256-Mbps to 512-Mbps. This requires both recorders to simultaneously record data at 8-Mbps per track. This allows the VLBA antenna to operate at a higher sample rate and increased resolution.

Basic Procedure

Basically this upgrade involves replacing the formatter firmware, adding three additional VME cards to the formatter, and adding new sampler cables so the back plane can support the additional boards. This procedure takes about 4 hours to complete and 2 hours of remote testing. The SOC Recorder lab will perform the testing remotely.

Successful completion of the modification will provide a recorder system that can use either a single recorder or both recorders simultaneously.

Step-by-step Procedure

1. Turn off the power. Verify that there are eight 40-pin cables located near the front of the formatter. Four of these should be connected to the D134 Transport Driver module of board set #1. The D134 Transport Driver module of board set #2 will use the other four cables. The other end of these cables is connected to the I/O Panel on the back of the D-Rack. If these cables are not installed call the Recorder Lab at 505-835-7103.

2. Verify that there are eight 40-pin ribbon cables between the I/O panel and the bulkhead. Verify there are four cables between the bulkhead and each recorder. Verify the odd and even cables and pin #1 are located correctly. See figure 1.

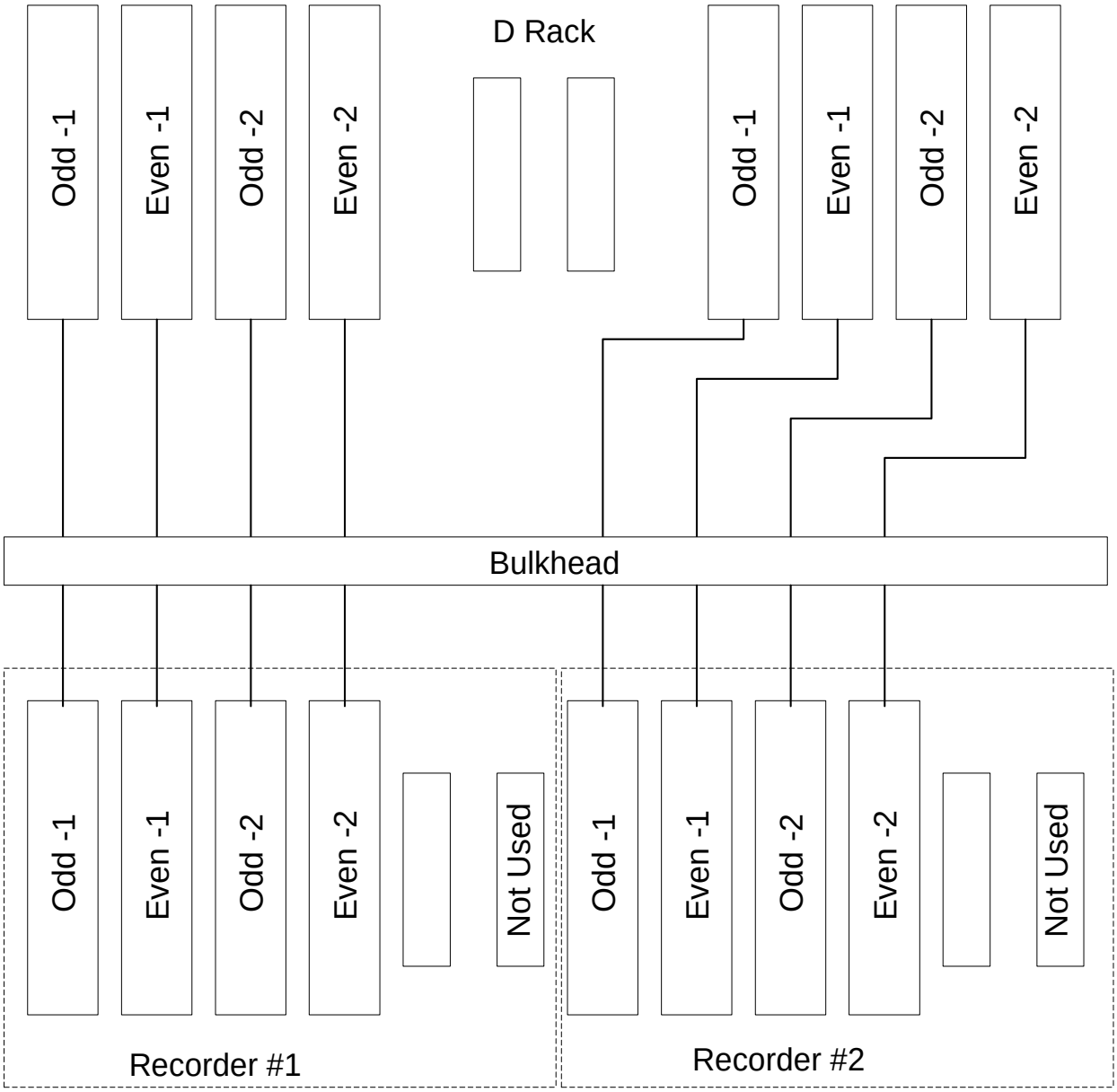


Figure 1. D Rack Cable Locations

3. Remove the cables from the back of the Sampler Module. A cover plate may be installed over the VLBA formatter back plane, which will need to be removed to obtain access. One cable is connected to the Sampler Module labeled #1 and the VLBA Formatter P3 backplane P-309. The other cable is connected to the Sampler Module labeled #2 and VLBA Formatter P3 backplane P-311.

4. Install the provided cable labeled SA1. Connect this cable to the lower P3 backplane connectors. Connect the end with the circuit card terminator to the P3 backplane connector P-309. Connect the center connector to the P3 backplane P-315. Connect the last connector to the back of the Sampler Module labeled SA1.

5. Install the provided cable labeled SA2. Connect the end with the circuit card terminator to the P3 backplane P-311. Connect the center connector to the P3 backplane P-317. Connect the last connector to the back of the Sampler Module labeled SA2.

6. Remove the terminators from D138 Digital Switch module of Board set #1. See figure 2 for the locations of the 9 Zip terminators that need to be removed, locations 7101, 7701, 7901, 8501, 7112, 7712, 7912, 8512, and 7923. D138 Digital Switch module of Board set #2 was shipped with the terminators removed.

7. Verify the addresses on Board sets #1 and #2, Table 1. These addresses are read from front to back with the VME bus connectors on the back of the board.

Table 1, VME Board Addresses

	BOARD SET #1	BOARD SET #2
D138 Digital Switch Module	180 21	680 31
D134 Transport Driver Module	380	880
D133 Header Control Module	280	780

Remove the terminators on both Digital Switch Boards

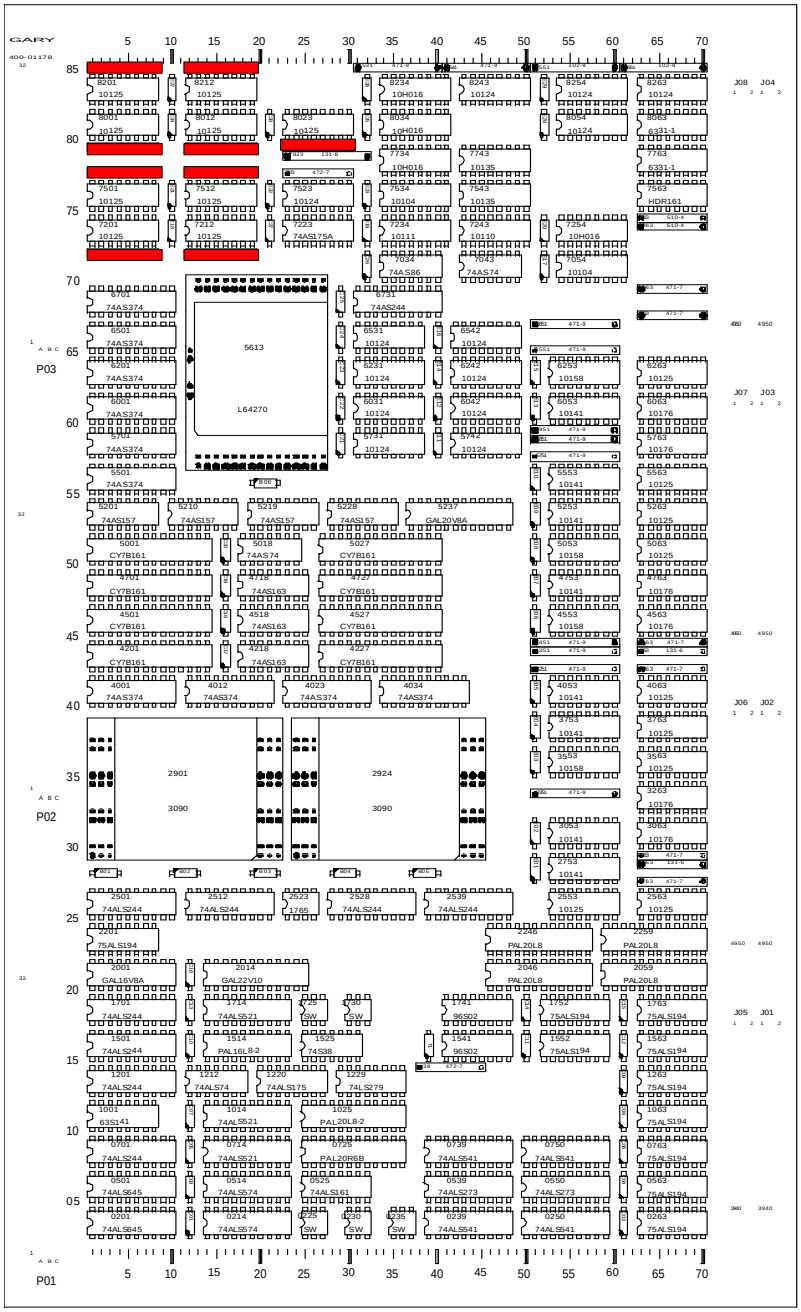


Figure 2. . D138 Digital Switch Module Terminator Locations

8. Install the Board set #2, Digital Switch, Header Control and the Transport Driver into the VME rack in the same order as Board Set #1.

9. Install the included short 40 Ribbon cables between the Digital Switch and the Header Control module, J1 and J2.

10. Install four 40-pin Ribbon cables to Transport Drive #2 board in the same order as the cables on the TD #1 board.

11. Install the provided firmware EPROMS (2) V3.08 on the MVME 117-4 board. Remove the EPROMS from Sockets U39 and U48 and install 9CCE into U37 and 9005 into U48.

12. Install cables from the Recorder I/O panel Odd-2 and Even-2 to the VME Write Module. See Figure 3. Verify that the connectors are placed over both rows of pins.

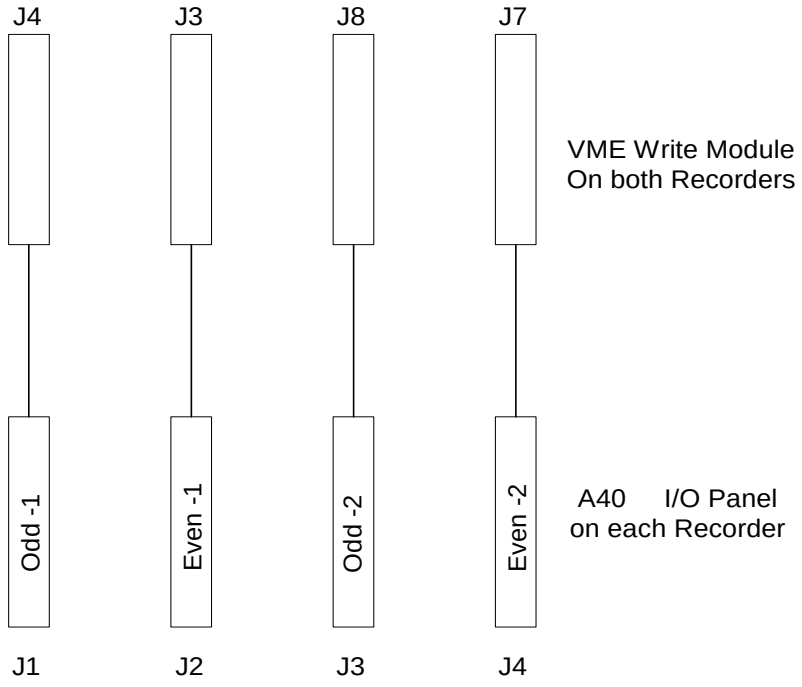


Figure 3. Recorder Cable Locations

13. Turn on the power supplies. Use the software package SCREEN to test the operation of each board set.

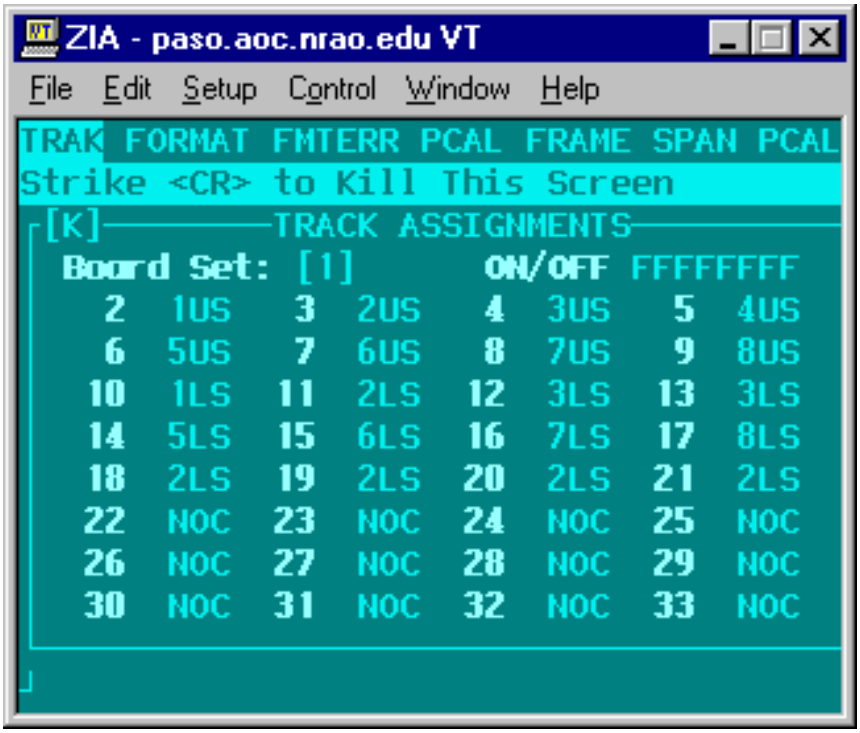
14. These tests use the RSCREEN program to test the various circuits of the formatter and recorder interface. Configure the Formatter to VLBA 1:1, SRATE = 8M, ORATE = 9.072. Using RSCREEN, MCB, MONREQ, query the locations for a read back.

Location	Board Name	Response	Comment
#2341`	DS-1	#01F0 #00B0	Pcalx Command – ON Pcalx Command - OFF
#234C	DS-2	#00A4 #00E4	Pcalx Command – ON Pcalx Command - OFF
#2342	HC-1	#0190 #0390	Aux Data Ram A Aux Data Ram B
#234D	HC-2	#0190 #0390	Aux Data Ram A Aux Data Ram B
#2344	TD-1	#3038	12344
#235C	TD-2	#3030	12336

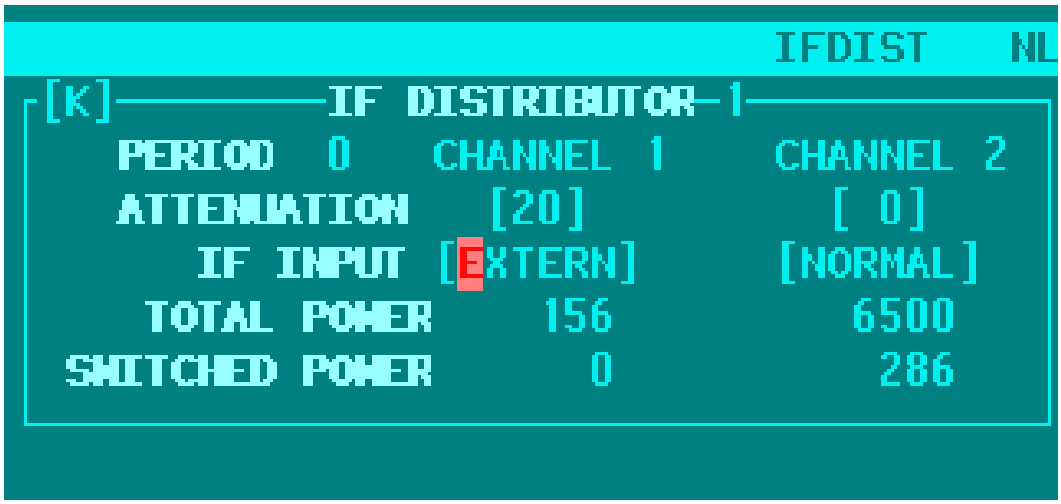
Note: Sending 8001 to address #2381 will re-initialize the formatter without a 117 reset.

15. Connect a BNC cable between BBC-1 LO Monitor output and IF Distributor-A Alternate Input #1, (the most-left-hand BNC). This will allow the BBC-1 to be used as a signal generator.

16. Use the RSCREEN PCAL command to check board set #1 and set #2. Set the RSCREEN, TRACK ASSIGNMENTS as follows. This setup is for board set #1. Enter a similar setup for board set #2. Note that the set-up is not complete and the user must complete 22-33 for both board sets.



17. Set the IF distributor as follows.



18. Setup the BBC 1 as a signal generator. Setup BBC 2-8 for LSB detection.

19. Set up the FORMAT SCREEN for MARK III.

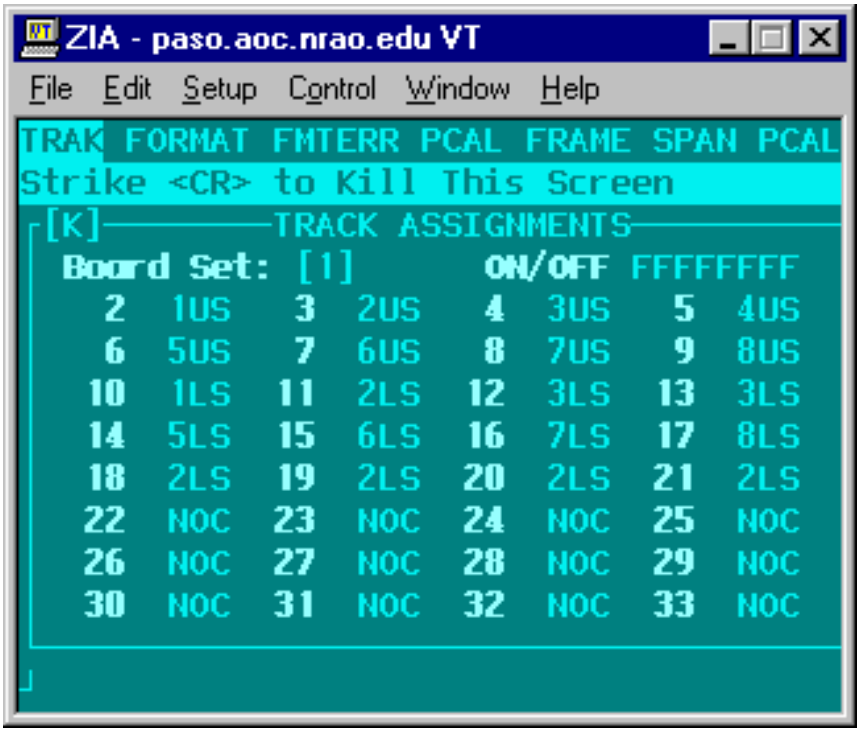
20. Enable the heads to write EN 1111, select BYPASS. Select Board set #1.

21. Run PCAL check for LSB operation (note 1LS will not operate because it is being used as a signal generator.

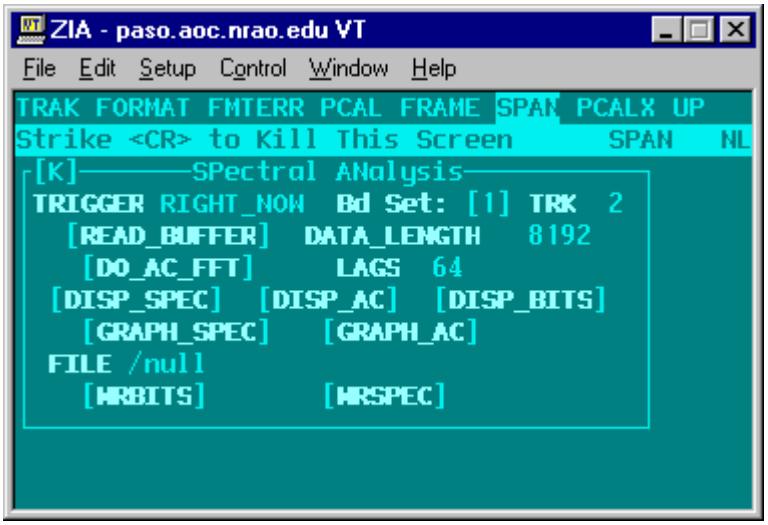
22. Using RSCREEN, PCALX, to test Board Set #1 and compare the results to set 20. Push the Phase button to view the Lower Side Bands.

Barrel Roll Test

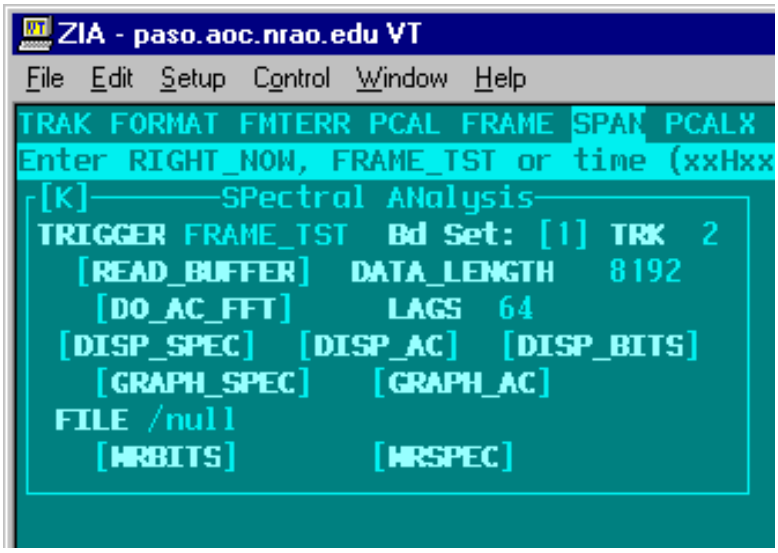
To test the barrel roll function set the FORMAT screen Barrel Roll to 16 (roll all 16 evens and all 16 odds). Set all of the TRAKs to either Upper Side band or Lower Side band see figure below. (note figure is incomplete).



Use the FORMAT – SPAN screen to check he barrel roll output. The TRIGGER RIGHT_NOW function will trigger a capture of the track but disables the barrel roll.



The second method uses the argument "FRAME_TST". This method also captures the data immediately but will not disable barrel roll, read extra tracks or demultiplex the bits in VLBA for 1:2 or 1:4 modes. This method is good for inspecting the formatter frames directly. Type FRAME_TST in the TRIGGER function.



Use the following steps to view the bits; TRIGGER, READ_BUFFER, DISP_BITS. The bits are described in detail in VLBA Acquisistion Memo #151.1 and Mark IV Memo #267. The last 8 bytes of the frame are labels. Note that the barrel roll will roll the tracks acording to the TRAK srceen. If track 2 is selected, as show in the figure, the SPAN output will look as follows:

0488 0800	bit reversed =	0	=BBC 1	(the second “8” means upper)
0488 4800		2	=BBC 3	(sideband is selected)

Testing the Digital Switch Board

There are four test to QA a Digital Switch board.

1) Configuration and FIFO load test

2) One Pulse-per-Second tests

3) Cross Point Switch using “TSTXPT”

4) PCAL counters using PCAL Software Suite.

Configuration and FIFO Load test

Using the SCREEN package to configure the Formatter to the Sample and Output Rates listed in the following tables. The clock frequency signal on the schematics (page 4) =ZLFIFO (4).

Configuration	Sample Rate	Output Rate	ZLFIFO (4)	QA Check
VLBA 1:1	250 K	. 284 K	250 K	
	500 K	.567 K	500 K	
	1 M	1.134 M	1.0 M	
	2 M	2.268 M	2.0 M	
	4 M	4.536 M	4.0 M	
	8 M	9.072 M	8.0 M	
VLBA 1:2	500 K	. 284 K	250 K	
	1 M	.567 K	500 K	
	2 M	1.134 M	1.0 M	
	4 M	2.268 M	2.0 M	
	8 M	4.536 M	4.0 M	
	16 M	9.072 M	8.0 M	
VLBA 1:4	1 M	. 284 K	250 K	
	2 M	.567 K	500 K	
	4 M	1.134 M	1.0 M	
	8 M	2.268 M	2.0 M	
	16 M	4.536 M	4.0 M	
	32 M	9.072 M	8.0 M	

VLBA 2:1	250 K	.567 K	500 K	
	500 K	1.134 M	1.0 M	
	1 M	2.268 M	2.0 M	
	2 M	4.536 M	4.0 M	
	4 M	9.072 M	8.0 M	
VLBA 4:1	250 K	1.134 M	1.0 M	
	500 K	2.268 M	2.0 M	
	1 M	4.536 M	4.0 M	
	2 M	9.072 M	8.0 M	
MARK III	1 M	1.125 M	1.0 M	
	2 M	2.25 M	2.0 M	
	4 M	4.5 M	4.0 M	
	8 M	9.0 M	8.0 M	

One Pulse-per-Second tests

1. Monitor for a 120ns (+/- 10 %) wide One-Pulse-per-Second at

   J01 Pin 35 –Pin 36 _____ (1263 pins 2-3)

   J02 Pin 35 –Pin 36 _____ (1263 pins 10-11)

2. Installed and configured the Digital switchboard as board set #1.

   Monitor for an 80 microsecond wide (+/- 10%) One-Pulse-per-Second at

   P02 Pin A04 –Pin C04 _____ (2201 pins 2-3)

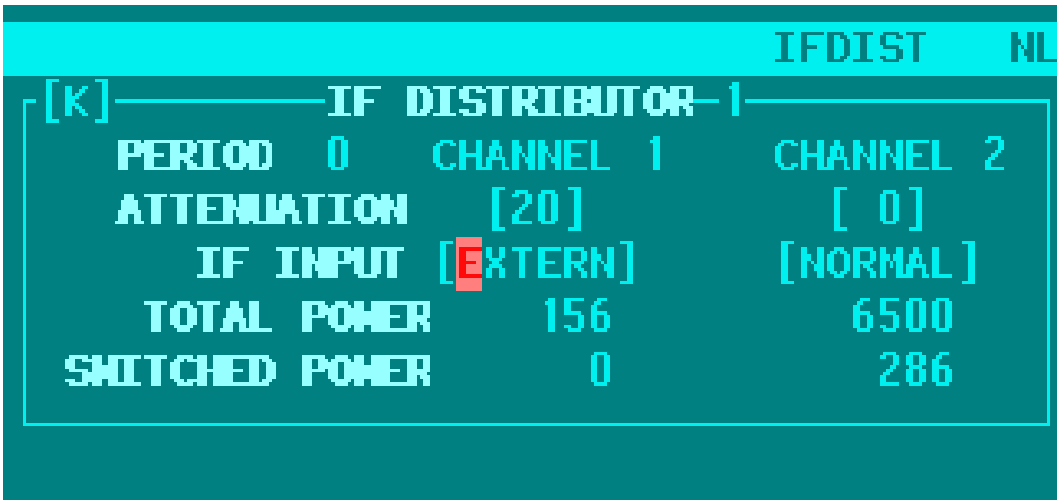
3. Installed and configured the Digital switchboard as board set #2.

   Verify the 80 microsecond One-Pulse-per-Second is inhibited.

   P02 Pin A04 –Pin C04 _____ (2201 pins 2-3)

Testing the Digital Switch -Cross Point Switch using "TSTXPT"

1. Set the IF distributor as show below.



2. Set BBC-5 to 750M and IF input B. Use it as a Signal Generator by connecting a BNC cable between BBC-5 LO Monitor output and IF Distributor-A Alternate Input #1, (the most-left-hand BNC). This will allow BBC1 to be used as a signal generator.

3. Set BBC-1 through BBC-4 to 750.05, 750.10, 750.15 and 750.2 respectively with Bandwidth of 250 kHz lower and upper and Gain = AUTO.

   Run TSTXPT

Track Number	=	0
Period	=	1 Second
Lowest BBC	=	1
Highest BBC	=	4
Sideband	=	L (lower)
Board Set	=	1

4. Connect Oscilloscope to the front panel connectors J-1 and J-2. See schematics for pin locations. Remember that the signals are differential. Verify the signal represents the magnitude and phase of each frequency, 50 kHz 100 kHz, 150 kHz, 200 kHz. Repeat for each Track 0-34.

Testing the Digital Switch - PCAL Counters using PCAL Software Suite

1. Set the IF-1 distributor Channel 1 to attenuation = 20 dB and Input = EXTERN.

2. Set BBC-5 to 750M and IF input B. Use it as a Signal Generator by connecting a BNC cable between BBC-5 LO Monitor output and IF Distributor-A Alternate Input #1, (the most-left-hand BNC). This will allow BBC-5 to be used as a signal generator.

3. Set BBC-1 through BBC-4 to Frequency = 750.10M, Bandwidth of 62.5 kHz lower and upper, Gain = AUTO.

4. Run PCALSET and use option 4. (Specify in units of 10 kHz i.e. 10kHz = 1)

5. Run PCALCHAN and use option 0. BBC-1, lower side band, sign bit. 1-second integration time.

6. Run PCALRUN to configure the formatter and start the counters.

7. Run RDCTR to read and display the output of the counters. Verify that the counter outputs Magnitude and Phase are the same for all eight extractors.

8. Repeat steps 5-8 for, BBC-2 L, BBC-3 L, and BBC-4 L.

9. Run PCALSTOP to stop the counters.

10. Set BBC-5 to 750.02M. Use it as a Signal Generator by connecting a BNC cable between BBC-5 LO Monitor output and IF Distributor-A Alternate Input #1, (the most-left-hand BNC). This will allow this BBC to be used as a signal generator.

11. Repeat steps 5-8 for BBC-1 U, BBC-2 U, BBC-3 U, and BBC-4 U.

12. Use BBC –1 as a signal generator and use BBCs 5-8. (Switch the Sampler Cable if a full compliment of BBCs are not installed.) Repeat the entire process for both lower and upper side bands.

    Note: To force reload of Xilinx counters

    Stop the phase cal extractors from running, (PCALSTOP)
    Change the setup of the phase cal extractors by sending a new tone using PCALRUN.

    Send data “8100” to address #2386 using MCB command. This sets bit 8.

    Send data “8001 to address #2382 using the MCB command. This re-configures the

formatter. During the re-configure the Xilinx will reload.

Header Control Tests using the HC Software Suite

1. Run AUXTEST to fill 32 Bits A side.

2. Input recognizable patterns such as DEAD, BADA, 1234, 9876.

3. Run HCTEST, 8112, **A** side,
   Check to see if the clock is incrementing.
   Check Barrel Roll indicator
   Verify fill bits are correct.

4. Run AUXTEST to fill 32 Bits B side with a recognizable pattern.

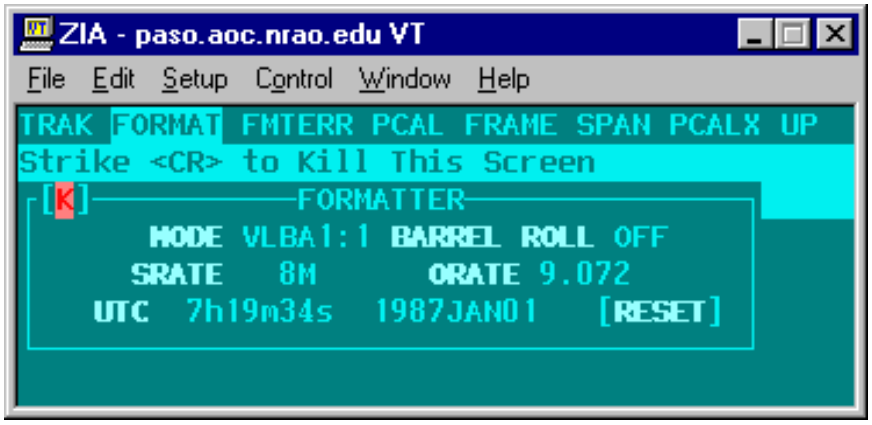
5. Run HCTEST, 8112, **B** side,
   Check to see if the clock is incrementing.
   Check Barrel Roll indicator
   Verify fill bits are correct

6. Run HCTEST 8110
   Fill 32 Bits with a recognizable pattern.
   Check to see if the clock is incrementing.
   Check Barrel Roll indicator
   Verify fill bits are correct

Transport Driver Board Test

1. Install Transport Driver board in VLB2, a functional Formatter. .

2. Configure the formatter to



3. Enable the heads, EN 1111, BYPASS, and speed 160

4. Turn on all of the tracks in the FORMAT Tracks screen
   Run ERRORS DELUX
   Verify that no errors are present on any track.
   Monitor the decode screen.
   Verify that the time, track, and head are correct for every track, 2-34.

5. Turn on the EVEN tracks in the FORMAT Tracks screen (555555555)
   Run ERRORS DELUX
   Verify that no errors are present on any EVEN track and the ODD tracks are OFF

6. Turn on the ODD tracks in the FORMAT Tracks screen (AAAAAAAA)
   Run ERRORS DELUX
   Verify that no errors are present on any ODD track and the EVEN tracks are OFF

7. Move the formatter output cables from the recorder #1 outputs to the recorder #2 outputs.
   Note move only the two 40-pin cables not the 20-pin cable. Repeat steps 4, 5, and 6.

8. Move the formatter cables back to the original position.