VLBA Electronics Memo No. 80

National Radio Astronomy Observatory

VLB Array Program

VLB Array Electronics Memo No. 130

VLBA Standard Interface Board Retrofit

Ron Weimer
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Ref: Tech Report No. 12 VLBA STANDARD INTERFACE MANUAL, & EDTN 159

Problem:

Some time ago I wrote Electronics Division Technical Note No. 159 describing a couple of problems with the Standard Interface Board (SIB). One problem described was analog address selection problems. This can be avoided by careful design of the interface controlling the SIB. The second problem described was one of the loading of analog monitor points by the Burr Brown INA 101 instrumentation op amp on the SIB. The loading occurred when the A/D was reading a positive voltage right after reading a negative voltage. During the slew from negative to positive, the input impedance of the INA 101 dropped from 10 gigaohms to around 1.6 K ohm. This low impedance could drain charge off of filter caps in monitor circuits. Depending on the source impedance of the monitor circuit, its voltage might not be recharged completely by the time the A/D converter sampled the voltage (around 200 µs).

Problem Fix:

Since most of the VLBA modules are already designed and in the field it did not seem practical to try to correct the SIB problem by redesigning the monitor circuits. We looked at a number of op amp suppliers and could not find a pin compatible replacement amp. Most new op amps do not come in the 10 pin metal can package that was used in the SIB. The Analog Device/PMI model AMP-02-EP looked like it would be electrically compatible.

Testing:

Some tests were run to determine if the AMP-02 would reduce the loading problem. The results are in Table 1. The tests were run using the weather station since it was easy to modify. Test 1 used the existing ±15 volt monitor points on the weather station. This gave a -7.5v reading followed by a +7.5v reading. The voltage divider gave a source impedance of 5K ohm. The voltage test points went through a MUX 08 and then to channel 1

of the SIB. Capacitors were added to the voltage dividers to simulate different monitor point time constants. A value of 0.01µf gave the same T(T = 50 microseconds) as the L104 test points that were first noticed with the loading problem. Test 2 was similar except that voltage dividers were connected directly to channels 3 and 4 of the SIB. This was done to see the effect of the MUX 08 in test 1. There was no significant difference in the results. Finally voltage dividers with a source impedance of 10 K ohms were connected to channel 3 and 4 and used in test 3. This simulated the L104 conditions even closer. A cap of 0.05 µf gave the T = 50 microseconds condition. Figures 1 through 6 show some scope traces taken during the above tests. A probe was connected across the cap and the traces show the discharge/charge voltages.

Test Results:

From the results shown in table 1 it is concluded that the AMP-02 is superior to the INA 101. Each code step of the A/D converter is 5 mv. The voltage offsets for the AMP-02 were always 3 code steps or less. With the L104 conditions the offset was typically 0 or 1 code steps. This compares to 100 to 780 mv offsets with the INA 101 op amp in use.

Implementation:

Since the AMP-02 is not pin compatible it was decided to design a circuit board which would plug into the 10 pin socket on the SIB and hold an AMP-02 in another 8 pin DIP socket. W. Zamora and W. Koski came up with the design and parts to implement this. Circuit board drawing is number B55002Q003. Pins to plug into the SIB socket were Augat part No. 8128-94P3. SIBs will be outfitted with the new amps. test and adjusted, and then sent in blocks to VLBA stations for retrofit into the system. Returns from the stations will then be retrofit etc.

Voltage Reading On Readblock Screen					
	BB-INA 101 AMP		AD/PMI-AMP-02		
	Voltage	Difference	Voltage	Difference	Conditions
	Volts	Millivolts	Volts	Millivolts	
Test 1	7.529	ref	7.529	ref	5K-no cap
	7.465	64	7.529	0	5K-.01 cap
	7.099	430	7.514	15	5K-.047 cap
Test 2	7.524	ref	7.524	ref	5K-no cap
	7.519	5	no read	no read	5K-.005 cap
	7.451	73	7.519	5	5K-.01 cap
	7.016	508	7.514	10	5K-.047 cap
Test 3	7.504	ref	7.509	ref	10K-no cap
	7.397	107	7.504	5	10K-.005 cap
	6.962	542	7.500	9	10K-.01 cap
	6.723	781	7.500	9	10K-.047 cap

Table 1

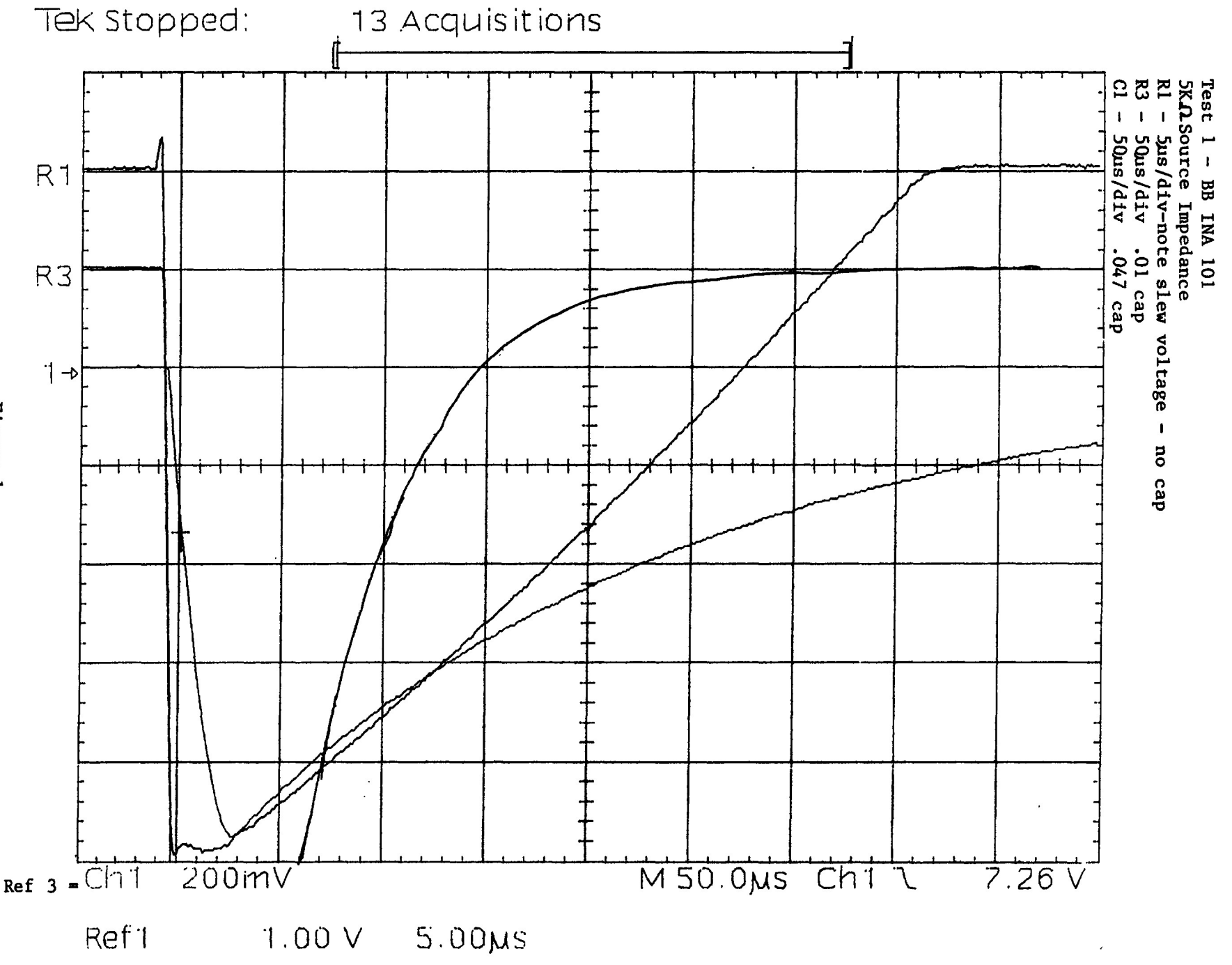

Tek Stopped: 13 Acquisitions
R1
R3
1→
Ch1 200mV
M 50.0µs Ch1 ⌊ 7.26 V
Ref 3 =
Ref1 1.00 V 5.00µs
Test 1 - BB INA 101
5KΩSource Impedance
R1 - 5µs/div-note slew voltage - no cap
R3 - 50µs/div .01 cap
C1 - 50µs/div .047 cap

Figure 1

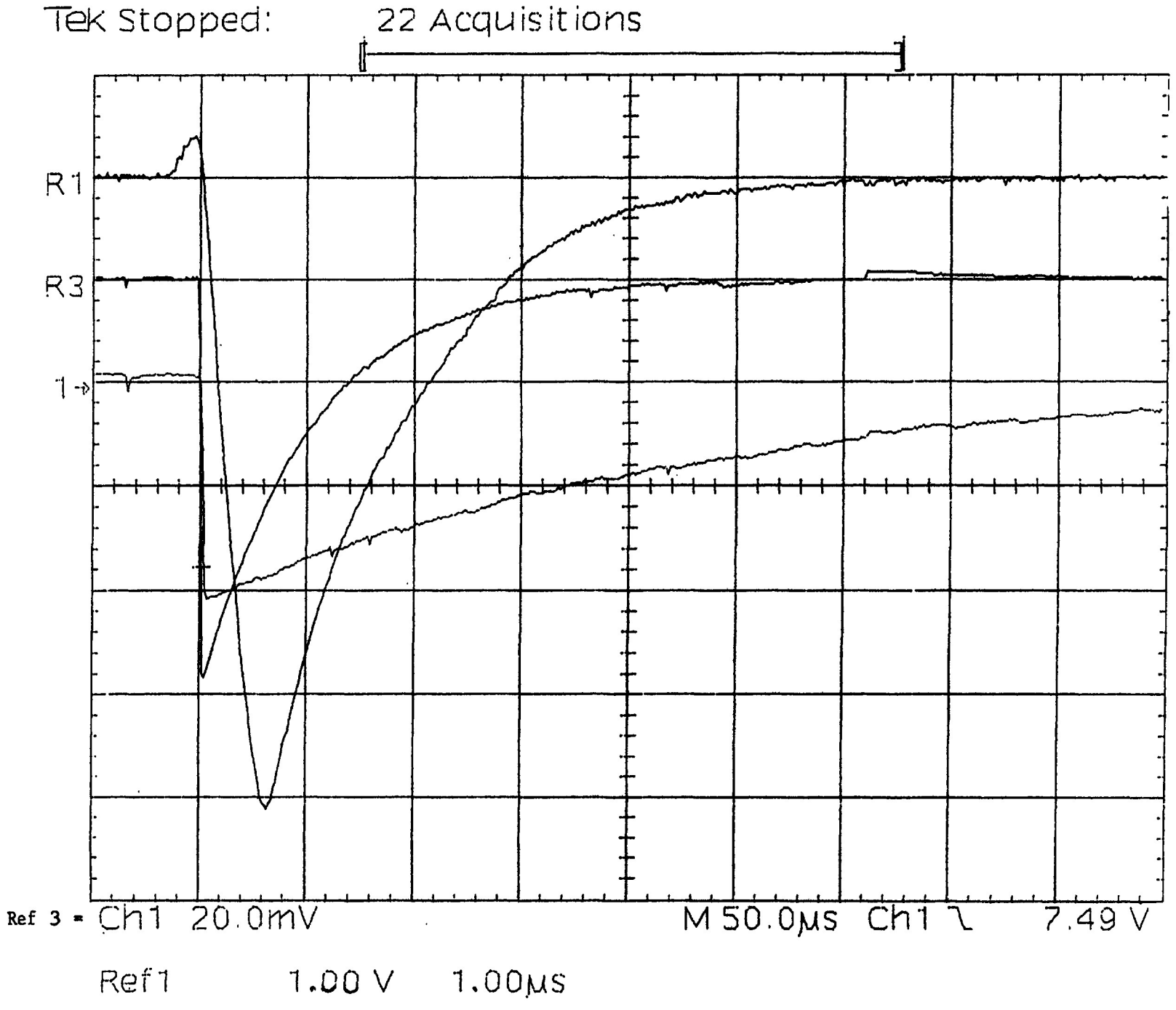

Tek Stopped: 22 Acquisitions
R1
R3
1→
Ref 3 = Ch1 20.0mV
M 50.0µs Ch1 ⌉ 7.49 V
Ref1 1.00 V 1.00µs
Test 1 AD/PMI AMP-02
5KΩ Source Impedance
R1 1µs/div
R3 50µs/div .01 cap
C1 50µs/div .047 cap

Figure 2

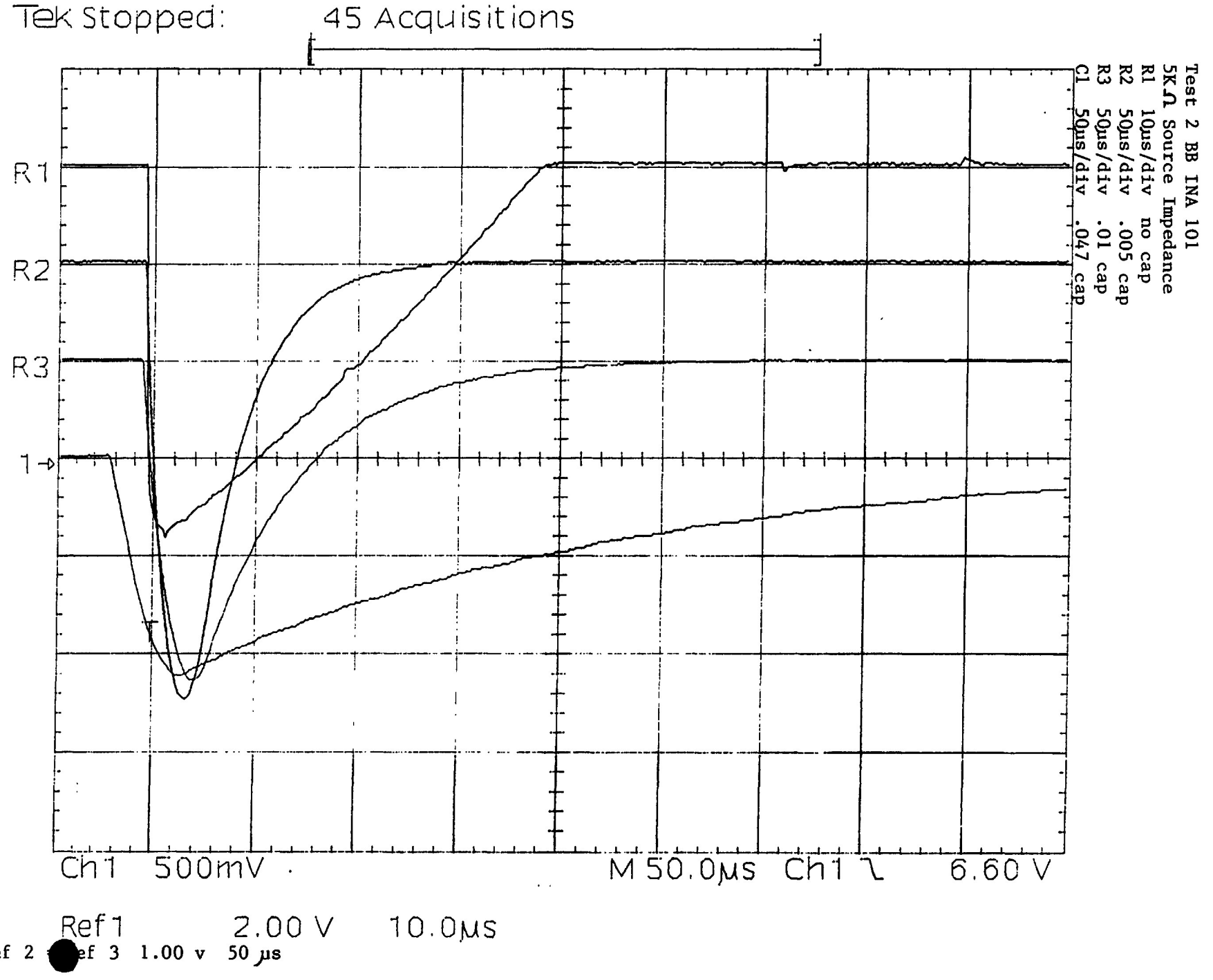
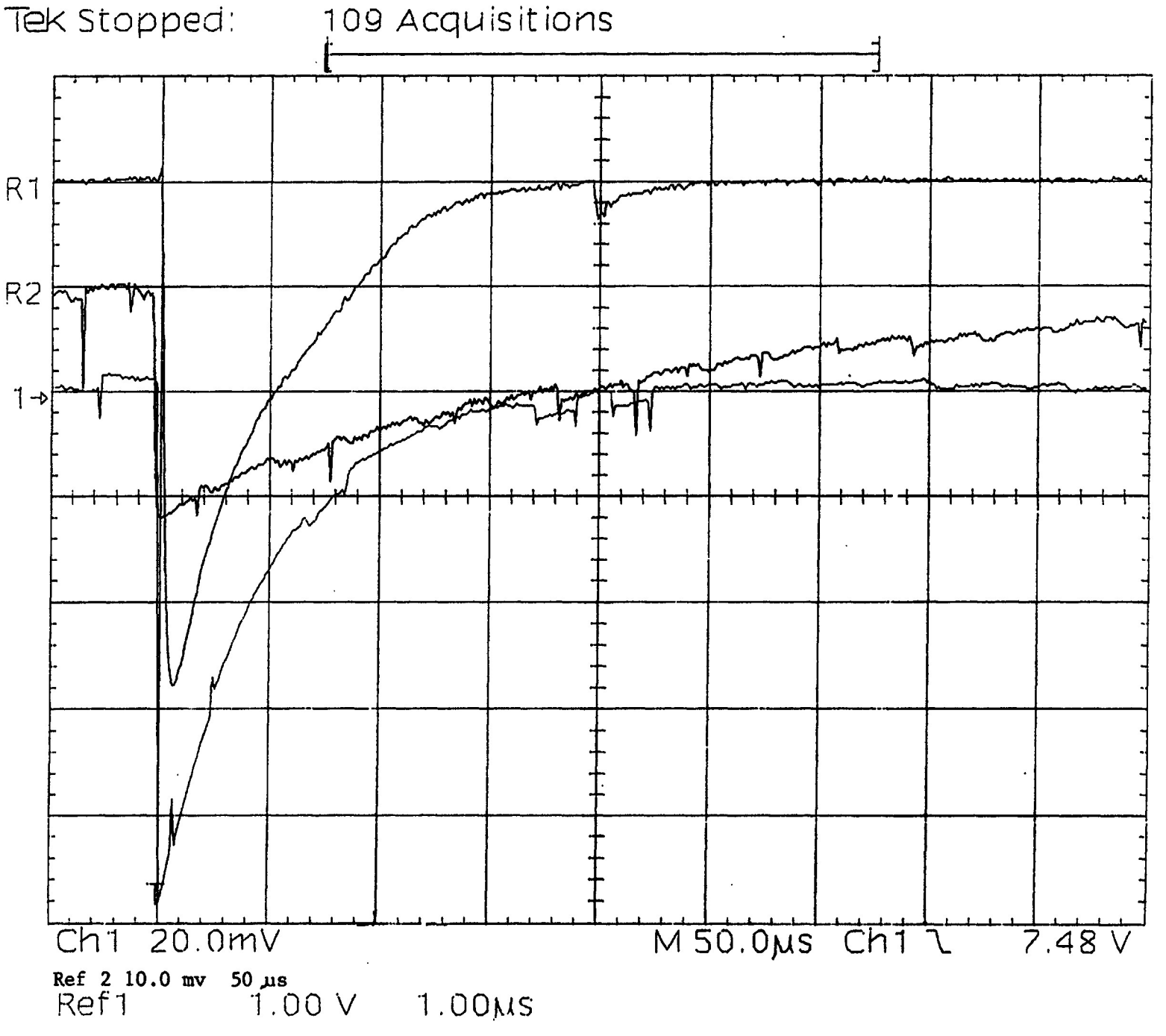
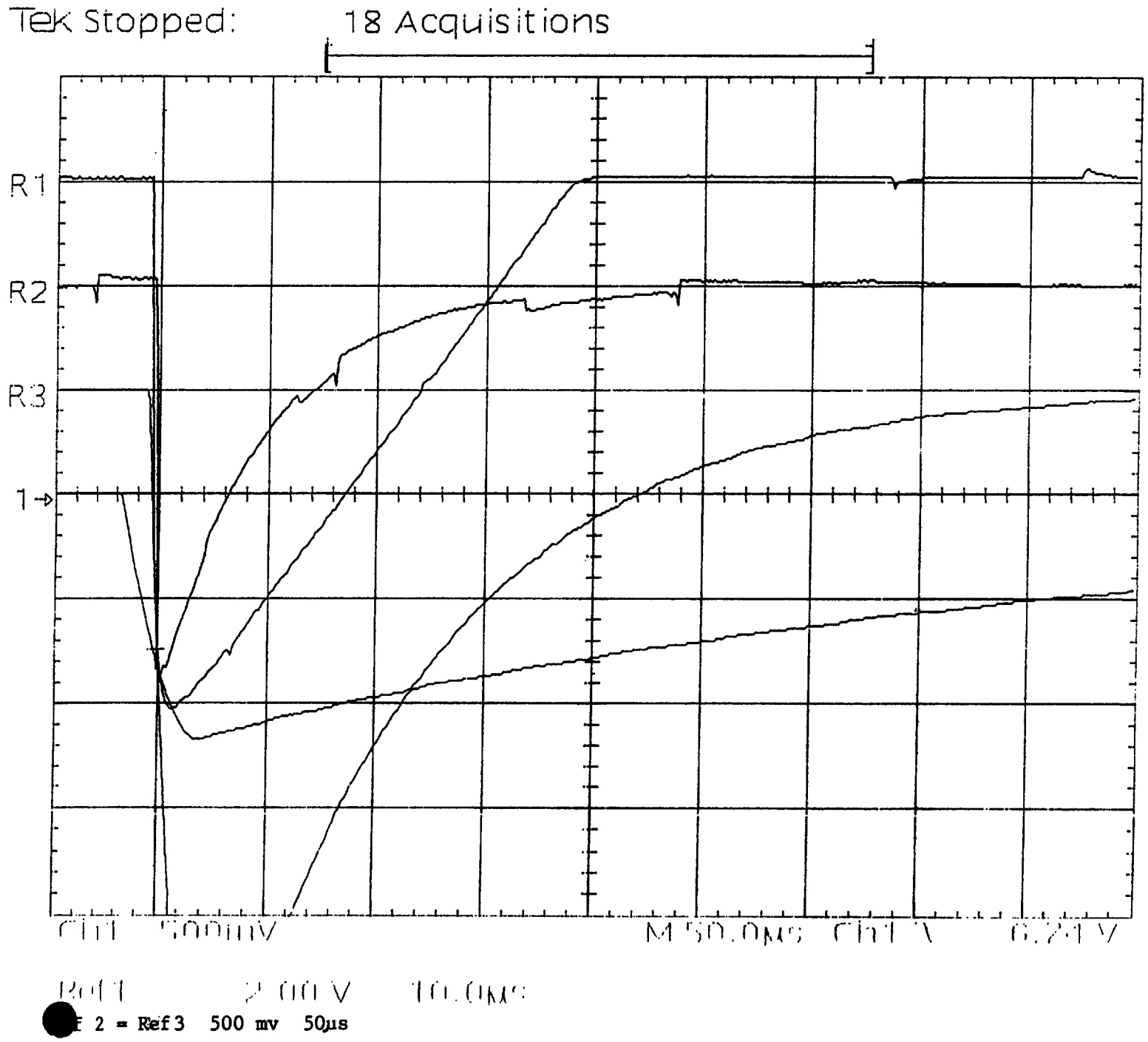

Tek Stopped: 45 Acquisitions
Test 2 BB INA 101
5KΩ Source Impedance
R1 10µs/div no cap
R2 50µs/div .005 cap
R3 50µs/div .01 cap
C1 50µs/div .047 cap
R1
R2
R3
1
Ch1 500mV
M 50.0µs Ch1 ∖ 6.60 V
Ref1 2.00 V 10.0µs
Ref 2 Ref 3 1.00 v 50 µs

Figure 3



Test 2 AD/PMI AMP-02
5KΩ Source Impedance
R1 - 1µs/div no cap
C1 50µs/div .01 cap
R2 50µs/div .047 cap

Figure 4



Test 3 - BB INA 101
10KΩ Source Impedance
R1 10µs/div no cap
R2 50µs/div .005 cap
R3 50µs/div .01 cap
C1 50µs/div .047 cap

Figure 5

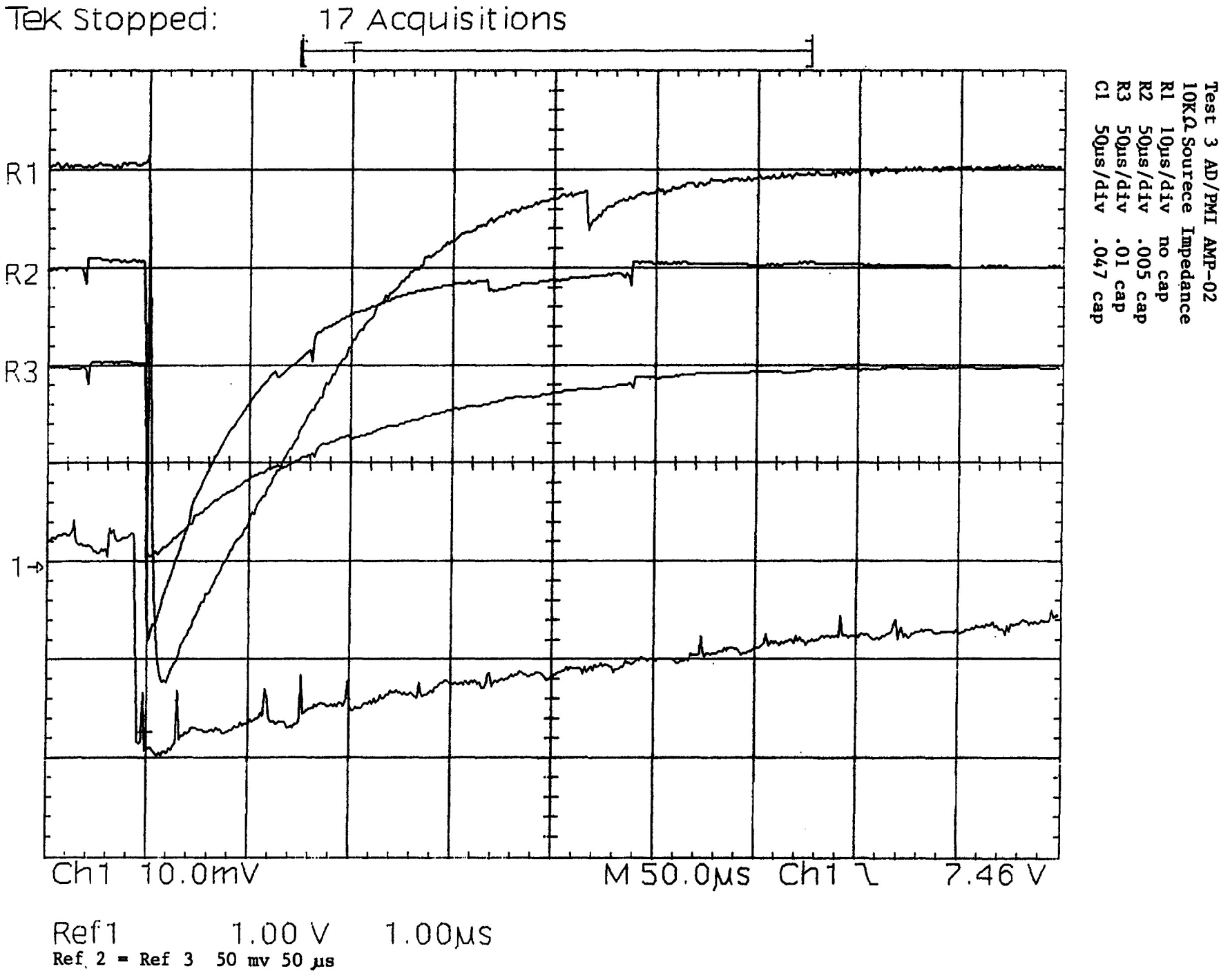

Tek Stopped: 17 Acquisitions
R1
R2
R3
1→
Ch1 10.0mV
M 50.0µs Ch1 ↘ 7.46 V
Ref1 1.00 V 1.00µs
Ref 2 = Ref 3 50 mv 50 µs
Test 3 AD/PMI AMP-02
10KΩ Source Impedance
R1 10µs/div no cap
R2 50µs/div .005 cap
R3 50µs/div .01 cap
C1 50µs/div .047 cap

Figure 6