VLB ARRAY MEMO No. 552

VLBA Electronics Memo No. 70

Station Timing System (860605)

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A block diagram of the station timing system is shown in Figure 1. This scheme is based largely upon VLBA memorandum #510, with some modifications resulting from the design review meeting earlier this month. The system in Figure 1 will comprise the Station Timing Module (L108), which will be located in the Master LO Rack. Two waveforms are used for the basic timing, a 5 MHz sine wave from the maser, and a series of pulses at 1 sec. intervals generated in the timing module.

The 5 MHz input goes first to a distribution system of buffer amplifiers which provides at least five outputs on rear-panel connectors. Four of the outputs are required by the baseband and recording systems. The 1 Hz pulses are generated by a synchronous counter which is triggered by the positive-going 5 MHz edges. The pulses are positive-going with 1 microsecond duration. The counter can be reset to synchronize the output with an external 1 pps timing signal, for which either positive- or negative-going pulses are acceptable. The reset occurs when a front-panel push button is activated. (To prevent accidental reset, the external timing signal should be connected to the front-panel input connector only when resetting is required. Alternatively, a more complex scheme, such as one requiring simultaneous commands from the push button and the central control computer, can be incorporated). At least eight 1 Hz outputs, buffered by 50 ohm, TTL-level drivers will be provided. Four of the signals are required for the baseband and recording systems.

As suggested in VLBA memorandum #504, a frequency of 80 Hz will be used for noise-source switching. In the baseband system, which is one place where this signal is required, it will be derived from the 5 MHz and 1 Hz signals. It is also derived in the same manner in the timing system in Figure 1, and transmitted by cable to the vertex room. The output of the circuit that divides by 62500 is reset on the first positive transition of the 5 MHz waveform following the positive-going edge of the 1 Hz signal. Four rear-panel outputs will be provided at 80 Hz, two from 50-ohm TTL-level drivers and two from RS485 drivers.

The buffer amplifiers for distribution of the 5 MHz should use the same high-stability circuit as is used in the L121 module (5 MHz Distributor) in the baseband converter rack. As an alternative to mounting all of the units in Figure 1 in a single module, the 5 MHz buffer can be omitted from the Station Timing Module and an extra L121 located in the Master LO Rack. In either case, both the timing circuitry and the buffer circuitry must run on power supplies connected to the uninterruptible power system.

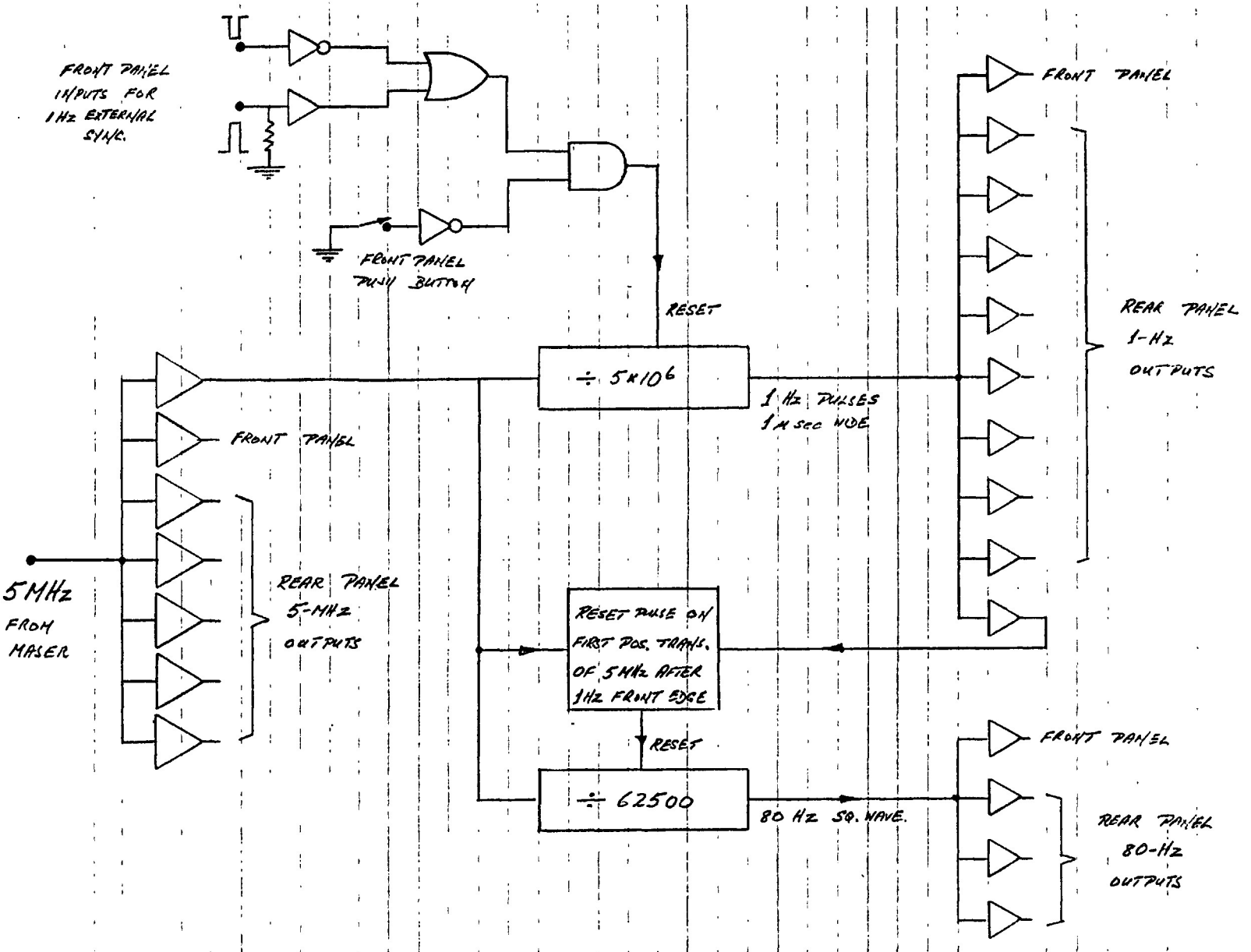

Fig. 1. Station Timing System.

A.R.T. 5/29/86