VLBA Electronics Memo No. 74

(860714)

BREADBOARD 100 MHZ PHASE-SHIFTER FOR INTERFEROMETER LOBE-ROTATION

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I. Introduction

This report documents the design, operation, and testing of a breadboard, station-based lobe rotator, considered for use in the Very-Long-Baseline-Array (VLBA).

The station-based lobe rotator is a device which inserts a controlled frequency shift into a 100 MHz frequency standard. This allows the referencing of the station clock to a common point, such as the Earth's center. Thus, the receiver information can be lobe rotated before being digitized and recorded.

II. Overview

Refer to Figure 1, the VLBA Lobe Rotator. The system includes the lobe rotator, and the means of testing it.

The lobe rotation is accomplished using a Number Controlled Oscillator (NCO). The NCO is on a single integrated circuit. The NCO adds a programmable phase increment to a phase accumulator. By varying the phase increment, the resulting output frequency can be varied in one milli-Hz steps.

Initially, the 100 MHz is split into three signals. The top 100 MHz signal on the diagram is divided by 20, to give a 5 MHz clock to the NCO. Alternatively, the 5 MHz could come directly from the maser.

The NCO outputs an eight bit sine wave. A D/A converter (DAC) provides an analog output. 78125 Hz was chosen as the center frequency for the NCO. The fringe frequency is added to this.

The DAC output is added to the 100 MHz via a phase locked loop (PLL). This outputs a signal at 100.078125 MHz plus the fringe frequency.

The 78125 Hz reference is generated by dividing the 5 MHz by 64. This 78125 Hz is mixed with the third 100 MHz signal. The 100 MHz plus or minus 78125 Hz is phase detected against the PLL output. When the NCO has been set to 78125 Hz, the test 100 MHz phase detector should output a DC component proportional to the phase difference.

III. Detailed Design

This section describes in detail the modules of the system.

The system is constructed using a single NRAO E13800MI wire-wrap board. The 100 MHz components are interconnected by OSM connectors.

Figure 2 shows the power levels. The Voltage Controlled Crystal Oscillator (VCXO) requires an attenuator followed by a buffer amplifier, since it has a high output impedance.

Figure 3 shows the vendor part numbers, at the block diagram level.

Figure 4 shows the clock driver for the ECL divider logic. The 100 MHz is initially amplified by the RCA differential amplifier. 4C refers to the location on the wire-wrap board. The emitter follower provides the necessary current. Three strip lines distribute the clock to the three rows of logic. Each row is terminated with the equivalent of 50 Ohms. The NRAO Wire-wrap Board E13800MI contains the layout for the clock driver.

Figure 5 shows the ECL divider circuitry. Synchronous counters are used to minimize phase instability. The flip-flops between stages resolve a race condition in the timing. The 5 MHz output is converted to TTL levels by the 10125. The 78125 Hz output goes through the voltage divider to provide a -7 dBm, 50 Ohm output. The 50 Ohms is based on a 7 Ohm ECL output impedance. The signal is AC coupled to the mixer.

Figure 6 shows the NCO and DAC. The NCO is a Stanford Telecommunications ST-1172A, 40 pin chip. Figure 7 shows the NCO's block diagram. The 32 bit, phase increment is read in as four, eight bit numbers. The address is set in by a two position Dual In-line Package (DIP) switch on the board. The eight bit quarters of the phase increment are set in by an eight position DIP switch. The data set into the DIP switches is strobed into memory by pressing the push button on the board. The high to low transition activates the WRN line, which loads data into the eight bit register specified by the address line. Also, the button activates the Ldstb line. The low to high transition loads the 8 bit registers into the 32 bit, delta phase register. The carry in (CI) and reset lines are grounded. Select A being grounded causes a sine look-up table to be used for the output. Section IV, the operating instructions, provides details on the use of the NCO.

The eight bit sine wave goes to the National DAC0801LCJ DAC. This outputs an analog current. Two ma. maximum output is specified by the current into pin 14. The OP-15 op amp serves as a current to voltage converter. The two ma. through the 1.5K feedback resistor gives three volts peak output. An adjustable one ma. is added into the summing junction to center the sine wave at zero volts. The push-pull emitter followers provide the current to drive the mixer. The crossover distortion is minimized by the op amp feedback. The 47 Ohm output resistor provides the output impedance. The output voltage is divided by two when driving a 50 Ohm load. Seven dBm is delivered to the mixer.

Figure 8 shows the mixer amplifier, loop phase detector, and loop filter. The DAC output can be seen entering from the top of the diagram. Mixed in is the

amplified signal from the mixer. Referring to the block diagram, this signal is the difference between the VCXO 100.078125 MHz plus the fringe rate signal, and the 100 MHz. There is a low pass filter at the mixer to attenuate 100 MHz components. The signal enters the board via the green and black twisted pair. There is additional filtering at the op amp. The amplifier has a voltage gain of 55. The emitter follower provides the current to drive the phase detector. AC coupling filters out low frequency noise and keeps the emitter follower out of saturation or cut-off.

The TAK-5 mixer on the board acts as the loop phase detector. The output of the phase detector is low pass filtered to attenuate the 156 KHz components. The gain of the loop phase detector was measured to be:

$$K_D = 0.178 \text{ V/radian}$$

A loop bandwidth of BW = 30 Hz was chosen, to be similar to the maser. A damping factor of D = 0.5 was chosen to minimize phase noise.

The gain factor of the VCXO is K_o = 6280 rad/v-sec.

$$\text{omega}_n = 2 * PI * 30$$
$$= 188 \text{ rad/sec.}$$

$$t_1 = K_o K_D / \text{omega}_n^2$$
$$= 6280 * 0.178 / 188^2 \text{ sec.}$$
$$= 0.0315 \text{ sec.}$$

$$t_1 = R_1 C$$

Chose C = 2.2 micro-F

$$R_1 = 0.0315 / 2.2E\text{-}6 \text{ Ohms}$$
$$= 15 \text{ K-Ohms}$$

$$t_2 = 2D / \text{omega}_n$$
$$= 2 * 0.5 / 188 \text{ sec.}$$
$$= 5.32 \text{ msec.}$$

$$R_2 = t_2 / C$$
$$= 5.32E\text{-}3 / 2.2E\text{-}6 \text{ Ohms}$$
$$= 2.4 \text{ K-Ohms}$$

The OP-07 was chosen as the active element in the loop filter for its stability. An offset potentiometer is provided. The output goes to the VCXO.

A factor in choosing the 30 Hz loop bandwidth is the magnitude of the phase error introduced by the rotation of the earth. This is defined in equation 4.7 of "Phaselock Techniques", by Floyd Gardner. This defines the acceleration phase error as:

$$\text{domega/dt} / \text{omega}_n^2 \text{ radians.}$$

Omega corresponds to the fringe rate in radians/second. $Omega_n$ is the loop bandwidth.

The fringe rate, $v = D\ v_{rf}/c\ \cos\theta\ d\theta/dt$ Hz,

where: D = station separation of 6000 miles.
v_{rf} = the rf frequency of 100 MHz.
θ = the zenith angle
$d\theta/dt$ = the rotational rate of the earth.
c = the velocity of light.

Differentiating:

$$dv/dt = -D\ v_{rf}/c\ \sin\theta\ (d\theta/dt)*(d\theta/dt)\ \text{Hz/sec.}$$

The maximum values can be obtained by setting the sine or cosine equal to one. Substituting, the maximum, absolute values are:

$$v = 235\ \text{Hz}$$

$$dv/dt = 0.017\ \text{Hz/sec}$$

These are within the actual VCXO parameters of plus or minus three KHz maximum deviation and one KHz maximum modulation rate.

Substituting, the acceleration phase error equals:

$$0.017/\ (30^2 * 2PI) = 3.00E\text{-}6\ \text{radians.}$$

Converting the acceleration phase error to time:

$$3.00E\text{-}6\ \text{radians} * 10{,}000\ \text{ps} / 2PI\ \text{radians} = 0.0048\ \text{ps.}$$

This compares well to the 0.60 ps phase error allowed for the maser, which will be discussed in section V.A, Short Term Stability. Thus, the allowable acceleration phase error must be considered in defining the lower limit for the loop bandwidth.

IV. Operating Instructions

The system uses the following power supply voltages and currents:

+15 Volts - 75 ma.
-15 Volts - 56 ma.
-5.2 Volts - 0.63 Amp
-20 Volts - 0.40 Amp
+5 Volts - 50 ma.

A stable 100 MHz reference is required to test the system. In operation, the maser 100 MHz output would be used. A Greenray Model YH-522-45 Oscillator was borrowed from Green Bank. 14 dBm of power was provided by 16 dB of attenuation, followed by 19 dB of amplification.

The phase increment must be initially entered into the NCO. This is accomplished via the DIP switches on the card. The two switch DIP enters the address. The eight switch DIP enters one quarter of the phase increment at a time. The phase increment is added to the phase accumulator at the 5 MHz clock rate. The following table shows the switch settings and corresponding output frequencies.

NCO Output Frequencies in Hz

Off = Logic 1

Address Switch #	Phase Switch #							
1 2	1	2	3	4	5	6	7	8
0 0						78125	39063	19531
0 1	9766	4883	2441	1221	610	305	153	76.3
1 0	38.1	19.1	9.54	4.77	2.38	1.19	0.60	0.298
1 1	0.149	0.075	0.037	0.019	0.009	0.005	0.0023	0.0012

To get a DC output from the test 100 MHz phase detector, a 78125 Hz output is required from the NCO. The 32 bits are entered by the following sequence:

Address	Phase Switches	
00	00000100	Push Button to strobe data in
01	00000000	Push Button
10	00000000	Push Button
11	00000000	Push Button

The PLL must acquire lock. Normally it will self-acquire lock within 2 minutes. The process can be observed by monitoring the output of the test 100 MHz phase detector. A sine wave will be observed. Initially it will slowly decrease in frequency. The rate of change will accelerate as lock is approached. The final output frequency will be the absolute value of the frequency entered via the switches minus 78125 Hz. Lock can also be observed by watching the control voltage on the VCXO. The PLL offset potentiometer is set to cause the control voltage to integrate towards +15 volts on turn on. Thus the loop drifts towards lock. If excessive time passes between turn-on and a frequency being entered into the switches, the loop amplifier might saturate. The system can be reset by turning the power off and on again. Alternatively, the loop offset potentiometer on 3B can be adjusted to pull the amplifier out of saturation towards lock. Readjust the potentiometer for a positive offset later, with the loop out of lock. The potentiometer can not pull the loop out of lock, once lock has been acquired.

For maximum linearity, it is desirable to have the phase detector DC output near zero volts. To slew the output, enter a small frequency difference. For example: Assume 78125 Hz is initially set. Set the address to 11 and the phase switches to 00000100, then push the button. This gives a slew frequency of 0.005 Hz. Set the phase switches to 00000001. When the test 100 MHz phase detector output gets near zero volts, push the button. Then set the switches to 00000000. Push the button again when the output is nearest zero volts.

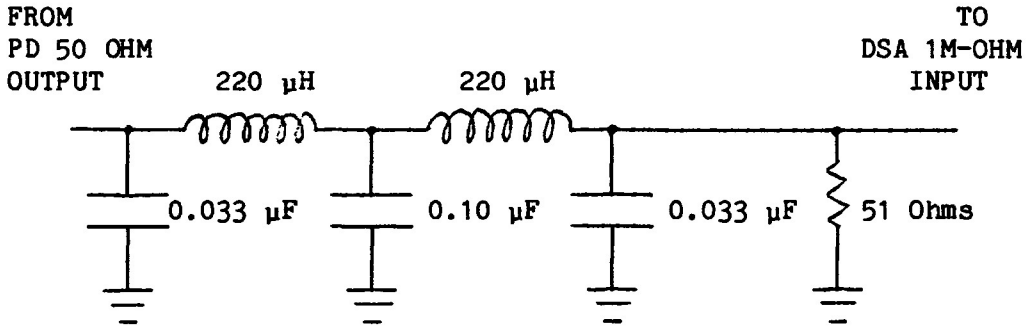
The test 100 MHz phase detector can be made to output a sine wave of frequency F by setting the switches to a frequency of 78125 Hz plus or minus F. For example: 00 - 00000100, 01 - 00000100, 10 - 00000000, 11 - 00000000, gives 305 Hz. Too large a frequency step will temporarily knock the loop out of lock. The output frequency is limited by the three KHz deviation of the VCXO.

V. Stability Measurements

A. Short Term Stability

Short term stability was evaluated using the HP 3561A Dynamic Signal Analyzer (DSA). The test 100 MHz phase detector output is filtered by the 5 pole Butterworth, low-pass filter, shown below.

50 KHz Low-Pass Filter



The filter is necessary to attenuate the 100 MHz and 156 KHz components. The dynamic range of the DSA is not great enough to include the 156 KHz signal level and the expected level of phase noise.

The output of the filter goes to the DSA. The input circuit ground switch is put in the float position. This cuts down 60 Hz pick-up by eliminating the ground loop.

The maser is specified, in specification A53308N001. The maser phase fluctuation should be less than 0.6 ps rms over the frequency range 1 Hz to 1 MHz. To measure the lobe rotator's phase fluctuation, the NCO output is set to 78125 Hz. The test 100 MHz phase detector then outputs a dc component. To have the phase detector in its linear region, and to keep the DSA from over-loading, the dc component is set near zero volts. The dc component can be slewed by turning on and off small frequency increments.

Figure 9 shows the outputs obtained from the DSA. The y axes show volt^2/Hz. On the DSA, auto range was turned off. A single auto-range gave a range of -41 dBV. A 50 Ohm load on the input of the DSA then gave a noise level of -158 dBV. This is below the phase noise values to be measured.

Figure 9A shows the phase noise from 0 to 200 Hz, on a linear scale. Note the reduction in phase noise in the initial 30 Hz, due to the PLL bandwidth. A

strong 60 Hz component can be seen. Broadening the loop bandwidth to 300 Hz, instead of 30 Hz, eliminated the 60 Hz phase peak.

The phase fluctuation can be calculated by integrating the graph with respect to frequency. On Figure 9A, each block is 5.623E-12 V^2/Hz by 20 Hz. This gives an area of 1.12E-10 V^2/block. 15 blocks are counted under the curve, temporarily ignoring the 60 Hz components. 1.12E-10 V^2/block * 15 blocks gives 1.69E-9 V^2. Taking the square root gives V_{RMS} = 4.11E-5 V. It is desired to express this as an rms time variation. The test 100 MHz phase detector gain, with the 50 KHz filter attached, measures K_D = 0.25 V/radian.

$$t_{RMS} = V_{RMS} * (\text{radian}/0.25\ V) * (1E4\ ps/2PI\ \text{radians})$$

$$t_{RMS} = V_{RMS} * 6366\ ps/V$$

For the phase noise 0 to 200 Hz, less the 60 Hz components:

$$t_{RMS} = 4.11E\text{-}5V * 6366\ ps/V$$
$$= 0.26\ ps.$$

Figure 9B shows the same signal on a log scale with a frequency range of 0 to 2 KHz. The three main components of the phase noise can be seen. They are:

1. The 1/f noise, as was measured with figure 9A.

2. The 60 Hz components.

3. The flat, broad-band noise at -135 dBV.

The phase noise due to the 60 Hz components can be calculated as follows. Using the display of figure 9B, the peak values were read on the DSA as follows:

60 Hz - 348.7E-12 V^2/Hz

120 Hz - 3.5E-12 V^2/Hz

180 Hz - 4.0E-12 V^2/Hz

240 Hz - 0.9E-12 V^2/Hz

The phase fluctuation can be obtained by integration. Each peak is assumed to be a triangle with a base width of the measurement band-width (19.1 Hz). Thus the integration yields:

$$(348.7 + 3.5 + 4.0 + 0.9)E\text{-}12\ V^2/Hz * 19.1\ Hz / 2 = 3.41E\text{-}9\ V^2$$

$$t_{RMS} = SQRT(3.41E\text{-}9\ V2) * 6366\ ps/V$$

$$= 0.37\ ps.$$

Figure 9C shows the 0 to 100 KHz spectrum of the same signal. The 78.125 KHz signal is due to some of the 100 MHz carrier being present from the previous

mixer. The 100 MHz then mixes with the 100.078125 MHz to give the 78.125 KHz. The 39.0625 KHz comes with the 78.125 KHz signal from the divide by 64. The next divider stage causes the distortion. The peaks at 21 KHz, 56 KHz, and 100 KHz are spurious signals from the DSA. They disappear when the DSA, input circuit ground switch is put in the chassis position (i.e. The input ground is not floating). Since these are not corruptions of the VCXO output, they can be ignored in computing the phase fluctuation of the VCXO. The dc spike can be ignored, since it is the constant phase offset. The flat portion represents the broad-band noise level of -135 dBV. The falling off, starting at 30 KHz, coincides with the 50 KHz filter curve. The rms phase fluctuation can be calculated by integrating with respect to frequency. It is assumed that all significant phase noise is less than 100 KHz. 100 KHz is also the upper limit of the DSA. -135 dBV equals 3.16E-14 V^2/Hz. Multiplying by 100,000 Hz gives 3.16E-9 V^2. This gives a phase fluctuation of:

$$t_{RMS} = SQRT(3.16E-9) * 6366 \text{ ps/V}$$
$$= 0.36 \text{ ps.}$$

Combining the 1/f and broad-band noise phase fluctuations gives:

$$t_{RMS} = SQRT(0.26^2 + 0.36^2) \text{ ps}$$
$$= 0.44 \text{ ps.}$$

Combining in the 60 Hz phase noise yields:

$$t_{RMS} = SQRT(0.44^2 + 0.37^2)$$
$$= 0.57 \text{ ps.}$$

However, the 60 Hz noise should be easily attenuated by building the system in a shielded enclosure, as opposed to the breadboard's open construction.

These all meet the maser specification of 0.6 ps rms. An improvement of a factor of three would be needed in a final system.

With the DSA in the 0 to 2 KHz range, the lobe rotator was set to output 305 Hz. An auto-range was performed to the -15dBV range. The 305 Hz carrier had a peak value of -27.4 dBV/Hz. The noise floor was down 90 dB, due to the dynamic range of the DSA. However, the carrier value could be compared to the noise from figure 9B, to give the actual dB below the carrier. Figure 9B shows the phase noise without a large carrier or DC component present to saturate the DSA. The following values were calculated:

100 Hz away	88 dBc/Hz
200 Hz away	96 dBc/Hz
1000 Hz away	106 dBc/Hz
2000 Hz away	107 dBc/Hz

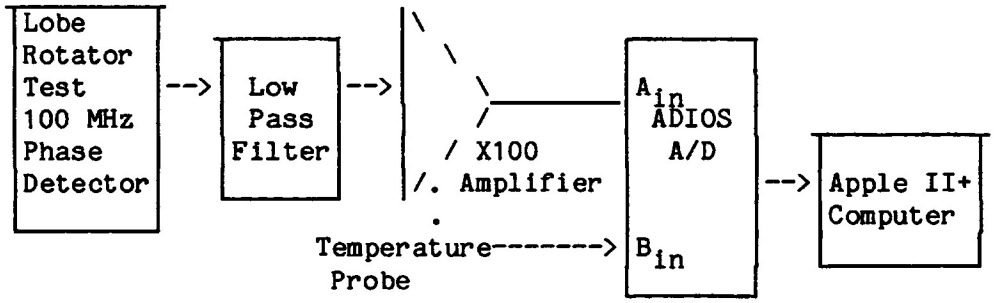
These values coincide well with the specification of the VCXO.

If the 100 MHz signal was multiplied to 100 GHz, the carrier to noise levels would deteriorate by 60 dB. Thus, it is evident that some noise improvement of the lobe rotator or further clean-up in a narrow-band PLL is needed. A 10 db lower phase noise VCXO is available which could improve the lobe rotator phase noise. This is further discussed in Section VI, Possible System Improvements.

B. Long Term Stability

The long term stability was analyzed using the Frequency Standard Test Program, which is described in Electronics Division Internal Report No. 232 by S. Weinreb.

Fig. 10. Long Term Stability Test Configuration



5 KHz Low Pass Filter Details

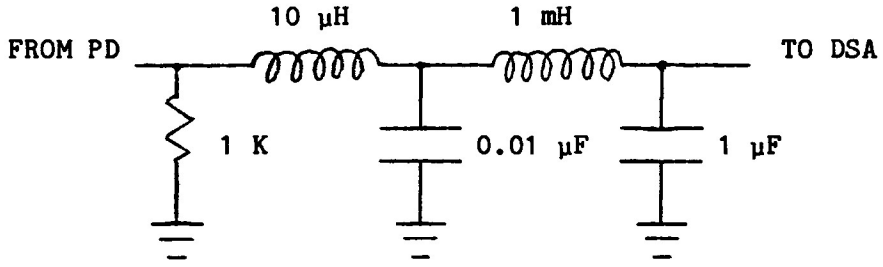


Figure 10 shows the long term stability test configuration. The test 100 MHz phase detector outputs to a two stage low pass filter. The 1K resistor provides a suitable load. The first stage filters out components 100 MHz and above. The second stage filters out 5 KHz and above. The output of the filter goes to the battery powered NRAO LOG AMP. The DB/DIV switch is in the LIN position for linear operation. The +/- switch is in the + position. The CAL/3 DB switch is in the CAL position. This provides a low noise linear amplifier with a gain of 100. The amplifier outputs to the ADIOS A/D A_{IN} port. A temperature probe is connected to the B channel, as described in Internal Report No. 232. The temperature probe is taped to the NRAO LOG AMP. The ADIOS A switches are set to +- 1 V. The B switches are set to + 10 V. The Apple II+ computer runs the program FST86. This takes the data and computes the Allan variances.

The following parameters were fed to the program:

1. Phase detector full scale = 30 ps.

This is calculated from the 100 MHz, test phase detector gain, K_D = 0.535 volts/radian. Note this is higher than the value used in the short term stability calculations. This is due to less loading by the LPF.

0.535 volts/radian * 100 gain * 2*PI radians / 10000 ps = 1 volt / 30. ps.

2. A perfect reference is assumed.

Figure 11 shows the long term stability outputs from the program. A continuous series of 13000 second runs was set up to run over night.

Figure 11A shows the last 13000 second run. The squares show the 1 second Allan variances. The crosses show the frequency drift. The line reflects the room temperature variation. The cycling of the air conditioner can be clearly seen. There is a peak to peak variation of 0.6 degrees C., and a period of 1800 seconds. The period was longer for night 13000 second runs. The temperature variation has only a minor effect on the lobe rotator operation.

Figure 11B shows the lobe rotator Allan variances for the 14.5 hours of data. The maser specification is shown on the diagram. The lobe rotator meets the criteria set forth in VLBA Acquisition Memo #60, by Alan Rogers. That criteria is that the Allan variance of the phase error in the rotation should be less than one third the maser Allan variance specification. The hump in the data around 1000 seconds can be attributed to the temperature cycling.

To determine the stability of the test 100 MHz phase detector, 9dBm at 100 MHz was fed directly into the L and R ports of the phase detector. Since this is 5 dB down from the power levels used in the lobe rotator, the full scale phase detector value of 30 ps was divided by 10E(-5/20) to give 53 ps. The Allan variance can be seen in Figure 11C. It is about an order of magnitude better than the total lobe rotator.

Figure 11D shows the stability of the X100 amplifier with a 50 Ohm load on the input. A 30 ps full scale value was used. This exceeds the stability of the phase detector as expected.

VI. Possible System Improvements

The breadboard system uses an open construction method. The system could be enclosed in a well shielded cabinet to reduce 60 Hz pick-up.

Currently, the 100 MHz components are interconnected by OSM connectors. A prototype system could have the 100 MHz components mounted on a PC board, interconnected by microstrips. This would reduce component cost and module size.

The mixer amplifier of figure 8 would be better mounted near the mixer, to reduce noise pickup.

The system is susceptible to microphonics, so a low vibration environment is desirable.

Having the system in a temperature controlled environment would enhance long term stability.

It would be desirable for a prototype system to contain circuitry to aid the PLL in acquiring lock. This could be achieved by alternately slewing the VCXO control voltage up and down. A lock detector could shut off the slewing mechanism, once lock is attained. Otherwise, continued slewing would stress the loop and cause a phase offset.

The phase increment could be entered via computer rather than by hand.

If it is desired that the output be at 100 MHz plus the fringe frequency, a second PLL could be added. This PLL could subtract the 78125 Hz reference from the current system output. This second PLL would add some phase instability.

Refer back to Figure 1. The lobe rotator output from the directional coupler had sidebands plus and minus 78125 Hz from the carrier. These were down 70 dB below the carrier. They were not present on the output of the VCXO. They are due to signals returning from the mixer into the 10 dB port of the directional coupler. These signals could be greatly attenuated by using a buffer amplifier from the directional coupler to the mixer.

A lower phase-noise VCXO could be used to improve the short term stability. Ed Selig at Vectron (203-853-4433) was contacted. The Vectron CO-233VFWT ($315) is the current VCXO. For $50 additional, they could reduce the phase noise 10 dB.

VII. Conclusion

This lobe rotator would be a viable way to implement lobe rotation by frequency offsetting the reference signal.

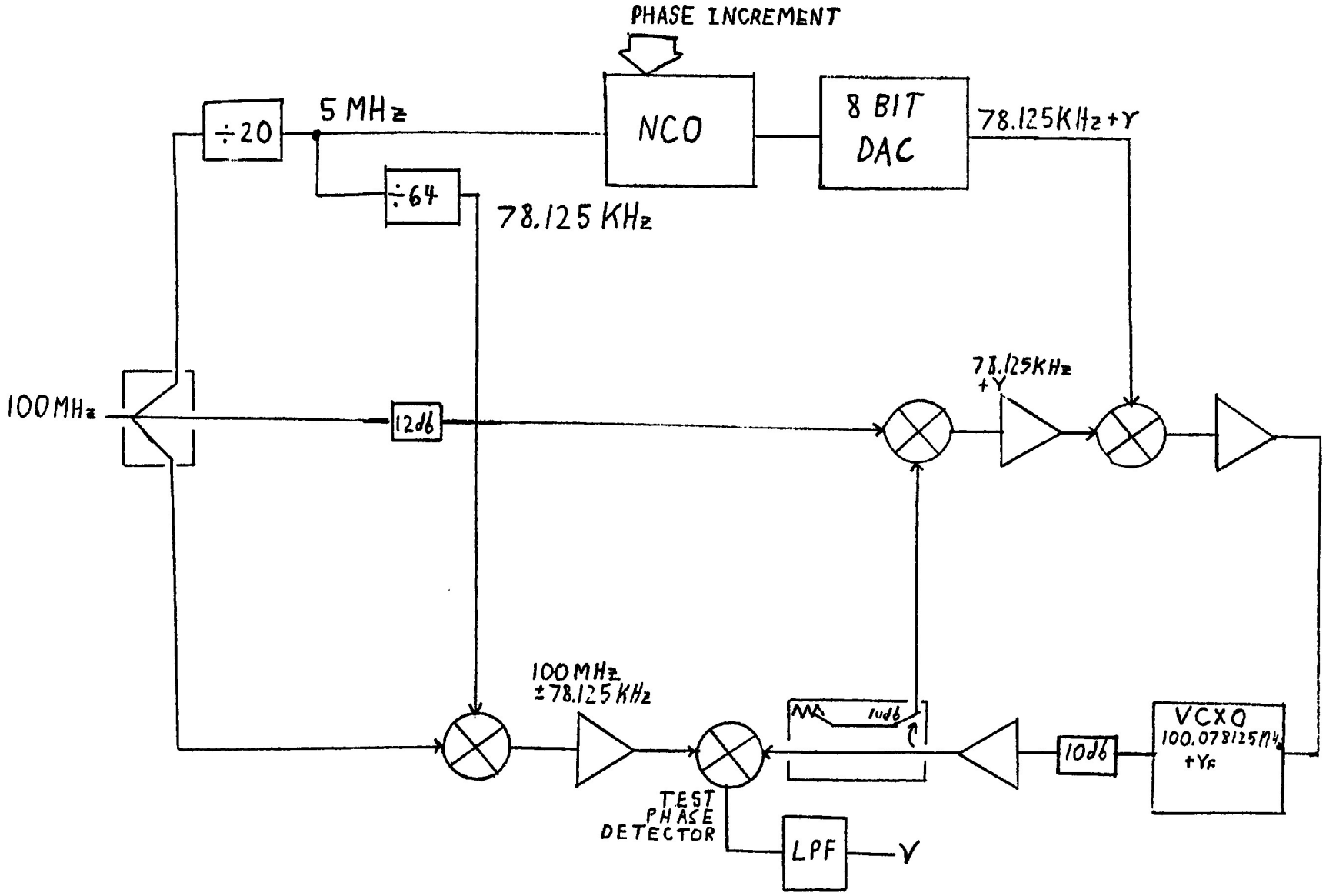


FIGURE 1

VLBA FRINGE ROTATOR

JHG 5/12/86

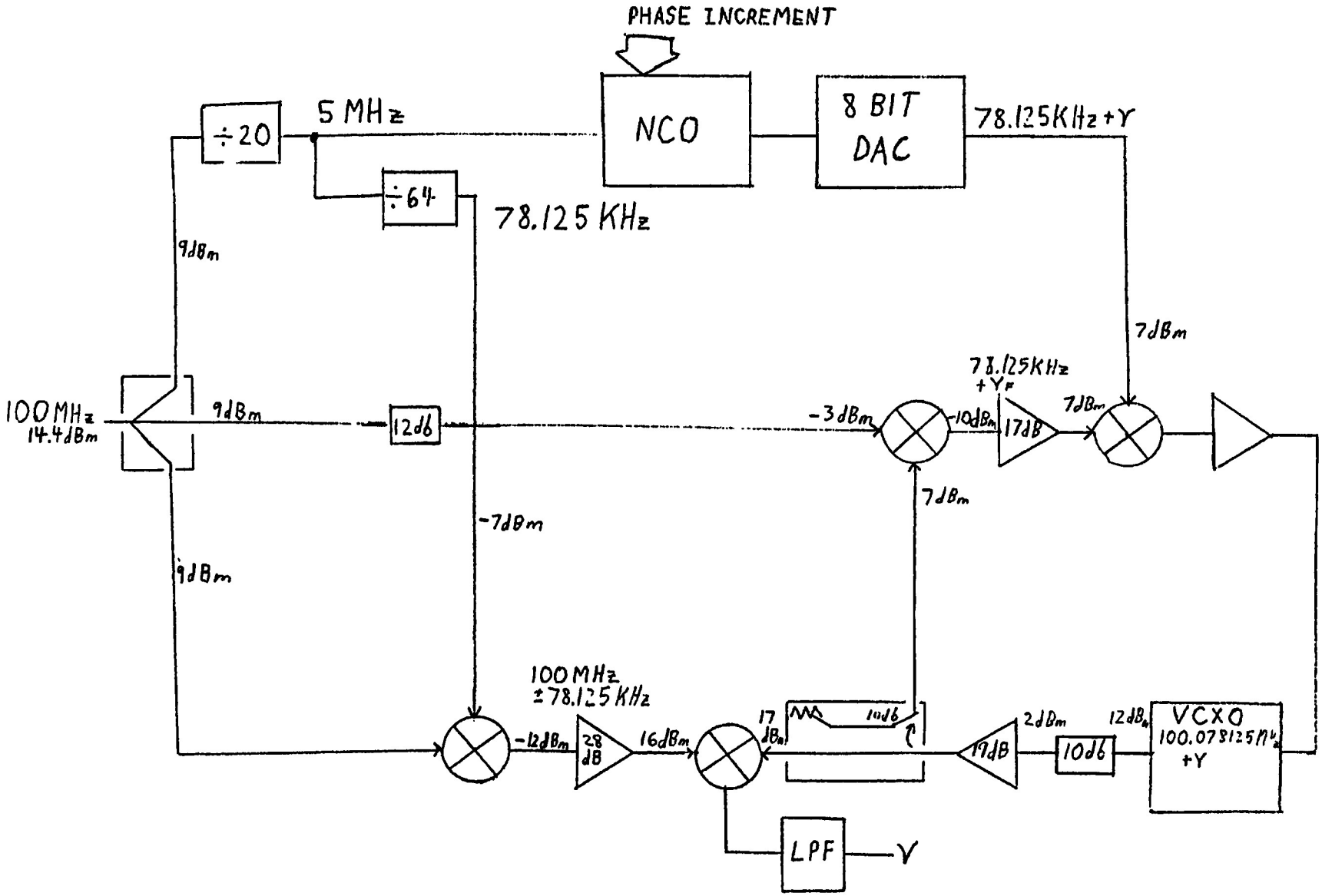
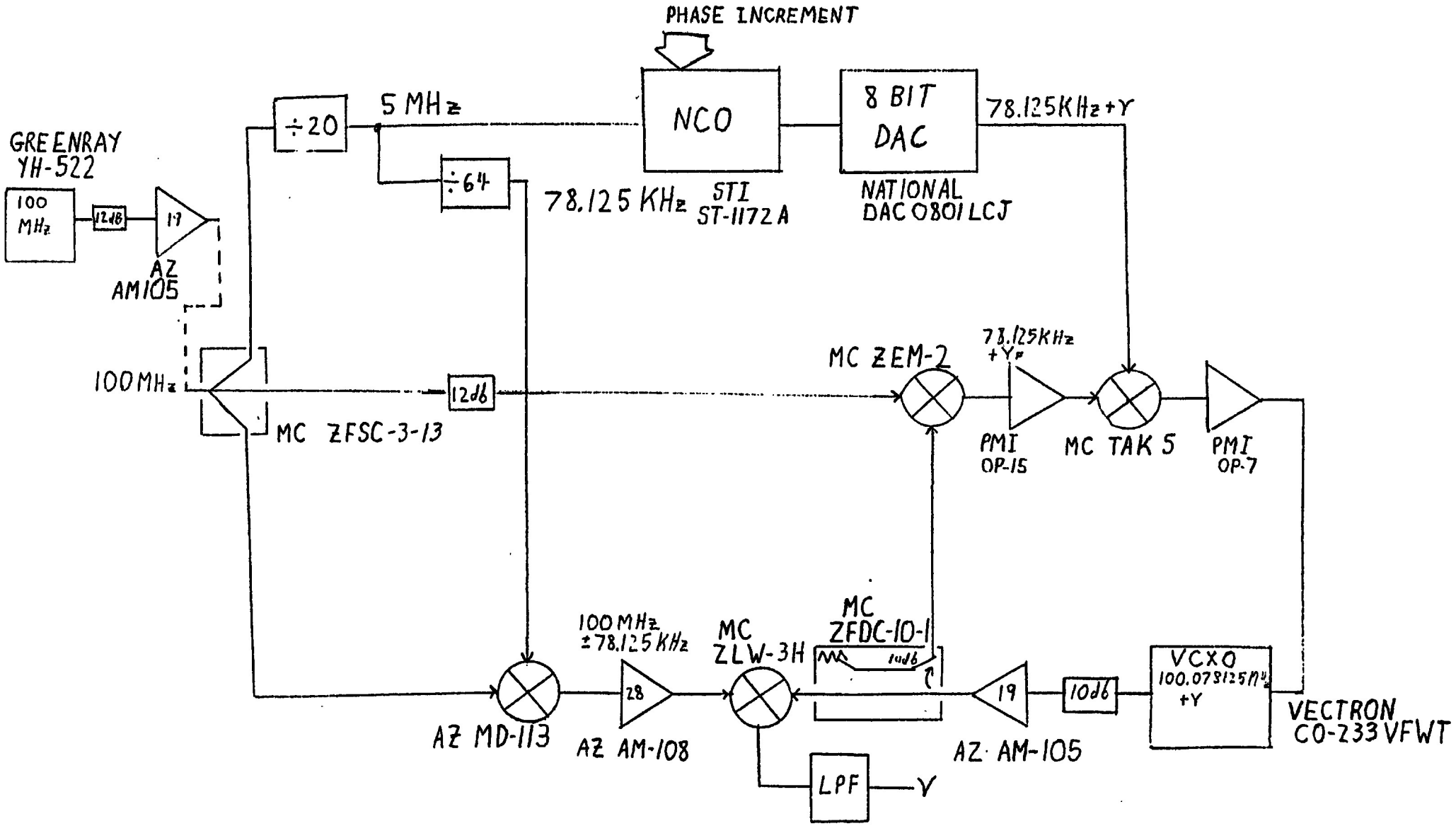


FIGURE 2

VLBA FRINGE ROTATOR POWER LEVELS

JHG 5/12/86



MC - Mini-Circuits
AZ - Anzac

FIGURE 3

VLBA FRINGE ROTATOR VENDORS

JHG 5/12/86

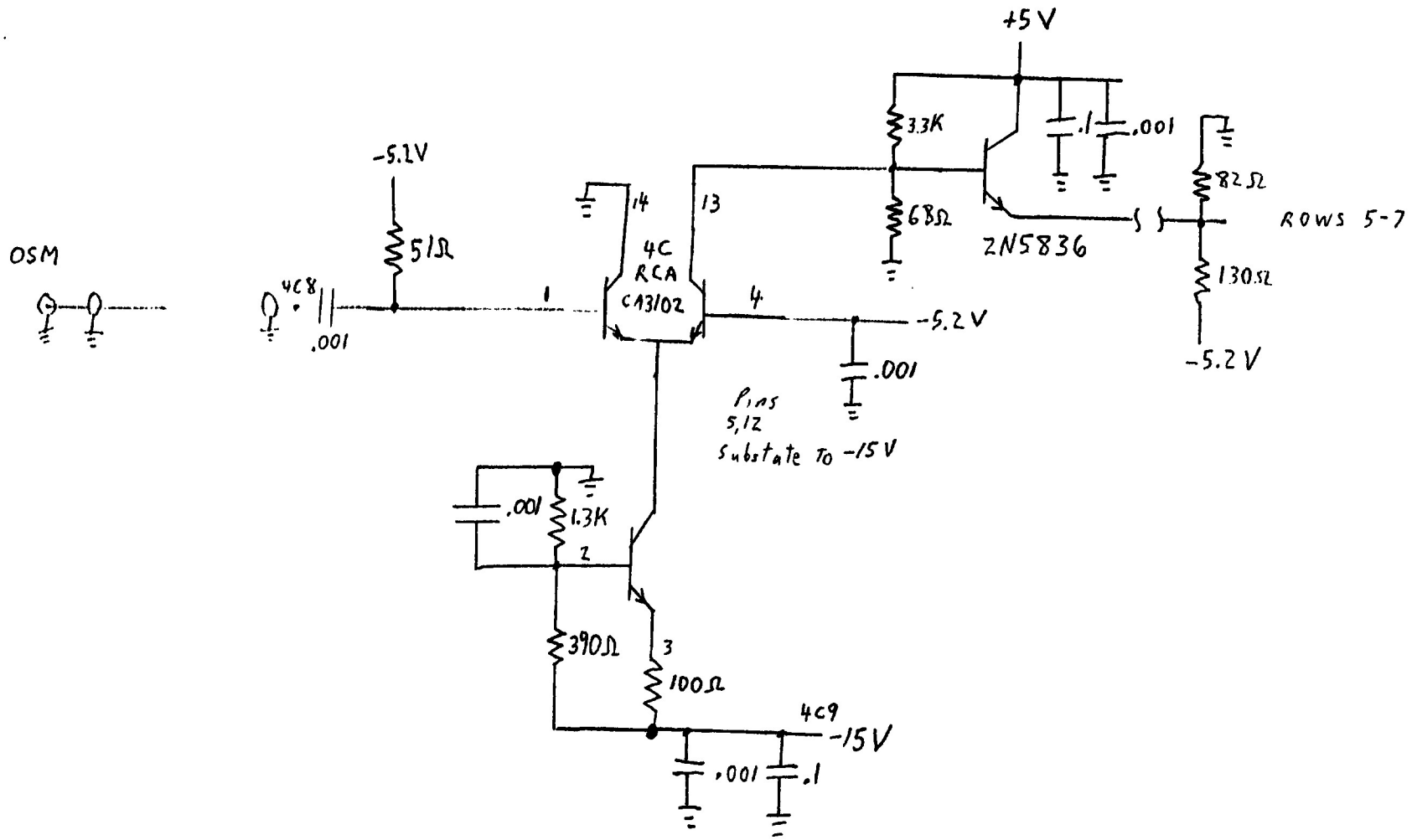


FIGURE 4
CLOCK DRIVER

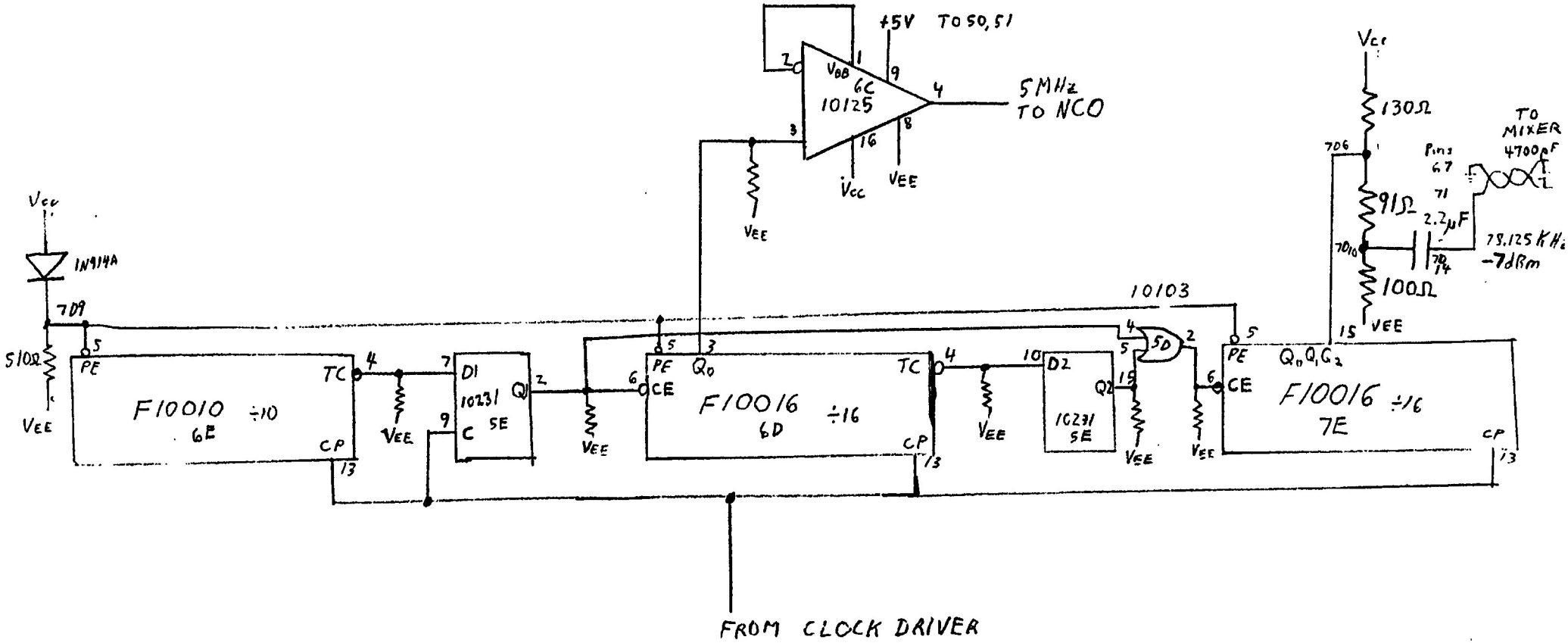
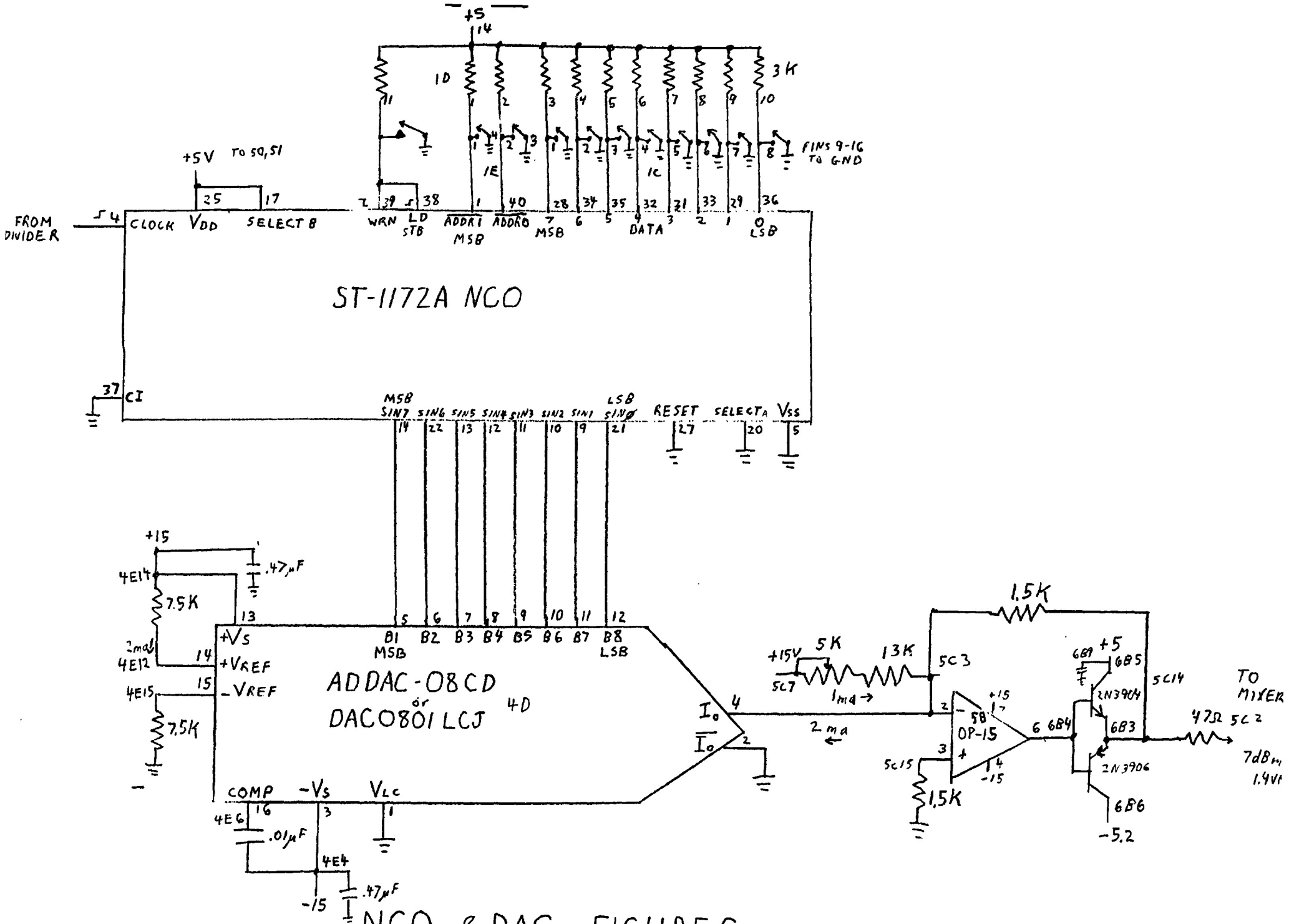


FIGURE 5
ECL DIVIDER

11.116, 10231, 10103, 10016, 10010 V_{CC} -1.16 V_{EE} -8
V_{CC} GND V_{EE} -5.2V
220Ω PULL-DN RESISTORS



NCO & DAC FIGURE 6

ST 1172A BLOCK DIAGRAM

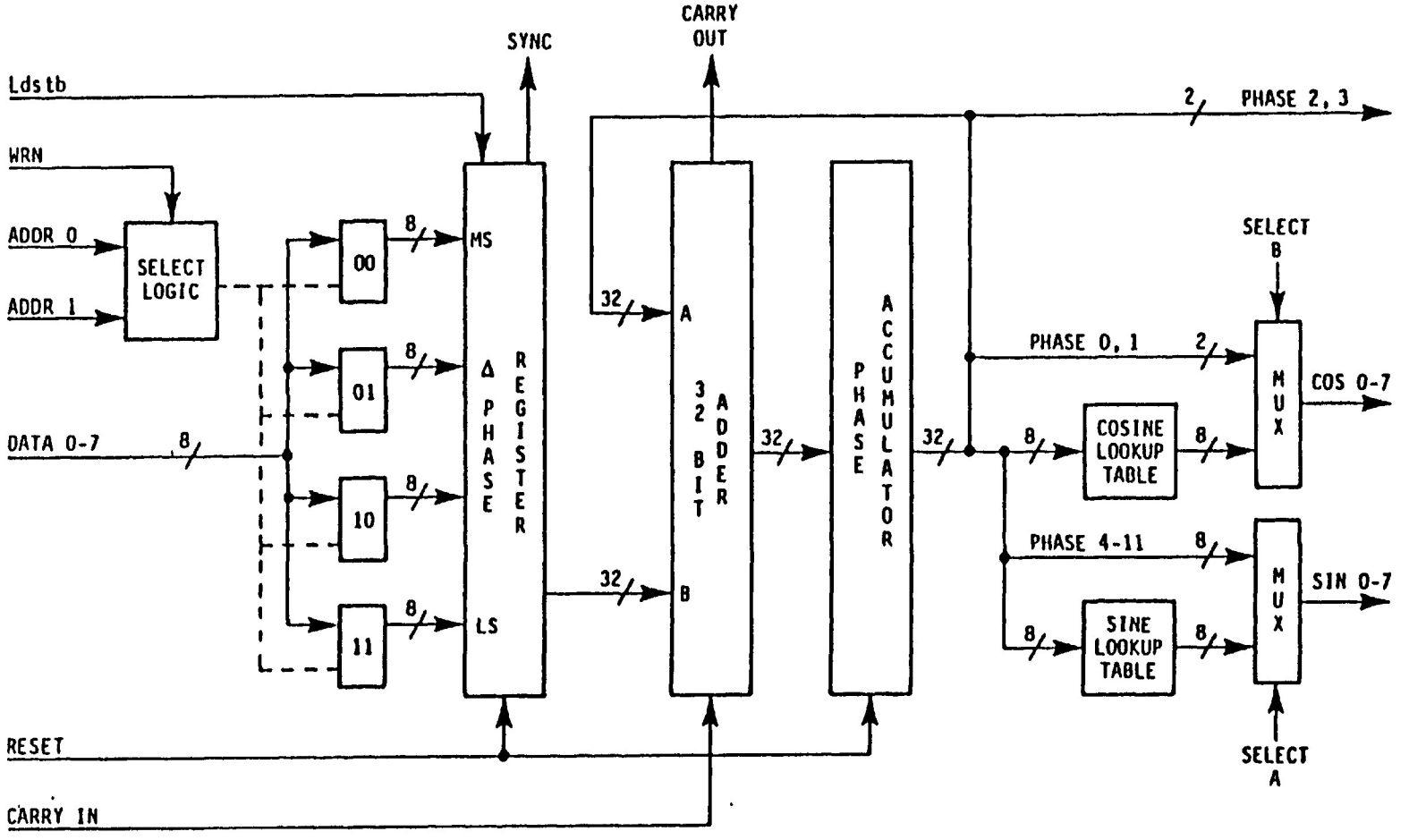


FIGURE 7

STANFORD TELECOMMUNICATIONS INC.
2421 Mission College Blvd., Santa Clara, CA 95054 408-748-1010

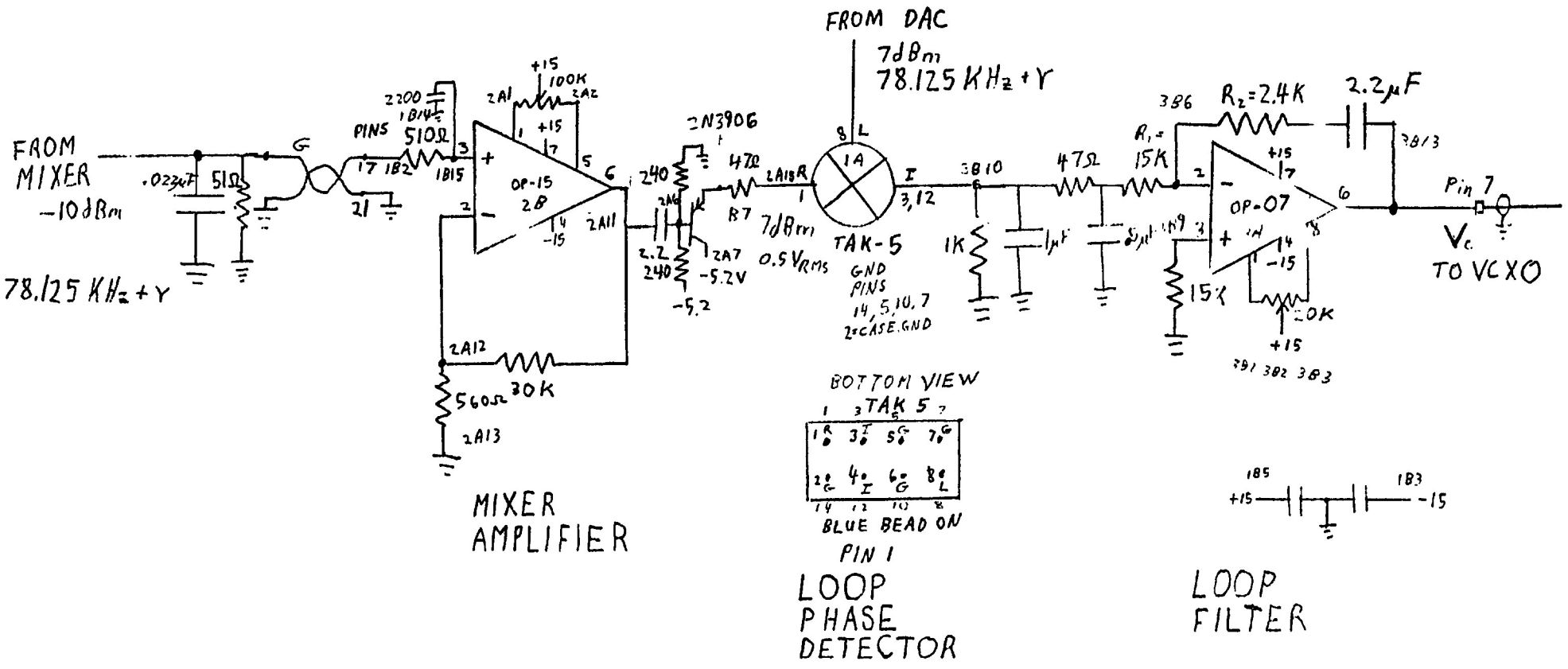


FIGURE 8

LOOP FILTER

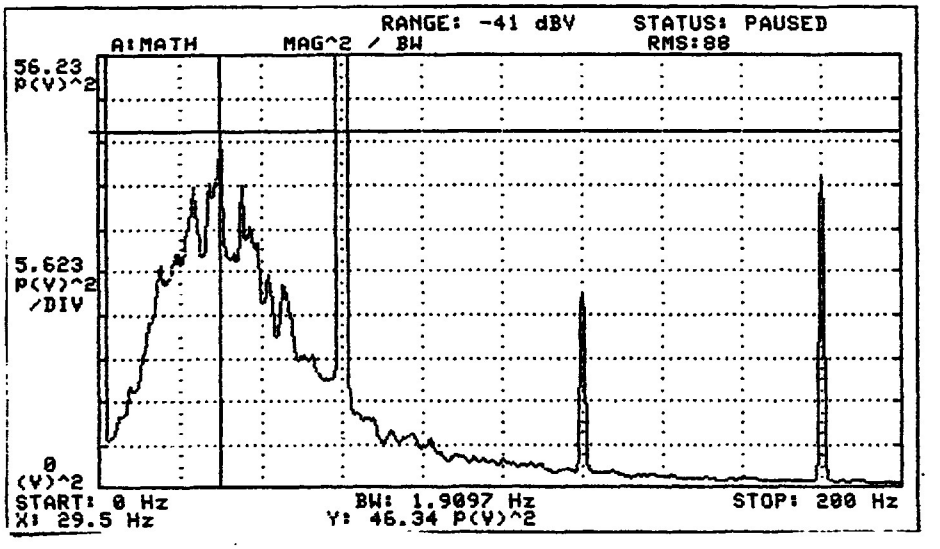
-5.2V Pins 98, 100

+5V Pins 50, 51

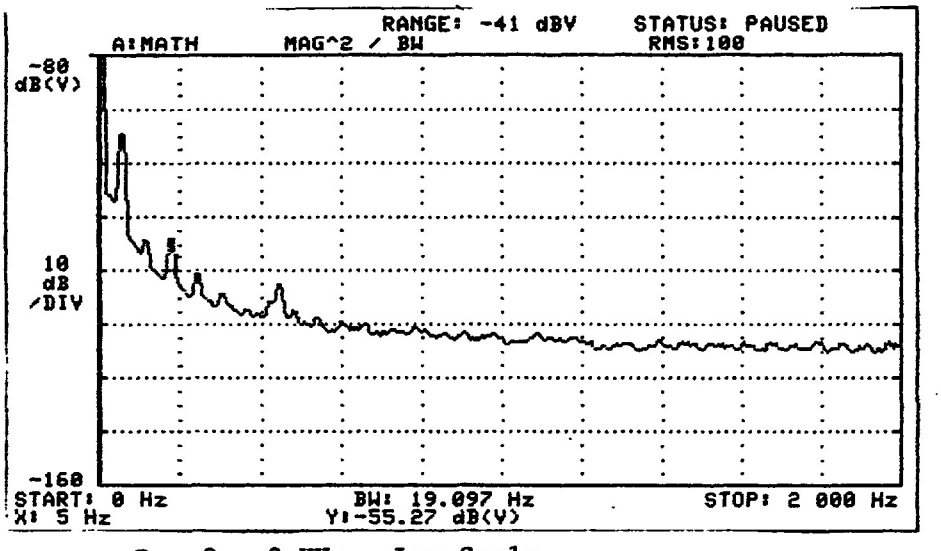
+15V Pins 3, 4

-15V Pins 33, 34

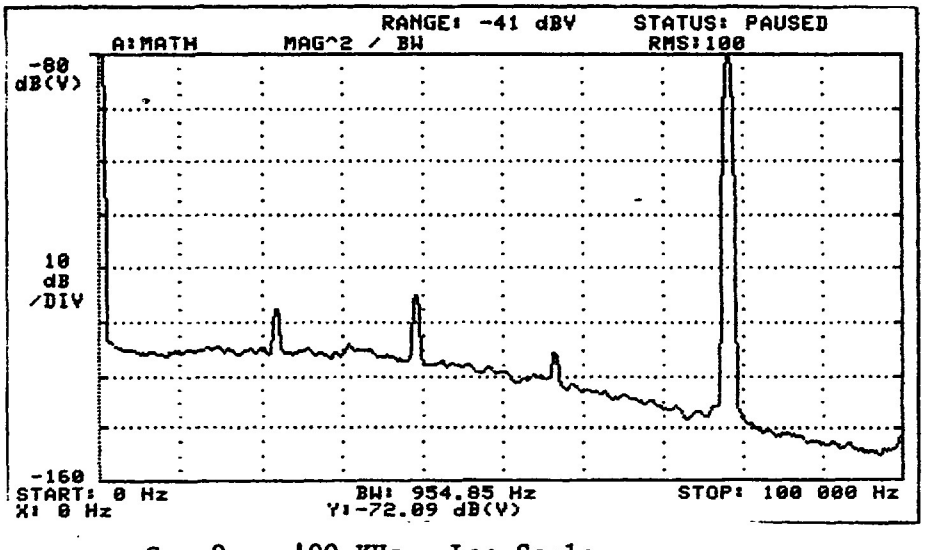
Figure 9 - Short Term Stability



A. 0 - 200 Hz - Linear Scale

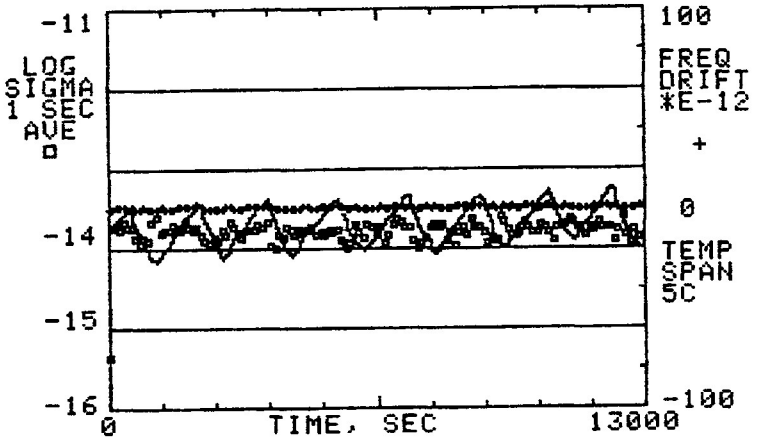


B. 0 - 2 KHz - Log Scale

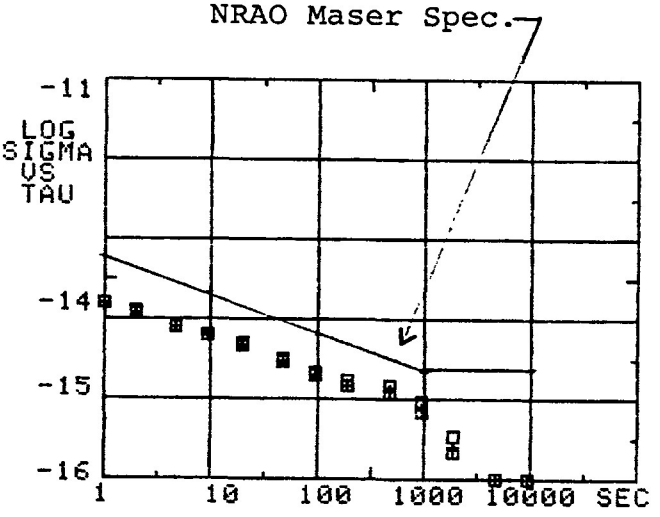


C. 0 - 100 KHz - Log Scale

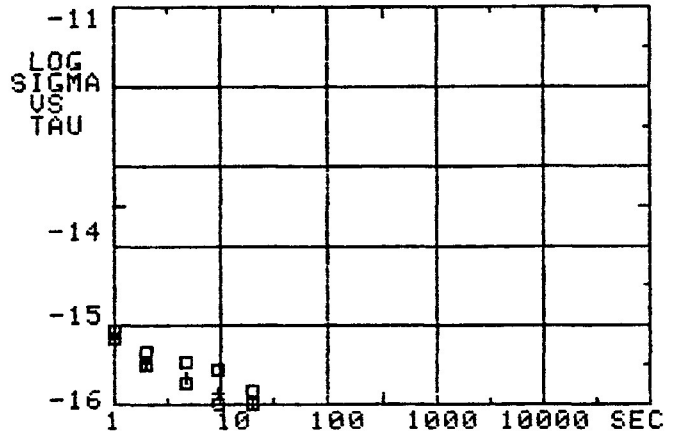
Figure 11 LONG TERM STABILITY



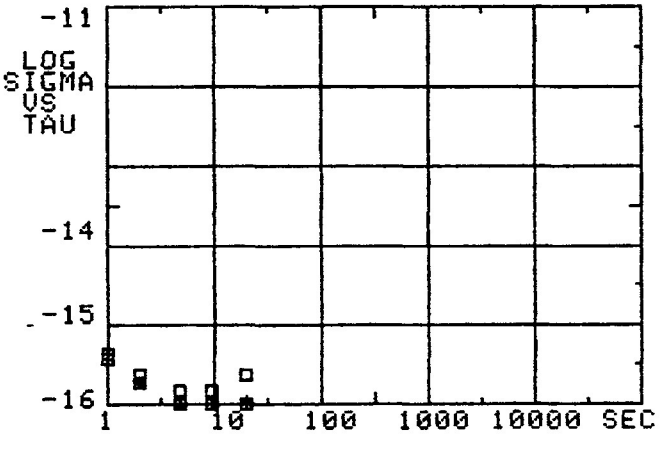
A. Fringe Rotator -
Last 13,000 Second Batch



B. Fringe Rotator -
Allan Variance Values



C. Test Phase Detector -
Allan Variance Values



D. X100 Amplifier -
Allan Variance Values