Interoffice

National Radio Astronomy Observatory

Charlottesville, Virginia

July 15, 1982

VLB ARRAY MEMO No. 101

To: VLBA Proposal Group

From: R. Escoffier

Subject: Possible Block Diagram for VLBA Correlator

In the first meeting of the VLBA correlator subgroup, we talked about working up block diagrams for various possible designs for a VLBA correlator. In response, I have attached the block diagram I worked with in the VLBA proposal correlator cost estimate. It is in a somewhat crude form as can be seen and was not meant to be published. However, if anyone thinks it useful, I could spend a week or so to clean it up and make it a little more coherent.

This design is based on the 100 MHz clock rate, recirculating VLA correlator and uses both custom IC's developed for the VLA correlator.

Figure 1 is the overall block diagram. This diagram shows the approximate size of each block by an estimate of P.C. cards needed for each. Printed circuit card size and density similar to the VLA design was assumed.

The next few figures are block diagrams of some of the individual cards. Figure 2 is a sketch design of a recirculator card. One such card will be required for each antenna. It will allow time sharing the 100 MHz correlators between the up to four 25 MHz input cards.

Figure 3 shows the fringe counter card. This card will track the fringe phases of up to 56 (or maybe only 28) bands using an initial phase and some number of phase derivatives. This fringe phase counter is outside of the recirculating path and additional fringe phase updating is needed at the 100 MHz recirculated data rate. Figure 4 shows these high speed fringe counters inside the recirculation path. Signal fan-out to the correlators also occurs on this card.

Figure 5 is a diagram of the correlator card. The two antenna fringe phases are subtracted on this card to yield the baseline fringe phase which is then applied to one signal path to accomplish fringe rotation. The baseline vernier bit is provided on this card as well as is baseline blanking, and the product count (V_8). Each recirculation (about 100 μsec) 64 12-bit integration results are generated by each such card. The recirculator can be programmed to yield either alternate bands (continuum) or additional lag channels (line) for subsequent integrations.

Figure 6 is a block diagram of the integrating system. The 12-bit serial correlator results are shifted in and added to partial integration products already in the integrating RAM's. When the integration is complete, the up to 819200 results are dumped into the storage RAM's for access by the computer system while the integrators are cleared for another integration.

Figure 7 is a diagram of an integrator/storage card.

Figure 8 tabulates card count, IC count, cost, and power consumption for the system. Based on the VLA experience, these numbers look fairly reasonable. The figure of 39,000 IC/system is about one-half the size of the VLA correlator. Figure 9 is a possible rack layout with 14 recorder racks, one rack for the recirculators and control logic, 4 racks for the drivers, correlators, and integration, and one (?) rack for a computer and array processor.

I did not include any self-test considerations in this design but since it is so closely parallels the VLA correlator, a self-test, self-heal capacity can be built in as desired, following the VLA design.

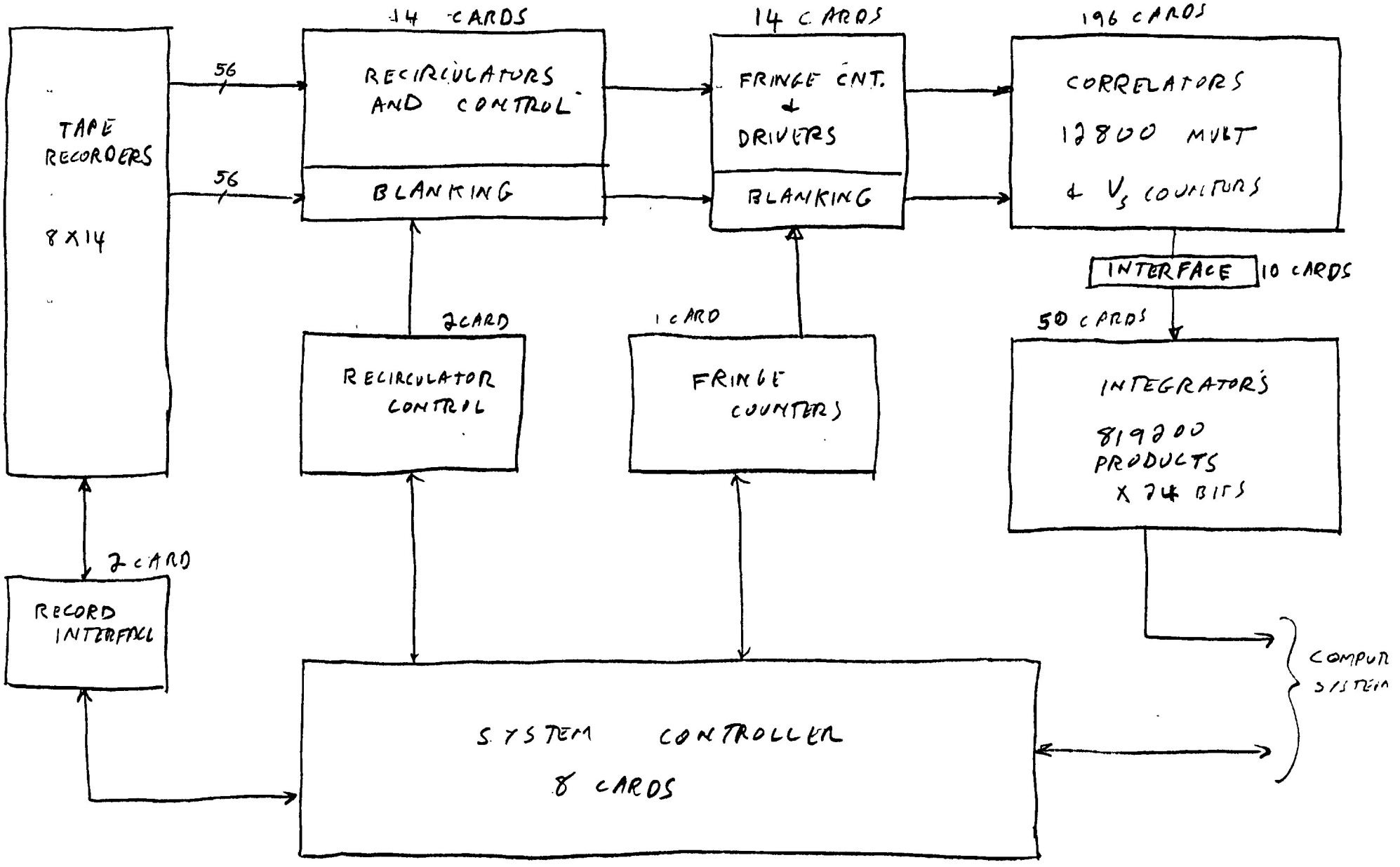
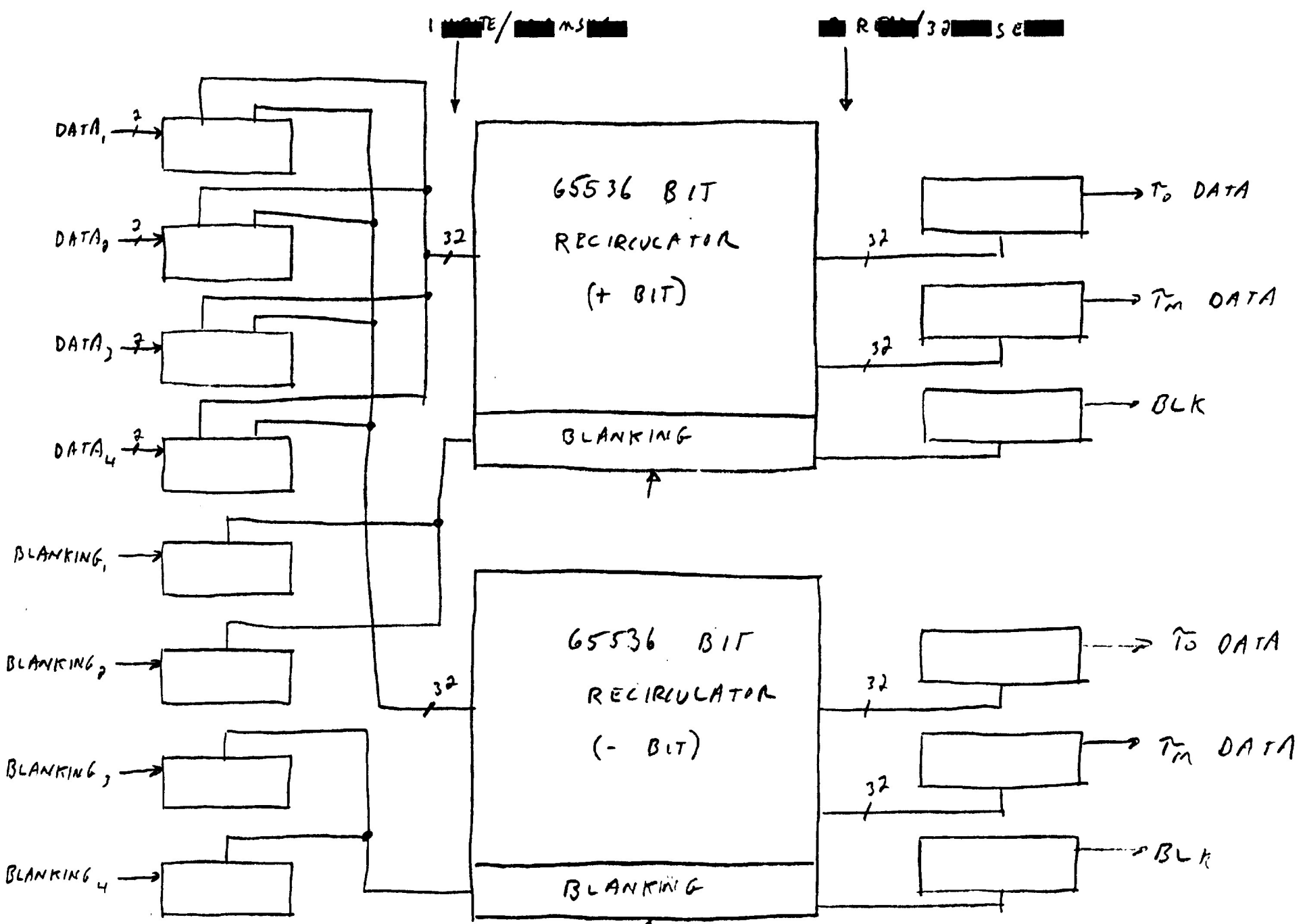


FIGURE 1

291 CARDS

1-22-82
RPE



IC	
16	8192 BIT MEM
36	SHIFT REG
32	ECL SHIFT REG
20	MISC
104	IC'S

FIGURE 2

ONE/ANT RECIRCULATOR

14 TOTAL

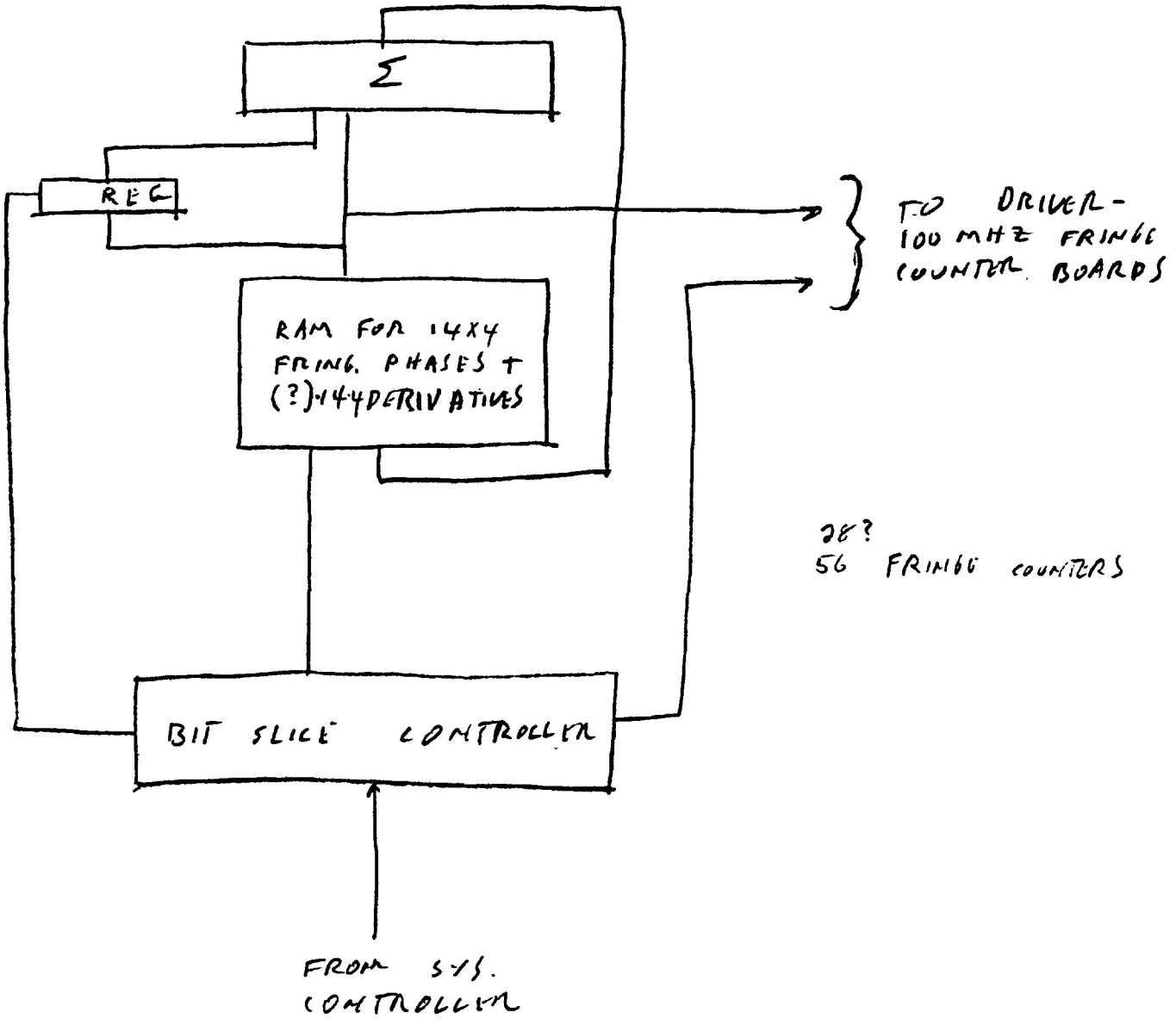
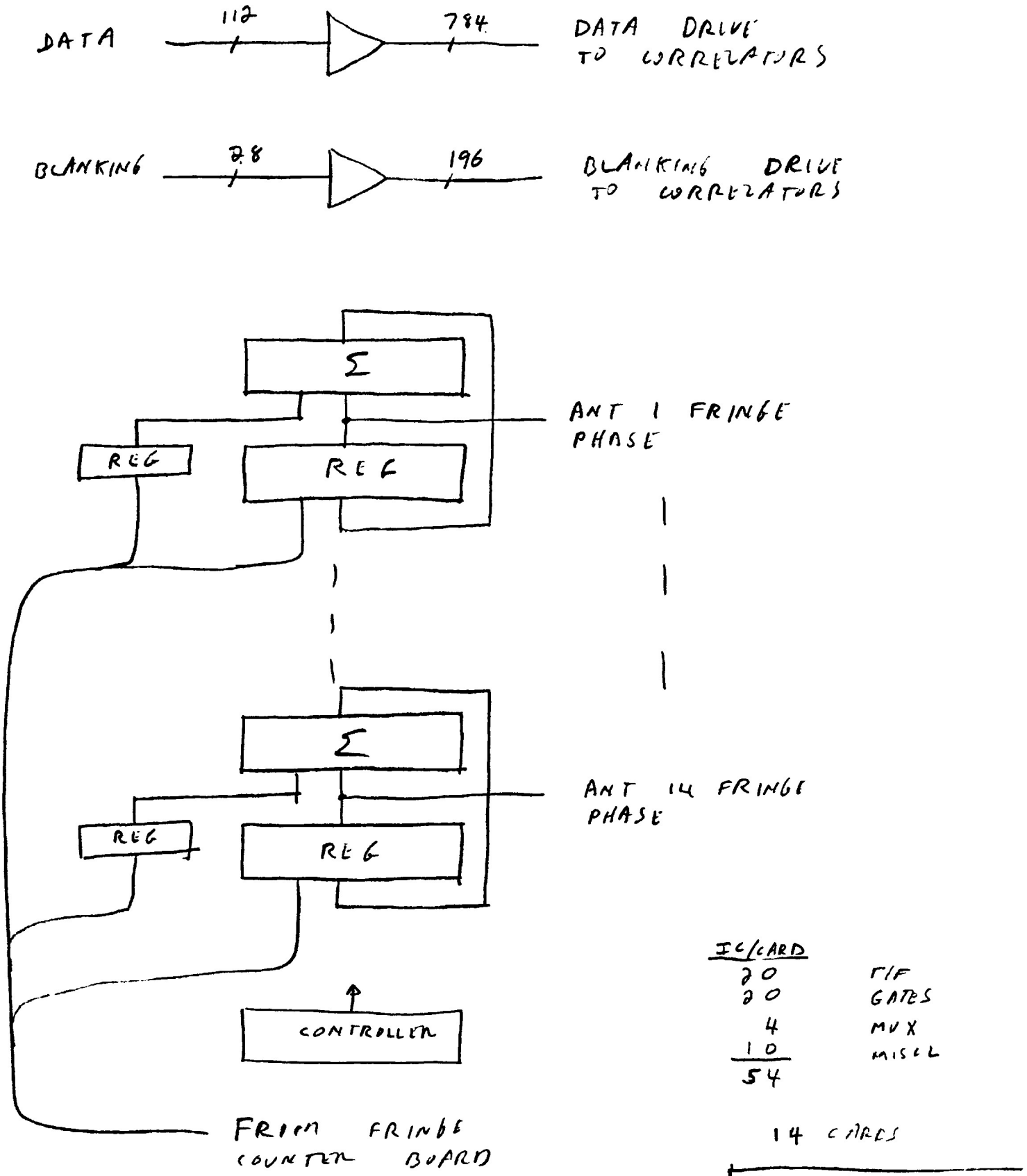


FIGURE 3

1 CARD

FRINGE COUNTERS



IC/CARD	
20	F/F
20	GATES
4	MUX
10	MISC
54	

14 CARDS

DRIVER SYSTEM AND 100 MHz FRINGE COUNTERS

FIGURE 4

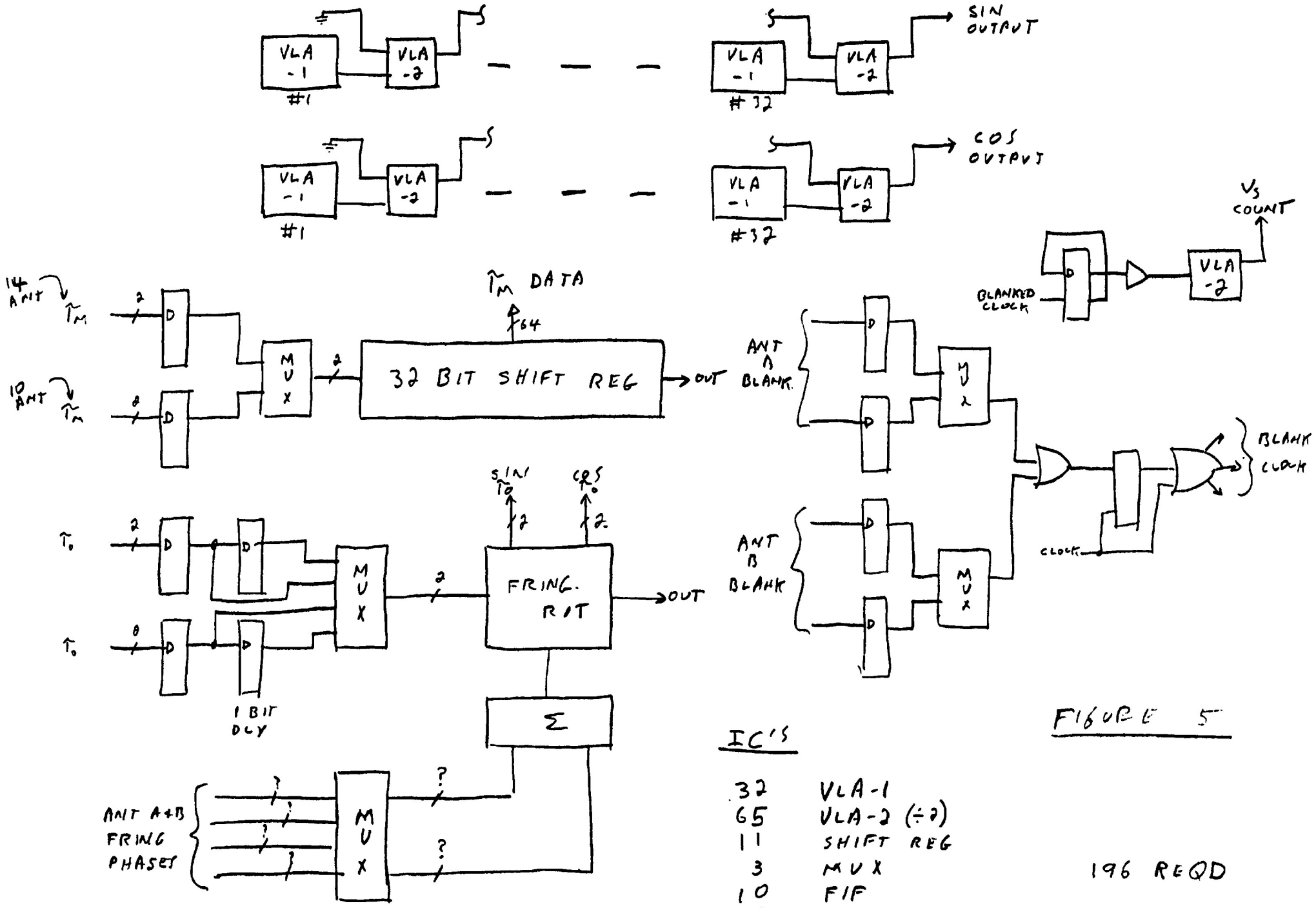


FIGURE 5

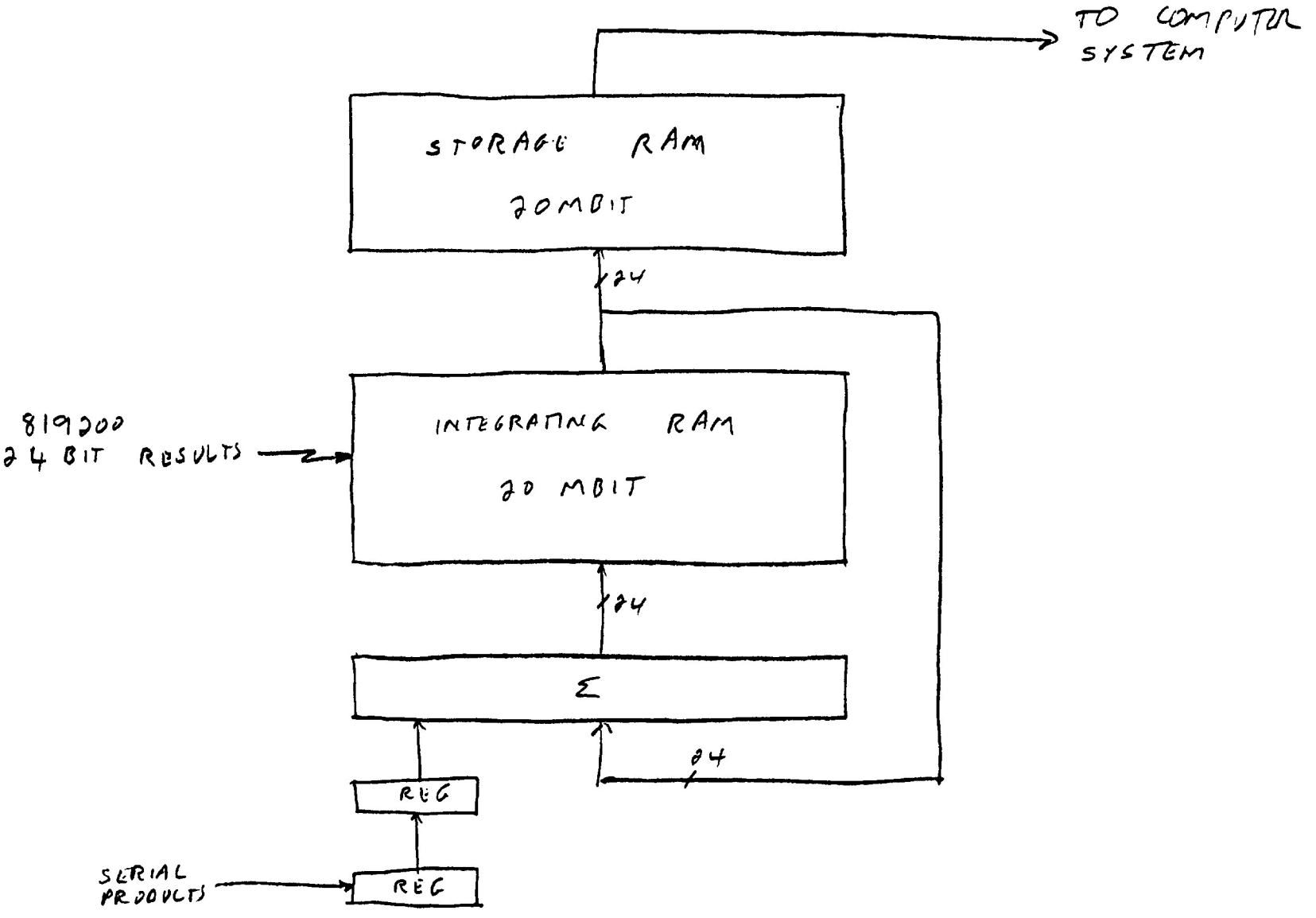
IC's

32	VLA-1
65	VLA-2 (÷2)
11	SHIFT REG
3	MUX
10	FIF
29	MISCL
150	

196 REQD

MULTIPLIER CARD

1-28-82 RPE

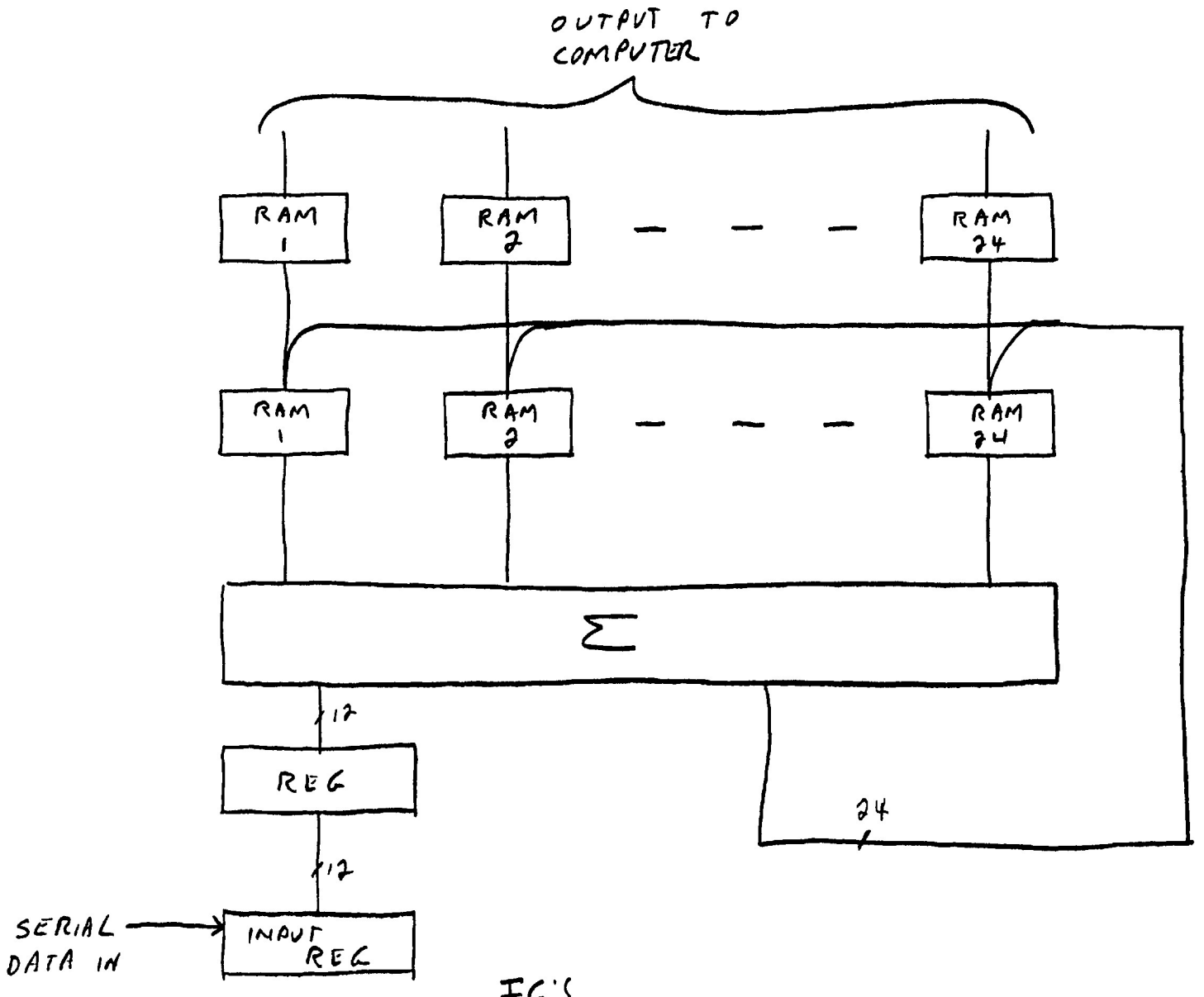


50 CARDS

FIGURE 6

INTEGRATOR

1-22-87 RPE



IC's	
48	16384 BIT RAMS
6	ADDERS
4	REG.
20	MISCL
78	

50 REQD

FIGURE 7

INTEGRATOR/STORAGE CARD

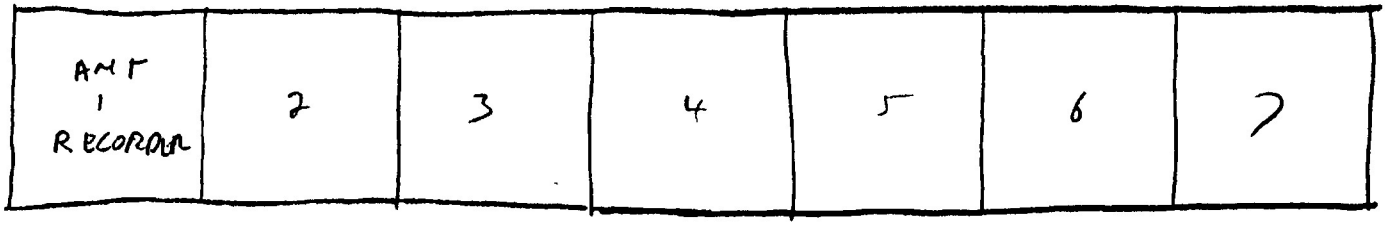
1-28-82 RPL

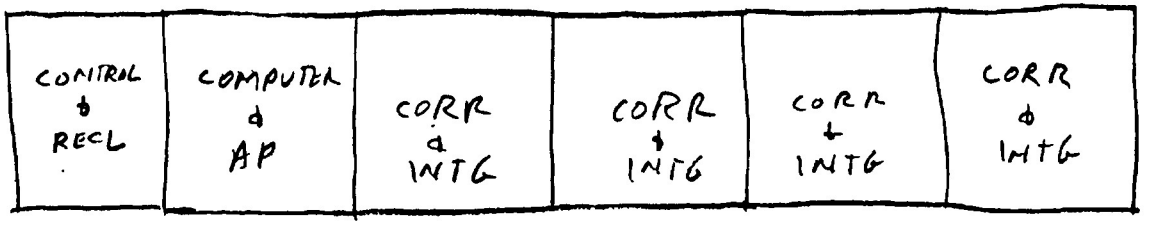
CARD	#/SYS	IC/CARD	COST/CARD	POWER/CARD	IC/SYS	COST/SYS	POWER/SYS
RECORDER INTERFACE	2	60	$200		120	$.4K	
RECIRCULATOR CONTROL	2	60	$200		120	.4K	
RECIRCULATOR	14	105	$628		1475	8.8K	
FRINGE COUNTERS	1	50	$250		50	.25K	
DRIVERS	14	54	$275		756	3.8K	
MULTIPLIERS	196	150	$1765	75W	29400	345K	14.7KW
INTEGRATORS	50	78	$485	40W	3900	24K	2 KW
SYSTEM CONTROLER	8	60	$370		480	3K	
INTERFACE	10	60	$160		600	1.6K	
MISCL	25	60	$130		1500	3.2K	
	322				39K	$392K	20KW

≃ 30KW w/INEFF.

POWER SUPPLIES	$30K
P.C. CARD DEVL	.40K
METAL WORK	8K
CABLES	10K
MOTHER BOARDS	10K
RACKS	5K
MISCL	50K
	153K

FIGURE 8


ANT
1
RECORDER
2
3
4
5
6
7


CONTROL
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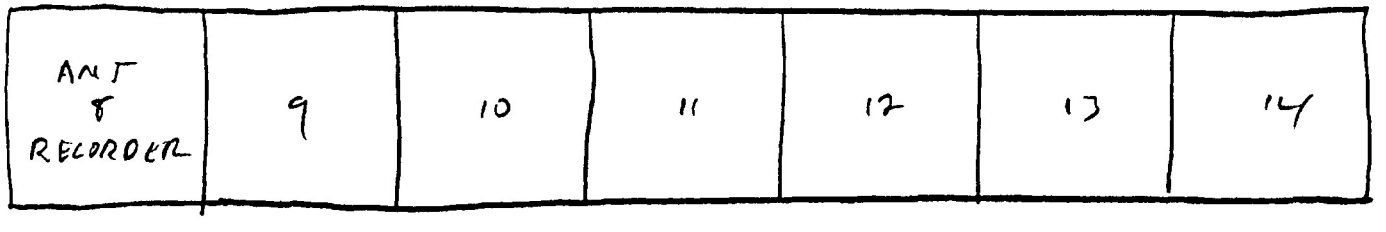
ANT
8
RECORDER
9
10
11
12
13
14

FIGURE 9