VLB ARRAY MEMO No. 110

Interoffice Memorandum
CALIFORNIA INSTITUTE OF TECHNOLOGY

To: R. Burns, VLBA Memo Series Date: 6 Aug 1982
From: Martin S. Ewing MSE Ext: 4970 Mail Code: 105-24
Subject: VLBA Overall Dataflow

In response to the Computer Group meeting yesterday, I offer the attached diagram. It shows one possible way of thinking about the processors and databases in the VLBA.

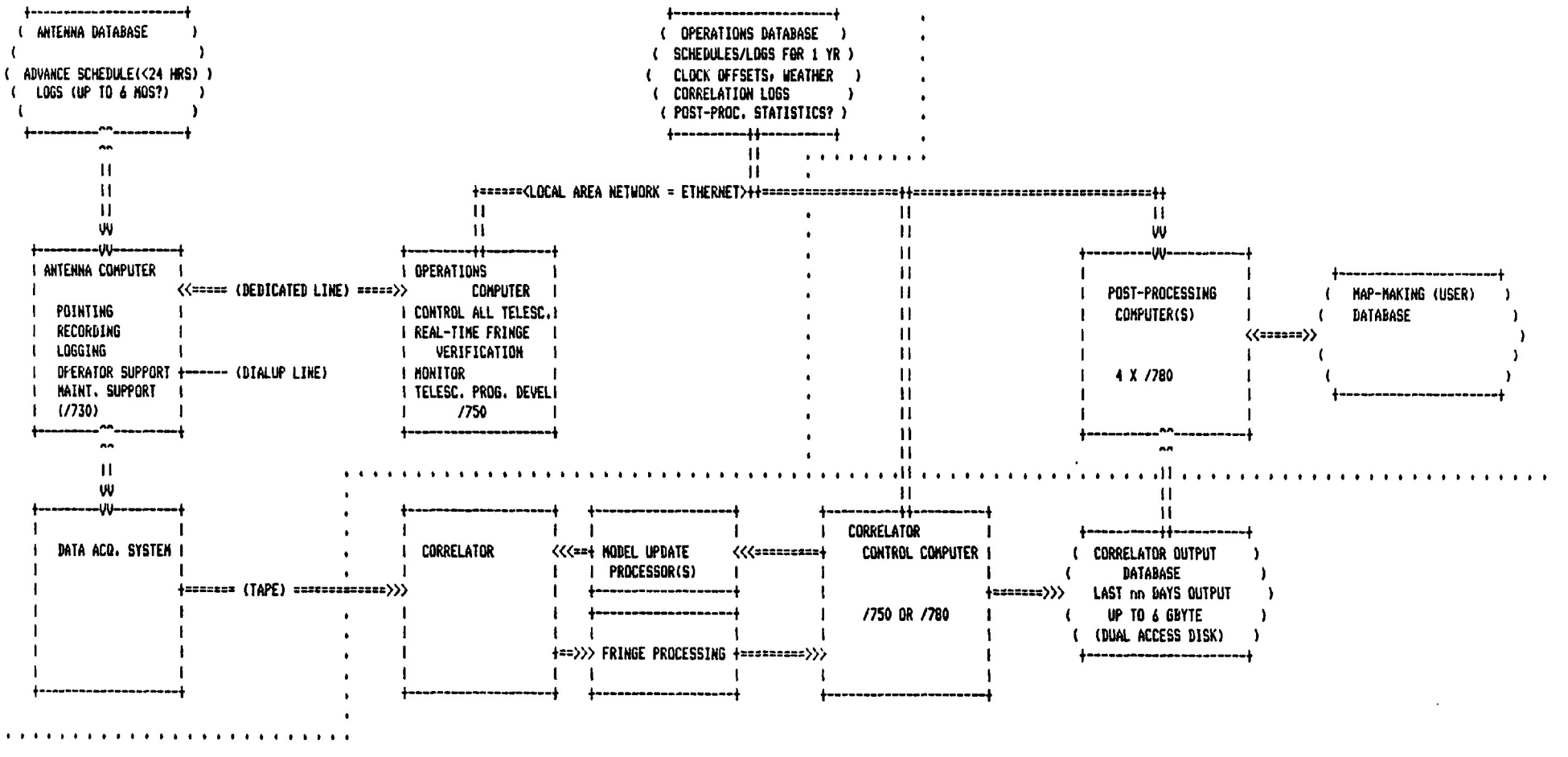
Notice that the figure is divided in three parts. Each section can operate independently of the others (for a while, at least). This may suggest a reasonable division in hardware and planning, too.

The computers are sized in terms of the DEC VAX family. Note that all major computers should be members of a compatible family to minimize networking, programming, and maintenance problems.

A /750-size CPU is needed in the Operations System to support real-time fringe checking. Excess capacity can be used for program development when fringe checking is not required.

The /730 at the antennas is just for sake of argument. Its compatibility with the 32-bit central computers is an attraction compared, for instance, to the PDP-11. Future pricing for low-end 32-bit machines will presumeably continue to approach that of the LSI-11/23 we have been proposing.

[UP TO 14 ANTENNAS INCLUDING PART-TIME STATIONS]



VLBA DATAFLOW DIAGRAM (MSE 8/82)