VLB ARRAY MEMO No. 117

VLSI FOR MULTI-LAG CROSS-CORRELATOR CIRCUIT
CROSS-CORRELATOR SLICE (CCS)

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DISTINCTIVE CHARACTERISTICS:

* 3-level 16-lag cross-correlation and integration slice

* Thirty-five 20-bit up/down integration counters

* Thirty-five 16-bit integration hold registers

* +1,0,-1 bit delay (vernier) for data & invalid, one stream

* 3-level phase mixing for one data stream

* Two 16-bit shift registers for data & invalid, one stream

* Hold register sequencing for data reading

* +5 volt power supply

* Advanced N-channel silicon gate MOS technology

* 16 Mhz data correlation bit-rate

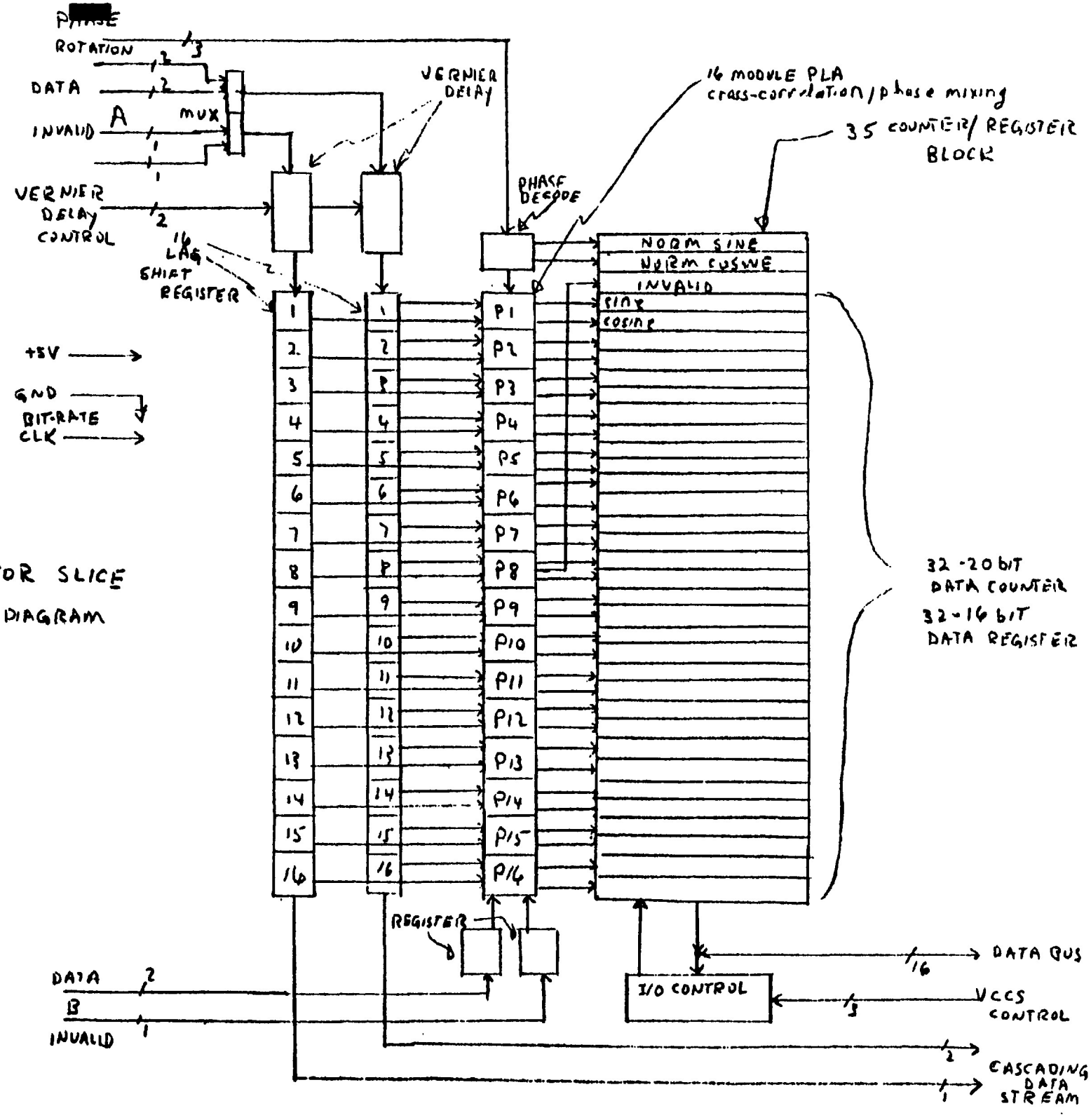
* 40 pin Hermetic DIP package

GENERAL DESCRIPTION:

The multi-lag Cross-Correlator Slice (CCS) is a VLSI circuit designed to service many types of correlation applications. It provides the capablity for +/- one bit delay, three-level phase mixing of one stream, lag delay for both data & invalid data streams, 3-level 16-lag complex cross-correlators, 20-bit integration for each lag and slice cascadable. A variety of programmable operating modes and control features allow the CCS to be personalized for particular applications as well as under program control.

The CCS includes thirty-five 20-bit up/down counters for cross-correlation integration and thirty-five 16-bit integration hold registers. Only the upper 16-bits of counters can be read by using the automatic sequencing function. Arm/disarm, save and clear commands, which drive the counters, are exchanged with the host controller over the 16 bidirectional data bus lines. The integration count may be read without disturbing the counting process. Count blanking may be made for each lag of the cross-correlator individually by the data invalid streams. Three additional counters, normalized sine/cosine and invalid, are then used for calculating the correct data integration counts.

The circuit is a complete 16-lag cross-correlator slice cascadable up to any number of lags. Any number of CCS's can be interconnected to form lags of 32, 48, 64 or more lags in 16-lag increments.



VLSI CROSS-CORRELATOR SLICE

GENERAL BLOCK DIAGRAM

COST BREAKDOWN OF THE VLSI CROSS-CORRELATOR SLICE

200 4in.-wafer @ $500.00/wafer = $100k & 20k chips

assume 25% usable chips => 5k chips

fab cost	100k
package cost $10.00/chip	50k
testing	50k
total	200k

$/chip = $40.00