VLB ARRAY MEMO No 118

JET PROPULSION LABORATORY

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TO: VLBA Proposal Group

FROM: John Peterson

SUBJECT: Application of a VLSI correlator chip

This design is based on a 16 MHz clock rate, recirculating correlator and uses VLSI correlator chips like those being designed at JPL.

Figure 1 is the block diagram for one baseline cross-correlator. This diagram shows a dynamic RAM dual-recirculator using 256k x 1 and VLSI cross-correlator/integration slice using 16 lags per slice. The recirculators are 2 mega-bits in size which will result in .1 sec or longer integration time. Data is then read out of the correlator chip on a 16-bit bus by automatic sequencing. The design is very simple and modular because a complete baseline correlator and integrator can be packaged on a card. A 14 station correlator would have 91 cards of the same type.

The recirculator can be programmed to the requirements of continuum and line observation as stated in the VLBA proposal, which are modes A,B,C,D & E.

The efficiency of a correlator design can be represented by its power consumption per multiplier megabit. That is, the "throughput power" of a correlator can be calculated as the number of multipliers times the bitrate in megabits per second (MMB).

PC=mW/MMB

The power consumption (PC) is not only a measure that specifies the operating cost of the correlator, it also sets its physical size, number of components and therefore its reliability.

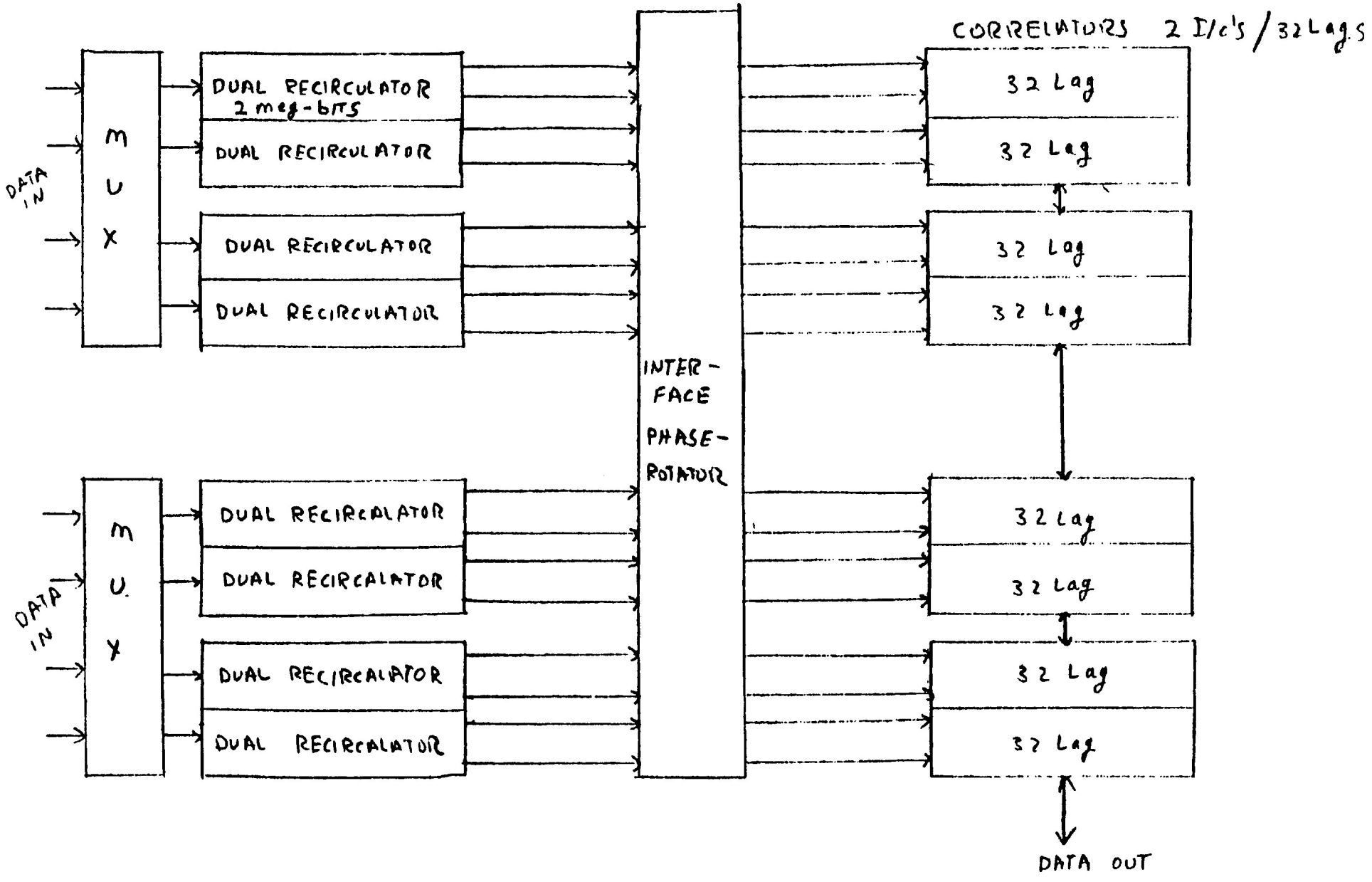
A comparision between the VLSI application to the VLBA correlator and the NRAO VLA correlator shows the VLSI application about twice as efficient, for 32 lags, as the NRAO VLA. For both systems no computer was included and both system produce a raw integrated correlation function. See page 4 for VLSI VLBA power consumption breakdown.

NRAO VLA:	20 mW/MMB
VLSI VLBA:	11 mW/MMB

A comparision was then made between adding more lags to the VLSI correlator and NRAO VLA type of correlator. This comparision is plotted on page 5. Mode A was selected because it gives the least number of lags per frequency band. The plot shows the efficiency of correlators from 16 lags to 1024 lags. The NRAO VLA correlator efficiency limit is about 17 mW/MMB. The VLSI correlator efficiency limit is about 2 mW/MMB or about 8.5 times more efficient.

Advantages in performance, cost, and density accrue in mapping an application directly onto silicon, optimized for the function required by the application. Pursuit of those improvements, like the comparisions shown above, will drive product designers to make silicon their design medium rather than support chips.

In conclusion, for any new correlator construction one should estimate the efficiency (PC) for different design and select the design with the lowest PC.



CORRELATOR BLOCK DIAGRAM (FIG. 1)

FIG. 1

VLSI VLBA Power Consumption Breakdown

I/C's per block (see fig. 1)

mux.....	4 I/C x	2 blocks =	8
recirculator & control.....	24 I/C x	8 blocks =	192
Interface/phase rot.....	50 I/C x	1 block =	50
VLSI corr. chip	2 I/C x	8 blocks =	16

TOTAL I/C per BASELINE			266 I/C's

14 stations = 91 cards @ 12" x 15" ea. (266 I/C's per card)

I/C total = 266 x 91 = 24.2k I/C's @ 8.5k watts

PC = mW/MM

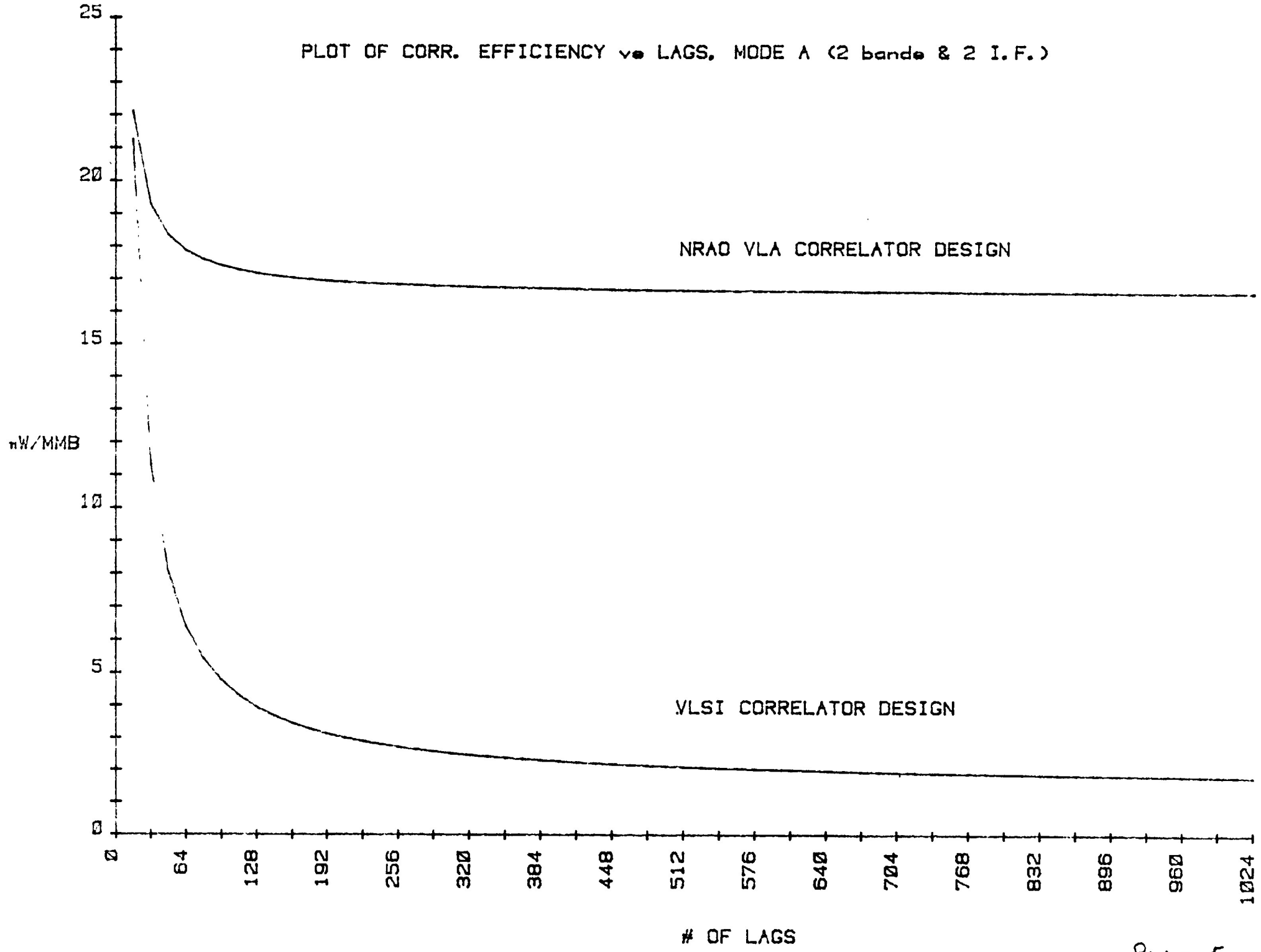
mW = 266 I/C's x .07 Amp x 5v x 1000 mWatts per Watts

mW = 93100

MMB = 2 mult x 256 lags x 16 meg Hz

MMB = 8192

PC = 11.36 mW/MMB


PLOT OF CORR. EFFICIENCY vs LAGS, MODE A (2 bands & 2 I.F.)
NRAO VLA CORRELATOR DESIGN
VLSI CORRELATOR DESIGN
nW/MMB
25
20
15
10
5
0
0
64
128
192
256
320
384
448
512
576
640
704
768
832
896
960
1024
OF LAGS