VLB ARRAY MEMO No. 121

To: VLBA Memo Series

From: B. G. Clark

Subj: VLBA Data System Block Diagram

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To date, nobody has circulated a block diagram with the level of detail in it that makes it pleasant for me to look at. I have therefore arogated that task in hopes that it might inspire somebody else to do a better job. That is, I have made several rather hopeless simplifications that I have no desire to remove. I have specified the interfaces between blocks to the extent that I am able (and have made arbitrary decisions on occasion there). Some of the interfaces I am completely unable to specify, and have marked on the diagram with a "?". These interfaces I would propose to assign to the group leader of the tape recorder system design group, and allow him maximum control and flexibility. This we can do because these interfaces do not interact strongly with the rest of the system.

The block diagram is predicated on the assumption that the tape recorder system will provide a 200 MBit/second data channel, and that logically, one enters and leaves the tape system with K bit streams, each with a data rate of 200 MBit/sec/K. This is shown in Figure 1. (The "telescope validity bits" would be results of local checking operations--say, one for "telescope off source", one for "LO chain unlocked", etc--and would change at a few times per second rate at most).

Figure 2 shows the reproduce half of the tape system. After considerable wishy-washying I have encluded the Delay Control as part of this system, rather than as part of the correlator system, as it seemed to make the interfaces easier to describe. Note that I have put in only one Delay Control per antenna--all bit streams must have the same delay tracking center. With bandwidths greater than about 2MHz it seems worthwhile to have a hardware delay extrapolator, whose design is essentially the same as that of the hardware phase extrapolator, except for the different data widths. The clock to update the delay should be the recirculator cycle, so that the fractional bit delays, which are used downstream, need not be recirculated. It is quite adequate for the computer to strobe in an initial delay and delay rate once per second.

The figure includes a large number of input lines from the computer. It seems unlikely that the best way to do this is simply by multi-conductor cable--some sort of serialization seems called for. Fortunately, specifying this is beyond the scope of a block diagram.

Not knowing how the fully integrated chips being designed at Cal Tech are intended to work, I have included Figure 4 as a device to indicate, conceptually, the functions that must be performed. I fully realize that, as drawn, it is not a very practical design for a chip--the inputs shown utilize 23 pins, and the diagram does not include the data readout function, which would take at least 3 more.

If we did want to use this sort of block diagram, which I will not defend, the number of pins could be cut down by sending some data in serially, eg the fractional delay, the validity bit, and the phase at the start of the recirculation cycle (this to be counted up or down). Then the pins become manageable--serial date antenna 1, serial data antenna 2, serial clock, data strobe, phase lsb antenna 1, phase lsb antenna 2, data antenna 1, data antenna 1, correlator clock, serial data output, output data clock, output chip select for a total of 12 pins, for instance.

The diagram is seriously incomplete in not showing the data readout/recirculation data summing. This can be a rather complicated mess, and appears to have rather critical data rates if the recirculators are made too small (100kBits looks more reasonable than the VLA's 10kBits). The diagram is also missing any discussion of the full 3-level capability. I think this should not be forgotten. One might hope that it could be selected by a "mode" pin on the correlator chip, and thus shuffle the problem off to the chip designer, but this might be a forlorn hope--we may also have to collect the two bits of the 3-level sample from different places. Incidentally, it is not out of the question to do everything with 3-level sampling. Five 3-level samples can be encoded onto 8 bits, which, for a given bit rate, gives about the same SNR as two level sampling.

I am sure I have done a number of things that various people will not like. I am not particularly anxious to defend them, and invite you to draw your own version. On the other hand, I think the level of detail is about the appropriate one for the current state of the discussions and even for setting the intergroup interface specifications.

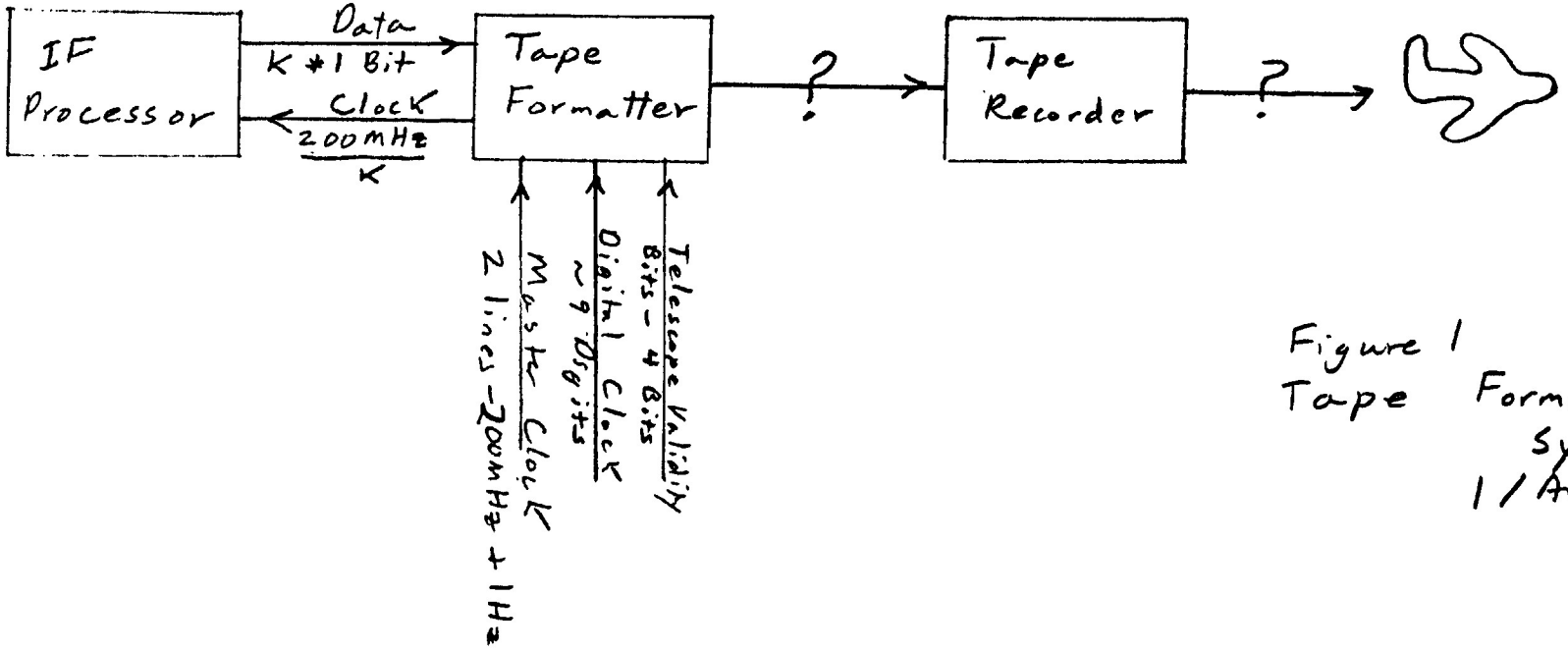

Figure 1
Tape Formatter/Recorder System
1/Antenna

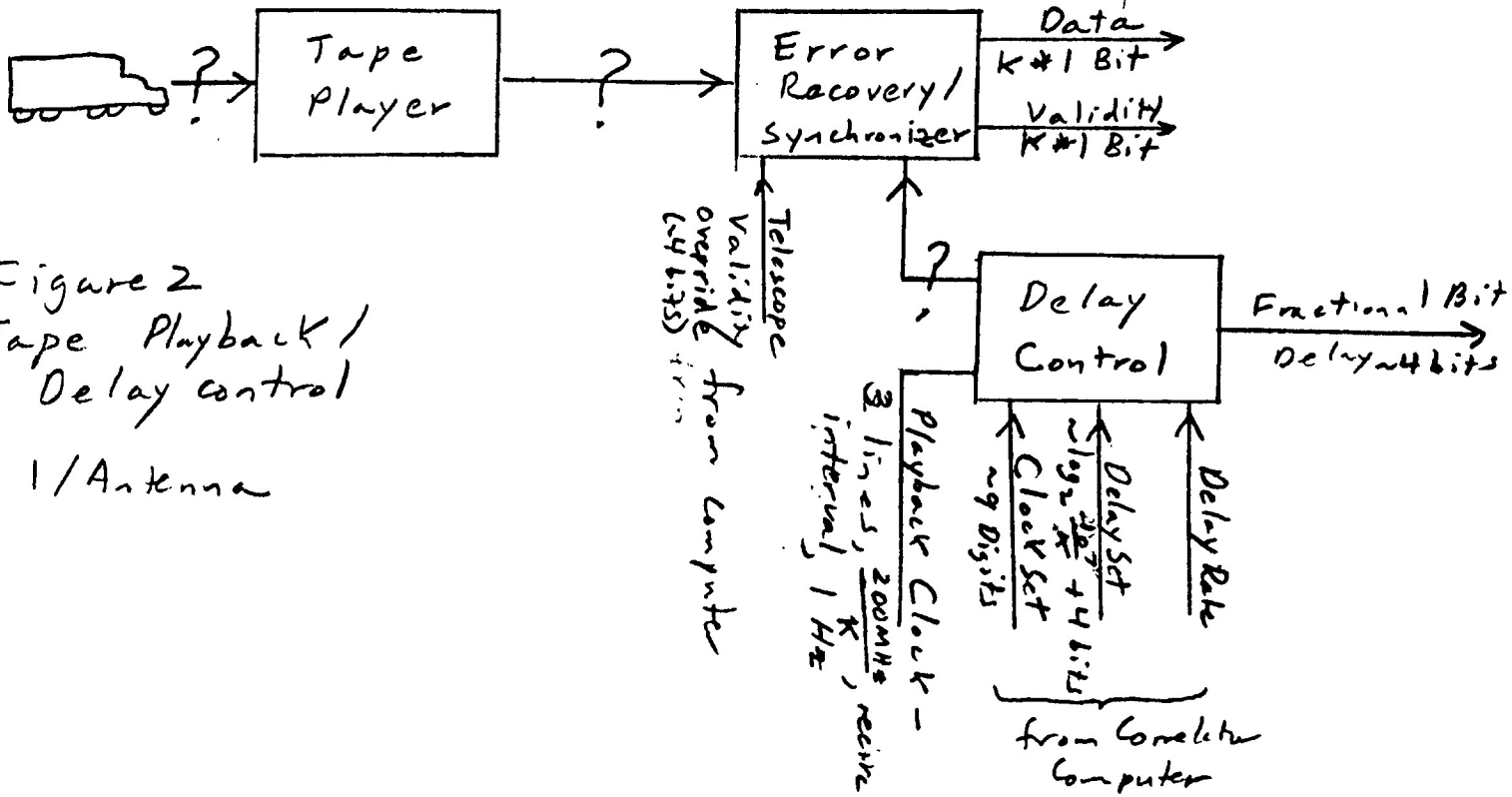

Figure 2
Tape Playback/ Delay control
1/Antenna

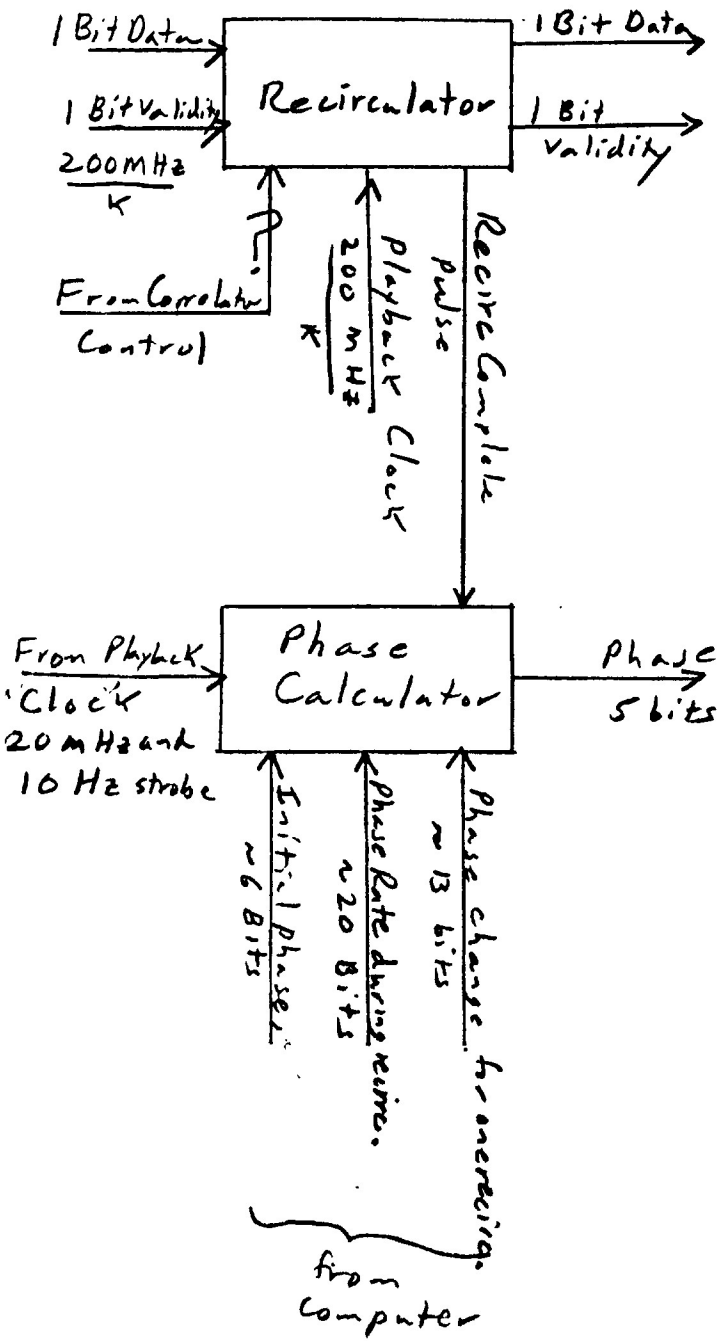

Figure 3
Recirculator / Phase Calculator
K per antenna

$\frac{200\ MHz}{200\ K}$ * recirc. factor / resampling factor

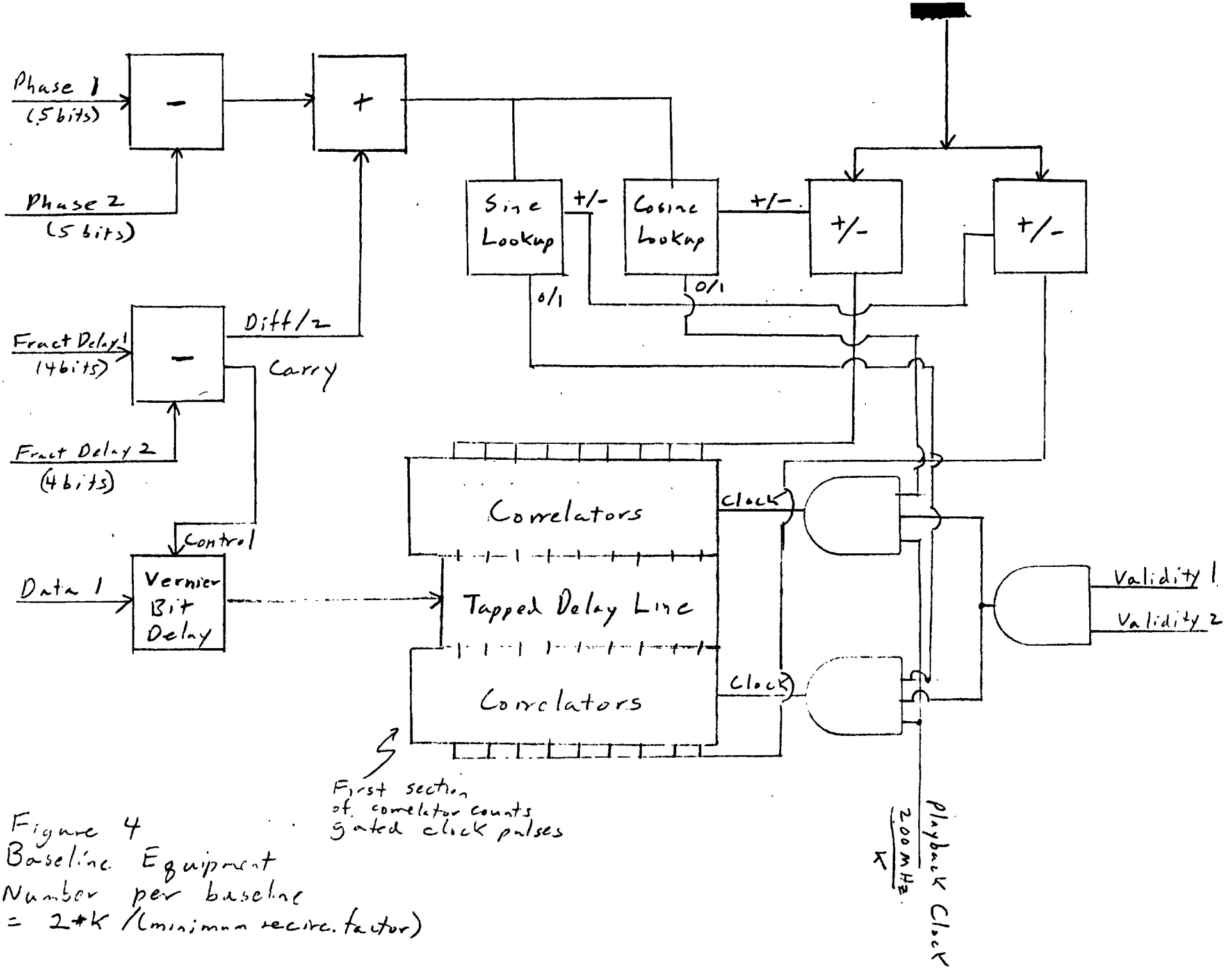

Figure 4
Baseline Equipment
Number per baseline
= 2*K / (minimum recirc. factor)