

VLB ARRAY MEMO No. 140

October 7, 1982

To: VLBA Recorder and Processor Groups
From: Haystack VLBI Group
Subject: Proposed Recorder Interface for VLBA

The following proposal is for the interface to/from the "black box" recording system. The structure of the recording machine and/or correlator are not specified.

#Channels to recorder: 32 (parallel independent)

#Channels from recorder: 32 data + 32 clock (parallel, independent,
undeskewed, unbuffered)
plus 2 independently-selectable channels (data + clock)

Bit rate/channel: 0.125, 0.250, 0.5, 1, 2, 4, 8, 16 Mbits/sec (unformatted)
Formatted data rate is 9/8 unformatted (18 Mbit/sec max).
All channels must operate at same data rate.

Data format: Same as present Mark III format except that a channel#
identifier will be added to the "auxilliary data" so that
both time and origin are specified.

Recorder control:

Recording:

Locking time: System shall be stabilized and recording usable
data within 3 seconds of the command to do so.

Read-while-write: Desirable, but not necessary.

Reproduce:

Locking time: System shall reproduce usable data within
1 sec after recorder speed arrives within $\pm 1\%$
of nominal speed.

Locking range: System shall maintain data lock over a speed
range of at least $\pm 1\%$ from nominal speed with
a minimum slew rate of 1%/sec.

Out-of-lock slew: Minimum out-of-lock slew rate shall be
twice the nominal playback speed, with a minimum
acceleration of 50% of nominal speed per second.

Drift: While reproducing within $\pm 1\%$ of nominal speed, bit
stream drift shall be no more than 10000 bits/sec
wrt externally supplied reference, and then be quickly
repositioned in increments of 10000 bits without loss
of data.

Jitter: Maximum clock jitter shall not exceed 5% of nominal
clock period.

Error-Rate: Worst-case error performance shall not exceed 1×10^{-3}

Control interface: IEEE-488 or RS-232

Electrical: All data and clock signals shall be ECL.

Control signals shall conform to IEEE-488 or RS-232 standards.

Interface organization: It is suggested that there be 3 independent connectors at the interface -

1. Acquisition system data interface -
32 data channels to recorder plus 2 selectable reproduce
2. Correlator system interface -
32 reproduce channels (data and clock for each)
3. Control interface.

Comments:

1. The maximum instantaneous bandwidth of the proposed system is 256 MHz.
2. The choice of the Mark III format, with only the slight modification indicated, was made after three years of experience with that format. No problems have been encountered or are anticipated with the data-replacement technique used by this format. Any aliasing due to the data-replacement is at a sufficiently high frequency (50 Hz min) as to be well outside normal fringe search ranges. Because the time code in the Mark III format has only millisecond resolution, the time tags for data rates exceeding 4 Mbits/sec will be truncated at the millisecond level. This leads to an unambiguous time tag provided the sample rate is known, and is the method currently used by Mark III at 8 Mbits/sec.
3. Note that, although the specification indicates 32 parallel reproduce channels, the electronics to support all of these would be needed only at the processor. Similarly, the record electronics are needed only in the acquisition system, although the recorder system should be able to support either or both by the simple addition of electronic modules.
4. The reproduce specification is for independent undeskewed channels. This requires that a separate clock signal line accompany each data line, but eliminates much electronics from the playback. Deskewing is most easily and logically implemented in the processor.
5. It is assumed that the correlator will have sufficient internal buffer space to accommodate the delay between any earth-based antennas. This allows for easy '4-antenna' experiment processing where data from widely-separated multiple sources may be on a single tape. This naturally leads to a minimum buffer space of approximately 256 Kbits and allows a fairly relaxed specification (10000 bits/sec) on reproduced-data drift rate.