VLB ARRAY MEMO No. 180

To: VLBA DESIGN GROUP 15 FEB., 1983
From: Martin Ewing
Subj: MINUTES OF CORRELATOR GROUP MEETING OF 15 FEB., 1983

Present: D. Fort, A. Rogers, A. Whitney, H. Hinteregger, H. Hvatum, K. Kellerman, C. Walker, B. Clark, A. Bridle, R. LaCasse, M. Ewing

PLAN B (joint US/Canada array) was discussed somewhat. Ewing's interest was to be sure that there were no features in the US proposal now being developed (PLAN A) that would be difficult to mesh with Canadian requirements, should PLAN B become a reality. Bridle and Fort saw none.

There is, however, some disagreement between the Canadian and US estimates for correlator and recording system costs. The Canadian estimate for a correlator (VLA-based) is higher ($Can 2 M+) and for data recording is lower than the corresponding US estimates. We could not immediately resolve the differences.

Discussion continued with Memo #176 (Ewing: VLSI-based correlator design). Walker noted that 32 msec delay coverage was generous for terrestrial baselines, but inadequate for space. This coverage was the smallest power of two that would satisfy terrestrial requirements, however. Walker also noted that the number of frequency channels was generous, MORE than spectroscopists had asked for! Ewing countered that the number of channels was not a "driver" for this design, but fell out from other considerations. A factor of two reduction is likely if the VLSI chip is reconfigured as a dual 8-channel device.

We could not leave alone the question of channelization! Supposedly we had settled on the "Rogers compromise" (up to 32 channels at up to 25 MHz bandwidth each), but this has some problems. One that was not resolved was the problem of filling up a defined aggregrate recording system bit capacity efficiently with a convenient number of channels. If the aggregate rate is 100 Mb/s, say, then 2 50 Mb/s channels fit well, but 6 16 Mb/s channels do not. The number 6 is awkward, and the 4 "left over" Mb/s might be inconvenient. Powers of 2 division down from 50 Mb/s would be more natural in this case.

Adopting Ewing's suggestion of 32 MHz (64 Mb/s) as the maximum, instead of 25 (50), just increases recording system cost. It may not affect correlator costs. His concern was utilizing the VLSI capacity most effectively. In a design like Memo #176, a basic correlator running at 16 Mb/s can make 32- or 64-Mb/s correlators in a "natural" way.

Kellerman appointed Clark, Rogers, and Ewing to resolve the whole channelization issue, and, closely coupled, the 2-/3-/4-level sampling issue.

An interesting prospect would be a "packet switching" correlator, in which a number of 16 Mb/s VLSI correlators act as "servers" processing data from the 32 "queues." This approach has a number of features in common with the recirculating systems. Ewing will consider further.