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VLB ARRAY MEMO No. 360

The NFRA New Generation VLBI Processor.

Progress Report on the Correlator Section, June 1984.

1. Introduction.

A year ago we described the general characteristics of a large bandwidth processor which would cater for ground-based VLBI observations in the decade 1990-2000 at centimetre and millimetre wavelengths, as well as at centimetre wavelengths with an orbiting element (QUASAT). In the intervening period, study of this concept has continued with particular attention being paid to the custom integrated circuits which would form the basis of the correlator. This is part of a larger study of four different correlator projects within the NFRA, all of which would be based on the same IC, but have different input switching matrices and internal connections to cater for their respective tasks. The other correlator projects under study are the replacement for the present WSRT digital line backend, a 1024 channel 1 GHz spectrometer for the UK/NL millimetre telescope, and 2 dimensional autocorrelator for speckle interferometry with the 4.2 m Herschel telescope on La Palma. In addition to the basic correlator chip, it is planned that a number of the "building blocks" of the correlators will be common e.g. custom IC's for the integrators; printed circuits for configuration selection, correlators, pre-integrators, integrators, and memory; and programmable controllers for these elements.

The advantages of this multi-pronged approach are that development costs are divided over the four projects (attractive in particular for the custom IC's), purchase of components can be combined with consequent reduction in costs, and development time can be minimised since the test facilities for all four projects are identical.

2. Features of the VLBI Correlator.

(i) General Remarks

The maximum load specified for the correlator is the simultaneous correlation of 1.024 GHz bandwidth mm VLBI data from 12 stations. The correlator will be built in modular form so that other combinations of

numbers of stations and bandwidths per station are possible, for example, 16 stations x 512 MHz or 20 stations x 256 MHz. The maximum unit of bandwidth in the correlator is taken to be 128 MHz on the assumption that future developments in recording technology will achieve this bandwidth per track. Initial operation may very likely be at low capacity with an overall bandwidth of 64 MHz per station conforming to the VLBA standard recording system. Since there is currently no research into recording technology in European VLBI circles, we are bound to accept the US standard at epoch 1988. The following generation of VLBI recorders should be investigated by a joint team from Europe, USA and Japan, and the EVN should be prepared to allocate resources to this project.

(ii) The correlator itself

The basic structure of the correlator consists of 8 sub-systems each responsible for the correlation of a maximum of 128 MHz bandwidth, and 8 post-correlation pre-processors for correction of the data before final integration (see Figure 1). The 8 sub-systems are each split into 4 correlator modules each capable of correlating 12 input signals of up to 32 MHz in bandwidth. The correlator modules are designed around a custom chip which can accomodate 1x1 bit, $1\frac{1}{2}x1\frac{1}{2}$ bit, and 2x2 bit correlation schemes. A feasibility study carried out within the NFRA indicates that a correlator chip with a capacity of 0.5 or 1 giga word operations/sec (32 or 64 MHz clock, 2x2 bit, 16 lags) can be produced with currently available technology and at a competitive cost. An alternative chip could be that designed for the Australia Telescope correlator (8 bits x 8 lags x 5 MHz), but use of this chip would entail a complicated switching matrix to change configuration. A greater number of the AT chips would be required to provide the processing power specified.

The total number of signal streams which can be correlated simultaneously is 32 for 12 stations, 16 for 16 stations, and 16 for 20 stations. The total bandwidth cannot exceed 1.024 GHz, but note that smaller bandwidth input signals can be provided for by reducing the clock rate of the correlator chip. As an example of the flexibility of the correlator, it would be possible to simultaneously correlate a maximum of 12 stations recording with the MkIII system in mode A (28 tracks or signal streams) by running the correlator at 1/16 speed. It is not a question of bandwidth restricting MkIII correlation for more than 12 stations, but the number of available inputs. A greater number of stations could be correlated for MkIII/mode B (14 tracks) or by recirculating the data.

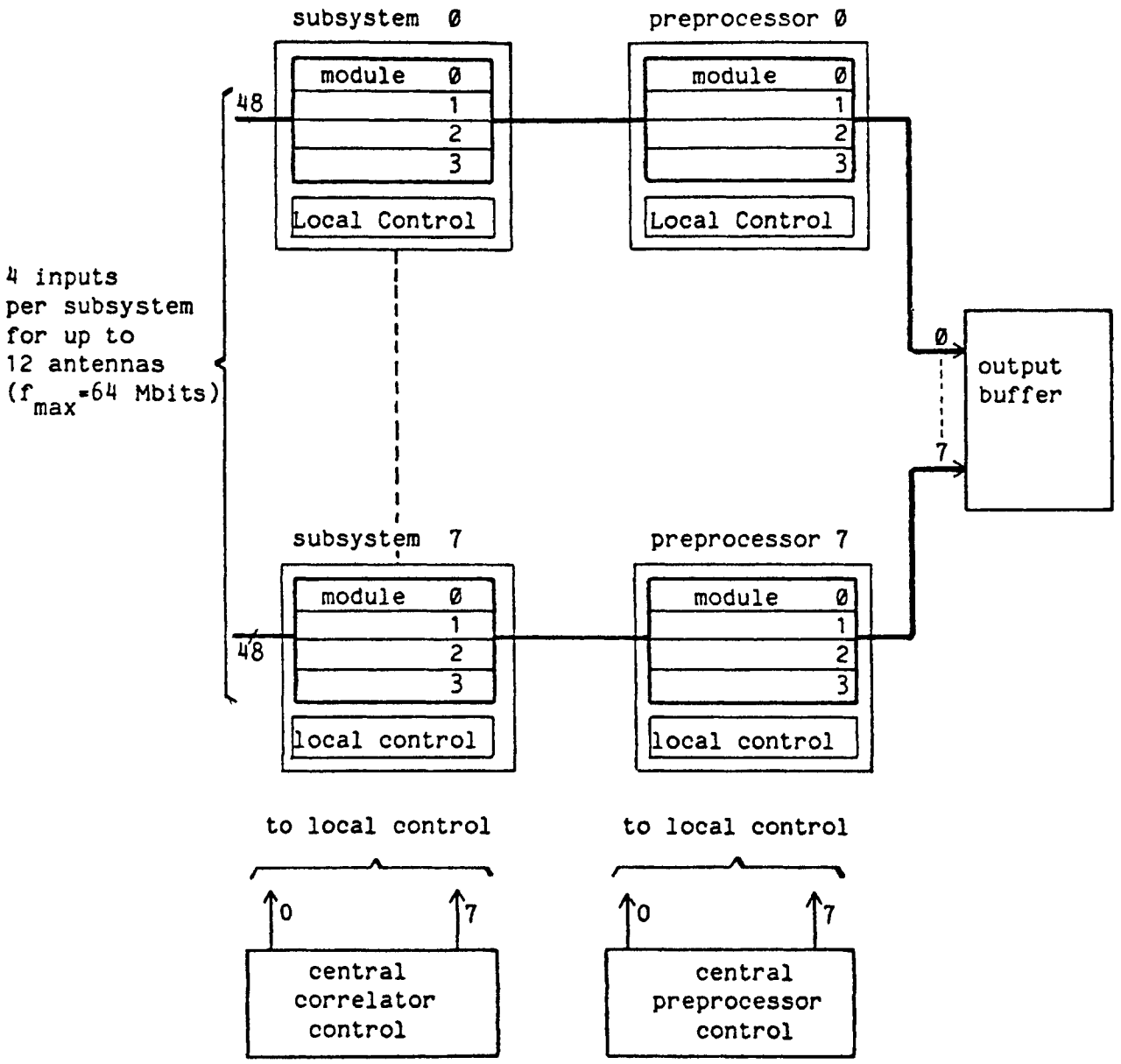


Figure 1. Blockdiagram of Westerbork VLBI correlator.

(iii) Spectral line capacity

The spectral line capacity of the correlator is given in the table below.

Bandwidth per station (MHz)	No.of complex freq.chan. per interferometer	Spectral resolution per channel (kHz)
8x128	128	8000
4x128	128	4000
2x128	128	2000
128	128	1000
64	256	250
32	512	62.5
16	512	31.25
8	512	15.6
4	512	7.8
2	512	3.9
1	512	2.0
etc.		

The maximum number of physical channels = 66 baselines x 32 correlator modules x 32 complex lags per module = 135168.

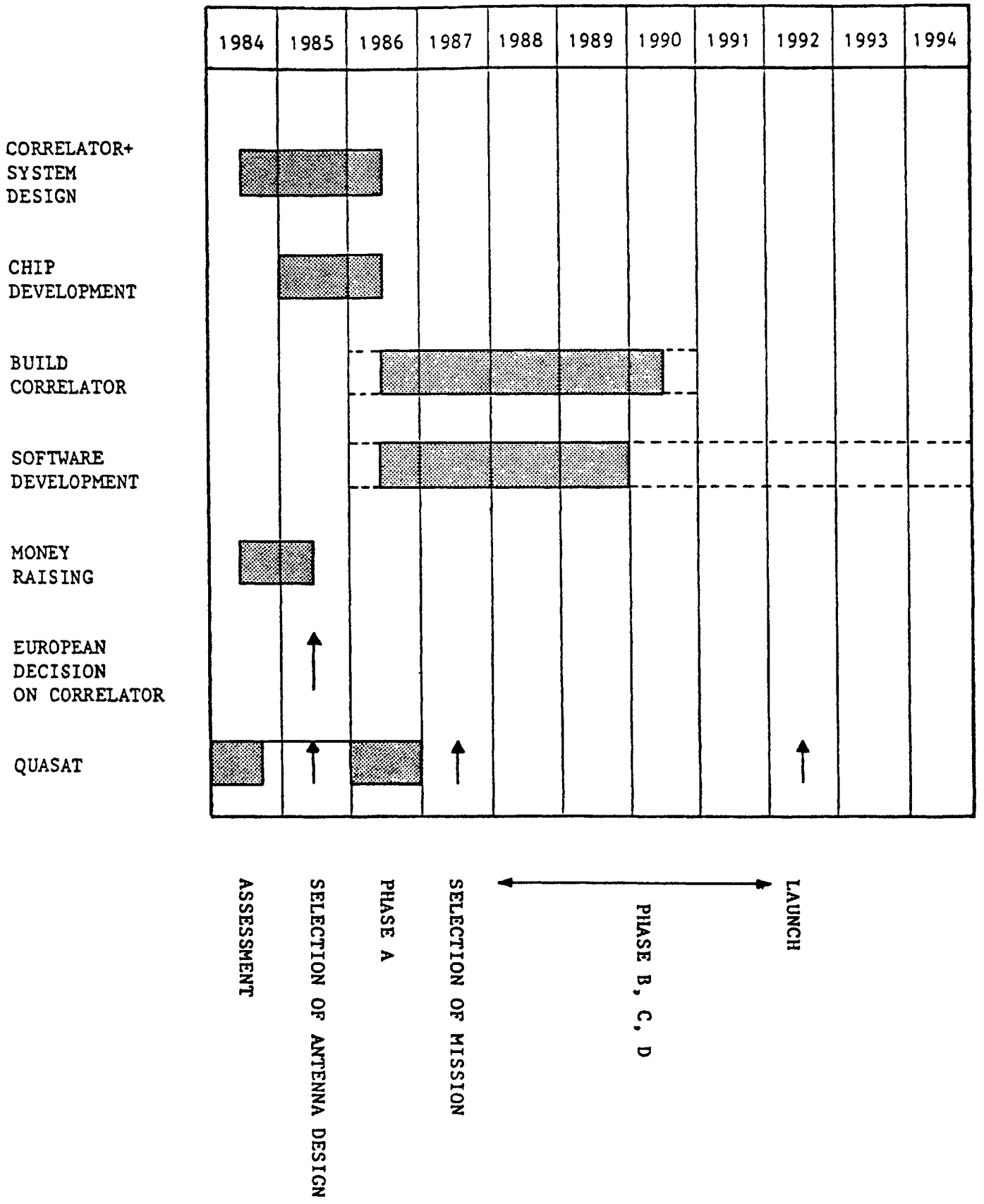
(iv) The post-correlation pre-processors

After correlation, the (maximum) 66 data streams per correlator module, proceed to the pre-processing modules where the following tasks are carried out, (see section 3.7 of NFRA ITR 165 "On the Use of Westerbork facilities for a VLBI Network Centre").

1) data compression - a Fourier transformation to 16 frequency points per baseline is carried out every 30 msec; integration to longer timescales then occurs per frequency point.

2) application of pre-determined phase corrections for residual fringe stopping, interferometer offsets, van Vleck corrections etc. every 30 msec.

VLBI CORRELATOR



Another potentially important use of this hardware is in a pipe-lined system allowing parallel processing of different field centres, particularly in the case where fringe and delay stopping are carried out at the interferometer elements themselves (see NFRA ITR 165 and VLBA Memos 326, 345 and 349). The pre-processors will have capacity for residual fringe rotation sufficient to ensure multiple fields of view. Antenna based fringe rotation reduces the required correlator capacity by a factor of 2; the reduction in cost will be less because of a considerable fixed overhead.

3. Development Scheme.

The following action is required in order to have an operational correlator in 1990.

1) Definition, building and testing of a custom designed chip set.

2) Realisation of the custom IC's by a manufacturer plus development of standard building blocks.

3) Development and testing of a small prototype of the basic correlator and final system design.

4) Construction of the correlator system and design of the signal processing.

5) Construction, system integration and testing.

Other segments of the processor such as the on-line and off-line software, fringe rotation and delay tracking systems, recorder systems, and computing requirements, will need to move ahead on similar time lines if the processor is to be operational in 1990.

Figure 2 is a bar-chart showing the major milestones.

4. Cost estimates for the processor.

The global estimate of the cost remains 15 Mfl ($ 5M), but we have increased the budget for recording systems and reduced the contingency.

Hardware

Correlator:		
custom chips (including development)	2	Mfl
boards, power supplies, cabling, control section, housing, cooling, etc.	1	"
post-correlation pre-processors	0.5	"
recording systems for 16 stations	8	"
Manpower	2	" (20 MY ($700K))
Contingency	1.5	"
Total	15	Mfl

A more detailed analysis will be carried out the beginning of 1985. Note that an antenna-based fringe rotation and delay tracking system would halve the size of the correlator, but save only 1 Mfl of the 3 Mfl budgetted for the correlator.