VLB ARRAY MEMO No. 393

Interoffice Memorandum

CALIFORNIA INSTITUTE OF TECHNOLOGY

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From: Martin S. Ewing Extension: 4970 Mail Code: 105-24

Subject: DPS/Correlator Interface Meeting 9/27/84

In conjunction with NASA Crustal Dynamics meetings in Pasadena, a meeting was held among Haystack, NRAO, and Caltech personnel on Sept. 27 to discuss the interface between the VLBA Data Playback System (DPS) to be delivered by Haystack and the VLBA Correlator to be delivered by Caltech.

Attendees: B. F. Burke, L. D'Addario, M. S. Ewing, D. N. Fort, H. Hinteregger, S. F. Kator, A. T. Moffet, T. J. Pearson, B. Rayhrer, A. C. S. Readhead, A. E. E. Rogers, R. C. Walker, J. Webber, A. R. Whitney.

Alan Rogers began with a summary presentation of the Haystack view of the Acquisition System, which was largely the same as the writeup available in "Blue Book" form of the Project Book. There will be 16 video converters (with independent LOs), each of which will generate a USB and LSB pair. All 32 IF channels will be digitized and will be available for recording.

We noted that this could be a case of exceeding the "basic" VLBA requirements; perhaps the second 16 channels should be considered a "positive option." Compared to a 16-channel system, a 32-channel system has better potential for (1) recording more bandwidth, (2) handling dispersed pulsar signals at narrower bands, and (3) evading RFI.

Bandwidths (sampling rates) from 8 (16) Mhz down to 62.5 (125) kHz are provided in powers of two. An external sample rate and IF filter are also included. Channels are sampled with 1- or 2-bit resolution. Restriction: All channels must be sampled at the same rate and with the same quantization.

[Ewing pointed out that in the current correlator perspective, bandwidth (sample rate) and quantization are separated. That is, the correlator accepts a certain number of samples per second regardless of 1- or 2-bit quantization. For 1-bit operation, the low-order bit is ignored. If tape consumption is not a strong limitation in the VLBA, 2-bit sampling would be the normal mode, since there is no loss of bandwidth.]

The Acquisition System is planned to use 32 tape tracks to hold the 2-bit samples of 16 channels or the 1-bit samples of 32 channels. In this sense there will still be a tradeoff between

number of channels and quantisation. Of course, the correlator (as now conceived) will accept only 16 channels at once.

On the subject of variable phase sampling (VPS): Jim Levine and Ray Escoffier are studying the benefits and impact of using this scheme (as found, e.g., at the VLA) in the VLBA. What would the cost be?

What is the "logical" impact of VPS? The station computer must accurately calculate source geometry and know UTC. The model used by the computer must be available to the correlator to apply phase corrections.

[Note: the VLA does this "open loop". The correlator assumes that VPS perfectly adjusts delay so that no phase corrections are necessary. This seems very worrisome to geodetic-oriented VLBI people. Does this limit VLA dynamic range? One sixteenth of a bit in delay is quite a lot of phase.]

Two ways were suggested to communicate VPS phase to the DPS and correlator. One would be simply to rely on precise replication of the antenna delay algorithms at the DPS and to be sure that the same parameters were used. Another would be to increase the precision of the tape time tags (by 4 bits) to resolve the steps of the VPS.

If the high-resolution time tag were used, the correlator control computer could simply present its "requested time" to the DPS in the same high resolution. No further interface complication would result in principle. However, in practice the DPS would have to communicate the delay error back to the correlator. The error could be larger than 1/16 bit if the station in question has no VPS (e.g., is a Mark III station) or if the VPS at the antenna somehow were tracking incorrectly. (This could happen if you were tracking a point away from the delay center.)

Since foreign antennas without VPS must be includable in the VLBA, the full fractional bit shift correction must be available in the correlator. Giving VPS to VLBA stations will increase the number of special cases that software must allow for. There will be 3 classes of baselines if some stations have VPS and others do not. Could there be closure problems?

The sense of the meeting seemed to be that VPS adds complexity to the Array, especially at the antennas, without a clear scientific benefit. The benefit of VPS is a potential gain of 3.5% in sensitivity for continuum, although the improvement is higher at the band edges in spectral line mode.

Next the meeting turned to phase calibration. There are various marginal reasons to prefer having the phase cal tones detected upstream from the correlator: Phase cal is a property of the antennas and can serve as a diagnostic in real time; Phase cal is more easily detected before the delay correction; and it is useful to know the phase cal results from the observing log

file before correlation begins. However, it appears that the correlator is still required to handle data from foreign antennas without record-time phase cal detectors and so the phase cal hardware must be provided. The phase cal hardware is comparable in complexity to a lobe rotator, but there are many fewer phase cal detectors (antenna-like) than lobe rotators (baseline-like). We will continue to plan for phase cal detectors in the correlator.

Is there a need to gather more station statistics in the phase-cal/autocorrelator modules? Rogers (Acquisition Memo 23) suggests using the correlator to measure sampling threshold biases instead of having phase switching at the antenna. This is fairly easy to implement in the correlator, but there was no clear consensus on whether this would obviate the need for phase switching.

The discussion moved on to the DPS Interface, specifically, Timing. Rogers continued to present his Acquisition Memos 19 and 20. The fundamental clock signal is 16 MHz, supplied by the correlator. This signal will run some kind of clock or counter in the DPS. This clock will be synchronized with the correlator clock by means of a time sync pulse, 1 pps in the Haystack memos. Some of the group felt that 0.1 pps would be easier for the control computer to identify without ambiguity; this rate is compatible with Haystack's thinking.

It is important to note that the 0.1 pps signal is used only for synchronizing clocks (much the same as VLBI formatter clocks are conventionally synchronized). Events in the DPS can be scheduled to occur at any bit number (in principle). Realistically, some convenient computer interrupt rate will define the times at which DPS activities occur. (This rate might be chosen in the range 10 - 500 Hz, I guess. -- MSE)

Benno injected his thought that a more efficient or logical approach would be for the DPS not to know anything about time (wall-clock or tape-) except to send the tape-time upstream to the correlator control computer (CC), as in Block II. The CC then would "close the loop" by comparing the tape-time with its desired time, and send correction (delta-t) commands down to the DPS. (Correlator Memo VC029)

The group responded with the general feeling that the CC should not be asked to close the loop for 20+ DPS units; that would be a CPU and communications burden. In general it should be sufficient to specify the desired bit to appear at a specific (mutual) clock time, and allow the DPS computer to perform the servo function. Of course, the DPS and CC must be coordinated so that the CC will always ask for a reasonable sync time. (Don't ask for a bit that appears on an unloaded tape, for instance.) Also, the CC must poll the DPS units regularly to see if the DPS has lost sync or encountered some other exceptional condition. Polling would have low time resolution. The DPS would rely on the 16 MHz validity bit stream to specify the correctness of

output data on a bit-by-bit basis.

[Note: We realized in this discussion that we will need some elaborate tape management functions, along with software to generate correlator control blocks. Some or all of this will be supplied by the Monitor & Control Group, we think. This interface is not yet specified, however.]

Now what about the Signal Interface? Haystack envisions the output clock rate being 16 Mb/s at all time. There is a natural bias with the longitudinal recorders always to play back at full speed. If widely varying playback rates are to be handled, extra equalizers are required. On the other hand, the correlator's fringe tracking burden is increased in proportion to whatever playback speedup factor is used. This argues for slower playback for narrowband experiments. (Without recirculation, however, the correlator cannot trade off frequency resolution for bandwidth.)

The VLBA must allow sampling rates down to 4 Ms/s for Mark III compatibility and to 125 kHz for spectral line work. In spectral line work, 4x oversampling would normally be used, however, bringing the sample rate up to 500 kHz for 62.5 kHz bandwidth. A separate sample clock can be provided by the DPS to the correlator, but this is probably redundant, since the information may be conveyed implicitly through the correlator setup blocks and DPS timing. The interface specification needs to be clarified on output sample rates and clock rates.

Benno raised the issue of whether ECL balanced line drivers and receivers were desirable, with their low voltage swings. He notes that Block II has had trouble even with TTL receivers that have much better common-mode rejection. The problems usually lie with ground loops.

Ewing added that the correlator group is considering high-speed multiplex transmission of antenna data streams through the correlator. Perhaps it would be sensible to have one engineering group responsible for both sending and receiving. If the correlator group did this, we would ask for space in the DPS rack for the line driver box. In this case the DPS-to-correlator electrical interface would only have cables a few feet long inside a single rack.

D'Addario points out that electrical interfaces (ECL/TTL) and particularly specific cabling and connector choices are probably premature now. First we should pin down logical interfaces.

Rogers continued. Rather general switching in the DPS would allow any output channel to originate from any IF channel with independently programmable delays (within limits). There are 32 IF "channels" from the video converters and 16 correlator input channels, but in fact 32 1-bit channels may be available on tape if desired. We need a more detailed specification of switching options.

DPS deskewing RAM will probably allow a +/- 32K bit electronic delay, says Whitney. The purpose of such a large delay is to promote fast tape synchronization. It also allows staggered delays on several output channels per IF channel, allowing a natural means of achieving high frequency resolution in spectroscopic modes. Memory is cheap, anyway.

Larry reminded us that the Monitor & Control Bus (MCB) can be used for the DPS interface, but that is not what it was invented for. It does not directly provide an ASCII communications channel, as we might wish. Rather, it transmits 16-bit data to and from a 64 KW address space, with devices mapped into blocks of the address space. There is no global command option (send same command to all devices), although this might be implemented. There are problems since each device is supposed to acknowledge all transfers addressed to it.

DPS units might use the MCB, since the Data Acquisition Systems will have to do so at the antennas. However, standard RS-232 ASCII lines to the control computer would be quite feasible also. The latter would be attractive in that the computer could address DPS units in parallel, and a certain amount of reliability would be added through redundancy. Also, the simple serial lines are easily interfaced to normal CRT terminals for checkout.

Haystack is considering a computer similar to an IBM XT (AT?) to control each DPS. Walker notes that if the DPS computer is lifted out of the "dumb controller" class, it becomes a candidate for regulation by the Computer Advisory Committee, which is seeking to hold down the number of computer types and to be sure that VLBA computer systems are generally maintainable.

Weary but not downtrodden, the contestants retreated from the field of honor to fight again another day.